SEU TESTS OF THE GWT SERIALIER

Test-beam at Louvain-la-Neuve and more

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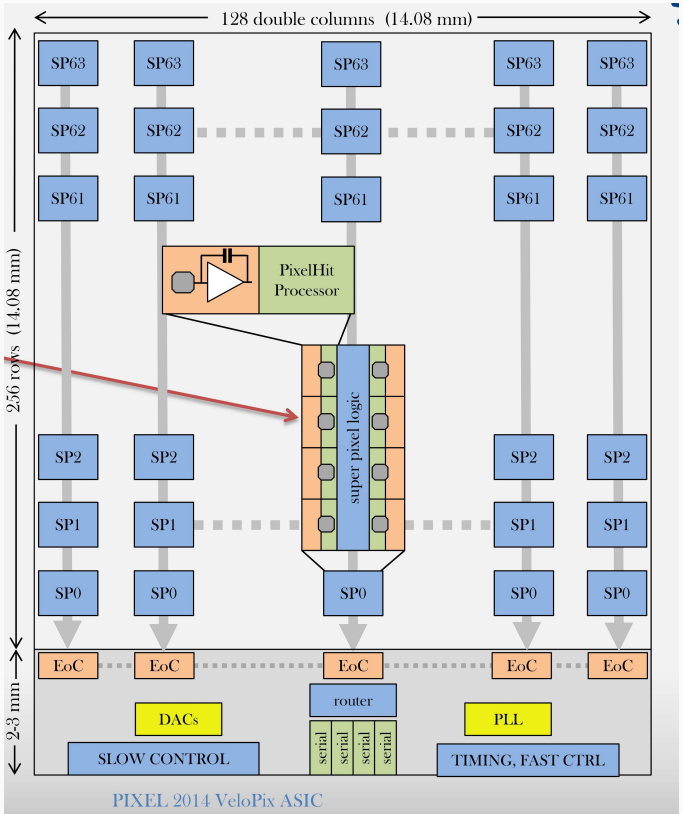
INTRODUCTION



Velo Pix

- Binary information gathered in 4x2 SP.
- Hitmap+BCID+SP_ID is propagated downwards.
- Data is send outside through the serializers.

GBT

- Developed at CERN to be used by everybody.
- Variable header length and data length.

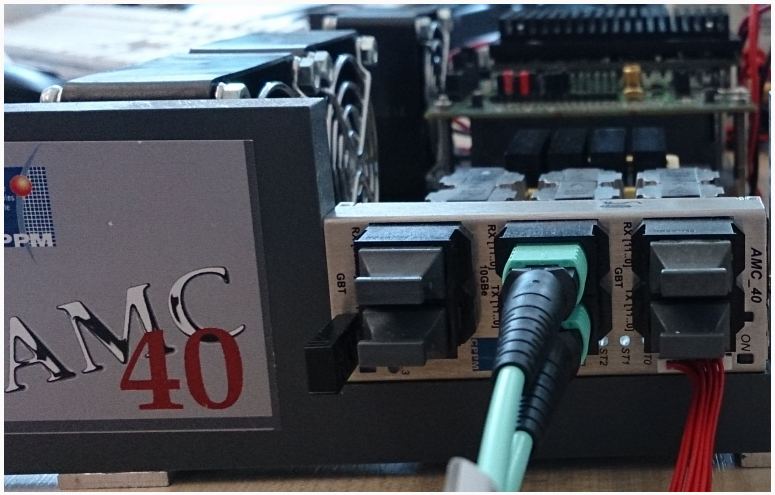
Gigabit Wireline Transceiver (GWT)

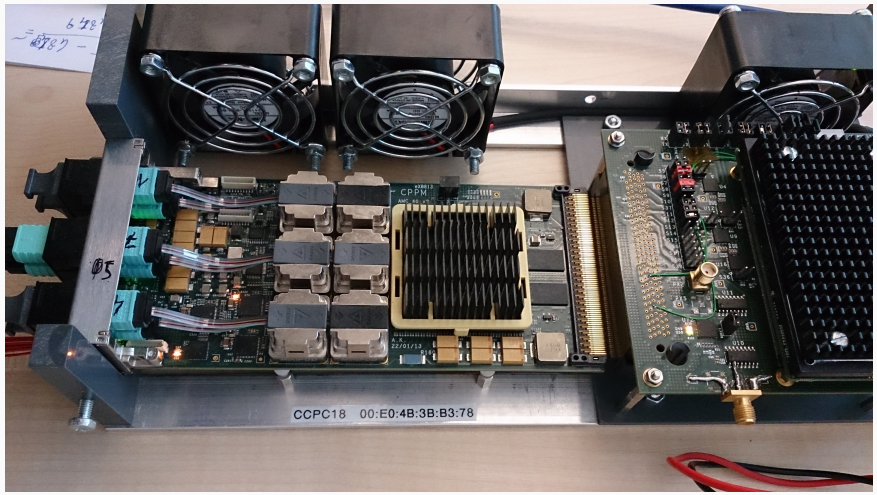
- Fixed header, data lenght to 128 bits.
- Slightly faster than GBT (5.12 *vs* 4.8 Gbps).
- Main advantage: lower power consumption.

Decided to use GWT in the VeloPix and GBT in for ECS (GBTx).

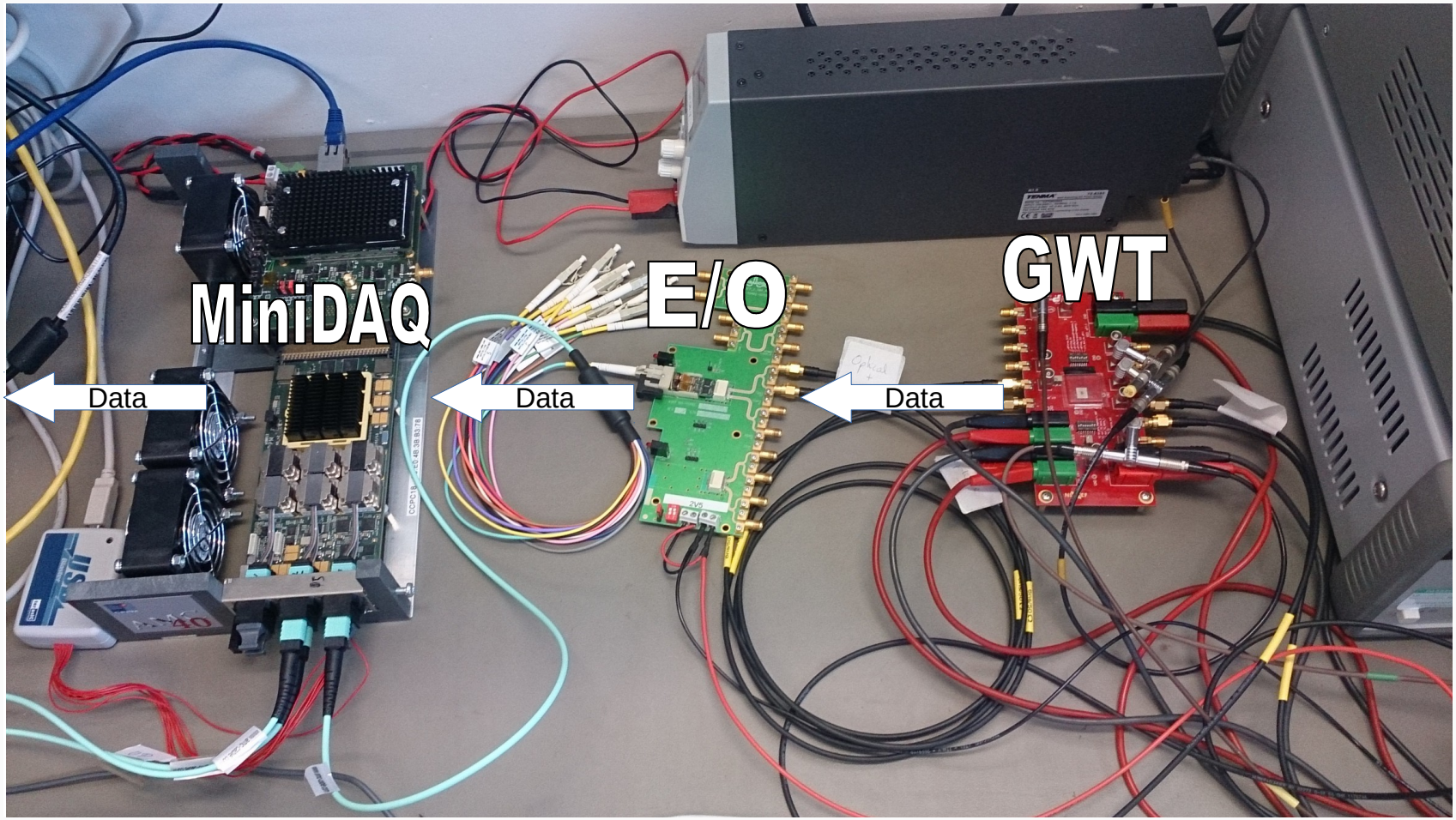
MiniDAQ

- DAQ prototype (AMC40). 6 FE links @ 5.12 Gbps.
- Output: 10 GBE link.
- Readout firmware is being developled for GBT.
- Some key components has to be adapted/re-writed.
- Performs: header-lock and data processing.





THE MINIDAQ DATA PATH



MiniDAQ data path.

The GWT board

a) Switch=00 : 010101 pattern at 5 Gbps
b) Switch=01 : FFFF0000 at 5 Gbps. Equivalent to 0101 at 320 MHz.
c) Switch=10 : PRBS at 5 Gbps. 16 bits “random” sequence.
d) Switch=11 : GWT pattern. 128 bits with header, scrambling, parity, BCID and SuperPixel hitmap.

Electrical-Optical converter

- Uses a VTTx/VTRx chip developed at CERN (EDMS: 1140665/1)

The MiniDAQ

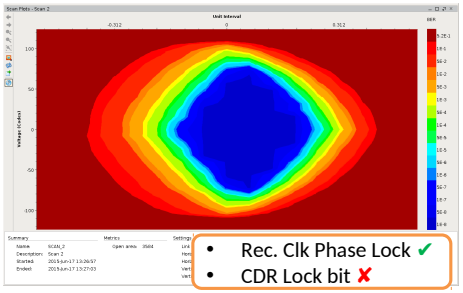
- Recovers the clock, locks the header, reconstruct the 128 b frame, process the data, generates UDP packets, sends data via 10 GbE optical link.

Test-beam purposes:

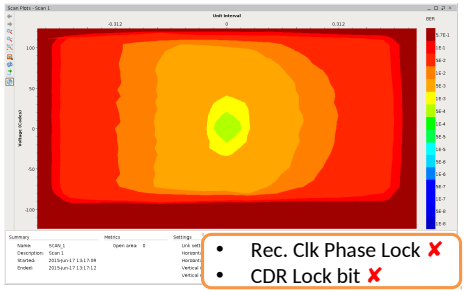
- How many data is loss by a SEU?
- How robust is the PLL to ionizing particles?
- Does GWT serializer is good enough?
- Does the MiniDAQ loss the header lock?

Eye diagrams of Gwt patterns (with PLL)

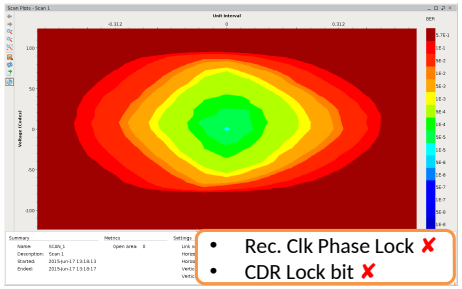
AAAA pattern



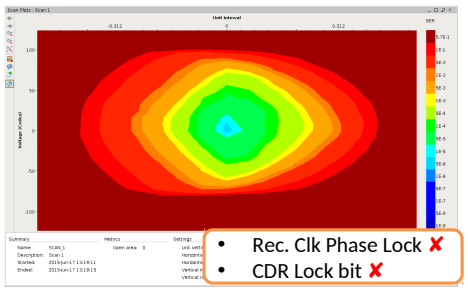
FF00 pattern



PBRS^16 pattern



scrambled pattern



FIRST TEST-BEAM

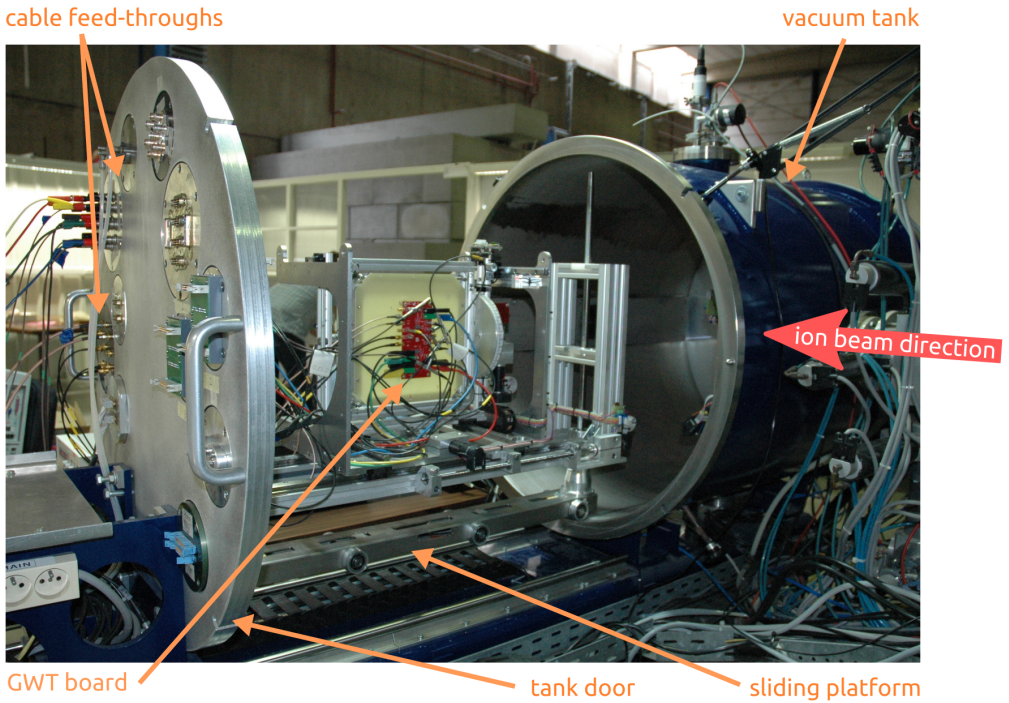
TEST BEAM @ LOUVAIN LA NEUVE (14/12/2014)

Beam

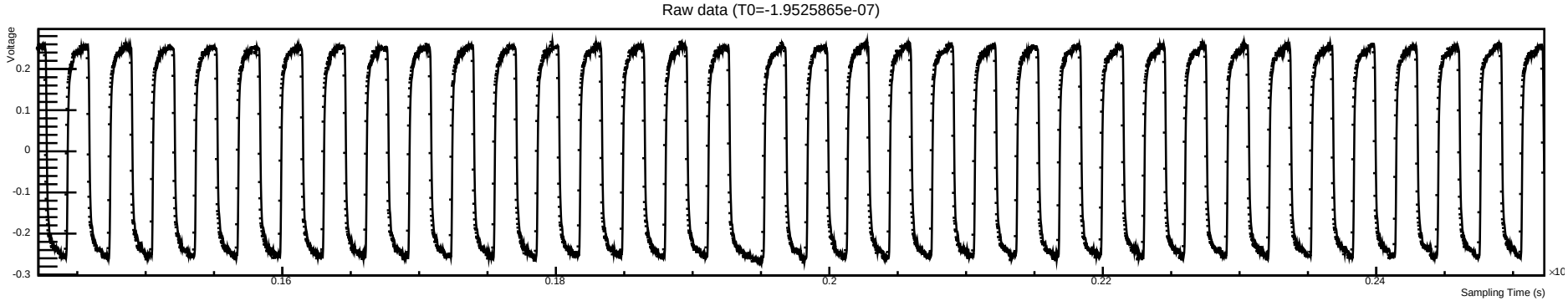
- Heavy ions $\rightarrow$ heavy ionization.
- Kripton-756, Niquel-567, Argon-372.
- 0^o and 30^o.

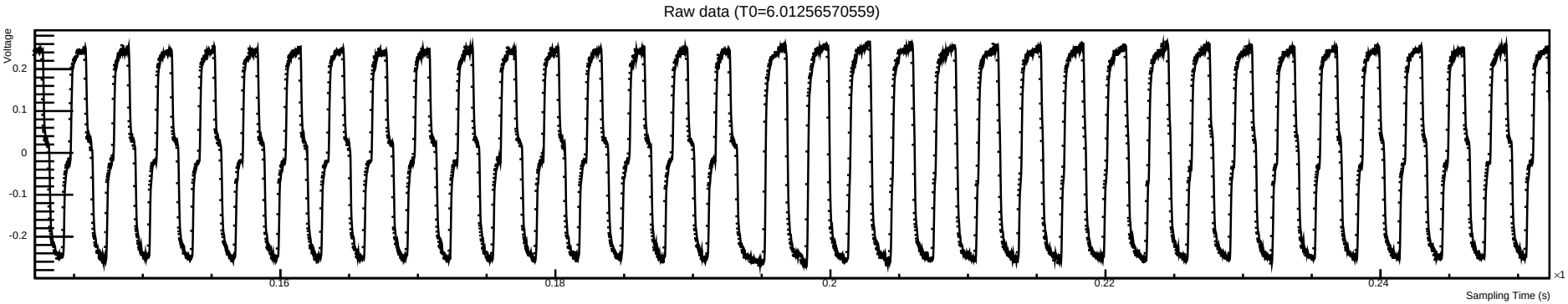
DAQ

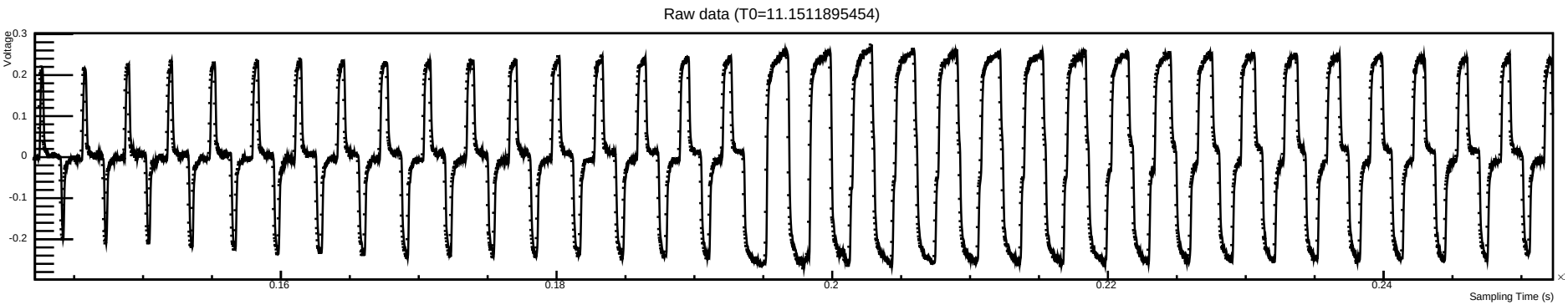
- Agilent DSO91204A 12GHz.
- Data: PLL clock monitoring. Differential.
- Signal: 320 MHz clock.
- Trigger: pulse width $>$ 1.56 ns.



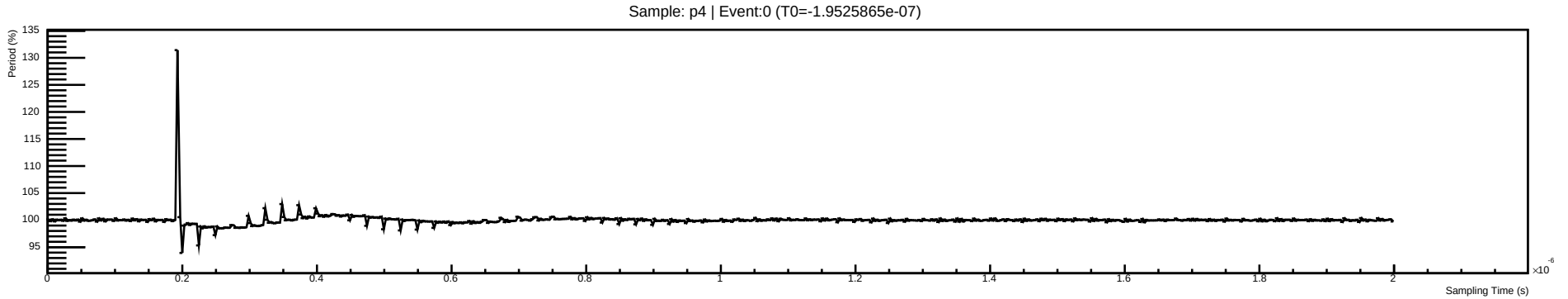
RAW DATA EXAMPLES

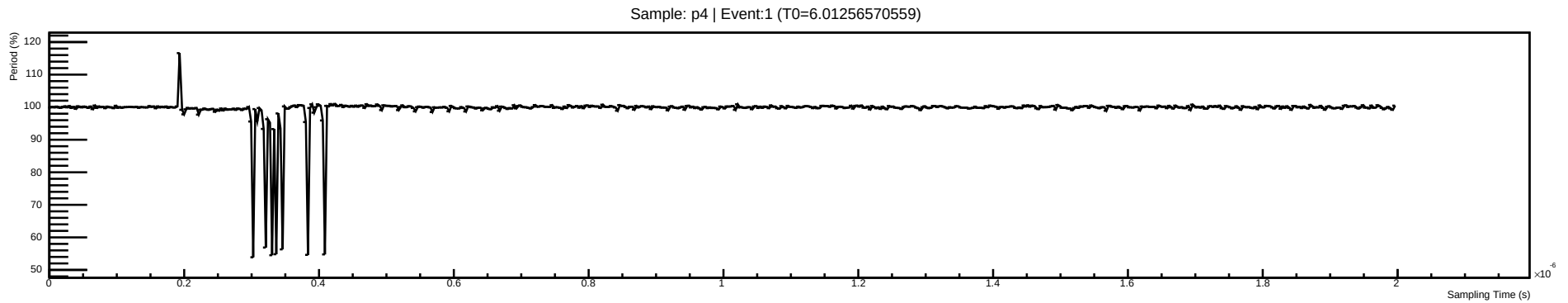


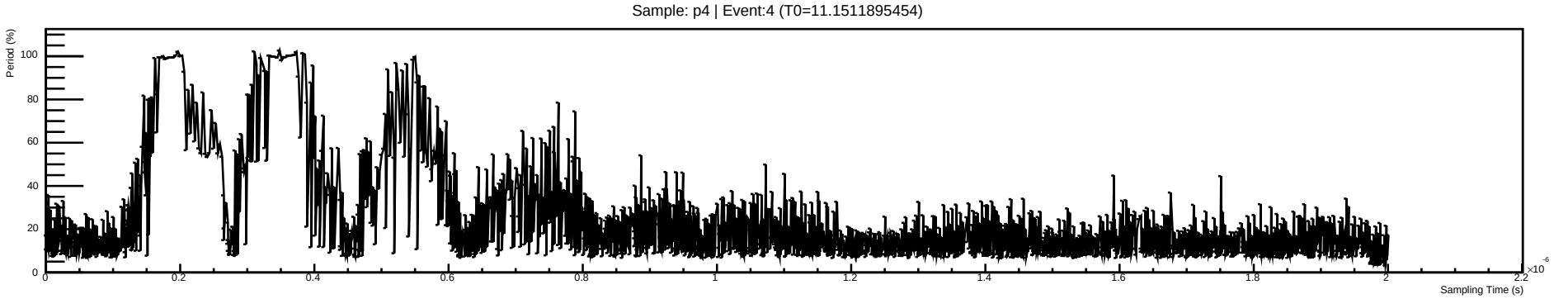




PERIOD







Recovery time (good event) < 1 µs.

SECOND TEST-BEAM

TEST BEAM @ LAUVAIN LA NEUVE (07/05/2015)

Beam

- Niquel, Argon & Neon.
- Krypton ionization irrealistic.
- 4 hours of beam $\rightarrow$ 250 GB.
- Individual

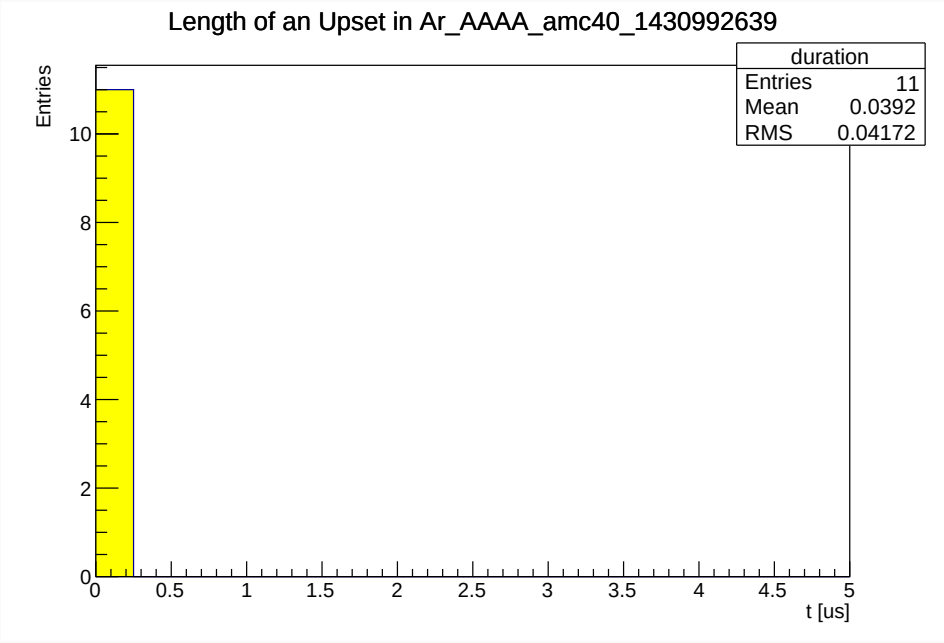
DAQ

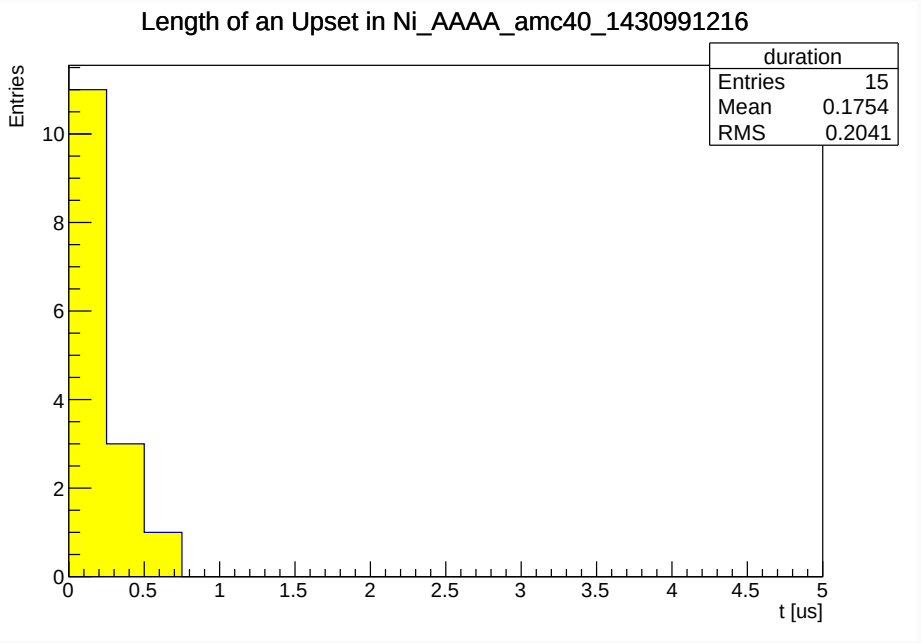
- AAAA and FFFF0000 patterns (MiniDAQ).
- 2 FGPA firmwares:
  - passthrough $\rightarrow$ raw data.
  - BERT (Bit Error RaTe).
- PLL clock monitoring, non-differential (Oscilloscope).

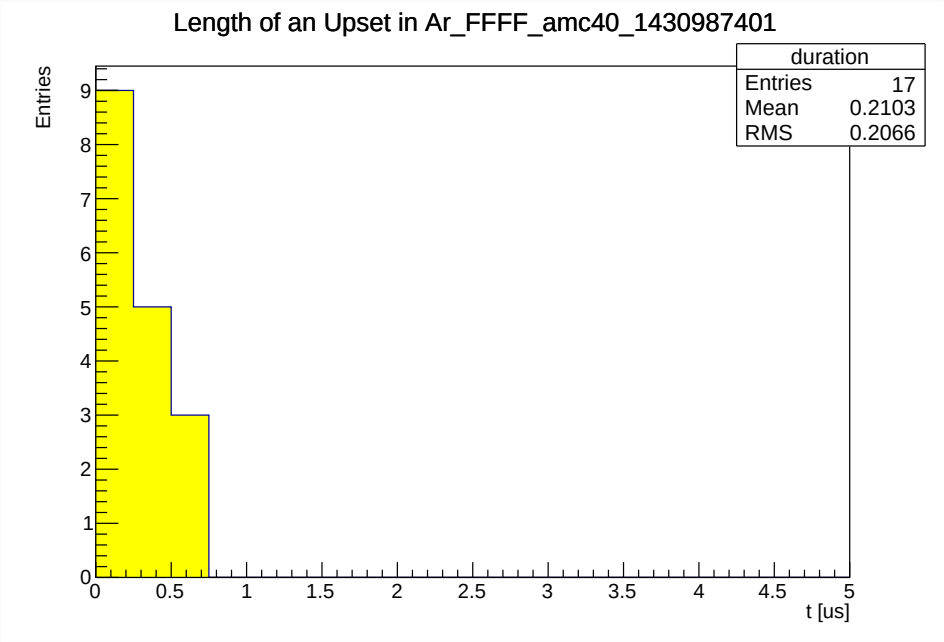
+

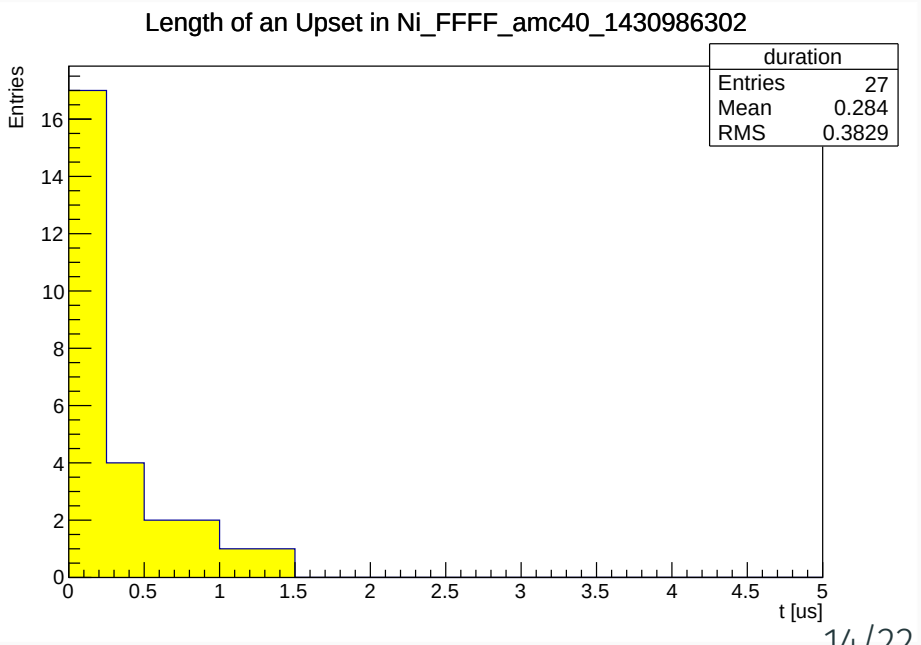
File name	No. of SEUs	Time in error, us	Size GB	No. of SEUs per GB	Time in error per GB, us
Ni_FFFF_amc40_1430986302	27	8.34	20	1.35	0.42
Ni_AAAA_amc40_1430991216	15	3.01	20	0.75	0.15
Ni_AAAA_amc40_1430991294	9	1.27	10	0.90	0.13
Ar_FFFF_amc40_1430987401	17	4.00	20	0.85	0.20
Ar_AAAA_amc40_1430992639	11	0.71	20	0.55	0.04
Ar_AAAA_amc40_1430992719	4	0.24	10	0.40	0.02
Ar_AAAA_amc40_1430992749	4	0.15	10	0.40	0.02
Ne_FFFF_amc40_1430989285	2	0.06	20	0.10	0.00
Ne_FFFF_amc40_1430989365	5	0.21	20	0.25	0.01

RECOVERY TIME AFTER SEU

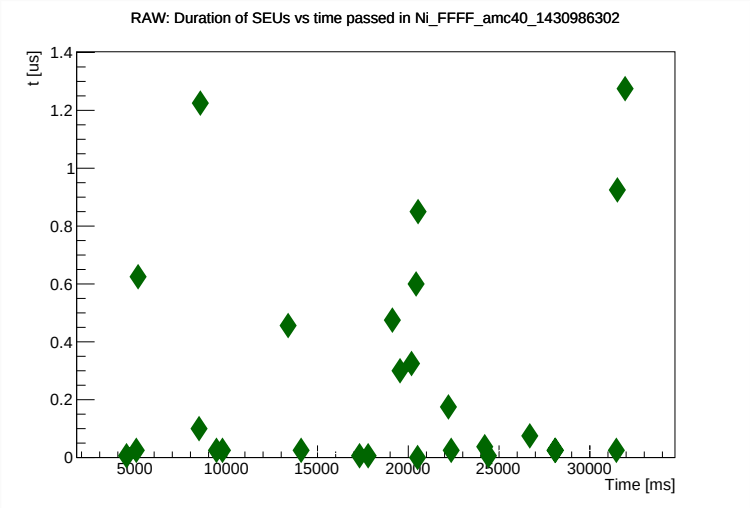




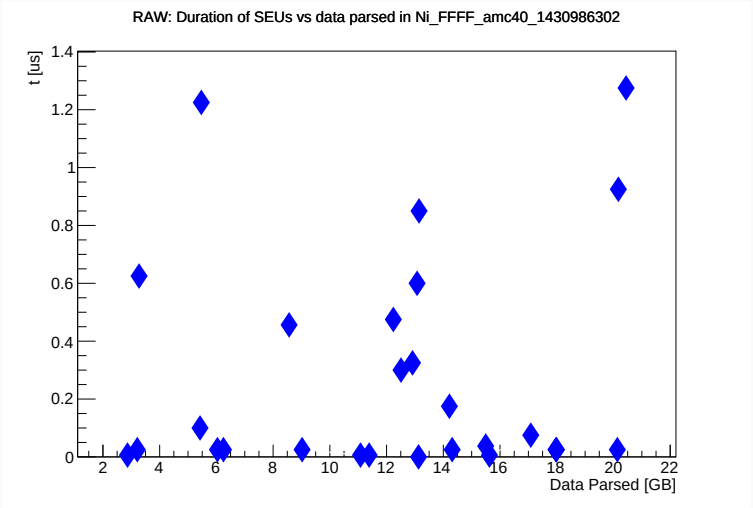




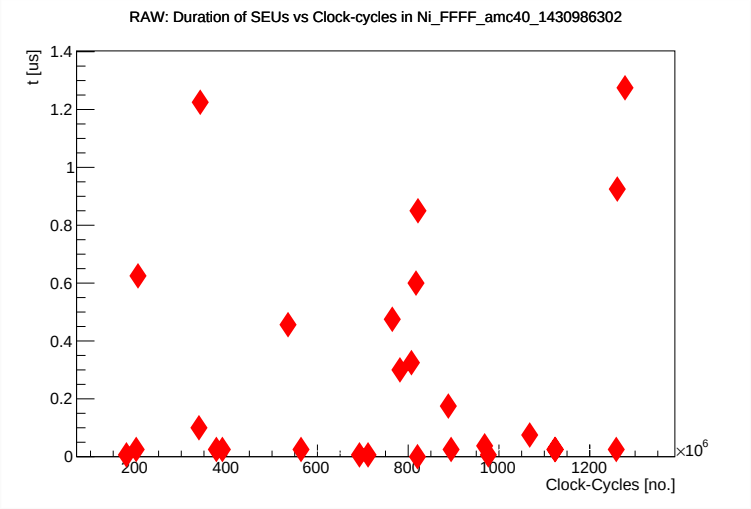
UPSET DEPENDENCES



SEU duration Vs time between upsets.

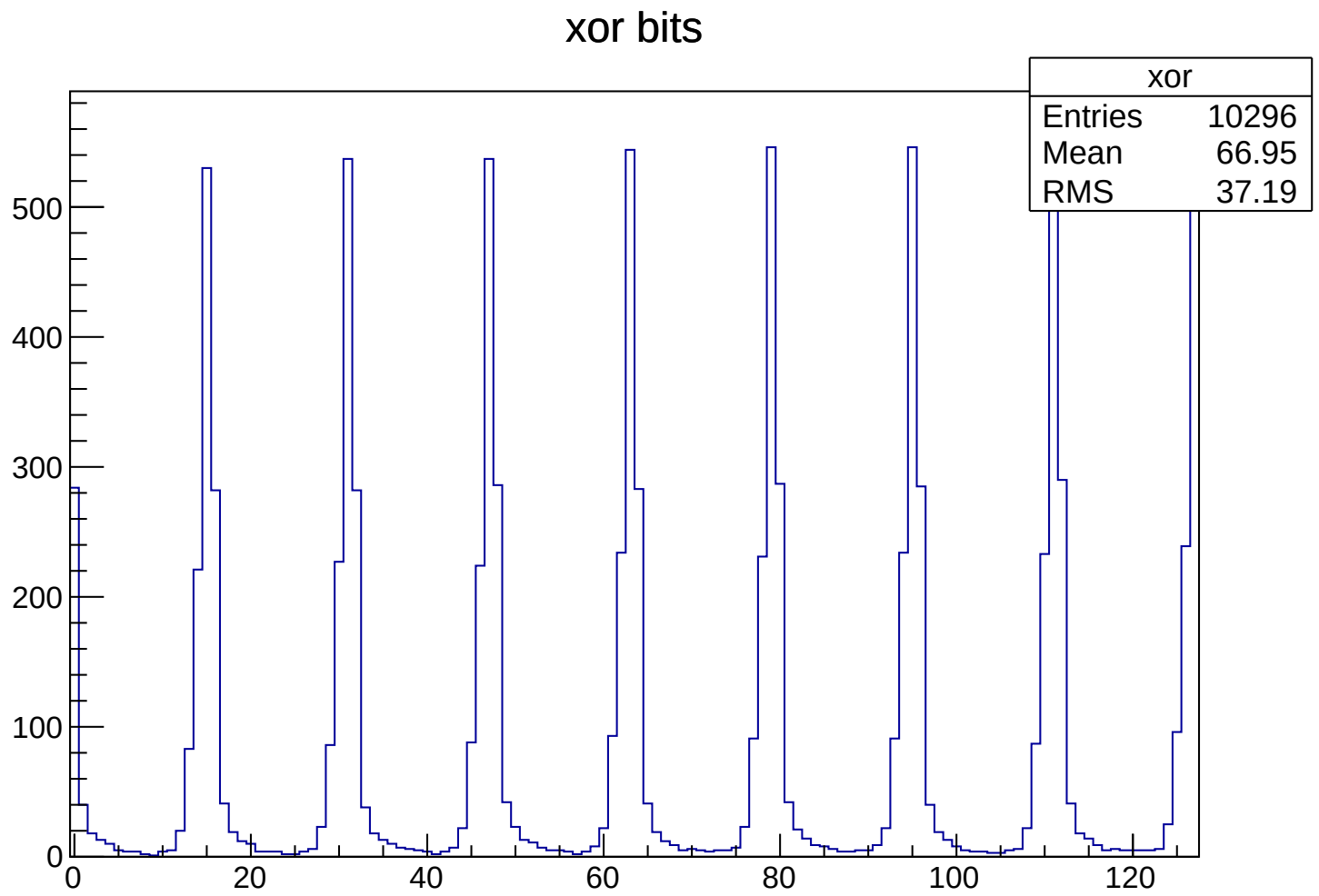


SEU duration Vs file size.

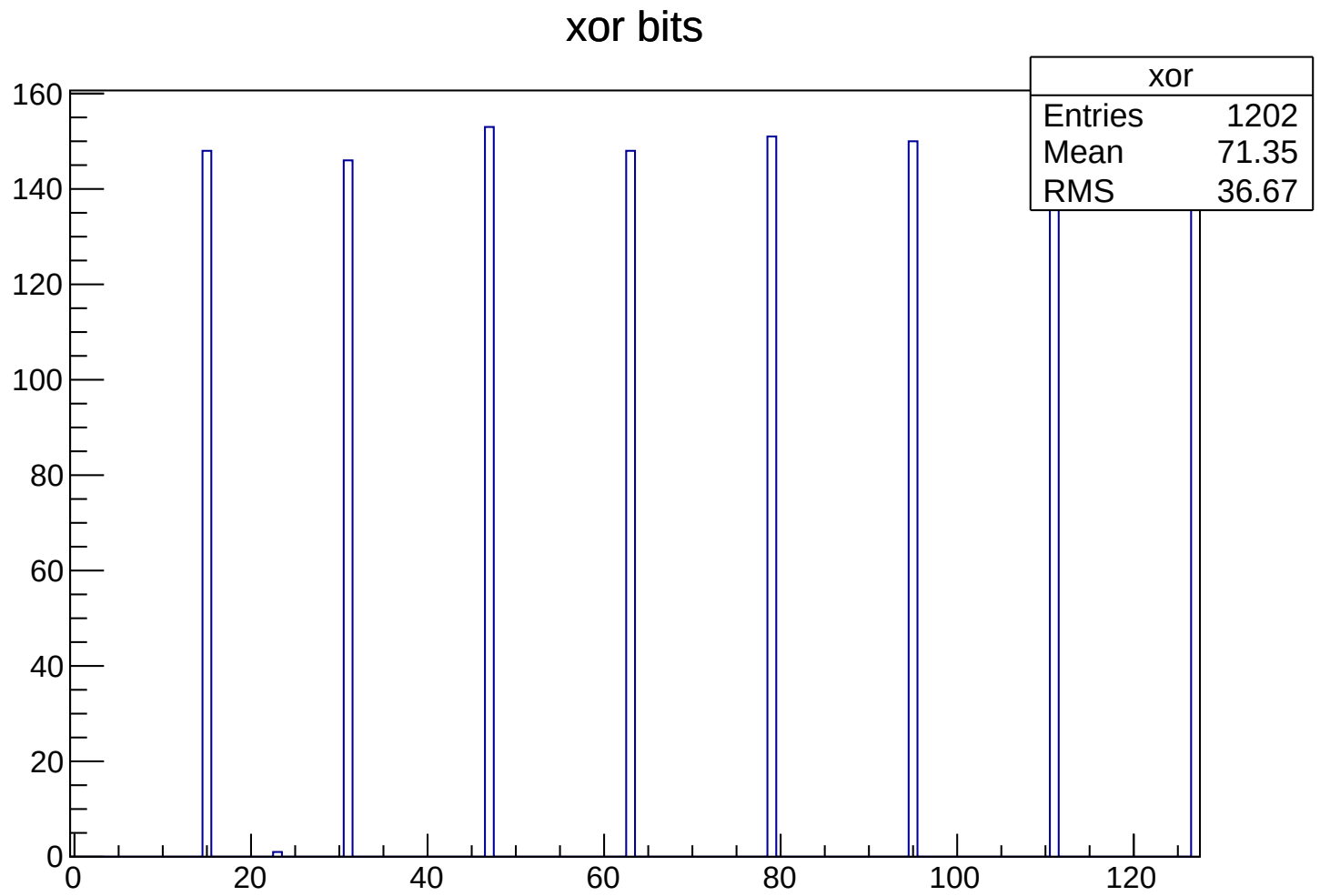


SEU duration Vs occurrance in clock cycle units.

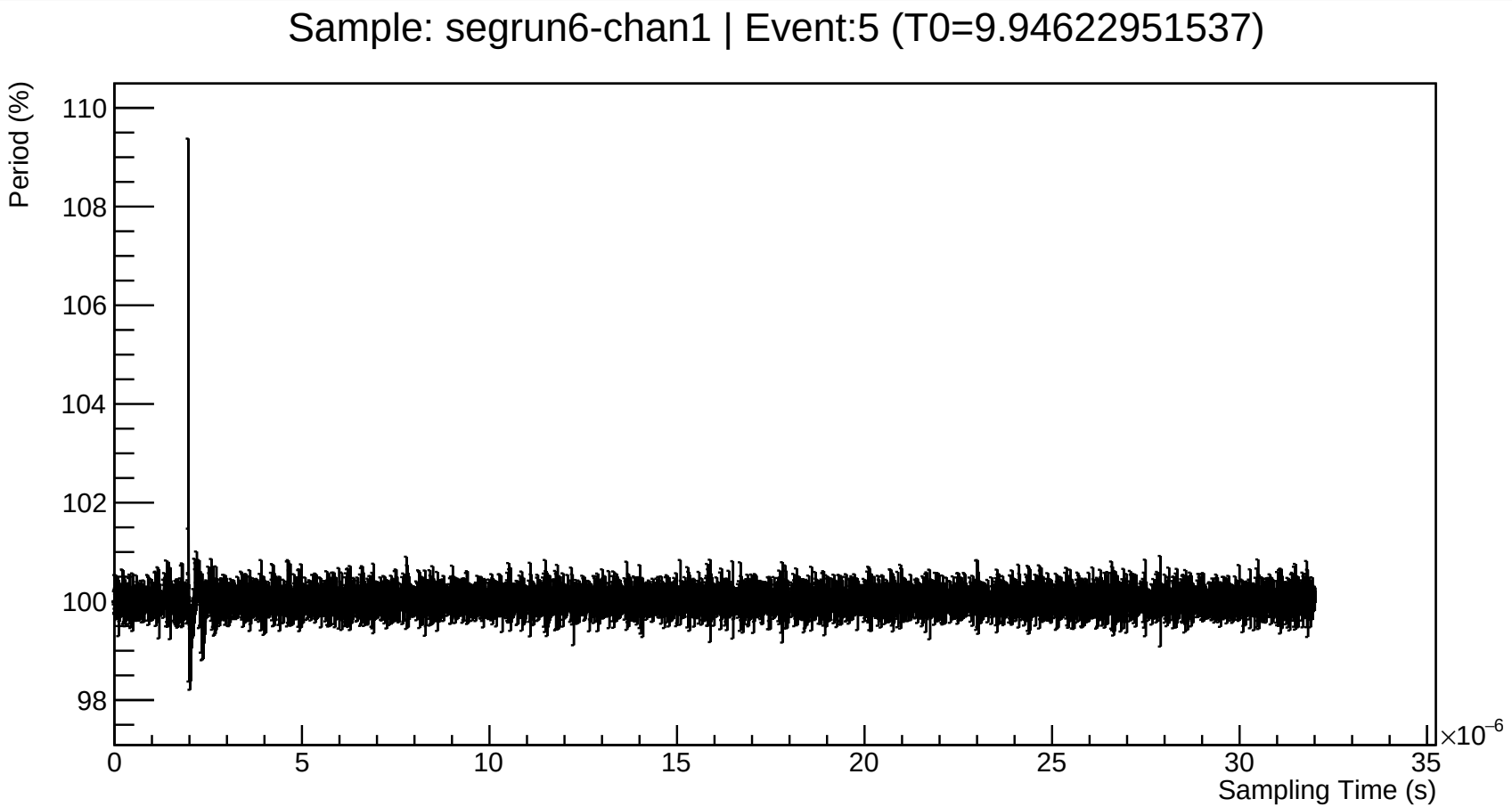
BERT Data


xor bits
xor
Entries 10296
Mean 66.95
RMS 37.19
0
100
200
300
400
500
0
20
40
60
80
100
120

BERT Data


xor bits
xor
Entries 1202
Mean 71.35
RMS 36.67
160
140
120
100
80
60
40
20
0
0
20
40
60
80
100
120

PLL SIGNAL (NON-DIFFERENTIAL)



WORK ONGOING

FPGA firmware

- Currently can lock to data, but not to GWT header.
- Implement a loop back to decouple problem between GWT and MiniDAQ.
- Router and data processing ongoing.

PLL

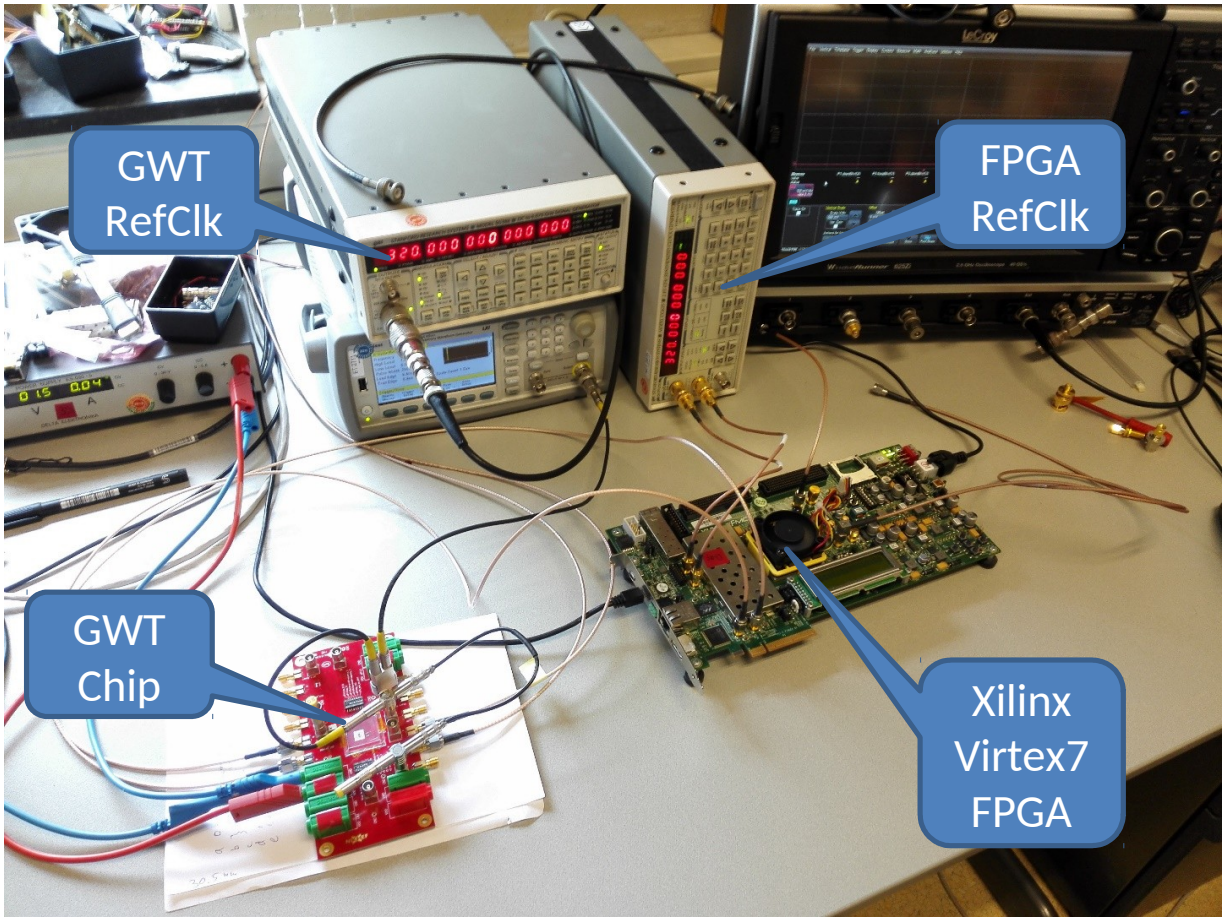
- Considering further test to investigate the “funny” PLL clock signal.

SUMMARY

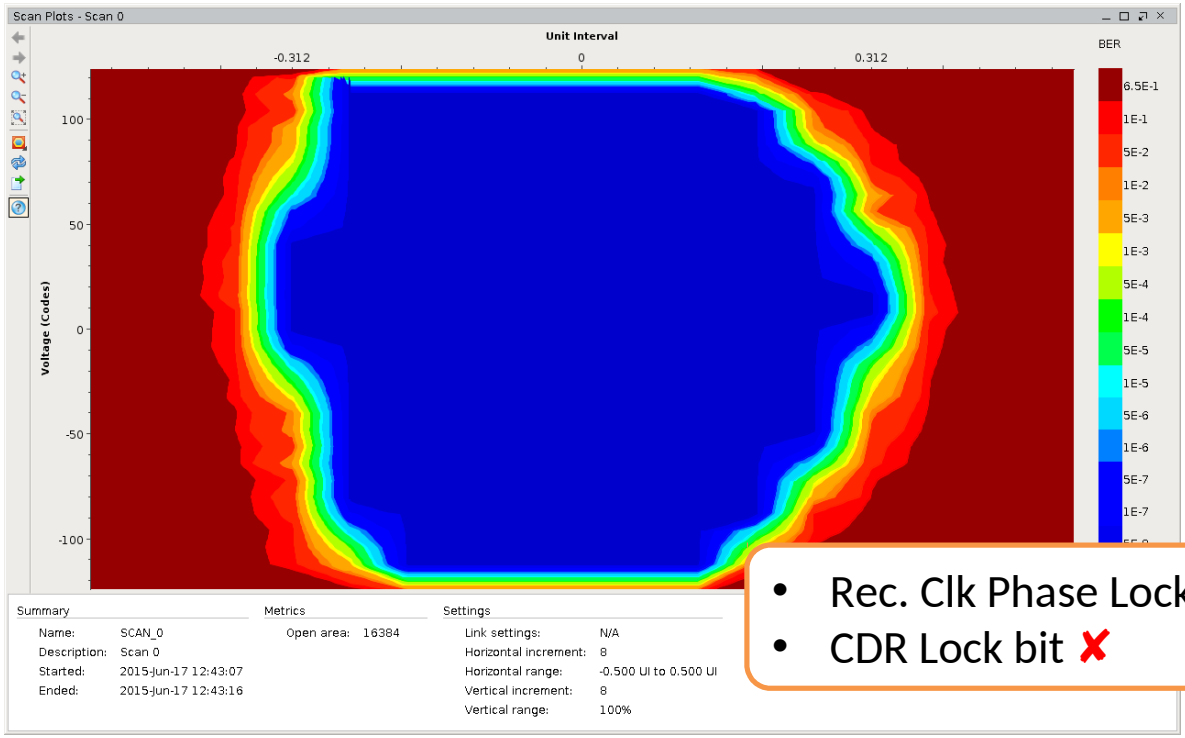
- GWT serializer is faster and less power demanding than GBT.
- DAQ firmware has to be adapted for GWT. Ongoing.
- Readout setup (MiniDAQ + PC + GWT board + ...) is easy to transport and set up.
- Test beam showed:
  - SEUs consistent with ionization power.
  - Unexpected effect in differencial PLL clock signal.
  - Recorevy times after SEU < 1.5 µs.
  - SEUs occurs randomly.
- Still work to do: firmware, future test-beams(?).

Backup Slides

Xilinx Ibert core measurement setup



Eye diagram of Clock generator @ 2.56GHz

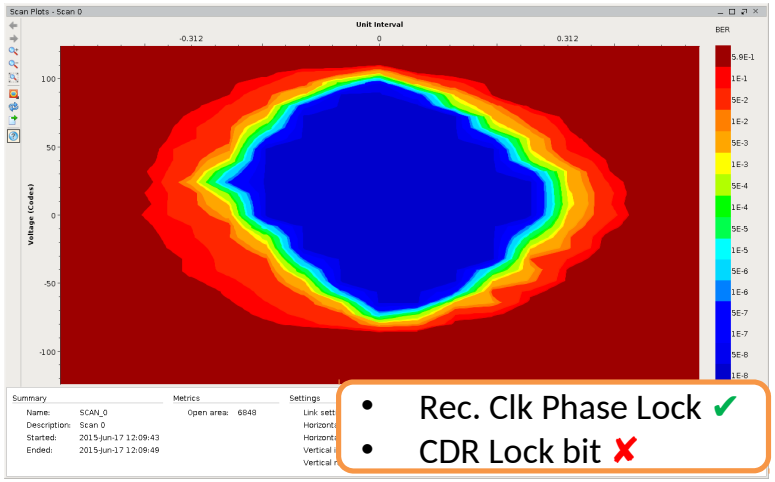


- Rec. Clk Phase Lock ✔
- CDR Lock bit ✘

✔ ✘

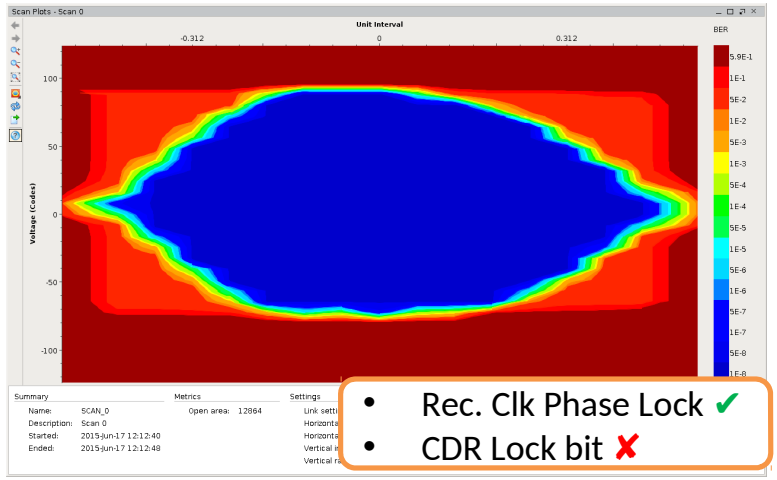
Eye diagrams of Gwt patterns (no PLL)

AAAA pattern



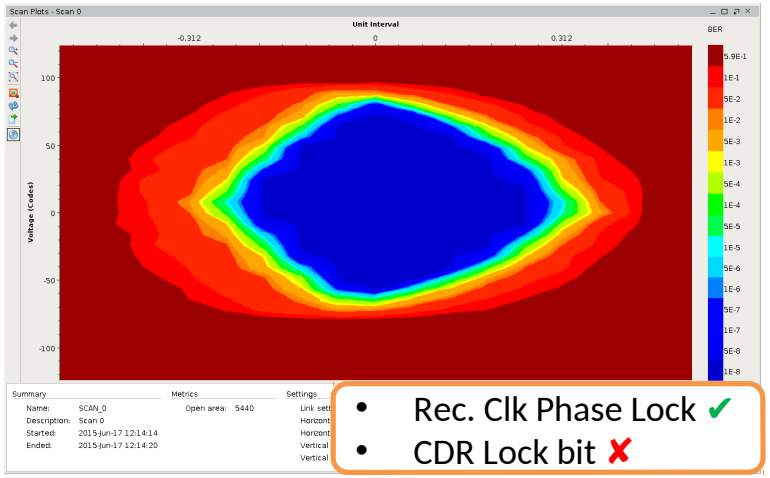
- Rec. Clk Phase Lock ✔
- CDR Lock bit ✘

FF00 pattern



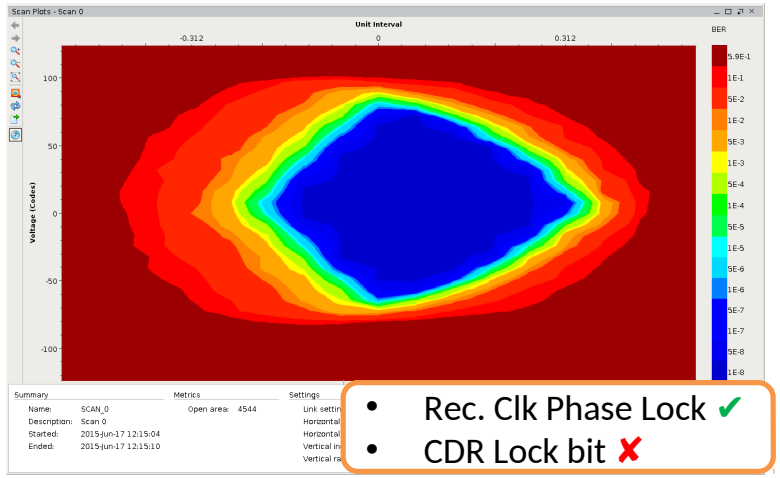
- Rec. Clk Phase Lock ✔
- CDR Lock bit ✘

PBRS^16 pattern



- Rec. Clk Phase Lock ✔
- CDR Lock bit ✘

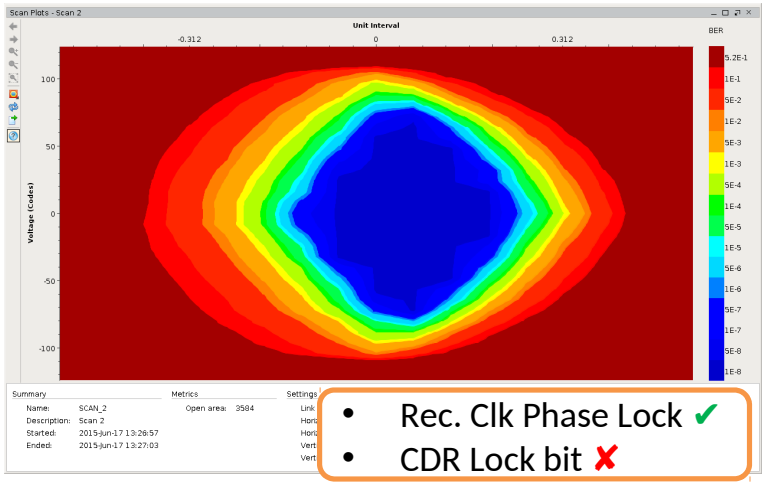
scrambled pattern



- Rec. Clk Phase Lock ✔
- CDR Lock bit ✘

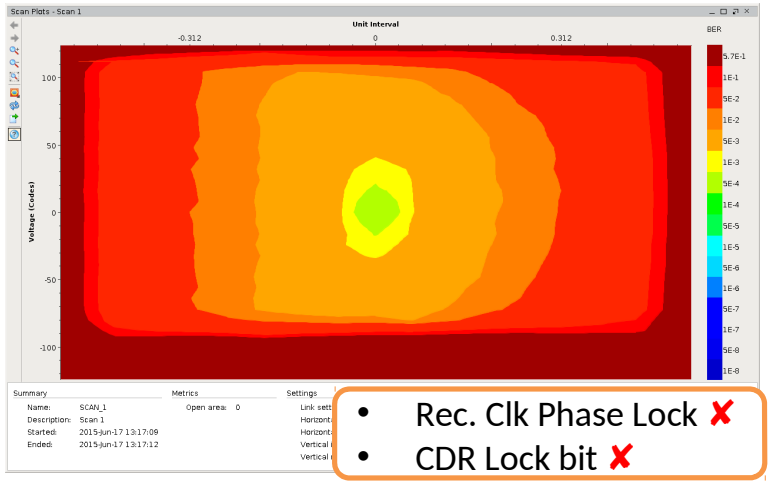
Eye diagrams of Gwt patterns (with PLL)

AAAA pattern



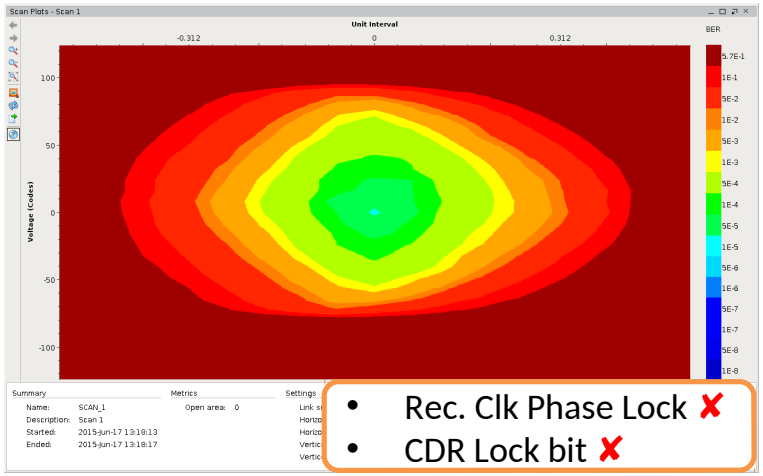
- Rec. Clk Phase Lock ✔
- CDR Lock bit ✘

FF00 pattern



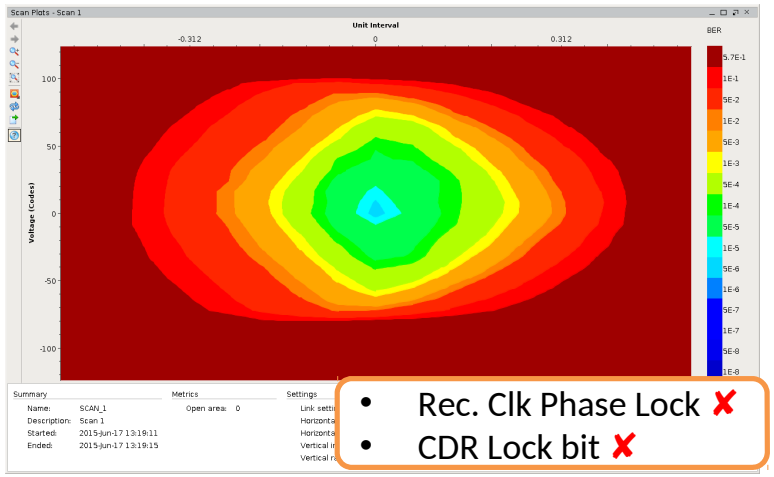
- Rec. Clk Phase Lock ✘
- CDR Lock bit ✘

PBRS^16 pattern



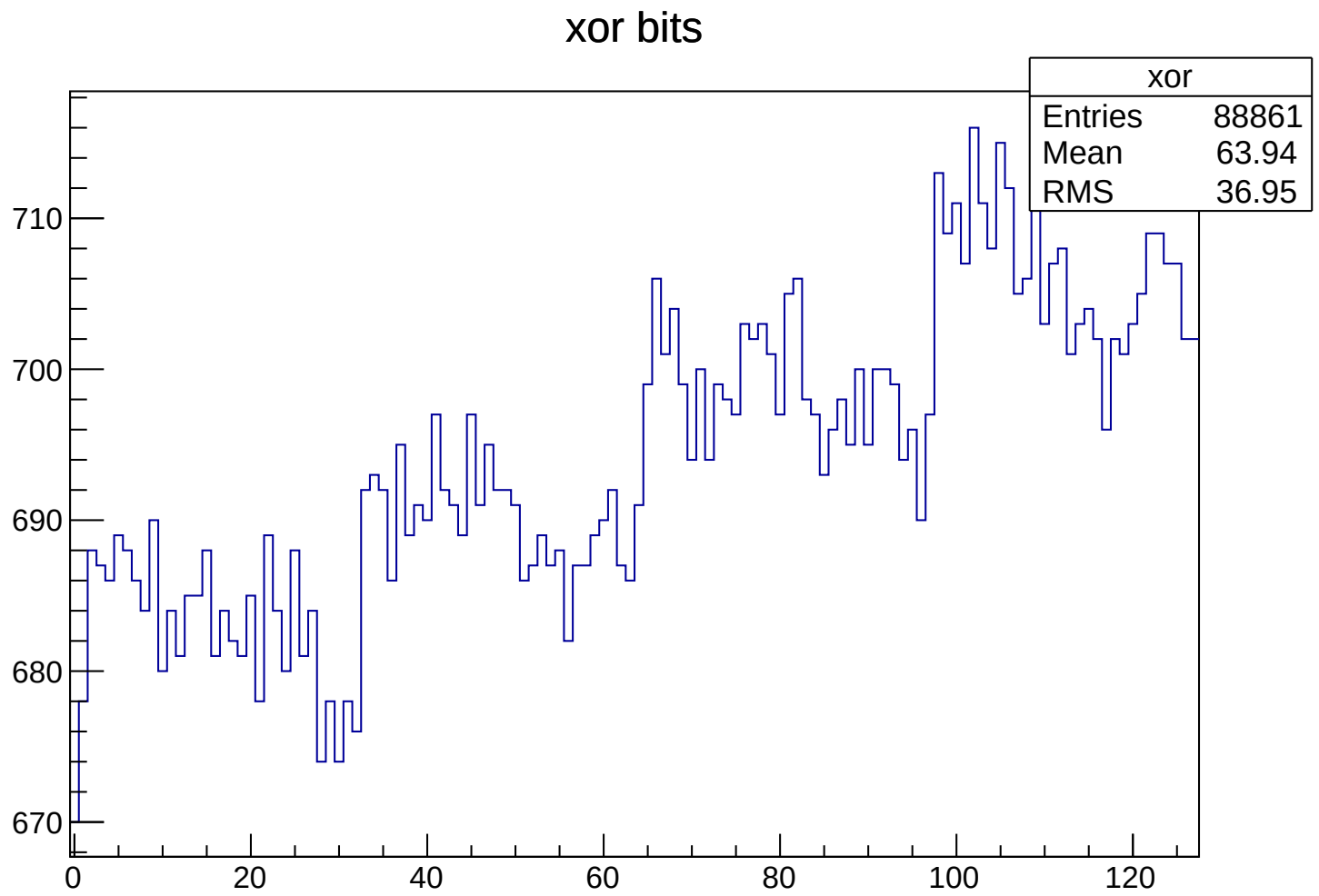
- Rec. Clk Phase Lock ✘
- CDR Lock bit ✘

scrambled pattern

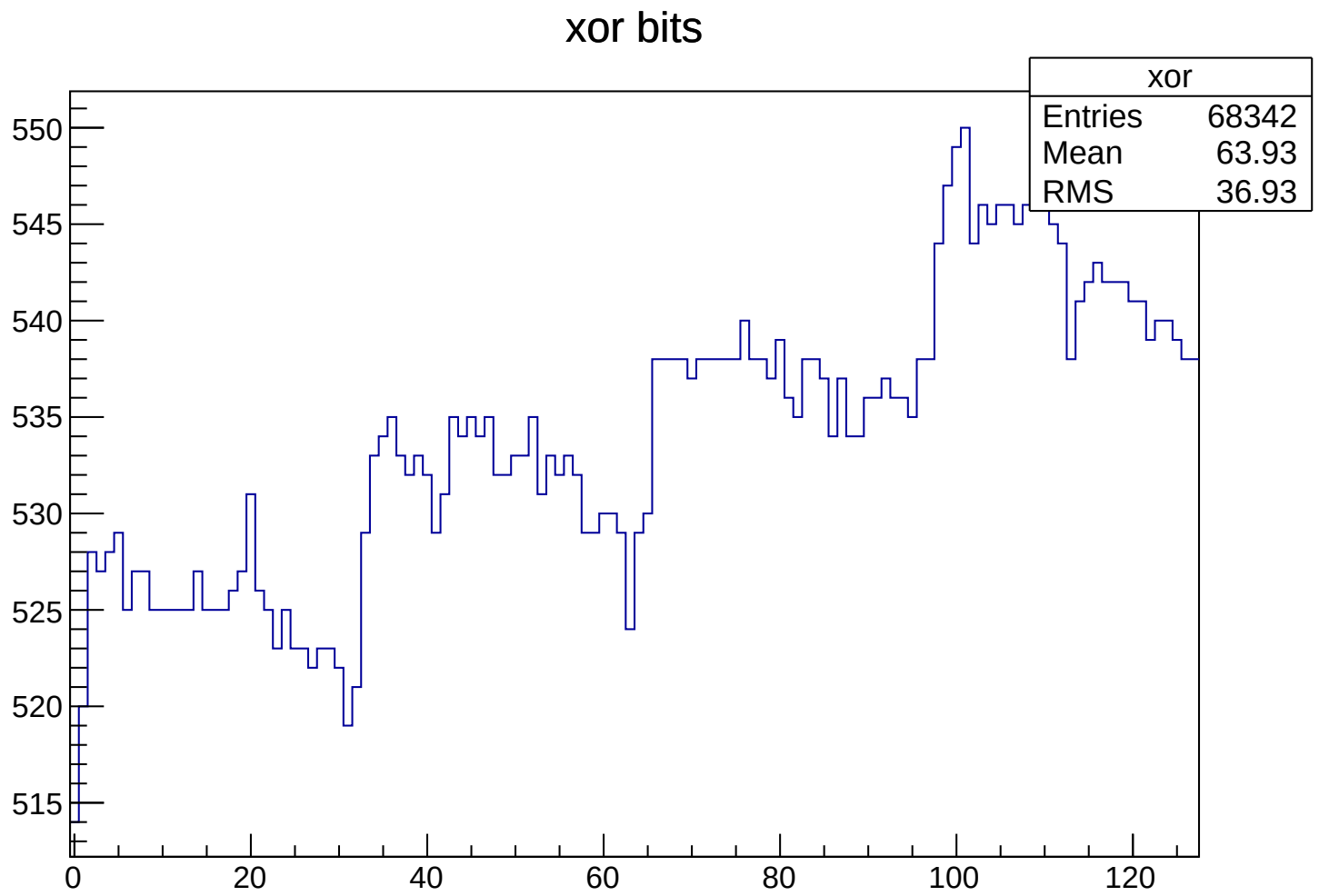


- Rec. Clk Phase Lock ✘
- CDR Lock bit ✘

BERT Data


xor bits
xor
Entries 88861
Mean 63.94
RMS 36.95
710
700
690
680
670
0
20
40
60
80
100
120

BERT Data


xor bits
xor
Entries 68342
Mean 63.93
RMS 36.93
550
545
540
535
530
525
520
515
0
20
40
60
80
100
120