Isolated Cluster Flagging Module

MPhys Presentation

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Presentation Overview

Background

- Introduction
- LHCb

The isolated cluster flagging block

- Generations of design

Testing

Introduction

- Cloned the updated VELO24 branch
  - vhd file containing entity definition missing - the file is RAM_ID_DEMUX.vhd in the specific velopix directory
  - Copied over file again and compiled without any
  - Would like to check this file is correct
- Currently redesigning the module to have constant timing

Position in firmware

- Data processing block has changed since this module was designed
  - Original positioning needed to be changed because of the edge detectors in the post router
  - The new position will be right at the start of the post router before the edge detectors
  - The flagging bit is the MSB of each 32bit word, therefore taking input from inflactionary_block

Timing

- Each data processor within the ICF block needs the following number of clock cycles per BCID:
  - 1 clock cycle to check if it is empty (0 SPPs)
  - 4 clock cycles to read in the 4 512bit frames associated with the BCID
  - 65 clock cycles to sort the columns and flag isolated clusters
  - 4 clock cycles to write it out
- The BCID processing is parallelised within the ICF module
- 16 rams could be processed every 229 clock cycles with 16 ICF modules

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Summary

- New design to fit in with the post router
- Timing now constant in new design
- Testing new design in Modelsim

- Outlook
  - Test the new top level in Modelsim
  - Incorporate into the post router as a drop in module