SPP Isolation Flagging Module

Progress Update

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23 March 2017

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Overview

Concept

- Function of the SPP isolation flagging module
- Block Diagrams

Implementation

- Implementation in VHDL
- Testing in Modelsim
- Incorporation into the full AMC40 Firmware

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The SPP isolation flagging module

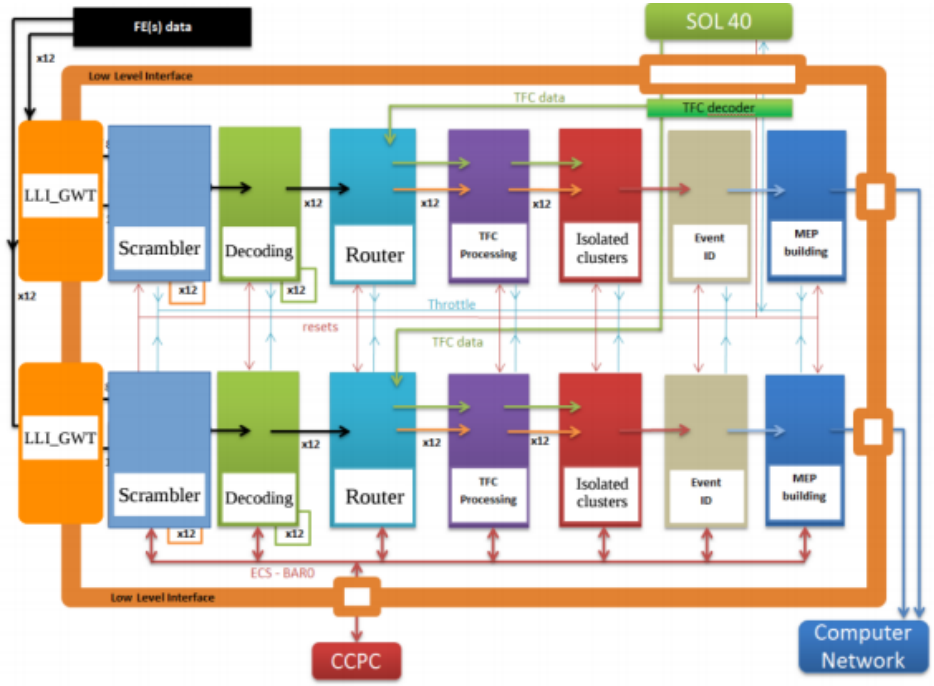

Figure : Drop in module (shown as "Isolated Clusters" in this image) to check for isolated clusters.

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The event isolation flagging module

Columns in the SPP

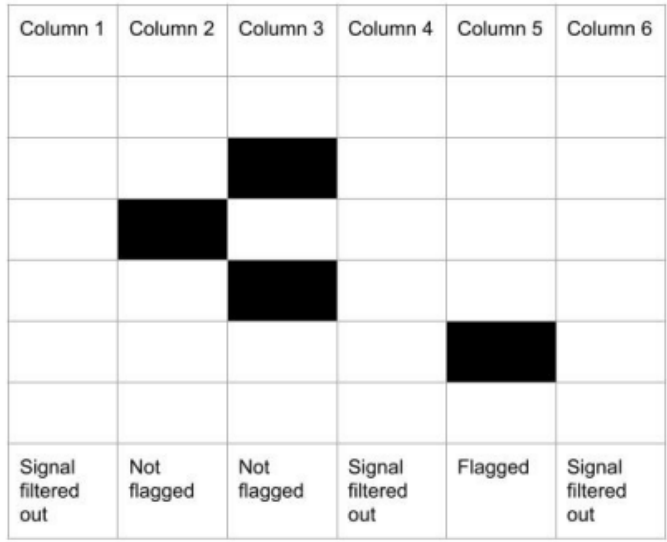

Figure : Columns with no neighbours are flagged. Doing this in the FPGA reduces load on CPU in software stage.

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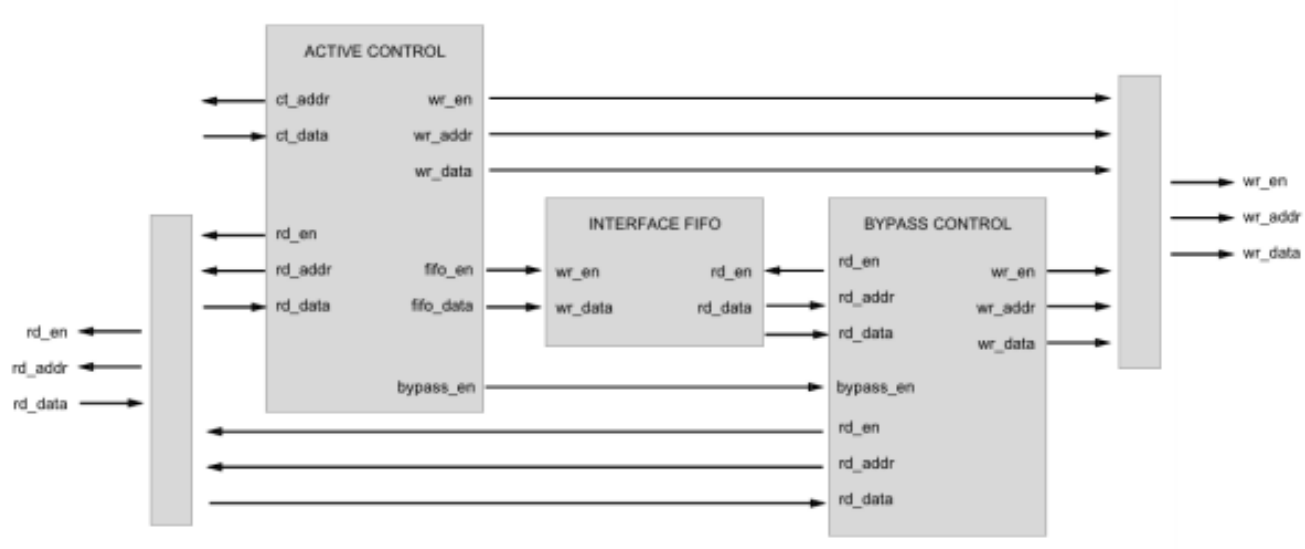
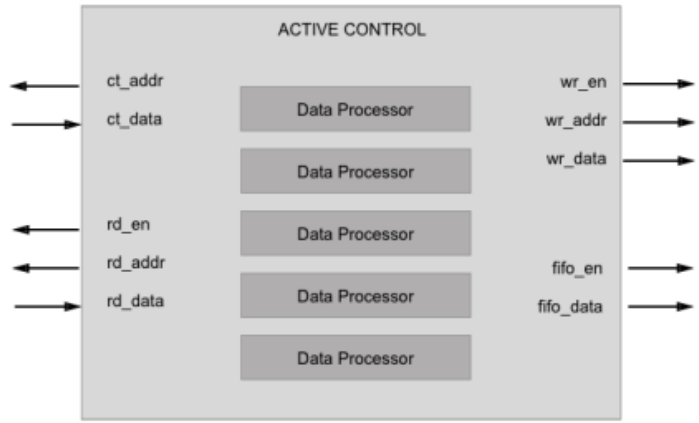
The event isolation flagging module

Top level block Diagram



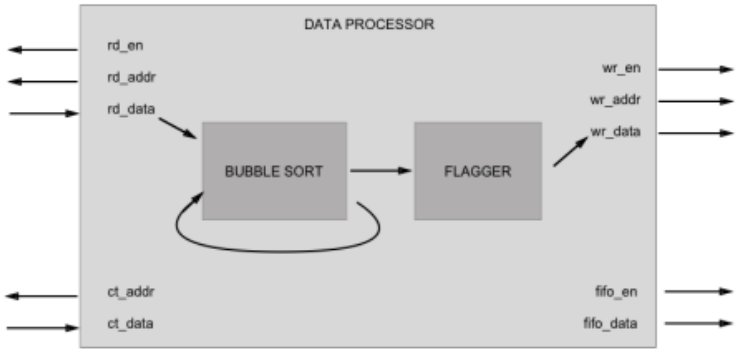
- Checks each column in SPP to see if it is isolated.

Active Control



- Assigns tasks to the next free data processor
- Keeps track of clock cycles.

Data Processor



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Implementation in VHDL

- Using code started by masters students last year
- Code now compiles and can be simulated in Modelsim.

Testing in Modelsim

- All low level blocks tested and working
- Generated random data packages to test at top level
- Next step: test with realistic data.

Incorporation into the full AMC40 Firmware

- Cloned the full AMC40 firmware repository (velo24 branch)
- Inserted data processing block
- Next step: ... .

Summary

- Implementation in Modelsim is complete; mid way through testing
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- Outlook
  - Complete testing in Modelsim with realistic data
  - Test as a standalone module in Quartus
  - Incorporate into full AMC40 firmware.