SINGLE STAGE TIA DATA

	311VGEE 317 VG		
Gate Voltage (VG)	Output Voltage (Vout)	Transimpedance Gain (M Ω)	
0.4	1.657663221	3.315326441	
0.6	1.657663219	3.315326438	
0.8	1.657663219	3.315326438	
1	1.657663219	3.315326438	
1.2	1.657662615	3.31532523	
1.4	1.556253466	3.112506931	
1.6	1.392032395	2.784064791	
1.8	1.379330409	2.758660817	
2	1.374790502	2.749581003	
Width of NMOS(μm)	Output Voltage (Vout)	Transimpedance Gain (M Ω)	
0.5	1.95	3.9	
1	1.66	3.32	
1.5	1.49	2.98	
2	1.37	2.74	
2.5	1.29	2.58	
3	1.22	2.44	
Width of PMOS(μm)	Output Voltage (Vout)	Transimpedance Gain (M Ω)	
1	1.66	3.32	
1.4	1.8	3.6	
1.8	1.91	3.82	
2.2	2	4	
2.6	2.07	4.14	
3	2.13	4.26	
	THREE STAGE TIA DATA		
Gate Voltage (VG)	Output Voltage (Vout)	Transimpedance Gain (M Ω)	
0.4	2.075408759	4.150817518	
0.6	2.075408759	4.150817518	
0.8	2.075408759	4.150817518	
1	2.075408759	4.150817518	
1.2	2.075408759	4.150817518	
1.4	2.075408759	4.150817518	
1.6	2.075408759	4.150817518	
1.8	1.722666066	3.445332133	
2	1.674717357	3.349434713	
2	1.074717337	3.343434713	
Width of NMOS(μm)	Output Voltage (Vout)	Transimpedance Gain ($M\Omega$)	
0.5		manishing caunce cam (ivizz)	
	2.37	4.74	
1	2.37	4.74	
1 1.5	2.37 2.08	4.74 4.16	
1.5	2.37 2.08 1.9	4.74 4.16 3.8	
1.5 2	2.37 2.08 1.9 1.77	4.74 4.16 3.8 3.54	
1.5 2 2.5	2.37 2.08 1.9 1.77 1.67	4.74 4.16 3.8 3.54 3.34	
1.5 2	2.37 2.08 1.9 1.77	4.74 4.16 3.8 3.54	
1.5 2 2.5 3	2.37 2.08 1.9 1.77 1.67 1.59	4.74 4.16 3.8 3.54 3.34	
1.5 2 2.5	2.37 2.08 1.9 1.77 1.67	4.74 4.16 3.8 3.54 3.34 3.18	

1.4	1.92	3.84
1.8	2.03	4.06
2.2	2.12	4.24
2.6	2.19	4.38
3	2.25	4.5