Lab Five
Fundamentals of Electronics
EECE2412/3

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Abstract

The purpose of this laboratory experiment is to introduce the performer to the operation of metal-oxide-semiconductor field effect transistor (MOSFET) operation in circuitry. These characteristics are then applied to construct a MOSFET inverter, and, finally, a CMOS digital logic inverter.

KEYWORDS: MOSFET, inverter, CMOS, digital logic

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1 Equipment

Available equipment included:

- CD4007 Chips
- Basic Circuit Components (Wires, Inductors, Capacitors, etc.)
- Keysight EDU36311A Dual DC Power Supply
- Keysight EDU33212A Function Generator
- Keysight DSOX1204G Digital Oscilloscope
- BNC Cables

2 Experimental Procedure

2.1 MOSFET Inverters

We begin by using a single transistor on the CD4007 chip to construct the following MOSFET inverter:

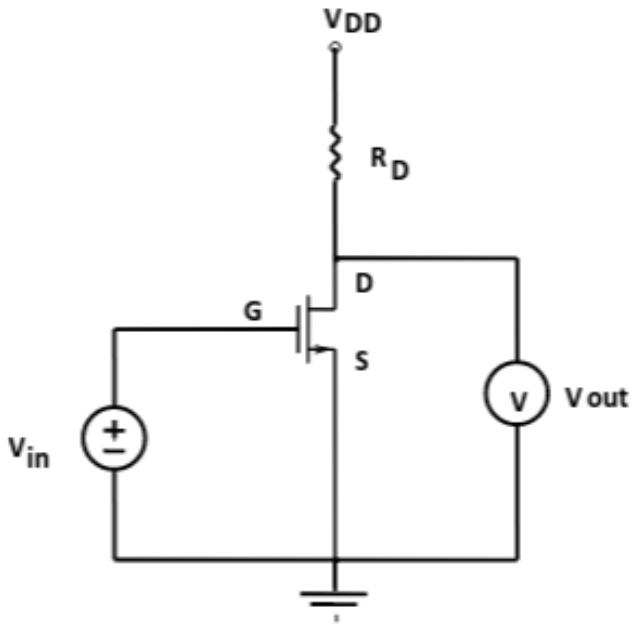

Figure 1: MOSFET Inverter (R_D = 10[kΩ], V_{DD} = 10[V], $0 \leq V_{in} \leq 10$[V])

Using the MOSFET shown in Figure 1 above, we may obtain the following voltage characteristics:

V_{in}[V]	V_{out}[V]	I_D[mA]
0	10	0
1.332	9.95	$5 \cdot 10^{-3}$
1.761	9	.1
1.96	8	.2
2.111	7	.3
2.241	6	.4
2.361	5	.5
2.471	4	.6
2.582	3	.7
2.682	2	.8
2.791	1	.9
3.182	.5	.95
10	.2726	.98274

To run through and obtain the above values took 5:56.68 for just the voltage values, and 10:06.15 to get all of the values (voltage and drain current).

2.2 Threshold Voltage

Based on our table above, we may conclude that the threshold voltage, V_T is approximately 1.278[V]. The actual voltage is obtained by plotting the square root of the drain current against the threshold voltage to get:

Figure 2: Square Root of Drain Current versus Gate-Source Voltage

From this, we may observe that the threshold voltage is, more accurately, $\boxed{V_T = 1.111[\text{V}]}$

2.3 Determining Constant Properties

We may find the value of:

$$\frac{1}{2}k_n\left(\frac{W}{L}\right)$$

for the MOSFET by simply rearranging our drain current formula to obtain:

$$\frac{1}{2}k_n\left(\frac{W}{L}\right) = \frac{.1}{(1.761 - 1.278)^2}$$

$$\boxed{\frac{1}{2}k_n\left(\frac{W}{L}\right) = 4.287 \cdot 10^{-3}}$$

2.4 Transfer Characteristics of the MOSFET

We may plot the output voltage versus the input to get:

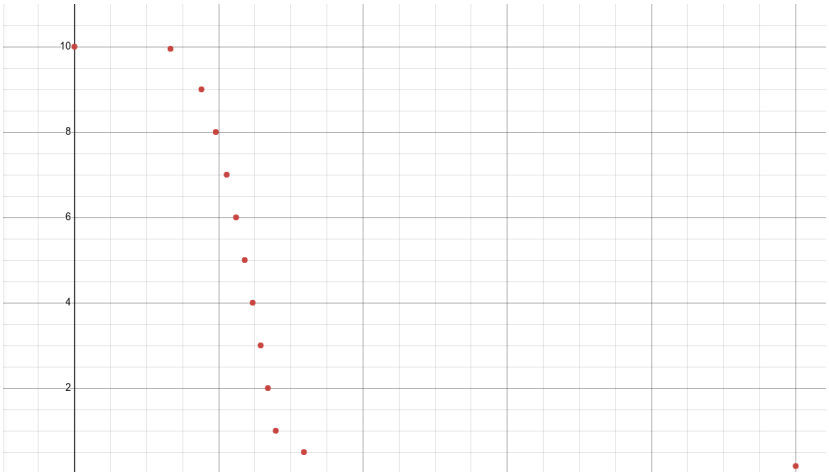

Figure 3: Transfer Characteristic Plot

We may observe from the plot that the modes of operation are, approximately as follows:

$$\boxed{\begin{cases} \text{Cutoff}, & 0 \leq V_{in} \leq 1.278[\text{V}] \\ \text{Triode}, & 1.278 \leq V_{in} \leq 3.182[\text{V}] \\ \text{Saturation}, & 3.182 \leq V_{in} \leq 10[\text{V}] \end{cases}}$$

2.5 Calculating the "On" Resistance

We may calculate the "on" resistance at the point when $V_{in} = 10[\text{V}]$. We may write this as:

$$R_{on} = \frac{V_{DS}}{I_D}$$

Since we know $V_{DS} = V_{out}$, we write:

$$R_{on} = \frac{.1726}{.98279 \cdot 10^{-3}}$$

$$\boxed{R_{on} = 175.63[\Omega]}$$

Since this value is greater than zero, this is not an ideal switch.

2.6 Determining the Bias Point

We know that the bias point occurs where the slope of the transfer plot is greatest. We observe that this occurs at $V_{GS} = 2.361$[V] and $V_{DS} = 5$[V]. The voltage gain at this point would be (inverted):

$$A_v = -\frac{5}{2.361}$$

$$\boxed{A_v = -2.1177}$$

2.7 Applying MOSFETs to CMOS Logic

We may construct the following circuit by using two of the transistors on the CD4007 chip:

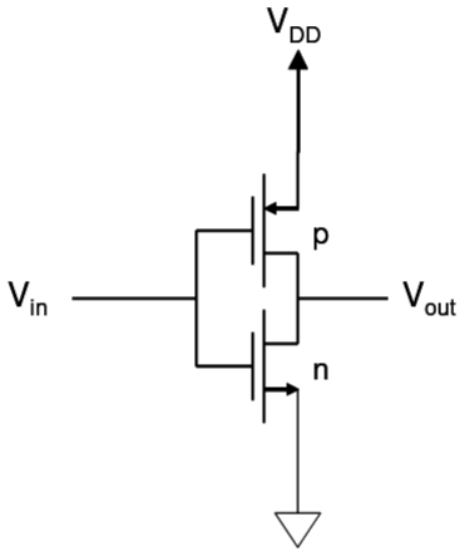

Figure 4: CMOS Logic Inverter

We may use this in a similar manner as the initial circuit, and find the voltage transfer characteristics:

V_{in}[V]	V_{out}[V]
0	10
1.89	9.95
3.62	9
4.28	8
4.56	7
4.7	6
4.77	5
4.83	4
4.88	3
4.98	2
5.56	1
6.36	.5
10	10[µV]

2.8 CMOS Logic Transfer Characteristics

We then plot this to get:

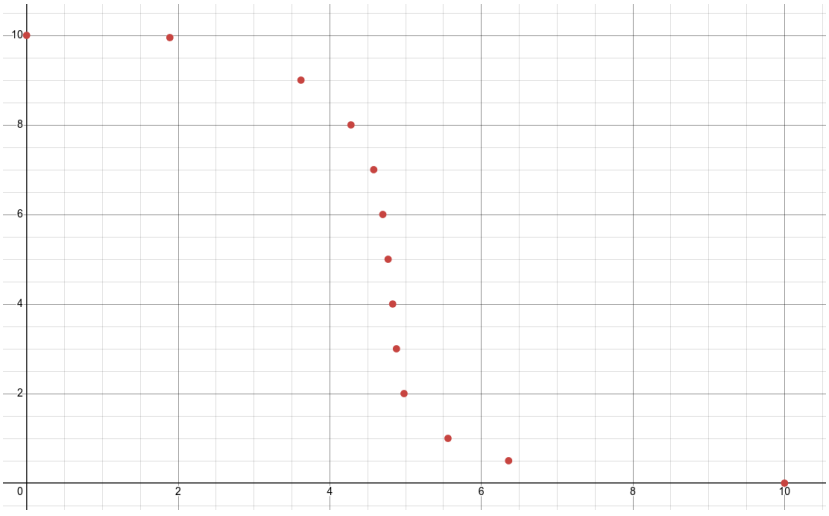

Figure 5: CMOS Logic Inverter Transfer Characteristics

We may determine that the bias point occurs at $(4.77, 5)$, which gives us a gain of:

$$A_v = -\frac{5}{4.77}$$

$$\boxed{A_v = -1.0482}$$

We know that there is know power dissipation in a logic circuit.

2.9 Building a 3-Input NOR Gate

We construct the following circuit:

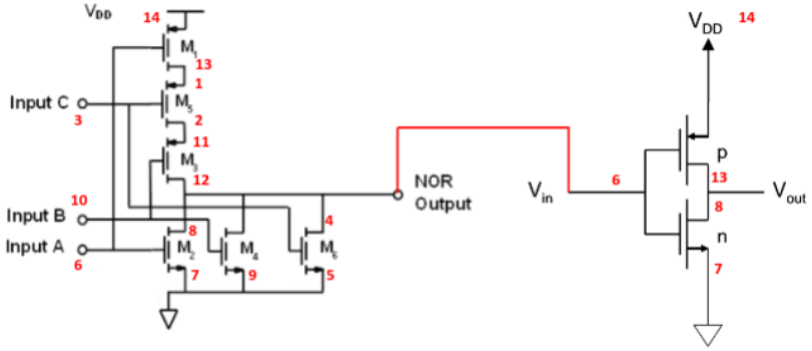

Figure 6: 3-Input NOR Gate Using MOSFETS

The physical construction of this looks like:

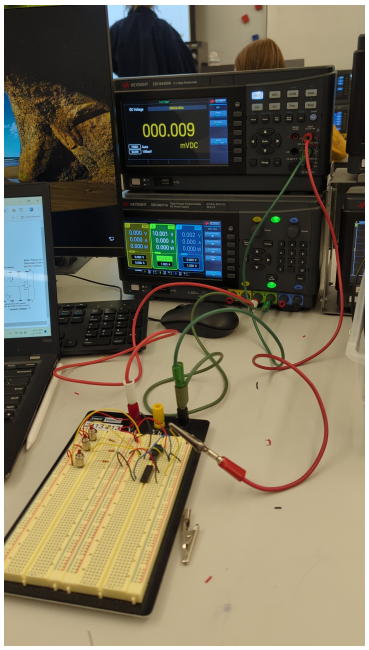

Figure 7: Physical 3-Input NOR Gate Circuit

The behavior of the circuit is as expected, and can be seen below:

Figure 8: Scan to View Circuit Behavior

3 Conclusion

Overall, this laboratory experiment allowed the performed to get a better understanding of the operation and applications of MOSFETs to various circuitry.