Homework 4

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1. (a) Let us assume the diode is in forward bias. In this case, the circuit consists simply of the source and resistor, which gives us current:

$$I = \frac{v_{in}}{R}$$

Given that this value is sinusoidal, when greater than zero, we know that our initial assumption was true. When the voltage is zero or negative, the ideal diode is reverse-biased. We can now proceed to say:

$$v_o = \begin{cases} v_{in}, & v_{in} > 0 \\ 0, & v_{in} \leq 0 \end{cases}$$

Given that the given equation is:

$$v_{in} = 10\sin(200\pi t)$$

we know that v_{in} is positive when $2n\pi \leq 200\pi t \leq (2n+1)\pi$, with $n = 0, 1, 2\cdots$. This gives: $(n/100) \leq t \leq (2n+1)/200$, which we can use to plot the transfer function (v_o/v_{in}):

$$H(t) = \frac{v_o}{v_{in}} = \begin{cases} 1, & (n/100) \leq t \leq (2n+1)/200 \\ 0, & \text{otherwise} \end{cases}$$

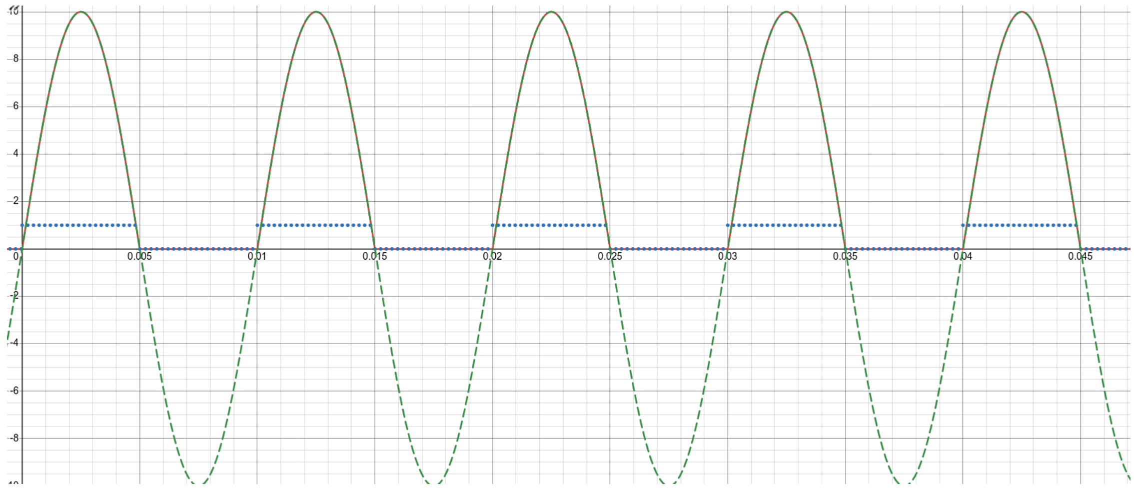

Figure 1: $H(t)$ (blue), v_{in} (green), and v_o (red) in Time Domain

Plotting v_o versus v_{in}, we find a linear relationship:

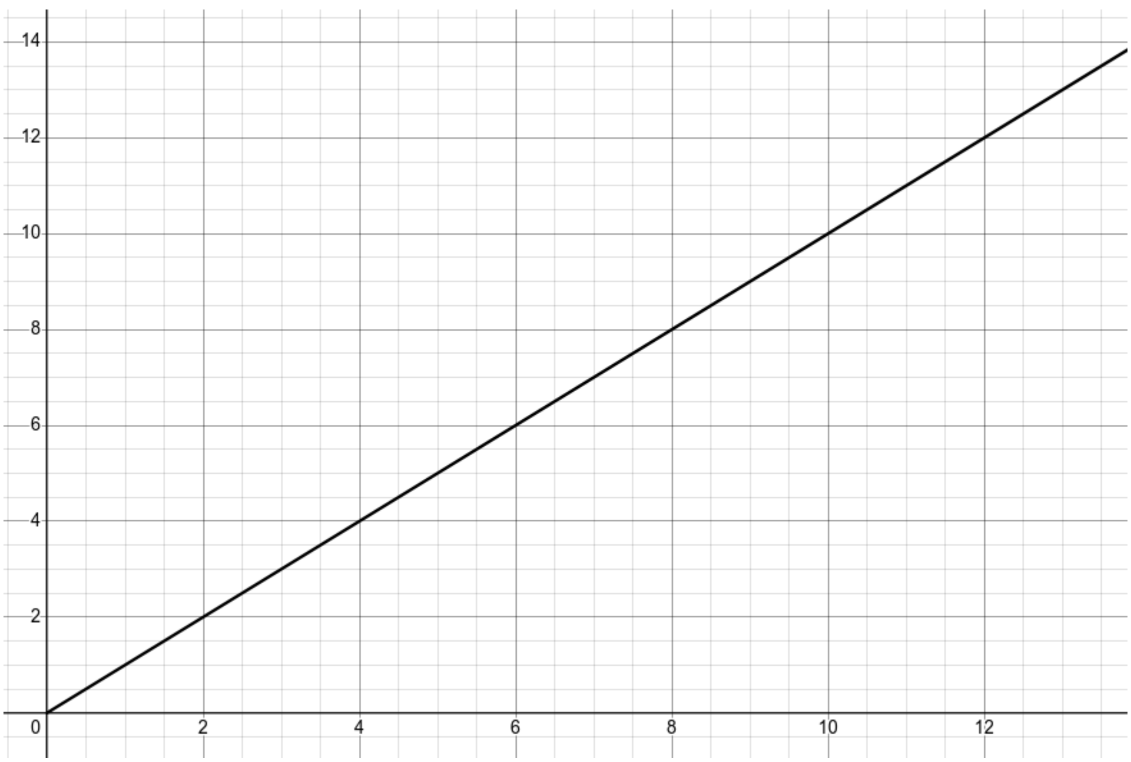

Figure 2: v_o versus v_{in} (1:1 relationship)

(b) Similar to part (a), let us assume this diode is forward biased. In this case, we have the same current flow, indicating that this assumption is correct; however, the cycle is reversed in that v_o is zero when the diode is forward-biased, and $v_o = v_{in}$ when it is reverse biased. Thus, we may write this as:

$$v_o = \begin{cases} v_{in}, & v_{in} \leq 0 \\ 0, & v_{in} > 0 \end{cases}$$

$$H(t) = \frac{v_o}{v_{in}} = \begin{cases} 0, & (n/100) \leq t \leq (2n+1)/200 \\ 1, & \text{otherwise} \end{cases}$$

This gives us the following plot:

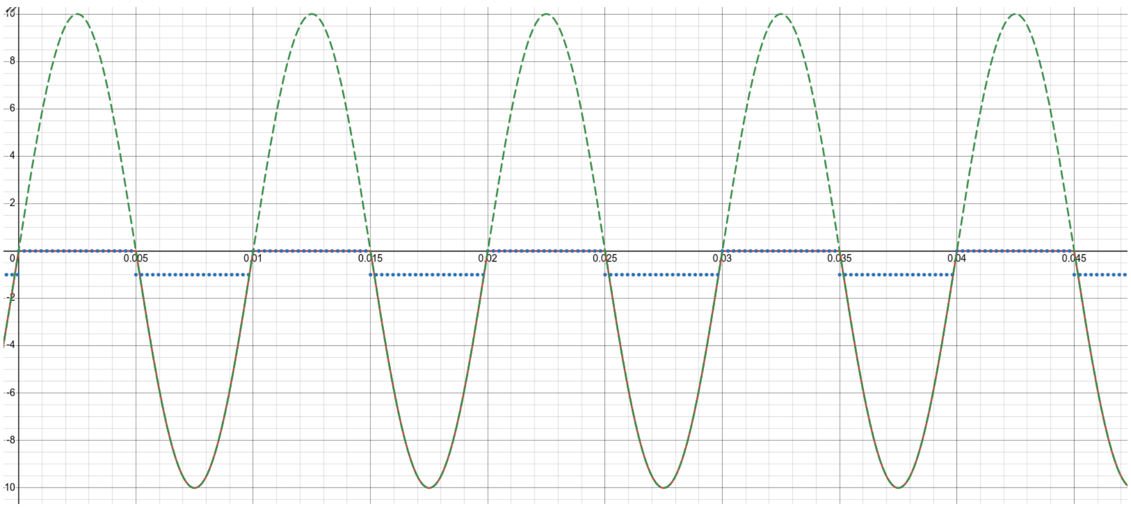

Figure 3: $H(t)$ (blue), v_{in} (green), and v_o (red) in Time Domain

Plotting v_o versus v_{in}, we find a linear relationship:

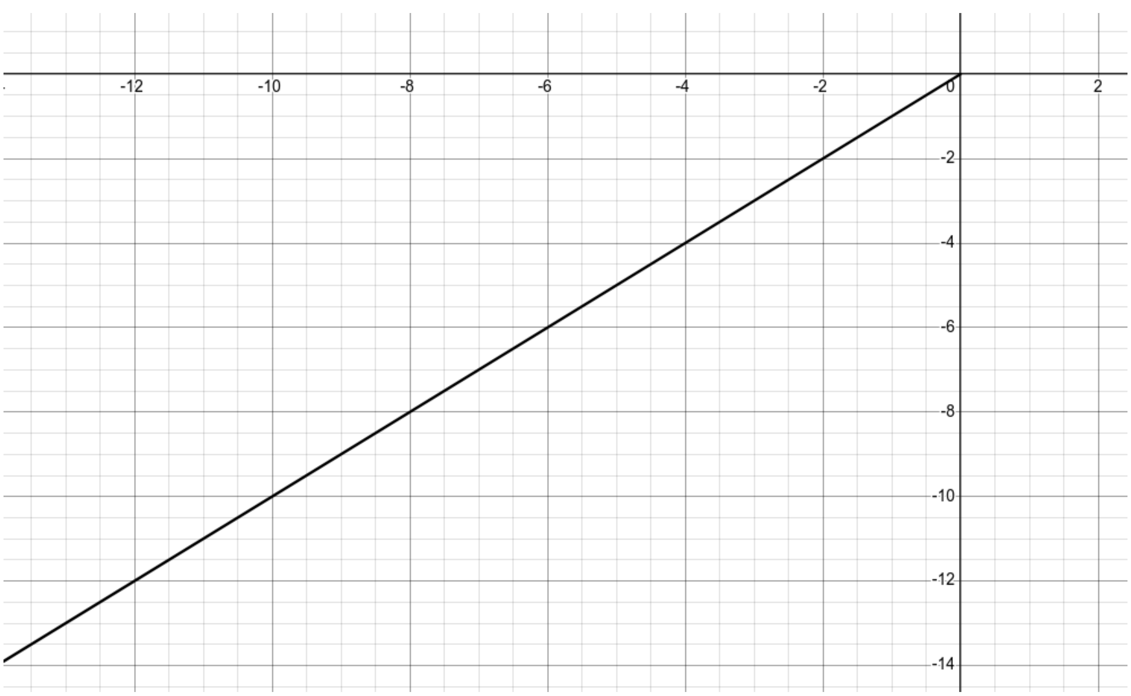

Figure 4: v_o versus v_{in} (1:-1 relationship)

(c) Using a non-ideal, constant voltage drop (CVD) model, we know that, since there is one diode in each circuit, the output will be .7[V] less for a forward-biased diode. For circuit 1, this gives us:

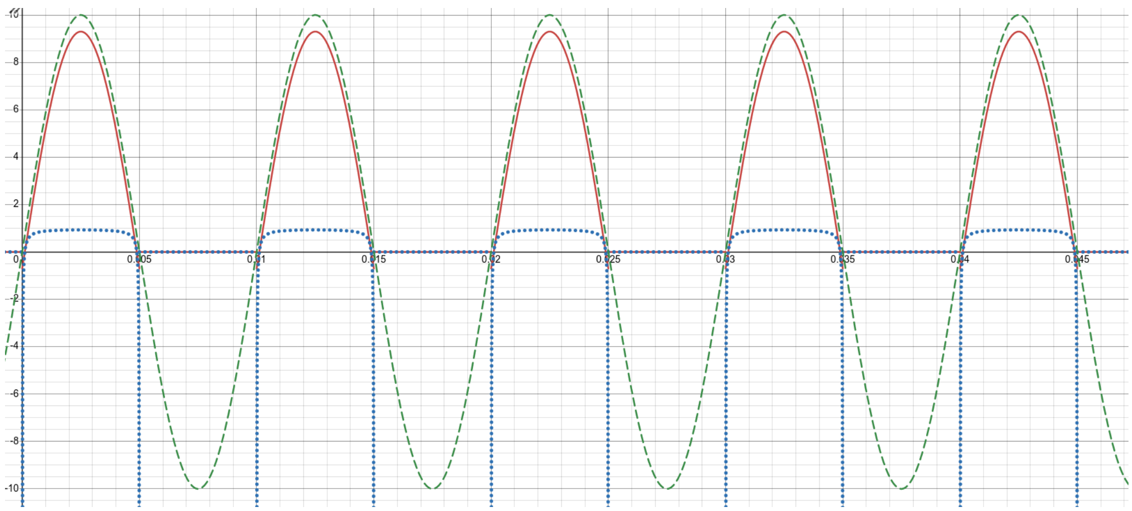

Figure 5: $H(t)$ (blue), v_{in} (green), and v_o (red) in Time Domain

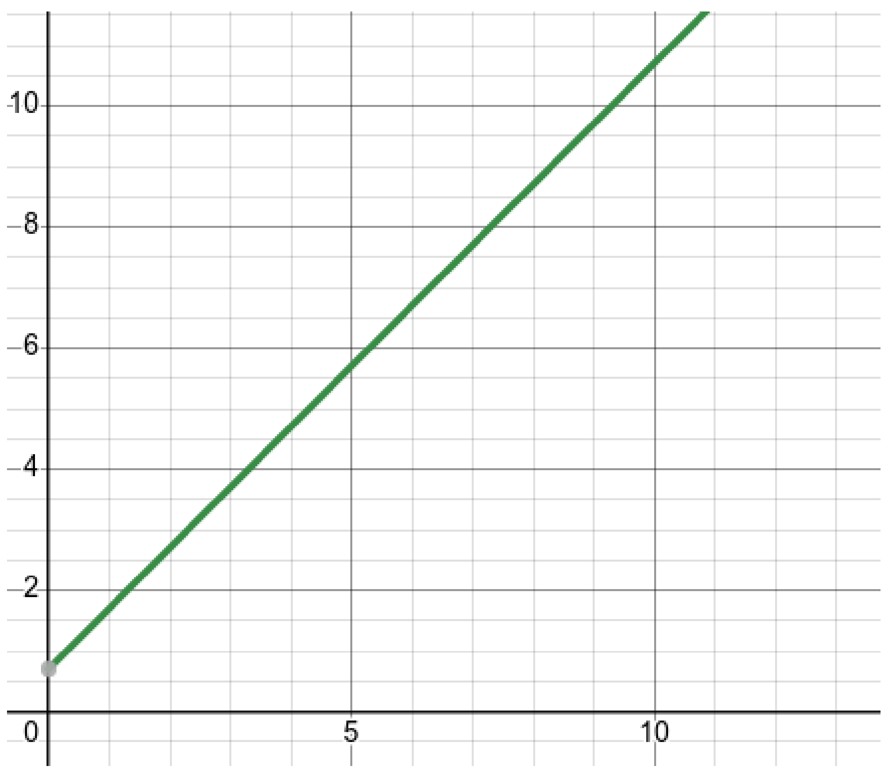

Figure 6: v_o versus v_{in}

Since the voltage was, initially, just zero when the diode was forward-biased (in the ideal case), with CVD we get:

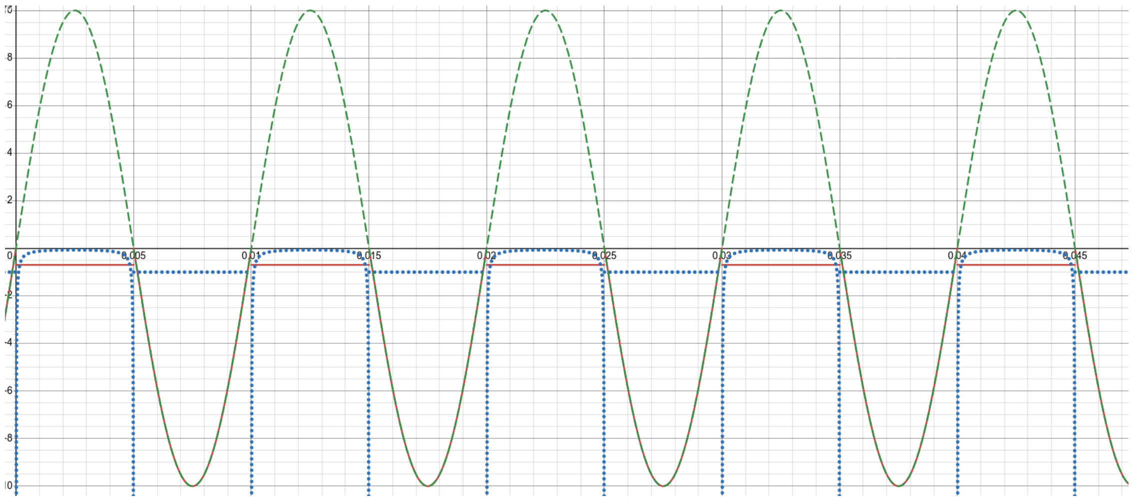

Figure 7: $H(t)$ (blue), v_{in} (green), and v_o (red) in Time Domain

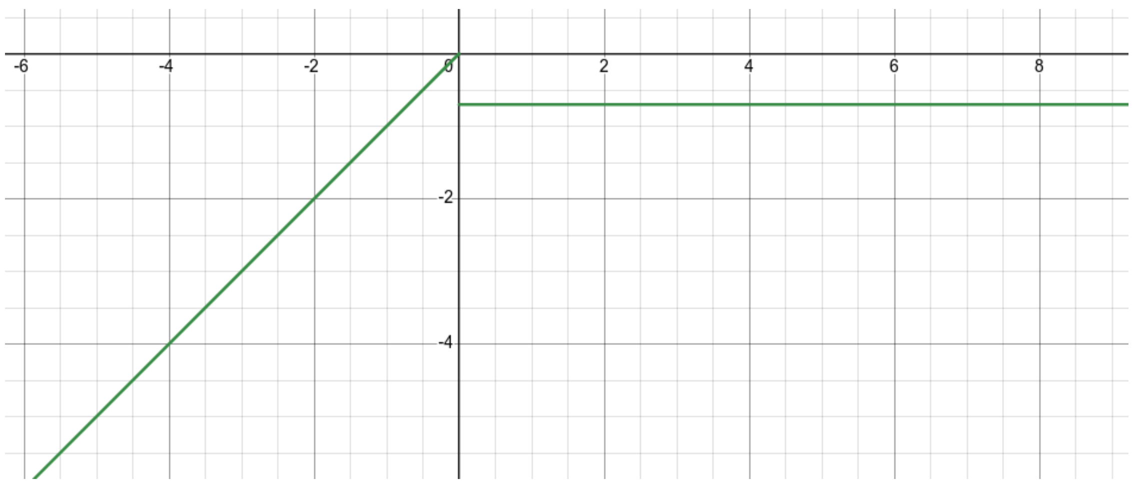

Figure 8: $H(t)$ (blue), v_{in} (green), and v_o (red) in Time Domain

2. (a) We begin by finding the maximum voltage value of the rectifier. Since we know the peak-to-peak ripple, we find the extrema:

$$V_{ext} = V_{avg} \pm \frac{V_{pp}}{2}$$

$$V_{ext} = 9 \pm 1$$

Thus, we see the minimum load voltage is 8[V], with:

$$\boxed{V_{max} = 10[\text{V}]}$$

(b) We know that the peak secondary voltage must be 10[V]. Given this, we can write the turns ratio as (note we need to convert to RMS value):

$$n = \frac{N_1}{N_2} = \frac{V_1}{V_2}$$

$$n = \frac{220}{10\sqrt{2}}$$

$$\boxed{n = 15.6}$$

(c) We can write the equation for capacitance as:

$$C = \frac{I_L T}{V_r}$$

$$C = \frac{(.1)(.01667)}{2}$$

$$\boxed{C = .833[\mathrm{mF}]}$$

We can now construct the circuit and get:

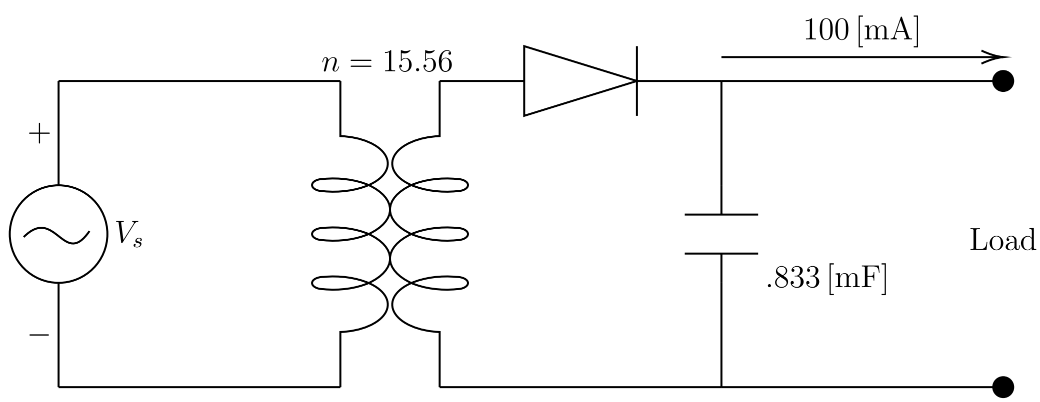

Figure 9: Half-Wave Rectifier Circuit, $V_{max} = 10[\mathrm{V}]$

3. (a) We can see that, if the diode is forward-biased, the current through D can be found as (since the AC source can be omitted in the CVD model):

$$I_D = \frac{7 - .7}{5k}$$

$$\boxed{I_D = 1.26[\mathrm{mA}]}$$

The output voltage is simply the drop across the diode, or:

$$\boxed{V_D = .7[\mathrm{V}]}$$

Since the sinusoid can not exceed $-1[\mathrm{V}]$, we see that the current is always positive, and, therefore, D is always forward-biased.

(b) We may write the Shockley equation as:

$$I_D = I_S\left(e^{\frac{V_D}{nV_T}} - 1\right)$$

Using the given values, we obtain:

$$I_D = 10^{-14}\left(e^{\frac{V_D}{(.025)}} - 1\right)$$

Using I_D from part (a), we get:

$$\left(2 \cdot 10^{10}\right)(6.3) + 1 = e^{40V_D}$$
$$V_D = \ln[\left(2 \cdot 10^{10}\right)(6.3) + 1]$$
$$\boxed{V_D = .639[\mathrm{V}]}$$

(c) The dynamic resistance formula may be written as:

$$r_d = \frac{nV_T}{I_D}$$

Which gets us:

$$r_d = \frac{(.025)}{1.26 \cdot 10^{-3}}$$
$$\boxed{r_d = 19.841[\Omega]}$$

This means that, in the small-signal model, the diode acts as a resistor, which means we have a voltage divider. We can find the AC voltage across the diode using:

$$V_{ac} = V_s\frac{19.841}{19.841 + 5000}$$

This gets us:

$$\boxed{V_{ac} = 3.953\sin(120\pi t)[\mathrm{mV}]}$$

Summing the AC and DC components (the DC value would be from the CVD model), we get:

$$\boxed{V_D = .7 + \left(3.953 \cdot 10^{-3}\right)\sin(120\pi t)[\mathrm{V}]}$$

4. We may begin by analyzing the circuit response to various values of V_s. Let us begin with the case when $V_s = 0$. Here, D_1 would form an open circuit, which lets us calculate the current:

$$I = \frac{5 - .7}{6k}$$
$$I = .7167[\text{mA}]$$

Thus, we can find V_o:

$$V_o = 5 - 5k(I)$$
$$\boxed{V_o = 1.4167[\text{V}]}$$

Here, let us call the node above the single kilo-ohm resistor and ground as V_n. We know that, when $V_s - .7 < V_x$, D_1 remains off, while D_2 is on, so the response remains the same as above (note: $V_x = .7167$[V] when D_1 is off); however, let us test $V_s - .7 \geq V_n$. In this case, D_2 is on until $V_n < 4.3$[V], or $V_s < 5$[V], at which point we can see:

$$V_o = V_s$$

In the case that $V_s \geq 5$[V], D_2 shuts off, and the output is simply 5[V]. Now that we have the pieces, we may plot the entire transfer function:

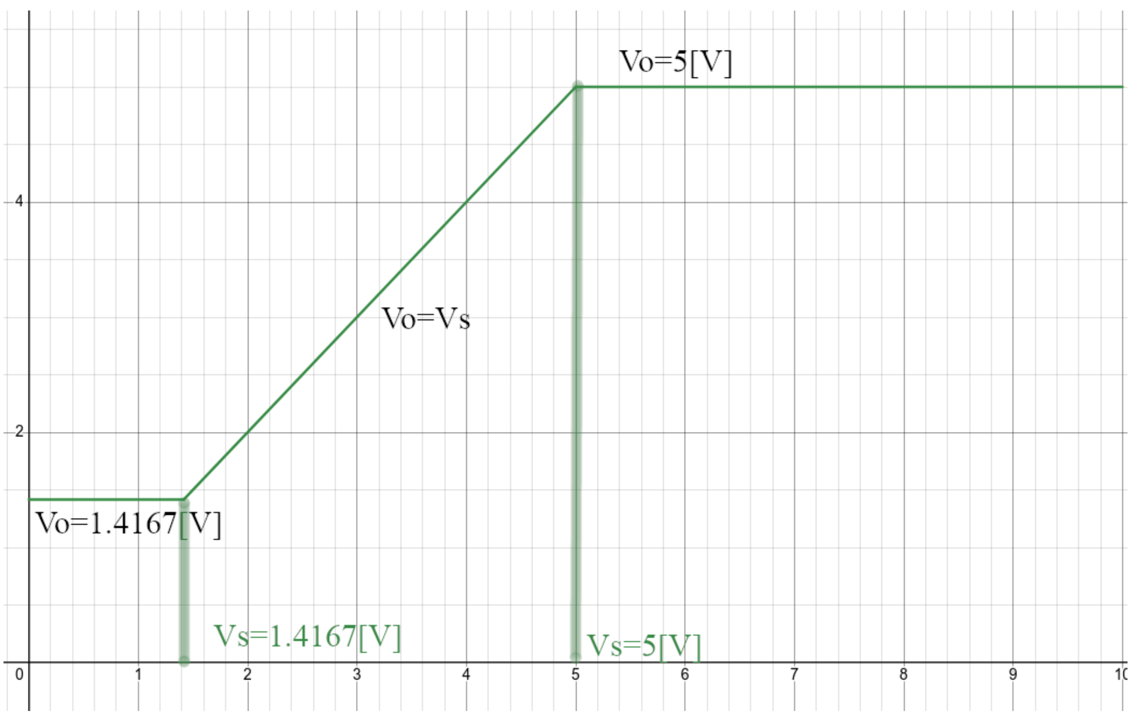

Figure 10: Transfer Characteristics of Given Circuit

5. We begin by generating the schematic:

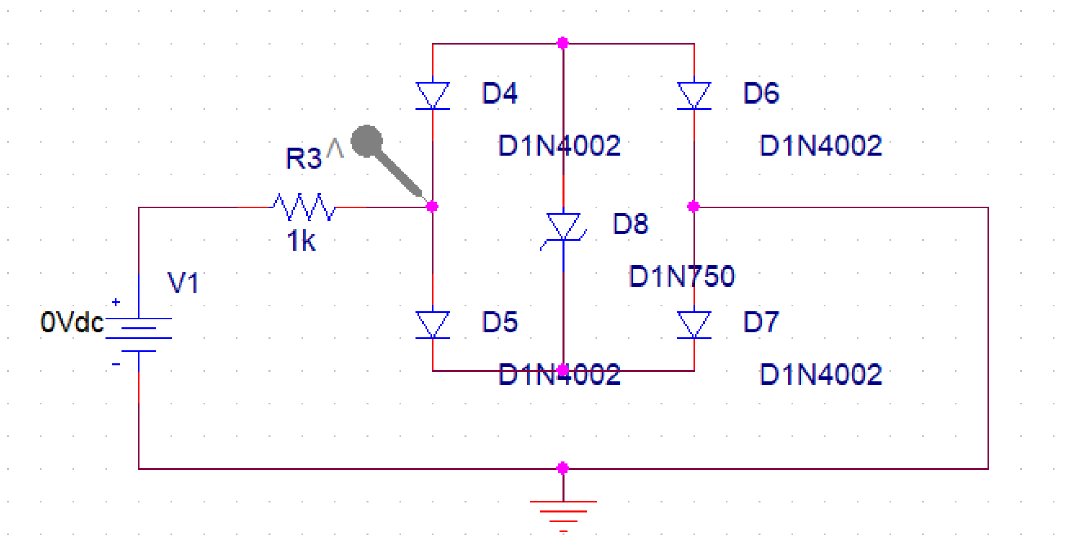

Figure 11: Schematic for DC Sweep

From here, we can simulate with the range $-15 \leq V_{in} \leq 15$:

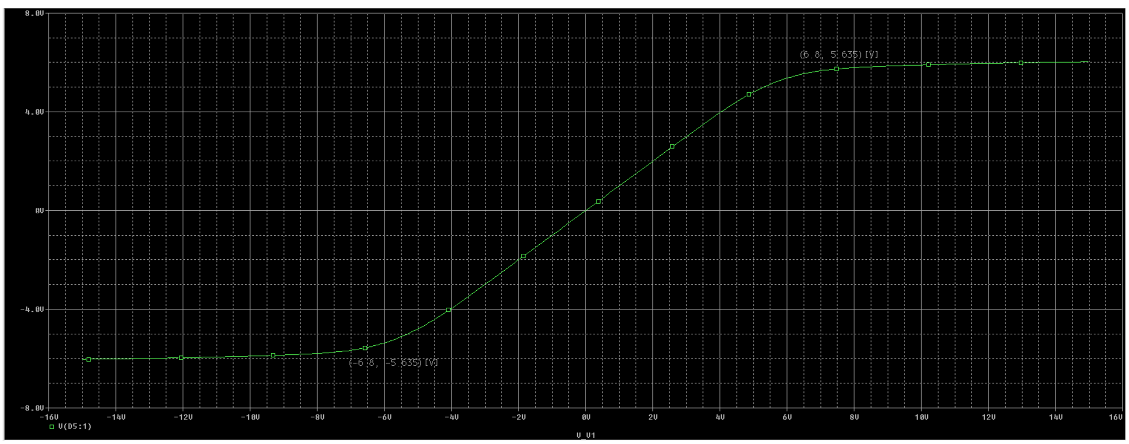

Figure 12: DC Sweep Transfer Characteristics

With the sweep, we may see that the maximum voltage magnitude is approximately 6[V], as expected for the circuit. Furthermore, the knee values occur at, approximately, the voltage value of the zener diode, or $V_z = 6.8$[V]. We can test the same circuit with an AC input:

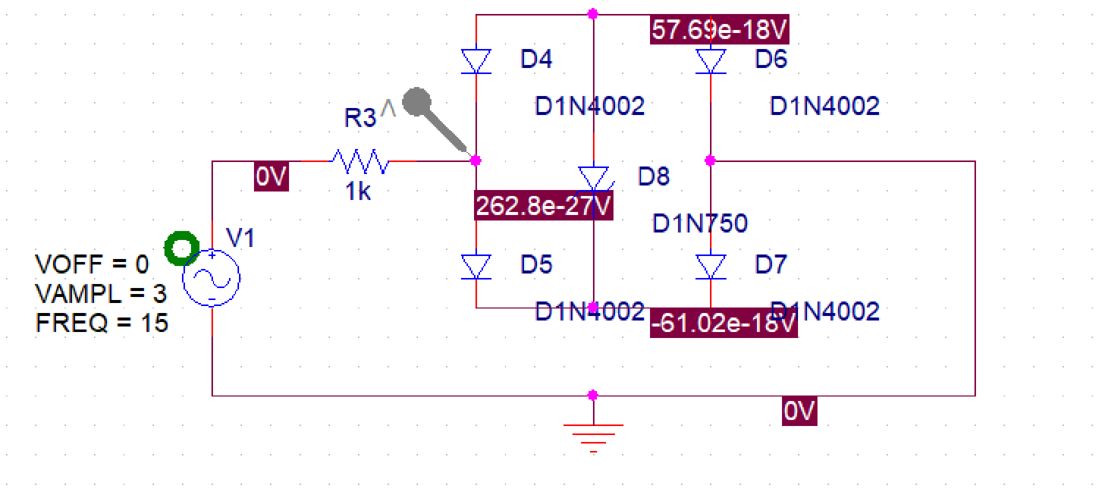

Figure 13: Schematic for AC Sweep

Using this circuit, we obtain the results for a wave with magnitude 3[V] and 12[V]:

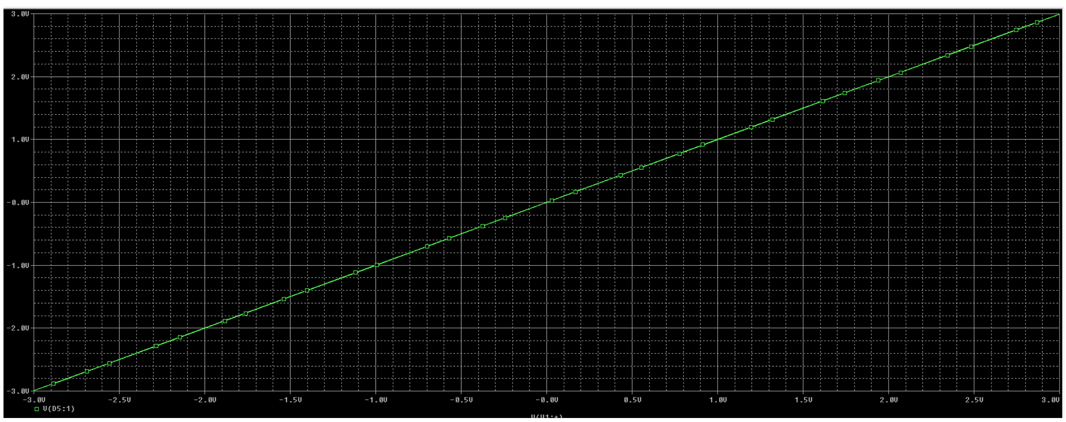

Figure 14: Transfer Characteristics for 3[V] Amplitude Input

Figure 15: Transfer Characteristics for 12[V] Amplitude Input

We may note that, for the 3[V] amplitude, the transfer characteristics are a perfect line, with a slope of 1. This is due to the fact that ± 3[V] is within the permitted voltage range of the diodes; however, the 12[V] amplitude exceeds the ± 6[V] input range. This causes the curve to become 'S' shaped, where it tapers off as the magnitudes approach 6[V]. Furthermore, note that the knee values occur at the same points, indicating that, for diodes, only the magnitude, and not frequency, of the input make a difference.