Homework 2

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1. We may begin to write KCL equations for the circuit. Let us call the voltage at the negative (upper) terminal V^-, the voltage at the bottom terminal V^+, and the voltages on the nodes V_1 and V_2. With this, we get:

$$\frac{V^- - V_{in}}{R} + \frac{V^- - V_1}{R} = 0$$
$$V^- = 0$$
$$V_{in} = -V_1$$

We write the next KCL:

$$\frac{V_1 - V^-}{R} + \frac{V_1}{R} + \frac{V_1 - V_2}{R} = 0$$
$$\frac{2V_1}{R} + \frac{V_1 - V_2}{R} = 0$$
$$V_2 = -3V_1$$

And finally the last KCL:

$$\frac{V_2 - V_1}{R} + \frac{V_2}{R} + \frac{V_2 - V_o}{R} = 0$$
$$3V_2 - V_1 = V_o$$

Combining with our first two KCL equations, we get:

$$-8V_{in} = V_o$$
$$\boxed{\frac{V_o}{V_{in}} = -8}$$

2. (a) We may begin by setting up equations per KVL:

$$\frac{V_s + V_i}{R_1} + \frac{V_o + V_i}{R_2} + \frac{V_i}{R_{in}} = 0$$
$$\frac{V_o + V_i}{R_2} + \frac{V_o - A_{OL}V_i}{R_o} = 0$$

We use these equations to solve for V_s and V_o, respectively:

$$V_o = \frac{R_2 A_{OL} - R_o}{R_o + R_2} V_i$$
$$V_s = \left[\left(\frac{R_1}{R_2}\right)\left(\frac{R_2 A_{OL} - R_o}{R_o + R_2}\right) + \left(1 + \frac{R_1}{R_2} + \frac{R_1}{R_{in}}\right)\right]$$

Substituting our known values, we get:

$$V_o = -9.9751 \cdot 10^4 V_i$$

And then we substitute this to get:

$$V_s = 9976.2V_i$$

Finally, to find the gain, we take:

$$\boxed{\frac{V_o}{V_s} \approx -10}$$

(b) We can see that the circuit may be written as:

$$V_s + R_1 i_s = -V_i$$

We can also develop:

$$V_i + (R_1 + R_o)\left[\frac{V_i}{R_{in}} + i_s\right] + A_{OL}V_i = 0$$

To find the impedance, we can use:

$$Z_{in} = \frac{V_s}{i_s}$$

We then use the first two equations to solve:

$$V_s + R_1 i_s - (R_1 + R_o)\left[\frac{V_s - R_1 i_s}{R_{in}} + i_s\right] + A_{OL}(V_s - R_1 i_s) = 0$$
$$\frac{V_s}{i_s} = -\frac{R_1 R_{in} + (R_1 + R_o)\left[R_{in} - R_1\right] - A_{OL} R_1 R_{in}}{R_{in} + R_1 + R_o + A_{OL} R_{in}}$$

We substitute known values to get:

$$\boxed{Z_{in} = 998[\Omega]}$$

For an ideal op-amp $A_{OL} \to \infty$, which gives us:

$$\boxed{Z_{in} = R_1 = 1000[\Omega]}$$

(c) To find the output impedance, we need to imagine we add a test voltage source, say V_t, which drives a test voltage, i_t back into the circuit. This would give us:

$$V_i = \frac{\left(\frac{1}{R_{in}} + \frac{1}{R_1}\right)^{-1}}{R_2 + \left(\frac{1}{R_{in}} + \frac{1}{R_1}\right)^{-1}} V_t$$

$$i_t = -\frac{V_t}{R_2 + \left(\frac{1}{R_{in}} + \frac{1}{R_1}\right)^{-1}} - \frac{V_t - A_{OL}V_i}{R_o}$$

We know that the input impedance will be the ratio of the test voltage to the test current. Thus, we insert V_i into the second equation:

$$i_t = -\frac{V_t}{R_2 + \left(\frac{1}{R_{in}} + \frac{1}{R_1}\right)^{-1}} - \frac{V_t - A_{OL}\left[\frac{\left(\frac{1}{R_{in}}+\frac{1}{R_1}\right)^{-1}}{R_2+\left(\frac{1}{R_{in}}+\frac{1}{R_1}\right)^{-1}} V_t\right]}{R_o}$$

$$\frac{i_t}{V_t} = -\frac{1}{R_2 + \left(\frac{1}{R_{in}} + \frac{1}{R_1}\right)^{-1}} - \frac{1 - A_{OL}\left[\frac{\left(\frac{1}{R_{in}}+\frac{1}{R_1}\right)^{-1}}{R_2+\left(\frac{1}{R_{in}}+\frac{1}{R_1}\right)^{-1}}\right]}{R_o}$$

$$\frac{V_t}{i_t} = -\left[\frac{1}{R_2 + \left(\frac{1}{R_{in}} + \frac{1}{R_1}\right)^{-1}} - \frac{1 - A_{OL}\left[\frac{\left(\frac{1}{R_{in}}+\frac{1}{R_1}\right)^{-1}}{R_2+\left(\frac{1}{R_{in}}+\frac{1}{R_1}\right)^{-1}}\right]}{R_o}\right]^{-1}$$

We then plug in known values to get:

$$\frac{V_t}{i_t} = -\left[\frac{1}{10^4 + \left(\frac{1}{10^6} + \frac{1}{10^3}\right)^{-1}} + \frac{1 - 10^5\left[\frac{\left(\frac{1}{10^6}+\frac{1}{10^3}\right)^{-1}}{10^4+\left(\frac{1}{10^6}+\frac{1}{10^3}\right)^{-1}}\right]}{25}\right]^{-1}$$

$$\boxed{Z_o = 2.753 \cdot 10^{-3}[\Omega]}$$

For $A_{OL} \to \infty$, we see that the whole expression becomes zero, as would be expected for the output impedance of an ideal op-amp.

3. (a) We begin by calculating the impedance from the capacitor:

$$z_c = -\frac{j}{\omega C}$$

We can tell that the output voltage is:

$$V_o = A_{OL}V^-$$

From here, we apply KCL:

$$j\omega C(V^- - V_i) + \frac{V^- - V_o}{R} = 0$$

And substitute from the equation above:

$$j\omega RC(V^- - V_i) + V^- - A_{OL}V^- = 0$$

$$j\omega RCV_i = j\omega RCV^- + V^- - A_{OL}V^-$$

This gives us the input voltage:

$$V_i = V^- + \frac{V^- - A_{OL}V^-}{j\omega RC}$$

$$V_i = \frac{j\omega RCV^- + V^- - A_{OL}V^-}{j\omega RC}$$

$$V_i = \frac{V^-(j\omega RC + 1 - A_{OL})}{j\omega RC}$$

We then take the ratio of the output to input and find the closed loop voltage gain:

$$A_{CL} = \frac{V_o}{V_i}$$

$$\boxed{A_{CL}(j\omega) = \frac{j\omega RCA_{OL}}{1 + j\omega RC - A_{OL}}}$$

(b) With an ideal op-amp, we know $A_{OL} \to \infty$. Thus, we may refactor our finding from (a) to write:

$$A_{CL}(j\omega) = \frac{j\omega RC}{(1/A_{OL})(1 + j\omega RC) - 1}$$

We know that, as $A_{OL} \to \infty$, $1/A_{OL} \to 0$, which gives us:

$$A^i_{CL}(j\omega) = -j\omega RC$$

This gives us a magnitude of:

$$\boxed{|A^i_{CL}(j\omega)| = \omega RC}$$

We may generate a bode plot for this differentiator, which would look like:

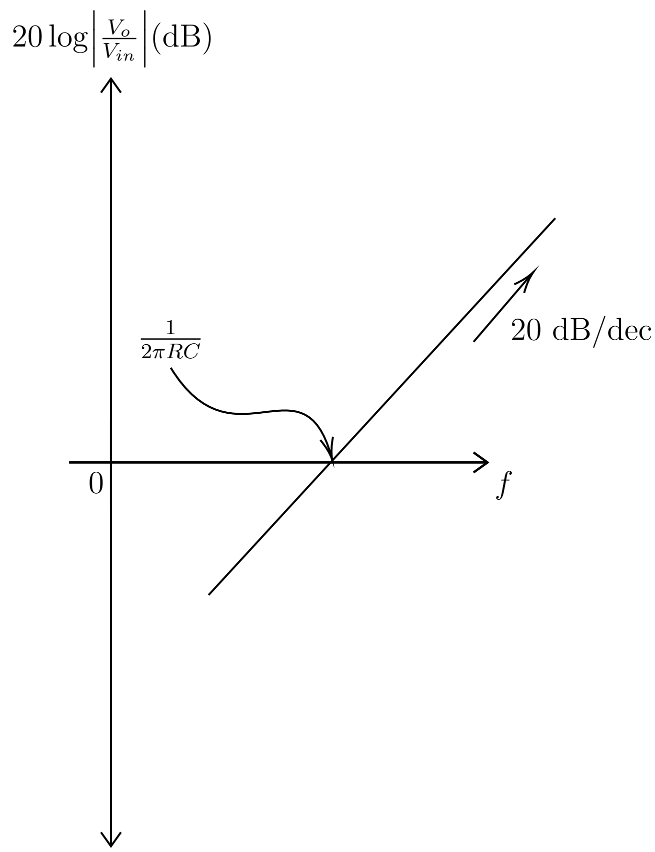

Figure 1: Bode Plot for Ideal Differentiator

And the phase plot is:

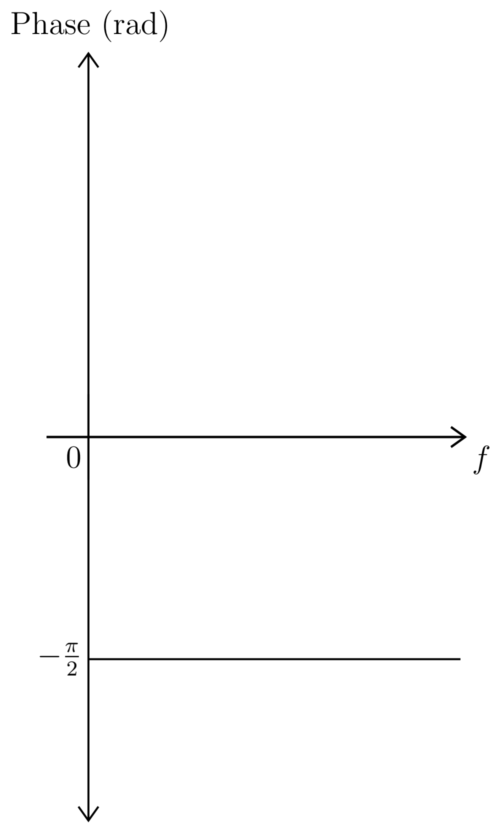

Figure 2: Phase Plot for Ideal Differentiator

(c) Using our equation from part (a), we may write:

$$A_{CL} = \frac{j(1000\pi)(10000)(20 \cdot 10^{-6})(10^4)}{1 + j(1000\pi)(10000)(20 \cdot 10^{-6}) - 10^4}$$

$$A_{CL} = \frac{j(1000\pi)(100)(20)}{1 + j(10\pi)(20) - 10^4}$$

$$A_{CL} = \frac{(2 \cdot 10^6)\pi j}{j(200\pi) - 9999}$$

$$A_{CL} = 39.331 - 625.910j$$

Now we find the magnitude:

$$|A_{CL}| = \sqrt{39.331^2 + 625.910^2}$$

$$|A_{CL}| = 627.14$$

Now we use the input amplitude to get the output amplitude:

$$|V_o| = |A_{CL}||V_i|$$

$$|V_o| = (627.14)(5 \cdot 10^{-3})$$

$$\boxed{|V_o| = 3.1357[\text{V}]}$$

4. (a) To start, it is given that the output voltage is:

$$V_o = .1[\text{V}]$$

Offset voltage can be found using the equation:

$$V_{IO} = \left(1 + \frac{R_2}{R_1}\right)^{-1} V_o$$

$$V_{IO} = \left(1 + \frac{100}{10}\right)^{-1} (\pm .1)$$

$$V_{IO} = (11)^{-1} (\pm .1)$$

$$\boxed{V_{IO} = \pm .00909[\text{V}]}$$

(b) The input bias current may be written as:

$$I_B = \frac{I_B^+ + I_B^-}{2}$$

Using KVL, we may write:

$$V_o - V^- = I_B^- R_2$$

Since the DC input voltage is zero, we know:

$$V^- = V^+ = 0$$

Therefore, we get:

$$V_o = I_B^- R_2$$

and since the terminals are balanced:

$$I_B^- = I_B^+$$

Which gives us:

$$I_B^- = \frac{V_o}{R_2}$$

$$I_B^- = \frac{\pm .1}{100000}$$

$$\boxed{I_B = I_B^- = I_B^+ = 1 \cdot 10^{-6}[\text{A}]}$$

(c) We need to place a compensating resistor on the positive terminal to ground in order to cancel the effects. This gives us:

$$V^+ = -I_B^+ R_c$$

Applying KCL, we find:

$$I_B^- = -\frac{V^-}{R_1} + \frac{V_o - V^-}{R_2}$$

$$I_B^- = -V\left[10^{-4} + 10^{-5}\right]$$

$$I_B^- = .00011 I_B^+ R_c$$

Since the two bias currents equal each other, we get:

$$1 = .00011 R_c$$

$$\boxed{R_c = 9090.9[\Omega]}$$

(d) The maximum offset current may be found using:

$$I_o = \frac{V_o}{R_2}$$

Using our known values, we substitute:

$$I_o = \frac{\pm .1}{10^5}$$

$$\boxed{I_o = \pm 1 \cdot 10^{-6}[\mathrm{A}]}$$

5. (a) The slew rate may be defined as:

$$SR = \left|\frac{dV_o}{dt}\right|$$

Since we know this is a triangular wave, we can identify the slope by simply using rise over run. This means that the rise would be 4[V] and the run is $.5(10^{-6})$. This gets us:

$$SR = \frac{4}{.5 \cdot 10^{-6}}$$

$$\boxed{SR = 8 \cdot 10^6 \left[\frac{\mathrm{V}}{\mathrm{s}}\right]}$$

(b) The full power bandwidth can be defined using:

$$V_o(t) = V_{max}\sin(\omega t)$$

Taking the derivative, we obtain:

$$\frac{dV_o(t)}{dt} = \omega V_{max}\cos(\omega t)$$

Since this differential is the slew rate, we write:

$$SR = 2\pi f_{fp} V_{max}\cos(\omega t)$$

We use the magnitude to get:

$$\frac{8\cdot 10^6}{2\pi V_{max}} = f_{fp}$$

$$f_{fp} = \frac{8\cdot 10^6}{2\pi V_{max}}$$

$$\boxed{f_{fp} = 6.3662\cdot 10^5[\mathrm{Hz}]}$$

(c) Since 5[MHz] is greater than the full-power bandwidth defined in part (b), the waveform outputted can not correspond to the full peak-to-peak value of 4[V]. Thus, the output would be transformed from sinusoidal to, most likely, a triangular wave.

6. The following schematic was used to simulate the plots below:

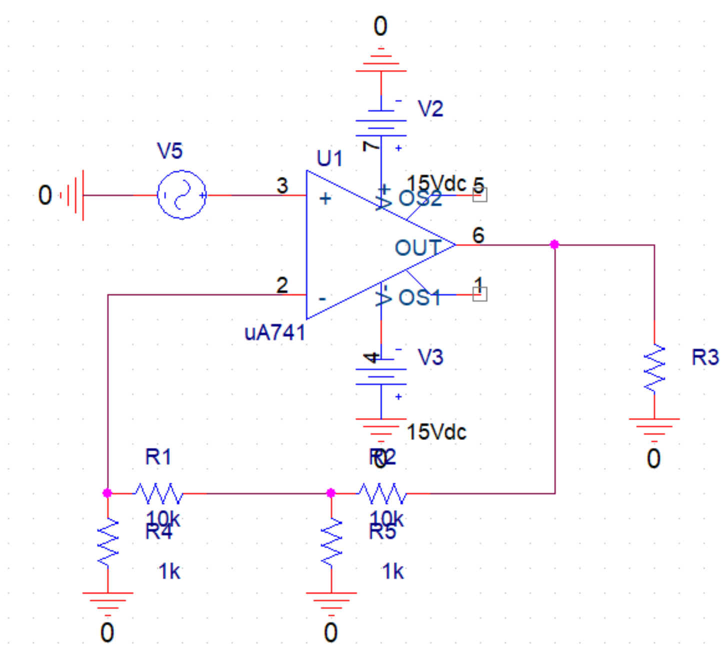

Figure 3: Schematic for Simulation

(a) See plot in Figure 3 below:

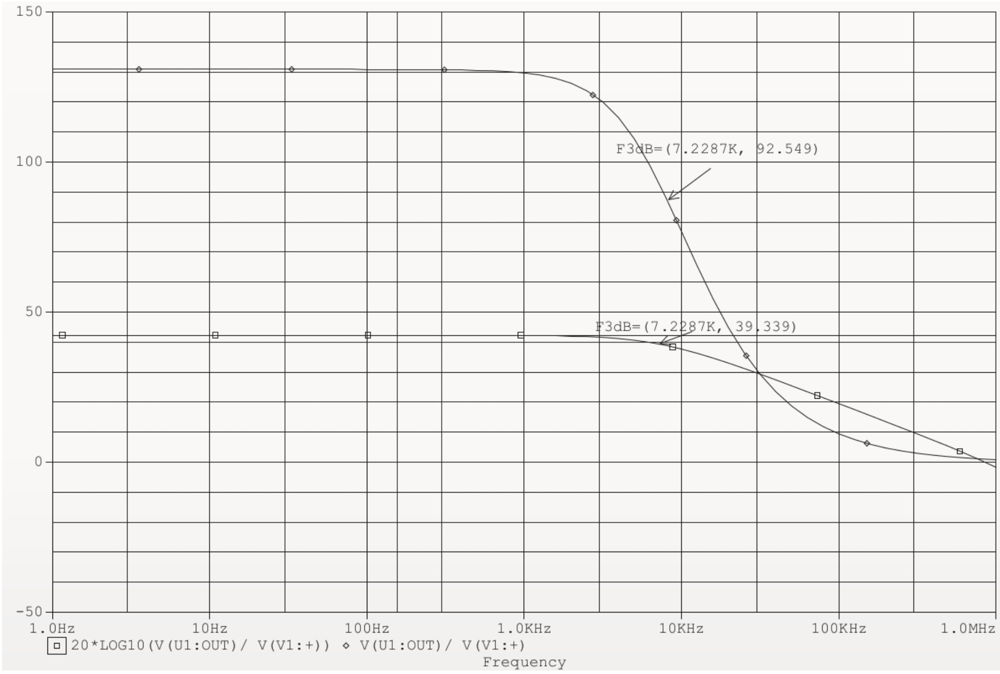

Figure 4: AC Gain (dB and Magnitude) vs. Frequency

Note: the critical frequency is, approximately, 7.2[kHz]

(b) Note: from this point onwards, the output voltage, V_o, uses axis 1, while the input, V_i, uses axis 2. See plot in Figure 5 below:

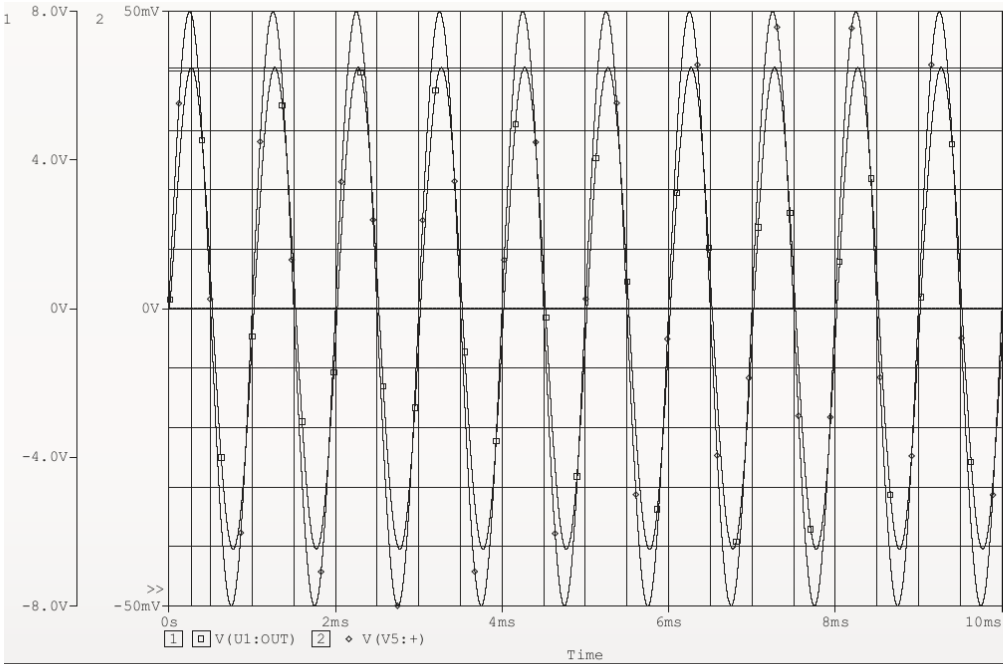

Figure 5: V_o and V_i vs. Time ($V_i = .05$[V] at 1[kHz])

We may notice that the phases are almost identical; however, the magnitude is significantly different. While the input is at the expected 50[mV], the output is approximately 6.5[V] in amplitude. Thus, we can calculate the gain as:

$$\boxed{A = \frac{6.5}{50 \cdot 10^{-3}} = 130 \left[\frac{\text{V}}{\text{V}}\right]}$$

(c) See plot in Figure 6 below:

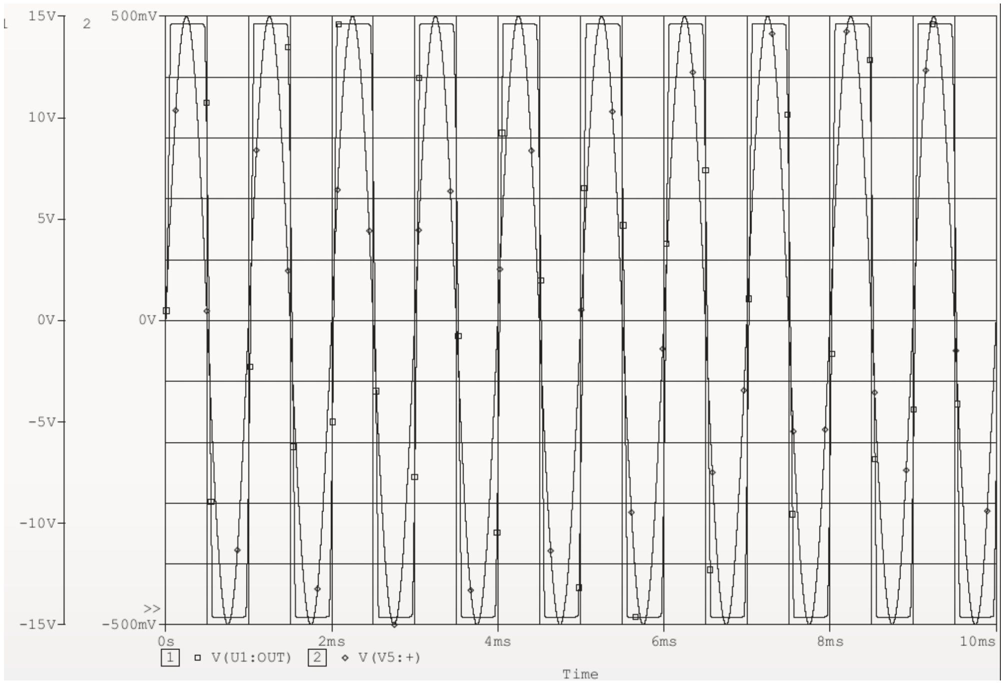

Figure 6: V_o and V_i vs. Time ($V_i = .5$[V] at 1[kHz])

For this plot, we see that, as the output approaches a magnitude of 15[V], it begins to form a square wave. This is to be expected, as a 15[V] output would saturate the op-amp due to being equivalent to the op-amp DC power supplies. Thus, the output is unable to extend beyond this magnitude, forming the square wave, as would be expected.

(d) See plot in Figure 7 below:

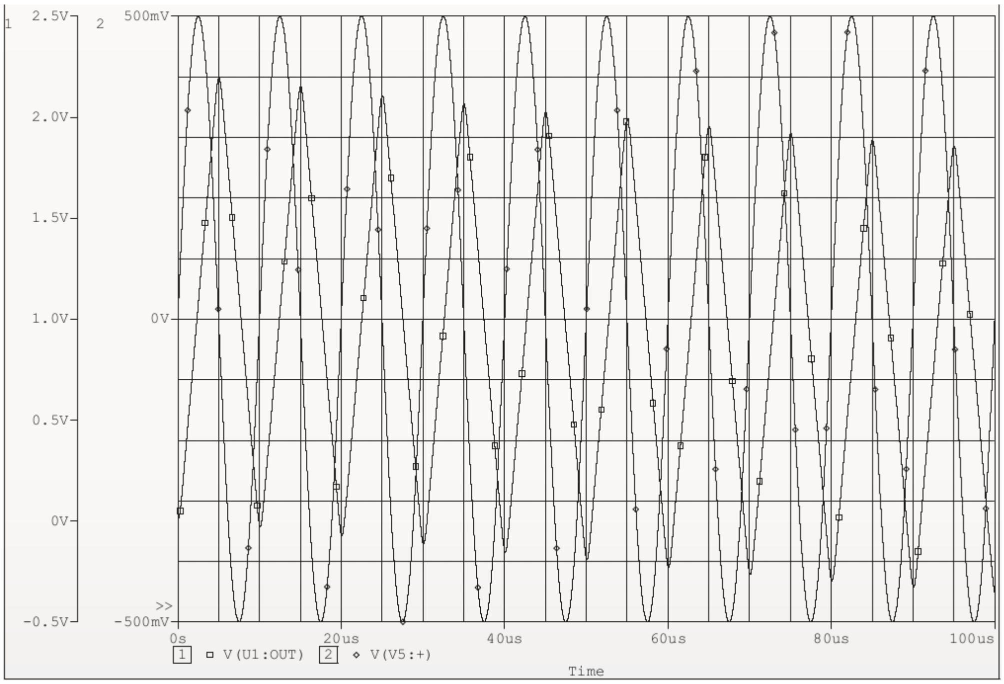

Figure 7: V_o and V_i vs. Time ($V_i = .5$[V] at 100[kHz])

We see that the output begins forming a triangle wave, instead of a sinusoid. Furthermore, the amplitude of the resulting triangle wave is less than would be expected for the gain. The former may be attributed to the slew rate of the op-amp, which, evidently, is less than the input frequency. As a result, the internal capacitors of the op-amp are unable to adjust to the oscillating voltage quickly enough, thus forming a triangle wave. The latter may be attributed to the fact that, as exemplified in Figure 4, the critical frequency (3dB frequency) occurs at 7.2[kHz], which would mean that, at 100[kHz], the op-amp would not output a gain that would be nearly as high as expected.

(e) See plot in Figure 8 below:

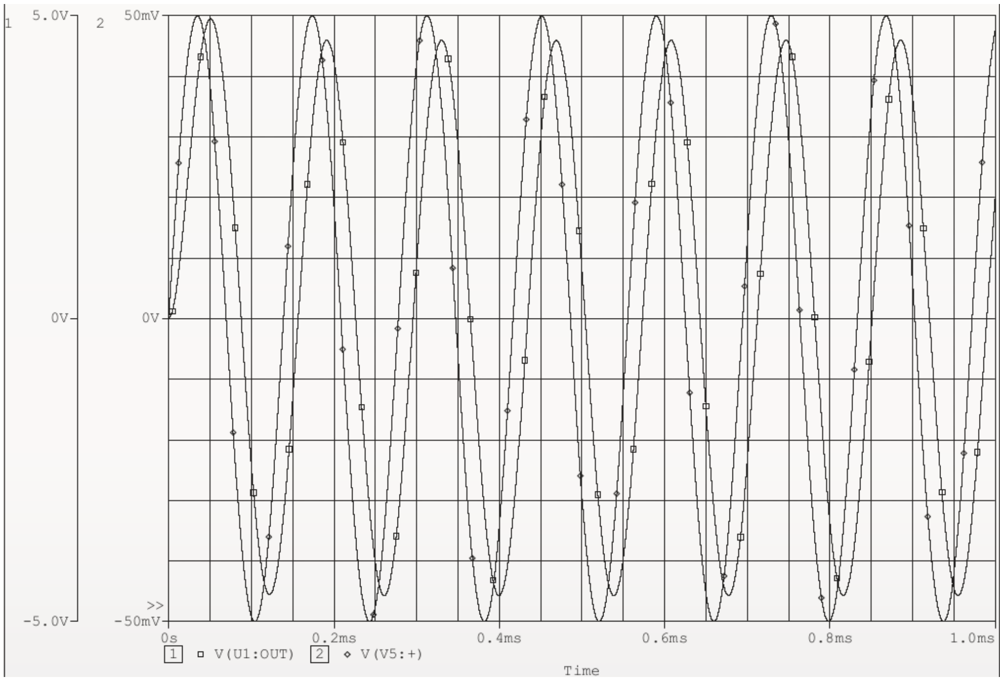

Figure 8: V_o and V_i vs. Time ($V_i = .05$[V] at 7.2[kHz])

In the figure, we see that, at a frequency of 7.2[kHz], the op-amp does not output a gain that is as high as at a frequency of 1[kHz]. This is due to the fact that, as shown in Figure 4, the critical frequency is at, approximately, 7.2[kHz]. Looking at Figure 4, we would expect that the gain would be around 92.5[V/V], as demarcated by the $F_{3\text{dB}}$ point. Calculating per the Figure 8, we get:

$$\boxed{A = \frac{4.59}{50 \cdot 10^{-3}} = 91.8 \left[\frac{\text{V}}{\text{V}}\right]}$$

This value is approximately the expected value.