Lecture 13

Michael Brodskiy
Professor: M. Onabajo

October 31, 2024

- General Amplifier Analysis Procedure
  - DC bias circuit analysis/design
    - Consider only DC sources (remove AC sources)
    - Ensure operation in the active region
    - Take desired Q-point parameters into account (g_m, r_π, etc.)
  - AC Analysis
    - Draw the AC equivalent circuit with the appropriate BJT model
    - Consider only AC sources (remove DC sources)
    - Midband (medium-frequency AC analysis):
      - Capacitor $\rightarrow$ short-circuit, inductor $\rightarrow$ open-circuit
    - Frequency-dependent analysis
      - Capacitor and inductor go to their frequency-dependent impedances
  - Removal of Sources
    - Voltage source $\rightarrow$ replace with a short-circuit
    - Current source $\rightarrow$ replace with an open-circuit
- The Early Effect (BJT Output Resistance)
  - As V_C increases, the depletion width of the B-C junction widens
- The Darlington Pair Configuration
  - Two transistors, cascaded with the second's base connected to the first's emitter
  - $\beta_{eff} = \beta_1 + \beta_2 + \beta_1\beta_2 \approx \beta_1\beta_2$
  - $V_{BEeff} = V_{BE1}+_{BE2} \approx 2V_{BE1}$
  - For active mode: $V_{CE} > V_{BE2} + V_{CE1(min)}$

- Current Sources
  - Ideal
    - An ideal source will tolerate any voltage (V_z) across its terminals
    - Infinite output resistance
  - Practical
    - A minimum compliance voltage must be maintained to guarantee a certain output current: $V_z > V_{comp}$
    - Finite output resistance
- Current Mirror concept
  - Often, a "golden current source" is replicated at multiple locations on the chip or printed circuit board (PCB)
  - Integrated circuit applications
    - I_{REF} can be on the chip or outside of the chip
    - Accurate reference (I_{REF}) generation is costly (expensive components or requirement for a lot of chip area)
    - The use of current mirrors is more efficient than generating multiple reference currents
- BJT as a Current Source
  - Requirements for a reliable collector current:
    - A fixed V_{BE} must be generated
    - The BJT should operate in the active region ($V_z > V_{CEmin}$)
  - A Diode-Connected BJT
    - Connect a reference current source to the collector, then short the collector to base
    - This ensures $V_C = V_B$, and forces the BJT to remain in the active region. The emitter generates Q_{ref} ("diode-connected")
    - The reference voltage generation:

$$I_C = I_S \left[e^{V_{BE}/V_T} - 1 \right] \approx I_s e^{V_{BE}/V_T}$$

$$V_1 = V_{BE} \approx V_T \ln \left(\frac{I_C}{I_S} \right)$$

- A Simple Current Mirror
  - The diode-connected Q_{ref} produces a reference voltage at the base of the diode-connect BJT

  - Connect another BJT's base to the base of the diode-connected BJT
  - $V_{em} = 0$[V] and $V_{ba} = V_x$ are identical for both BJTs
    * Forces I_{mirror} (the current into the collector of the second BJT) to be equal to the reference current I_{ref} (ignoring base currents) if $Q_1 = Q_{ref}$
    * With different BJT characteristics:

$$I_{mirror} \approx \frac{A_1}{A_{ref}} I_{ref} = \frac{I_{S1}}{I_{Sref}} I_{ref}$$

- Resistor-Transistor Logic (RTL)
  - Gives good insights into the concept of using analog transistors for digital signal processing
  - Logic states: high ("1") or low ("0")
  - RTL logic levels: V_{CC} or $\approx .2 - .3$[V]
  - Not popular anymore