

Seven-Segment Display  
Embedded Design: Enabling Robotics  
EECE2160

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### **Abstract**

The purpose of this laboratory experimentation is to fabricate and understand the process of digital logic circuits. This laboratory procedure allows for the formation of a deeper understanding of real-life digital logic applications through the integration of a seven-segment display. Optimally-minimized boolean equations were then constructed from Karnaugh maps to construct final circuit designs.

**KEYWORDS:** minimization, boolean equation, seven-segment display, optimal,  
Karnaugh map

# 1 Equipment

Available equipment included:

- DE1-SoC board
- DE1-SoC Power Cable
- USB-A to USB-B Cable
- Computer
- Quartus Prime Schematic Software

# 2 Pre-Lab

The pre-lab consisted of the construction of a truth table based on the provided scenario, as well as subsequent conversion to minimized boolean equations through the use of Karnaugh maps.

## 2.1 Truth Table

#	In3	In2	In1	In0	a	b	c	d	e	f	g
0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	1	1	0	0	1	1	1	1
2	0	0	1	0	0	0	1	0	0	1	0
3	0	0	1	1	0	0	0	0	1	1	0
4	0	1	0	0	1	0	0	1	1	0	0
5	0	1	0	1	0	1	0	0	1	0	0
6	0	1	1	0	0	1	0	0	0	0	0
7	0	1	1	1	0	0	0	1	1	1	1
8	1	0	0	0	0	0	0	0	0	0	0
9	1	0	0	1	0	0	0	0	1	0	0

Table 1: Digits to display on a 7-stage display (0 for on, 1 for off)

## 2.2 Karnaugh Maps

In3In2   In1In0	00	01	11	10
00	0	1	0	0
01	1	0	0	0
11	x	x	x	x
10	0	0	x	x

Table 2: Karnaugh Map for  $A \rightarrow In2In1'In0' + In3'In2'In1'In0$

In3In2   In1In0	00	01	11	10
00	0	0	0	0
01	0	1	0	1
11	x	x	x	x
10	0	0	x	x

Table 3: Karnaugh Map for  $B \rightarrow In2In1'In0 + In2In1In0'$

In3In2   In1In0	00	01	11	10
00	0	0	0	1
01	0	0	0	0
11	x	x	x	x
10	0	0	x	x

Table 4: Karnaugh Map for  $C \rightarrow In3'In2'In1In0'$

In3In2   In1In0	00	01	11	10
00	0	1	0	0
01	1	0	1	0
11	x	x	x	x
10	0	0	x	x

Table 5: Karnaugh Map for  $D \rightarrow In2In1'In0' + In3'In2'In1'In0 + In2In1In0$

In3In2   In1In0	00	01	11	10
00	0	1	1	0
01	1	1	1	0
11	x	x	x	x
10	0	1	x	x

Table 6: Karnaugh Map for  $E \rightarrow In2In1'In0' + In0$

In3In2   In1In0	00	01	11	10
00	0	1	1	1
01	0	0	1	0
11	x	x	x	x
10	0	0	x	x

Table 7: Karnaugh Map for  $F \rightarrow In3'In2'In0 + In3'In2'In1 + In1In0$

In3In2   In1In0	00	01	11	10
00	1	1	0	0
01	0	0	1	0
11	x	x	x	x
10	0	0	x	x

Table 8: Karnaugh Map for  $G \rightarrow In3'In2'In1' + In2In1In0$

### 3 Introduction

This lab revolved around the concept of seven-segment display integration. Displays consist of seven segments (thus the name), labeled A-G. Activating a certain sequence of these segments will result in the display of a certain number. Using the truth table, Karnaugh maps, and boolean equations generated in the pre-lab, this lab will concern the formation of a schematic to display a certain 4-bit number.

First and foremost, the aforementioned boolean equations were used to fully construct a seven-segment display digital logic circuit. This logic circuit was first functionally simulated, and then tested by flipping various combinations of switches to reach a desired output.

Next, some additional logic was added to the circuit, as an extra switch, which turned the seven-segment display on or off, was added. When on, this switch would activate the display, and display numbers as usual. When off, the switch dims the display, and nothing is displayed no matter the combination of number switches used.

As a final step, the concept of the control switch was applied to each of the 6 seven-segment displays present of the DE1-SoC board, allowing for the displays to show the same number on up to 6 displays, if all of the switches were to be turned on. Each display was controlled by the switch directly below it.

### 4 Discussion & Analysis

#### 4.1 Assignment 1

The first of the assignments concerned the creation of the initial digital logic circuit. First and foremost, the equations derived in Tables 1-8 were combined to create one big circuit. This circuit is shown in Figure 1. Prior to compiling and uploading to the board, a functional simulation was run to confirm the accuracy of the circuit, which was correct. The results of the simulation are shown in Figure 2

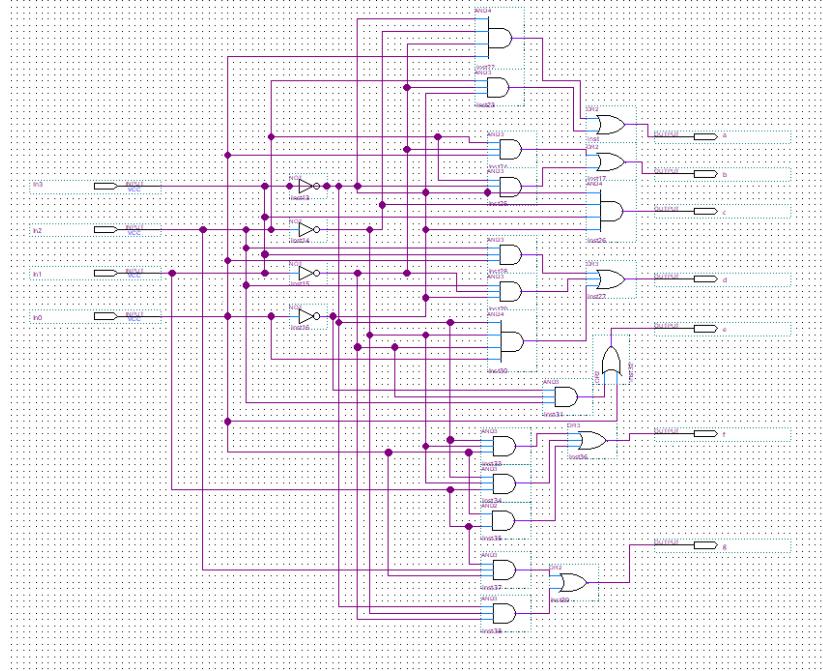


Figure 1: The Seven-Segment Single-Control Circuit

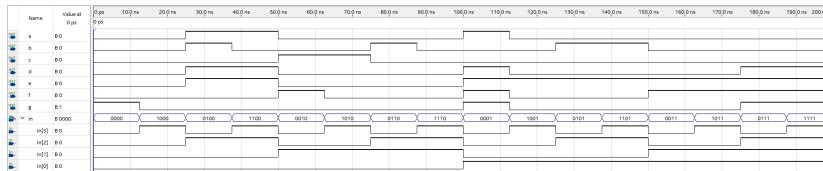


Figure 2: The Seven-Segment Single-Control Circuit Simulation

## 4.2 Assignment 2

For this assignment, the BCD system based on the derived Boolean equations created in Assignment 1 were uploaded to the DE1-SoC board for testing on the first 7-digit display (HEX0). When assigning pins, the first four inputs for switches SW[3] (PIN\_AF10), SW[2] (PIN\_AF9), SW[1] (PIN\_AC12), and SW[0] (PIN\_AB12) were assigned to be the four inputs into the system IN3, IN2, IN1, and IN0 respectively. As for the outputs (a, b, c, d, e, f, g), these were assigned to HEX0[0] (PIN\_AE26), HEX0[1] (PIN\_AE27), HEX0[2] (PIN\_AE28), HEX0[3] (PIN\_AG27), HEX0[4] (PIN\_AF\_28), HEX0[5] (PIN\_AG28), and HEX0[6] (PIN\_AH28). The results of the testing on the DE1-SoC are shown in Figures 3-12 below.

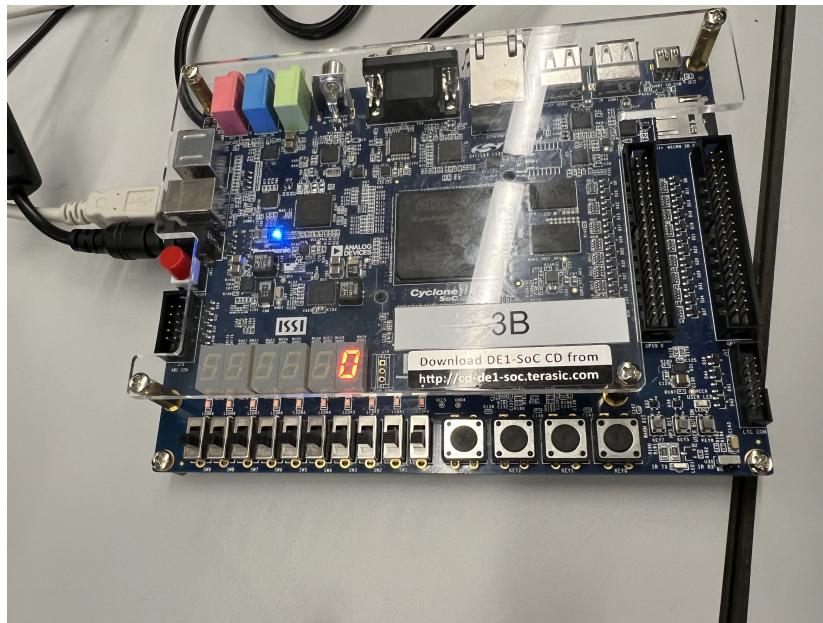


Figure 3: DE1-SoC Displaying 0 on HEX0 with no inputs

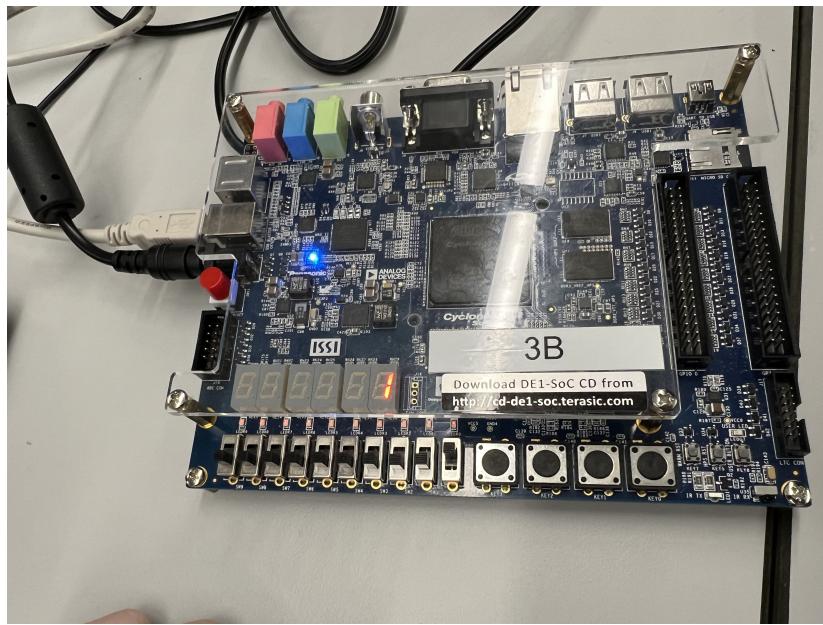


Figure 4: DE1-SoC Displaying 1 on HEX0 with input IN0

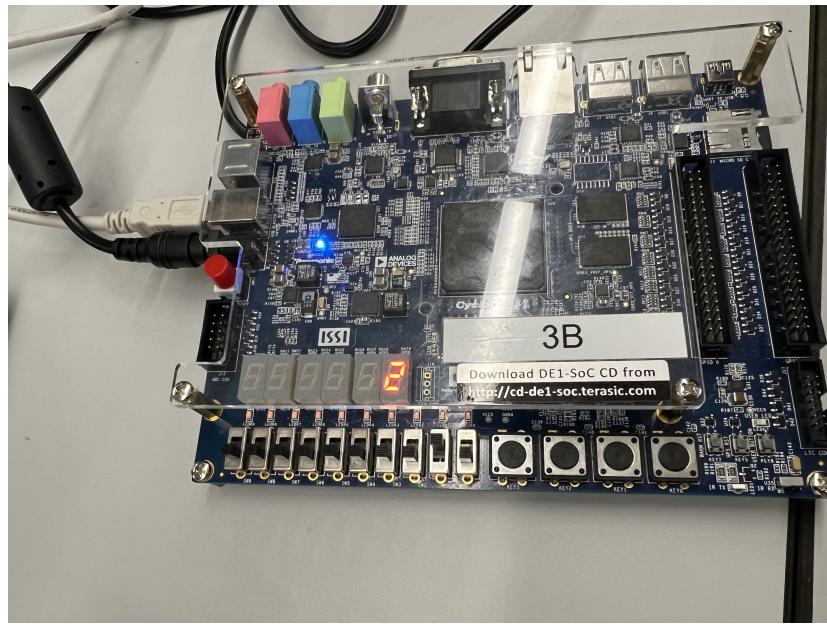


Figure 5: DE1-SoC Displaying 2 on HEX0 with input IN1

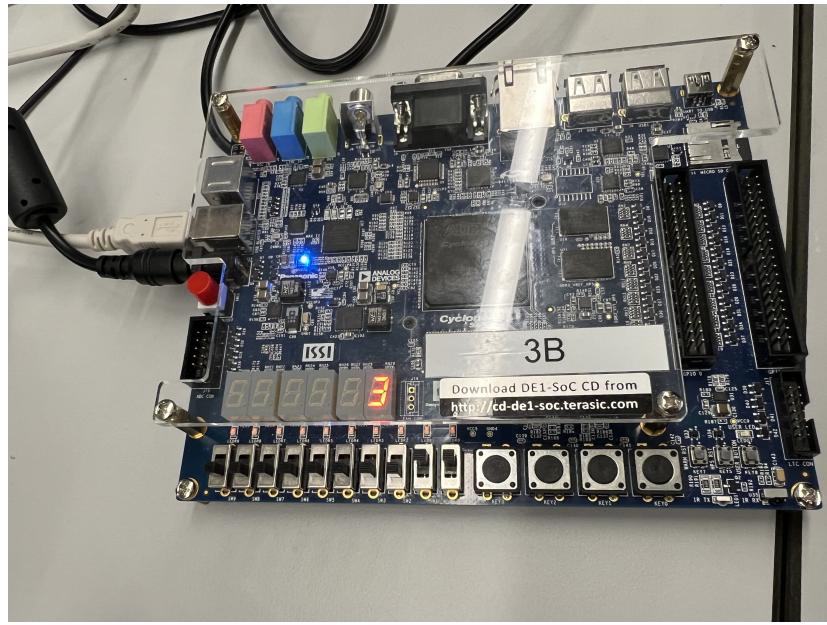


Figure 6: DE1-SoC Displaying 3 on HEX0 with input IN0 and IN1

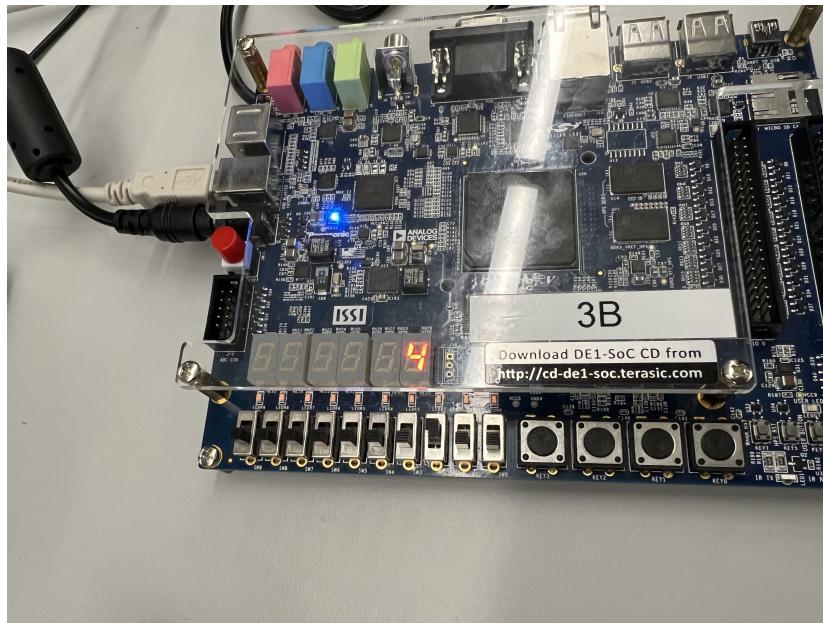


Figure 7: DE1-SoC Displaying 4 on HEX0 with input IN2

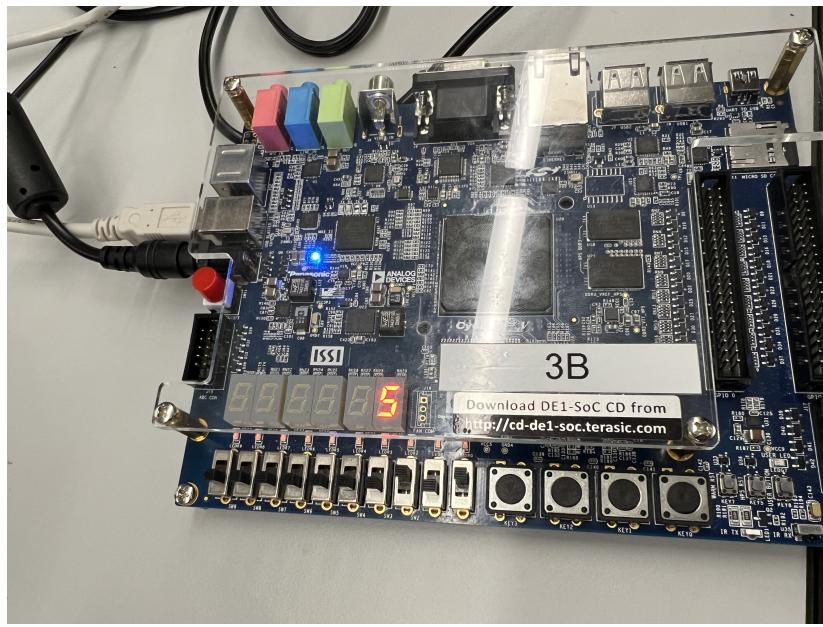


Figure 8: DE1-SoC Displaying 5 on HEX0 with input IN2 and IN0

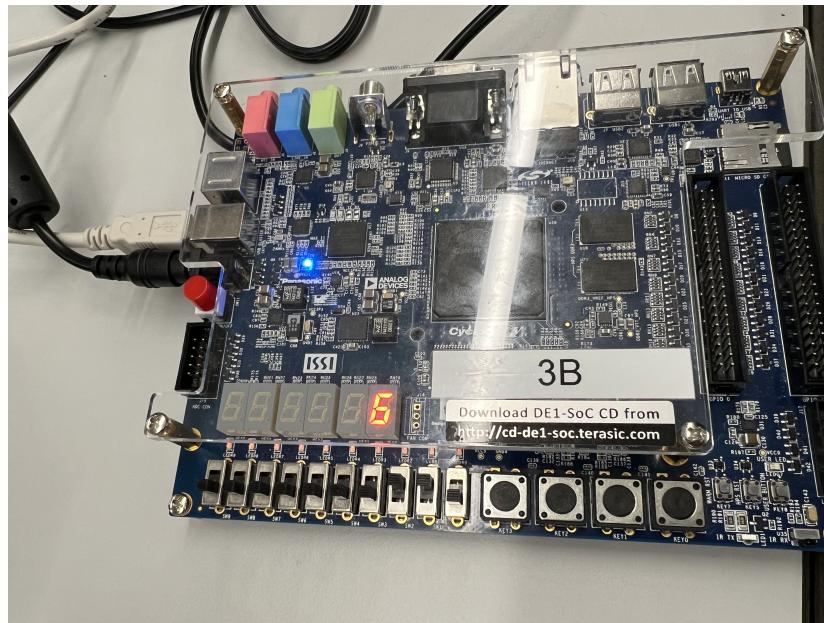


Figure 9: DE1-SoC Displaying 6 on HEX0 with input IN1 and IN2

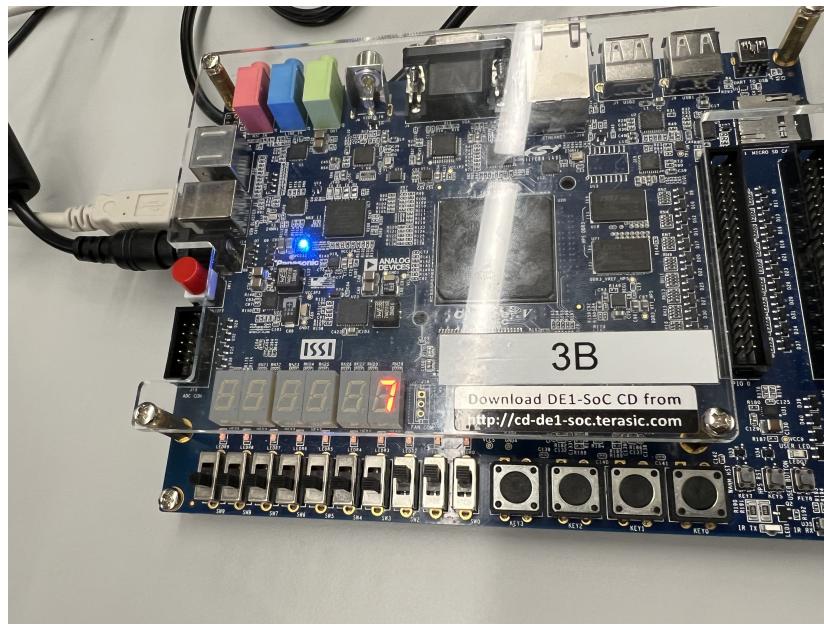


Figure 10: DE1-SoC Displaying 7 on HEX0 with input IN0, IN1, and IN2

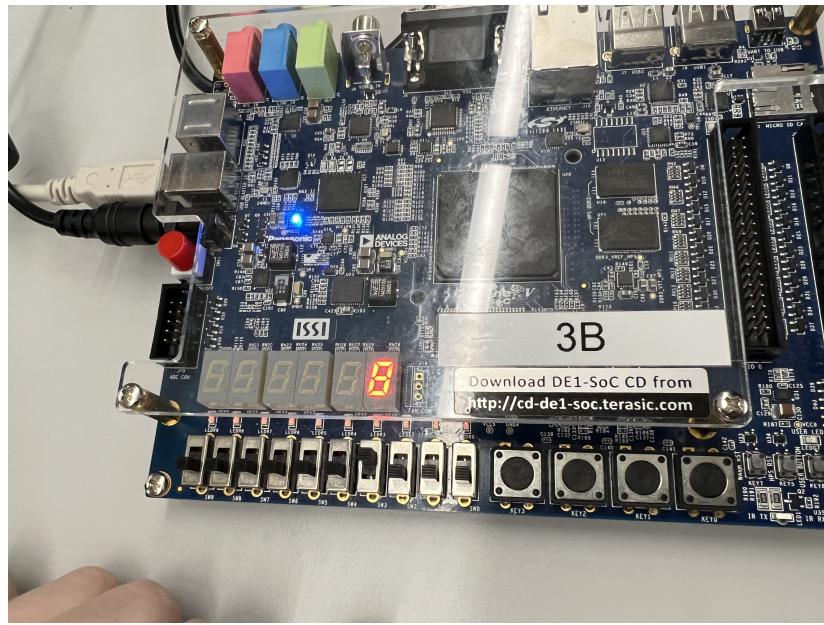


Figure 11: DE1-SoC Displaying 8 on HEX0 with input IN3

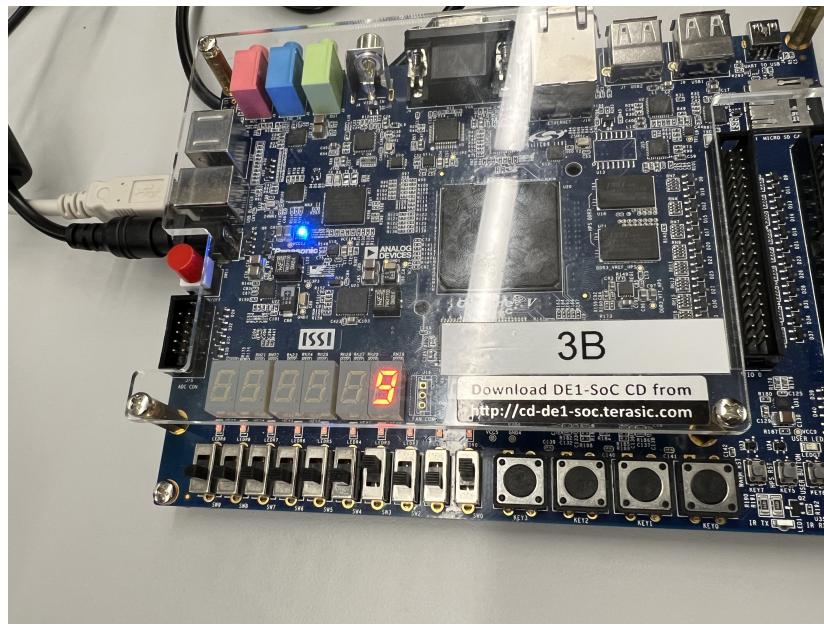


Figure 12: DE1-SoC Displaying 9 on HEX0 with input IN0 and IN3

All displayed numbers with corresponding inputs on the DE1-SoC board matched the expected outputs from the truth table.

### 4.3 Assignment 3

In Assignment 3, the goal was to have the ability for the display to be off, meaning all the segments are off, when not in use. To do this, an enable input, that acted as an on/off switch, was added into the circuit design, as shown in Figure 13 below.

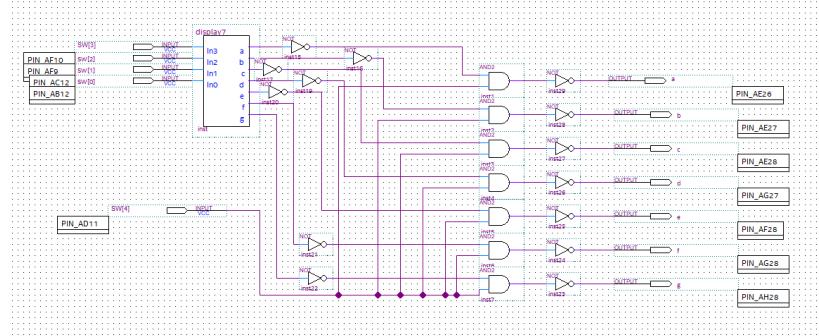


Figure 13: Compressed digital display block with additional input and logic to act as an enable switch

As can be seen in Figure 13, in order to add the enable input, the digital display design created in Assignment 1 was packed into a logic block called *display7*. The output of *display7*, which are the segments that are to be turned on, were inverted with NOT gates and inputted into separate AND gates with the enable input. Thus, all the on segments with an output of 0 are inverted to 1 and all off segments with an output of 1 were inverted to 0. In the case of the enable input being 0, the on segments (now 1's) going into the AND gate with the enable input of 0, will output all 0. Additionally, all the off segments (now 0's) go into the AND gate with the enable input of 0, which will output all 0. However, 0 designates that a segment is on, so additional NOT gates were added after the AND gates to invert all 0's to 1's. To adequately test this circuit, a simulation was run with the Waveform Simulation software. The results of the simulation are shown in Figure 14.

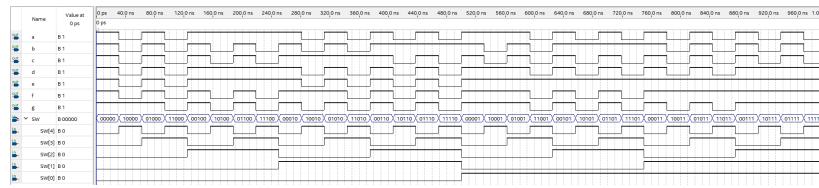


Figure 14: Waveform Simulation Results With an Enable Input (SW[4])

#### **4.4 Assignment 4**

### **5 Conclusion**