Adders, Subtractors, & Multipliers

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- The Half Adder
  - Specification
    - 2 Inputs (X, Y)
    - 2 Outputs (C, S)

X	Y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

- The Full Adder
  - A combinational circuit that adds 3 input bits to generate a sum bit and a carry bit ("half adder with carry in")
  - Specification:
    - Three Inputs (X, Y, Z)
    - Two Outputs (S, C)

X	Y	Z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

- Implementations of Multi-bit Adders:
  - Ripple Carry Adder
    - The carry ripples from one column to the next, and then from one stage to the next
    - Composed of n 1-bit full adders
    - Carries ripple from LSB stage to MSB stage
      - Delay: $n\cdot$ (delay of single FA stage)
      - Area required is linear in n
  - 4-bit Ripple Carry Adder
    - Composed of 4 1-bit Full Adders
  - Assume gate delay $= T$ nanoseconds

  - $8T$ to compute the last carry
  - Total delay $= 8 + 1 = 9T$
  - 1 delay from first half adder

- An adder/subtractor is built using full adders and XOR gates
- Binary Multiplication
  - Multiplication is achieved by adding a list of shifted multiplicands according to the digits of the multiplier