Preparing for Lab One

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- For our first lab, we will be using the DE1-SoC development board

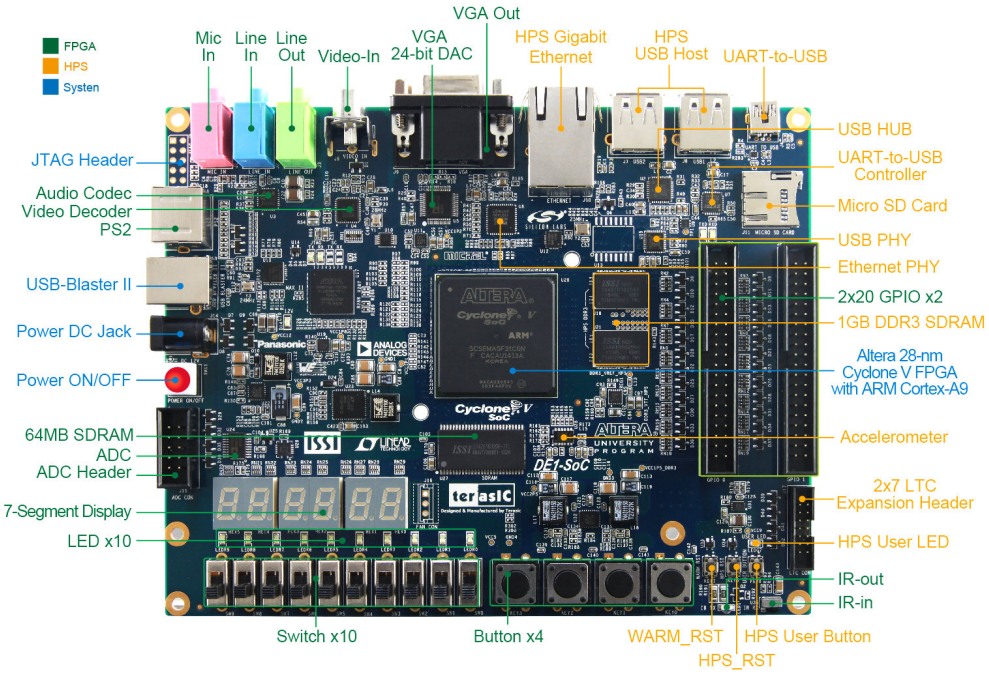

Figure 1: An example showing the top layout of a DE1-SoC board

- A VGA cable is necessary for monitor output

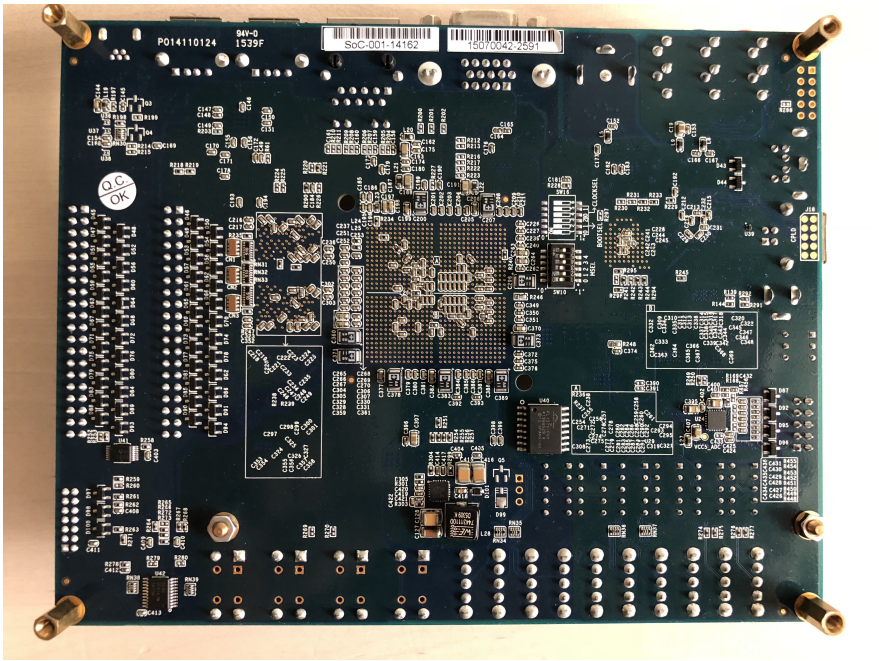

Figure 2: An example showing the bottom layout of a DE1-SoC board

- The abstract section of the lab report should essentially be the lab introduction, but in your own words
- Include pictures of the board, necessary figures, and excel or MATLAB table representations of data in lab reports
- Conclusion sums up what was learned from the lab
- References are required if outside sources were used
- In this lab we will design a circuit capable of adding two binary numbers, and we will use the Quartus Prime Schematic to simulate and validate its behavior. This tool allows you to construct complex circuits with a hierarchical schematic design, which you can then test with different artificial inputs. We will also upload our designs into the FPGA on the Intel DE1-SoC Board and verify the designs using Switches and LEDs on the board.
- A half adder is a circuit capable of adding two 1-bit numbers. The circuit has two inputs and two outputs. The circuit can add two 1-bit numbers (inputs), for example, $1_2 + 1_2 = 10_2$. We call the least significant bit as Sum, and the most significant bit as Carry for the two outputs.
- Pre-Lab Truth Table for a Half-adder Circuit:

A	**B**	**Sum**	**Cout**
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

- We will design a half-adder using Quartus Schematic and run the simulation with Waveform
- Looking at the table, the circuit will have two inputs, A and B, and two outputs, Sum and Cout
- Additionally, it is clear that the Carry requires an "and" because both A and B have to be 1, while Sum requires an "xor" because only A or B can be 1 to make it 1
- The sum can be written as Sum $= (\bar{A} \bullet B) + (A \bullet \bar{B})$
- The carry can be written as Cout $= A \bullet B$
- In this lab, we will be given the circuit drawing, but, normally, we will design the circuit ourselves
- The purpose of this lab is to understand how to draw a schematic and upload it to a board

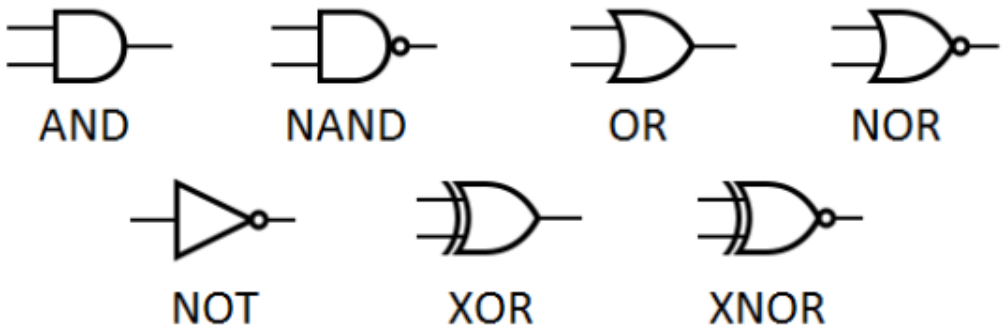

Figure 3: Logic Gate Symbols

- Once the circuit is fully designed, without error, it is necessary to test the circuit before uploading anything to the board using a simulator
- We will be using the above symbols in this project