
STM32
CubeMX

1. Description

1.1. Project

Project Name	STM32CubeMX
Board Name	B-U585I-IOT02A
Generated with:	STM32CubeMX 6.7.0
Date	01/25/2023

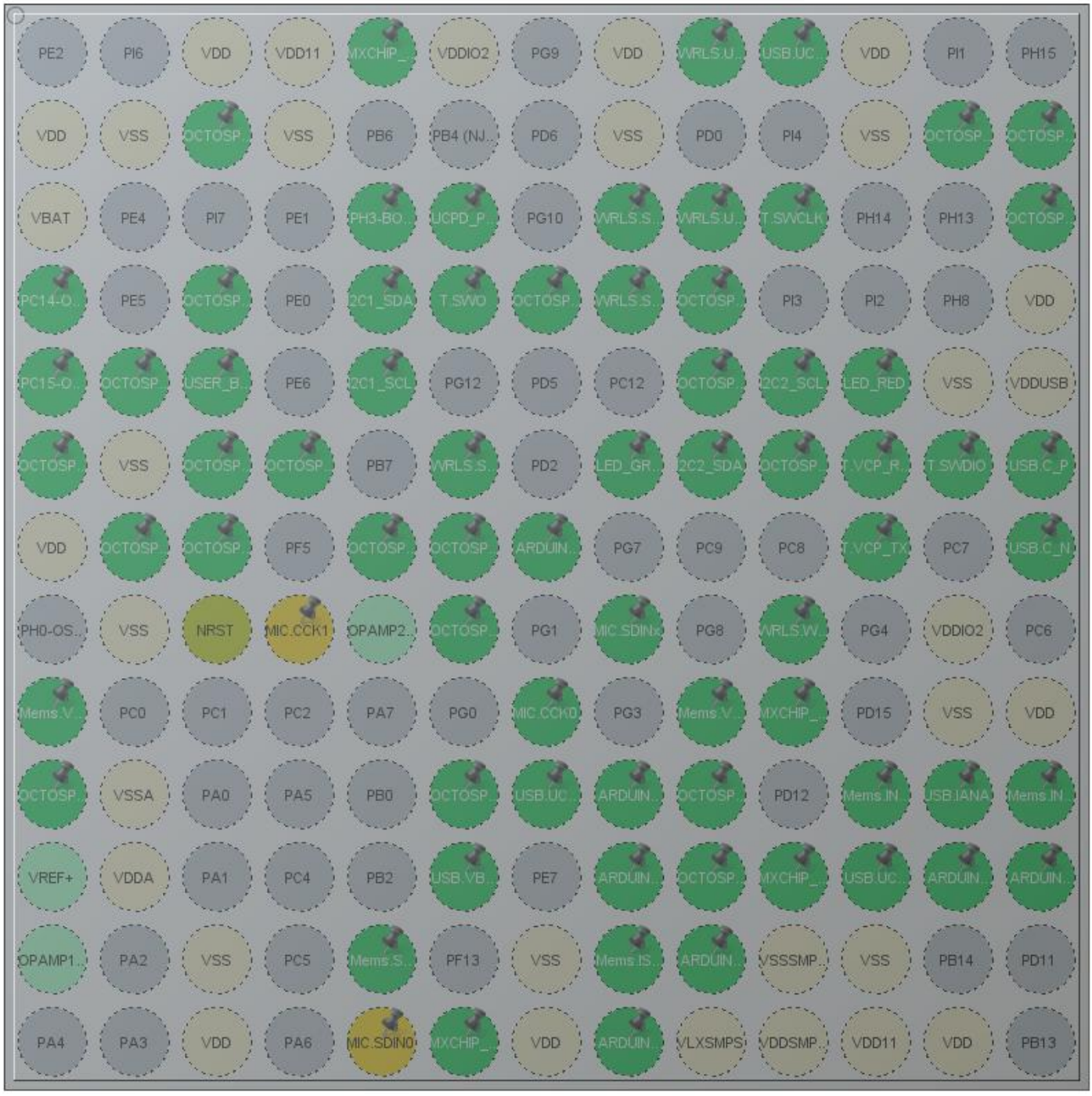
1.2. MCU

MCU Series	STM32U5
MCU Line	STM32U575/585
MCU name	STM32U585AIIxQ
MCU Package	UFBGA169
MCU Pin number	169

1.3. Core(s) information

Core(s)	ARM Cortex-M33

2. Pinout Configuration



UFBGA169 (Top view)

3. Pins Configuration

Pin Number UFBGA169	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
A3	VDD	Power		
A4	VDD11	Power		
A5	PG15	I/O	GPIO_EXTI15	MXCHIP_FLOW
A6	VDDIO2	Power		
A8	VDD	Power		
A9	PC11	I/O	UART4_RX	WRLS.UART4_RX
A10	PA15 (JTDI)	I/O	UCPD1_CC1	USB.UCPD_CC1
A11	VDD	Power		
B1	VDD	Power		
B2	VSS	Power		
B3	PI5	I/O	OCTOSPIM_P2_NCS	OCTOSPI.F_NCS
B4	VSS	Power		
B8	VSS	Power		
B11	VSS	Power		
B12	PI0	I/O	OCTOSPIM_P1_IO5	OCTOSPI.R_IO5
B13	PH12	I/O	OCTOSPIM_P2_IO7	OCTOSPI.F_IO7
C1	VBAT	Power		
C5	PH3-BOOT0 *	I/O	GPIO_Input	PH3-BOOT0
C6	PB5 *	I/O	GPIO_Output	UCPD_PWR
C8	PD4	I/O	SPI2_MOSI	WRLS.SPI2_MOSI
C9	PC10	I/O	UART4_TX	WRLS.UART4_TX
C10	PA14 (JTCK/SWCLK)	I/O	DEBUG_JTCK-SWCLK	T.SWCLK
C13	PH10	I/O	OCTOSPIM_P2_IO5	OCTOSPI.F_IO5
D1	PC14-OSC32_IN (PC14)	I/O	RCC_OSC32_IN	PC14-OSC32_IN
D3	PE3	I/O	OCTOSPIM_P1_DQS	OCTOSPI.R_DQS
D5	PB9	I/O	I2C1_SDA	
D6	PB3 (JTDO/TRACESWO)	I/O	DEBUG_JTDO-SWO	T.SWO
D7	PD7	I/O	OCTOSPIM_P1_IO7	OCTOSPI.R_IO7
D8	PD3	I/O	SPI2_MISO	WRLS.SPI2_MISO
D9	PH11	I/O	OCTOSPIM_P2_IO6	OCTOSPI.F_IO6
D13	VDD	Power		
E1	PC15-OSC32_OUT (PC15)	I/O	RCC_OSC32_OUT	PC15-OSC32_OUT
E2	PF0	I/O	OCTOSPIM_P2_IO0	OCTOSPI.F_IO0
E3	PC13 *	I/O	GPIO_Input	USER_Button
E5	PB8	I/O	I2C1_SCL	
E9	PH9	I/O	OCTOSPIM_P2_IO4	OCTOSPI.F_IO4

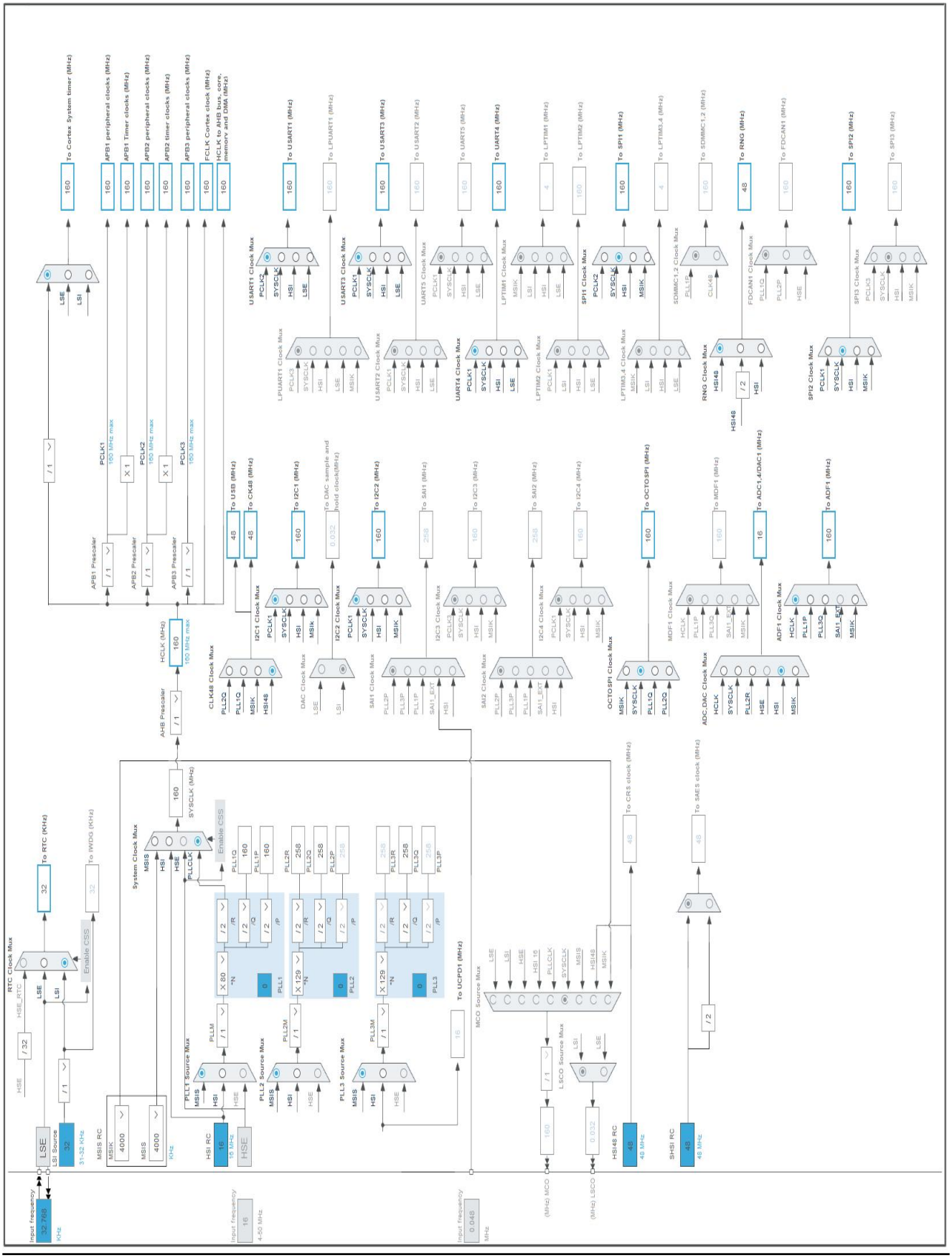
Pin Number UFBGA169	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
E10	PH4	I/O	I2C2_SCL	
E11	PH6 *	I/O	GPIO_Output	LED_RED
E12	VSS	Power		
E13	VDDUSB	Power		
F1	PF8	I/O	OCTOSPIM_P1_IO0	OCTOSPI.R_IO0
F2	VSS	Power		
F3	PF1	I/O	OCTOSPIM_P2_IO1	OCTOSPI.F_IO1
F4	PF2	I/O	OCTOSPIM_P2_IO2	OCTOSPI.F_IO2
F6	PD1	I/O	SPI2_SCK	WRLS.SPI2_SCK
F8	PH7 *	I/O	GPIO_Output	LED_GREEN
F9	PH5	I/O	I2C2_SDA	
F10	PH2	I/O	OCTOSPIM_P1_IO4	OCTOSPI.R_IO4
F11	PA10	I/O	USART1_RX	T.VCP_RX
F12	PA13 (JTMS/SWDIO)	I/O	DEBUG_JTMS-SWDIO	T.SWDIO
F13	PA12	I/O	USB_OTG_FS_DP	USB.C_P
G1	VDD	Power		
G2	PF7	I/O	OCTOSPIM_P1_IO2	OCTOSPI.R_IO2
G3	PF9	I/O	OCTOSPIM_P1_IO1	OCTOSPI.R_IO1
G5	PF3	I/O	OCTOSPIM_P2_IO3	OCTOSPI.F_IO3
G6	PF4	I/O	OCTOSPIM_P2_CLK	OCTOSPI.F_CLK_P
G7	PA8 *	I/O	GPIO_Input	ARDUINO_D9_DATAREADY
G11	PA9	I/O	USART1_TX	T.VCP_TX
G13	PA11	I/O	USB_OTG_FS_DM	USB.C_N
H2	VSS	Power		
H3	NRST	Reset		
H4	PF10 **	I/O	MDF1_CCK1	MIC.CCK1
H6	PF6	I/O	OCTOSPIM_P1_IO3	OCTOSPI.R_IO3
H8	PE10	I/O	ADF1_SDI0	MIC.SDINx
H10	PG6 *	I/O	GPIO_Output	WRLS.WKUP_B
H12	VDDIO2	Power		
J1	PH1-OSC_OUT (PH1) *	I/O	GPIO_Output	Mems.VL53_xshut
J7	PE9	I/O	ADF1_CCK0	MIC.CCK0
J9	PG5 *	I/O	GPIO_Input	Mems.VLX_GPIO
J10	PD14	I/O	GPIO_EXTI14	MXCHIP_NOTIFY
J12	VSS	Power		
J13	VDD	Power		
K1	PC3	I/O	OCTOSPIM_P1_IO6	OCTOSPI.R_IO6
K2	VSSA	Power		

Pin Number UFBGA169	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
K6	PF12	I/O	OCTOSPIM_P2_DQS	OCTOSPI.F_DQS
K7	PE8	I/O	GPIO_EXTI8	USB.UCPD_FLT
K8	PE14	I/O	SPI1_MISO	ARDUINO_D12_SPI1_MISO
K9	PB10	I/O	OCTOSPIM_P1_CLK	OCTOSPI.R_CLK_P
K11	PD10 *	I/O	GPIO_Input	Mems.INT_IIS2MDC
K12	PD13 *	I/O	GPIO_Input	USB.IANA
K13	PG2 *	I/O	GPIO_Input	Mems.INT_LPS22HH
L2	VDDA	Power		
L6	PF14	I/O	GPIO_Analog, ADC4_IN5	USB.VBUS_SENSE
L8	PE13	I/O	SPI1_SCK	ARDUINO_D13_SPI1_SCK
L9	PB11	I/O	OCTOSPIM_P1_NCS	OCTOSPI.R_NCS
L10	PB12 *	I/O	GPIO_Output	MXCHIP_NSS
L11	PB15	I/O	UCPD1_CC2	USB.UCPD_CC2
L12	PD8	I/O	USART3_TX	ARDUINO_D1_TX
L13	PD9	I/O	USART3_RX	ARDUINO_D0_RX
M3	VSS	Power		
M5	PF11 *	I/O	GPIO_Output	Mems.STSAFE_RESET
M7	VSS	Power		
M8	PE11 *	I/O	GPIO_Input	Mems.ISM330DLC_INT1
M9	PE15	I/O	SPI1_MOSI	ARDUINO_D11_SPI1_MOSI
M10	VSSSMPS	Power		
M11	VSS	Power		
N3	VDD	Power		
N5	PB1 **	I/O	MDF1_SDI0	MIC.SDIN0
N6	PF15 *	I/O	GPIO_Output	MXCHIP_RESET
N7	VDD	Power		
N8	PE12 *	I/O	GPIO_Output	ARDUINO_D10_SPI1_NSS
N9	VLXSMPS	Power		
N10	VDDSMPS	Power		
N11	VDD11	Power		
N12	VDD	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	STM32CubeMX
Project Folder	D:\GitHub\MiloradCvjetkovic\Forked\MDK-Packs\B-U585I-
Toolchain / IDE	MDK-ARM V5.32
Firmware Package Name and Version	STM32Cube FW_U5 V1.1.1
Application Structure	Basic
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Add necessary library files as reference in the toolchain project configuration file
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_GPDMA1_Init	GPDMA1
4	MX_ICACHE_Init	ICACHE
5	MX_ADC4_Init	ADC4
6	MX_ADF1_Init	ADF1
7	MX_I2C1_Init	I2C1
8	MX_I2C2_Init	I2C2
9	MX_OCTOSPI1_Init	OCTOSPI1
10	MX_OCTOSPI2_Init	OCTOSPI2
11	MX_SPI1_Init	SPI1

Rank	Function Name	Peripheral Instance Name
12	MX_SPI2_Init	SPI2
13	MX_USART1_UART_Init	USART1
14	MX_USART3_UART_Init	USART3
15	MX_UART4_Init	UART4
16	MX_UCPD1_Init	UCPD1
17	MX_USB_OTG_FS_PCD_Init	USB_OTG_FS
18	MX_RNG_Init	RNG
19	MX_RTC_Init	RTC

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32U5
Line	STM32U575/585
MCU	STM32U585AIIxQ
Datasheet	DS13086_Rev1

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

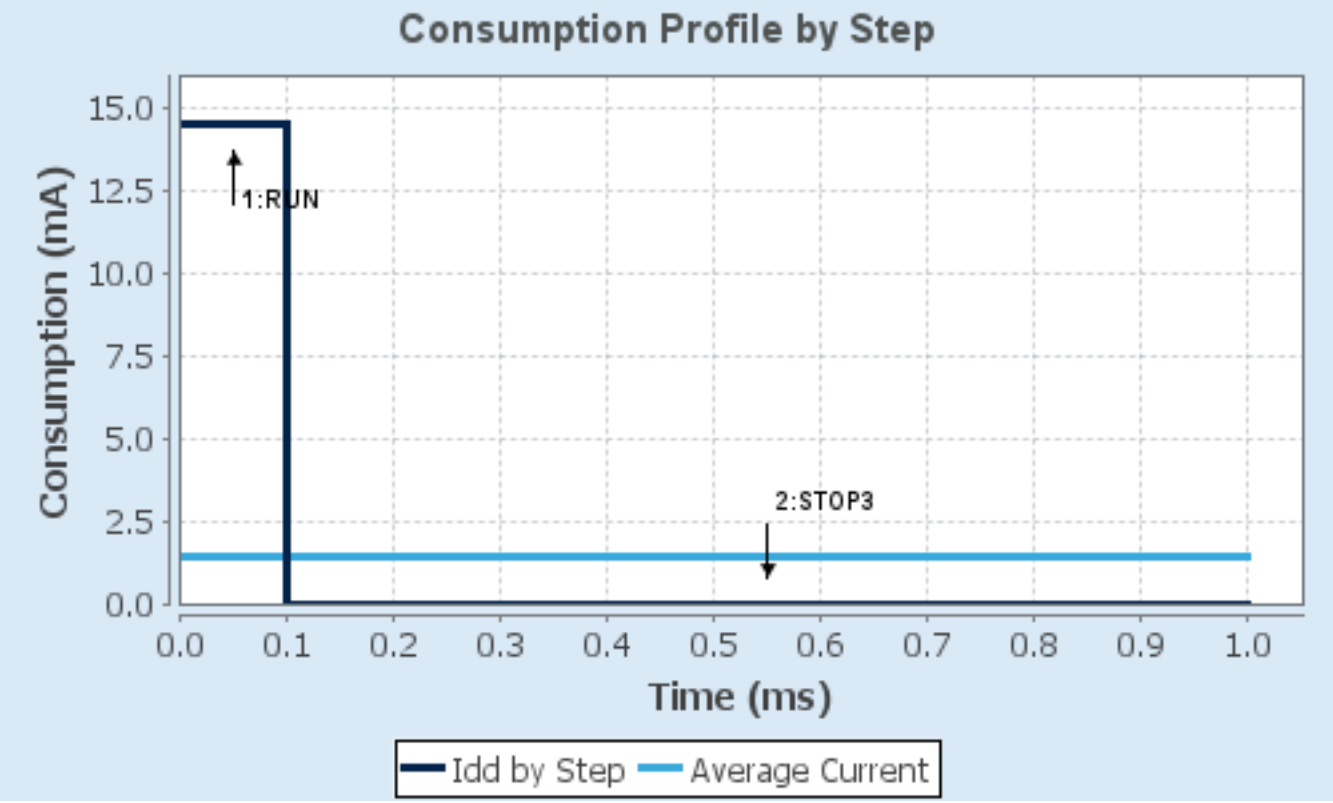
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP3
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-High	NoScale/SMPS
Fetch Type	FLASH_PwrDwnBank2/ART/ Cache2Ways	FLASH
CPU Frequency	160 MHz	0 Hz
Clock Configuration	HSE BYP PLL ALL_RAM_RETENTION	ALL_CLOCKS_OFF
Clock Source Frequency	16 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	14.5 mA	1.8 µA
Duration	0.1 ms	0.9 ms
DMIPS	200.0	0.0
Ta Max	103.43	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	1.45 mA
Battery Life	3 months, 6 days, 2 hours	Average DMIPS	20.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
15.0
12.5
10.0
7.5
5.0
2.5
0.0
1:RUN
2:STOP3
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. ADC4

mode: IN5

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Sequencer	Sequencer set to fully configurable
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Low Power Auto Wait	Disabled
Low Power Auto Off	Low power disabled and auto off disabled
SamplingTime Common 1	1.5 Cycles
SamplingTime Common 2	1.5 Cycles
Trigger Frequency	Low frequency
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Oversampling Mode	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	1
Rank	1
Channel	Channel 5
Sampling Time	Sampling time common 1
Offset Number	No offset

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.2. ADF1

mode: Activate ADF

mode: Common Clock CCK0

7.2.1. ADF Instance:

Common Clock configuration:

Processing clock divider	1
Output Clock Activation	Disable

Serial Interface (SITF):

Serial interface mode	LF Master SPI
Serial interface clock source	Common clock 0 source
SPI Threshold	4

Digital Filter:

Delay	0
CIC Mode	One filter in Sinc4 order
Decimation Ratio	2
Gain	0
Reshape Filter	Disable
High pass filter	Disable
Sound Activity	Disable
Acquisition mode	Asynchronous, continuous
FIFO Data Transfer threshold	when RXFIFO is not empty
Samples to discard	0

7.3. DEBUG

Debug: Trace Asynchronous Sw

7.4. I2C1

I2C: I2C

7.4.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0

Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x30909DEC ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

Autonomous Mode:

Autonomous Mode	Disable

7.5. I2C2

I2C: I2C

7.5.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x30909DEC ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

Autonomous Mode:

Autonomous Mode	Disable

7.6. ICACHE

Mode: 2-ways set associative cache

7.7. LPBAM

mode: LPBAM Scenario uses resources from Smart Run Domain only

mode: LPBAM Scenario is hosted by LPDMA1

7.8. LPBAMQUEUE

mode: QUEUE MODE

7.8.1. Parameter Settings:

DMA Channel Configuration:	
Priority	Low
DMA Channel Interrupt Configuration:	
Data Transfer Error Interrupt	Disable
Update Link Error Interrupt	Disable
User Setting Error Interrupt	Disable
Transfer Complete Interrupt	Disable
Trigger Overrun Interrupt	Disable

7.9. OCTOSPI1

Mode: Octo SPI

Clock: Port1 CLK

Chip Select: Port1 NCS

Data Strobe: Port1 DQS (RWDS)

Data [3:0]: Port1 IO[3:0]

Data [7:4]: Port1 IO[7:4]

7.9.1. Parameter Settings:

Generic:	
Fifo Threshold	1
Dual Quad mode	Disable
Memory Type	**AP Memory ***
Device Size	**23 ***
Chip Select High Time	1
Free Running Clock	Disable
Clock Mode	Low
Wrap Size	Not Supported
Clock Prescaler	**2 ***
Sample Shifting	None

Delay Hold Quarter Cycle	**Enable ***
Chip Select Boundary	**10 ***
Maximum Transfer	0
Refresh Rate	**100 ***

Delay Block Settings:

Status (DLYB)	**Used ***
Unit Delay Cell	0
Output Clock Phase	0

7.10. OCTOSPI2

Mode: Octo SPI

Clock: Port2 CLK

Chip Select: Port2 NCS

Data Strobe: Port2 DQS (RWDS)

Data [3:0]: Port2 IO[3:0]

Data [7:4]: Port2 IO[7:4]

7.10.1. Parameter Settings:

Generic:

Fifo Threshold	**4 ***
Dual Quad mode	Disable
Memory Type	**Macronix ***
Device Size	**26 ***
Chip Select High Time	**2 ***
Free Running Clock	Disable
Clock Mode	Low
Wrap Size	Not Supported
Clock Prescaler	**4 ***
Sample Shifting	None
Delay Hold Quarter Cycle	**Enable ***
Chip Select Boundary	0
Maximum Transfer	0
Refresh Rate	0

Delay Block Settings:

Status (DLYB)	**Used ***
Unit Delay Cell	0
Output Clock Phase	0

7.11. PWR

mode: Dead Battery Signals disabled

mode: Power saving mode

mode: Privilege attributes

7.11.1. Power Saving:

System power supply:	
Power Regulator	**SMPS ***
SRAM power down in Run mode:	
SRAM1 power down in Run mode	Disable
SRAM2 power down in Run mode	Disable
SRAM3 power down in Run mode	Disable
SRAM4 power down in Run mode	Disable
SRAM power down in Stop mode:	
SRAM1 Page1 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM1 Page2 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM1 Page3 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM2 Page1 power down in Stop (0, 1, 2) mode	Disable
SRAM2 Page2 power down in Stop (0, 1, 2) mode	Disable
SRAM3 Page1 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM3 Page2 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM3 Page3 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM3 Page4 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM3 Page5 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM3 Page6 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM3 Page7 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM3 Page8 power down in Stop (0, 1, 2, 3) mode	Disable
SRAM4 power down in Stop (0, 1, 2, 3) mode	Disable
ICACHE power down in Stop (0, 1, 2, 3) mode	Disable
DCACHE1 power down in Stop (0, 1, 2, 3) mode	Disable
DMA2D RAM power down in Stop (0, 1, 2, 3) mode	Disable
PKA32 RAM power down in Stop (0, 1, 2, 3) mode	Disable
PERIPH RAM power down in Stop (0, 1, 2, 3) mode	Disable
SRAM fast wakeup:	
SRAM4 fast wakeup from Stop (0, 1, 2, 3) modes	Disable

7.11.2. PWR Privilege :

Privilege PWR:

PWR Privilege	Disable

7.12. RCC

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.12.1. RCC Privilege :

Privilege RCC:

Privilege of RCC Non-Secure Items	Disable

7.12.2. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	4 WS (5 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
MSI Calibration Value	16
MSIS/MSIK Auto Calibration	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

PLL1/2/3 Parameters:

PLL1M BOOST EPOD Clock Divider	1
PLL1 input frequency range	Between 4 and 8 MHz

Low Power Parameters:

MSI in Stop mode	Disabled
HSI in Stop mode	Disabled

7.13. RNG

mode: Activated

7.13.1. Parameter Settings:

Clock Error Detection	Enable

7.14. RTC

mode: Activate Clock Source

7.14.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255
Bin Mode	Free running BCD calender mode

7.14.2. RTC Privilege:

Privilege RTC:

RTC full privilege	Disable

Backup register:

Start zone 1	RTC_BKP_DR0
Start Zone 2	RTC_BKP_DR0
start zone 3	RTC_BKP_DR0

Privilege Backup register :

Backup Register PrivZone	Non-privilege

Privilege RTC Feature:

RTC Initialisation	Non-Privilege
RTC Alarm A	Non-Privilege
RTC Alarm B	Non-Privilege
RTC Calibration	Non-Privilege
RTC TimeStamp	Non-Privilege
RTC WakeUpTimer	Non-Privilege

7.15. SPI1

Mode: Full-Duplex Master

7.15.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**8 ***
Baud Rate	**20.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Autonomous Mode:

State	Disable

CRC Parameters:

CRC Calculation	Disabled

Advanced Parameters:

NSSP Mode	**Disabled ***
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled
Ready Master Management	Internal
Ready Signal Polarity	High

7.16. SPI2

Mode: Full-Duplex Master

7.16.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**8 ***
Baud Rate	**20.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Autonomous Mode:

State	Disable

CRC Parameters:

CRC Calculation	Disabled

Advanced Parameters:

NSSP Mode	**Disabled ***
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled
Ready Master Management	Internal
Ready Signal Polarity	High

7.17. SYS

Timebase Source: SysTick

7.18. UART4

Mode: Asynchronous

7.18.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration
Autonomous Mode	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable

Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.19. UCPD1

UCPD Mode: Dual Role

7.19.1. Parameter Settings:

Version	1.0

7.20. USART1

Mode: Asynchronous

7.20.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	**Enable ***
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	**half full configuration ***
Autonomous Mode	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable

MSB First	Disable

7.21. USART3

Mode: Asynchronous

7.21.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration
Autonomous Mode	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.22. USB_OTG_FS

Mode: Device_Only

7.22.1. Parameter Settings:

Speed	Full Speed 12MBit/s
Low power	Disabled
Battery charging	Disabled
Link Power Management	Disabled

VBUS sensing	Disabled
Use dedicated end point 1 interrupt	Disabled
Signal start of frame	Disabled

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC4	PF14	ADC4_IN5	Analog mode	No pull-up and no pull-down	n/a	USB.VBUS_SENSE
ADF1	PE10	ADF1_SDI0	Alternate Function Push Pull	No pull-up and no pull-down	Low	MIC.SDINx
	PE9	ADF1_CCK0	Alternate Function Push Pull	No pull-up and no pull-down	Low	MIC.CCK0
DEBUG	PA14 (JTCK/SWCLK)	DEBUG_JTCK-SWCLK	n/a	n/a	n/a	T.SWCLK
	PB3 (JTDO/TRACESWO)	DEBUG_JTDO-SWO	n/a	n/a	n/a	T.SWO
	PA13 (JTMS/SWDIO)	DEBUG_JTMS-SWDIO	n/a	n/a	n/a	T.SWDIO
I2C1	PB9	I2C1_SDA	Alternate Function Open Drain	**Pull-up ***	Low	
	PB8	I2C1_SCL	Alternate Function Open Drain	**Pull-up ***	Low	
I2C2	PH4	I2C2_SCL	Alternate Function Open Drain	**Pull-up ***	Low	
	PH5	I2C2_SDA	Alternate Function Open Drain	**Pull-up ***	Low	
OCTOSPI1	PI0	OCTOSPIM_P1_IO5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	OCTOSPI.R_IO5
	PE3	OCTOSPIM_P1_DQS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	OCTOSPI.R_DQS
	PD7	OCTOSPIM_P1_IO7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	OCTOSPI.R_IO7
	PF8	OCTOSPIM_P1_IO0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	OCTOSPI.R_IO0
	PH2	OCTOSPIM_P1_IO4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	OCTOSPI.R_IO4
	PF7	OCTOSPIM_P1_IO2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	OCTOSPI.R_IO2
	PF9	OCTOSPIM_P1_IO1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	OCTOSPI.R_IO1
	PF6	OCTOSPIM_P1_IO3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	OCTOSPI.R_IO3
	PC3	OCTOSPIM_P1_IO6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	OCTOSPI.R_IO6
	PB10	OCTOSPIM_P1_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	OCTOSPI.R_CLK_P

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PB11	OCTOSPIM_P1_NCS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	OCTOSPI.R_NCS
OCTOSPI2	PI5	OCTOSPIM_P2_NCS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	OCTOSPI.F_NCS
	PH12	OCTOSPIM_P2_IO7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	OCTOSPI.F_IO7
	PH10	OCTOSPIM_P2_IO5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	OCTOSPI.F_IO5
	PH11	OCTOSPIM_P2_IO6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	OCTOSPI.F_IO6
	PF0	OCTOSPIM_P2_IO0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	OCTOSPI.F_IO0
	PH9	OCTOSPIM_P2_IO4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	OCTOSPI.F_IO4
	PF1	OCTOSPIM_P2_IO1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	OCTOSPI.F_IO1
	PF2	OCTOSPIM_P2_IO2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	OCTOSPI.F_IO2
	PF3	OCTOSPIM_P2_IO3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	OCTOSPI.F_IO3
	PF4	OCTOSPIM_P2_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	OCTOSPI.F_CLK_P
	PF12	OCTOSPIM_P2_DQS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	OCTOSPI.F_DQS
RCC	PC14-OSC32_IN (PC14)	RCC_OSC32_IN	n/a	n/a	n/a	PC14-OSC32_IN
	PC15-OSC32_OUT (PC15)	RCC_OSC32_OUT	n/a	n/a	n/a	PC15-OSC32_OUT
SPI1	PE14	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	ARDUINO_D12_SPI1_MISO
	PE13	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	ARDUINO_D13_SPI1_SCK
	PE15	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	ARDUINO_D11_SPI1_MOSI
SPI2	PD4	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	WRLS.SPI2_MOSI
	PD3	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	WRLS.SPI2_MISO
	PD1	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	WRLS.SPI2_SCK
UART4	PC11	UART4_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	WRLS.UART4_RX
	PC10	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	WRLS.UART4_TX
UCPD1	PA15 (JTDI)	UCPD1_CC1	Analog mode	No pull-up and no pull-down	n/a	USB.UCPD_CC1
	PB15	UCPD1_CC2	Analog mode	No pull-up and no pull-down	n/a	USB.UCPD_CC2
USART1	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	T.VCP_RX

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	T.VCP_TX
USART3	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***	ARDUINO_D1_TX
	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***	ARDUINO_D0_RX
USB_OTG_FS	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	USB.C_P
	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	USB.C_N
Single Mapped Signals	PF10	MDF1_CCK1	Alternate Function Push Pull	No pull-up and no pull-down	Low	MIC.CCK1
	PB1	MDF1_SDI0	Alternate Function Push Pull	No pull-up and no pull-down	Low	MIC.SDIN0
GPIO	PG15	GPIO_EXTI15	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	MXCHIP_FLOW
	PH3-BOOT0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	PH3-BOOT0
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	UCPD_PWR
	PC13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	USER_Button
	PH6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_RED
	PH7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_GREEN
	PA8	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ARDUINO_D9_DATAREADY
	PG6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	WRLS.WKUP_B
	PH1-OSC_OUT (PH1)	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Mems.VL53_xshut
	PG5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Mems.VLX_GPIO
	PD14	GPIO_EXTI14	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	MXCHIP_NOTIFY
	PE8	GPIO_EXTI8	External Interrupt Mode with Rising edge trigger detection	**Pull-up ***	n/a	USB.UCPD_FLT
	PD10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Mems.INT_IIS2MDC
	PD13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	USB.IANA
	PG2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Mems.INT_LPS22HH
	PF14	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	USB.VBUS_SENSE
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**High ***	MXCHIP_NSS
	PF11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Mems.STSAFE_RESET
	PE11	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Mems.ISM330DLC_INT1
	PF15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MXCHIP_RESET
	PE12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**High ***	ARDUINO_D10_SPI1_NSS

8.2. GPDMA1

Channel 5 - 2 Words Internal FIFO : Standard Request Mode
Channel 4 - 2 Words Internal FIFO : Standard Request Mode
Channel 3 - 2 Words Internal FIFO : Standard Request Mode
Channel 2 - 2 Words Internal FIFO : Standard Request Mode

8.2.1. All Channels:

Channel 2:

Request	GPDMA1_REQUEST_SPI1_RX

Channel 3:

Request	GPDMA1_REQUEST_SPI1_TX

Channel 4:

Request	GPDMA1_REQUEST_SPI2_RX

Channel 5:

Request	GPDMA1_REQUEST_SPI2_TX

8.2.2. SECURITY:

CH5:

Enable Channel as Privileged	NON PRIVILEDGED

CH4:

Enable Channel as Privileged	NON PRIVILEDGED

CH3:

Enable Channel as Privileged	NON PRIVILEDGED

CH2:

Enable Channel as Privileged	NON PRIVILEDGED

8.2.3. CH5:

Circular configuration:

Circular Mode	Disable

Request Configuration:

Request	**SPI2_TX ***
DMA Handle in IP Structure	hdmatx
Block HW request protocol	Single/Burst Level

Channel configuration:

Priority	**High ***
Transaction Mode	Normal
Direction	**Memory To Peripheral ***

Source Data Setting:

Source Address Increment After Transfer	**Enabled ***
Data Width	Byte
Burst Length	1
Allocated Port for Transfer	Port 0

Destination Data Setting:

Destination Address Increment After Transfer	Disabled
Data Width	Byte
Burst Length	1
Allocated Port for Transfer	Port 0

Data Handling:

Data Handling Configuration	Disable

Trigger:

Trigger Configuration	Disable

Transfer Event Configuration:

Transfer Event Generation	The TC (and the HT) event is generated at the (respectively half) end of each block

8.2.4. CH4:

Circular configuration:

Circular Mode	Disable

Request Configuration:

Request	**SPI2_RX ***
DMA Handle in IP Structure	hdmarx
Block HW request protocol	Single/Burst Level

Channel configuration:

Priority	**High ***
Transaction Mode	Normal
Direction	Peripheral To Memory

Source Data Setting:

Source Address Increment After Transfer	Disabled
Data Width	Byte
Burst Length	1
Allocated Port for Transfer	**Port 1 ***

Destination Data Setting:

Destination Address Increment After Transfer	**Enabled ***
Data Width	Byte
Burst Length	1
Allocated Port for Transfer	**Port 1 ***

Data Handling:

Data Handling Configuration	Disable

Trigger:

Trigger Configuration	Disable

Transfer Event Configuration:

Transfer Event Generation	The TC (and the HT) event is generated at the (respectively half) end of each block

8.2.5. CH3:

Circular configuration:

Circular Mode	Disable

Request Configuration:

Request	**SPI1_TX ***
DMA Handle in IP Structure	hdmatx
Block HW request protocol	Single/Burst Level

Channel configuration:

Priority	**High ***
Transaction Mode	Normal
Direction	**Memory To Peripheral ***

Source Data Setting:

Source Address Increment After Transfer	**Enabled ***
Data Width	Byte
Burst Length	1
Allocated Port for Transfer	Port 0

Destination Data Setting:

Destination Address Increment After Transfer	Disabled
Data Width	Byte
Burst Length	1
Allocated Port for Transfer	Port 0

Data Handling:

Data Handling Configuration	Disable

Trigger:

Trigger Configuration	Disable

Transfer Event Configuration:

Transfer Event Generation	The TC (and the HT) event is generated at the (respectively half) end of each block

8.2.6. CH2:

Circular configuration:

Circular Mode	Disable

Request Configuration:

Request	**SPI1_RX ***
DMA Handle in IP Structure	hdmarx
Block HW request protocol	Single/Burst Level

Channel configuration:

Priority	**High ***
Transaction Mode	Normal
Direction	Peripheral To Memory

Source Data Setting:

Source Address Increment After Transfer	Disabled
Data Width	Byte
Burst Length	1
Allocated Port for Transfer	**Port 1 ***

Destination Data Setting:

Destination Address Increment After Transfer	**Enabled ***
Data Width	Byte
Burst Length	1
Allocated Port for Transfer	**Port 1 ***

Data Handling:

Data Handling Configuration	Disable

Trigger:

Trigger Configuration	Disable

Transfer Event Configuration:

Transfer Event Generation	The TC (and the HT) event is generated at the (respectively half) end of each block

8.3. LINKEDLIST

8.4. LPDMA1

8.5. NVIC configuration

8.5.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	14	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
EXTI Line8 interrupt	true	8	0
EXTI Line14 interrupt	true	8	0
EXTI Line15 interrupt	true	8	0
GPDMA1 Channel 2 global interrupt	true	8	0
GPDMA1 Channel 3 global interrupt	true	8	0
GPDMA1 Channel 4 global interrupt	true	8	0
GPDMA1 Channel 5 global interrupt	true	8	0
SPI1 global interrupt	true	8	0
SPI2 global interrupt	true	8	0
USART1 global interrupt	true	8	0
USART3 global interrupt	true	8	0
UART4 global interrupt	true	8	0
Flash non-secure global interrupt	unused		
RCC non-secure global interrupt	unused		
I2C1 Event interrupt	unused		
I2C1 Error interrupt	unused		
I2C2 Event interrupt	unused		
I2C2 Error interrupt	unused		
USB OTG FS global interrupt	unused		
OCTOSPI1 global interrupt	unused		
RNG global interrupt	unused		
FPU global interrupt	unused		
UCPD1 global interrupt	unused		
Instruction cache global interrupt	unused		
ADF interrupt	unused		
ADC4 (12bits) global interrupt	unused		
OCTOSPI2 global interrupt	unused		

8.5.2. NVIC Code generation

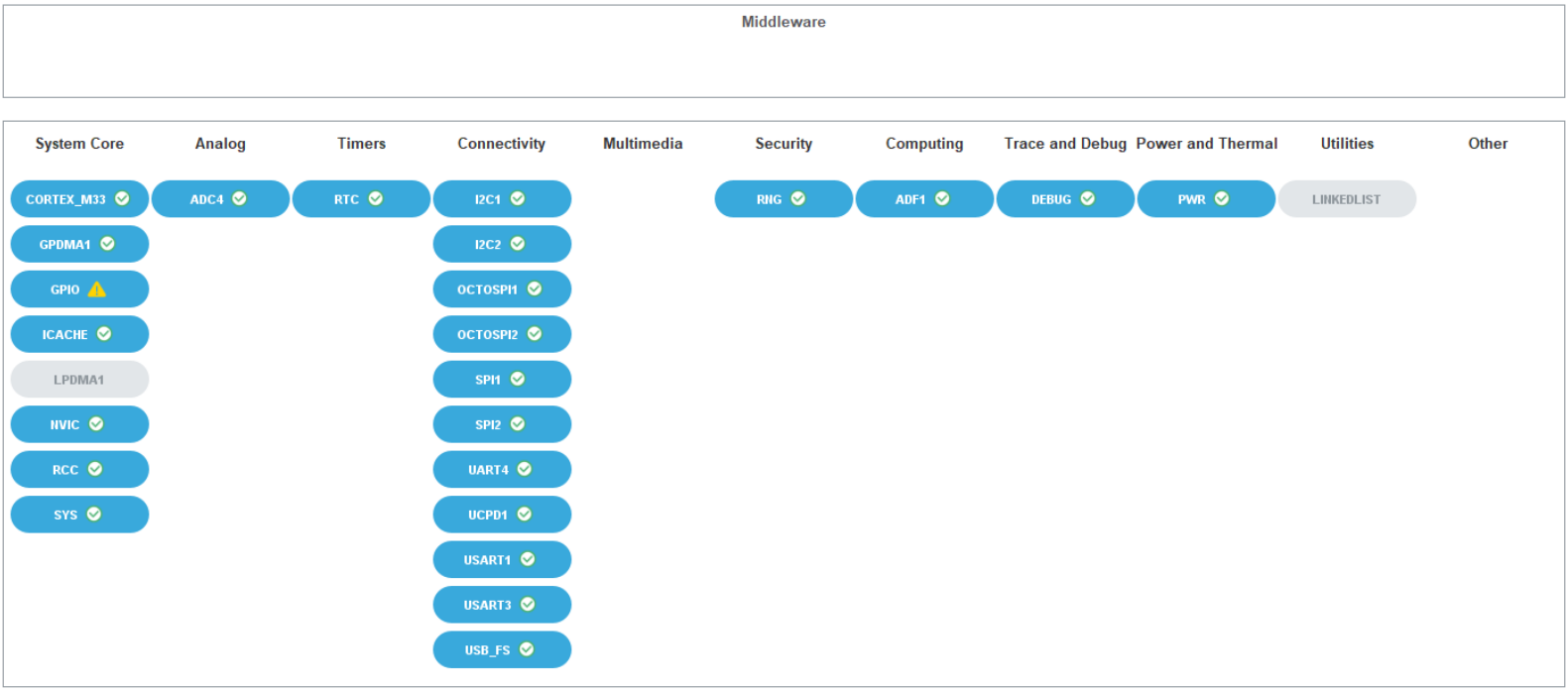
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	false	true
EXTI Line8 interrupt	false	true	true
EXTI Line14 interrupt	false	true	true
EXTI Line15 interrupt	false	true	true
GPDMA1 Channel 2 global interrupt	false	true	true
GPDMA1 Channel 3 global interrupt	false	true	true
GPDMA1 Channel 4 global interrupt	false	true	true
GPDMA1 Channel 5 global interrupt	false	true	true
SPI1 global interrupt	false	true	true
SPI2 global interrupt	false	true	true
USART1 global interrupt	false	true	true
USART3 global interrupt	false	true	true
UART4 global interrupt	false	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current



10. Docs & Resources

Type	Link