MIMXRT1064-EVK

Table of Content

Page 1	COVER
Page 2	BLOCK DIAGRAM
Page 3	MAIN POWER
Page 4	POWER DOMAIN
Page 5	MIMXRT1064DVL6A
Page 6	LCD
Page 7	USB
Page 8	CAN
Page 9	AUDIO
Page 10	ETHERNET
Page 11	SD/FLASH/EMMC
Page 12	ARDUINO/JTAG
Page 13	SDRAM
Page 14	FREELINK
Page 15	CSI
Page 16	BOOT
Page 17	MISC
Page 18	
Page 19	
Page 20	
Page 21	
Page 22	
Page 23	
Page 24	
Page 25	
Page 26	
Page 26	
Page 27	
Page 28	

Revision History

Rev. Code	Date	By	Description
A	2018-7-4	Shawn Shi	Initial Release
A1	2019-2-21	Shawn Shi	Update BOM: change R126 to R129 from populate to DNP, Populate SW5, Change C88 to 2.2uF/35V. Add notes for DQS PIN
A2	2020-03-12	Shawn Shi	Update BOM: Change U32 from DNP to populate

1. Unless Otherwise Specified:

   All resistors are in ohms, 1/16 Watt,0402
   All capacitors are in uF,0402
   All voltages are DC
   All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

ICAP Classification: CP: ___ IUO: X PUBI: ___

Drawing Title: MIMXRT1064-EVK

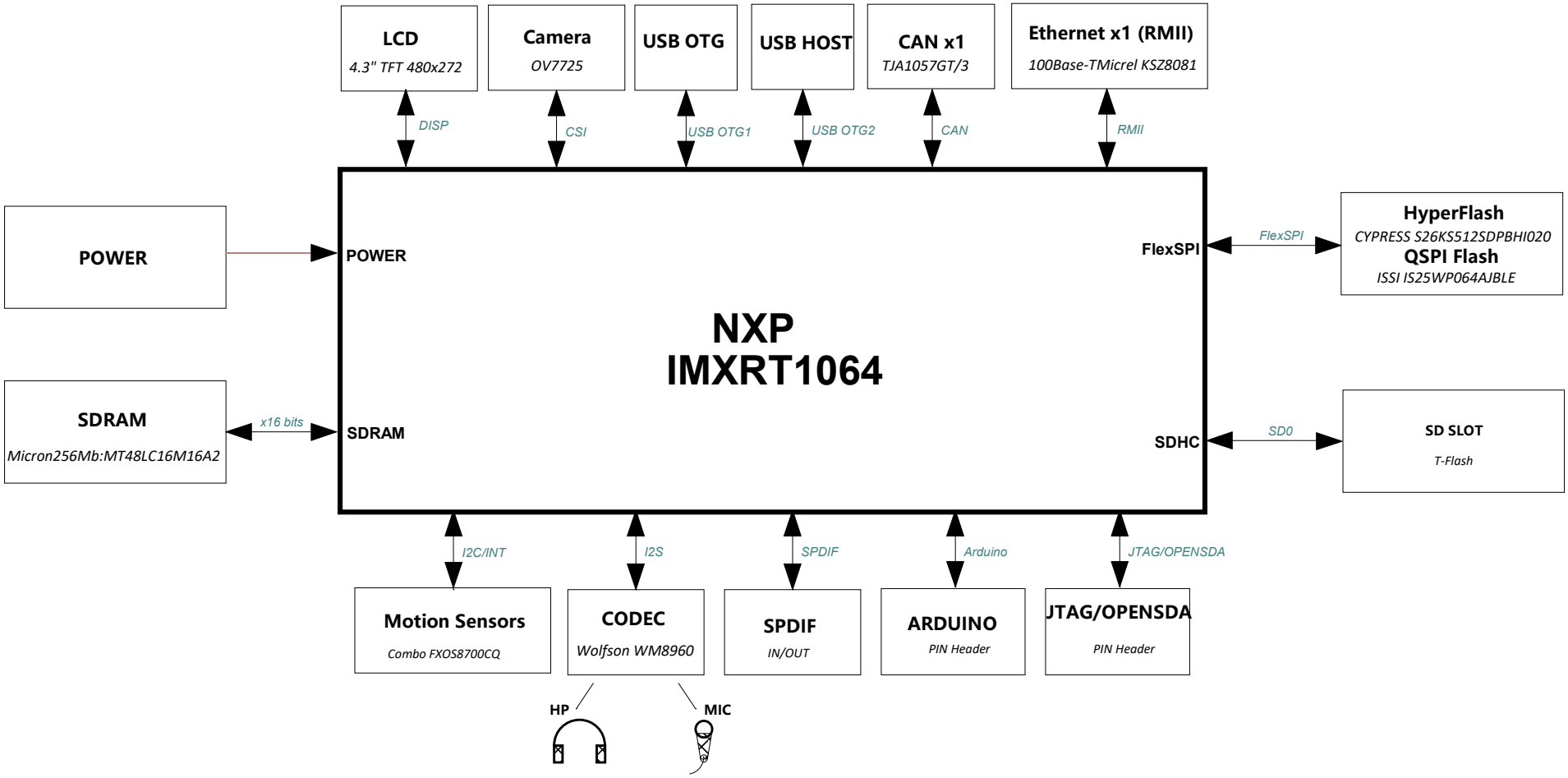
Page Title: COVER

Size	Document Number	Rev
C	SCH-32221, PDF: SPF-32221	A2

Date: Thursday, March 12, 2020 | Sheet 1 of 17

Blcok Diagram Rev A2#####

MIMXRT1064-EVK



ICAP Classification: CP: ___ IUO: X PUBI: ___

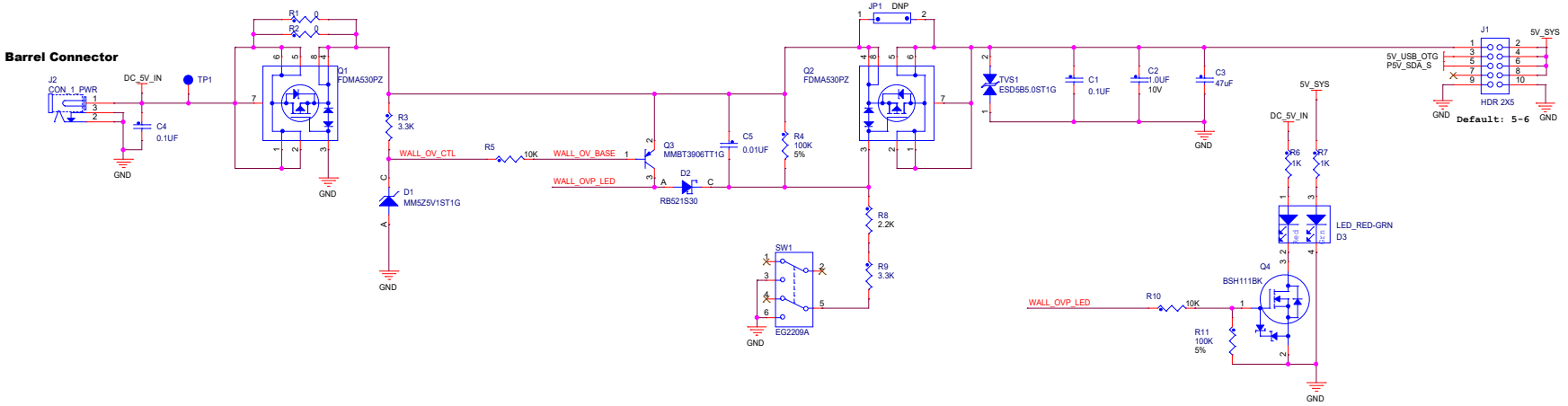
Drawing Title: MIMXRT1064-EVK

Page Title: BLOCK DIAGRAM

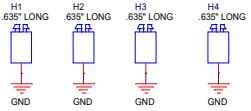
Size	Document Number	Rev
C	SCH-32221, PDF: SPF-32221	A2

Date: Thursday, March 12, 2020 | Sheet 2 of 17

Main Power



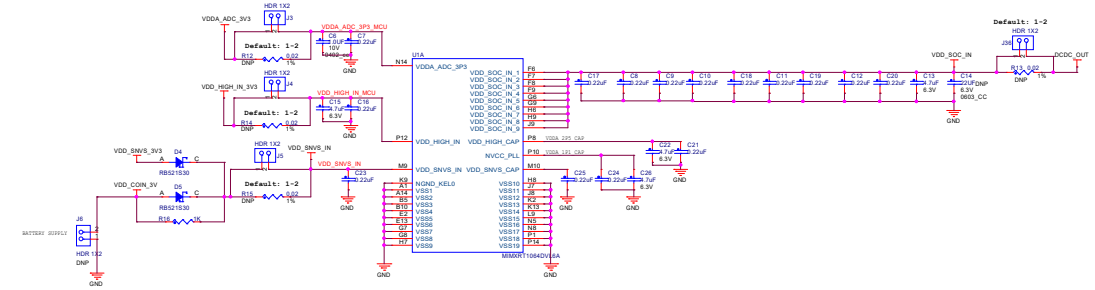
Board Mounting Holes

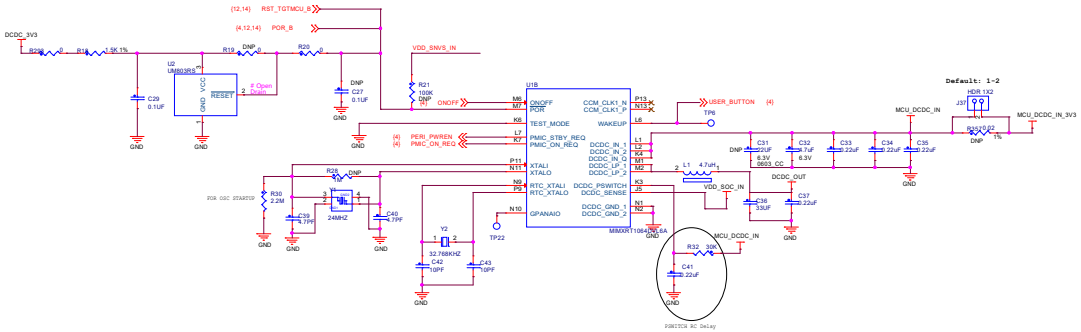


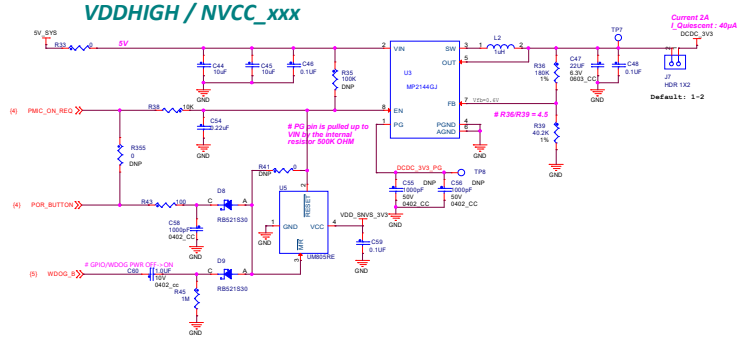
Ground TPs

Layout Note: Place Ground TPs
to assist signal measurement.

ICAP Classification:	CP: ___	IUO: X	PUBI: ___
Drawing Title:	MIMXRT1064-EVK		
Page Title:	MAIN POWER		
Size C	Document Number SCH-32221, PDF: SPF-32221		Rev A2
Date: Thursday, March 12, 2020	Sheet 3 of 17		



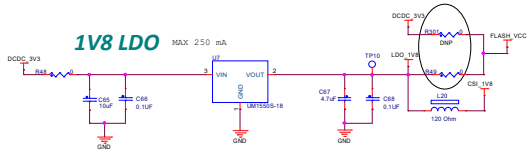




VDDHIGH / NVCC_xxx

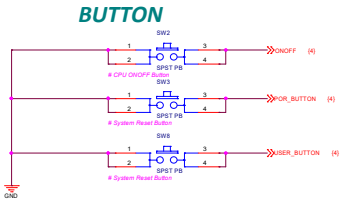
1V8 LDO

MAX 250 mA

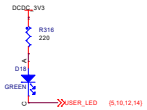


FLASH VCC

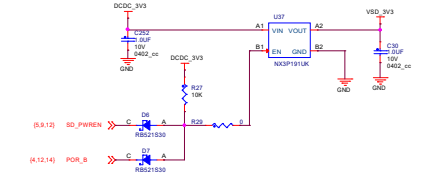
BUTTON



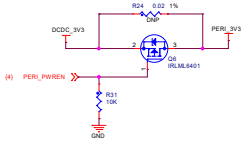
USER LED



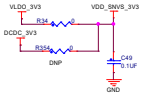
SD CARD POWER SWITCH



LCD 3V3 POWER SWITCH

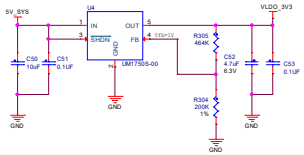


SNVS

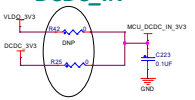


ADC

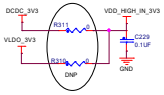
3V3 LDO for SNVS



DCDC_IN

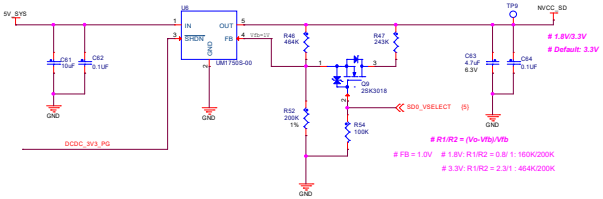


VDD_HIGH_IN



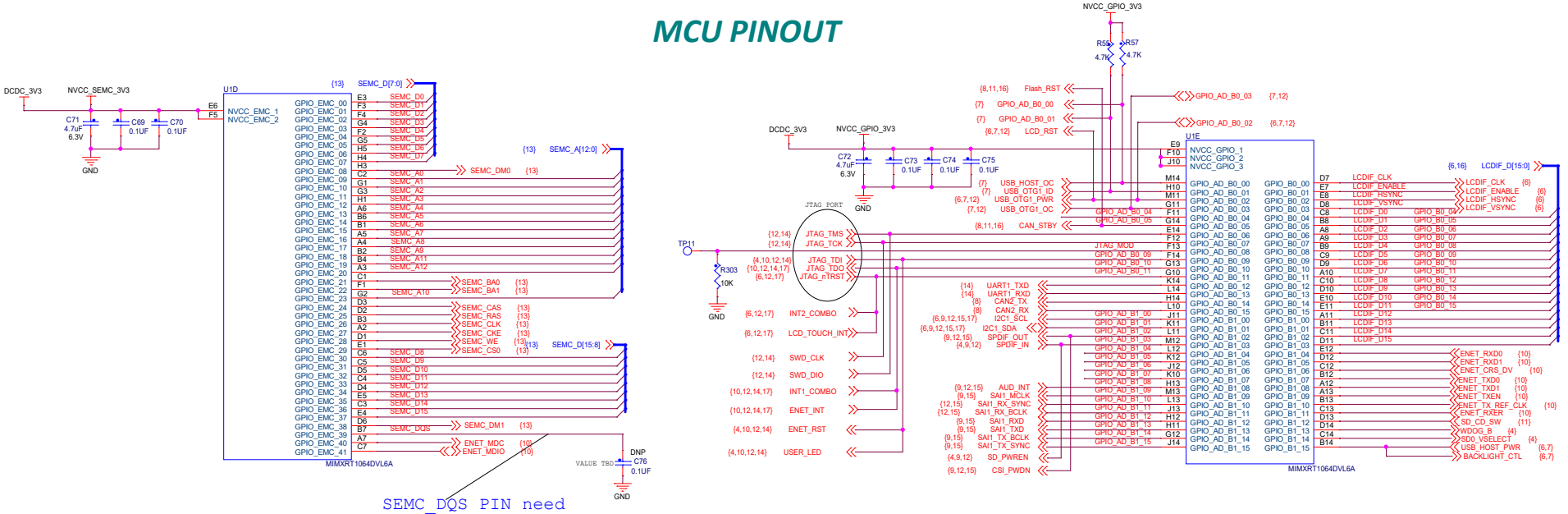
NVCC_SD <SD3.0>

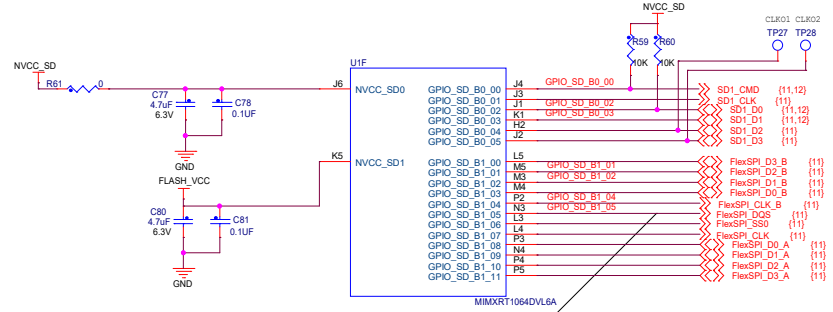
MAX 350 mA

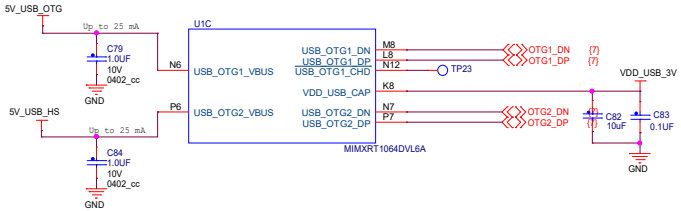


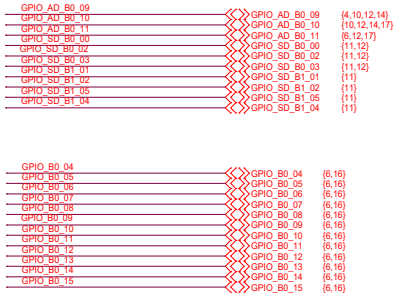
ICAP Classification:	CP:	IUO: X PUBI:
Drawing Title:	MIMXRT1064-EVK	
Page Title:	POWER DOMAIN	
Size: D	Document Number: SCH-32221_PDF: SPF-32221	Rev: A2
Date: Thursday, March 12, 2020	Sheet 4 of 17	

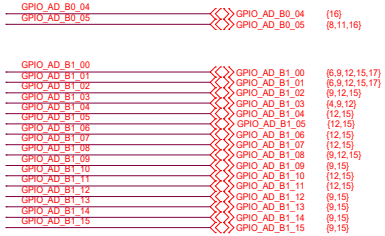
MCU PINOUT





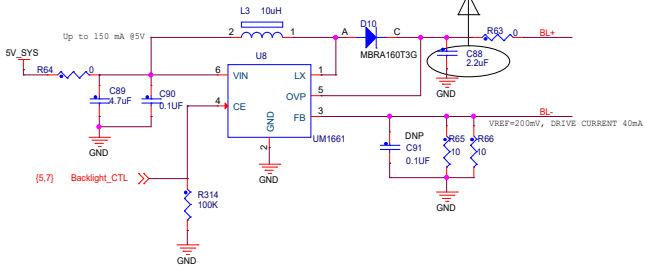






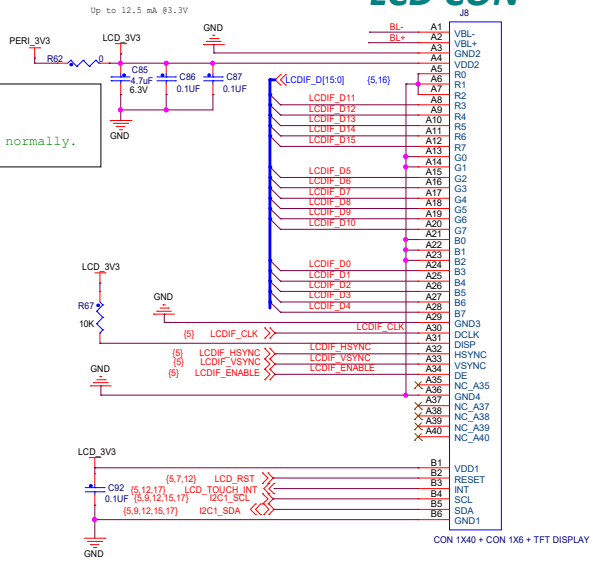
ICAP Classification:	CP: ___	IUO: X	PUBI: ___
Drawing Title:	MIMXRT1064-EVK		
Page Title:	MIMXRT1064DVL6A		
Size: C	Document Number: SCH-32221, PDF: SPF-32221		Rev: A2
Date: Thursday, March 12, 2020	Sheet 5 of 17		

Backlight Control



Note:
If you use LCD module for Rev A, need to
change C88 to 2.2uf/35V or 1.0uf/35V
to ensure the backlight control circuits working normally.

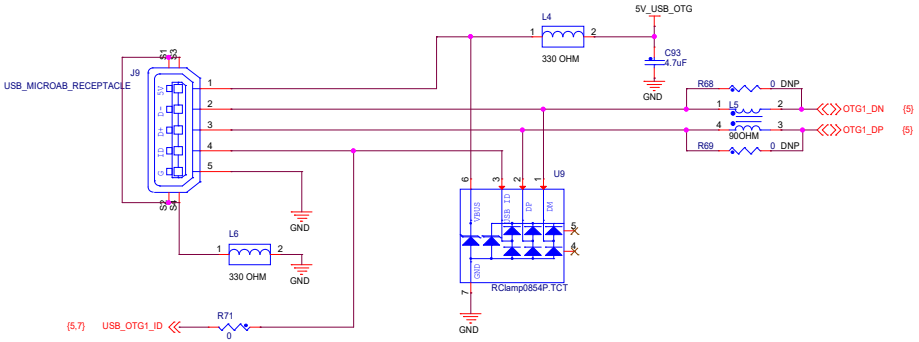
LCD CON



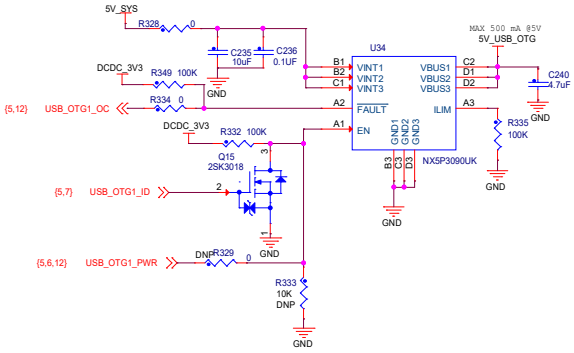
CON 1X40 + CON 1X6 + TFT DISPLAY

ICAP Classification:	CP: ___	IUO: X	PUBI: ___
Drawing Title:	MIMXRT1064-EVK		
Page Title:	LCD		
Size C	Document Number SCH-32221, PDF: SPF-32221		Rev A2
Date: Wednesday, August 26, 2020	Sheet 6 of 17		

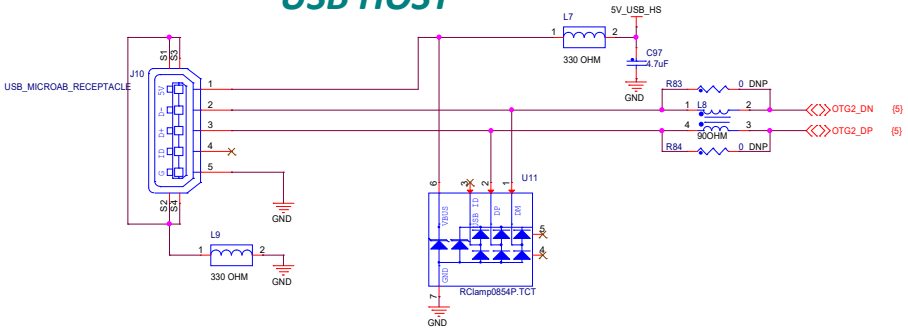
USB OTG

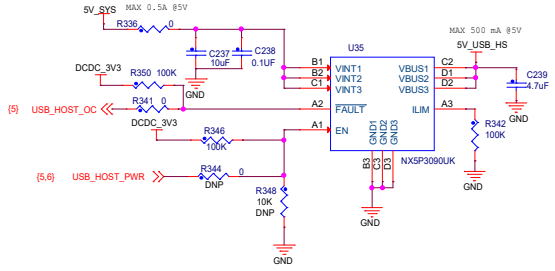


USB POWER



USB HOST





ICAP Classification: CP: ___ IUO: X PUBI: ___

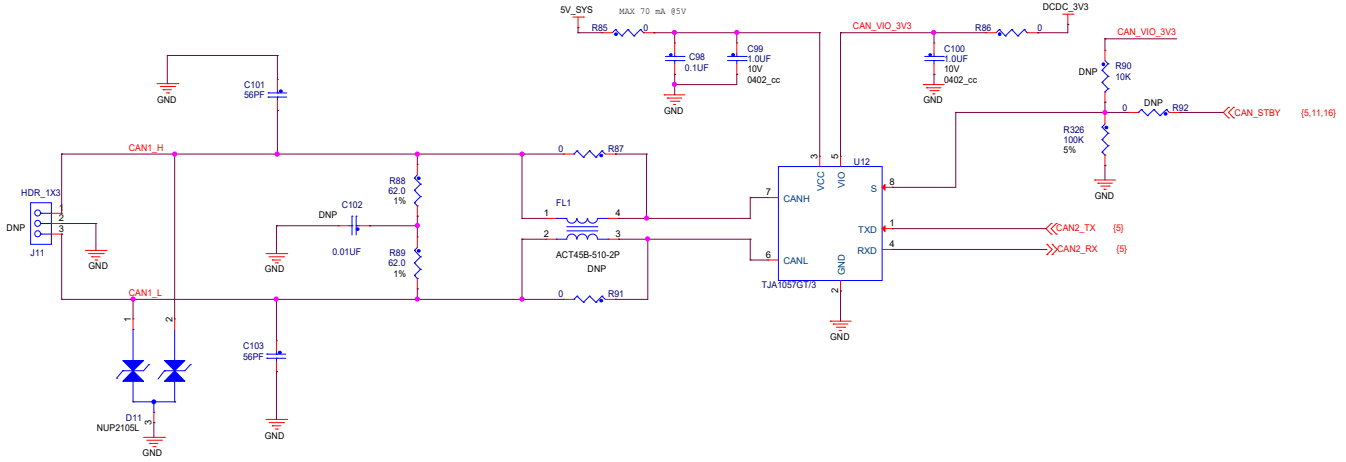
Drawing Title: **MIMXRT1064-EVK**

Page Title: **USB**

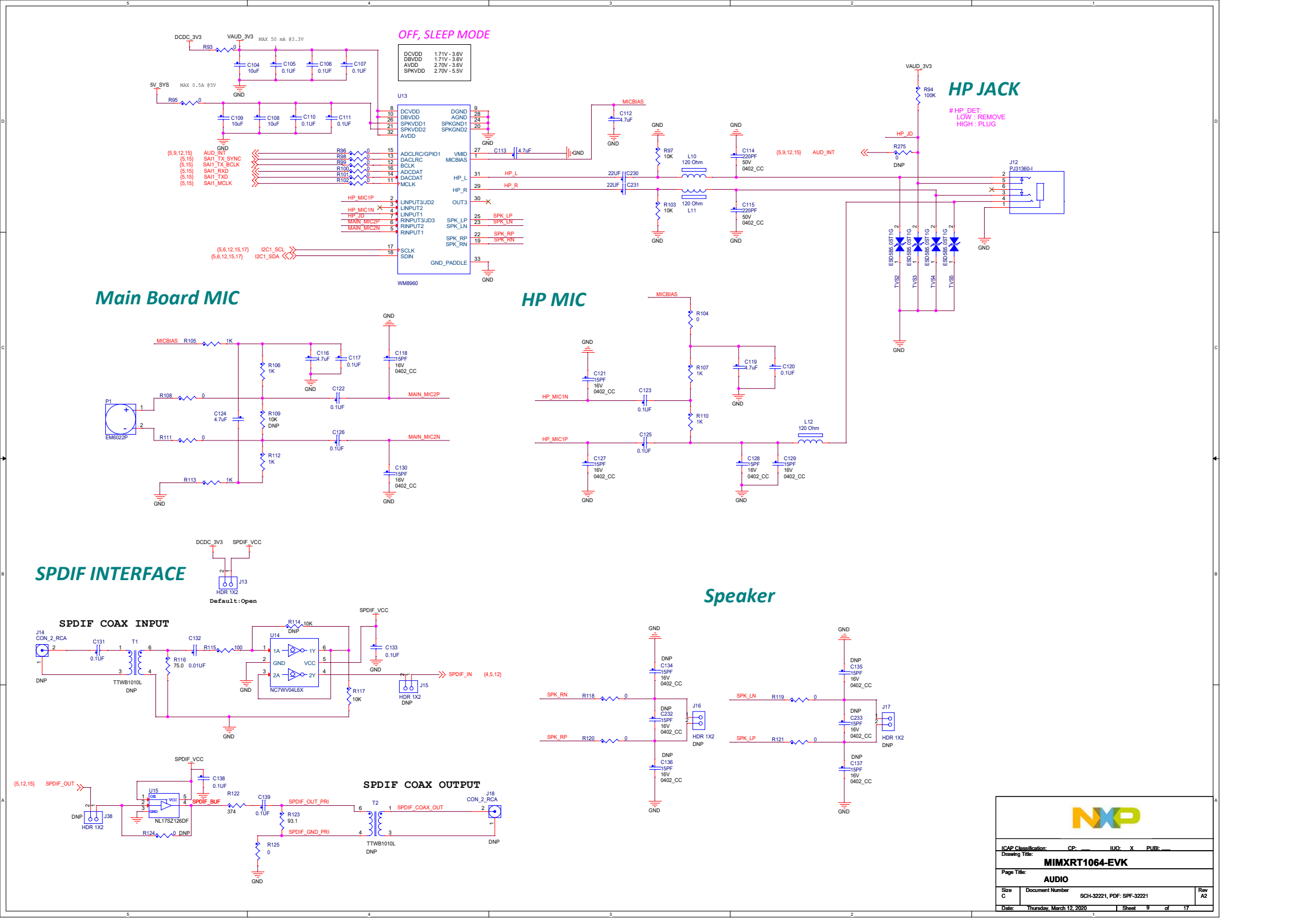
Size	Document Number	Rev
C	SCH-32221, PDF: SPF-32221	A2

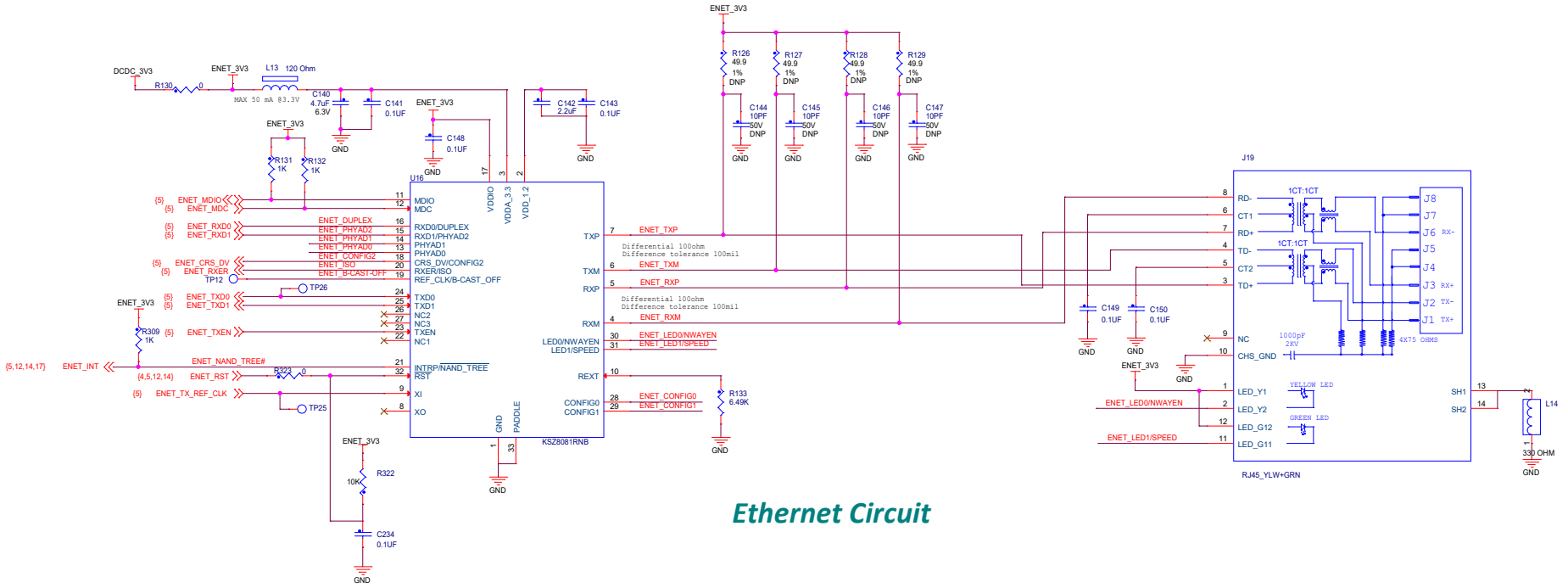
Date: Thursday, March 12, 2020 | Sheet 7 of 17

CAN BUS

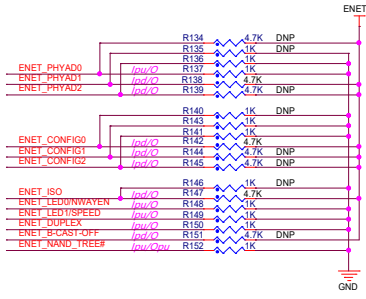


ICAP Classification:	CP: ___ IUO: X PUBI: ___	
Drawing Title:	MIMXRT1064-EVK	
Page Title:	CAN	
Size C	Document Number SCH-32221, PDF: SPF-32221	Rev A2
Date: Thursday, March 12, 2020	Sheet 8 of 17	


OFF, SLEEP MODE
DCVDD 1.71V - 3.6V
DBVDD 1.71V - 3.6V
AVDD 2.70V - 3.6V
SPKVDD 2.70V - 5.5V
U13
WM8960
HP JACK
HP_DET:
LOW : REMOVE
HIGH : PLUG
J12
PJ31360-I
Main Board MIC
HP MIC
SPDIF INTERFACE
Default:Open
SPDIF COAX INPUT
SPDIF COAX OUTPUT
Speaker
MIMXRT1064-EVK
AUDIO
ICAP Classification:
Drawing Title:
Page Title:
Size C
Document Number SCH-32221, PDF: SPF-32221
Rev A2
Date: Thursday, March 12, 2020
Sheet 9 of 17



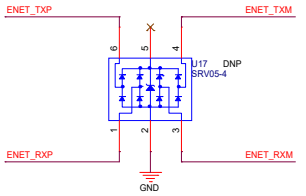
Ethernet Circuit



# CFG	Description
PHYAD[2:0]	PHY ADDR 00-XXX (00010 DEFAULT)
CONFIG[2:0]	IF MODE 001 RMII 101 RMII Back-to-Back xxx Reserved-not used
ISO	ISOLATE mode Pull-up = Enable Pull-down (default) = Disable
SPEED	SPEED mode Pull-up (default) = 100Mbps Pull-down = 10Mbps

# CFG	Description
DUPLEX	DUPLEX mode Pull-up (default) = Half Duplex Pull-down = Full Duplex
NWAYEN	Nway Auto-Negotiation Pull-up (default) = Enable Pull-down = Disable
B_CAST_OFF	Broadcast Off - for PHY Address 0 Pull-up = PHY Address 0 set as unique PHY addr Pull-down (default) = PHY Address 0 set as broadcast PHY addr
NAND_TREE#	NAND Tree Mode Pull-up (default) = Disable Pull-down = Enable

ESD PROTECTION



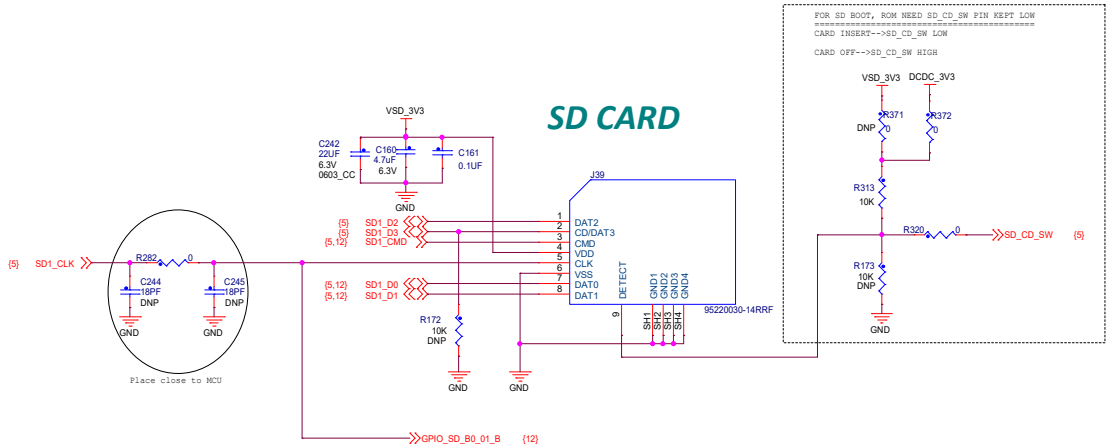
ICAP Classification: CP: ___ IUO: X PUBI: ___

Drawing Title: **MIMXRT1064-EVK**

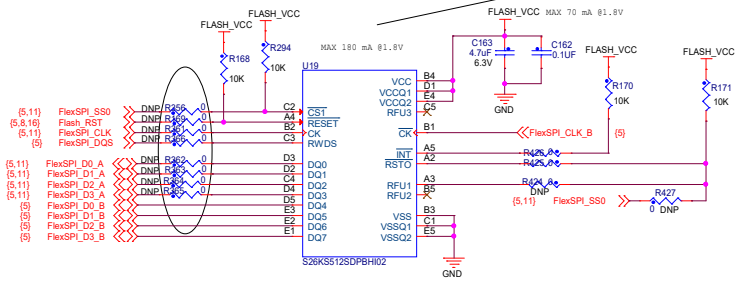
Page Title: **ETHERNET**

Size	Document Number	Rev
C	SCH-32221, PDF: SPF-32221	A2

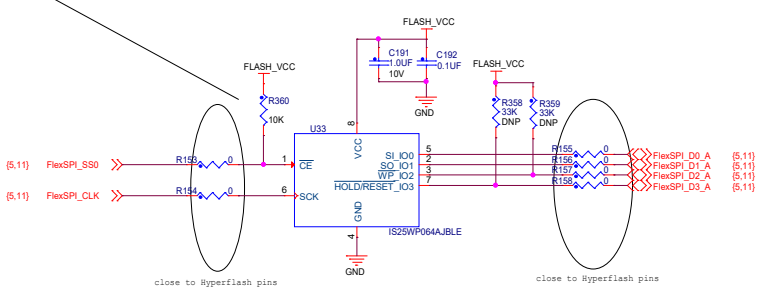
Date: Thursday, March 12, 2020 Sheet 10 of 17



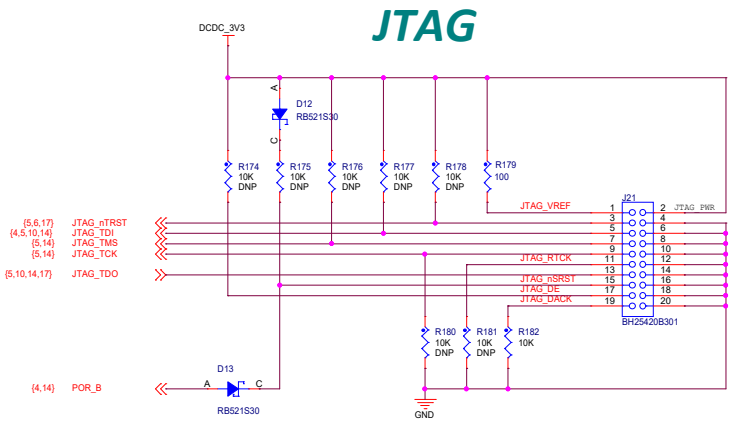
OPTION1: USE Hyperflash(DNP R153~R158, Mount R356,R361~R366)
OPTION2: USE QSPI FLASH(Mount R153~R158, DNP R356,R361~R366)



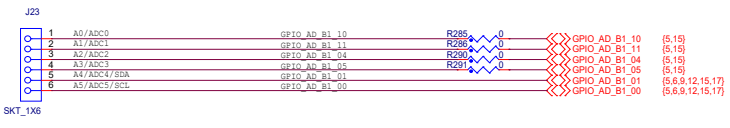
Share the same package with S27KS0641DPBHI023
(if HYPERRAM is replaced, then DNP R425,R426,Mount R424,R427)

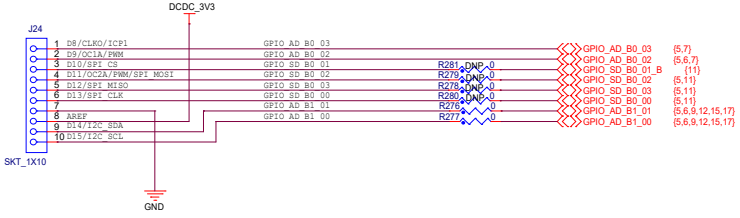


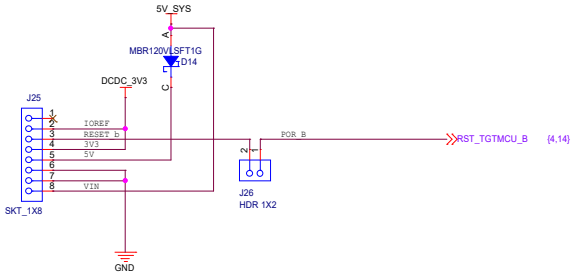
ICAP Classification:	CP: ___	IUO: X	PUBI: ___
Drawing Title:	MIMXRT1064-EVK		
Page Title:	SD/FLASH		
Size C	Document Number SCH-32221, PDF: SPF-32221		Rev A2
Date: Thursday, March 12, 2020	Sheet 11 of 17		



Arduino Interface

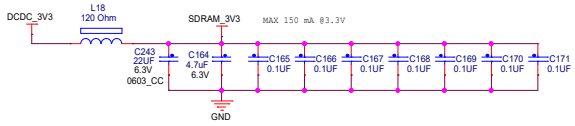


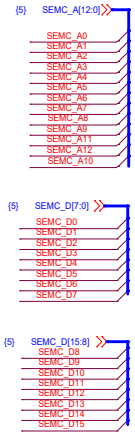


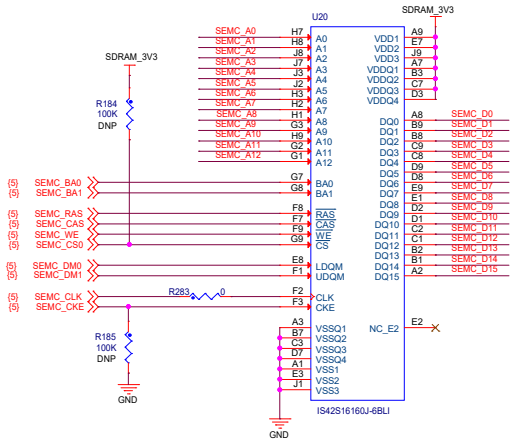


ICAP Classification:	CP: ___	IUO: X	PUBI: ___
Drawing Title:	MIMXRT1064-EVK		
Page Title:	DEBUG/JTAG		
Size: C	Document Number: SCH-32221, PDF: SPF-32221		Rev: A2
Date: Thursday, March 12, 2020	Sheet 12 of 17		

SDRAM

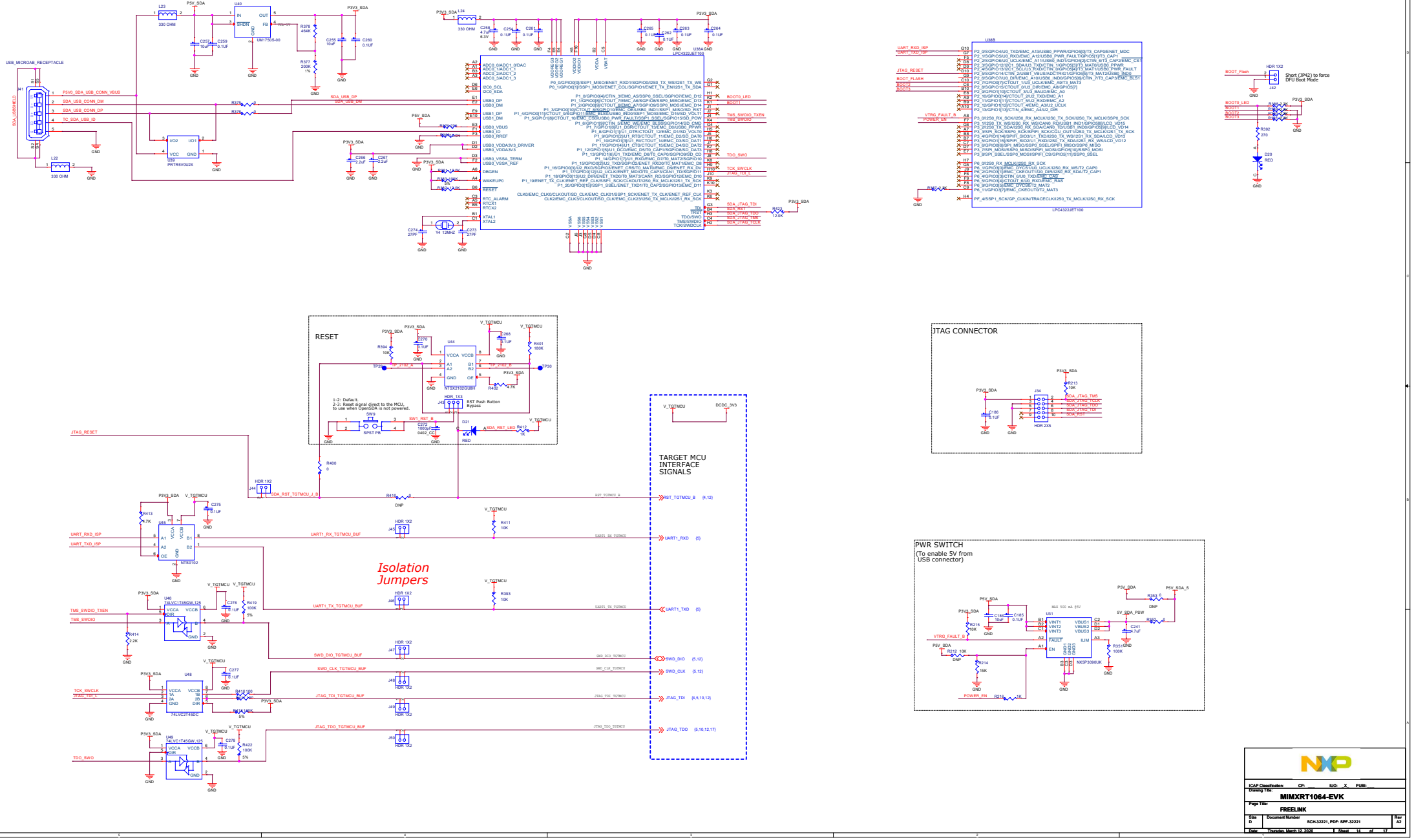




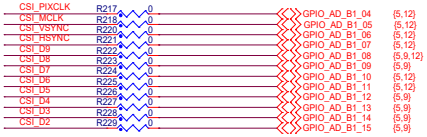


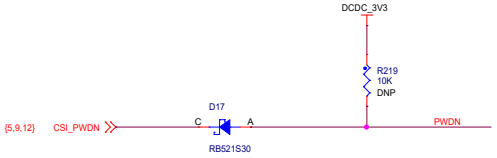
ICAP Classification:	CP: ___	IUO: X	PUBI: ___
Drawing Title:	MIMXRT1064-EVK		
Page Title:	SDRAM		
Size C	Document Number SCH-32221, PDF: SPF-32221		Rev A2
Date: Thursday, March 12, 2020		Sheet 13 of 17	

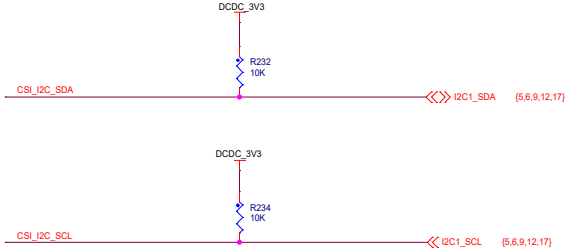
Freelink Interface



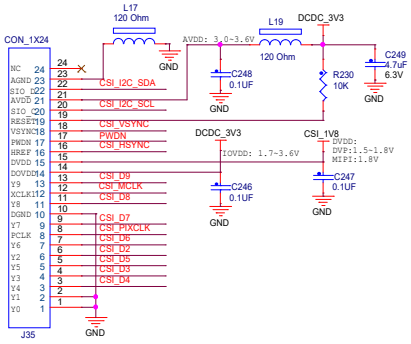
Camera Signals







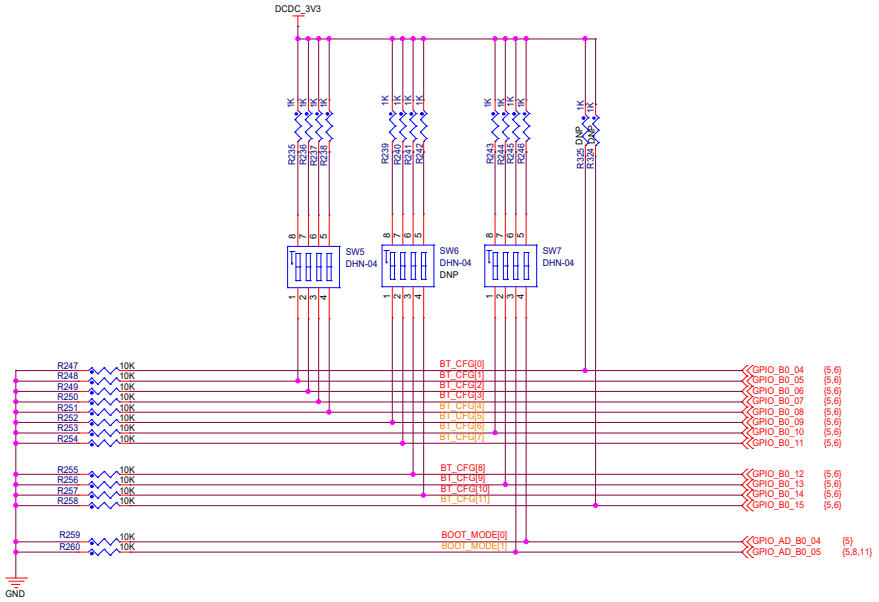
FPC FOR MT9M114/OV7725 MODULE



ICAP Classification:	CP: ___	IUO: X	PUBI: ___
Drawing Title:	MIMXRT1064-EVK		
Page Title:	CSI		
Size C	Document Number SCH-32221, PDF: SPF-32221		Rev A2
Date: Thursday, March 12, 2020	Sheet 15 of 17		

FUSE MAP

	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
TYPE	**BOOT_CFG[11]**	**BOOT_CFG[10]**	**BOOT_CFG[9]**	**BOOT_CFG[8]**	**BOOT_CFG[7]**	**BOOT_CFG[6]**	**BOOT_CFG[5]**	**BOOT_CFG[4]**	**BOOT_CFG[3]**	**BOOT_CFG[2]**	**BOOT_CFG[1]**	**BOOT_CFG[0]**
FlexSPI1 - Serial NOR	*Infinit-Loop: (Debug USE only) 0 - Disable 1- Enable*	*FLASH_TYPE 000-Device supports 3B read by default 001-Device supports 4B read by default 010-HyperFlash 1V8 011-HyperFlash 3V3 100-MXIC Octal DDR*			*0*	*0*	*0*	*0*	*HOLD TIME: 00 - 500us 01 - 1ms 10 - 3ms 11 - 10ms*		*EncryptedXIP 0 - Disabled 1- Enabled*	*Reserved*
SD	*Infinit-Loop: (Debug USE only) 0 - Disable 1- Enable*	*Reserved*	*Bus Width: 0 - 1-bit 1 - 4-bit*	*SD1 VOLTAGE SELECTION: 0 - 3.3V 1 - 1.8V*	*0*	*1*	*SD/SDXC Speed: 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104*		*SD Power Cycle Enable: '0' - No power cycle '1' - Enabled via USDHC_RST pad*	*SD Loopback Clock Source Sel: (for SDR50 and SDR104 only) '0' - through SD '1' - direct*	*Port Select: 0 - eSDHC1 1 - eSDHC2*	*Fast Boot: 0 - Regular 1 - Fast Boot*



ICAP Classification: CP: ___ IUO: X PUBI: ___

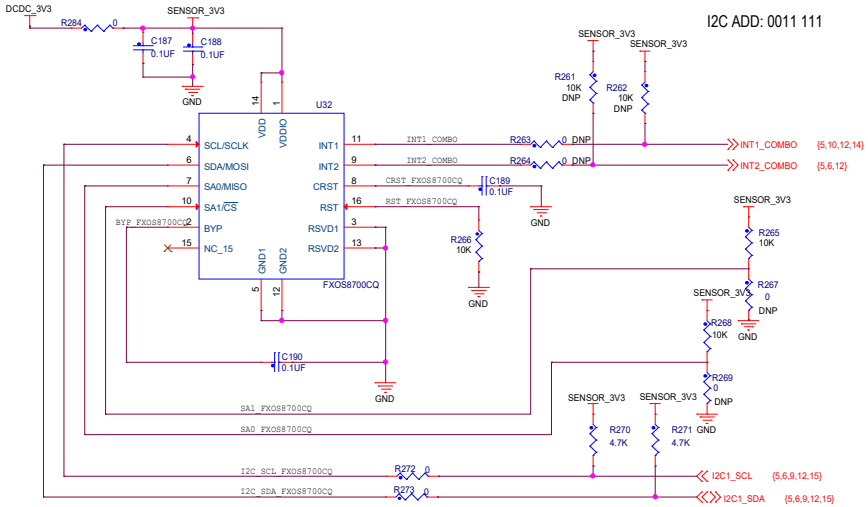
Drawing Title: **MIMXRT1064-EVK**

Page Title: **BOOT**

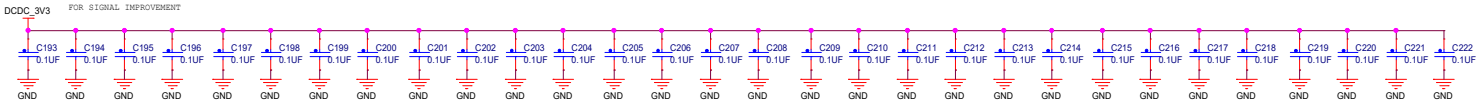
Size	Document Number	Rev
C	SCH-32221, PDF: SPF-32221	A2

Date: Thursday, March 12, 2020 Sheet 16 of 17

COMBO SENSOR



FXOS8700CQ COMBO SENSOR



ICAP Classification:	CP: ___	IUO: X	PUBI: ___
Drawing Title:	MIMXRT1064-EVK		
Page Title:	MISC		
Size: C	Document Number: SCH-32221, PDF: SPF-32221		Rev: A2
Date: Thursday, March 12, 2020	Sheet 17 of 17		