



Islamic University of Technology (IUT)

Organization of Islamic Cooperation (OIC)



**Department of Electrical and Electronic Engineering
(EEE)**

Report Submission Date: 21st May, 2018

Course: EEE 4308 (Digital Electronics Lab)

Experiment Name: Basic Calculator Design using Logic Gates.

Name	: Md Mohi Uddin Khan
Student ID	: 160021163
Section	: C1
Course Name	: Digital Electronics Lab.
Course No.	: EEE 4308

INTRODUCTION:

The project to be submitted is a simple calculator using only logic gates. For this, I designed some separate units for different action. They are:

1. Adder Subtractor unit
2. Multiplier unit
3. Divider unit
4. Input keyboard unit
5. Memory unit
6. Display unit

Adder-Subtractor Unit

In this unit the operations of addition and subtraction of single digit (4 bit Binary) decimal number, I used 2 Full Adders, 2 XOR gate IC, 1 Not gate IC, 1 AND gate IC, 1 OR gate IC. These are 1st logically derived in my note book.

*** Adder - Subtractor unit design:

Sample cases:

(i) $\begin{array}{r} 9 \\ (+) 8 \\ \hline 17 \end{array}$

(ii) $\begin{array}{r} 8 \\ (+) 9 \\ \hline 17 \end{array}$

(iii) $\begin{array}{r} 9 \\ (-) 8 \\ \hline 1 \end{array}$

(iv) $\begin{array}{r} 8 \\ (-) 9 \\ \hline -1 \end{array}$

(iii) $\begin{array}{r} 1001 \\ (-) 1000 \\ \hline \end{array}$

2's Complement of B: (+)

$$\begin{array}{r} 1001 \\ 1000 \\ \hline 10001 \end{array}$$

Carry 1
Sign flag for '+'

(iv) $\begin{array}{r} 1000 \\ (-) 1001 \\ \hline \end{array}$

2's comp of B: (+)

$$\begin{array}{r} 1000 \\ 0111 \\ \hline 01111 \end{array}$$

Carry 0
If Without Cout rest portion is complemented (if 2) (bcz, there's no end carry):

$$\begin{array}{r} 01111 \\ 0111 \\ \hline 01001 \end{array}$$

Sign flag for '-'

(i) & (ii)

$$\begin{array}{r} 1001 \\ (+) 1000 \\ \hline 10001 \end{array}$$

checker

$$\begin{array}{r} (+) 110 \\ \hline 10111 \\ \hline 17 \end{array}$$

So, For addition C_{in} (i.e. C_0 in IC) is 0; I need a checker & +6 adder.
 For subtraction C_{in} (i.e. C_0 in IC) is 1; I don't need a BCD checker & +6 adder. But we need a checker for the determination of addition or subtraction operation using which we can invert the Cout (sample case iii & iv) or using which we can do this task.

Adder-Subtractor checker: ^{whether} output X_1 will decide, 2's complement of $S_3 S_2 S_1 S_0$ is needed or not. X_1 is also the C_{in} of the 2nd F/A IC.

C_{in}	C_{out}	X_1
0	0	0
0	1	0
1	0	1
1	1	0

$$\therefore X_1 = C_{in} \overline{C_{out}}$$

C_{in} & X_1 '1' means subtraction operation.
'0' means addition operation.

Invalid BCD checker:

C_{in}	C_{out}	$P_3 P_2 P_1 P_0$	F
0	0	0 to 9	0
means addition operation	0	10 to 15	1
	1	16 to 19	
	1	20 to 31	X → don't care
means subtraction operation	1	0 or 1	0
	1	10 to 15	X

$C_{out} = 0$						$C_{out} = 1$						$C_{out} = 0$						$C_{out} = 1$					
$P_3 P_2$	$P_3 P_2$	00	01	11	10	$P_3 P_2$	$P_3 P_2$	00	01	11	10	$P_3 P_2$	$P_3 P_2$	00	01	11	10	$P_3 P_2$	$P_3 P_2$	00	01	11	10
00						00		1	1	1	1	00						00					
01						01		X	X	X	X	01						01					
11		1	1	1	1	11		X	X	X	X	11		X	X	X	X	11		X	X	X	X
10				1	1	10		X	X	X	X	10				X	X	10			X	X	

$C_{in} = 0$

$C_{in} = 1$

$C_{in} = 0$

$C_{in} = 1$

$$\therefore F = \overline{C_{in}} (C_{out} + P_3 P_2 + P_3 P_1) = \overline{C_{in}} \{C_{out} + P_3 (P_1 + P_2)\}$$

For MSB 7 Segment Display: Either 1 or - will be displayed. '1' in case of addition & '-' in case of subtraction (B7A).
Truth table for active low converter design because common anode 7 segment display is used.

	Cin	Car	Cor	d	e	f	g
means addition	0	0	0	0	0	0	0
	0	0	1	1	1	0	0
	0	1	0	1	1	0	0
	0	1	1	X	X	X	X
means subtraction	1	0	0	0	0	0	1
	1	0	1	X	X	X	X
	1	1	0	0	0	0	0
	1	1	1	X	X	X	X

$$\begin{aligned}
 b \& c &= \overline{(\overline{Car} + \overline{Cor}) \overline{Cin}} \\
 &= \overline{Car + Cor + Cin} \\
 &= \overline{Car} \cdot \overline{Cor} + \overline{Cin}
 \end{aligned}$$

Referring to the sample cases: If 2's complement can be done in 2nd step; '-' comes in that step. So, checker for that step can be used for '-' display.

So, $g = \overline{X_1}$ for active low converter design.

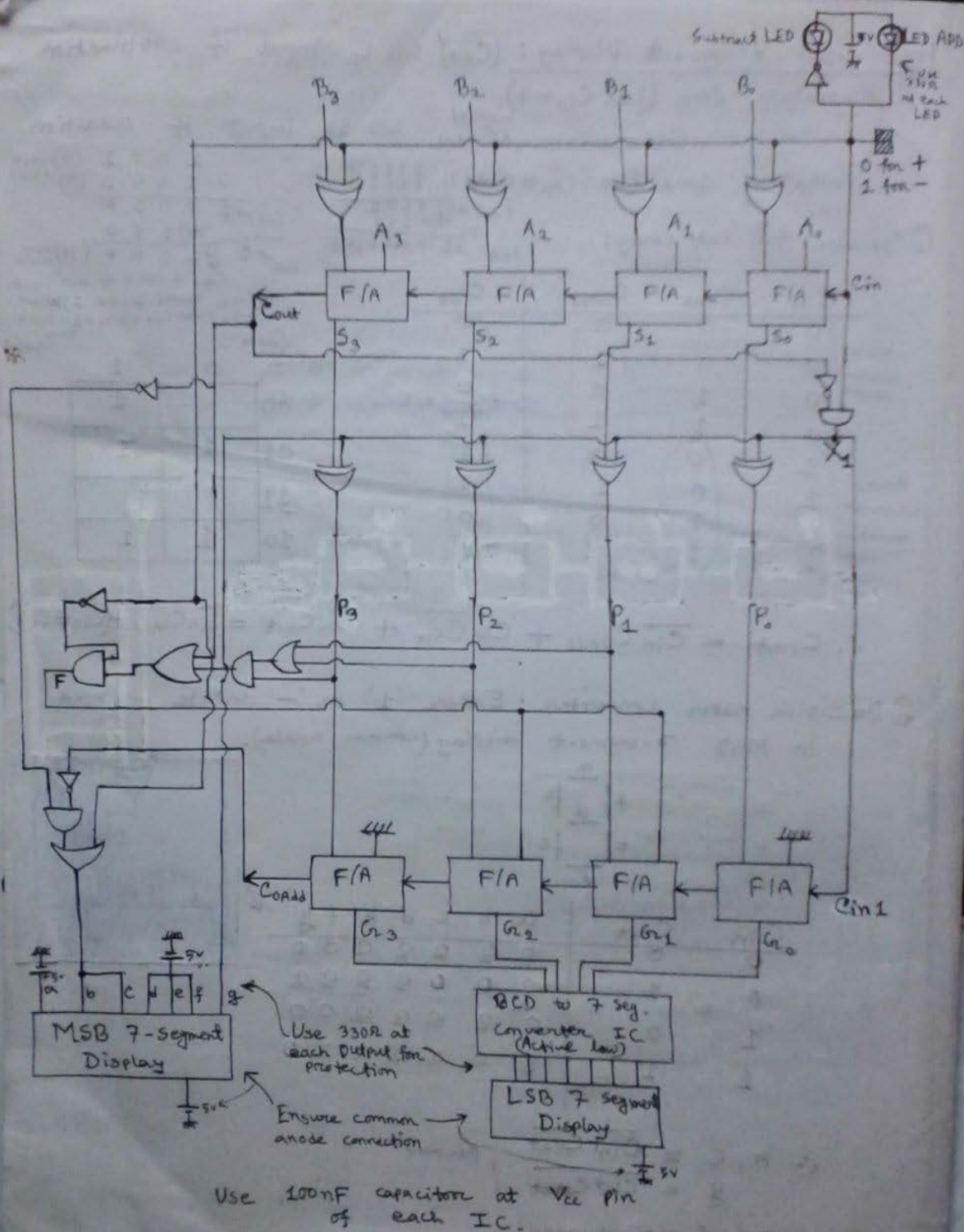
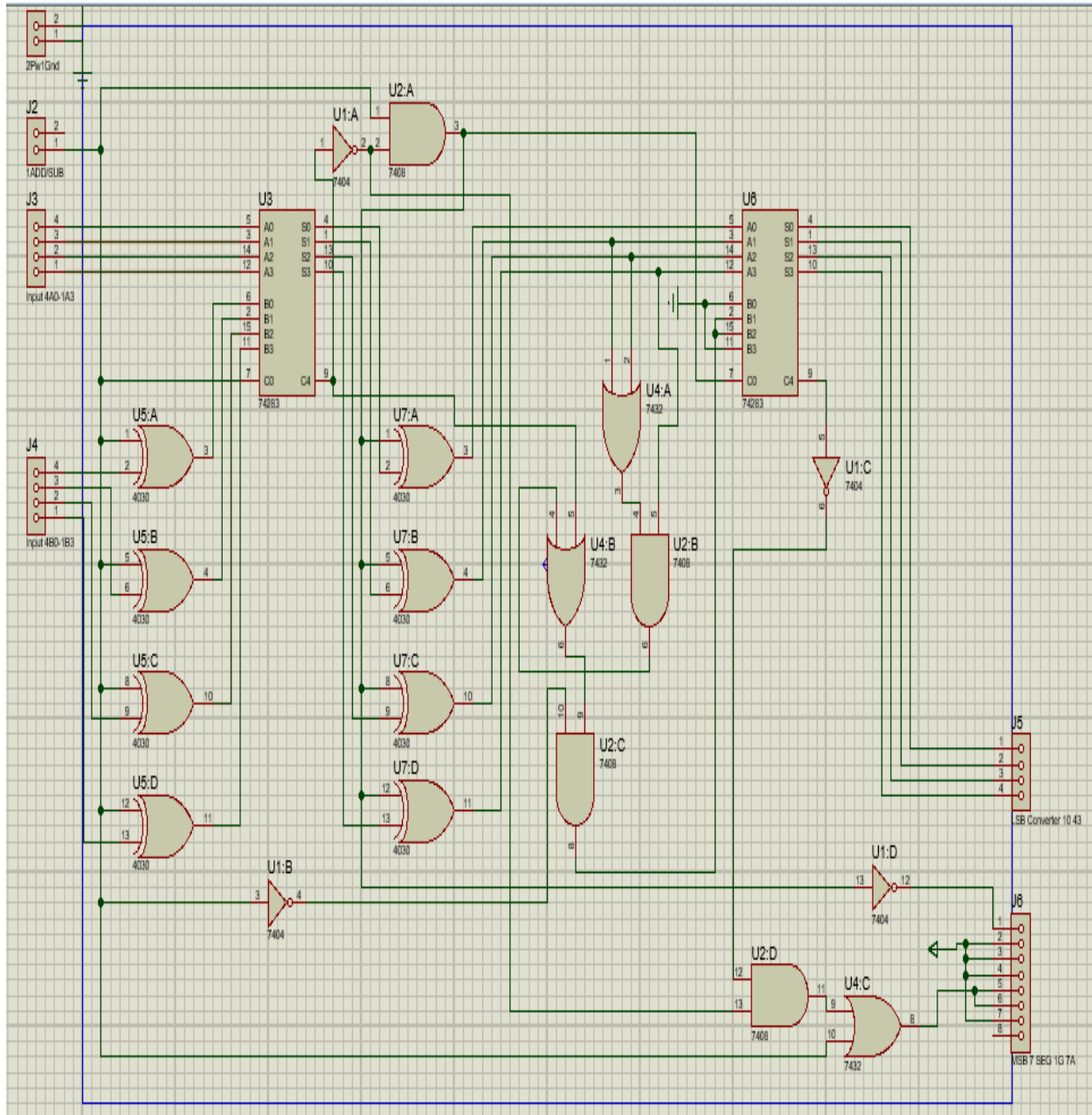
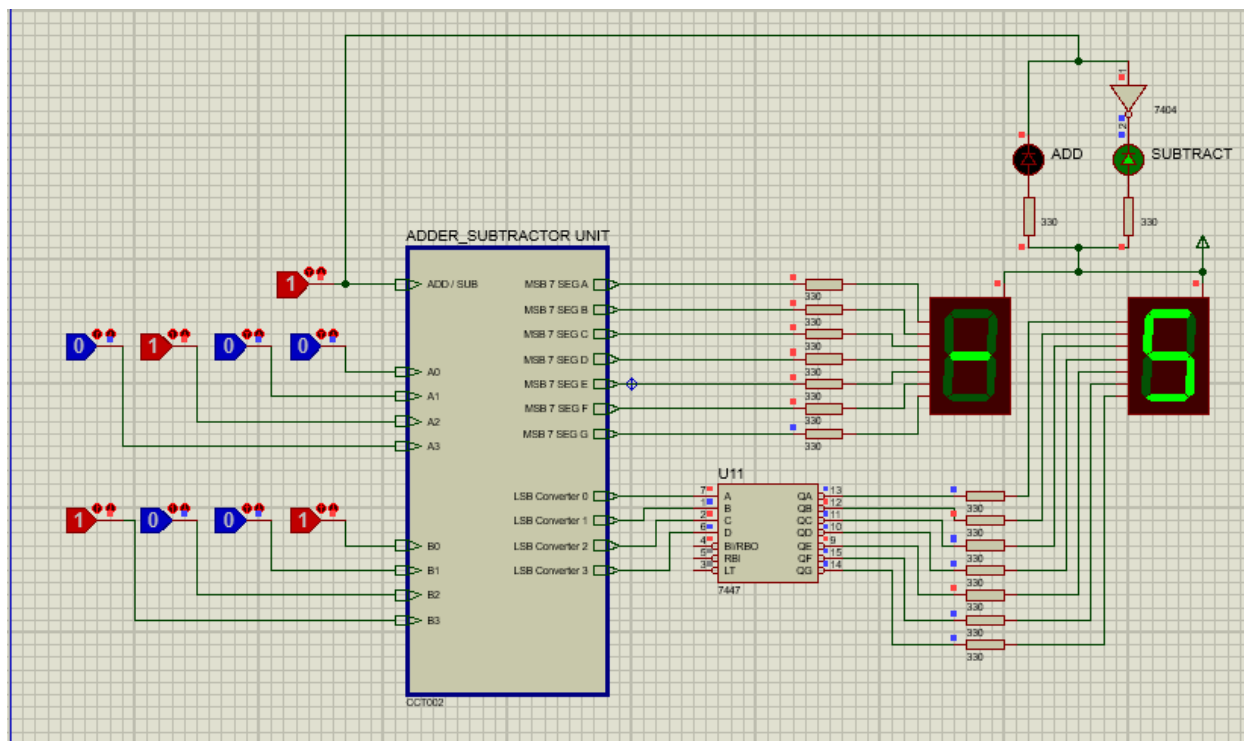
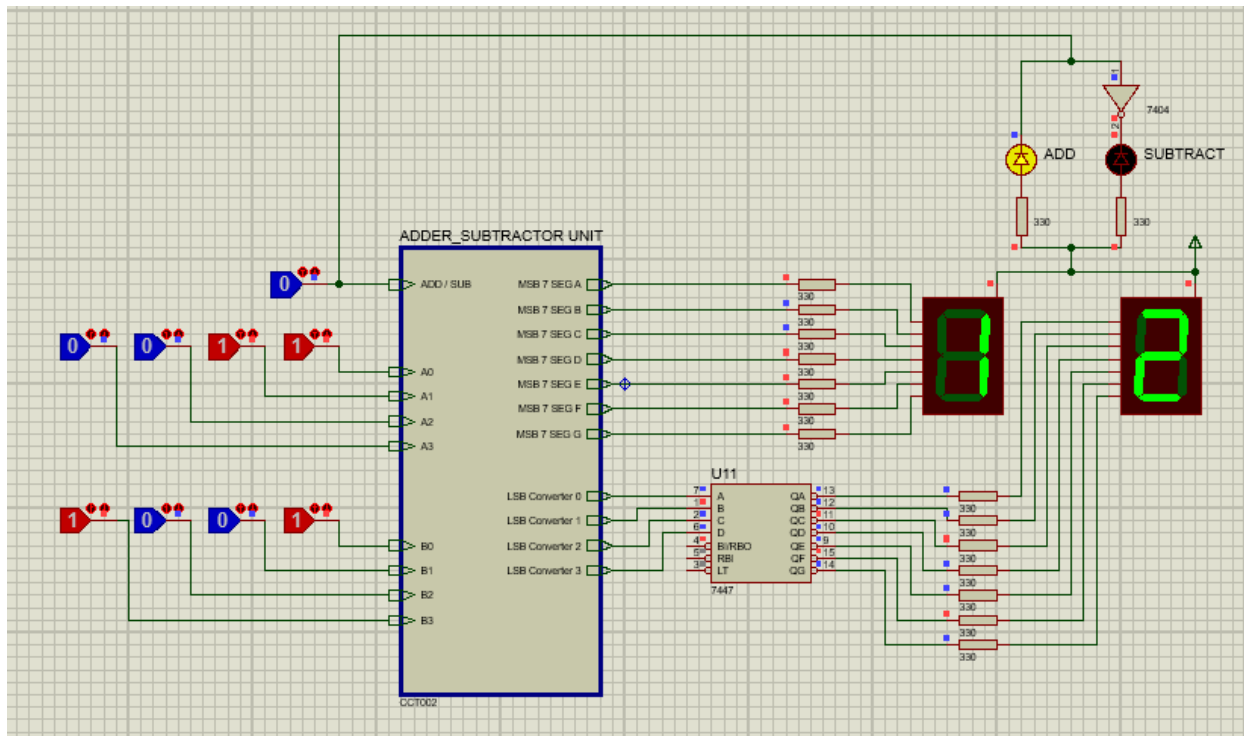


Fig : Circuit diagram of Adder-Subtraction Unit.

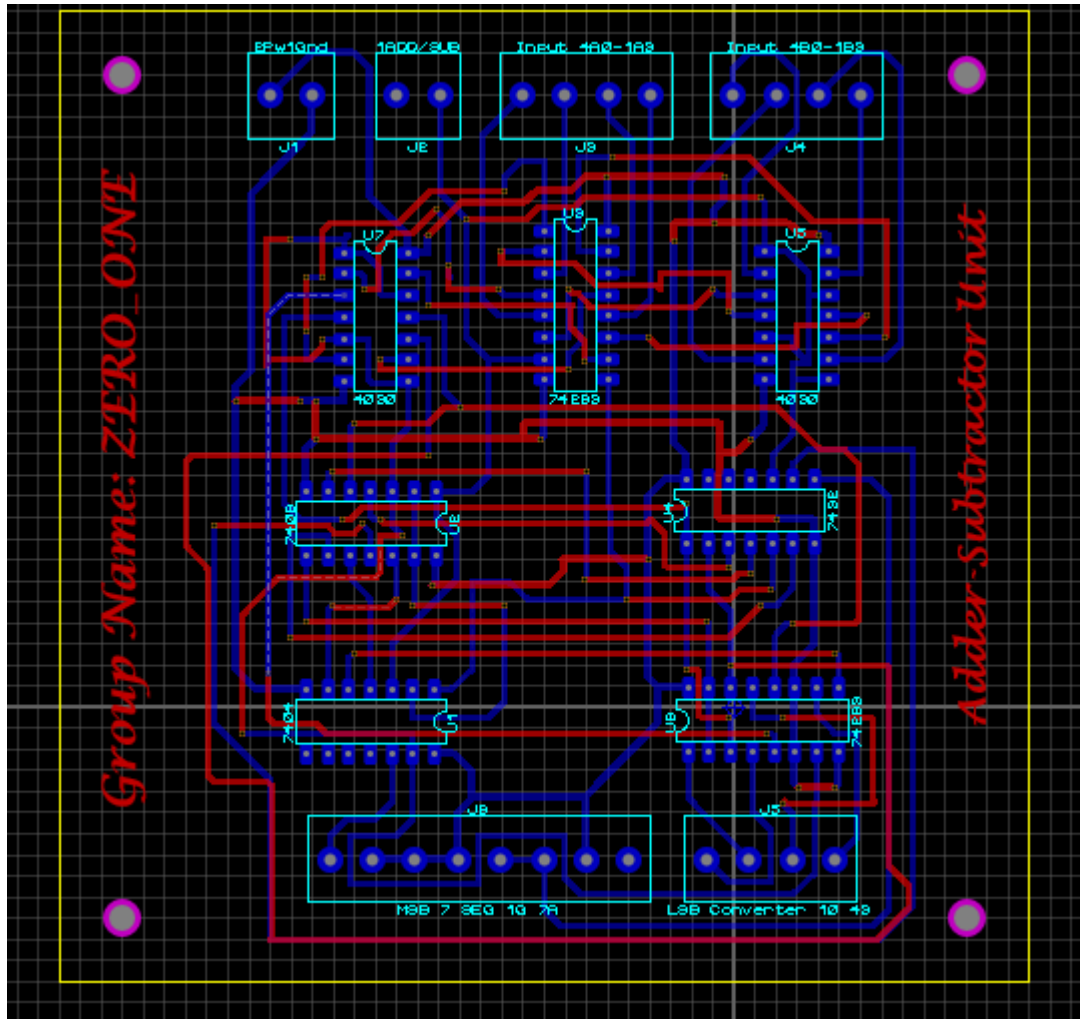
Then these were implemented in Proteus 8.



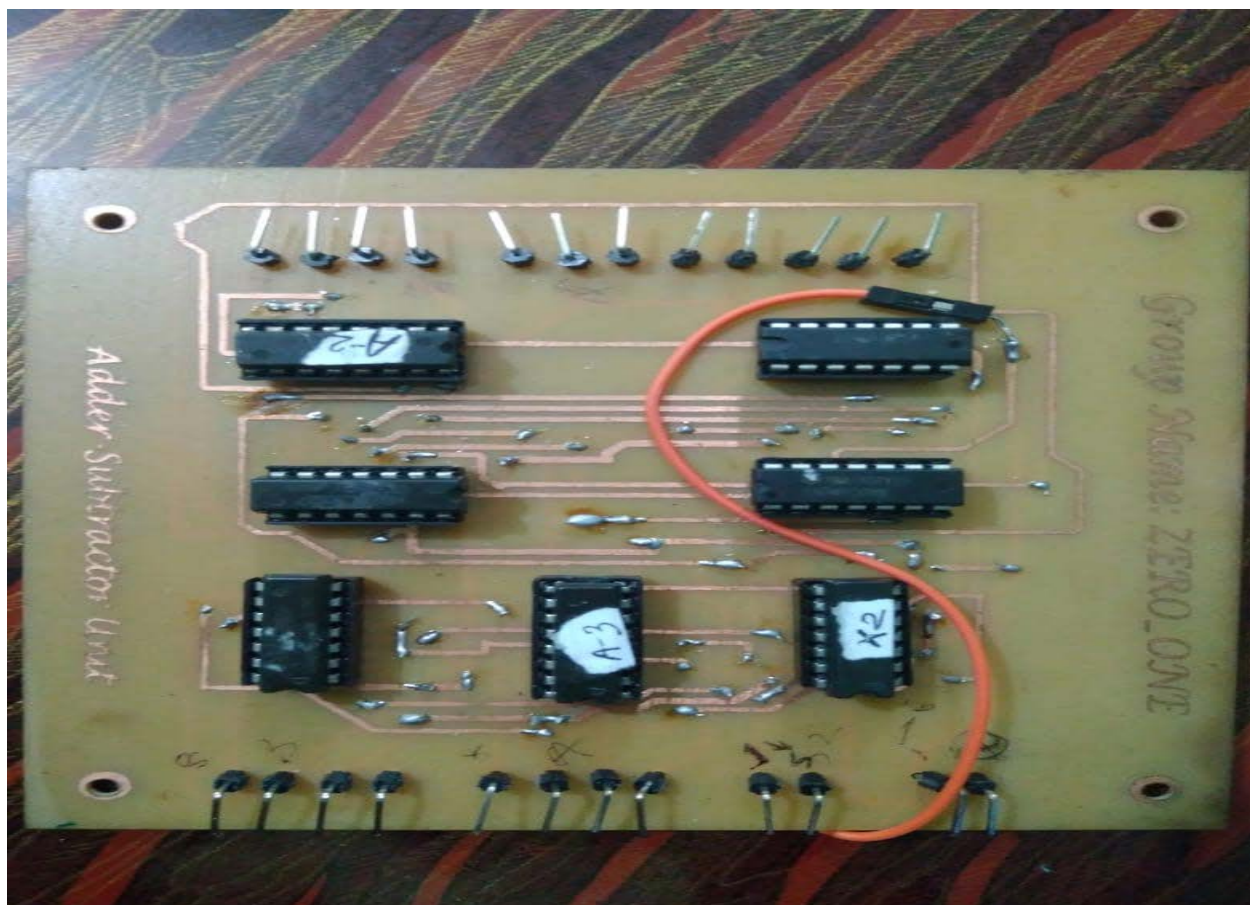
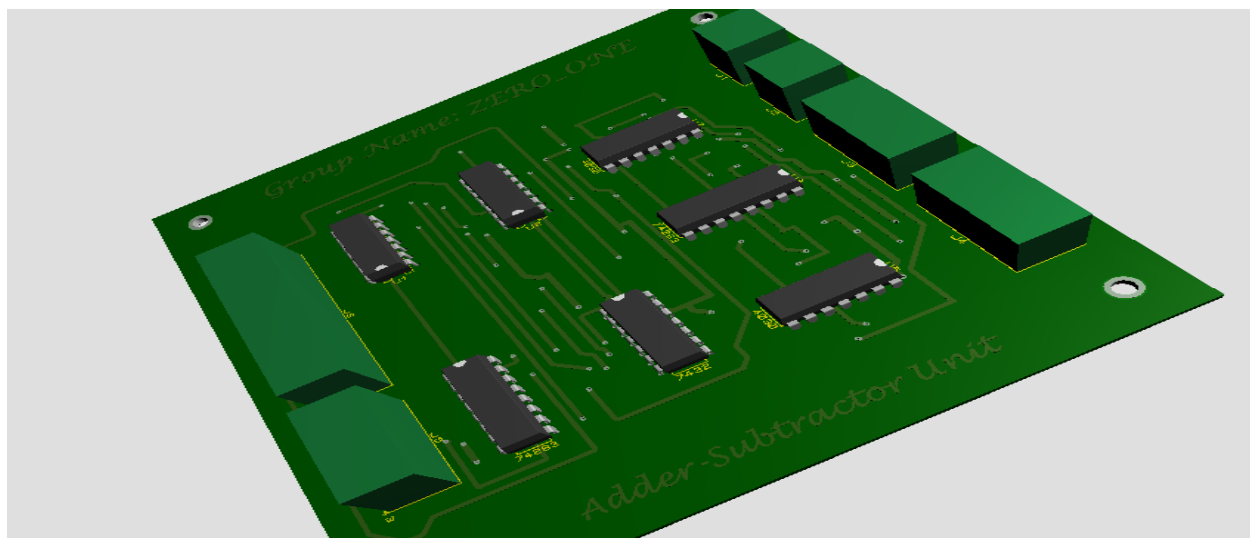
The output obtained as desired. The output are shown in 7 segment common anode display.



Then, I had done the PCB design. Here 1st I had to make slight changes to our design by adding terminal blocks instead of logic-states and logic-probes. Then this was used to design the final PCB layout. I processed the PCB to be double layered. So the remaining connections had to be done.



Finally the PCB design was completed. And the 3D design along with the original PCB is given below:

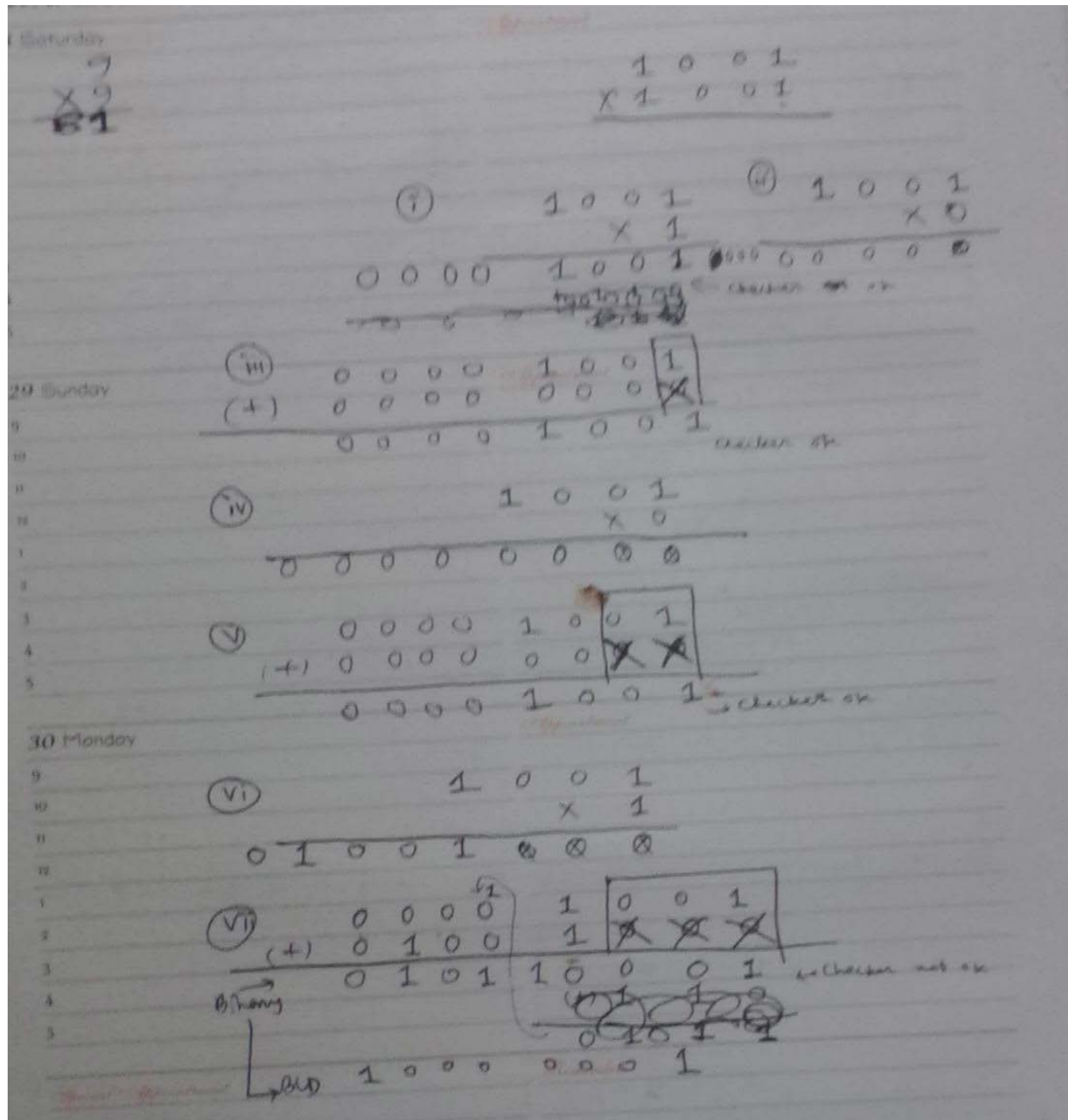


Multiplier:

In this unit the operations of addition and subtraction of single digit, 4 bit decimal number. Here I used 7 AND gate IC, 8 full adders, 3 OR gate IC and an Encoder.

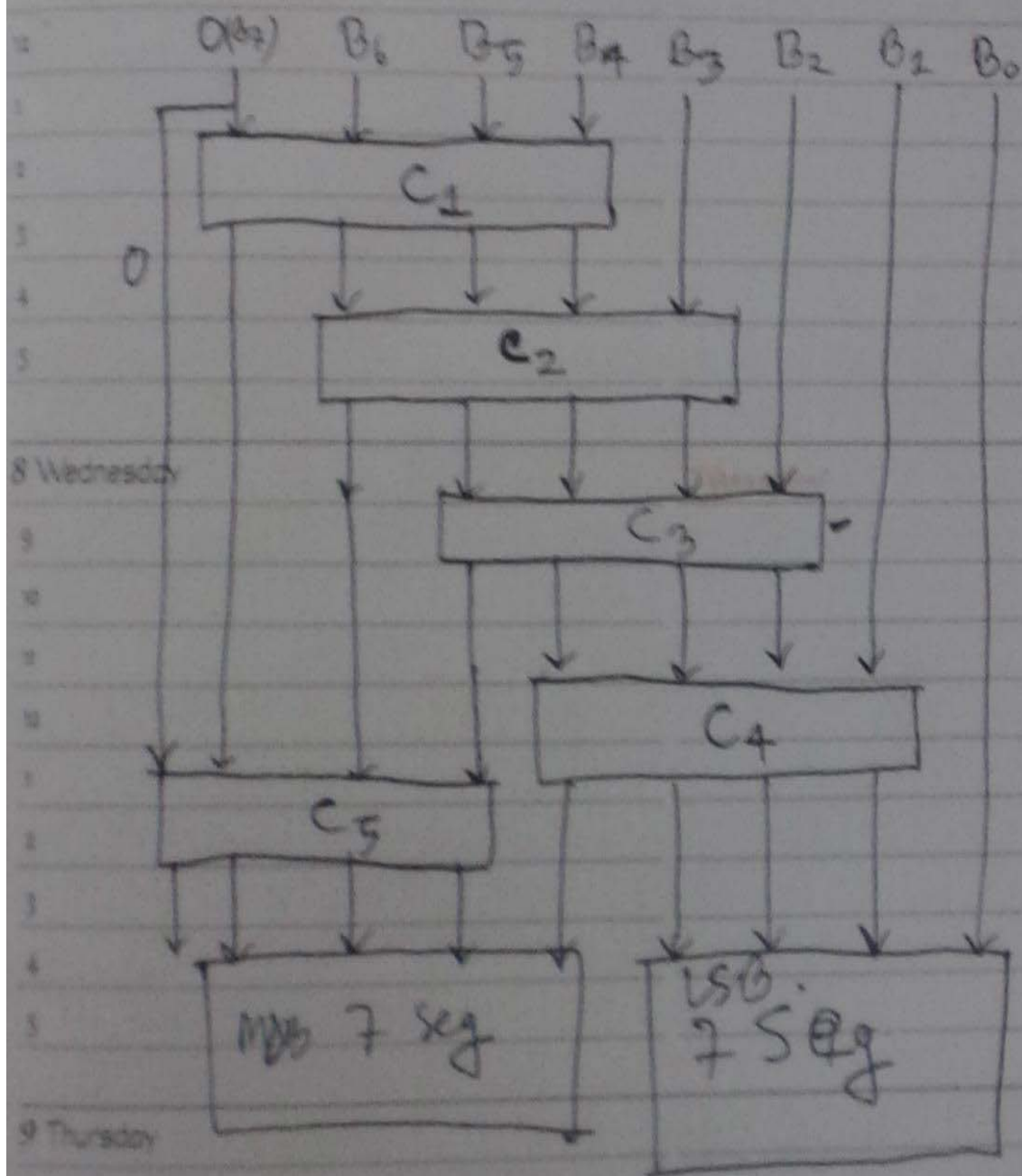
Then as before the steps are performed

1st the written rough calculations:



7 Tuesday

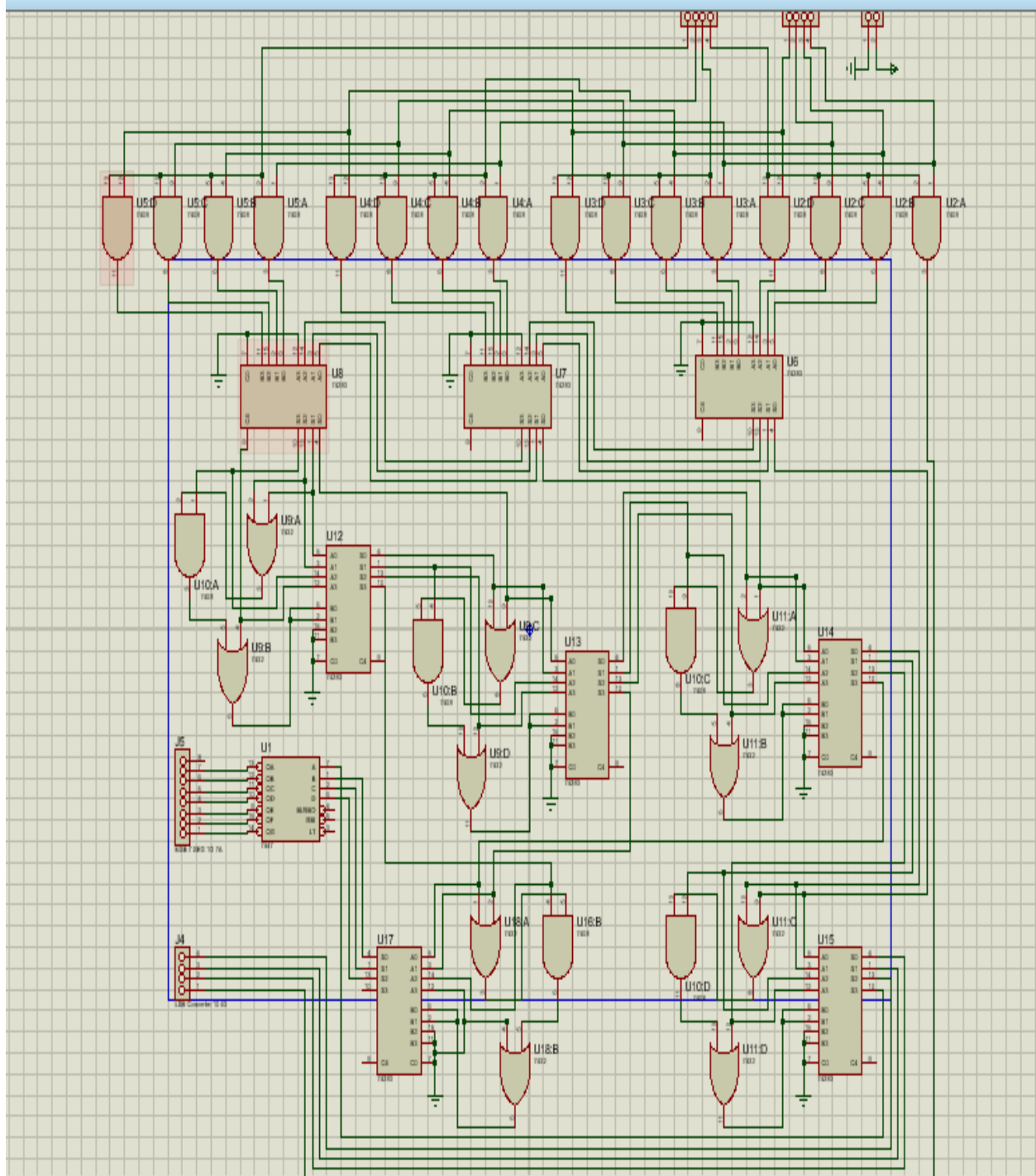
Binary to B4 Convert using Double-Dabble:



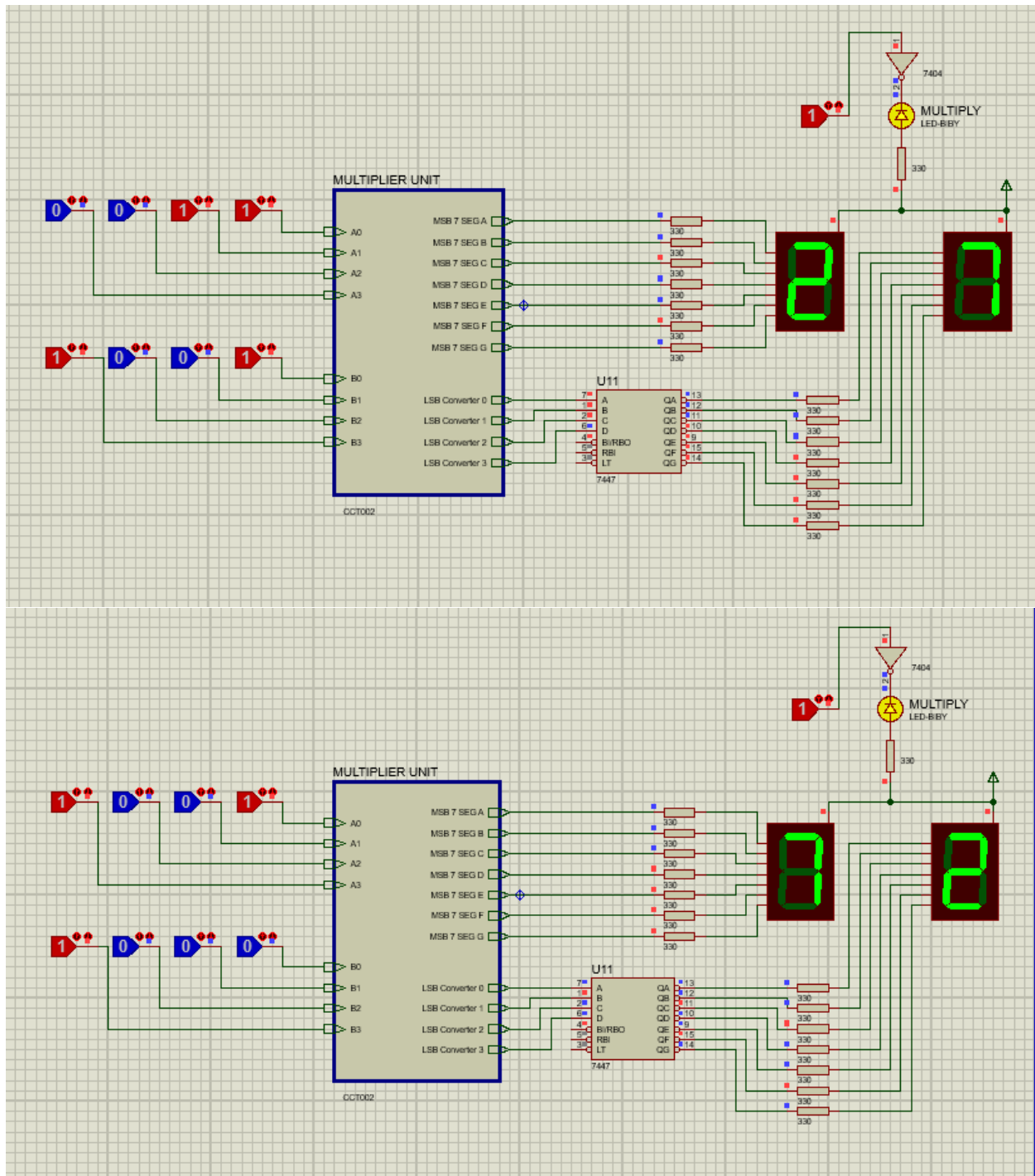
8 Wednesday

9 Thursday

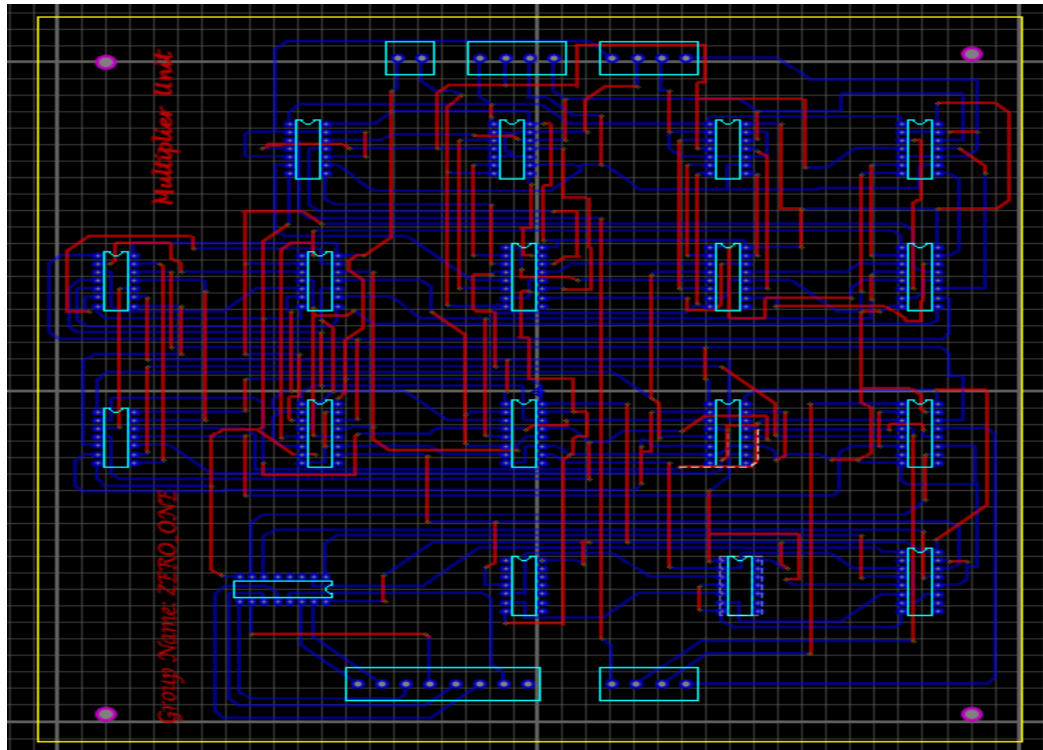
Then the proteus Implementation:



The outputs are checked and obtained as desired:



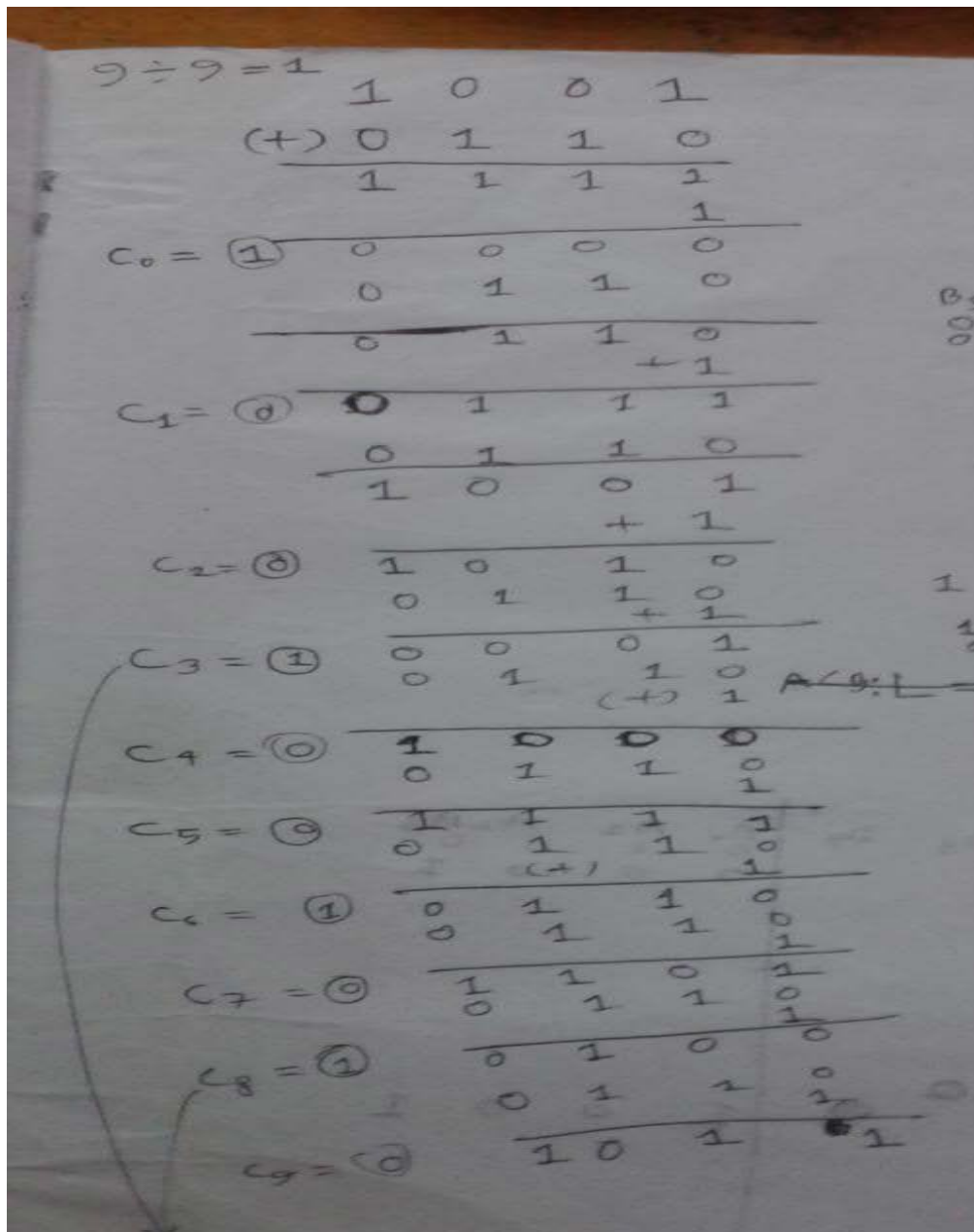
Then after adding the terminal blocks the PCB design was made and printed:



Divider Unit

In this unit of the Division operation single digit (4 bit binary) decimal number is divided by another single digit Decimal number. But in this particular divider, the decimal places (i.e. Remainders) are not shown. Only the integer will be displayed. Here I used a total of 18 ICs including 9 Full adders, 4 Inverter IC, 2 OR gate IC, 2 AND gate IC and an 10 to 4 line Encoder.

As before the logical calculations and designs are done by hand calculation.



Unit

20 = 4 Enc

	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	D ₈	D ₉	A ₀	A ₁	A ₂	A ₃
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10	0	0	0	0	0	0	0	0	0	0	1	0	0	1

Truth table for 10 to 4 line Encoder
used for summing up the required
carry outs which is the quotient.

For ERROR: If 2nd Input B is 0 then E will be shown in MSB
 & LSB display will be off.
 7 seg display. Otherwise B will be off. Let's take input B as 0000
 efficient in design.

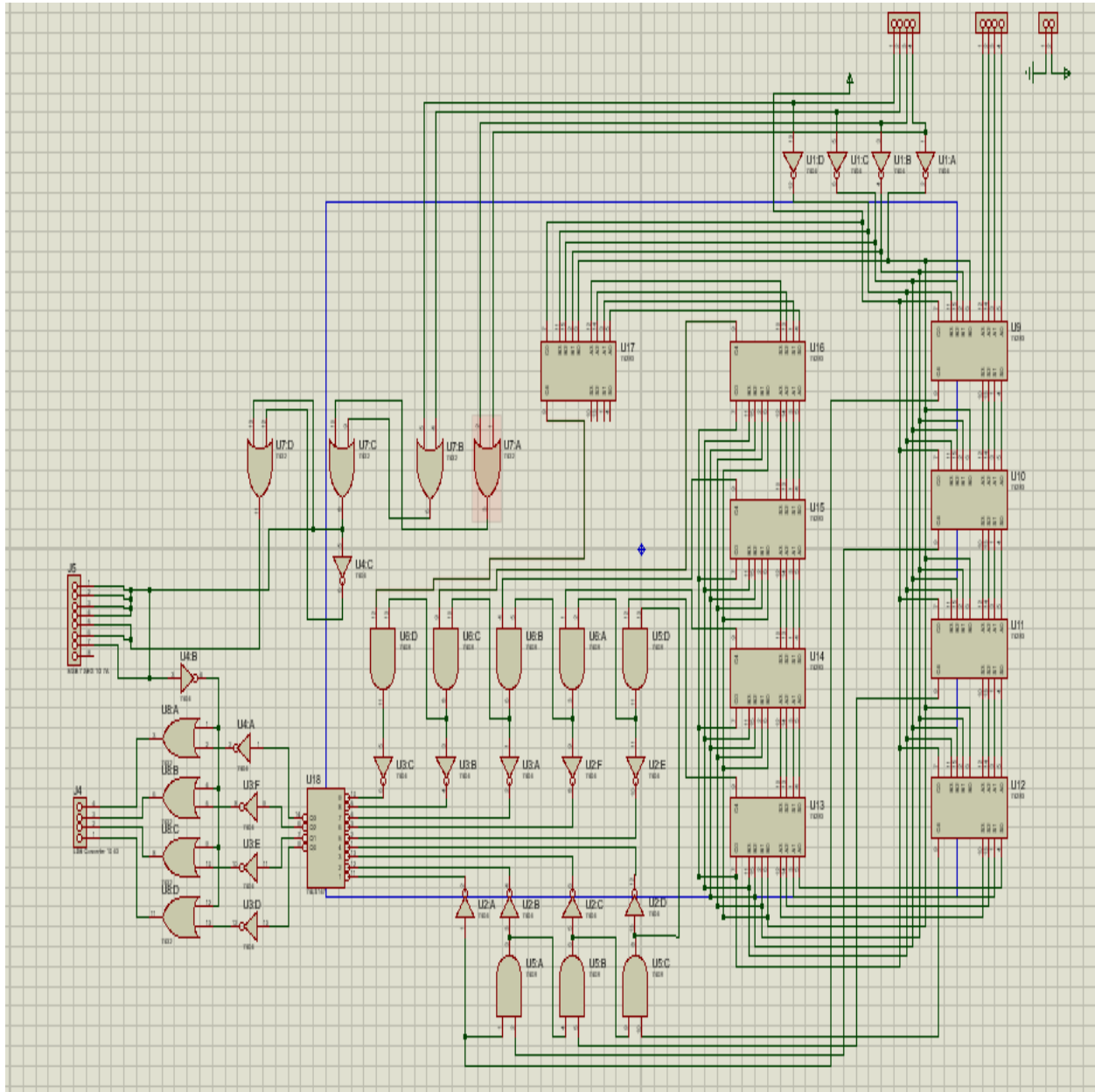
Active Low common design

$\overline{B_3}$	$\overline{B_2}$	$\overline{B_1}$	$\overline{B_0}$	X_{MSB}	a	b	c	d	e	f	g
0	0	0	0	0	0	1	1	0	0	0	0
0	0	0	1	1	1	1	1	1	1	1	1
0	0	1	0	1							
0	0	1	1	1							
0	1	0	0	1							
0	1	0	1	1							
0	1	1	0	1							
0	1	1	1	1							
1	0	0	0	1							
1	0	0	1	1							
1	0	1	0	1							
1	0	1	1	1							
1	1	0	0	1							
1	1	0	1	1							
1	1	1	0	1							
1	1	1	1	1							

$\therefore X = \overline{B_0} + \overline{B_1} + \overline{B_2} + \overline{B_3}$
 $a, d, e, g = X_{MSB}$
 $b, c = \overline{X_{MSB}} + X_{MSB}$
 7 seg LSB = $\overline{X_{MSB}} + (a, b, c, d)$ of 7 seg display

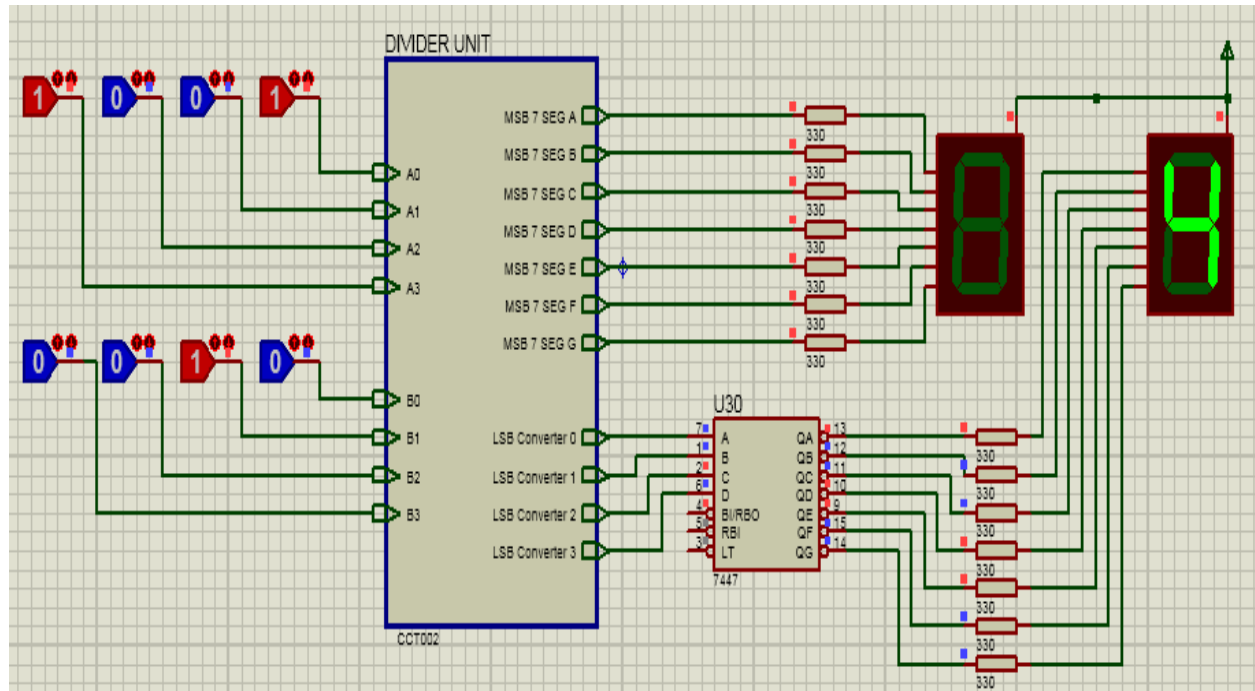
Truth table & Boolean Expression for Showing 'E' (Error) in case of any digit divided by zero.

Then done the Proteus Implementation and output generation.

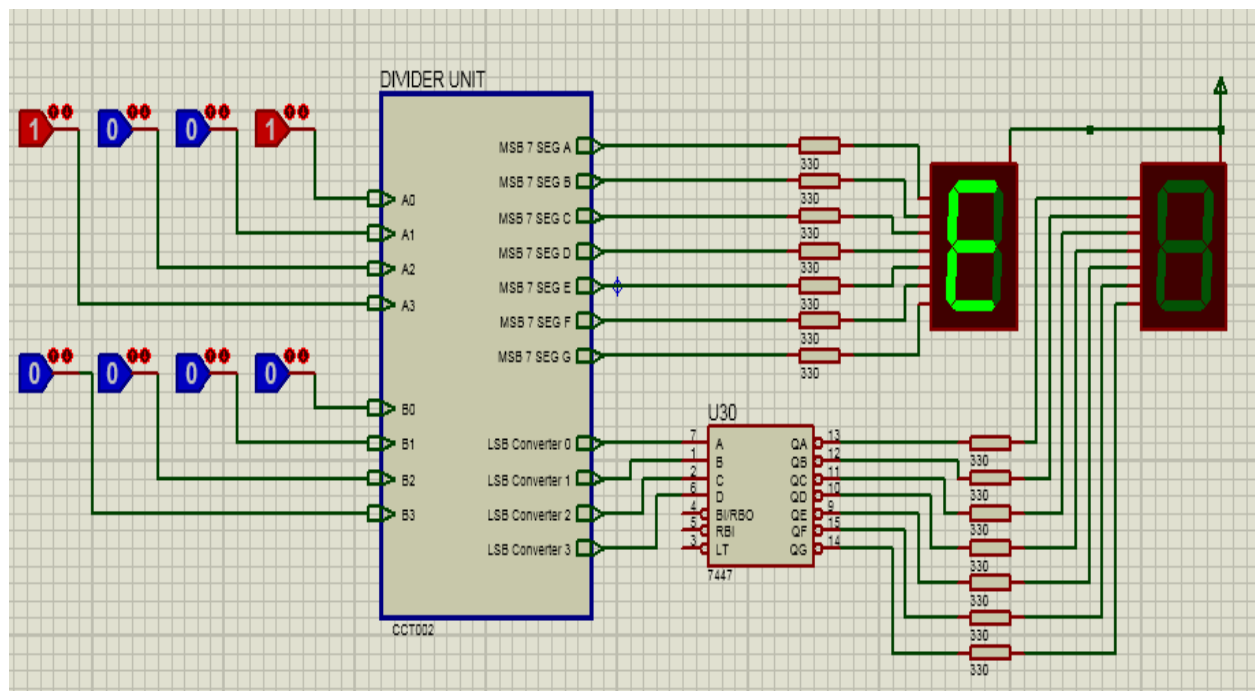


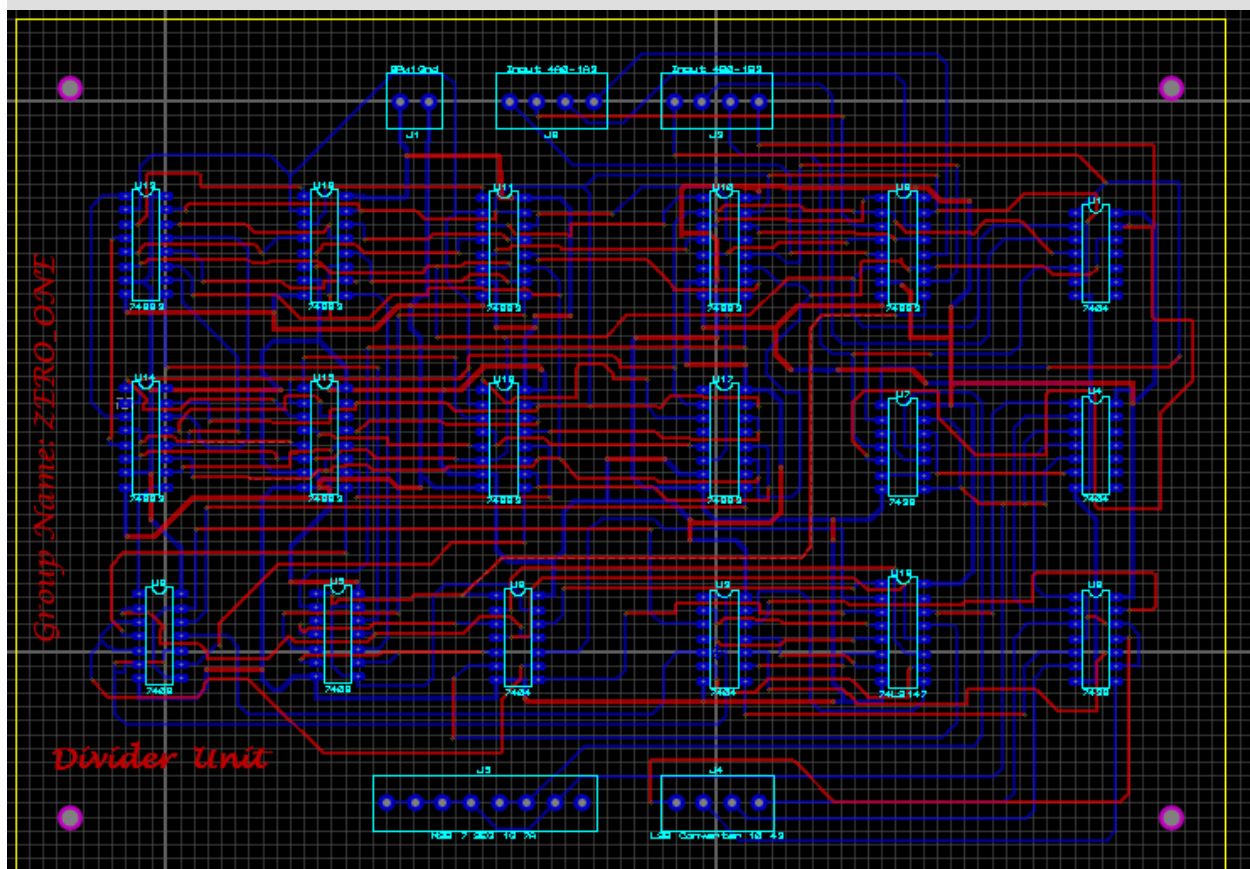
2nd input is subtracted 9 times from 1st input & successive differences. To make the undesired carry outs (if required subtraction is completed before 9th step) forcibly '0' I used AND gates.

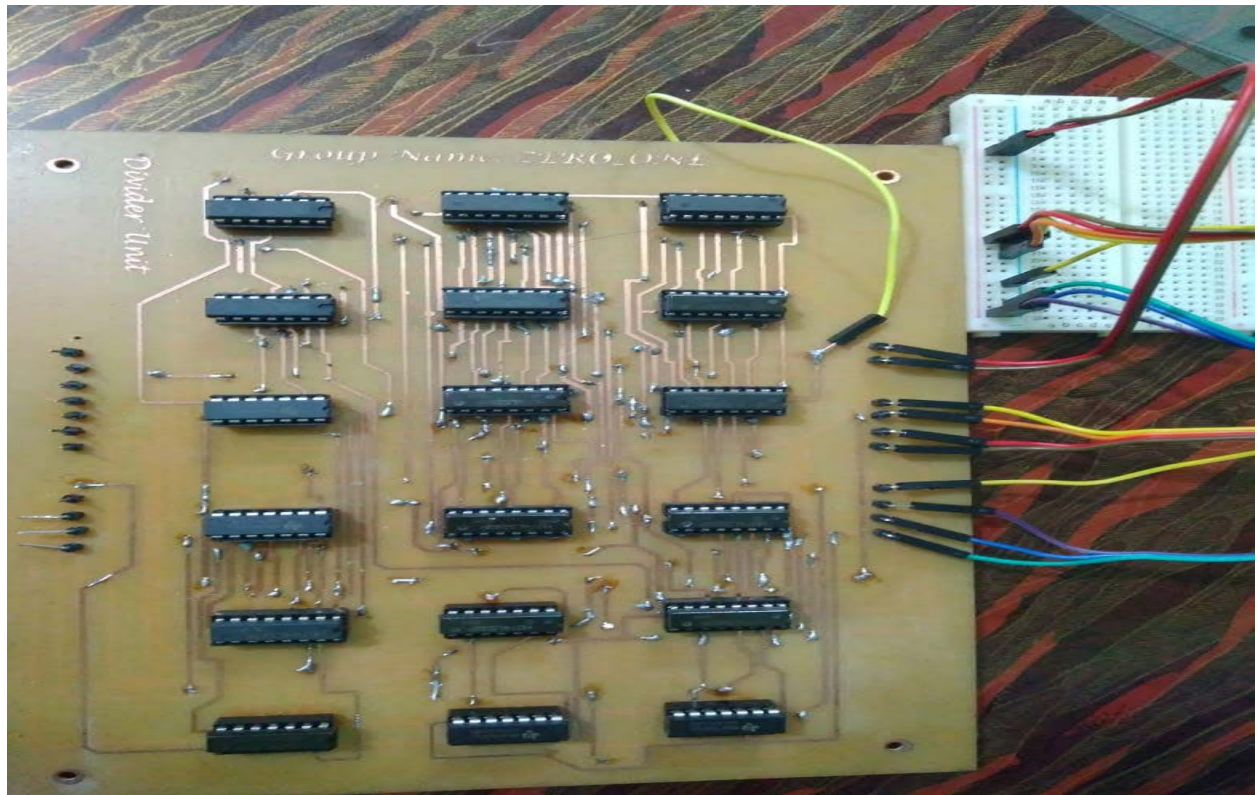
To make required carry outs suitable for using in 10 to 4 line decoder they are inverted using NOT gates.



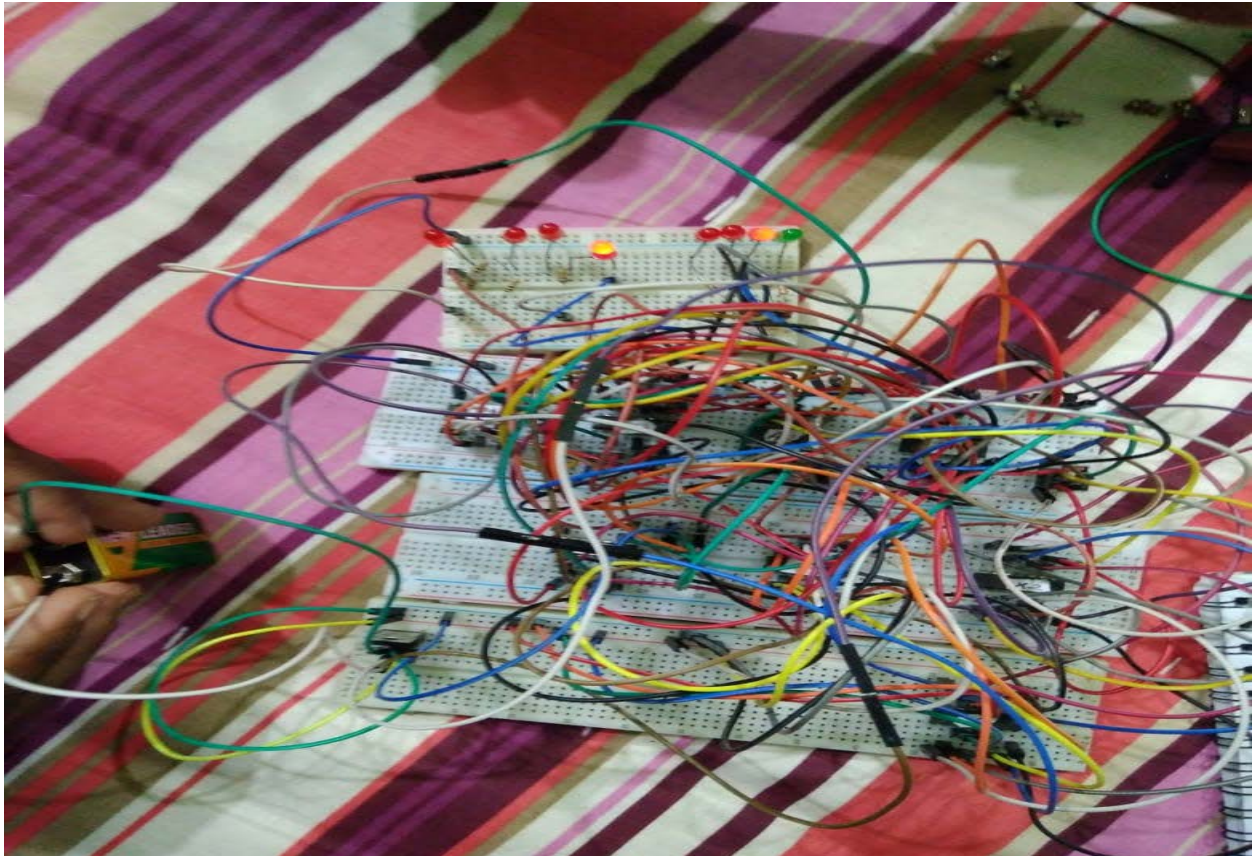
It's designed such that 'E'(Error) will be displayed if any digit is divided by 0
(e.g.: 9/0 in the following picture)







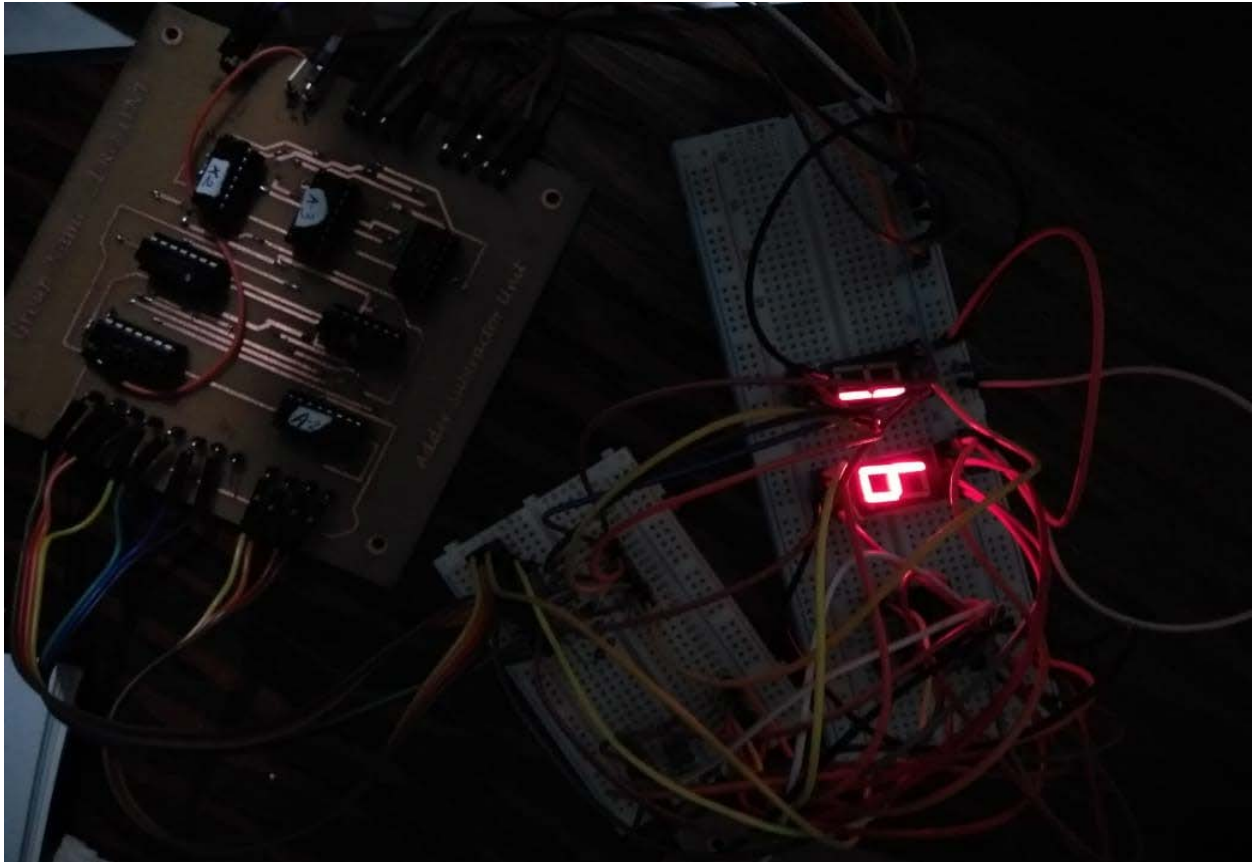
In case of adder-subtractor unit, I first implemented the circuit on breadboard and got the results in the form of binary outputs which are indicated by LEDs. LED on meant 1 and off meant 0.



Display Unit

The display unit consists of 2 common anode 7 segment single digit displays, BCD to 7 seg converts and power supply. When the outputs came to be 0, any desired segment would light up.

The output looked as below:



COSTINGS

The overall costing for buying the different components and accessories for the hardware implementation was BDT 3788 . And details of the costings are given below:

[illegible][illegible]

বিশুদ্ধিমানের রাহমানের রাহিম
ক্যান মেমো

মেসার্স রুহুল এন্টারপ্রাইজ
M/S. RUHUL ENTERPRISE

রেডিও, টিভি, ভিডিও, ভিস, টেপ-রেকর্ডার, আই.পি.এস, ইলেকট্রনিক আই,জি,বি,টি ও
এমপ্লিফায়ারের যন্ত্রাংশসহ সকল প্রকার ইলেকট্রনিক যন্ত্রাংশের পাইকারী ও খুচরা বিক্রয়।
এইচ টি ইলেকট্রিক এন্ড ইলেকট্রনিক্স মার্কেট, চাঁদপুর টাওয়ার, (২য় তলা) ১৩৬/১ নবাবপুর, ঢাকা-১১০০
মোবা : ০১৭২৬-০৪২৮৪৬, ০১৯৭৭-০৬৭১৩১৭, ০১৭৬০-৬৭১৩১৭

নং- 4667 তারিখ- 8/4/18

নাম : *Arif*

ঠিকানা :

নং	মালের বিবরণ	পরিমাণ	দর	টাকা
১	74LS32	6	15	90
২	86	2	15	30
৩	47	2	50	100
৪	08	9	12	108
৫	06	5	12	60
৬	283	20	15	300
৭				
৮				
৯				
১০				
১১				
১২				
১৩				
১৪				
১৫				

কা কথায় :

মোট: 588

বিঃ দ্রঃ- বিক্রিত মাল ফেরত লওয়া হয় না।

ক্রয়তার স্বাক্ষর

বিক্রেতার স্বাক্ষর

আজাদ ইলেকট্রনিকস্
AZAD ELECTRONICES

এখানে সকল প্রকার রেডিও, টিভি, টেপ, ভিসিপি, সিডি, ভিসিডি ও
এমপ্লিফায়ার এর পার্টস পাইকারী ও খুচরা বিক্রয় করা হয়।
আঃ রহিম মুক্তিযোদ্ধা টাওয়ার, দোকান নং-১২/এ দ্বিতীয় তলা, ১৩৮/৩৯ নবাবপুর রোড
ঢাকা-১১০০, মোবাইলঃ ০১৭১১-২২৩৯০৮

নাম : *Arif* নং 903

ঠিকানা : তারিখ 08/04/18

নং	মালের বিবরণ	পরিমাণ	দর	টাকা
১	ATI 5 Fan	1	50	50
২	Switch	16	5	80
৩	104/50v	48	1	48
৪	330R Resistor	20	1	20

বিক্রিত মাল পরিবর্তন ও ফেরৎ লওয়া হয় না।

মোট 198

ক্রয়তার স্বাক্ষর

বিক্রেতার স্বাক্ষর

