# STM32F4 Cheat Sheet

## 1 NVIC

NVIC_*XXX*(*YYY*_IRQ >> 3) = *YYY*_IRQ & 0b111;
NVIC_ISER – Interrupt Set-Enable
NVIC_ICER – Interrupt Clear-Enable
NVIC_ISPR – Interrupt Set-Pending
NVIC_ICPR – Interrupt Clear-Pending
NVIC_IPR(*XXX*_IRQ) – Interrupt Priority
NVIC_IRQ(*XXX*_IRQ) = *handler*;

## 2 EXTI/SYSCFG

1 bit/input line
EXTI_IMR – Interrupt Mask
EXTI_EMR – Event Mask
EXTI_RTSR – Rising Trigger Selection
EXTI_FTSR – Falling Trigger Selection
EXTI_PR – Pending
EXTI{0-4, 9_5, 15_10}_IRQ

SYSCFG_EXTICR1-4 – EXTernal Interrupt Configuration
A(0b0000)-I(0b1000) (4-bit)

## 3 GPIO{A-I}

GPIO*X*_MODER – MODE
2-bit/pin: GPIO_MODER_{ IN, OUT, ALT, ANA }

GPIO*X*_OTYPER – Output TYPE
1-bit/pin: 0 – push-pull, 1 – open-drain

GPIO*X*_PUPDR – Pull-Up/Pull-Down
2-bit/pin: GPIO_PUPDR_{ PU, PD }

GPIO*X*_IDR – Input Data
GPIO*X*_ODR – Output Data
1-bit/pin

GPIO*X*_BSRR – Output Bit Set/Reset
bit 15-0: set, 31-16: reset

GPIO*X*_AFRL – Alternate Function Low (pin 7-0)
GPIO*X*_AFRL – Alternate Function High (pin 15-8)
4-bit/pin

## 4 DAC

DAC_CR – Control
DAC_EN{1-2} – ENable
DAC_SWTRIGR – SoftWare TRIGger
DAC_SWTRIG{1-2}

DAC_DHR12R{1-2} – 12-bit right-aligned holding
DAC_DHR12L{1-2} – 12-bit left-aligned holding

## 5 ADC{1-3}

ADC*X*_SR – Status Register
ADC_EOC – End Of Conversion
ADC*X*_CR1 – Control Register 1
ADC_{12b, 10b, 8b, 6b}
ADC_DISCEN – DISContinuous mode ENable
ADC_SCAN – SCAN mode
ADC_EOCIE – End Of Conversion Interrupt Enable
ADC*X*_CR1 – Control Register 2
ADC_SWSTART – SoftWare START
ADC_EXTEN_{rise, fall, both} – EXTernal Trigger ENable
ADC_EXTSEL_*XXX* – EXTernal event SELect
T1{CC1, CC2, CC3}, T2{CC2, CC3, CC4, TRGO}
T3{CC1, TRGO}, T4CC4, T5{CC1, CC2, CC3}
T8{CC1, TRGO}, EXTI11
ADC_EOCS End Of Conversion Selection
ADC_CONT Continuous conversion
ADC_ADON A.D Converter ON

ADC*X*_SQR1 SeQuence Register 1 (channels 16-13)
bit 23-20 – Length
ADC*X*_SQR2 SeQuence Register 2 (channels 12-7)
ADC*X*_SQR3 SeQuence Register 3 (channels 6-1)
5-bit/input channel
ADC*X*_DR – Data Register

ADC_IRQ – unique interrupt

## 6 TIM{1-14}

TIM*X*_CR1 – Control Register 1
TIM_ARPE – Auto-Relad Preload Enable
TIM_UDIS – Update DISable
TIM_CEN – Counter Enable
TIM*X*_CR2 – Control Register 2
TIM_MMS_*XXX* – Master Mode Selection
RESET, ENABLE, UPDATE, COMPARE_PULSE
COMPARE1, COMPARE2, COMPARE3, COMPARE4
TIM*X*_SMCR – Slame Model Control Register
TIM_ECE – External Clock Enable
TIM_TS_ – Trigger Selection
ITR0, ITR1, ITR2, ITR3,
TI1F_ED, TI1FP1, TI2FP2, ETRF
TIM*X*_SR – Status Register
TIM_CC{1-4}F – Capture/Compare interrupt flag
TIM_UIF – Update Interrupt Flag
TIM*X*_EGR – Event Generation Register
TIM_UG – Update Generation
TIM*X*_CCMR1 – Capture/Compare mode (channel 1, 2)
TIM*X*_CCMR2 – Capture/Compare mode (channel 3, 4)
TIM_CC{*1-4*}S_ – capture/compare selection
OUT, TI1/TI3, TI2/TI4, TRC
*Output*
TIM_OC*Y*M_ – mode
FROZEN, SET, CLR, TOGGLE, PWM1, PWM2
*Input*
TIM*X*_CCER - Capture/Compare Enable Register
CC{*1-4*}NP – Capture/Compare output polarity
CC{*1-4*}P – Capture/Compare output polarity
CC{*1-4*}E – Capture/Compare output enable
TIM*X*_CNT - CouNTer
TIM*X*_PSC - PreSCaler
TIM*X*_ARR - Auto-Reload Register
TIM*X*_CCR*1-4* – Capture/Compare Register

TIM{*2-7, 9-14*}_IRQ
TIM{*1, 8*}_{BRK, UP, TRG_COM, CC}_IRQ