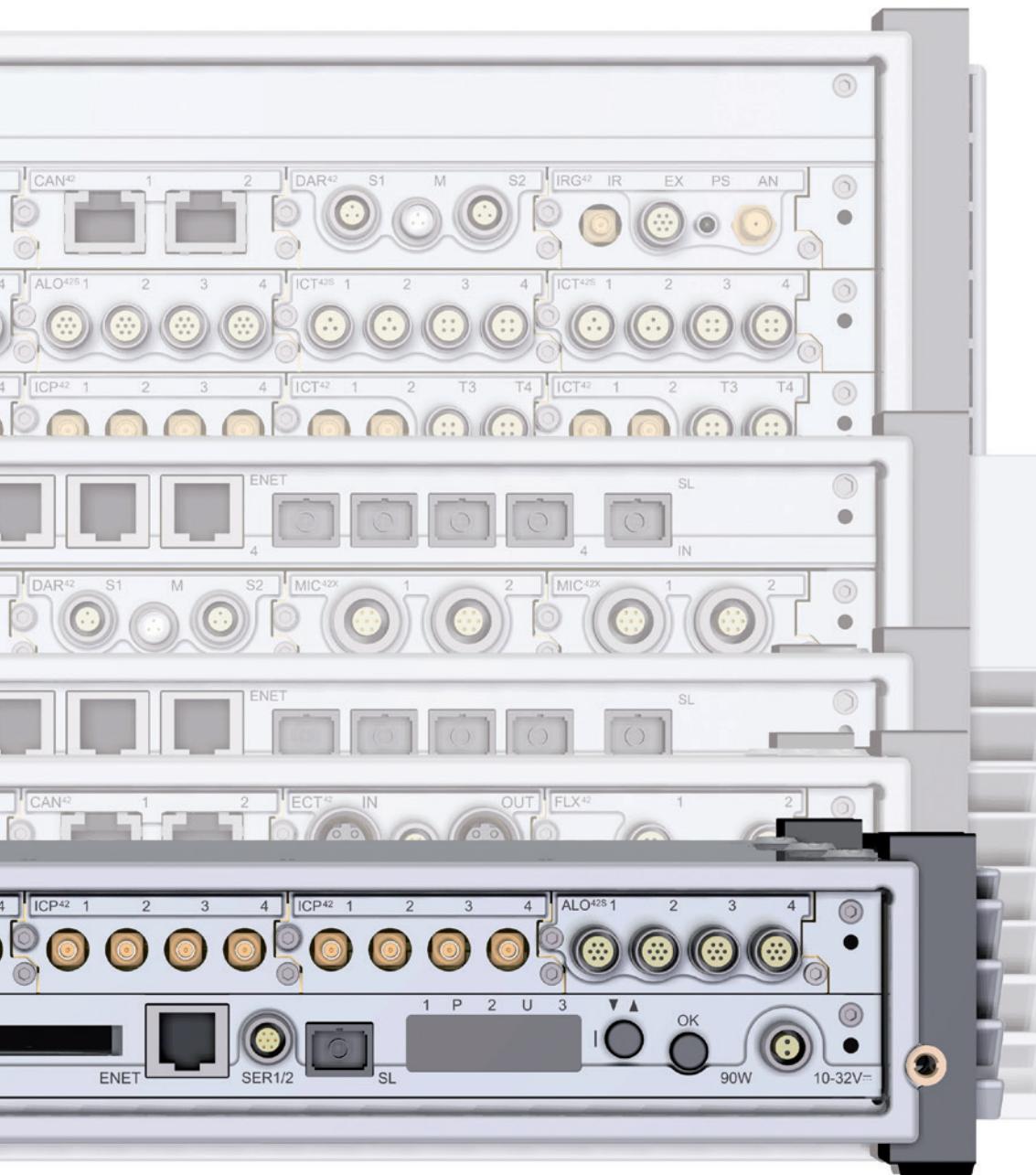


# PAK MKII

## user manual

revision 10.3



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# PAK MKII



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# PAK MKII



# INTRODUCTION

## working through the user manual

The PAK MKII is a highly innovative data acquisition system and therefore undergoes continual development. Before operating the PAK MKII for the first time, please read the instructions carefully as they will aid in the avoidance of problematic situations and will help ensure the validity of measurement data when working with the PAK MKII.

The PAK MKII User Manual revision 10.1 describes only the current hardware components including the 42 Module series, PQ12/20/30 Controllers as well as SC42/SC42S Signal Conditioning Boards. If you are working with an older component from the 41 Module series, PQ11/EP1A/PPC7 Controller or SC41 Signal Conditioning Boards, please refer to the PAK MKII User Manual revision 9.1.

### NAVIGATION

To assist you in reading this manual, please make use of the bookmarks as well as the following hyperlinks:

- The links to relevant sections on all Contents pages
- The links back to the Contents page found in the grey chapter title banner on every page

### CONTACTS

Should you have read this manual thoroughly and are still experiencing difficulties, please contact your local agent. Details of international partners can be found on the back cover.

### NOTE

The external power supply is not part of the PAK MKII system and is thus not discussed in this manual. For further specifications in this regard refer to relevant supplier's details.

# chapter one

## An Introduction to PAK MKII Data Acquisition Hardware

### NOTE:

- Specifications for each Hardware tier is available under GETTING TO KNOW THE PAK MKII

As a comprehensive all-in-one solution PAK MKII implements and integrates all the necessary measurement functions such as signal conditioning, filtering, sampling, data organization, data distribution and data access management into one system.

Essentially a measurement instrument, the PAK MKII is ideally suited to a number of applications which may have some or all of the following requirements:

- Mobile and stationary use
- Slow and high speed data acquisition
- Few and many channels
- Normal or demanding operating environments

The PAK MKII system takes the concept of modularity to an unusually deep level with it being repeated in 5 sub-system levels or tiers, namely SubModules, Modules, VMEbus boards, Mainframes and SyncLink Clusters. These 5 tiers of PAK MKII modularity are collectively known as 5tModularity™.

### VMEBUS BOARDS (t3)

The core of any modular concept should be powerful and versatile but most importantly stable and sustainable. For some 25 years after its launch, VME is still flourishing and is associated with at least 30 other standards. It is predominantly used in aerospace, military, industrial, measurement, control and research applications. It was for this reason that the VMEbus was chosen as the core of the PAK MKII concept.

### MODULES (t2)

Although the VMEbus is flexible, a more compact tier of modularity is required for signal conditioning amplifiers. A Sub-VMEbus concept was therefore devised where 4 signal conditioning Modules fit onto a special VMEbus board which provides the mechanical and electronic infrastructure for these Modules. This board belongs to the Signal Conditioning series. Modules are easily inserted and extracted through the front panel of the SC42 allowing Users the flexibility of self configuring the measurement system for a particular test.

### SUBMODULES (t1)

A SubModule is sometimes required to provide a special interface to an individual sensor. An example of this includes using K-type thermocouples and Pt100 sensors on the same Module to measure temperature. SubModules are thus used to further personalize a Module.

# working through the User Manual

## MAINFRAMES (t4)

Different sized Mainframes optimize the number of channels to be measured whilst at the same time offer freedom to accommodate additional boards at a later stage. In this way the PAK MKII grows according to the User's demands.

## SYNCLINK CLUSTER CONCEPT (t5)

A SyncLink Cluster concept was developed to allow any number of Mainframes to be synchronized together, effectively allowing numerous Mainframes to operate as one virtual Mainframe.

These Clusters are useful as they reduce sensor cable lengths, increase the data rate coming from a test, allow for greater geographical reach and accommodate a limitless channel count. Such a Cluster would normally demand higher data rates for which Gigabit Ethernet is implemented.

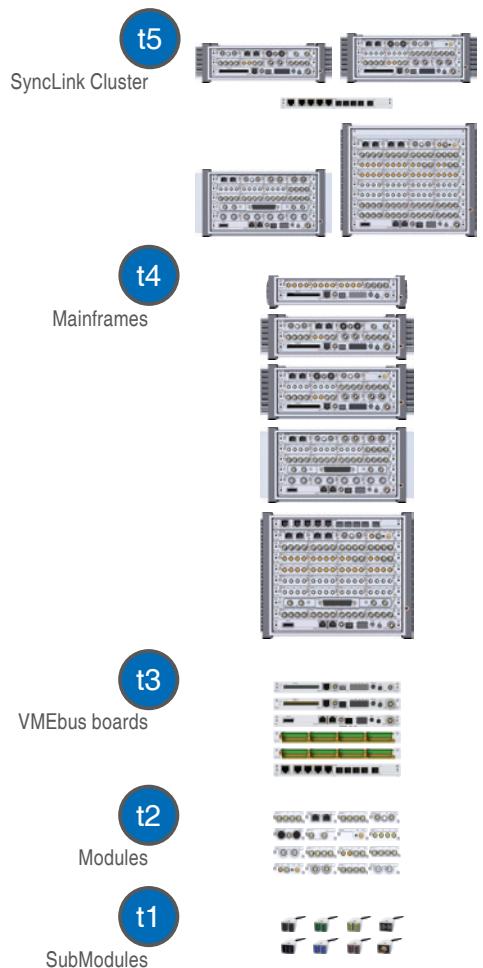
## COMPONENT SERIES – STANDARD, S AND X

A range of speciality series has been designed to complement the standard series.

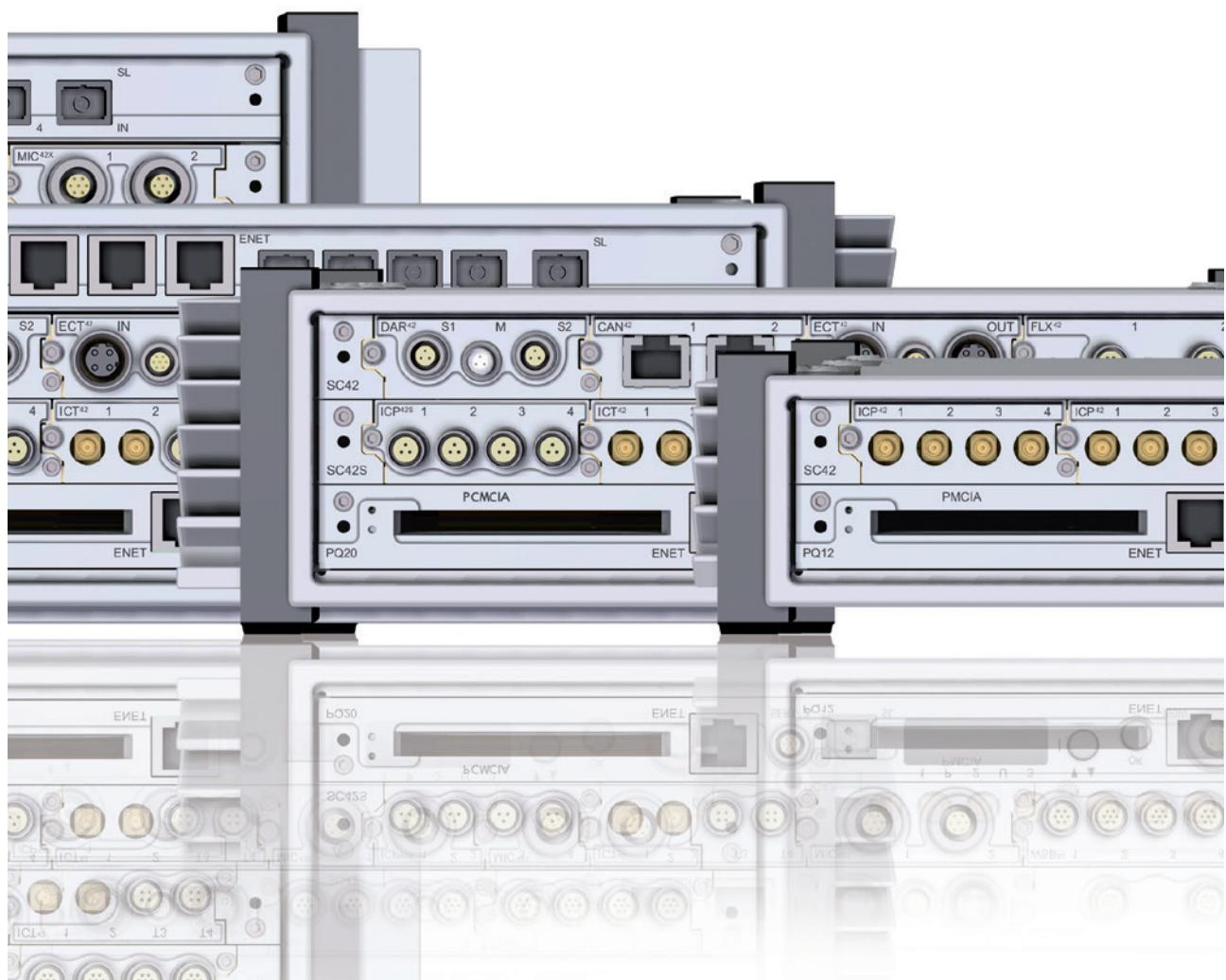
The S series is a range of components with enhanced speed. For Modules this indicates 24 bit, 204.8 kSa/s on the primary input or output channels (e.g. ICP42S or ALO42S). To achieve this enhanced speed on all the Module channels, the S series of Signal Conditioning Boards were developed (e.g. SC42S).

The X series indicates eXtra features that extend the functionality of the standard series, for example the MIC42X includes ICP® mode.

## Understanding the 5 Tiers of Modularity



# PAK MKII



## chapter two

# SETTING UP the PAK MKII

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# chapter two

## General Warnings

### HANDLING:

Even though PAK MKII has been designed to withstand rough handling within reason, it is still a highly sensitive and complex electronic instrument and must be handled with care.

### DAMAGE:

Do not use a damaged PAK MKII, power supply, cable or any other PAK MKII component. Return to the supplier for repairs.

### REPAIR:

Do not attempt to repair any damaged PAK MKII, power supply, cable or any other PAK MKII component. Return to the supplier for repairs.

### FLAMMABLE ENVIRONMENTS:

The PAK MKII may not be operated or stored in flammable environments (fumes, gasses, liquids, etc.).

### HARSH ENVIRONMENTS:

The PAK MKII may not be operated in excessively harsh environments (corrosive, hot, radio active, oily, etc.).

### WET ENVIRONMENTS:

The PAK MKII is not waterproof and may not be operated in excessively moist environments.

### DISPOSAL:

Return to the supplier for safe disposal. The battery pack can explode if disposed of incorrectly.

# setting up the PAK MKII

## ESD AND OTHER PRECAUTIONS

All VMEbus boards and Modules are highly sensitive to electrostatic discharge (ESD) and may be damaged by such a discharge. Damage may occur over several events and could result in measurement inaccuracy.

To avoid damage to the PAK MKII, antistatic precautions must be followed especially when swapping VMEbus boards or Modules. Antistatic precautions are advisable especially when connecting sensors to Modules.

## ESD and Other Precautions

### STANDARD PRECAUTIONS INCLUDE:

1. Discharge any excess static your body may contain by touching the exposed metal of the Mainframe's Chassis Ground Socket.
2. When swapping VMEbus boards or Modules, work on an Earthed Antistatic Mat while wearing an earthed Antistatic Wrist Strap.
3. VMEbus boards and Modules must be handled by their front panels or aluminum covers.
4. Place VMEbus boards and Modules in antistatic bags immediately after removal from PAK MKII.
5. Store and transport VMEbus boards and Modules in padded antistatic packaging.
6. Never stack VMEbus boards or Modules on top of each other.
7. Do not mark the front panels using any pen or writing tool which cannot easily be removed as additional charges will be incurred should the VMEbus board or Module be returned for repair.
8. When connecting signals to Modules, beware of electrostatic charge that might have built up on the signal cables or sensors.

# chapter two

## Grounding

Each Module's power and Analog Ground is isolated from the rest of the PAK MKII. A resistor allows the Module Analog Ground to float away from Chassis Ground.

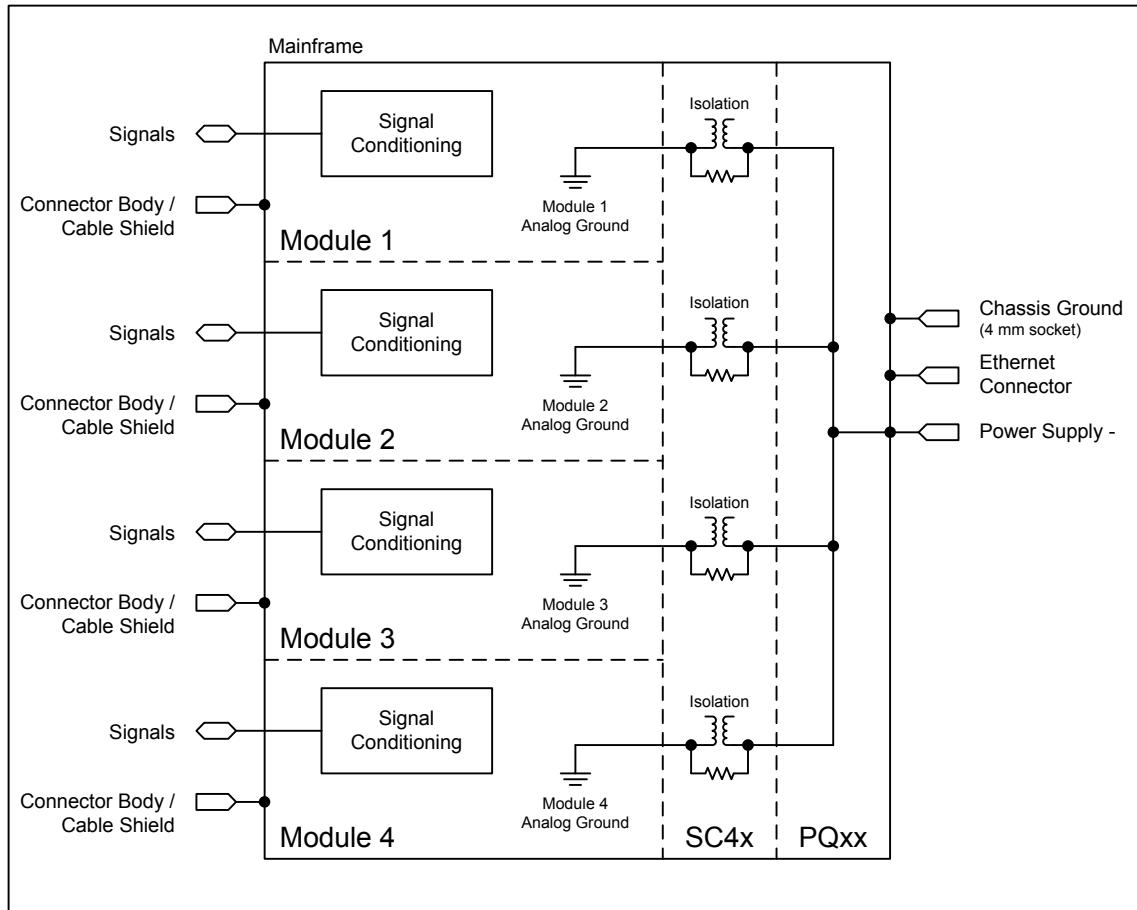
Selected Modules are fitted with a software controlled Chassis Ground switch/relay which allows the Module Analog Ground and the Chassis Ground to be connected to each other.

Chassis Ground is directly connected to the power supply negative and the Ethernet cable shield. Depending on the specific power supply used, the power supply may or may not be connected to earth.

Grounding setups must be evaluated on a case by case basis. It is often best to experiment with different grounding setups to determine the best combination within the specific environment and constraints.

The Ethernet connector body is connected to the PAK MKII chassis ground, and it is therefore recommended to use UTP network cable to avoid ground loops. Do not use the Ethernet connector as the primary earth connection on the PAK MKII.

### PAK MKII Grounding



# setting up the PAK MKII

The PAK MKII complies with the EMC directives as described in the “CE Compliance” section.

Please note however that when connecting cables, sensors or third party devices to the PAK MKII, electromagnetic noise could be introduced into the measurements.

Obey good measurement practices:

1. Remove or isolate electromagnetic noise sources.
2. Use shielded cables, with the shield and signal voltage difference minimized.
3. Use twisted pair cables with differential measurements.
4. Avoid ground loops by isolating sensors and/or cable shields.
5. Use low impedance signal sources where possible.

## Electromagnetic Immunity

### NOTE:

A revised blue CAN cable with better EMI is available for the CAN Module.

## GUIDELINES TO SUPPORT COOLING

Over-temperature protection has been included in the PAK MKII firmware. Guidelines for optimal cooling are:

1. Place the PAK MKII where there is a free flow of cool air.
2. Place the PAK MKII horizontally to allow optimal airflow through the fins located on the left and right sides.
3. Do not cover the PAK MKII fins or cooling fans.
4. Elevate off carpet or other thermal insulating material.
5. Avoid direct sunlight.
6. Charging of the PAK MKII battery does introduce additional heat.

## ENSURING EFFICIENT TRANSFER OF HEAT

In ensuring the efficient transfer of heat from each Module/VMEbus board into the Mainframe, Users must check that:

1. VMEbus boards' expanders are fastened.
2. Both screws of Modules are fastened.

## Positioning the PAK MKII for Effective Cooling

### PLEASE REFER:

1. Chapter three:  
Using the PAK MKII  
Temperature Protection and Cooling

# chapter two

## Connecting Power

### WARNING:

Never switch off or reset the PAK MKII while it is busy booting or while a firmware upgrade is in progress. This could permanently damage the system. Only when the PAK MKII display indicates IDLE or FAIL is further User interaction required.

### PLEASE REFER:

1. Chapter four:  
Power Cable Specifications
2. Chapter four:  
Further System Specifications

## Connecting Ethernet

### HINT:

When using Ethernet on the PAK MKII use only a UTP cable. This will ensure the correct screening of signals throughout the length of the cable.

### GUIDELINES TO CONNECTING POWER

The PAK MKII requires a special power cable. Do not attempt to use third party cables as this may damage your system.

When running the PAK MKII from low voltages, the increased current could cause power cables and connectors to heat up. When the supply voltage is lowered, there is a quadratic increase in heat caused by more current flowing through the resistance of the cable and connector. When powering larger PAK MKII systems, it is therefore recommended to:

1. Use short cables
2. Use higher voltages, e.g. 24 V instead of 12 V
3. Avoid any intermediate connectors or joints in the power cable.

The PAK MKII should always be switched off in a safe manner using the Web Interface or User Interface buttons on the PQ Controller. Never switch off by disconnecting the power supply if a battery is not present. Permanent hardware damage could result.

A Fast Ethernet connection (10/100 BASE-T) is available on any PAK MKII with a PQ12/PQ20/PQ30 Controller card. An RJ45 connector is available at the controller board's front panel and can accept compatible Ethernet cables. A Gigabit Ethernet connection (1000 BASE-T) is available on any PAK MKII with a PQ30 Controller card. The Ethernet interface cannot be used in combination with the Wireless LAN interface since only one of the two interfaces on the controller board can be active at a time.

### USING ETHERNET

To use the Ethernet interface, Users need simply plug in an Ethernet cable. The PAK MKII will automatically detect the Ethernet cable and initialize it as the primary network interface. The PQ30 has two RJ45 connectors available. The one closest to the text 'ENET' should be used to connect the PAK MKII. The one furthest from the text 'ENET' is reserved for future applications. Once booted, the User interface can be used to acquire the controller's IP address. Thereafter the Web Server can be used (with the IP address as hyperlink) to make modifications to the network setup.

### CONNECTION RANGE

Both Gigabit and Fast Ethernet connections have a range of 100 m. If a longer distance is required then a repeater station will be needed at intervals of every 100 m.

# setting up the PAK MKII

An IEEE 802.11 b Wireless LAN network connection is available on any PAK MKII with a PQ12/PQ20 Controller card. A PCMCIA slot is available at the Controller board's front panel and can accept compatible 802.11 b Wireless LAN PCMCIA cards. The Wireless LAN network interface can be used as an alternative to the Ethernet interface where truly mobile operation of the PAK MKII is required. The Wireless LAN interface cannot be used in combination with the Ethernet interface since only 1 of the 2 interfaces on the Controller board can be active at a time.

## USING WIRELESS LAN

To use the Wireless LAN network interface, Users must simply make sure that a supported Wireless LAN board is inserted into the PCMCIA slot before power-up. The PAK MKII will automatically detect the Wireless LAN card and attempt to initialize it as the default network interface.

## SUPPORTED 802.11 B WIRELESS LAN CARDS

IEEE 802.11 b Wireless LAN boards with the Intersil Prism chipset are supported. Both 3.3 V and 5 V cards are supported. The Wireless LAN interface has been thoroughly tested with the Lucent OriNOCO/WaveLAN Gold card (now Agere OriNOCO) which supports 104/128 bit encryption.

## CONNECTION RANGE AND THROUGHPUT

The connection range and throughput are a function of the specific Wireless LAN board in use. A throughput of between 1 Mbit/s and 11 Mbit/s is supported.

## Connecting Wireless LAN

### NOTE:

An IEEE 802.11 b Wireless LAN is not available on the PQ30.

### WARNING:

The PAK MKII Wireless LAN interface is NOT hot-swappable. Before inserting or removing a Wireless LAN PCMCIA card, ensure that the PAK MKII system is powered-down. Failure to do may damage the Wireless LAN PCMCIA card and/or interface.

### PLEASE REFER:

1. Chapter three:  
Using the PAK MKII  
User Interface for the PQ12, PQ20  
and PQ30

# chapter two

## Interchangeability of Modules

### WARNING:

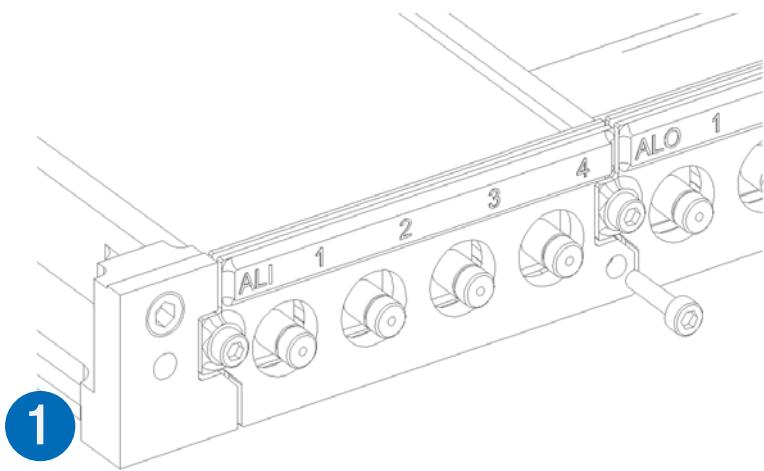
When removing Modules it is essential that proper safety precautions be followed to avoid electrostatic discharge. Do not press down on Module connectors. PLEASE FOLLOW THE ADJACENT STEPS.

1. **ONLY personnel suitably trained in the PAK MKII should be permitted to remove/insert Modules.** Please contact your local distributor or support for further details on training.
2. **Avoid electrostatic discharge:** Put on an Antistatic Wrist Strap, which is connected to an Earthed Antistatic Mat.
3. **Only handle Modules by their front panels or board edges and store them immediately following removal in their anti-static bags.** All Modules are highly sensitive to electrostatic discharge and may be rendered inoperative by such a discharge. Damage may occur over time and could result in measurement inaccuracy.
4. **Ensure that the PAK MKII is switched off** (display must be dark) before an Module may be removed. As the PAK MKII contains an internal battery pack merely disconnecting the external power supply is not sufficient. Removing a Module while the PAK MKII is running will cause damage to the Module and the SC4x VMEbus board.
5. **Not only must the PAK MKII be switched off before the Module can be removed but the Module must have cooled down to approximately 40 °C.** This is important as the permanent screw retainer used between the jacking screw and its nut (see following diagrams) could fail at high temperatures.
6. **All empty Module slots of the PAK MKII must be covered using blank Module panels (MBL).** Failure to do so may allow dust or other objects to damage the PAK MKII.

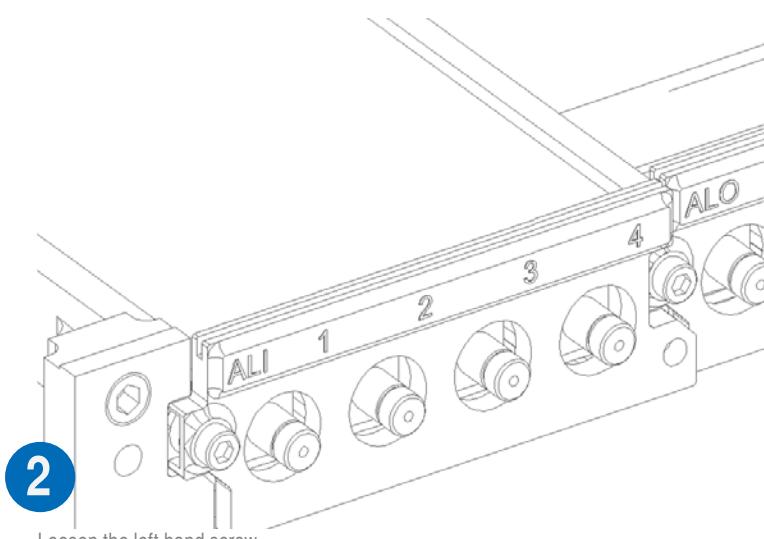
### PLEASE REFER:

1. Setting up the PAK MKII:  
ESD and Other Precautions
2. Chapter three:  
Using the PAK MKII:  
Automatic Upgrades

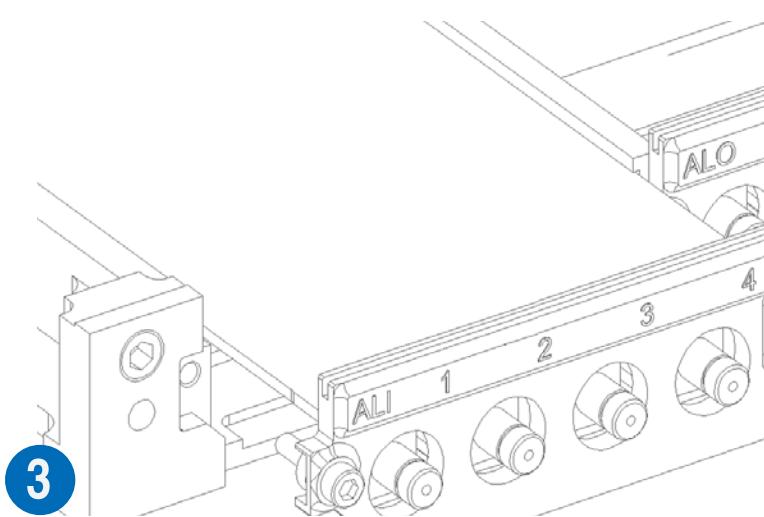
# setting up the PAK MKII



Loosen and remove the right hand screw



Loosen the left hand screw



Hold the front panel and pull the Module out

Each Module is fastened to the SC4x chassis with 2 M2.5 socket head cap screws. They can be loosened with a 2.0 mm Allen key. The order in which these screws are loosened is important as one screw is used as a jacking screw.

## REMOVING A MODULE

1. Obtain an anti-static bag into which the Module can be placed.
2. Put on an Antistatic Wrist Strap, which is connected to an Earthed Antistatic Mat.
3. Disconnect all sensors and cables connected to Module.
4. Loosen and remove the right hand screw (M2.5 x 6 socket head cap screw) with a 2.0 mm Allen key.
5. Loosen the left hand screw. Whilst turning out (loosening) this screw, the Module will be pulled out of its slot automatically since it has a jacking nut immediately behind its front panel.
6. When the left hand screw has been completely loosened, whilst holding the front panel, pull the Module out of its slot and place it in an anti-static bag immediately.
7. All empty Module slots of the PAK MKII must be covered either with another Module or by using a blank Module panel (MBL). Failure to do so may allow dust or other objects to damage the PAK MKII.

# chapter two

## Interchangeability of Modules

continued

### INSERTING A MODULE

1. Put on an Antistatic Wrist Strap, which is connected to an Earthed Antistatic Mat.
2. Do not press down on Module connectors.
3. Take the Module out of its anti-static bag and push it into the empty SC4x Module slot until the left hand screw engages its thread.
4. Fasten the left hand screw with a 2.0 mm Allen key. The Module is pulled in whilst fastening the screw.
5. Fasten the right hand screw (M2.5 x 6 socket head cap screw) with a 2.0 mm Allen key. On the next power-up, the PAK MKII will automatically detect the newly installed Module.

### PLEASE REFER:

1. Chapter three:  
Using the PAK MKII:  
Automatic Upgrades

# setting up the PAK MKII

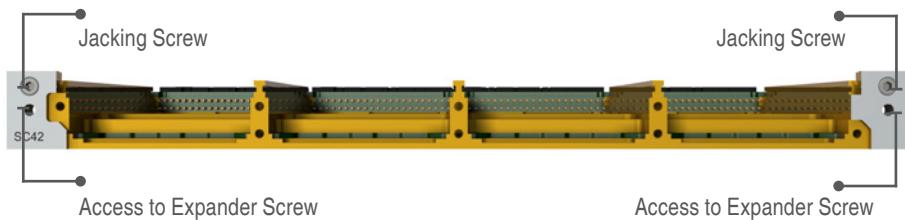
VMEbus boards should not be swapped by someone who does not have sufficient knowledge of the system as components are easily damaged. Damaged components may not cause complete system failure but may affect measurement accuracy or product reliability.

If it is necessary to swap VMEbus boards between systems it should only be performed by suitably trained employees under the correct conditions according to certain precautions.

## Interchangeability of VMEbus Boards

### CHANGING VMEBUS BOARDS

ONLY technical personnel, who have been trained to perform this task, should be allowed to remove VMEbus boards. When untrained personnel remove VMEbus boards all guarantees and warranties will be void.



#### Example of a VMEbus board with Jacking Screws and holes to access Expander Screws

Each VMEbus board is fastened into the PAK MKII Mainframe by two expanders, which are located behind the two holes indicated in the figure. After loosening the Expander Screws, the VMEbus board can be removed by alternatively turning in (clockwise) the two Jacking Screws.

### SCREW SIZES

Use a 2.5 mm Allen key for all VMEbus boards.

### WARNING:

When removing VMEbus boards proper safety precautions must be followed to avoid electrostatic discharge.

### WARNING:

Only remove a VMEbus board when the PAK MKII is switched off. Remember that the PAK MKII contains a battery pack internal to the PAK MKII, so merely disconnecting the external power supply is not sufficient.

### WARNING:

All empty slots of the PAK MKII must be covered using blank VMEbus boards (VB10).

### WARNING:

Avoid placing VMEbus boards on top of each other outside of the Mainframe.

# chapter two

## NOTE:

No force is required to remove the VMEbus board. If the VMEbus board difficult to remove, loosen the Expander Screws more and turn the Jacking Screws in deeper.

## WARNING:

When removing a VMEbus board, EMC Strips could cause damage to the bottom of the VMEbus board being removed if downward force is applied.

### TO REMOVE A VMEBUS BOARD

1. Obtain an antistatic bag and padded packaging into which the VMEbus board can be placed.
2. Put on an Antistatic Wrist Strap, which is connected to an Earthed Antistatic Mat.
3. Place the PAK MKII on the Earthed Antistatic Mat with slot 1 on the bottom.
4. Connect the PAK MKII Mainframe to earth using the Chassis Ground Socket.
5. Disconnect the power and ensure the system is switched off.
6. Disconnect any cables that are connected to the VMEbus board being removed.
7. If the system is hot, wait until it is cool to the touch. This will avoid burns and allow the thermal expansion to subside making VMEbus boards easier to remove.
8. In the case of a SC4x, remove all Modules from the SC4x that is being removed.
9. Loosen the two expanders belonging to the VMEbus board which must be removed, by inserting an Allen key through the expander holes, and turning the Allen key anticlockwise by about 4 turns.
10. Using the Allen key, alternatively turn one screw half a turn clockwise, then turn the other screw half a turn clockwise, and so on, until the VMEbus board is freed from its backplane connector (jacking).
11. Pull out the VMEbus board from its slot, holding it by its front panel or Board edges, and place it into an antistatic bag.
12. Store or transport the VMEbus board in padded antistatic packing.

### TO INSERT A VMEBUS BOARD

1. Put on an Antistatic Wrist Strap, which is connected to an Earthed Antistatic Mat.
2. Place the PAK MKII on the Earthed Antistatic Mat with slot 1 on the bottom.
3. Connect the PAK MKII Mainframe to earth using the Chassis Ground Socket.
4. Disconnect the power and ensure the system is switched off.
5. Take the VMEbus board out of its antistatic bag and place it on the Earthed Antistatic Mat.
6. In the case of a SC4x, remove all Modules from the SC4x being inserted.
7. Loosen the two Expander Screws by inserting an Allen key through the expander holes, and turning the Allen key anticlockwise.
8. Screw the two Jacking Screws out (anticlockwise) until they extend 2 mm out of the front of the VMEbus board.
9. Push the VMEbus board into the empty slot, ensuring that the backplane connectors are properly mated. If necessary, place the PAK MKII on its Rear Cover Plate to apply more force. Take care not to apply force to any connector, switch or display.
10. Fasten the Expander Screws using an Allen key. Turn it clockwise until the expanders are tightly locked. The locking torque is 0.70 Nm.
11. Screw the two Jacking Screws in (clockwise) securely using only a thumb and forefinger. The Jacking Screws should be tight enough as to not vibrate loose.

## WARNING:

NEVER apply force to any connector, switch or display.

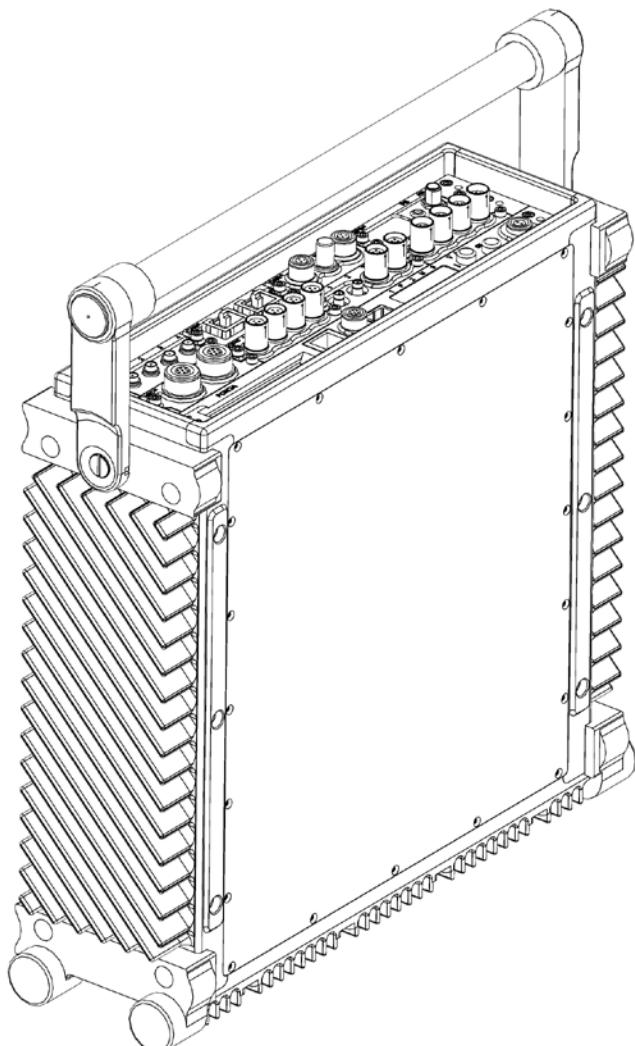
# setting up the PAK MKII

A convenient carrying handle is provided on MF02, MF03, MF04 and MF06. The PAK MKII's handle can be locked into five different positions namely -90°, -60°, 0°, +60° and +90° (where positive is the upward direction).

When carrying the PAK MKII by its handle, it is suggested that the handle first be moved to the 0° position - i.e. the handle must be pointing in a direction parallel to the length of the Mainframe.

## TO CHANGE THE POSITION OF THE HANDLE

1. Push in both the push buttons on either side of the handle (where it meets the Mainframe).
2. While holding both these buttons in, adjust the handle as required and release both depressed buttons.



Mainframe handle in the 0° carrying position

## Using the Handle



### NOTE:

When carrying the PAK MKII by its handle ensure that the handle is in the 0° position.

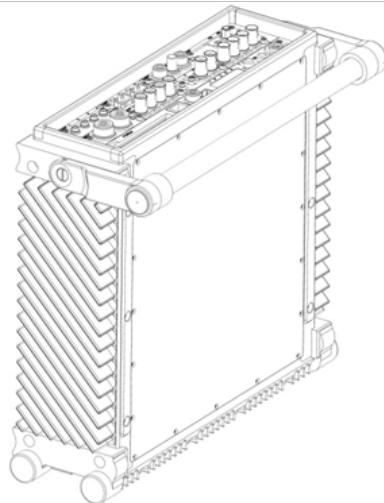
# chapter two

## Removing the Handle

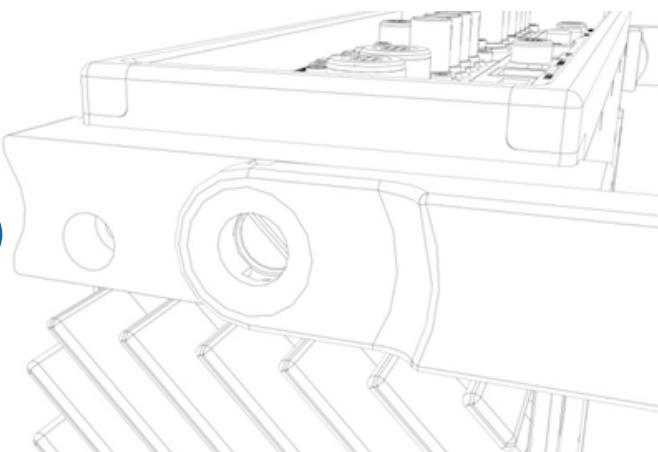
### REMOVING THE HANDLE

1. Place PAK MKII Mainframe on feet.
2. Make sure the handle is set at -90° as shown in adjacent figure.
3. With a slotted or flat screwdriver (6 mm x 1.25 mm), push the push button in all the way, rotate 45° clockwise and release.
4. While holding the handle assembly in place, repeat step 3 on the other side.
5. Gently pull the handle assembly upwards and away from the Mainframe; making sure it is horizontal at all times.

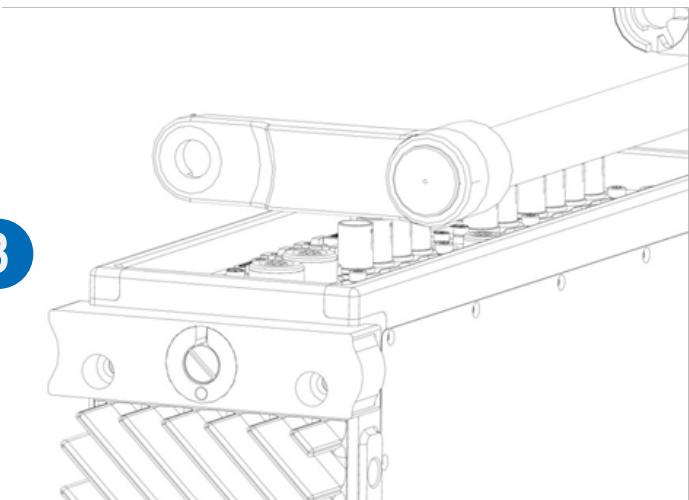
1



2

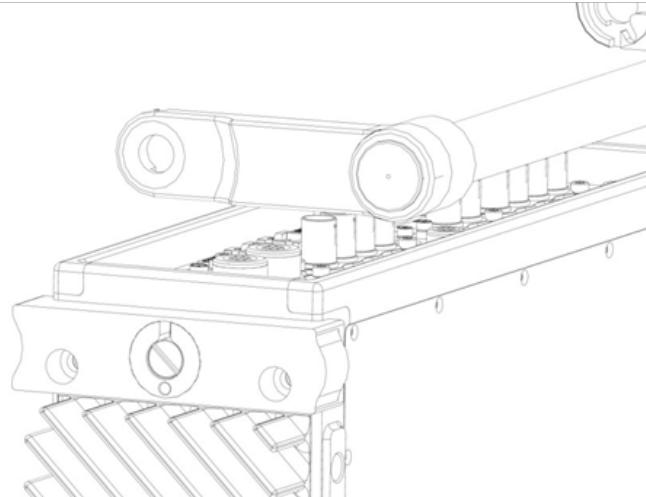


3

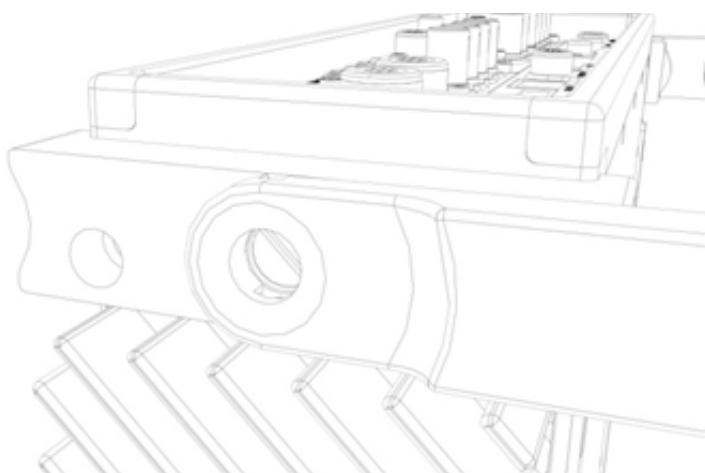


# getting to know the PAK MKII

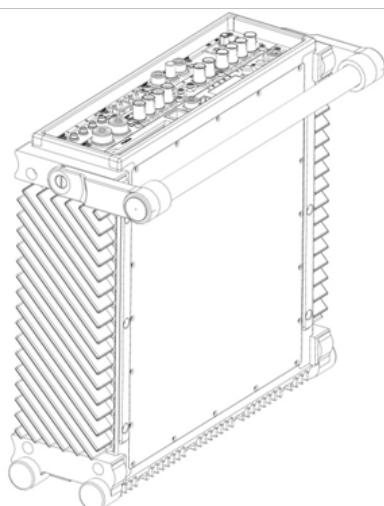
1



2



3

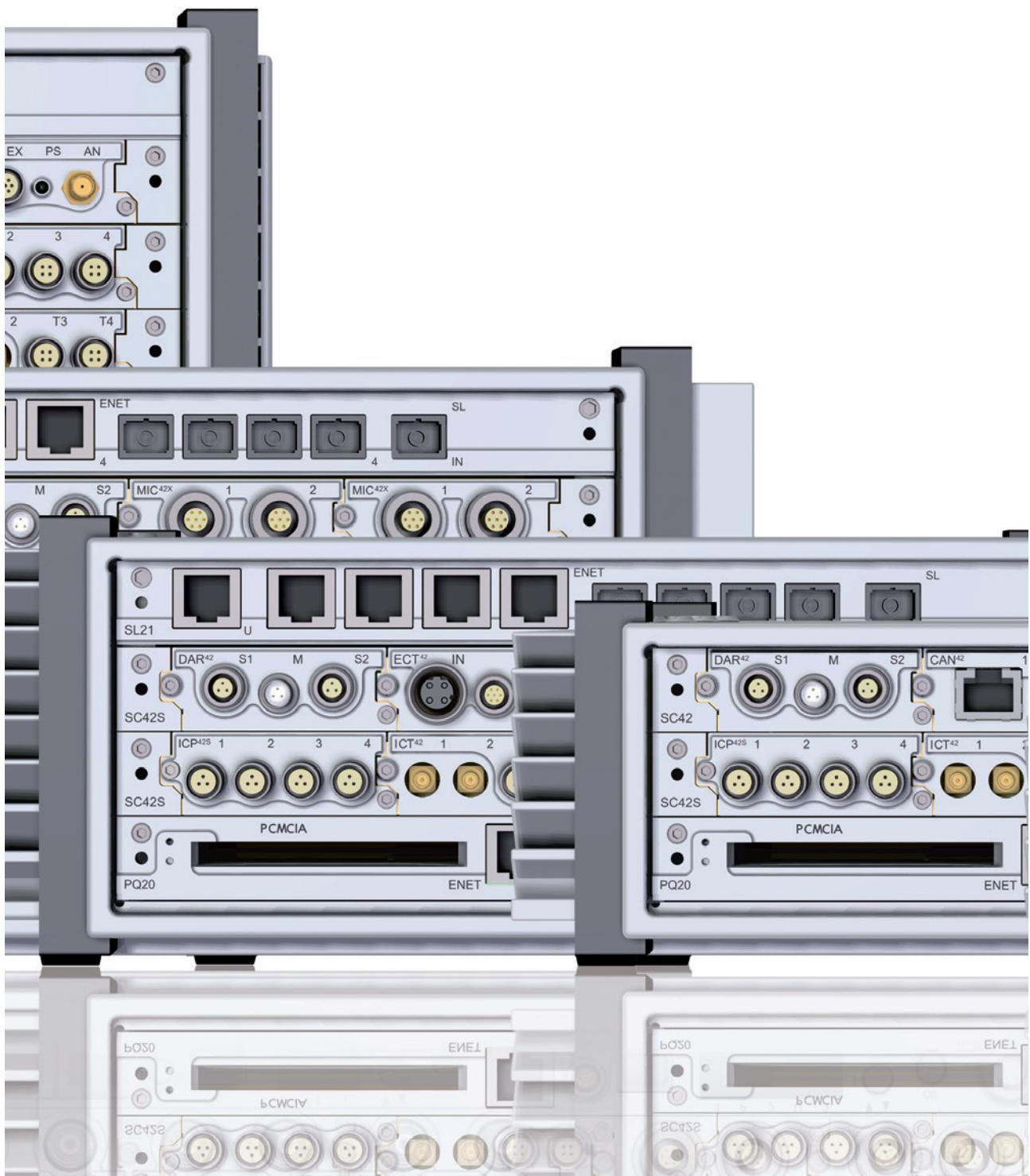


## Replacing the Handle

### REPLACING THE HANDLE

1. With the Mainframe on its feet, hold the handle assembly in the -90° position above the Mainframe.
2. Hold the handle above the Mainframe so that the position of the protruding pins of the push button fit into the slots on the handle assembly.
3. With the handle assembly in the approximate position, push down and turn the push button anti-clockwise with slotted or flat screwdriver (6 mm x 1.25 mm).
4. The push button will spring back into position if the handle is perfectly aligned.
5. Repeat on other side.

# PAK MKII



## chapter three

# USING the PAK MKII

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# chapter three

## User Interface for the PQ12, PQ20 and PQ30

### WARNING:

In order for the PAK MKII system to start up correctly power must be connected to the PAK MKII power connector and an Ethernet cable to the Ethernet port. When doing so Users must ensure that the correct voltage and polarity are adhered to.

The User Interface allows the User to perform a series of control commands as well as to obtain specified system information. The User Interface of the PQ12 and PQ20 consists of an eight character display, 5 LEDs and 2 buttons for scroll and select functions. The User Interface of the PQ30 consists of a four character display, 5 LEDs and 2 buttons for scroll and select functions.

### HOW TO OPERATE THE PQ12, PQ20 AND PQ30 USER INTERFACE

2 buttons are present on the User Interface of the PQ12, PQ20 and PQ30. The 1st button of the User Interface is used to scroll through the different menu items. The 2nd button is for making a selection on the User Interface and will execute the menu item command currently displayed. At times some commands need to be acknowledged as a safety feature.

SCROLL	Button 1
SELECT	Button 2
POWER-UP	Button 1

### SWITCHING ON THE PAK MKII

1. Power-up by pressing button 1.
2. LEDs will flash briefly to indicate their proper operation.
3. When START? or ON? appears on the display press button 2 to select. SURE? or SURE is then displayed. Press button 2 again to select.
4. When PAK MKII or MKII appears on the display the system has started to boot.
5. If running off the battery pack the display shows BACKUP or BKP.
6. When Wait... or Wait appears on the display (typically after 15 s), the PAK MKII has started to initialize its SC4x boards and Modules. The initialization will typically take 10 s unless the PAK MKII needs to internally upgrade the SC4x and Module firmware. In this case the initialization can take up to more than 1 min, depending on the number of SC4x boards and Modules to be upgraded. DO NOT TRY TO SWITCH OFF OR REBOOT THE PAK MKII AT THIS STAGE.
7. When Idle... or Idle appears on the display, the PAK MKII has powered up and booted successfully.

# using the PAK MKII

## SWITCHING OFF THE PAK MKII

1. Scroll using button 1 until OFF? is displayed.
2. Select using button 2. SURE? or SURE is then displayed.
3. Select using button 2 again.
4. PAK MKII switches off. With the above-mentioned procedure the User consciously follows a sequence to switch off the PAK MKII. By following such a procedure the PAK MKII will be switched off irrespective of whether a test is running or not. Valuable data may be lost.

## RESETTING THE PAK MKII

1. Press SCROLL (button 1) until SYSRST? or RST is displayed.
2. Select using button 2. SURE? or SURE is then displayed.
3. Select using button 2 again.
4. A system reset will be performed causing the PAK MKII to reboot. With the above-mentioned procedure the User consciously follows a sequence to switch off the PAK MKII. By following such a procedure the PAK MKII will be switched off irrespective of whether a test is running or not. Valuable data may be lost.

## INCREASING AND DECREASING DISPLAY BRIGHTNESS

The brightness of the PAK MKII display is managed via the User Interface. Holding in the OK button will cycle through the brightness of the display. Hold in the OK button and the brightness will slowly change. At the desired brightness release the button.

## IP ADDRESS OF PAK MKII

To display the PAK MKII IP address:

1. Scroll until IP? is displayed.
2. Select using button 2. Display shows SURE? or SURE
3. Press button 2 to select again. For a PQ12 and PQ20 the display shows 2 x 2 IP address groups 192.168 and 1.231 to give the complete IP address 192.168.1.231. For a PQ30 the display shows 4 x 1 IP address groups namely 192., 168., 1. and 231. to give the complete IP address 192.168.1.231.
4. After displaying the IP address, the PAK MKII displays other information on the Controller and SC4x firmware versions which are currently executing on the PAK MKII.
  - The Controller firmware release number is displayed (e.g. 1-4-a).
  - The Controller firmware release information is displayed (e.g. 13582605).
  - The SC4x firmware release number is displayed (e.g. 1-4-a).
  - The SC4x firmware release information is displayed (e.g. 16230809).
5. The system will then return to its normal display.

## User Interface for the PQ12, PQ20 and PQ30

continued

## WARNING:

Never switch off or reset the PAK MKII while it is busy booting or while a firmware upgrade is in progress. This could permanently damage the system. Only when the PAK MKII display indicates IDLE or FAIL is further user interaction required.

# chapter three

## User Interface for the PQ12, PQ20 and PQ30

continued

### WARNING:

Fast-charging uses approximately an additional 24 W of electrical input power. If the input power supply cannot provide the additional power, the system might reset. Fast-charging can only be performed before the system boots. Furthermore it is recommended that fast-charging is performed in an area with a free flow of cool air as fast-charging introduces additional heat into the system.

### NOTE:

- If the external power is removed while charging is in progress, the PAK MKII will switch off.
- As NiCd batteries have a memory effect, it is advisable to allow the battery pack to charge to its full capacity before ending the charging process early or removing power.
- Due to the properties of NiCd rechargeable batteries, recharging can only be performed when the battery pack is in the temperature range of 10 °C to 45 °C.

### CHARGING THE BATTERY PACK (FSTCHRG? OR FCH? / SLOCHRG? OR SCH?)

In order for the PQ12, PQ20 and PQ30 UPS to perform its function of supplying the PAK MKII with backup power, the battery pack must be charged.

During normal operation, the PAK MKII trickle-charges the battery pack (without any User intervention) to ensure maximum capacity at all times. Note that trickle-charging is intended to only maintain the current battery charge.

To recharge a discharged battery pack the fast-charge or slow-charge method must be used. The User can request the PQ12 / PQ20 / PQ30 to fast or slow-charge a battery pack via the board's User Interface. It takes typically 2 to 3 h to recharge a completely discharged battery pack using fast-charge and 16 h when using slow-charge.

While the battery pack is being charged using fast-charge, the rest of the PAK MKII system will remain off and will thus not be able to operate as normal. This protects the PAK MKII from overheating.

To charge the battery pack while the PAK MKII system is operational, slow-charge must be selected. This method allows the User to continue working without overheating the PAK MKII system since the slow-charge method only places a small additional load on the PSU. The drawback is that it can take up to 16 h to fully recharge the battery pack.

#### To fast-charge or slow-charge the battery pack while the PAK MKII is not operational:

1. Ensure the PAK MKII is powered-down.
2. Press button 1 to power-up.
3. When START? or SRT? appears on the display, use button 1 to scroll through the menu until the display shows FSTCHRG? or FCH? respectively SLOCHRG? or SCH?.
4. Press button 2 to select this menu item. The display shows SURE? or SURE.
5. Press button 2 again. It may take up to 5 min before charging commences.
6. LEDs 3, 2 and 1 will light up in sequence. The sequence will be slower for slow-charge.

#### To slow-charge the battery pack while the PAK MKII is operational:

1. If the PAK MKII is powered-down, first power-up the PAK MKII as usual. Wait for the PAK MKII to boot (i.e. until Idle... or Idle is displayed).
2. Scroll using button 1 and 2 until the display shows SLOCHRG? or SCH?.
3. Press button 2 to select this menu item. The display shows SURE? or SURE.
4. Press button 2 again. It may take up to 5 min before charging commences.
5. LEDs 3, 2 and 1 will light up in sequence. The sequence will be slower than fast-charge.
6. The User may now continue to use the PAK MKII system.
7. To end charging, scroll to select and execute the menu item ENDCHRG? or ECH?.

# using the PAK MKII

## INFO

This menu item shows information and firmware versions related to the PQ12, PQ20 or PQ30.

The information displayed is (for example):

1. The PSU firmware version currently executing on the PQ12, PQ20 or PQ30:

PSU Firmware : 1

2. The hardware version information for the PQ12, PQ20 or PQ30 that includes the name, revision and build number for the printed-circuit board (PCB):

PCB Name : PQ30

PCB Rev : 0

PCB Build : AAAA

3. The UPS, CPLD and FPGA firmware programmed onto the PQ12, PQ20 or PQ30 which is not remotely upgradable and hence their current version is displayed here (note that this information is related to the PQ12, PQ20 or PQ30 build number):

UPS Firmware : 01

CPLD Firmware : 01

FPGA Firmware : 01

4. The PQ12, PQ20 or PQ30 serial number (shown without the center 'M' character for space reasons):

Serial Number : 05062269

## User Interface for the PQ12, PQ20 and PQ30

continued

## NOTE:

For a MF02 (8 cell battery pack) the voltage levels are as follows:

- BAT FULL (> 10 V)
- BAT OK+ (9.4 V to 10 V)
- BAT OK- (8.6 V to 9.4 V)
- BAT LOW (< 8.6 V).

For a MF03, MF04, MF06 and MF10 (12 cell battery pack) the voltages levels are as follows:

- BAT FULL (> 15.6 V)
- BAT OK+ (13.2 V to 15.6 V)
- BAT OK- (12.7 V to 13.2 V)
- BAT LOW (< 12.7 V).

## BATTERY PACK TEMPERATURE (BAT STS? OR BAT?)

For the status of the PAK MKII battery pack:

Scroll until BAT STS? or BAT? is displayed.

1. Select using button 2.
2. Display shows SURE? or SURE. Press button 2 to select again.
3. Display shows WAIT... or WAIT. During this time the system will run off the battery pack while measuring its voltage.
4. The display shows BAT:xxx.x where xxx.x is the current battery pack voltage. The nominal voltage is 9.6 V but may vary depending on the residual charge.
5. A comment regarding the battery pack status is displayed based on the battery pack voltage.
6. The battery pack temperature will be displayed in degrees Celsius.
7. The system will then return to its normal display.

## User Interface for the PQ12, PQ20 and PQ30

continued

### NOTE:

- If menu item BAT STS? or BAT? is displayed but no valid battery pack is fitted, the display will show the message NO BAT or NOBT.

### WARNING:

If the battery pack is nearly or completely discharged the system might reset.

### TEMP? OR TMP?

For the status of the temperature of the PQ12, PQ20 and PQ30

1. Scroll until TEMP? or TMP? is displayed.
2. Select using button 2.
3. Display shows SURE? or SURE Press button 2 to select again.
4. Display shows xx.xDEGC (xx.x the temperature in °C) or on the PQ30 it displays xx.xx followed by DEGC.
5. The system will then return to its normal display.

### POWER SUPPLY STATUS: PSTATUS? OR PST?

This menu item measures and displays the electrical voltage and/or current levels of the current PAK MKII power input as well as that of internal power supplies that form part of the PAK MKII power supply function.

1. Press SCROLL until PSTATUS? or PST? is displayed.
2. Press the SELECT button, the display shows SURE? or SURE.
3. Press the SELECT button again and some or all of the following information will be displayed:
  - PSTATUS or PST:  
Power Supply Firmware Version
  - PSV: xx Indicates the currently executing power supply firmware version
  - VSTATUS or VST:  
Voltages (the valid voltage range is shown in brackets):
    - VP: xx.x:  
Primary input voltage (measured at the PAK MKII power input)
    - VS: .xx:  
Secondary input voltage (battery pack)
    - VF: .xx  
Final input voltage used by UPS to supply the PAK MKII
    - V3: .xx  
Voltage of 3.3 V supply (3.2 V to 3.45 V)
    - V5: .xx  
Voltage of 5 V supply (4.85 V to 5.25 V)
    - V12: .xx  
Voltage of 12 V supply (11.7 V to 12.6 V)
    - V20: .xx  
Voltage of 20 V intermediate supply (20 V to 32 V)

# using the PAK MKII

- ISTATUS or IST:  
Currents:
- IP: xx.x  
Primary input current (measured at the PAK MKII power input)
- IB: +/-xx.x  
Battery pack input(+)/output(-) current
- I33: xx.x  
Current of 3.3 V supply
- I5: xx.x  
Current of 5 V supply
- I12: xx.x  
Current of 12 V supply
- I20: xx.x  
Current of 20 V intermediate supply

4. The system will automatically return to its normal display.

## NET SWAP

The Net Swap menu item requests the PAK MKII to swap between the Ethernet and Wireless LAN network interfaces in order to activate the current non-active interface and to deactivate the current active interface. To activate the Wireless LAN network interface a Wireless LAN PCMCIA card must already be inserted before this menu item is selected.

1. Press SCROLL until NET Swap is displayed.
2. Press SELECT, the display shows SURE?.
3. Press SELECT again, the result of the request is displayed when completed.
4. The system will then return to its normal display.

## NET IF?

The NET IF? menu item requests the PAK MKII to display which network interface (Ethernet or Wireless LAN) is currently active.

1. Press SCROLL until NET IF? is displayed.
2. Press SELECT, the display shows SURE?.
3. Press SELECT again, information about the currently active network interface is displayed for example Ethernet is currently active or WLAN is currently active.
4. The system will automatically return to its normal display.

## User Interface for the PQ12, PQ20 and PQ30

continued

### NOTE:

- The PQ30 does not provide the NET Swap option as it does not support Wireless LAN.

### NOTE:

- The PQ30 does not provide the NET IF option.

# chapter three

## User Interface for the PQ12, PQ20 and PQ30

continued

### NOTE:

- To determine the current power supply firmware version see the description for menu item PSTATUS? or PST?.

### WLAN?

This menu item will request the PAK MKII to display the current values of the main Wireless LAN parameters. A Wireless LAN PCMCIA card does not have to be present for this function to execute successfully. The PQ30 does not provide the WLAN option.

1. Press SCROLL until WLAN? is displayed.
2. Press SELECT, the display shows SURE?.
3. Press SELECT again, the Wireless LAN parameters are displayed.
4. The system will automatically return to its normal display.

### AUTO ON? / MAN ON?

MAN ON? (Manual On) – The user switches the PAK MKII on using the user interface.

AUTO ON? (Automatic On) – The user can either switch the PAK MKII on using the user interface, or the PAK MKII will switch itself on when it detects a voltage is present at its power connector. (Please note that the default mode is MAN ON whereby the user switches the PAK MKII on using the user interface.)

AUTO ON is intended for use when the location of the PAK MKII makes it difficult for the user to reach the user interface. In that instance once external power has been switched on, the PAK MKII will power up. (Please note that for AUTO ON to work, the PAK MKII must detect a change in voltage at its power connector. Typically this change would be from 0 V to 12..30 V.)

To set the AUTO ON option:

1. Select AUTO ON?
2. Press button 2 to confirm. The display shows SURE?.
3. Press button 2 again. The PAK MKII system will now turn on automatically when power is applied. When power is applied the display will show ON IN 5s (5 s) and count down to 0 s before completely starting the system. During this count down the user can halt the count down by pressing any user interface button. Normal functions available before startup can then be selected in the usual manner. If left to count down the system will start.

To set the MAN ON option:

1. Select MAN ON?
2. Press button 2 to confirm. The display shows SURE?. This will restore the system power up option back to the manual on.

# using the PAK MKII

## FIRMWARE UPGRADE MESSAGES

Once a PAK MKII system has booted successfully, the PAK software is able to upgrade the PAK MKII firmware over the network connection, should this be necessary. The PAK MKII firmware is further subdivided into 3 sections each corresponding to the target device i.e. SC4x/Controller/MiniTerminal. During an upgrade, a message indicating the firmware section currently being upgraded is displayed as follows:

- Wait:SCU or SCU – The message is displayed while SC4x, Controller and MiniTerminal firmware is being upgraded from over the network
- Wait:UGS or UGS – The message is displayed while SC4x firmware is being upgraded from over the network
- Wait:UGI or UGI – This message is displayed while Controller firmware is being upgraded from over the network
- Wait:UMT or UMT – This message is displayed while MiniTerminal firmware is being upgraded from over the network
- Wait:MDU or MDU – This message is displayed while Module firmware is being upgraded from the SC4x

PAK 5.6 and later additionally indicates an upgrade progress percentage on the display during booting and upgrading.

## POWER SUPPLY FIRMWARE UPGRADING

The power supply firmware is upgradable. If required, this upgrading will automatically occur during the boot up of the PAK MKII and will therefore interrupt the normal boot-up procedure.

The power supply firmware upgrading can be identified by the message BootLoad or Boot initially appearing on the PAK MKII display for a few seconds. Thereafter the symbols ////////////// rotate on the display. As an additional indication of this mode, LED 1 blinks on and off. After the upgrade process has completed successfully (which may take up to 1 minute) the message START? or SRT? will appear on the display. Boot the PAK MKII again by pressing SELECT (SURE? or SURE appears on the display) and SELECT again to confirm. If START? or SRT? does not appear after several minutes the PAK MKII may be powered-down and powered-up again to re-execute the power supply firmware upgrade procedure.

The power supply firmware upgrading can typically be expected after the PAK MKII has been programmed with new firmware.

## User Interface for the PQ12, PQ20 and PQ30

continued

# chapter three

## User Interface for the PQ12, PQ20 and PQ30

continued

### NOTE:

- Only the first reason mentioned for LED 3 flashing is self-recovering in that charging will commence as soon as the battery pack temperature reaches the valid range.
- If the battery pack is damaged or not connected, the UPS will not function. However, the PAK MKII should still be able to function normally from an external power source.
- Due to the properties of NiCd rechargeable batteries, recharging can only be performed when the battery pack is in the temperature range of 10 °C to 45 °C.

### INTERPRETING THE LEDS

1. LED 1 On: System running from the battery pack.
2. LED 1 Pulsing once every five seconds: System is alive.
3. LED 2 Flashing: Battery pack low. BAT LOW or LOW will appear on the display. When the capacity of the battery pack is exhausted the system will switch off and valuable data may be lost. It is therefore important to halt all tests as quickly as possible or reconnect external power should this occur.
4. LED 3 Flashing: Battery pack error. Possible reasons include :
  - The battery pack temperature is out of the valid charging range
  - The temperature sensor of the battery pack is malfunctioning
  - The maximum cell voltage exceeds 1.8 V (for NiCd and Ni-MH packs)
  - The input voltage to the battery charger of the PAK MKII power supply board is too low. This can either be caused by a fault on the PAK MKII power supply board or an unstable external input voltage supplied to the PAK MKII
  - No battery pack is present
5. LED 3, 2, 1 Flashing in sequence: Battery pack is being charged.
6. LED P on: The polarity of the power input supplied to the PAK MKII is incorrect.
7. LED U on: The power input voltage is above or below the allowed voltages.



# using the PAK MKII

Over temperature shutdown functionality is included in the PAK MKII firmware to protect against overheating. The over temperature protection in the PAK MKII firmware periodically measures the temperature of each Module and VMEbus board present in the system in order to determine the maximum temperature value (`MaxTemp` or `Max`) inside the PAK MKII. The `MaxTemp` or `Max` value initiates the following actions:

MaxTemp < 83 °C	No action
83 °C < MaxTemp < 85 °C	Fan action: The speed of the fan (if present) will be automatically set to full speed, thereby overriding the User value. Once the MaxTemp has fallen below 80 °C the speed of the fan will return to the previously selected User value.
85 °C < MaxTemp < 86 °C	5 minute countdown: The PAK MKII firmware will begin a 5 minute countdown after which it will automatically switch off the PAK MKII unless <code>MaxTemp</code> or <code>Max</code> falls below 85 °C again. Information on the countdown will be written to the PAK MKII User Interface display on a continuous basis.
MaxTemp > 86 °C	Shutdown: Even if the 5 minute countdown has not yet been completed, the PAK MKII will switch off immediately. At shutdown the message <code>SYSOFF</code> or <code>OFF</code> will appear on the display for a few seconds.

## Temperature Protection and Cooling

### NOTE:

- `TEMP?` or `TMP?` displays only the temperature of the system board on which the User Interface is located. This temperature is typically from 2 °C to 10 °C lower than `MaxTemp` or `Max`, depending on the PAK MKII configuration.

### NOTE:

The Dynamic Speed option sets the fan Controller to constantly evaluate the current temperature of the PAK MKII with respect to a reference value, and adjust the fan speed accordingly. If it is 3 °C higher than the reference value, it will set the fan to full speed and if it is 3 °C below, it will stop the fan. For temperatures between these two extremes, it will set the speed of the fan depending on how much above or below the reference value it is. The reference value is determined by the User selecting either “Lower Temperature” (reference value is 55 °C), or “Lower Speed” (reference value is 65 °C).

# chapter three

## Automatic Upgrades

The PAK MKII system may require automatic firmware upgrades from time to time. This will typically initiate after installation of a new PAK version/service release and builds, or after any PAK MKII hardware component changes.

### **WARNING:**

Never switch off or reset the PAK MKII while it is busy booting or while a firmware upgrade is in progress. This could permanently damage the system. Only when the PAK MKII display indicates IDLE or FAIL is further User interaction required.

### **FIRMWARE UPGRADE**

A firmware upgrade can take a couple of minutes to complete, and is indicated on the PAK MKII display by either:

- Wait:SCU or :SCU
- Wait:UGS or :UGS
- Wait:UGI or :UGI
- Wait:UMT or :UMT
- Wait:MDU or :MDU

PAK 5.6 and later additionally indicates an upgrade progress percentage on the display during boot-up and upgrading.

The system will reset automatically if required after upgrading, and should recover automatically in the unlikely event of a failed upgrade effort.

# using the PAK MKII

The PAK MKII contains a web server which provides an additional interface to configure the PAK MKII. The web server is accessed by opening a web browser on a PC, connected to the same network as the PAK MKII, and typing in the PAK MKII IP address in the browser's 'Address' field.

## Web Server

### WEB SERVER

The following PAK MKII parameters can be configured via the web server:

1. IP address
2. Wireless LAN parameters (only visible for Controller boards with a Wireless LAN interface)
3. Default fan speed and fan behavior (applicable only to Mainframes with fans). For further details on Dynamic Speed option see temperature protection and cooling
4. MiniTerminal enable/disable
5. PAK MKII on/off and restart
6. Power saving options
7. Battery parameters (only when a battery is detected)
8. Current Controller board firmware
9. Signal conditioning board firmware
10. Signal conditioner board boot status
11. Boot parameters

In the bottom right hand corner of the main page an information icon links to a web page that contains the following PAK MKII system information:

1. Controller card type and serial number
2. System card types and serial numbers
3. Module types, slot specifications, build numbers and serial numbers
4. Firmware revisions

# chapter three

Web Server System Information e.g. PQ30

The screenshot displays the 'PAK MK II Configuration' page of the MÜLLER-BBM VibroAkustik Systeme web interface. The top navigation bar includes the company logo and a blue header bar with a waveform graphic. Below the header, there are four small thumbnail images: a white airplane, a white car, a bridge, and a water drop. The main content area is titled 'PAK MK II Configuration'.

**System Info**

**Controller Information**

Controller Type:	PQ30
Serial Number:	0310M9103
Build Revisions:	A*AA

**Network Settings**

**Basic Settings**

Controller Firmware:	4-4-g 10300212
FPGA Revision:	f

**Power Options**

**Battery**

**Power Supply Information**

**Advanced**

Power Supply Firmware:	11
Power Consumption:	56.03 W
Power Supply Temperature:	50 degC
Current Fan Speed:	Off

**Signal Conditioner Information**

Firmware: 4-4-a 14272911

Slot	Type	Serial Number	Build
1	SC42S5	0110M8915	DCCB
2	SC42S5	0110M8923	DCCB

**Module Information**

Slot	Type	Type ID	Build	Serial Number	Temp
1.1	ICP42S8	0x58	BCAGS	1109M8306	54 degC
1.2	ICP42S8	0x58	BCAGS	1008M5611	56 degC
1.3	ICP42S8	0x58	BCAGS	1109M8207	56 degC
1.4	ICP42S8	0x58	BCAGS	1109M8222	54 degC
2.1	ICM42S1	0x54	CE*BS	0610M9564	54 degC
2.2	ICM42S1	0x54	CE*BS	0610M9572	57 degC
2.3	ICM42S1	0x54	CE*BS	0610M9565	56 degC
2.4	ICM42S1	0x54	CE*BS	0610M9570	53 degC

[printer friendly view](#)

The System Info section includes **Controller Information**, **Power Supply Information**, **Signal Conditioner Information** as well as **Module Information**.

# using the PAK MKII

Network Settings e.g. PQ20

The screenshot shows the 'PAK MK II Configuration' interface for the MÜLLER-BBM VibroAkustik Systeme. The left sidebar has navigation links: System Info, Network Settings (which is selected and highlighted in blue), Basic Settings, Power Options, Battery, and Advanced. The main content area is divided into three sections: LAN Settings, WLAN Settings, and Network Status.

**LAN Settings**

MAC Address:	00:07:47:01:03:5c
IP Address:	192.168.1.249
Password:	[redacted]
<input type="button" value="Submit"/>	

**WLAN Settings**

MAC Address:	No hardware detected
Current Signal Strength:	na
Current Bit Rate:	na
IP Address:	192.168.2.204
Network Name:	pak-mobil-01
Network Mode:	Adhoc
Channel Number:	3
Encryption Key:	[redacted]
Encryption:	Disabled
Password:	[redacted]
<input type="button" value="Submit"/>	

**Network Status**

Active Interface:	LAN
Set Active:	LAN
Password:	[redacted]
<input type="button" value="Submit"/>	

*- Page may fail to redirect if new IP is on a different subnet.*

The Network Settings section includes **LAN Settings**, **WLAN Settings** and **Network Status**.

# chapter three

Basic Settings e.g. PQ20

The screenshot shows the 'PAK MK II Configuration' interface. On the left, a sidebar lists navigation options: System Info, Network Settings, Basic Settings (which is selected and highlighted in blue), and Power Options. Below the sidebar are four small thumbnail images: a white aircraft, a car wheel, a sunburst pattern, and a water droplet.

**Fan Settings**

Current Fan Speed:	Maximum
Fan Behaviour:	Constant Speed
Fan Speed Setting:	Maximum
Submit	

**Mini-Terminal Settings**

Current Status:	Active: No MT detected
Status on Bootup:	Enabled
Submit	

**Turn Off MKII**

Setting:	Choose Option
Confirm:	
Submit	

Basic Settings section includes **FAN Settings** (for PAK MKII Mainframes where fan is present), **MiniTerminal Settings**, **Turn off PAK MKII Settings** (such as restart, standby and switchoff).

## WARNING:

Never switch off or reset the PAK MKII while it is busy booting or while a firmware upgrade is in progress. This could permanently damage the system. Only when the PAK MKII display indicates IDLE or FAIL is further user interaction required.

# using the PAK MKII

Power Options e.g. PQ30

The screenshot shows the MÜLLER-BBM VibroAkustik Systeme web interface. The top navigation bar includes icons for a plane, a car, a fan, and a ship. The main title is "PAK MK II Configuration". On the left, a sidebar lists "System Info", "Network Settings", "Basic Settings", "Power Options" (which is selected), "Battery", "Advanced", and "Local Storage". The "Power Options" section contains three tabs: "General", "Power Scheme Settings: Global", and "Power Schema Settings: PAK MKII Running on Battery". The "General" tab shows "Power Status: Active and Ready" and "Power Source: Plugged". The "Power Scheme Settings: Global" tab shows "Power Down after: Never" for both "No Activity" and "Standby after". The "Power Schema Settings: PAK MKII Running on Battery" tab shows "Power Down after: Never" for both "No Activity" and "Standby after". A "Submit" button is at the bottom of this tab.

The Power Options section includes General; Power Scheme Settings: Global and Power; Schema Settings: PAK MKII Running on Battery

# chapter three

Battery e.g. PQ20

The screenshot displays the 'PAK MK II Configuration' interface for the MÜLLER-BBM VibroAkustik Systeme. On the left, a vertical menu lists 'System Info', 'Network Settings', 'Basic Settings', 'Power Options', 'Battery' (which is highlighted in blue), and 'Advanced'. The main content area is divided into three sections: 'General Information' (Power Source: Plugged, Battery Pack Type: [empty]), 'Battery Status' (Current Charge: na, Battery Pack Voltage: na, Battery Temperature: +24, Update button), and 'Battery Pack' (Battery is Currently: Trickle Charging, Action: Choose Option dropdown, Submit button). A note at the bottom states: '- Slow Charging may cause noise interference during measurements  
- Updating the battery voltage and charge state may cause noise, or in the worst case the system to switch off if the battery is low.'

Battery section includes **General Information**, **Battery Status** (updated after selecting Update option). If the PAK MKII does not contain a battery, the web server will display "No battery has been detected in this system".

# using the PAK MKII

Advanced e.g. PQ20

MÜLLER-BBM  
VibroAkustik Systeme

PAK MK II Configuration

System Info

Network Settings

Basic Settings

Power Options

Battery

Advanced

**Change Password**

Current Password:

New Password:

Confirm New Password:

**Submit**

**Low Level Information**

Type:

**Submit**

Advanced section includes **Change Password** (A password must consist of a minimum of 4 characters.), **Low Level Information** (Only the initial password is shown as password. Once changed it is shown as xxxxxx).

# chapter three

Local Storage e.g. PQ30

The screenshot shows a web-based configuration interface for the MÜLLER-BBM VibroAkustik Systeme PAK MK II. The top header features the company logo and the text "VibroAkustik Systeme". Below the header, there are four small thumbnail images: a white airplane, a green car, a sunburst, and a water droplet. The main title "PAK MK II Configuration" is centered above the configuration panels.

The left sidebar contains navigation links: System Info, Network Settings, Basic Settings, Power Options, Battery, Advanced, and Local Storage. The "Local Storage" link is highlighted with a blue bar and a blue bullet point.

The right side of the interface is divided into several configuration sections:

- Storage Device Selection**:  
Current Storage Device: Internal  
Preferred Storage Device: Internal  
Change Preferred Device: A dropdown menu with options "Internal" (selected) and "External".
- Format Storage Device**:  
Setting: Choose Option (dropdown menu)  
Confirm: (empty input field)  
Submit: (button)
- S.M.A.R.T overall-health self-assessment test result:** Passed

# using the PAK MKII

Local Storage e.g. PQ30 continued

## General S.M.A.R.T Values:

Offline Status:	(0x00) Offline Collection Never Started
Self Test Status:	(0) Self Test Completed or Not Run, 0 seconds remain
Offline Completion time:	120 seconds
Offline Capability:	(0x5B)
S.M.A.R.T Capability:	(0x0003)
Error Logging Capability:	(0x00)
Short Self Test Polling Time:	2 minutes
Extended Self Test Polling Time:	12 minutes
Conveyance Self Test Polling Time:	0 minutes

## Vendor Specific S.M.A.R.T Attributes with Thresholds:

ID	Attribute Name	Flag	Value	Worst	Thresh	Type	Updated
1	Raw Read Error Rate	0x0Ah	100	100	0	Advisory	Always
2	Throughput Performance	0x05h	100	100	50	Pre-Failure	Offline
3	Spin Up Time	0x07h	100	100	50	Pre-Failure	Always
5	Reallocated Sector Count	0x13h	100	100	50	Pre-Failure	Always
7	Seek Error Rate	0x0Bh	100	100	50	Pre-Failure	Always
8	Seek Time Performance	0x05h	100	100	50	Pre-Failure	Offline
9	Power-On Hours Count	0x12h	100	100	0	Advisory	Always
10	Spin-up Retry Count	0x13h	100	100	50	Pre-Failure	Always
12	Power Cycle Count	0x12h	100	100	0	Advisory	Always
167	Unknown Vendor Specific Attribute	0x22h	100	100	0	Advisory	Always
168	Unknown Vendor Specific Attribute	0x12h	100	100	0	Advisory	Always
169	Unknown Vendor Specific Attribute	0x13h	100	100	10	Pre-Failure	Always
173	Unknown Vendor Specific Attribute	0x12h	200	200	0	Advisory	Always
175	Unknown Vendor Specific Attribute	0x13h	100	100	10	Pre-Failure	Always
192	Power-Off Retract Cycle	0x12h	100	100	0	Advisory	Always
194	HDA Temperature	0x23h	71	39	30	Pre-Failure	Always
197	Current Pending Sector Count	0x12h	100	100	0	Advisory	Always
240	Head Flying Hours	0x13h	100	100	50	Pre-Failure	Always

The Local Storage section includes Storage Device Selection, Format Storage Device and S.M.A.R.T. overall-health self-assessment test result. If the PAK MKII does not contain a local storage option, the web server will not display the section.

# PAK MKII



# GETTING TO KNOW the PAK MKII

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## Mainframes

The Mainframe of the PAK MKII refers to the enclosure in which the PAK MKII system boards, the VMEbus backplane, the battery pack (if present) and fans (if present) are housed. 5 different series of Mainframes exist namely:

1. MF02: 2-slot PAK MKII Mainframe
2. MF03: 3-slot PAK MKII extended temperature Mainframe
3. MF04: 4-slot PAK MKII extended temperature Mainframe
4. MF06: 6-slot PAK MKII extended temperature Mainframe
5. MF10: 10-slot PAK MKII extended temperature Mainframe

### NOTE:

Numbering of VMEbus slots starts at the bottom.



MF04 front view

Mainframes are machined from aluminum and accommodate between 2 and 10 VMEbus boards.

The PAK MKII system's Power Supply is contained on a VMEbus board. This enhances the modularity of the system as it can be readily maintained and upgraded. Third party VMEbus boards designed according to IEEE 1101.2 can also be accommodated. An optional battery is contained behind the backplane.

All VMEbus boards are cooled by conduction only. This is advantageous as no dirty or dusty air moves within the Mainframe. The external surfaces of the smaller Mainframes (MF02, MF03) are cooled through natural convection. The MF04 and MF06 are cooled through a combination of natural and external forced convection while the MF10 is externally cooled by forced convection only. Where forced convection is provided, the fan speed is controlled by software to maintain a suitable running temperature. For noise sensitive measurements the fan can be switched off for periods of up to 20 minutes during which time the Mainframe acts as a large heat sink. The fan is automatically restarted when the Mainframe becomes too hot.

### NOTE:

A convenient carrying handle is provided for all Mainframes except the 10-slot Mainframes. It can be removed when required.

# getting to know the PAK MKII

## Mainframe Specifications

MF02 (M515)	slot 1:	PQ12/PQ20/PQ30	Power Supply and System Controller	
	slot 2:	SC42/SC42S	Data acquisition	
	Number of channels (if 4ch/Module):	16	Fan:	None
	External surface cooling system:	Natural Convection	Internal board's cooling system:	Conduction
	Dimensions (W H D):	291 x 68 x 267 mm	Volume:	5.3 liter
	Mass fully populated with battery*:	4.3 kg	Mass fully populated without battery:	4.0 kg
	Battery type:	NiCd	Battery cells:	8
	Battery capacity:	16.3 Wh		
MF03 (M381)	slot 1:	PQ12/PQ20/PQ30	Power Supply and System Controller	
	slot 2 - 3:	SC42/SC42S	Data acquisition	
	Number of channels (if 4ch/Module):	32	Fan:	None
	External surface cooling system:	Natural Convection	Internal board's cooling system:	Conduction
	Dimensions (W H D):	307 x 88 x 267 mm	Volume:	7.2 liter
	Mass fully populated with battery*:	6.4 kg	Mass fully populated without battery:	5.6 kg
	Battery type:	NiCd	Battery cells:	12
	Battery capacity:	33.1 Wh		
MF04 (M386)	slot 1:	PQ20/PQ30	Power Supply and System Controller	
	slot 2-4:	SC42/SC42S	Data acquisition	
	Number of channels (if 4ch/Module):	48	Fan:	Yes
	External surface cooling system:	Natural/Forced Convection	Internal board's cooling system:	Conduction
	Dimensions (W H D):	307 x 109 x 287 mm	Volume:	9.6 liter
	Mass fully populated with battery*:	9.3 kg	Mass fully populated without battery:	8.5 kg
	Battery type:	NiCd	Battery cells:	12
	Battery capacity:	33.1 Wh		

# chapter four

## Mainframe Specifications continued

<b>MF06 (M382)</b>	slot 1:	PQ20/PQ30	Power Supply and System Controller	
	slot 2-6:	SC42/SC42S	Data acquisition	
	Number of channels (if 4ch/Module):	80	Fan:	Yes
	External surface cooling system:	Natural/Forced Convection	Internal board's cooling system:	Conduction
	Dimensions (W H D):	307 x 151 x 287 mm	Volume:	13.3 liter
	Mass fully populated with battery*:	13.4 kg	Mass fully populated without battery:	10.8 kg
	Battery type:	NiCd	Battery cells:	12
	Battery capacity:	72 Wh		
<b>MF10 (M395)</b>	slot 1:	PQ30	Power Supply and System Controller	
	slot 2-9:	SC42/SC42S	Data acquisition	
	slot 10:	SL2x	Synchronization option	
	Number of channels (if 4ch/Module)	128	Fan:	Yes
	External surface cooling system:	Forced Convection	Internal board's cooling system:	Conduction
	Dimensions (W H D):	291 x 231 x 333 mm	Volume:	22.3 liter
	Mass fully populated with battery*:	19.8 kg	Mass fully populated without battery:	17.3 kg
	Battery type:	NiCd	Battery cells:	12
	Battery capacity:	72 Wh		

Note: Mainframe slots are numbered from the bottom

\* Available slots populated with SC boards and ICP Modules.

# getting to know the PAK MKII

All PAK MKII systems are optionally equipped with an internal battery pack. When the power input voltage to the PAK MKII drops below the threshold voltage (typically between 8.5 and 9.6 V, depending on the power supply technology used) the UPS on a PQxx will supply the PAK MKII with power via the battery pack.

If the PAK MKII runs for more than 4 s from its battery pack, the message BACKUP or BKP will appear on the PAK MKII display.

If thereafter the PAK MKII power input voltage rises above the threshold, the UPS will automatically switch back to the PAK MKII power input as the primary power supply for the PAK MKII.

The PAK MKII can run from the battery pack for the specified battery pack temperature of -20 °C to 65 °C, although battery capacity will decrease at low temperatures. No protection is provided for the case when the PAK MKII attempts to run off the battery pack below -20 °C.

## Uninterruptible Power Supply (UPS)

### PLEASE REFER:

1. Chapter three:  
Using the PAK MKII:  
User interface of relevant board for information regarding the PAK MKII battery pack

# chapter four

## Fastening Points

### NOTE:

Numbering of VMEbus slots starts at the bottom.

### WARNING

Do not unscrew Mainframe screws while hot.

6 threaded female fastening points are present on both the top and bottom faces of the PAK MKII enclosure. The bottom face refers to the face closest to slot 1 of the Mainframe.

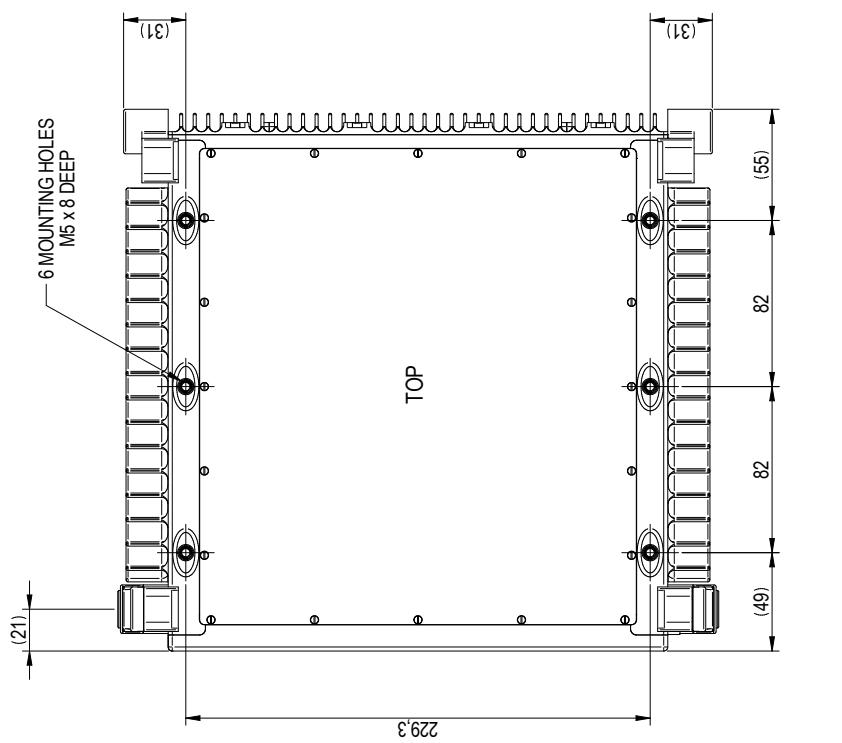
### Mainframe fastening points specifications

Parameter	Value
Hole size	M5 x 8 mm deep
Spacing between any 2 holes of the 3 holes running from front to rear	82 mm
Spacing between left and right sets of 3 holes	229.3 mm
Maximum shear/normal force applied to any screw	500 N

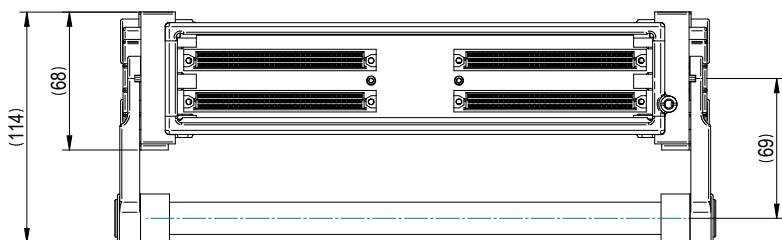
## Mainframe Dimensions

The dimensions of the various Mainframes are shown on the next few pages.

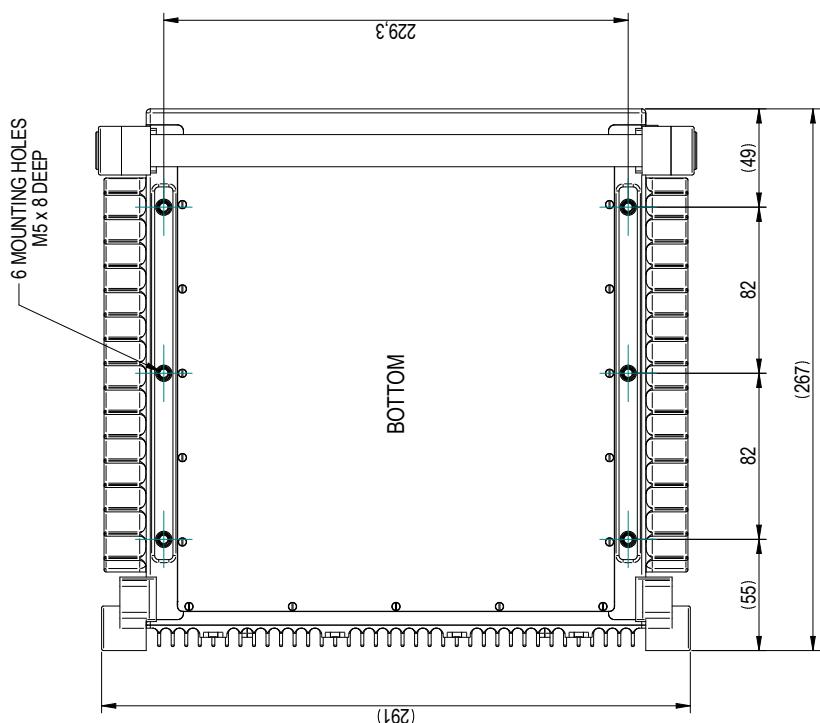
# getting to know the PAK MKII



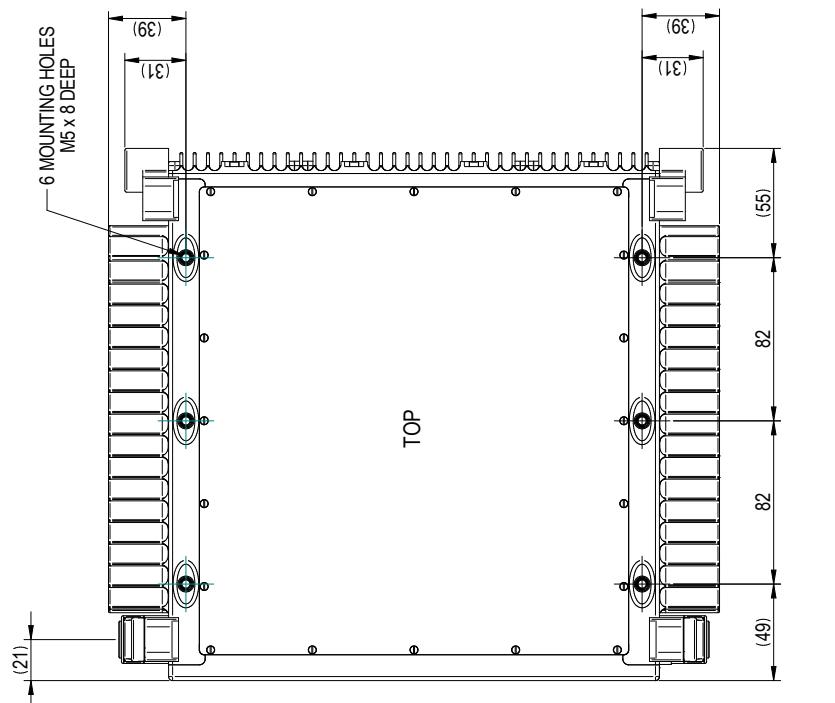
Dimensions MF02



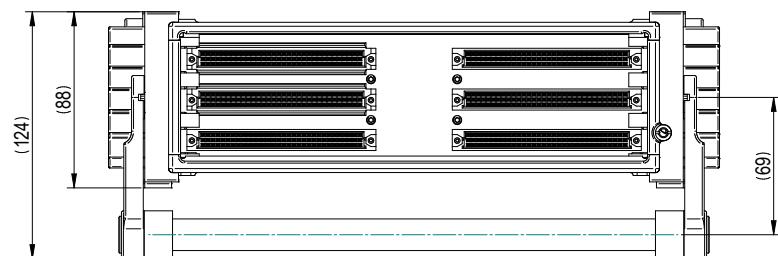
GENERAL SIZES AND MOUNTING DETAIL - MF02 (M515)



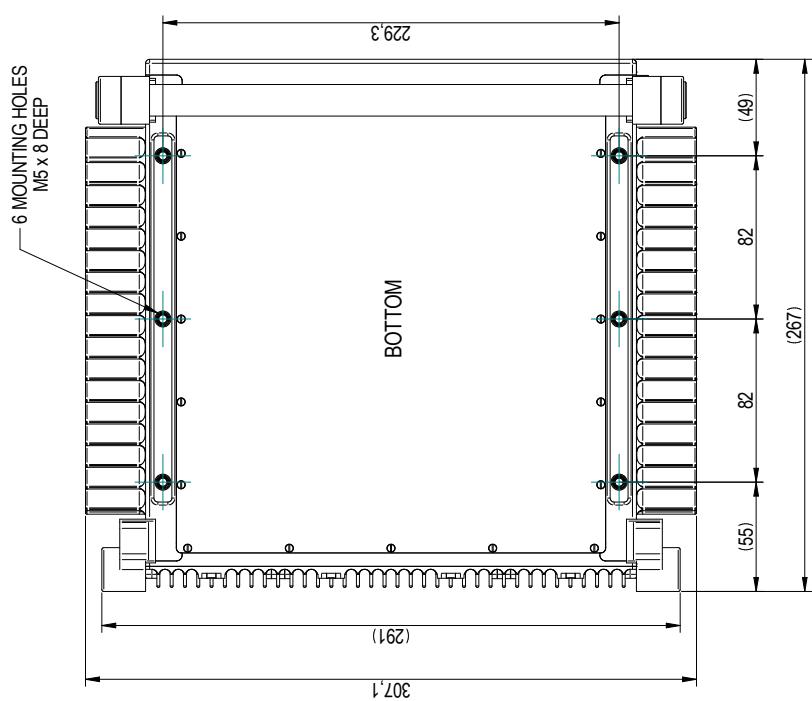
# chapter four



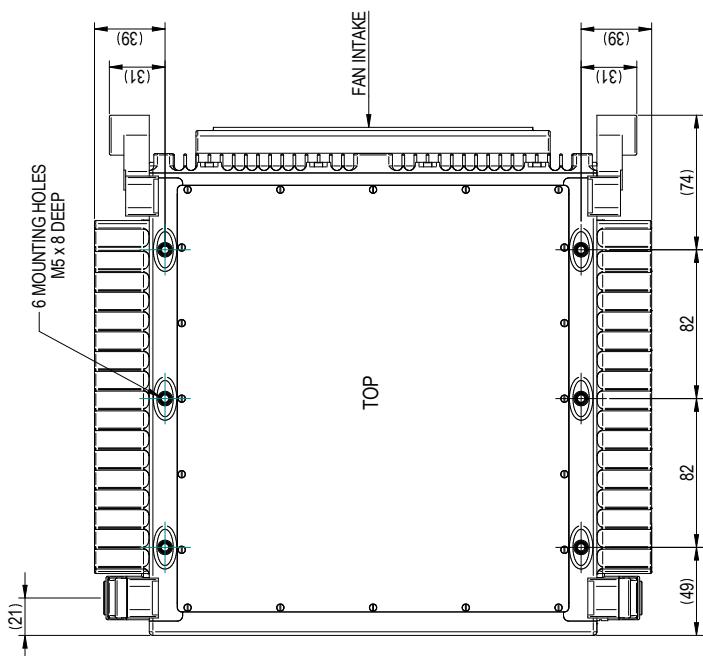
Dimensions MF03



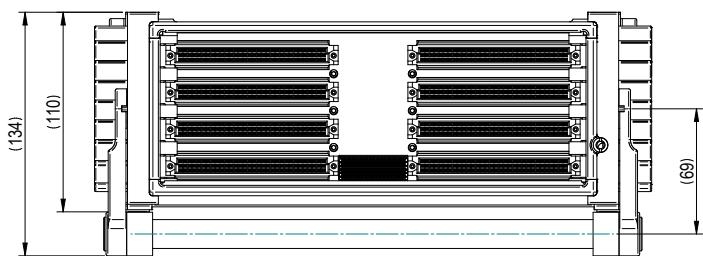
GENERAL SIZES AND MOUNTING DETAIL - MF03 (M381)



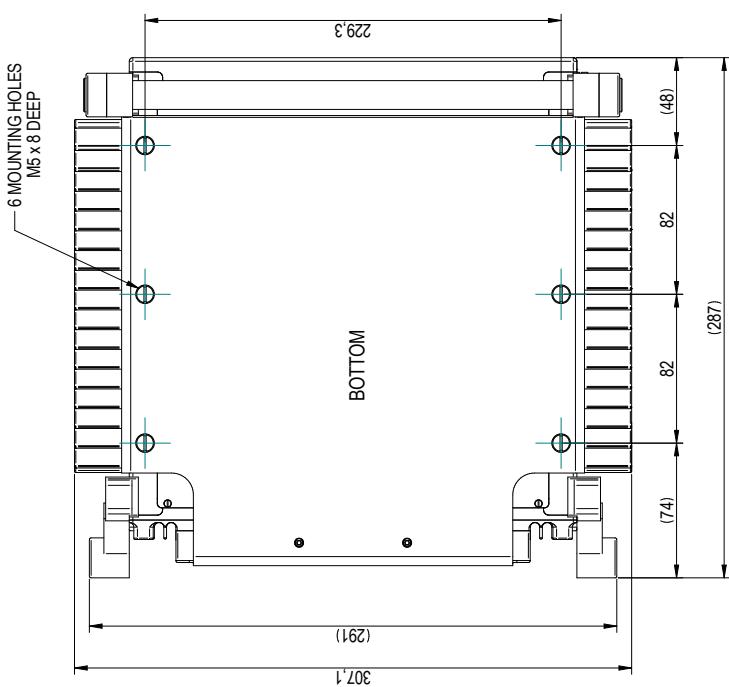
# getting to know the PAK MKII



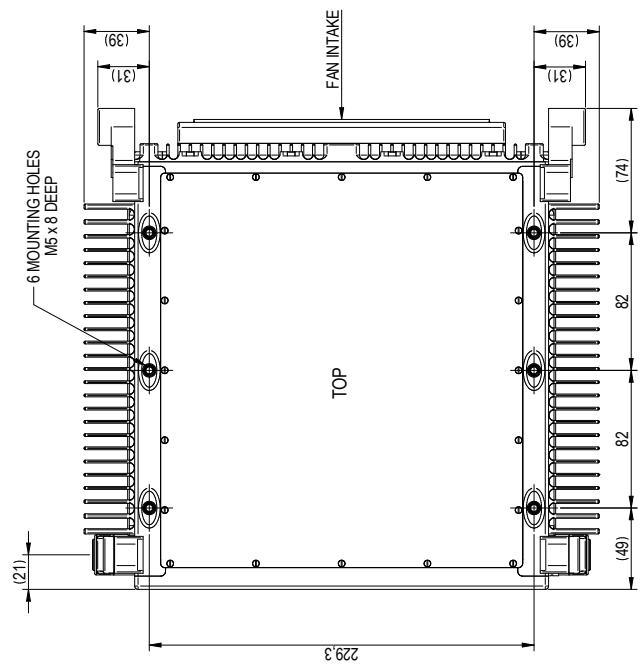
Dimensions MF04



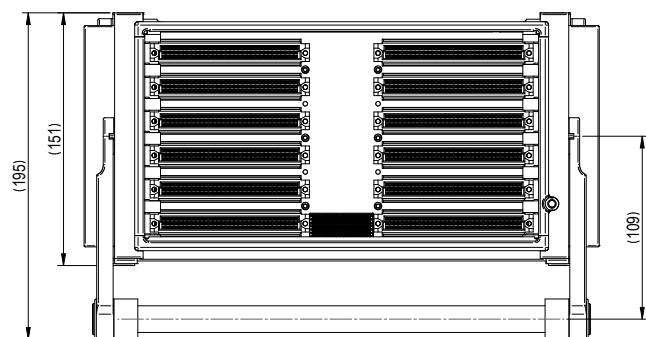
GENERAL SIZES AND MOUNTING DETAIL - MF04 (M386)



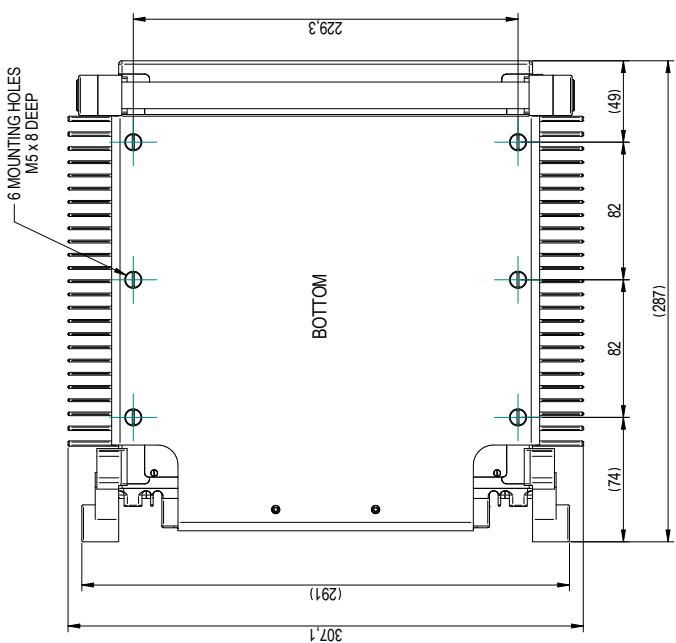
# chapter four



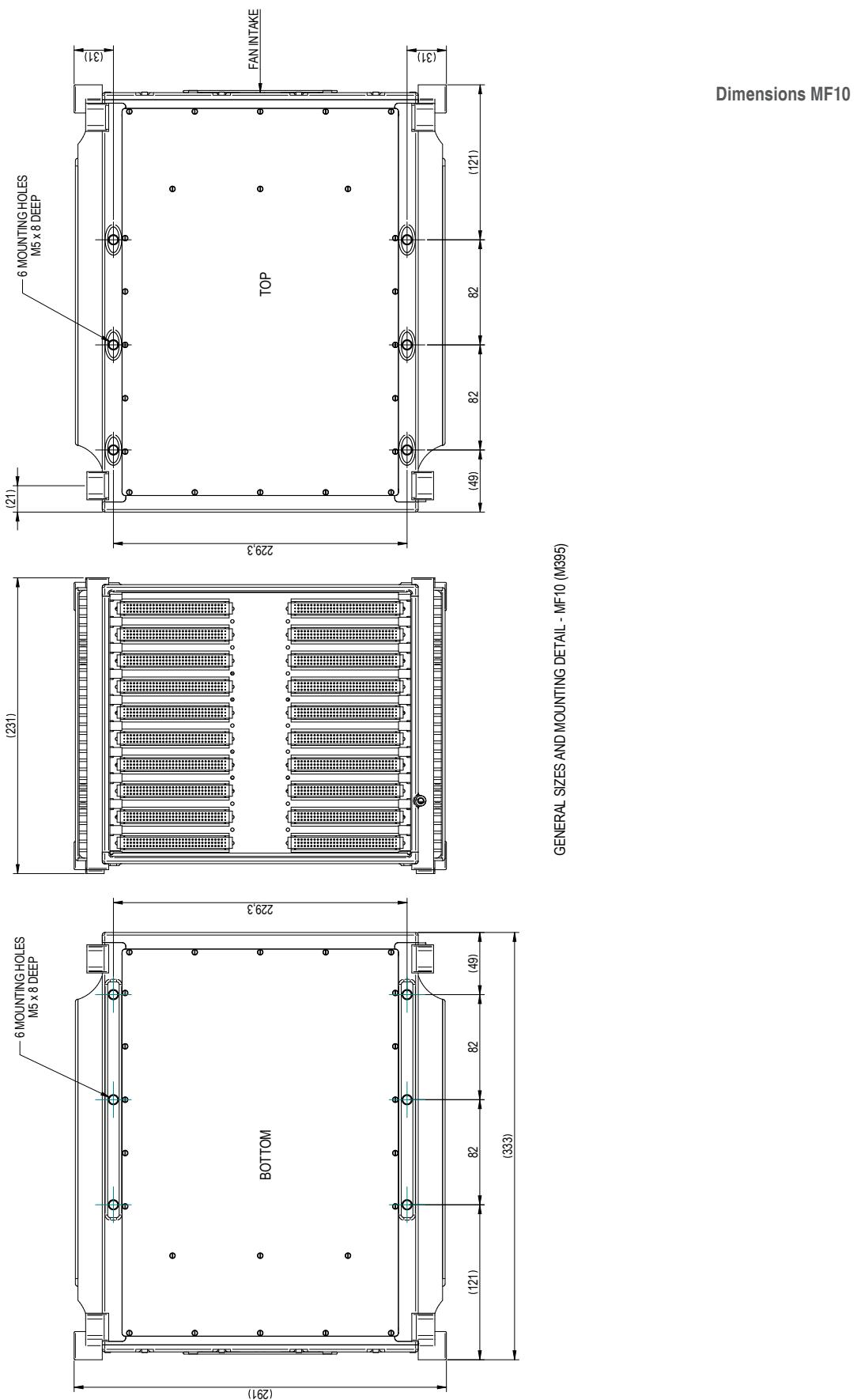
Dimensions MF06



GENERAL SIZES AND MOUNTING DETAIL - MF06 (M382)



# getting to know the PAK MKII



# chapter four

## Further System Specifications

Class	Property	MF02	MF03	MF04	MF06	MF10	Units
Physical	Maximum Environmental Temperature	62	60	58	56	55	°C
	Minimum Environmental Temperature	-20	-20	-20	-20	-20	°C
Power	Typical Power Input	External DC supply + Internal Battery Pack					
	Power Consumption (with most demanding Modules)	30	50	75	120	200	W
	Maximum Available Power	150	150	200	200	200	W

These values are an indication of the power consumption for typical Mainframe configurations, and are not intended as an explicit specification for the external power supply.

# getting to know the PAK MKII

## VMEbus boards

---

The PAK MKII system uses the VMEbus standard for its main communication bus. The VMEbus standard is a well defined mechanical and electrical standard. Each Mainframe houses a VMEbus backplane which will accept multiple VMEbus boards. For the PAK MKII system these VMEbus boards are designated PQx, SCx or SLx.

# chapter four

## PQ12 and PQ20



### NOTE:

TVS - Transient Voltage Suppressor Diode

MOV - Metal Oxide Varistor

EMI - Electro Magnetic Interference

The PQ12 is a dual function board combining a VMEbus System Controller, Master, Arbiter and Interrupt Handler with a 90 W VMEbus Power Supply for use in MF02 and MF03 Mainframes.

The PQ20 is a dual function board combining a VMEbus System Controller, Master, Arbiter and Interrupt Handler with a 150 W VMEbus Power Supply for use in MF04 and MF06 Mainframes. It can also be used in MF02 and MF03 Mainframes when higher data rates are required.

### FEATURES

1. VME64 single board Controller.
2. Contains the MPC866 processor running at a CPU clock frequency of 128 MHz.
3. Functions as Controller and power supply for MF02 and MF03 Mainframes. The PQ20 can also be used in MF04 and MF06 Mainframes.
4. 10/100 Mbit/s (half- and full-duplex) Ethernet interface with auto-negotiation and auto-MDI/MDIX.
5. IEEE 802.11 b Wireless LAN interface that is accessible at its front panel.
6. SyncLink interface.

For its power supply function the PQ12 contains a 90 W and the PQ20 a 150 W high-efficiency DC/DC power supply which supplies power to the rest of the PAK MKII system boards.

Each have the following features:

1. Voltage input range: 10 V to 30 V DC.
2. Continuous polarity reversal allowed up to 60 V.
3. Continuous over-voltage allowed up to 60 V.
4. Input current monitoring to guard against power input overload. Further over-voltage and over-current protection are provided by a fuse, TVS and MOV combination. A relay opens under fault conditions and isolates the power supply from damaging voltages and currents.
5. Over-voltage lockout (input voltage > 33 V).
6. Under-voltage lockout (no start-up with input voltage < 8.5 V) protects against erratic behavior at low input voltages and exceeding the input current limit.
7. Transient protection by TVS and MOV.
8. Feed-through filters incorporated in the power supply input lines for reduced EMI.

# getting to know the PAK MKII

9. Error LEDs indicate reverse polarity and out-of-range input voltage.
10. Low radiated noise achieved by out of phase and synchronized switching.

The PQ12/PQ20 power supply contains an Uninterruptible Power Supply for battery backup operation using the internal battery pack of the PAK MKII. A battery pack output voltage of 8.5 V to 24 V is supported regardless of the external power input voltage level (in other words, the threshold for switching between the power input and the battery pack is 8.5 V).

**The battery charger of the PQ12/PQ20 power supply has the following features:**

1. Support for multi-chemistry type batteries: NiCd with Ni-MH.
2. Support for a battery pack output voltage of 8.5 V to 24 V.
3. Constant charging current up to 3 A.
4. Programmable charge algorithm (12-bit DAC for voltage and current adjustment).
5. Battery identification, reading of charging parameters and temperature information stored on EEPROM on battery pack.
6. Improved isolation between the battery and the rest of the system in order to minimize leakage current during standby.

## PQ12 and PQ20 continued



PQ12 front panel



PQ20 front panel

## PQ12 AND PQ20 FRONT PANEL

The PQ12 and PQ20 front panel has the following features:

1. PCMCIA slot.
2. ENET (RJ45 female connector) provides the Ethernet interface.
3. SER1/2 (Lemo 0B.307 female connector) provides a serial interface to the MiniTerminal.
4. SL (Fiber-optic SC connector) provides a SyncLink receiver to connect to a SyncLink cluster.
5. A display with 8 characters which displays commands and system information.

# chapter four

## PQ12 and PQ20

continued

### PLEASE REFER:

1. Chapter four

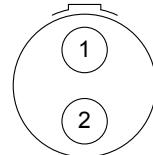
Getting to know the PAK MKII:

Power Cable Specifications

6. LEDs 1, P, 2, U and 3 provide system status and error information (positioned above the display).
7. Buttons 1 and 2 are used to access and perform different system functions.
8. Power input connector for connecting an external power supply to the PAK MKII.

### PQ12 PIN DEFINITION

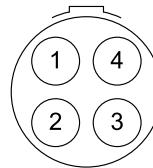
1. 2-pin Lemo connector (Lemo FGG.0B.302.CYCD562)
2. Pin 1 = -ve
3. Pin 2 = +ve



Pin definitions for the PQ12 2-pin Lemo power connector (when looking into the connector)

### PQ20 PIN DEFINITION

1. 4-pin Lemo connector (Lemo FGG.1B.304.CYCD72Z)
2. Pin 1 & Pin 4: +ve
3. Pin 2 & Pin 3: -ve



Pin definitions for the PQ20 4-pin Lemo power connector (when looking into the connector)

# getting to know the PAK MKII

The PQ30 is the latest addition to Mecalc's PQ family of VMEbus System Controllers. It replaces the PPC7D/VS20 combination with one VMEbus card, thus opening an additional slot in the Mainframe. It is a dual function board combining a VMEbus System Controller and a 200 W VMEbus Power Supply and features the latest VMEbus specification. The PQ30 is aimed at the high sampling rate/data throughput applications but can fulfill any of the current requirements. The PQ30 can be used in the 2-slot, 3-slot, 4-slot, 6-slot and 10-slot Mainframes.

## PQ30



Front panel PQ30



Front panel PQ30 with eSATA

### FEATURES:

1. VMEbus System Controller
2. 200 W VMEbus Power Supply, able to power up an MF10 Mainframe
3. 1 GHz PowerPC processor
4. 512 MByte DDR2 memory
5. 2 x 1 Gigabit Ethernet ports
6. PMC, PCI Mezzanine Card expansion slot
7. SyncLink input for synchronization in Cluster or SuperCluster
8. RS232 port for use with MiniTerminal
9. 10-32 V DC input from external source
10. UPS support for Mainframes with internal battery
11. Fast battery charger
12. New bottom cover for increased cooling and protection
13. Internal Solid-State Disk (SSD) for offline data storage (with PMC201) in different sizes
14. eSATAp port for future use (with PMC201)
15. Auto Power-On

### NOTE:

1. To utilize the maximum capabilities of the PQ30 it should be used in combination with the SC42S but is fully compatible with the SC42.
2. Please consult your local supplier to determine if your current mainframe is compatible or upgradable for the PQ30 Controller.
3. Only 42 series components will work with the PQ30 Controller.

### PLEASE REFER:

1. Chapter four:  
Getting to know the PAK MKII:  
Maximum Network Data Transfer  
Rates

## PQ30

continued

Controller Name	Features	Hard drive
PQ30	1 GHz PowerPC processor 512 MByte DDR2 memory	None (No PMC201 card is present.)
PQ30 (with PMC201)	1 GHz PowerPC processor 512 MByte DDR2 memory	Internal SSD

### DETAILED FEATURE DESCRIPTION

- VMEbus System Controller:  
The PQ30 is a VMEbus system controller in the PAK MKII. It exceeds the capabilities of the PPC7D/VS20 combination which it replaces.
- 200 W VMEbus Power Supply, able to power up an MF10 Mainframe:  
The Power Supply on the PQ30 has been increased to 200 W capable of powering up a fully populated 10-slot Mainframe with 8 SC42/42S cards and 1 SL21 card.
- 1 GHz PowerPC processor:  
Processing speed on the PQ30 has been increased. This allows faster data streaming between the analog front end and either the SSD or external PC running PAK.
- 512 MByte DDR2 memory:  
System memory on the PQ30 has been increased.
- 2 x 1 Gigabit Ethernet ports:  
Ethernet speed has been increased to Gigabit Ethernet. One port is for the transferring of data between the PAK MKII and the PC. The second port is reserved for future use.
- PMC, PCI Mezzanine Card expansion slot:  
The PMC slot can house a variety of PCI Mezzanine cards to increase the functionality of the PQ30.
- SyncLink input for synchronization in Cluster or SuperCluster:  
The SyncLink functionality is available on the PQ30.
- RS232 port for use with MiniTerminal:  
The RS232 port is still provided for use with the current and future versions of the MiniTerminal.

# getting to know the PAK MKII

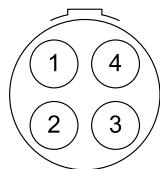
- 10-32 V DC input from external source:  
Power to the PQ30 remains the same as for the PQ12 and the PQ20, namely 10-32 V DC.
- UPS support for Mainframes with internal battery:  
The PQ30 provides UPS support for Mainframes with an internal battery.
- Fast battery charger:  
The PQ30 still provides the functionality to enable the User to charge the internal battery quickly.
- New bottom cover for increased cooling and protection:  
A new bottom cover has been designed to both protect and aid in the cooling of the PQ30.

## PQ30

continued

### PQ30 PIN DEFINITION

1. 4-pin Lemo connector (Lemo FGG.1B.304.CYCD72Z)
2. Pin 1 & Pin 4: +ve
3. Pin 2 & Pin 3: -ve



Pin definitions for the PQ30 4-pin Lemo power connector (when looking into the connector)

### PLEASE REFER:

1. Chapter four:  
Power Cable Specifications

# chapter four

## Power Cables

		Power Source			
		Bench / Battery	Cigarette Lighter Socket	Delta Brick (24 V, 180 W)	Deutronic Brick (24 V, 110 W)
System / Controller	MF02 (PQ12, PQ20, PQ30)	210K, 218K	211K, 219K	222K	212K, 220K
	MF03 (PQ12, PQ20, PQ30)	210K, 218K	211K, 219K	222K	212K, 220K
	MF04 (PQ20, PQ30)	213K, 216K, 221K	214K	215K, 217K	n.a.
	MF06 (PQ20, PQ30)	213K, 216K, 221K	214K	215K, 217K	n.a.
	MF10 (PQ30)	216K, 221K	n.a.	n.a.	n.a.

### POWER CABLE DETAILS

Target Controller(s)	Termination	Max. Current	Length	Name
PQ12 (Lemo FGG.0B.302.CYCD56)	Banana plugs	7.5 A	2.0 m	210K
			Variable	218K
	Cigarette lighter plug		2.0 m	211K
			Variable	219K
	Deutronic Brick (24 V, 110 W)		0.5 m	212K
			Variable	220K
			2.0 m	222K
			2.0 m	215K
PQ20, PQ30 (Lemo FGG.1B.304.CYCD.72Z)	Delta Brick (24 V, 180 W)	15.0 A	2.0 m	217K
			Variable	
	Banana plugs	20.0 A	2.0 m	213K
	Cigarette lighter plug		2.0 m	214K
	Banana plugs		2.0 m	216K
			Variable	221K

# getting to know the PAK MKII

## Fuse Specifications

The PQ12, PQ20 and PQ30 fuse is not User replaceable, and if blown the card must be returned for repair. A blown fuse is highly unlikely since it means that the primary relay protection circuit of the PQ12, PQ20 or PQ30 has failed.

## Maximum Network Data Transfer Rates

Network Interface	Controller Card	MSa/s Note 1,2,3		MB/s (Maximum) Note 1,2,3
		16-bit	24-bit	
Ethernet (100 Mbit/s)	PQ12	2.5	1.6	5.0
	PQ20	3.6	2.4	7.2
Ethernet (1000 Mbit/s)	PQ30	19.6	13.1	39.3
Wireless LAN (802.11 b)	PQ12/PQ20	0.4	0.2	0.7

Note 1: MSa/s = 1 000 000 samples per second and MB/s = 1 MBytes per second

Note 2: These values are an indication only and may differ depending on the number and type of Modules, the network setup, and the specifications of the host PC used in the measurements.

Note 3: If PAK Software reports too high data rate, the PAK MKII is unable to transfer all the data before the internal buffers overflow.

# chapter four

## SyncLink Clusters and SuperClusters

### NOTE:

1. In a SuperCluster, all the SyncLink clock inputs of the PAK MKII systems must be from the same level of SL21. The unused SL21 (top level) outputs that provide the clock inputs of the second level SL21s may not be used to connect to additional PAK MKII systems.
2. The Master Sampling Rate (MSR) of all the PAK MKII systems in a SyncLink cluster must be the same. It cannot differ from PAK MKII to PAK MKII within the Cluster.

SyncLink takes the concept of modularity one step further by providing the means to group up to 4 Mainframes together to form a Cluster, up to 4 Clusters together to form a SuperCluster and so on. In this way a limitless number of Mainframes are grouped together providing a limitless channel count, greater geographic reach, improved cable management and reduced bottlenecks.

The SyncLink Cluster concept operates using a common clock transmitted over a single fiber-optic cable from an SL21 VMEbus board to a PQ12, PQ20 or PQ30 contained in slot 1 of each Mainframe. This cable follows the same routing path as the Ethernet cable used to transfer data to each Mainframe. A fiber-optic cable is used to ensure sub-50 ns timing resolution and immunity to outside electrical interference.

In order to simplify the routing of cables, the SL21 board contains a 5 port 1000 BASE-T Ethernet switch together with a 4 port fiber-optic SyncLink source and 1 port fiber-optic SyncLink receiver in a single VMEbus board. These ports allow Mainframes to be grouped together in units of 4 to form a Cluster. Only one SL21 board is required per Cluster and can be plugged into anyone of the Mainframes which form that Cluster.

This concept is scalable, since by simply adding an additional SL21 board, 4 Clusters can be linked together. As such 16 Mainframes will only need 5 SL21 boards. There is no limit to adding more Mainframes as long as the appropriate SL21 boards are added.

### DEALING WITH REMOTE MEASUREMENT SITUATIONS:

1. Clusters allow a distribution of Mainframes to reach remotely placed sensors
2. Measurements within one Cluster can be spread over a large area with a 1000 m radius
3. Measurements within one SuperCluster can be spread over a large area with a 2000 m radius

# getting to know the PAK MKII

## ADVANTAGES OF CLUSTERS AND SUPERCLUSTERS

1. SyncLink fiber-optic cable and SyncLink hub mimics Ethernet's CAT5E cable and switch, providing identical routing paths for both cables
2. Channel count is increased. A 10-slot Mainframe can have 128\* channels, a Cluster of 4 Mainframes 496\*, a SuperCluster of 16 Mainframes 1968\*. There is no Master/Slave limitation. (\*Calculated on an average of 4 channels per Module in an MF10 Mainframe)
3. Clusters and SuperClusters have the benefit of shorter signal cables contributing to lower cabling costs, reduced cable noise, reduced cabling faults and improved cabling management
4. SyncLink optimizes measurement infrastructure and cost as multiple small systems can be used separately in some applications but also together for larger tests

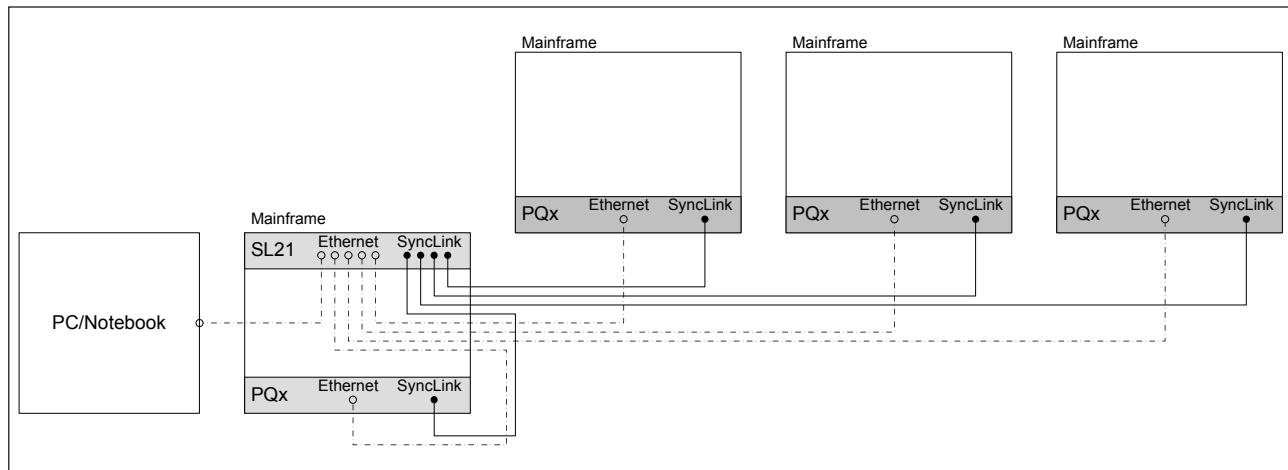
## OPTICAL FIBER CABLE

1. Simplex Jumper, Multi mode 50/125 um, 3.0 mm Jacketed Cable, Riser Rated, 10 m length
2. End 1: SC Connector, Standard PC + Polish, Straight Boot, standard color
3. End 2: SC Connector, Standard PC + Polish, Straight Boot, standard color

## NOTE:

1. 1000 m is suggested as the maximum optical fiber cable length between SyncLink transmitter and receiver.
2. It is required that all optical fiber cables in a SyncLink Cluster have the same length.
3. The Master Sampling Rate (MSR) must be the same for all the PAK MKII systems in the SyncLink Cluster.

## A SyncLink Cluster with an SL21 and PQ12/PQ20/PQ30 Controller:



# chapter four

## SyncLink Board SL21

The SyncLink (SL) Board transmits the SyncLink synchronization clock to all PAK MKII systems that are part of the SyncLink Cluster. The SL21 has an additional optical fiber input which effectively allows the SyncLink Cluster (entity) to be clustered and thus forming a SuperCluster where a limitless number of PAK MKII's can be connected together. Each SyncLink cluster needs only one SL21 which can be inserted into any of the PAK MKII VME slots in the Cluster.

### NOTE:

- Only one SL board is required per SyncLink Cluster.
- The SL board can be inserted into any Mainframe slot normally used for an SC4x card

### SL21 FRONT PANEL

5 port Gigabit Ethernet switch containing:

- 1 port on the far left which is connected to the Workstation or to another SL21 at a higher level
- 4 ports to the right which service the 4 Mainframes in the Cluster or another 4 SL21 boards in a SuperCluster

5 port SyncLink hub containing:

- 1 port fiber-optic SyncLink receiver which is the port on the far right and which is left open if there is only one Cluster or in the case of a SuperCluster is connected to another SL21 at a higher level
- 4 port fiber-optic SyncLink source which provides the SyncLink signal to the 4 Mainframes in the Cluster or to 4 further SL21 boards in a SuperCluster

1 SL21 board is required per Cluster and can be inserted into any of the 4 Mainframes forming the Cluster. It can also be inserted into its own Mainframe. Only 1 additional SL21 board is required for a SuperCluster of up to 4 Clusters (or up to 16 Mainframes)



SL21 front panel

# getting to know the PAK MKII

## SyncLink Gigabit Ethernet

Although one Ethernet port is marked as 'U' to indicate 'Upload to PC', any of the 5 ports may be used for the connection between the SL21 and a PC or notebook. The front panel is marked only to facilitate with cable configuration.

### SL21 Gigabit Ethernet features:

1. Full-duplex 10/100/1000 Mbit/s connection with auto-negotiation
2. Auto crossover detection (auto-MDI/MDIX)
3. 2 status LEDs on the RJ45 connector of the port which indicates if the Ethernet link is up: Green indicates a 100 Mbit/s connection and amber (orange) a Gigabit connection

The routing of the Ethernet signal of the PAK MKII to which the SL21 is fitted is not done internally and therefore an Ethernet cable must be externally connected from the PAK MKII's normal Ethernet output to one of the SL21 Ethernet ports.

### NOTE:

- The Ethernet cable should not be shorter than 30 cm.

# chapter four

## Signal Conditioning Boards SC4x

The SC4x VMEbus board provides the isolated power, signal processing and mechanical infrastructure for up to 4 Modules.

The board has 5 powerful 24-bit DSPs to process large volumes of data transferred between the VMEbus and each Module. 4 DSPs are dedicated to the specific Module slots and the 5th DSP is for administration and hosting tasks. The DSPs are used for anti-aliasing, smoothing, decimation, interpolation, digital filtering, event processing, etc.

The SC4x provides isolated power for each Module, a DC accurate calibration engine used to calibrate each Module, sample timing infrastructure as well as internal communication interfaces used to set parameters for each channel.

48

Additionally the SC4x provides the flexibility of easy interchangeability of Modules within the same Mainframe or other Mainframes. This empowers Users to configure their PAK MKII measurement system to satisfy their measurement and control requirements. Modules are plugged in through the front panel of the SC4x and can be inserted and removed without removing the SC4x board itself.

### NOTE:

The self-calibration procedure is handled by the PAK software. It is recommended that the self-calibration should be executed at the operating temperature of the PAK MKII. Do not reset your PAK MKII while it is calibrating.

### SELF CALIBRATION

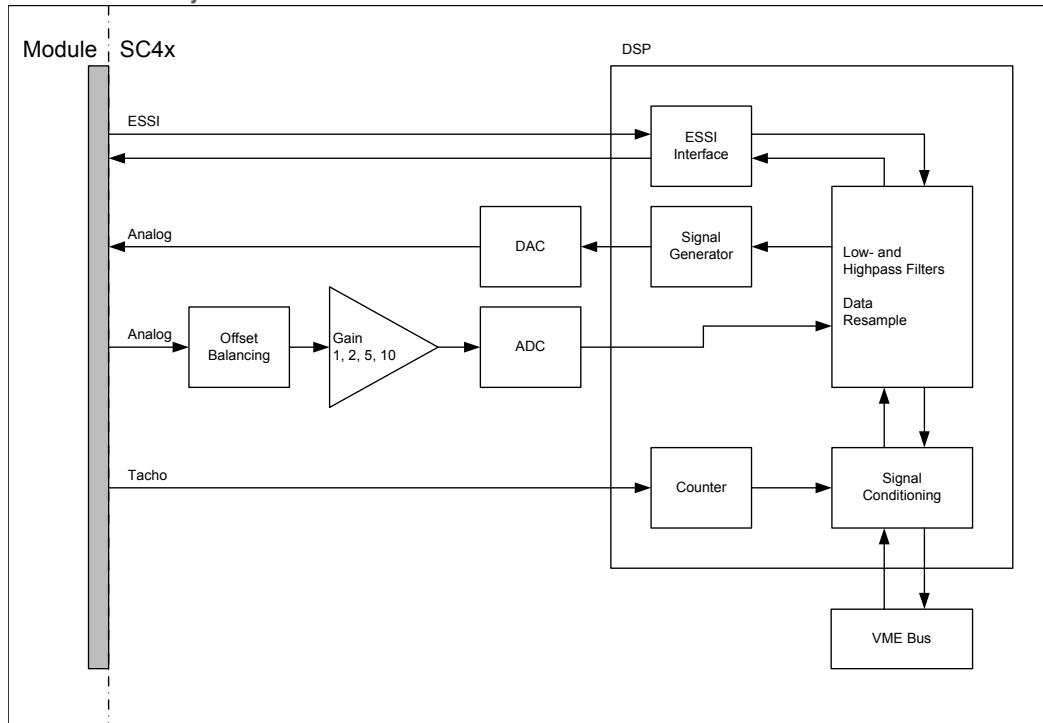
Each PAK MKII is fitted with a self calibration feature. Each SC4x has accurate internal references and DACs that are used to generate calibration signals which are switched into the front end of each channel. Calibration values are written into non-volatile system memory which expires automatically with hardware changes or firmware upgrades.

# getting to know the PAK MKII

## SC4X SIGNAL CONDITIONING AND ANALOG-TO-DIGITAL CONVERSION

The Module slot connector forms the interface by which various types of data and control signals are passed between the Module and SC4x. The figures in the following sections detailing each Module will show the signal path from where it enters the Module at the front panel until the final sample value is available.

### SC4x functionality



The available functionality on the SC4x per Module slot which can be summarized as:

1. Analog offset balancing
2. Analog programmable gain amplifier
3. 16-bit analog-to-digital converter
4. 16-bit digital-to-analog converter
5. Digital signal processing (DSP)

The DSP provides the following functionality:

6. Digital low- and high pass filters
7. Signal conditioning

8. Data resampler
9. Counter with data compression
10. ESSI (enhanced synchronous serial interface) for high-speed serial communication with certain Modules
11. Gain, offset and phase corrections

For all Modules that do not contain an onboard ADC the effective sampling rate per channel is determined by the 16-bit ADC located on the SC4x in combination with the SC4x card's digital data resampler.

For all Modules that do have an onboard

ADC (e.g. ICP42) the effective sampling rate per channel is determined by the ADC located on the Module in combination with the SC4x card's digital data resampler.

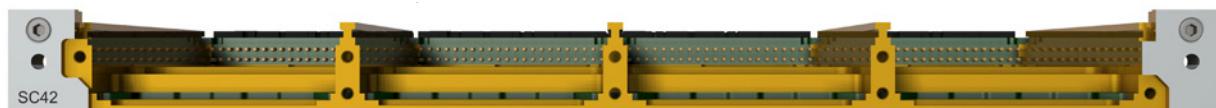
The Module-SC4x interface shows the different formats in which a data signal may be passed from a Module to the SC4x. The types are:

- Analog
- Tacho (Tacho input signal from an ICT Module)
- ESSI (e.g. ICP42)

# chapter four

## SC42

The SC42 board is a VMEbus Signal Conditioning Engine and Infrastructure suitable for all Mainframes and Modules. In 24 bit mode it provides a sampling rate of 102.4 kSa/s per channel for a 4 channel Module or 204.8 kSa/s per channel for a 2-channel Module (e.g. MIC42X). In 16 bit mode, a sampling rate of 204.8 kSa/s per channel for a 4 channel Module is provided.



SC42 front panel

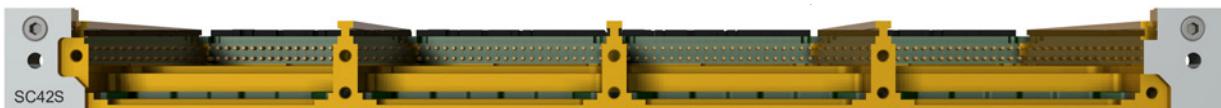
### FEATURES:

1. VMEbus Slave and Interrupter
2. Mechanics to accommodate 4 Modules
3. Provides accurate timing infrastructure for 4 Modules
4. 5 separate 24 bit DSPs, one per Module and one on the board
5. 4 isolated power supplies, one per Module
6. Houses the Module's auto calibration engine
7. Thermally optimized and encased in aluminum

# getting to know the PAK MKII

The SC42S board is a VMEbus Signal Conditioning Engine and Infrastructure suitable for all Mainframes and 42 series Modules but especially suited for the S-series Modules. In 24 bit mode it provides a sampling rate of 204.8 kSa/s per channel for a 4 channel Module. It is intended to be used with the PQ30 Controller for high-speed multi-channel measurements.

## SC42S



SC42S front panel

### FEATURES:

1. VMEbus Slave and Interrupter
2. Mechanics to accommodate 4 Modules
3. Provides accurate timing infrastructure for 4 Modules
4. 5 separate 24 bit DSPs, one per Module and one on the board
5. 4 isolated power supplies, one per Module
6. Houses the Module's auto calibration engine
7. Thermally optimized and encased in aluminum

### NOTE:

Only 42 series components will work with an SC42S.

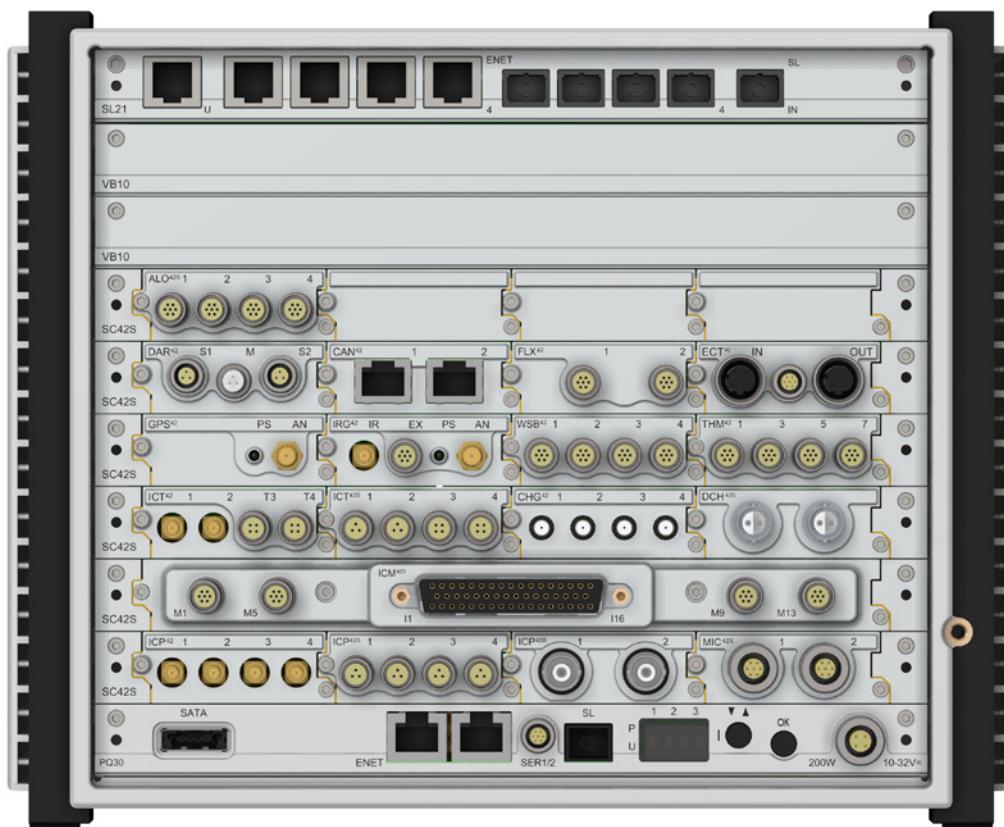
# chapter four

## Modules

As VMEbus boards are too large to provide a sufficient variety of signal conditioning amplifiers in a single Mainframe, a Sub-VMEbus conceptual tier exists where 4 Modules can be inserted into the front panel of an SC4x VMEbus board.

All Modules can easily be inserted and extracted through the front panel of the SC4x allowing the User complete freedom to configure the measurement system for a particular test. Typically each Module contains 4 channels (some may contain 1, 2 or 8).

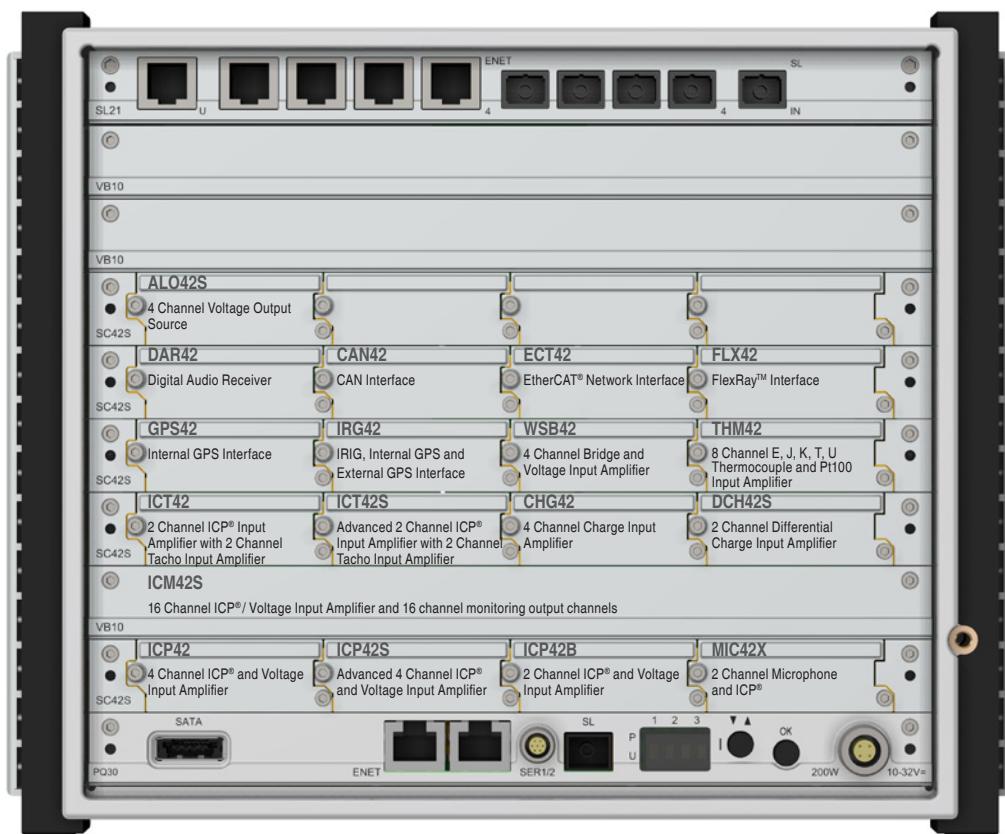
MF10 populated with the current range of Modules



# getting to know the PAK MKII

Modules are innovatively packaged in an aluminum casing so as to optimize both size and thermal performance. Most Modules are galvanically isolated allowing a 50 V difference between the ground potential of the Module and that of the Mainframe.

## Modules



# chapter four

## ICP Module

## 4 Channel Analog/ICP® Input

### WARNING:

Ensure that an analog sensor is never connected to any ICP® channel set to measure an ICP® signal (ICP® mode). In this mode, a 4 mA current may flow into the analog sensor and inflict damage to it. Note that a change made to the ICP® channel's mode in the graphical User interface will only change on the Module itself when a measurement is started.

### DESCRIPTION

The ICP Module provides 4 input channels for measuring analog or ICP® signals. The ICP® interface of the Module is compatible with an ICP® transducer, commonly used to measure acceleration, force and pressure. These transducers are popular due to their relaxed cable requirements.

The following Module interface modes exist (can be selected per channel):

1. *ICP® mode*: ICP® interface for connecting to ICP® sensors; a 4 mA constant excitation current is provided via the channel input
2. *AI mode* (Analog Input mode): Typical analog interface allowing the measurement of analog signals that fall within the supported voltage and frequency ranges

### TYPES

Three ICP Module types exist, these being:

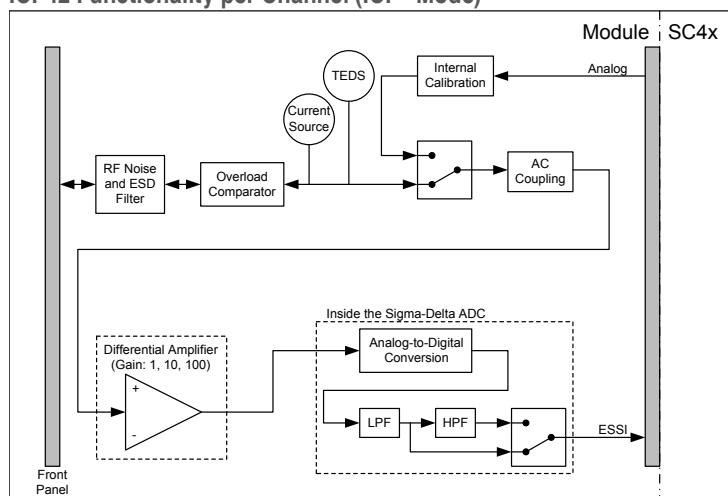
1. ICP42 with a 24-bit ADC and the following sampling limits:
  - $\leq 102.4$  kHz / channel for all four channels
2. ICP42B with a 24-bit ADC and the following sampling limits:
  - $\leq 204.8$  kHz / channel for two channels
3. ICP42S with a 24-bit ADC and the following sampling limits:
  - $\leq 204.8$  kHz / channel for four channels (SC4x dependant)

# getting to know the PAK MKII

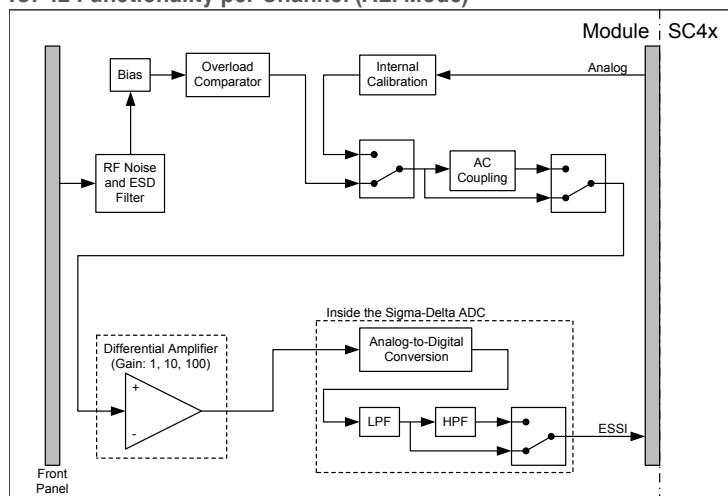


ICP42

## ICP42 Functionality per Channel (ICP® Mode)



## ICP42 Functionality per Channel (ALI Mode)

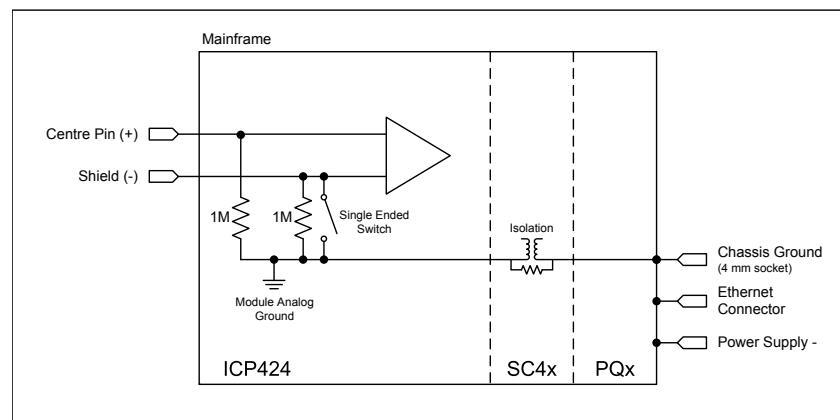


# chapter four

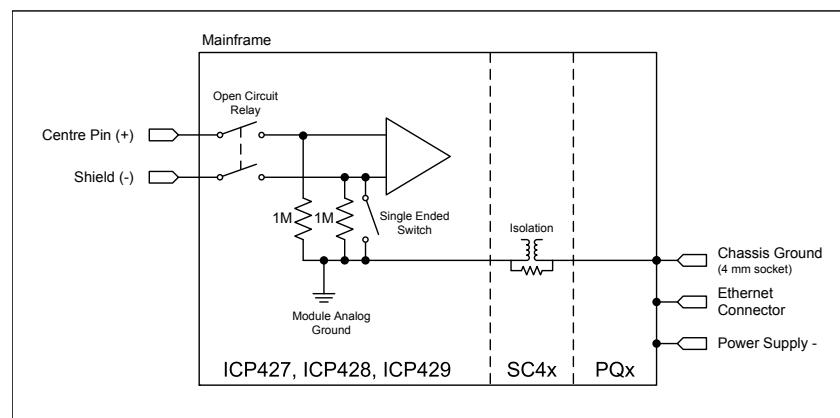
## ICP42 continued

### ICP42 GROUNDING DIAGRAMS: ALI MODE (VOLTAGE INPUT MODE)

ICP424 Grounding Diagram (ALI Mode)



ICP427, ICP428, ICP429 Grounding Diagram (ALI Mode)

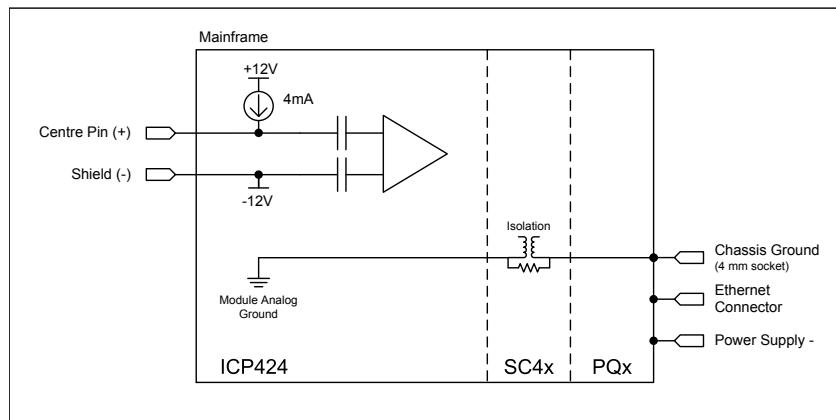


PAK Ground Setting (ALI Mode)	Single-Ended Switch
Module Ground	Closed
Differential	Open

# getting to know the PAK MKII

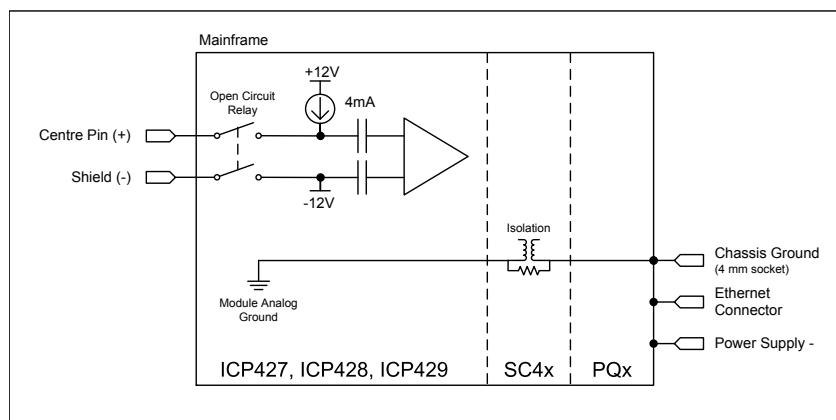
## ICP42 GROUNDING DIAGRAMS: ICP® INPUT MODE

ICP424 Grounding Diagram (ICP® Input Mode)



**ICP42**  
continued

ICP427, ICP428, ICP429 Grounding Diagram (ICP® Input Mode)



# chapter four

## ICP42 Specifications

### DC and AC Accuracy

Function	Range	Input Voltage	Error Specification ( $\pm$ % of range) $T_A = 23^\circ\text{C} \pm 5^\circ\text{C}$
DC Voltage	100 mV	100 mV	0.529
	1.0 V	1.0 V	0.086
	10.0 V	10.0 V	0.096
AC Voltage	100 mV	100 mV	0.593
	1.0 V	1.0 V	0.148
	10.0 V	10.0 V	0.143

Conditions:

- Within 30 minutes after “self calibration”
- Following the required 1 hour warm-up period of the PAK MKII
- Module Temperature of  $55^\circ\text{C} \pm 7^\circ\text{C}$
- $T_A$  : ambient temperature
- 90 Day Specifications of the Agilent 34410A are used

### UNDERSTANDING THE % OF RANGE ERROR

The range error compensates for inaccuracies that result from the function and range the User selects. Example: Consider an input signal of  $5 \text{ V}_{\text{DC}}$  in the 10 V range. The  $5 \text{ V}_{\text{DC}}$  signal would be measured in the 10V range.

$$\text{Error} = \pm 0.096 \% \times 10.0 = \pm 9.6 \text{ mV}$$

# getting to know the PAK MKII

## ICP42 Specifications continued

### Excitation

Function	Minimum	Maximum	Unit
Excitation Voltage	22.00	24.00	V
Constant Current	3.92	4.18	mA

Conditions:

- Within 30 minutes after “self calibration”
- Following the required 1 hour warm-up period of the PAK MKII
- Module Temperature of  $55^{\circ}\text{C} \pm 7^{\circ}\text{C}$
- $T_A$  : ambient temperature
- 90 Day Specifications of the Agilent 34410A are used

### Bandwidth Specifications

The published attenuation values include the errors made during the measurement (DMM measurement errors) as well as errors made with the RMS calculation and represents the attenuation relative to the input voltage.

#### Bandwidth Specifications for a 102400 Hz Sampling Rate

Passband characteristics ( $f_s = 102400$ Hz)					
Parameter	Frequency (Hz)	Frequency Specification (Hz)		Attenuation (dB) $T_A = 23^{\circ}\text{C} \pm 5^{\circ}\text{C}$	
		Min	Max	Min	Max
Passband	100	-	100.01	-	0.018
	1000	-	1000.05	-	0.018
	25500	-	25502	-	0.030
	46600	-	46603	-	0.050
	47500	-	47503	-	0.110
	50150	-	50153	-	2.800
	53000	53000	-	16.900	-

# chapter four

## ICP42 Specifications continued

### Bandwidth Specification for a 51200 Hz Sampling Rate

Passband characteristics (fs = 51200 Hz)					
Parameter	Frequency (Hz)	Frequency Specification (Hz)		Attenuation (dB)	
		Min	Max	Min	Max
Passband	100	-	100.02	-	0.018
	1000	-	1000.05	-	0.018
	22900	-	22901	-	0.030
	23600	-	23601	-	0.062
	24600	-	24601	-	1.020
	25080	-	25081	-	2.700
	26500	26500	-	17.000	-

Conditions:

- Within 30 minutes after “self calibration”
- Following the required 1 hour warm-up period of the PAK MKII
- Module Temperature of  $55^{\circ}\text{C} \pm 7^{\circ}\text{C}$
- $T_A$  : ambient temperature
- 90 Day Specifications of the Agilent 34410A are used

# getting to know the PAK MKII

## ICP42 Features

Parameter	Mode	Value			
Module Connector	-	SMB Male			
Channels	-	4 input			
Interface	ICP®	For ICP® sensors, 4 mA excitation, 22 V span			
	ALI	For analog source voltages			
Input Coupling Note 12	ICP®	AC			
	ALI	DC or AC			
AC Coupling Frequency Response (first order response)	ICP® / ALI	Attenuation	Min	Max	Unit
		-3 dB	-	0.25	Hz
Input Bias	ICP®	Differential			
	ALI	Differential, single-ended to Module Ground (isolated) or single-ended to Chassis Ground (non-isolated)			
Input Voltage Range	ICP® / ALI	$\pm 10\text{ V}$ , $\pm 1.0\text{ V}$ , $\pm 100\text{ mV}$			
Input Impedance	ALI	$2\text{ M}\Omega \parallel 2.2\text{ nF}$ (Differential) $1\text{ M}\Omega \parallel 2.2\text{ nF}$ (Single Ended)			
DC Offset Note 2, 9	ICP® / ALI	$11\text{ }\mu\text{V}$ ( $\pm 10\text{ V}$ ), $1\text{ }\mu\text{V}$ ( $\pm 1.0\text{ V}$ ), $0.2\text{ }\mu\text{V}$ ( $\pm 100\text{ mV}$ )			
Maximum Sampling Rate per Channel (fs)	ICP® / ALI	102.4 kHz			
Other Sampling Rates	-	Available through digital LP filters and decimation			
Onboard ADC	-	4 x sigma-delta			
Resolution	-	16/24-bit			
Digital HP Filter Note 1	-	$-3\text{ dB}$ at 1 Hz, $-0.1\text{ dB}$ at 6.5 Hz ( $fs \leq 48\text{ kHz}$ ), $-3\text{ dB}$ at 2 Hz, $-0.1\text{ dB}$ at 13 Hz ( $fs = 96\text{ kHz}$ ) Filter scales with sampling rate			
Digital LP Filter Note 1	-	Passband = $0.45 * fs$ Stopband = $0.55 * fs$ Passband ripple = $\pm 0.001\text{ dB}$ ( $fs \leq 48\text{ kHz}$ ), $\pm 0.003\text{ dB}$ ( $fs = 96\text{ kHz}$ ) Stopband attenuation = 110 dB ( $fs \geq 48\text{ kHz}$ ) Stopband attenuation = 80 dB ( $fs < 48\text{ kHz}$ )			

# chapter four

## ICP42 Features continued

Parameter	Mode	Value
<b>Optional Programmable Digital IIR Filter</b>	-	Band pass/stop : 6 dB/octave High/Low pass: 12 dB/octave
<b>SNR</b> (fs = 48 kHz) Note 2, 3, 9	ALI	136 dB ( $\pm 10$ V), 135 dB ( $\pm 1.0$ V), 130 dB ( $\pm 100$ mV)
<b>THD</b> (fs = 48 kHz) Note 2, 4, 9	ALI	104 dB ( $\pm 10$ V), 106 dB ( $\pm 1.0$ V), 100 dB ( $\pm 100$ mV)
<b>SFDR<sub>IV</sub></b> (fs = 48 kHz) Note 2, 5, 9, 10	ALI	115 dB ( $\pm 10$ V), 133 dB ( $\pm 1.0$ V), 136 dB ( $\pm 100$ mV)
	ICP®	114 dB ( $\pm 10$ V), 133 dB ( $\pm 1.0$ V), 146 dB ( $\pm 100$ mV)
<b>SFDR<sub>10V</sub></b> (fs = 48 kHz) Note 2, 5, 9, 11	ALI	135 dB ( $\pm 10$ V), 153 dB ( $\pm 1.0$ V), 156 dB ( $\pm 100$ mV)
	ICP®	134 dB ( $\pm 10$ V), 153 dB ( $\pm 1.0$ V), 166 dB ( $\pm 100$ mV)
<b>SFDR<sub>H</sub></b> (fs = 48 kHz) Note 2, 6, 9, 10	ALI	114 dB ( $\pm 10$ V), 118 dB ( $\pm 1.0$ V), 106 dB ( $\pm 100$ mV)
<b>Crosstalk</b> (fs = 48 kHz) Note 2, 7, 9	ALI	133 dB ( $\pm 10$ V), 131 dB ( $\pm 1.0$ V), 110 dB ( $\pm 100$ mV)
<b>Noise Floor</b> (fs = 48 kHz) Note 2, 8, 9, 10	ALI	-128 dB ( $\pm 10$ V), -146 dB ( $\pm 1.0$ V), -157 dB ( $\pm 100$ mV)
<b>Phase Accuracy</b>	-	< 0.2 ° at 10 kHz
<b>Overflow Detection</b>	-	Analog window comparators
<b>Module Calibration</b>	-	Internal amplitude and phase calibration
<b>Protection</b>	ICP® / ALI	2 kV ESD
	ICP®	Short circuit between sensor case and ground
<b>Galvanic Isolation</b>	-	50 V
<b>TEDS</b>	-	Support for IEEE 1451.4 Class 1

The different modes and parameter values mentioned in the features table are all software-selectable.

**Note 1:** Digital filters form part of the onboard ADC. Channels 1 and 2 are converted by the 2-channel sigma-delta ADC and thus share the same HP and LP filter setup. The same is true for channels 3 and 4.

# getting to know the PAK MKII

## ICP42 Features continued

Note 2: Measured after Module auto calibration has been applied.

Note 3: Signal to Noise Ratio (SNR): The ratio of the rms signal amplitude to the rms noise value excluding harmonics. Input signals are 7.5 V<sub>amplitude</sub> ( $\pm 10$  V Range), 750 mV<sub>amplitude</sub> ( $\pm 1$  V Range) and 75 mV<sub>amplitude</sub> ( $\pm 100$  mV Range) @ 1 kHz.

Note 4: Total Harmonic Distortion (THD): The ratio of the root-sum-squares of the first 10 harmonic amplitudes to the fundamental signal amplitude. Input signals are 7.5 V<sub>amplitude</sub> ( $\pm 10$  V Range), 750 mV<sub>amplitude</sub> ( $\pm 1$  V Range) and 75 mV<sub>amplitude</sub> ( $\pm 100$  mV Range) @ 1 kHz.

Note 5: Spurious Free Dynamic Range (SFDR): The ratio of the full scale input to the amplitude of the largest spurious spectral component (Inputs terminated with a short circuit. Measurement bandwidth: 100 Hz to  $f_s / 2$  excluding harmonics).

Note 6: Spurious Free Dynamic Range (SFDR<sub>H</sub>): The ratio of the fundamental signal amplitude to the amplitude of the highest peak including the first and all other harmonics. Measurement bandwidth: 100 Hz to  $f_s / 2$ . Input signals are 7.5 V<sub>amplitude</sub> ( $\pm 10$  V Range), 750 mV<sub>amplitude</sub> ( $\pm 1$  V Range) and 75 mV<sub>amplitude</sub> ( $\pm 100$  mV Range) @ 1 kHz.

Note 7: Crosstalk: Signal is played into a channel while the remaining channels are short circuited. The crosstalk is the ratio of the fundamental signal amplitude of the input channel to the signal amplitude at the fundamental frequency on the remaining channels. Input signals are 7.5 V<sub>amplitude</sub> ( $\pm 10$  V Range), 750 mV<sub>amplitude</sub> ( $\pm 1$  V Range) and 75 mV<sub>amplitude</sub> ( $\pm 100$  mV Range) @ 1 kHz.

Note 8: Noise Floor: The rms noise value specified in dB when the inputs are terminated with a short circuit.

Note 9: Listed values are typical measurement values.

Note 10: 0 dB is equal to 1 V.

Note 11: 0 dB is equal to 10 V.

Note 12: ICP® mode is AC coupled in hardware by default.

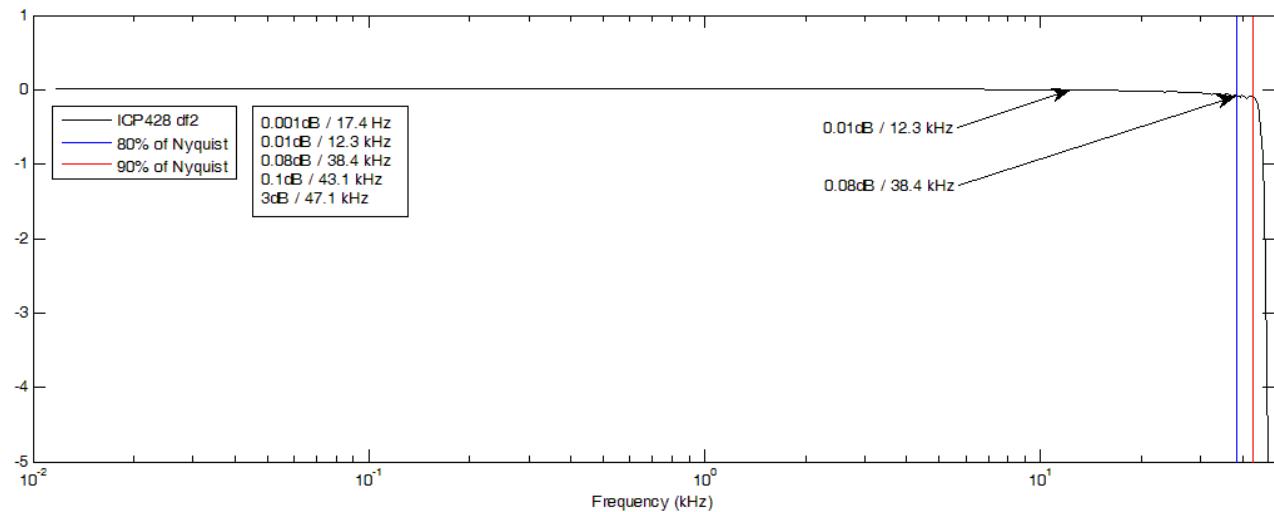
## ICP42 Connector Pin Definition

Connector	Polarity
Center Pin	Signal +
Shield	Signal -

# chapter four

## ICP42 Features continued

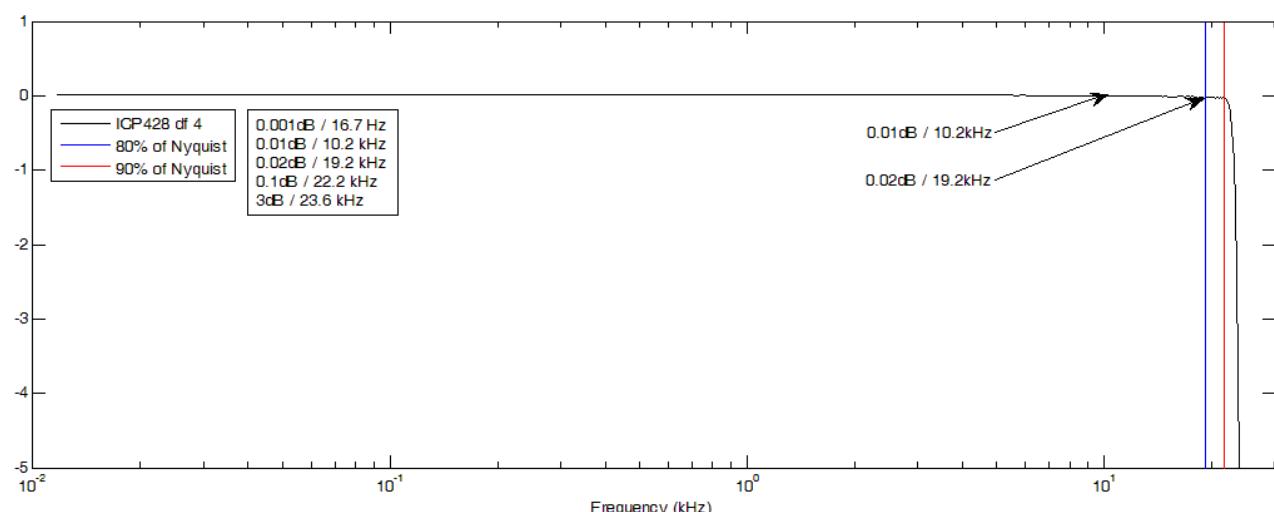
### Frequency Response Analysis



#### Notes:

Nyquist frequency is 48 kHz

0 dB equals 7.5 Vpp



#### Notes:

Nyquist frequency is 24 kHz

0 dB equals 7.5 Vpp

# getting to know the PAK MKII



**ICP42B**

## DESCRIPTION

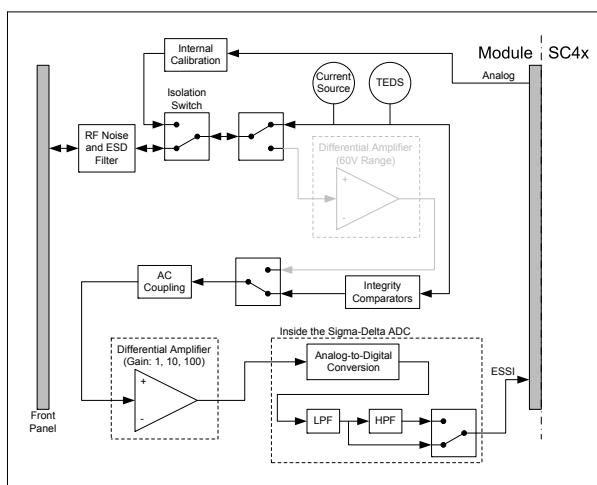
The ICP42B Module is a 2 channel BNC connector version of the ICP42 Module. This Module supports  $\pm 60$  V input signal and sampling rates up to 204.8 kSa/s. Both channels operate independently from each other, each with its own software configurable settings.

The Module is used with any ICP® based sensor commonly used to measure acceleration, force or pressure and with any voltage source up to  $\pm 60$  V.

## FEATURES

- All ICP42 features plus 204.8 kSa/s sampling rate and 60 V input range
- BNC connectors

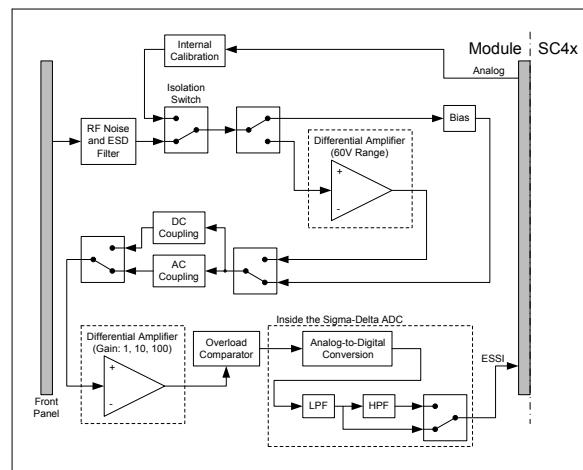
## ICP42B Functionality per Channel (ICP® Mode)



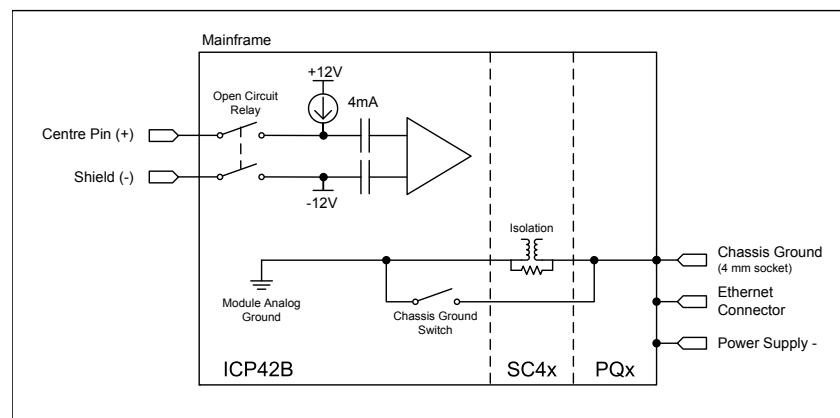
# chapter four

## ICP42B continued

ICP42B Functionality per Channel (ALI Mode)



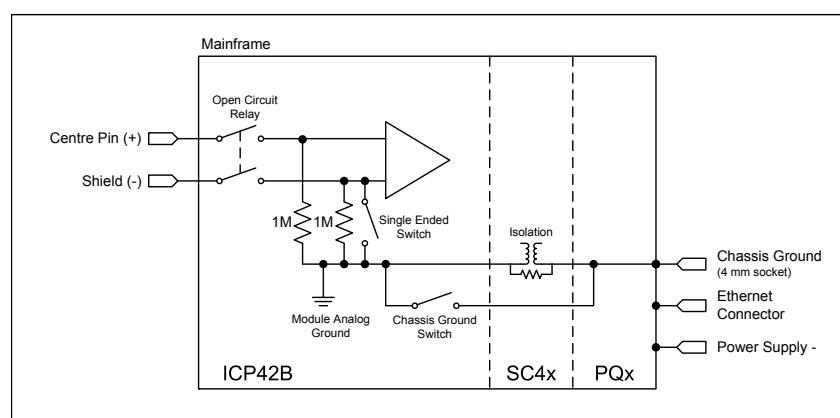
ICP42B Grounding Diagram (ICP® Input Mode)



### NOTE:

Please refer to ICP42S for PAK grounding settings.

ICP42B Grounding Diagram (ALI Mode)



# getting to know the PAK MKII

## ICP42B Specifications

### DC and AC Accuracy

Function	Range	Input Voltage	Error Specification ( $\pm$ % of range)
			$T_A = 23^\circ\text{C} \pm 5^\circ\text{C}$
DC Voltage	100 mV	100 mV	0.529
	1.0 V	1.0 V	0.086
	10.0 V	10.0 V	0.096
AC Voltage	100 mV	100 mV	0.593
	1.0 V	1.0 V	0.148
	10.0 V	10.0 V	0.143

Conditions:

- Within 30 minutes after “self calibration”
- Following the required 1 hour warm-up period of the PAK MKII
- Module Temperature of  $55^\circ\text{C} \pm 7^\circ\text{C}$
- $T_A$  : ambient temperature
- 90 Day Specifications of the Agilent 34410A are used

## UNDERSTANDING THE % OF RANGE ERROR

The range error compensates for inaccuracies that result from the function and range the User selects. Example: Consider an input signal of  $5 \text{ V}_{\text{DC}}$  in the 10 V range. The  $5 \text{ V}_{\text{DC}}$  signal would be measured in the 10V range.

$$\text{Error} = \pm 0.096 \% \times 10.0 = \pm 9.6 \text{ mV}$$

# chapter four

## ICP42B Specifications continued

### Excitation

Function	Minimum	Maximum	Unit
Excitation Voltage	22.00	24.00	V
Constant Current	3.92	4.18	mA

Conditions:

- Within 30 minutes after “self calibration”
- Following the required 1 hour warm-up period of the PAK MKII
- Module Temperature of  $55^{\circ}\text{C} \pm 7^{\circ}\text{C}$
- $T_A$  : ambient temperature
- 90 Day Specifications of the Agilent 34410A are used

### Bandwidth Specifications

The published attenuation values include the errors made during the measurement (DMM measurement errors) as well as errors made with the RMS calculation and represents the attenuation relative to the input voltage.

#### Bandwidth Specifications for a 102400 Hz Sampling Rate

Passband characteristics (fs = 102400 Hz)						
Parameter	Frequency (Hz)	Frequency Specification (Hz)		Attenuation (dB)		$T_A = 23^{\circ}\text{C} \pm 5^{\circ}\text{C}$
		Min	Max	Min	Max	
Passband	100	-	100.01	-	0.018	
	1000	-	1000.05	-	0.018	
	25500	-	25502	-	0.030	
	46600	-	46603	-	0.050	
	47500	-	47503	-	0.110	
	50150	-	50153	-	2.800	
	53000	53000	-	16.900	-	

# getting to know the PAK MKII

## ICP42B Specifications continued

### Bandwidth Specification for a 51200 Hz Sampling Rate

Passband characteristics ( $f_s = 51200$ Hz)					
Parameter	Frequency (Hz)	Frequency Specification (Hz)		Attenuation (dB) $T_A = 23^\circ\text{C} \pm 5^\circ\text{C}$	
		Min	Max	Min	Max
Passband	100	-	100.02	-	0.018
	1000	-	1000.05	-	0.018
	22900	-	22901	-	0.030
	23600	-	23601	-	0.062
	24600	-	24601	-	1.020
	25080	-	25081	-	2.700
	26500	26500	-	17.000	-

Conditions:

- Within 30 minutes after “self calibration”
- Following the required 1 hour warm-up period of the PAK MKII
- Module Temperature of  $55^\circ\text{C} \pm 7^\circ\text{C}$
- $T_A$  : ambient temperature
- 90 Day Specifications of the Agilent 34410A are used

# chapter four

## ICP42B Features

Parameter	Mode	Value			
Module Connector	-	BNC			
Channels	-	2 input			
Interface	ICP®	For ICP® sensors, 4 mA excitation, 22 V span			
	ALI	For analog source voltages			
Input Coupling Note 12	ICP®	AC			
	ALI	DC or AC			
AC Coupling Frequency Response (first order response)	ICP® / ALI	Attenuation	Min	Max	Unit
		-3 dB	-	0.25	Hz
Input Bias	ICP®	Differential			
	ALI	Differential, single-ended to Module Ground (isolated) or single-ended to Chassis Ground (non-isolated)			
Input Voltage Range	-	$\pm 60$ V (only ALI mode), $\pm 10$ V, $\pm 1.0$ V, $\pm 100$ mV			
Input Impedance	-	$2 \text{ M}\Omega \parallel 300 \text{ pF}$ (Differential) ( $\pm 10$ V, $\pm 1.0$ V, $\pm 100$ mV) $1 \text{ M}\Omega \parallel 300 \text{ pF}$ (Single Ended) ( $\pm 10$ V, $\pm 1.0$ V, $\pm 100$ mV)			
DC Offset Note 2, 9	ICP® / ALI	130 $\mu$ V ( $\pm 60$ V), 11 $\mu$ V ( $\pm 10$ V), 1 $\mu$ V ( $\pm 1.0$ V), 0.2 $\mu$ V ( $\pm 100$ mV)			
Maximum Sampling Rate per Channel (fs)	-	204.8 kHz			
Other Sampling Rates	-	Available through digital LP filters and decimation			
Onboard ADC	-	2x Sigma-Delta			
Resolution	-	16/24-bit			
Digital HP Filter Note 1	-	$-3$ dB at 1 Hz, $-0.1$ dB at 6.5 Hz ( $fs \leq 48$ kHz), $-3$ dB at 2 Hz, $-0.1$ dB at 13 Hz ( $fs = 96$ kHz), $-3$ dB at 4 Hz, $-0.1$ dB at 26 Hz ( $fs = 192$ kHz) Filter scales with sampling rate			
Digital LP Filter Note 1	-	Passband = $0.45 * fs$ Stopband = $0.55 * fs$ Passband ripple = $\pm 0.005$ dB ( $fs \leq 48$ kHz), $\pm 0.005$ dB ( $fs = 96$ kHz), $\pm 0.005$ dB ( $fs = 192$ kHz) Stopband attenuation = 100 dB ( $fs \geq 48$ kHz) Stopband attenuation = 80 dB ( $fs < 48$ kHz)			

# getting to know the PAK MKII

## ICP42B Features continued

Parameter	Mode	Value
<b>Optional Programmable Digital IIR Filter</b>	-	Band pass/stop : 6 dB/octave High/Low pass: 12 dB/octave
<b>SNR</b> (fs = 48 kHz) Note 2, 3, 9	ALI	123 dB ( $\pm 60$ V), 136 dB ( $\pm 10$ V), 135 dB ( $\pm 1.0$ V), 130 dB ( $\pm 100$ mV)
<b>THD</b> (fs = 48 kHz) Note 2, 4, 9	ALI	96 dB ( $\pm 60$ V), 104 dB ( $\pm 10$ V), 106 dB ( $\pm 1.0$ V), 100 dB ( $\pm 100$ mV)
<b>SFDR<sub>IV</sub></b> (fs = 48 kHz) Note 2, 5, 9, 10	ALI	93 dB ( $\pm 60$ V), 115 dB ( $\pm 10$ V), 133 dB ( $\pm 1.0$ V), 136 dB ( $\pm 100$ mV)
	ICP®	114 dB ( $\pm 10$ V), 133 dB ( $\pm 1.0$ V), 146 dB ( $\pm 100$ mV)
<b>SFDR<sub>10V</sub></b> (fs = 48 kHz) Note 2, 5, 9, 11	ALI	113 dB ( $\pm 60$ V), 135 dB ( $\pm 10$ V), 153 dB ( $\pm 1.0$ V), 156 dB ( $\pm 100$ mV)
	ICP®	134 dB ( $\pm 10$ V), 153 dB ( $\pm 1.0$ V), 166 dB ( $\pm 100$ mV)
<b>SFDR<sub>H</sub></b> (fs = 48 kHz) Note 2, 6, 9, 10	ALI	101 dB ( $\pm 60$ V), 114 dB ( $\pm 10$ V), 118 dB ( $\pm 1.0$ V), 106 dB ( $\pm 100$ mV)
<b>Crosstalk</b> (fs = 48 kHz) Note 2, 7, 9	ALI	114 dB ( $\pm 60$ V), 133 dB ( $\pm 10$ V), 131 dB ( $\pm 1.0$ V), 110 dB ( $\pm 100$ mV)
<b>Noise Floor</b> (fs = 48 kHz) Note 2, 8, 9, 10	ALI	-106 dB ( $\pm 60$ V), -128 dB ( $\pm 10$ V), -146 dB ( $\pm 1.0$ V), -157 dB ( $\pm 100$ mV)
<b>Phase Accuracy</b>	-	< 0.2 ° at 10 kHz
<b>Overflow Detection</b>	-	Analog window comparators
<b>Module Calibration</b>	-	Internal amplitude and phase calibration
<b>Protection</b>	ALI / ICP®	2 kV ESD
	ICP®	Short circuit between sensor case and ground

# chapter four

## ICP42B Features continued

Parameter	Mode	Value
Galvanic Isolation	-	50 V
TEDS	-	Support for IEEE 1451.4 Class 1

The different modes and parameter values mentioned in the features table are all software-selectable.

Note 1: Digital filters form part of the onboard ADC.

Note 2: Measured after Module auto calibration has been applied.

Note 3: Signal to Noise Ratio (SNR): The ratio of the rms signal amplitude to the rms noise value excluding harmonics. Input signals are  $7.5 \text{ V}_{\text{amplitude}}$  ( $\pm 10 \text{ V}$  Range),  $750 \text{ mV}_{\text{amplitude}}$  ( $\pm 1 \text{ V}$  Range) and  $75 \text{ mV}_{\text{amplitude}}$  ( $\pm 100 \text{ mV}$  Range) @ 1 kHz.

Note 4: Total Harmonic Distortion (THD): The ratio of the root-sum-squares of the first 10 harmonic amplitudes to the fundamental signal amplitude. Input signals are  $7.5 \text{ V}_{\text{amplitude}}$  ( $\pm 10 \text{ V}$  Range),  $750 \text{ mV}_{\text{amplitude}}$  ( $\pm 1 \text{ V}$  Range) and  $75 \text{ mV}_{\text{amplitude}}$  ( $\pm 100 \text{ mV}$  Range) @ 1 kHz.

Note 5: Spurious Free Dynamic Range (SFDR): The ratio of the full scale input to the amplitude of the largest spurious spectral component (Inputs terminated with a short circuit. Measurement bandwidth: 100 Hz to  $f_s / 2$  excluding harmonics).

Note 6: Spurious Free Dynamic Range (SFDR<sub>H</sub>): The ratio of the fundamental signal amplitude to the amplitude of the highest peak including the first and all other harmonics. Measurement bandwidth: 100 Hz to  $f_s / 2$ . Input signals are  $7.5 \text{ V}_{\text{amplitude}}$  ( $\pm 10 \text{ V}$  Range),  $750 \text{ mV}_{\text{amplitude}}$  ( $\pm 1 \text{ V}$  Range) and  $75 \text{ mV}_{\text{amplitude}}$  ( $\pm 100 \text{ mV}$  Range) @ 1 kHz.

Note 7: Crosstalk: Signal is played into a channel while the remaining channels are short circuited. The crosstalk is the ratio of the fundamental signal amplitude of the input channel to the signal amplitude at the fundamental frequency on the remaining channels. Input signals are  $7.5 \text{ V}_{\text{amplitude}}$  ( $\pm 10 \text{ V}$  Range),  $750 \text{ mV}_{\text{amplitude}}$  ( $\pm 1 \text{ V}$  Range) and  $75 \text{ mV}_{\text{amplitude}}$  ( $\pm 100 \text{ mV}$  Range) @ 1 kHz.

Note 8: Noise Floor: The rms noise value specified in dB when the inputs are terminated with a short circuit.

Note 9: Listed values are typical measurement values.

Note 10: 0 dB is equal to 1 V.

Note 11: 0 dB is equal to 10 V.

Note 12: ICP® mode is AC coupled in hardware by default

## ICP42B Connector Pin Definition

Connector	Polarity
Center Pin	Signal +
Shield	Signal -

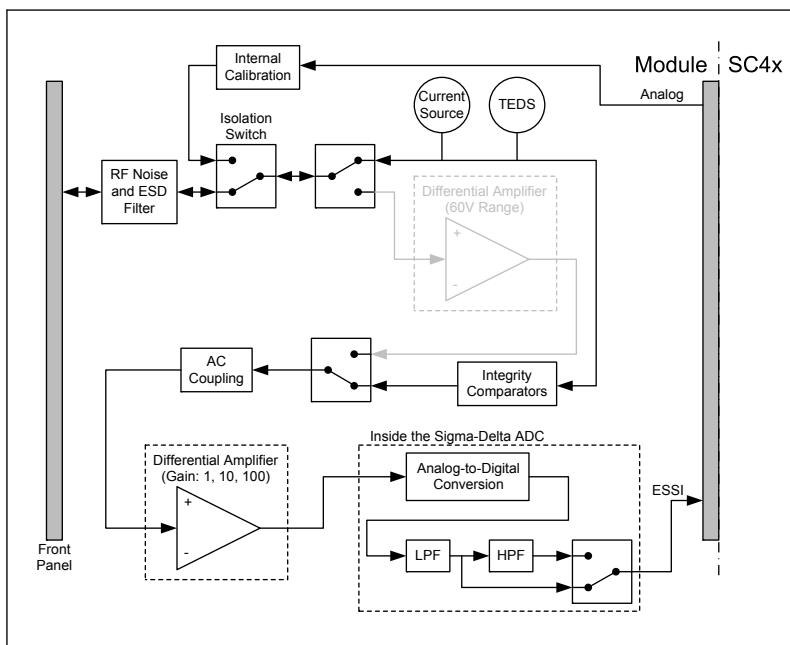
# getting to know the PAK MKII



**ICP42S**

ICP® integrity checking and overvoltage detection in ICP® and ALI mode is included with this module. When the module is in ICP® mode, the integrity checking is automatically activated. From the set limits the module will detect if the ICP sensor is working as expected and will inform the user if this is not the case. Overvoltage detection is always enabled and the module will inform the user of any overvoltage conditions that occur.

## ICP42S Functionality per Channel (ICP® Mode)



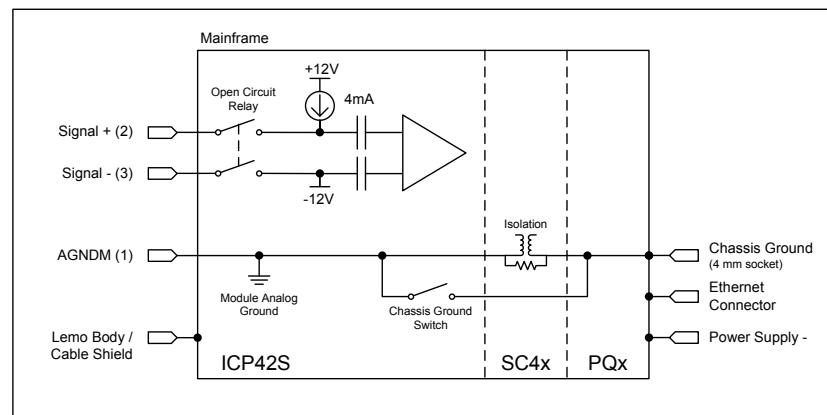
## NOTE:

No sample mode exists as channels 1 to 4 can each be sampled at the maximum sampling rate of 204.8 kHz.

# chapter four

## ICP42S continued

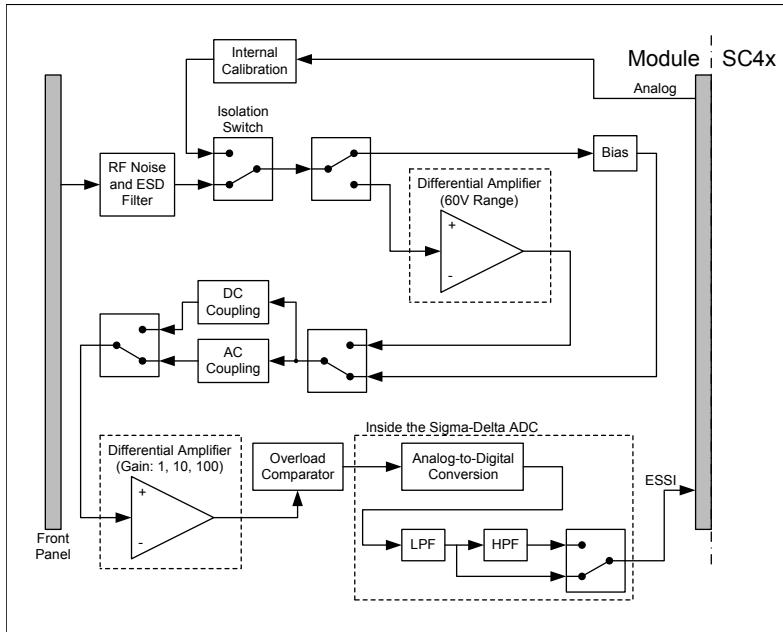
ICP42S Grounding Diagram (ICP® Input Mode)



PAK Ground Setting (ICP® Mode)	Chassis Ground Switch
Differential	Open
Diff. (Analog to System Ground)	Closed

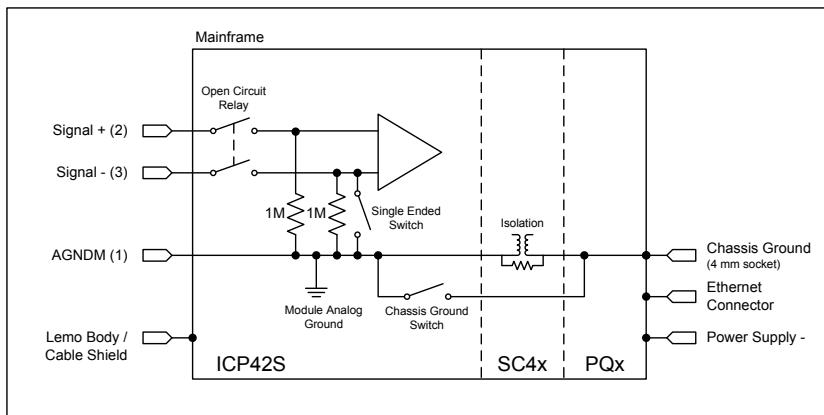
# getting to know the PAK MKII

## ICP42S Functionality per Channel (ALI Mode)



**ICP42S**  
continued

## ICP42S Grounding Diagram (ALI Mode)



PAK Ground Setting	Single-Ended Switch	Chassis Ground Switch
Module Ground	Closed	Open
Differential	Open	Open
System Ground	Closed	Closed
Diff. (Analog to System Ground)	Open	Closed

# chapter four

## ICP42S Specifications

### DC and AC Accuracy

Function	Range	Input Voltage	Error Specification ( $\pm$ % of range) $T_A = 23^\circ\text{C} \pm 5^\circ\text{C}$
DC Voltage	100 mV	100 mV	0.529
	1.0 V	1.0 V	0.086
	10.0 V	10.0 V	0.096
AC Voltage	100 mV	100 mV	0.593
	1.0 V	1.0 V	0.148
	10.0 V	10.0 V	0.143

Conditions:

- Within 30 minutes after “self calibration”
- Following the required 1 hour warm-up period of the PAK MKII
- Module Temperature of  $55^\circ\text{C} \pm 7^\circ\text{C}$
- $T_A$  : ambient temperature
- 90 Day Specifications of the Agilent 34410A are used

### UNDERSTANDING THE % OF RANGE ERROR

The range error compensates for inaccuracies that result from the function and range the User selects. Example: Consider an input signal of  $5 \text{ V}_{\text{DC}}$  in the 10 V range. The  $5 \text{ V}_{\text{DC}}$  signal would be measured in the 10V range.

$$\text{Error} = \pm 0.096 \% \times 10.0 = \pm 9.6 \text{ mV}$$

# getting to know the PAK MKII

## ICP42S Specifications continued

### Excitation

Function	Minimum	Maximum	Unit
Excitation Voltage	22.00	24.00	V
Constant Current	3.92	4.18	mA

Conditions:

- Within 30 minutes after “self calibration”
- Following the required 1 hour warm-up period of the PAK MKII
- Module Temperature of  $55^{\circ}\text{C} \pm 7^{\circ}\text{C}$
- $T_A$  : ambient temperature
- 90 Day Specifications of the Agilent 34410A are used

# chapter four

## ICP42S Specifications continued

### Bandwidth Specifications

The published attenuation values include the errors made during the measurement (DMM measurement errors) as well as errors made with the RMS calculation and represents the attenuation relative to the input voltage.

#### Bandwidth Specifications for a 204800 Hz Sampling Rate

Passband characteristics (fs = 204800 Hz)					
Parameter	Frequency (Hz)	Frequency Specification (Hz)		Attenuation (dB) $T_A = 23^\circ\text{C} \pm 5^\circ\text{C}$	
		Min	Max	Min	Max
Passband	100	-	100.01	-	0.018
	1000	-	1000.05	-	0.018
	51100	-	51103	-	0.094
	90000	-	90005	-	0.150
	95000	-	95005	-	0.234
	100500	-	100505	-	3.700
	106000	106000	-	14.500	-

#### Bandwidth Specifications for a 102400 Hz Sampling Rate

Passband characteristics (fs = 102400 Hz)					
Parameter	Frequency (Hz)	Frequency Specification (Hz)		Attenuation (dB) $T_A = 23^\circ\text{C} \pm 5^\circ\text{C}$	
		Min	Max	Min	Max
Passband	100	-	100.01	-	0.018
	1000	-	1000.05	-	0.018
	25500	-	25502	-	0.030
	46600	-	46603	-	0.050
	47500	-	47503	-	0.110
	50150	-	50153	-	2.800
	53000	53000	-	16.900	-

# getting to know the PAK MKII

## ICP42S Specifications continued

### Bandwidth Specification for a 51200 Hz Sampling Rate

Passband characteristics ( $f_s = 51200$ Hz)					
Parameter	Frequency (Hz)	Frequency Specification (Hz)		Attenuation (dB) $T_A = 23^\circ\text{C} \pm 5^\circ\text{C}$	
		Min	Max	Min	Max
Passband	100	-	100.02	-	0.018
	1000	-	1000.05	-	0.018
	22900	-	22901	-	0.030
	23600	-	23601	-	0.062
	24600	-	24601	-	1.020
	25080	-	25081	-	2.700
	26500	26500	-	17.000	-

Conditions:

- Within 30 minutes after “self calibration”
- Following the required 1 hour warm-up period of the PAK MKII
- Module Temperature of  $55^\circ\text{C} \pm 7^\circ\text{C}$
- $T_A$  : ambient temperature
- 90 Day Specifications of the Agilent 34410A are used

# chapter four

## ICP42S Features

Parameter	Mode	Value			
Module Connector	-	Lemo EHG.0B.303.CLN			
Channels	-	4 input			
Interface	ICP®	For ICP® sensors, 4 mA excitation, 22 V span			
	ALI	For analog source voltages			
Input Coupling Note 12	ICP®	AC			
	ALI	DC or AC			
AC Coupling Frequency Response (first order response)	ICP® / ALI	Attenuation	Min	Max	Unit
		-3 dB	-	0.25	Hz
Input Bias	ICP®	Differential			
	ALI	Differential, single-ended to Module Ground (isolated) or single-ended to Chassis Ground (non-isolated)			
Input Voltage Range	-	$\pm 60$ V (only ALI mode), $\pm 10$ V, $\pm 1.0$ V, $\pm 100$ mV			
Input Impedance	-	$2 \text{ M}\Omega \parallel 300 \text{ pF}$ (Differential) ( $\pm 10$ V, $\pm 1.0$ V, $\pm 100$ mV) $1 \text{ M}\Omega \parallel 300 \text{ pF}$ (Single Ended) ( $\pm 10$ V, $\pm 1.0$ V, $\pm 100$ mV) $600 \text{ k}\Omega \parallel 100 \text{ pF}$ (Differential) ( $\pm 60$ V)			
DC Offset Note 2, 9	ICP® / ALI	130 $\mu$ V ( $\pm 60$ V), 11 $\mu$ V ( $\pm 10$ V), 1 $\mu$ V ( $\pm 1.0$ V), 0.2 $\mu$ V ( $\pm 100$ mV)			
Maximum Sampling Rate per Channel (fs)	-	204.8 kHz			
Other Sampling Rates	-	Available through digital LP filters and decimation			
Onboard ADC	-	4x sigma-delta			
Resolution	-	16/24-bit			
Digital HP Filter Note 1	-	$-3$ dB at 1 Hz, $-0.1$ dB at 6.5 Hz ( $fs \leq 48$ kHz), $-3$ dB at 2 Hz, $-0.1$ dB at 13 Hz ( $fs = 96$ kHz), $-3$ dB at 4 Hz, $-0.1$ dB at 26 Hz ( $fs = 192$ kHz) Filter scales with sampling rate			
Digital LP Filter Note 1	-	Passband = $0.45 * fs$ Stopband = $0.55 * fs$ Passband ripple = $\pm 0.005$ dB ( $fs \leq 48$ kHz), $\pm 0.005$ dB ( $fs = 96$ kHz), $\pm 0.005$ dB ( $fs = 192$ kHz) Stopband attenuation = 100 dB ( $fs \geq 48$ kHz) Stopband attenuation = 80 dB ( $fs < 48$ kHz)			

# getting to know the PAK MKII

## ICP42S Features continued

Parameter	Mode	Value
<b>Optional Programmable Digital IIR Filter</b>	-	Band pass/stop : 6 dB/octave High/Low pass: 12 dB/octave
<b>SNR</b> (fs = 48 kHz) Note 2, 3, 9	ALI	123 dB ( $\pm 60$ V), 136 dB ( $\pm 10$ V), 135 dB ( $\pm 1.0$ V), 130 dB ( $\pm 100$ mV)
<b>THD</b> (fs = 48 kHz) Note 2, 4, 9	ALI	96 dB ( $\pm 60$ V), 104 dB ( $\pm 10$ V), 106 dB ( $\pm 1.0$ V), 100 dB ( $\pm 100$ mV)
<b>SFDR<sub>IV</sub></b> (fs = 48 kHz) Note 2, 5, 9, 10	ALI	93 dB ( $\pm 60$ V), 115 dB ( $\pm 10$ V), 133 dB ( $\pm 1.0$ V), 136 dB ( $\pm 100$ mV)
	ICP®	114 dB ( $\pm 10$ V), 133 dB ( $\pm 1.0$ V), 146 dB ( $\pm 100$ mV)
<b>SFDR<sub>10V</sub></b> (fs = 48 kHz) Note 2, 5, 9, 11	ALI	113 dB ( $\pm 60$ V), 135 dB ( $\pm 10$ V), 153 dB ( $\pm 1.0$ V), 156 dB ( $\pm 100$ mV)
	ICP®	134 dB ( $\pm 10$ V), 153 dB ( $\pm 1.0$ V), 166 dB ( $\pm 100$ mV)
<b>SFDR<sub>H</sub></b> (fs = 48 kHz) Note 2, 6, 9, 10	ALI	101 dB ( $\pm 60$ V), 114 dB ( $\pm 10$ V), 118 dB ( $\pm 1.0$ V), 106 dB ( $\pm 100$ mV)
<b>Crosstalk</b> (fs = 48 kHz) Note 2, 7, 9	ALI	114 dB ( $\pm 60$ V), 133 dB ( $\pm 10$ V), 131 dB ( $\pm 1.0$ V), 110 dB ( $\pm 100$ mV)
<b>Noise Floor</b> (fs = 48 kHz) Note 2, 8, 9, 10	ALI	-106 dB ( $\pm 60$ V), -128 dB ( $\pm 10$ V), -146 dB ( $\pm 1.0$ V), -157 dB ( $\pm 100$ mV)
<b>Phase Accuracy</b>	-	< 0.2 ° at 10 kHz
<b>Overflow Detection</b>	-	Analog window comparators
<b>Module Calibration</b>	-	Internal amplitude and phase calibration
<b>Protection</b>	ALI / ICP®	2 kV ESD
	ICP®	Short circuit between sensor case and ground

# chapter four

## ICP42S Features continued

Parameter	Mode	Value
Galvanic Isolation	-	50 V
TEDS	-	Support for IEEE 1451.4 Class 1

The different modes and parameter values mentioned in the features table are all software-selectable.

*Note 1:* Digital filters form part of the onboard ADC. Channels 1 and 2 are converted by the 2-channel sigma-delta ADC and thus share the same HP and LP filter setup. The same is true for channels 3 and 4.

*Note 2:* Measured after Module auto calibration has been applied.

*Note 3:* Signal to Noise Ratio (SNR): The ratio of the rms signal amplitude to the rms noise value excluding harmonics. Input signals are 7.5 V<sub>amplitude</sub> ( $\pm 10$  V Range), 750 mV<sub>amplitude</sub> ( $\pm 1$  V Range) and 75 mV<sub>amplitude</sub> ( $\pm 100$  mV Range) @ 1 kHz.

*Note 4:* Total Harmonic Distortion (THD): The ratio of the root-sum-squares of the first 10 harmonic amplitudes to the fundamental signal amplitude. Input signals are 7.5 V<sub>amplitude</sub> ( $\pm 10$  V Range), 750 mV<sub>amplitude</sub> ( $\pm 1$  V Range) and 75 mV<sub>amplitude</sub> ( $\pm 100$  mV Range) @ 1 kHz.

*Note 5:* Spurious Free Dynamic Range (SFDR): The ratio of the full scale input to the amplitude of the largest spurious spectral component (Inputs terminated with a short circuit. Measurement bandwidth: 100 Hz to  $f_s / 2$  excluding harmonics).

*Note 6:* Spurious Free Dynamic Range (SFDR<sub>H</sub>): The ratio of the fundamental signal amplitude to the amplitude of the highest peak including the first and all other harmonics. Measurement bandwidth: 100 Hz to  $f_s / 2$ . Input signals are 7.5 V<sub>amplitude</sub> ( $\pm 10$  V Range), 750 mV<sub>amplitude</sub> ( $\pm 1$  V Range) and 75 mV<sub>amplitude</sub> ( $\pm 100$  mV Range) @ 1 kHz.

*Note 7:* Crosstalk: Signal is played into a channel while the remaining channels are short circuited. The crosstalk is the ratio of the fundamental signal amplitude of the input channel to the signal amplitude at the fundamental frequency on the remaining channels. Input signals are 7.5 V<sub>amplitude</sub> ( $\pm 10$  V Range), 750 mV<sub>amplitude</sub> ( $\pm 1$  V Range) and 75 mV<sub>amplitude</sub> ( $\pm 100$  mV Range) @ 1 kHz.

*Note 8:* Noise Floor: The rms noise value specified in dB when the inputs are terminated with a short circuit.

*Note 9:* Listed values are typical measurement values.

*Note 10:* 0 dB is equal to 1 V.

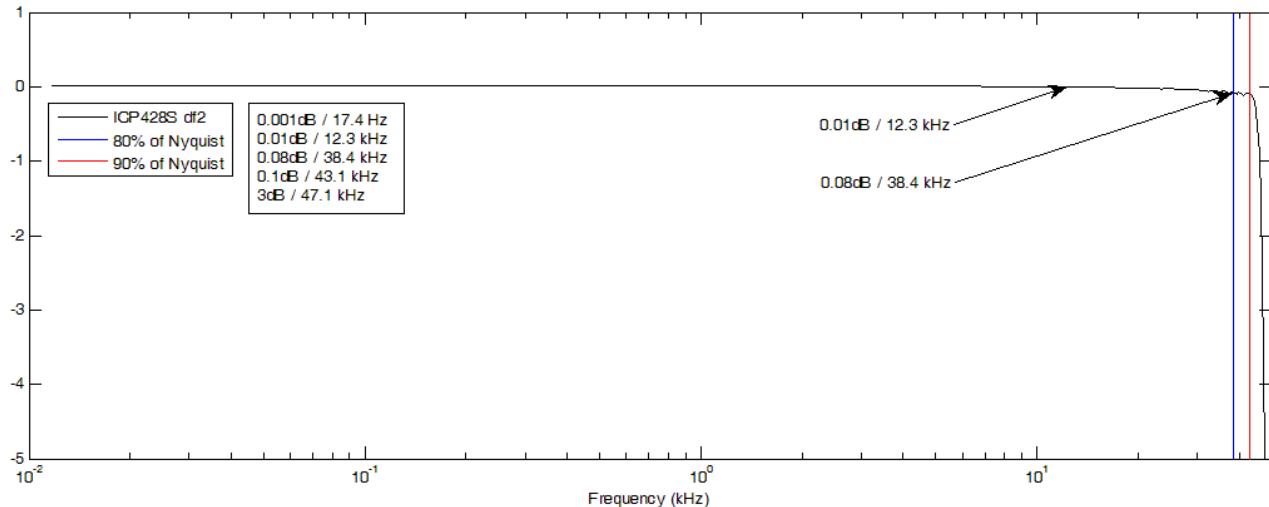
*Note 11:* 0 dB is equal to 10 V.

*Note 12:* ICP® mode is AC coupled in hardware by default

# getting to know the PAK MKII

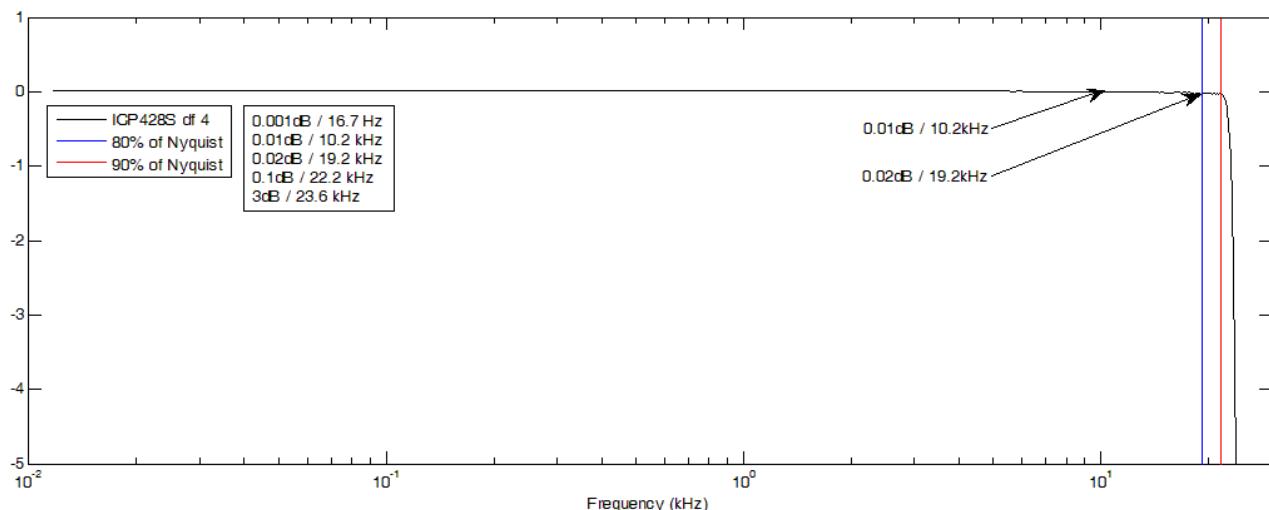
## ICP42S Features continued

### Frequency Response Analysis



#### Notes:

Nyquist frequency is 48 kHz. 0 dB equals 7.5 Vpp.



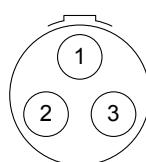
#### Notes:

Nyquist frequency is 24 kHz. 0 dB equals 7.5 Vpp.

## CONNECTOR PIN DEFINITIONS

Following are the Lemo connector pin definitions for each channel input of the ICP42S:

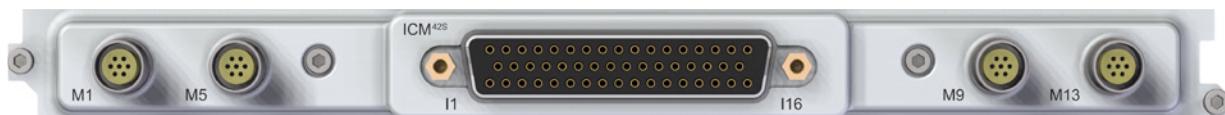
- Pin 1: AGNDM
- Pin 2: Signal +
- Pin 3: Signal -



Pin definitions for the three pin Lemo on the ICP42S Modules (when looking into the connector). It also applies to the ICP® channels on the ICT42S.

## ICM42S

The ICM42S builds on the ICP42 series. The ICM42S has a single DB50 connector with 16 ICP® input channels and four 7-pin Lemo connectors with a monitoring output channel for every input channel (16 monitoring output channels).



ICM42S front panel

### CHANNEL FEATURES

1. Analog input (ALI) mode
2. ICP® mode (with 4 mA current source)
3. DC or AC coupling
4. Input ranges:  $\pm 10$  V,  $\pm 1$  V,  $\pm 0.1$  V
5. Output gain: 1, 10, 100 V/V
6. TEDS read/write
7. Sampling rates up to 204.8 kSa/s
8. 24-bit resolution
9. Improved front end protection
10. High input impedance in power down
11. ICP® integrity checking
12. Overvoltage detection front end only
13. Differential, pseudo differential or single-ended inputs
14. Improved calibration accuracy
15. DB50 with 16 input channels
16. 16 Monitoring output channels
17. Monitoring output channel calibration / self test
18. Individual CGND switches for each channel
19. Muting the monitoring output channel

# getting to know the PAK MKII

## DETAILED FEATURE DESCRIPTION: ICP® CHANNELS

### Analog Input Mode

In this mode the Module input is a voltage with the highest input range being  $\pm 10$  V. There are 3 hardware input ranges, namely  $\pm 10$  V,  $\pm 1$  V and  $\pm 0.1$  V. Two different input biasing modes are available in this mode, namely differential and single-ended. The input biasing has been extended and differs slightly from the ICP42 series. In differential mode the positive and negative signal line is connected to GND through  $1\text{ M}\Omega$  resistors. Single-ended mode has three possible setup conditions the first where the negative signal line is connected directly to Analog Ground, the second where the negative signal line is connected directly to Chassis Ground but no connection exists between Analog and Chassis Ground and the third option is where the negative signal line is connected to Analog Ground and Analog Ground is tied to Chassis Ground. Please find a detailed grounding section under the Module application heading.

### ICP® Mode

A 4 mA current is supplied as required by the ICP® sensors. In this mode AC coupling is always enabled, and the Module must be in differential input biasing.

### AC/DC Coupling

When AC mode is enabled (selectable in ALI mode, always enabled for ICP® mode) the -3 dB cutoff frequency of the filter is approximately 3.5 Hz.

### TEDS

The TEDS circuitry complies with the IEEE 1451.4 standard. The negative terminal is connected to the Modules ground, and the positive terminal to the TEDS I/O line. The Module supports TEDS version 0.9 and version 1.0.

### Sampling Rates

The Module can sample up to 204.8 kSa/s.

### High Input Impedance at Power Down

The Module switches to high input impedance at power down.

### ICP® Integrity Checking and Ovvoltage Detection

ICP® integrity checking and overvoltage detection in ICP® and ALI mode is included with this Module. When the Module is in ICP® mode, the ICP® integrity checking is automatically activated. From the set limits the Module can detect four fault conditions on the ICP® channel namely: sensor connected correctly, no sensor connected, positive signal line shorted circuited to the negative signal line and negative signal line short circuited to GND. When the Module is in ALI mode the integrity circuit will compare the input signals against the fixed limits and inform the User if the input exceeds these limits.

## ICM42S

continued

# chapter four

## ICM42S

continued

### DETAILED FEATURE DESCRIPTION: OUTPUT CHANNELS

#### Monitoring Output Channels

The monitoring output channels play out whatever signal was played into that specific channel. There is an output monitoring channel for every input channel. The monitoring output channels have three possible gain settings namely a gain of 1, 10 or 100 V/V. These gains scale automatically with the Modules selected input range. When the Module is in the 10 V input range an output gain of 1 is selected (maximum output signal  $\pm 10$  V), when the Module is in 1 V input range an output gain of 10 is selected (maximum output signal  $\pm 10$  V) and when the Module input range is 100 mV an output gain of 100 is selected (maximum output signal  $\pm 10$  V).

### ICM42S Specifications

#### DC and AC Accuracy

Function	Range	Input Voltage	Error Specification ( $\pm$ % of range) $T_A = 23^\circ\text{C} \pm 5^\circ\text{C}$
DC Voltage	100 mV	100 mV	0.529
	1.0 V	1.0 V	0.086
	10.0 V	10.0 V	0.096
AC Voltage	100 mV	100 mV	0.593
	1.0 V	1.0 V	0.148
	10.0 V	10.0 V	0.143

Conditions:

- Within 30 minutes after “self calibration”
- Following the required 1 hour warm-up period of the PAK MKII
- Module Temperature of  $55^\circ\text{C} \pm 7^\circ\text{C}$
- $T_A$  : ambient temperature
- 90 Day Specifications of the Agilent 34410A are used

# getting to know the PAK MKII

## UNDERSTANDING THE % OF RANGE ERROR

The range error compensates for inaccuracies that result from the function and range the User selects. Example: Consider an input signal of 5 V<sub>DC</sub> in the 10 V range. The 5 V<sub>DC</sub> signal would be measured in the 10V range.

$$\text{Error} = \pm 0.096 \% \times 10.0 = \pm 9.6 \text{ mV}$$

### Excitation

Function	Minimum	Maximum	Unit
Excitation Voltage	22.00	24.00	V
Constant Current	3.92	4.18	mA

Conditions:

- Within 30 minutes after “self calibration”
- Following the required 1 hour warm-up period of the PAK MKII
- Module Temperature of 55 °C ± 7 °C
- T<sub>A</sub> : ambient temperature
- 90 Day Specifications of the Agilent 34410A are used

# chapter four

## ICM42S Specifications continued

### Bandwidth Specifications

The published attenuation values include the errors made during the measurement (DMM measurement errors) as well as errors made with the RMS calculation and represents the attenuation relative to the input voltage.

#### Bandwidth Specifications for a 204800 Hz Sampling Rate

Passband characteristics (fs = 204800 Hz)					
Parameter	Frequency (Hz)	Frequency Specification (Hz)		Attenuation (dB) $T_A = 23^\circ\text{C} \pm 5^\circ\text{C}$	
		Min	Max	Min	Max
Passband	100	-	100.01	-	0.018
	1000	-	1000.05	-	0.018
	51100	-	51103	-	0.094
	90000	-	90005	-	0.150
	95000	-	95005	-	0.234
	100500	-	100505	-	3.700
	106000	106000	-	14.500	-

#### Bandwidth Specifications for a 102400 Hz Sampling Rate

Passband characteristics (fs = 102400 Hz)					
Parameter	Frequency (Hz)	Frequency Specification (Hz)		Attenuation (dB) $T_A = 23^\circ\text{C} \pm 5^\circ\text{C}$	
		Min	Max	Min	Max
Passband	100	-	100.01	-	0.018
	1000	-	1000.05	-	0.018
	25500	-	25502	-	0.030
	46600	-	46603	-	0.050
	47500	-	47503	-	0.110
	50150	-	50153	-	2.800
	53000	53000	-	16.900	-

# getting to know the PAK MKII

## ICM42S Specifications continued

### Bandwidth Specification for a 51200 Hz Sampling Rate

Passband characteristics ( $f_s = 51200$ Hz)					
Parameter	Frequency (Hz)	Frequency Specification (Hz)		Attenuation (dB) $T_A = 23^\circ\text{C} \pm 5^\circ\text{C}$	
		Min	Max	Min	Max
Passband	100	-	100.02	-	0.018
	1000	-	1000.05	-	0.018
	22900	-	22901	-	0.030
	23600	-	23601	-	0.062
	24600	-	24601	-	1.020
	25080	-	25081	-	2.700
	26500	26500	-	17.000	-

Conditions:

- Within 30 minutes after “self calibration”
- Following the required 1 hour warm-up period of the PAK MKII
- Module Temperature of  $55^\circ\text{C} \pm 7^\circ\text{C}$
- $T_A$  : ambient temperature
- 90 Day Specifications of the Agilent 34410A are used

# chapter four

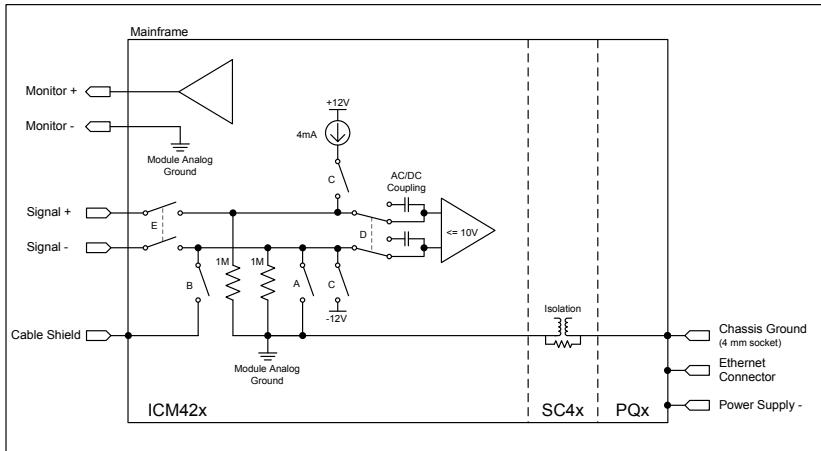
## ICM42S Features

### Module Features

Parameter	Mode	Value
Module Connector		DB50 and Lemo EHG.0B.307
Channel		16 input, 16 output
Interface	ICP®	For ICP® sensors, 4 mA excitation, 22 V span
	ALI	For analog source voltages
Input Coupling	ICP®	AC
	ALI	DC or AC
Input Biasing	ICP®	Differential
	ALI	Differential, single-ended to Module Ground (isolated), single-ended to Chassis Ground (non-isolated) or single-ended to Chassis Ground
Input Voltage Range	ICP® / ALI	±10 V, ±1.0 V, ±100 mV
Input Impedance		2 MΩ    300 pF (Differential) 1 MΩ    300 pF (Single-Ended)
Sampling Rate / Channel (Max)	-	204.8 kHz
Resolution	-	16 / 24 bit
Phase Accuracy (Same Voltage Range)		< 0.2° at 10 kHz
TEDS		Support for IEEE 1451.4 Class 1
Galvanic Isolation		50 V
Protection	ICP® / ALI	2 kV ESD
	ICP®	Short circuit protection between case and ground

# getting to know the PAK MKII

## ICM42S Grounding Diagram



**ICM42S**  
continued

## ICM42S Grounding Settings

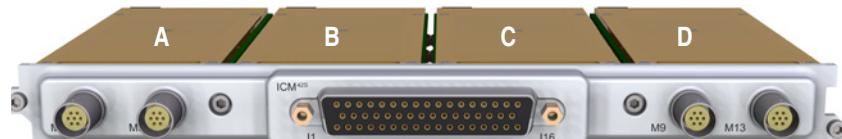
PAK Ground Setting ↓	A	B	C	D
ALI (Voltage Input) Mode				
Module Ground	Closed	Open	Open	AC/DC
Differential	Open	Open	Open	AC/DC
System Ground	Closed	Closed	Open	AC/DC
Diff. (Analog to System Ground)	Open	Closed	Open	AC/DC
ICP® Mode				
Differential	Open	Open	Closed	AC Coupling

# chapter four

## ICM42S

continued

### PIN DESCRIPTIONS AND REFERENCE PICTURES



#### ICM42S with reference numbering:

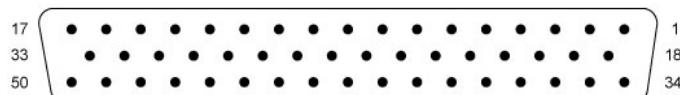
In the pin diagram and explanations below reference is made to the Module slots A to D from left to right where the Module slots provide the 16 input channels as follows:

1. Module slot A provides channel 1 to 4,
2. Module slot B provides channel 5 to 8,
3. Module slot C provides channel 9 to 12 and
4. Module slot D provides channel 13 to 16.

The 7-pin Lemo connectors are referred to as M1, M5, M9 & M13 (from left to right) and shows the monitoring channels of the Lemo connector. The numbering is as follows:

1. M1 provides the positive and negative pins for monitoring channel 1 to 4,
2. M5 provides the positive and negative pins for monitoring channel 5 to 8,
3. M9 provides the positive and negative pins for monitoring channel 9 to 12 and
4. M13 provides the positive and negative pins for monitoring channel 13 to 16.

# getting to know the PAK MKII



**ICM42S**

continued

Pin descriptions of a DB50 female connector (when looking into the connector)

## PIN DIAGRAM LOOKING INTO THE FEMALE DB50

### DB50 Pin Descriptions (SC4x Card Layout)

Channel	Leg	Pin	Channel	Leg	Pin	Channel	Leg	Pin	Channel	Leg	Pin
CH-1	+	1	CH-5	+	5	CH-9	+	26	CH-13	+	30
CH-1	-	18	CH-5	-	22	CH-9	-	43	CH-13	-	47
CH-1	Shield	34	CH-5	Shield	38	CH-9	Shield	10	CH-13	Shield	14
CH-2	+	35	CH-6	+	39	CH-10	+	11	CH-14	+	15
CH-2	-	2	CH-6	-	6	CH-10	-	27	CH-14	-	31
CH-2	Shield	19	CH-6	Shield	23	CH-10	Shield	44	CH-14	Shield	48
CH-3	+	3	CH-7	+	7	CH-11	+	28	CH-15	+	32
CH-3	-	20	CH-7	-	24	CH-11	-	45	CH-15	-	49
CH-3	Shield	36	CH-7	Shield	40	CH-11	Shield	12	CH-15	Shield	16
CH-4	+	37	CH-8	+	41	CH-12	+	13	CH-16	+	17
CH-4	-	4	CH-8	-	8	CH-12	-	29	CH-16	-	33
CH-4	Shield	21	CH-8	Shield	25	CH-12	Shield	46	CH-16	Shield	50
Module Slot A			Module Slot B			Module Slot C			Module Slot D		
ICM42S – DB50 Input											

Note: Pin 9 & 42 are reserved pins used with one wire protocol to identify the DB50 connector and backplane (to be implemented).

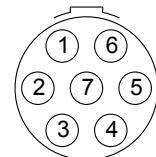
# chapter four

## ICM42S continued

### 7-PIN LEMO PIN DESCRIPTIONS

#### Pin description when looking into the 7-pin Lemo connector

1. Monitoring output channel 2 positive,
2. Monitoring output channel 3 positive,
3. Monitoring output channel 1 positive,
4. Monitoring output channel 4 & channel 1 negative,
5. Monitoring output channel 3 negative,
6. Monitoring output channel 2 negative and
7. Monitoring output channel 4 positive.



#### Monitoring Output (MO) Channel Pin Mapping to the 7-pin Lemo Connectors (M1, M5, M9 & M13)

Pin Number	Module A	Module B	Module C	Module D
1	MO channel 2+	MO channel 6+	MO channel 10+	MO channel 14+
2	MO channel 3+	MO channel 7+	MO channel 11+	MO channel 15+
3	MO channel 1+	MO channel 5+	MO channel 9+	MO channel 13+
4	MO channel 1- & 4 -	MO channel 5- & 8 -	MO channel 9- & 12 -	MO channel 13- & 16 -
5	MO channel 3-	MO channel 7-	MO channel 11-	MO channel 15-
6	MO channel 2-	MO channel 6-	MO channel 10-	MO channel 14-
7	MO channel 4+	MO channel 8+	MO channel 12+	MO channel 16+

# getting to know the PAK MKII

## 2 Channel Analog/ICP Input + 2 Channel Tacho Input

### ICT Module

#### DESCRIPTION

The ICT Module provides 2 input channels (channels 1 and 2) for measuring analog or ICP® signals and another 2 input channels (channels 3 and 4) for measuring Tacho signals.

The Tacho signal can be measured as number of pulses/sample period.

All with a 20 ns resolution. Such measurements can typically be used as a primary rate input for order tracking.

#### TYPES

2 ICT Module types exist, these being:

1. ICT42

- ICP® channels sample rate  $\leq$  102.4 kHz (SC42)
- Tacho channels 700 kPulses/s for a single channel or 350 kPulse/s via both Tacho channels

2. ICT42S

- ICP® channels sample rate  $\leq$  204.8 kHz (SC42S)
- Tacho channels 700 kPulses/s for a single channel or 350 kPulse/s via both Tacho channels

## ICT42



### NOTE:

The sampling speed of scope mode on the ICT42 Module is limited to 204.8 kHz.

Channels 1 and 2 have the same performance parameters as the first 2 channels of the ICP42 Module.

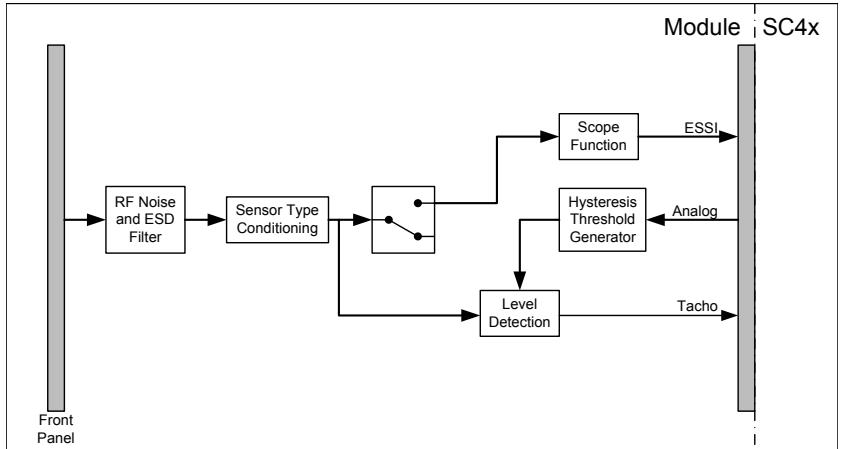
Channels 3 and 4 of the ICT Module are Tacho and scope input channels. Each Tacho channel functions separately and is connected to its own Tacho sensor. The scope channels display the input of the tacho channels and can only display a single channel at one time. These channels can be switched during a measurement and are used to setup the triggering levels.

As standard the ICT42 has a 4-pin Lemo connector for each Tacho input at the Module front panel. 2 of the Lemo connector pins are for the Tacho signal. The 2 additional pins provide an excitation voltage that may be used as a power supply to external Tacho sensors. The Excitation+ and Excitation- lines are each protected against a current overload by a 140 mA self-resetting fuse. There are two options for the excitation output: either 24 V or 12 V can be provided (in both cases the Excitation+ is +12 V; the Excitation- can be either 0 V or -12 V).

One of the new features on the ICT42 is to set-up a Tacho input channel in scope mode. In this mode the ICT42 will acquire the Tacho signal which will be transferred to application software for graphical displaying. Scope mode is considered a pre-test setup to configure the trigger and hysteresis levels. Scope mode may be disabled to save on Module power consumption.

# getting to know the PAK MKII

## ICT42 Functionality per Tacho Input Channel



**ICT42**  
continued

## ICT42 Features for Tacho Channels

Parameter	Value
Module Connector	Lemo EHG.0B.304
Channels	2 Tacho signal inputs
Tacho Sensor	Voltage (single-ended or differential)
Excitation Voltage Level	0 V... 12 V (12 V), -12 V... +12 V (24 V)
Excitation Maximum Current	140 mA (fused)
Coupling	DC or AC
Input Impedance	240 kΩ
Input Voltage Range	±2 V, ±15 V, ±60 V
Over-voltage Range	±60 V
Trigger Accuracy	Threshold detection with hysteresis; 16-bit threshold resolution
Counter Resolution	20 ns

# chapter four

## ICT42 Features for Tacho Channels continued

Parameter	Value
Maximum Input Pulse Rate Note 2	700 kPulses/s or 350 kPulses/s (Note 1)
Minimum Pulse Width	800 ns
Scope Mode	$25.5 \text{ kHz} < f_s < 204.8 \text{ kHz}$
Module Calibration	Internal amplitude and phase calibration
Protection	ESD 2 kV
Galvanic Isolation	50 V
TEDS	Not supported

The different parameter values mentioned in the features table are all software-selectable. This includes trigger and hysteresis levels.

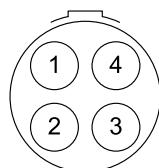
**Note 1:** For PAK MKII firmware version 3-5-B (and thereafter) with PAK version 5.4 Service Release 7.1 (and thereafter) the maximum pulse rate is 700 kPulses/s when 1 tacho input is acquired or 350 kPulses/s when both the tacho inputs are acquired.

**Note 2:** Maximum input pulse rate scales with master sampling rate (MSR).

## CONNECTOR PIN DEFINITIONS

Following are the Lemo connector pin definitions for each tacho input of the ICT42:

- Pin 1: Signal-
- Pin 2: Excitation+
- Pin 3: Excitation-
- Pin 4: Signal+



Pin definitions (when looking into the connector)

# getting to know the PAK MKII

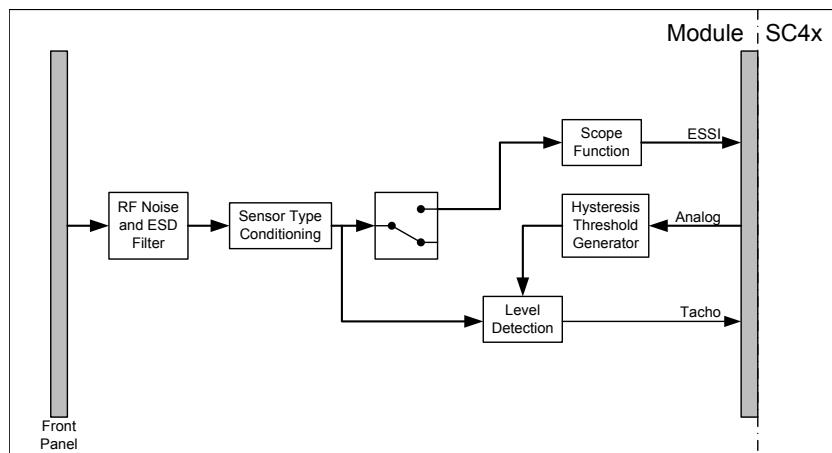


ICT42S

The ICT42S Module follows on the ICT42 Module with some added features. For example it supports  $\pm 60$  V range on the ICP® channels and higher sampling rates in scope mode. The sampling speed of scope mode on the ICT42S Module is 9.71 MHz.

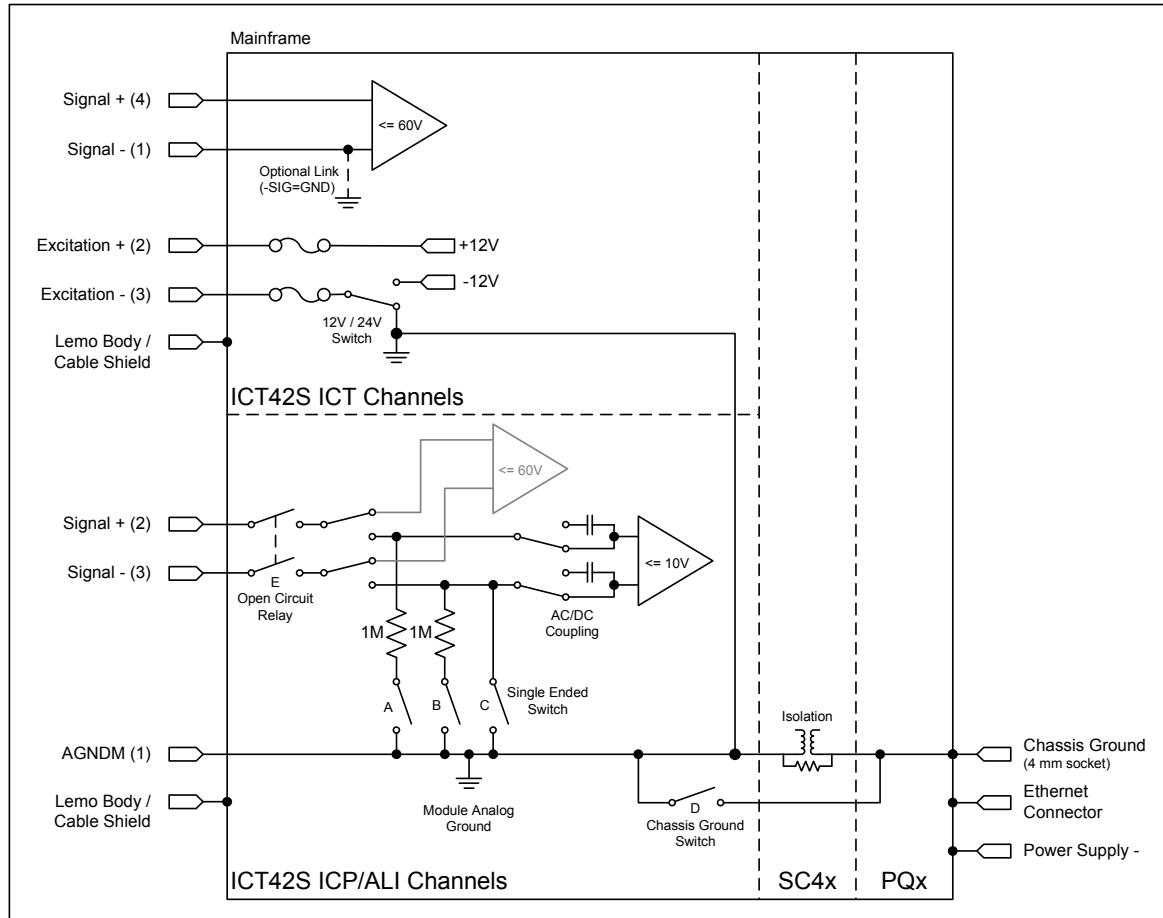
The following figure provides further insight into the ICT42S tacho channel functionality while the table contains the tacho input specifications (see the ICP42S description for the ICP® channel specifications).

## ICT42S Functionality per Tacho Input Channel



# chapter four

## ICT42S Grounding Diagram



## ICT42S Grounding Settings

PAK Ground Setting ↓	Single-Ended Switch (C)	Chassis Ground Switch (D)	Signal + 1M (A)	Signal – 1M (B)
<b>ALI (voltage input) Mode</b>				
Module Ground	Closed	Open	Closed	Open
Differential	Open	Open	Closed	Closed
System Ground	Closed	Closed	Closed	Open
Diff. (Analog to System Ground)	Open	Closed	Closed	Closed
<b>ICP® Mode</b>				
Differential	Open	Open	Open	Open
Diff. (Analog to System Ground)	Open	Closed	Open	Open

# getting to know the PAK MKII

## ICT42S Features for Tacho Channels

Parameter	Value
Module Connector	Lemo EHG.0B.304
Channels	2 Tacho signal inputs
Tacho Sensor	Voltage (single-ended or differential)
Excitation Voltage Level	0 V... 12 V (12 V), -12 V... +12 V (24 V)
Excitation Maximum Current	140 mA (fused)
Coupling	DC or AC
Input Impedance	240 kΩ
Input Voltage Range	±2 V, ±15 V, ±60 V
Over-voltage Range	±60 V
Trigger Accuracy	Threshold detection with hysteresis; 16-bit threshold resolution
Counter Resolution	20 ns
Maximum Input Pulse Rate Note 2	700 kPulses/s or 350 kPulses/s (Note 1)
Minimum Pulse Width	800 ns
Scope Mode	25.5 kHz < fs < 9.71 MHz (Note 3) (Sampling rate scales with fs)
Module Calibration	Internal amplitude and phase calibration
Protection	ESD 2 kV
Galvanic Isolation	50 V
TEDS	Not supported

# chapter four

## ICT42S continued

### ICT42S Specifications for Tacho Channels continued

The different parameter values mentioned in the specifications table are all software-selectable. This includes trigger and hysteresis levels.

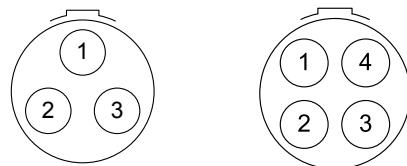
*Note 1:* For PAK MKII firmware version before 4-2-g and before PAK version 5.5 the maximum pulse rate is 700 kPulses/s when 1 tacho input is acquired or 350 kPulses/s when both the tacho inputs are acquired.

*Note 2:* Maximum input pulse rate scales with master sampling rate (MSR).

*Note 3:* Sampling rates of up to 9.71 MHz are supported on the ICT42S.

### CONNECTOR PIN DEFINITIONS FOR ICT42S

Following are the Lemo connector pin definitions for the ICT42S:



Lemo pin definitions (when looking into the connector)

Pin	ICP®/ALI Channels	ICT Channels
1	AGNDM	Signal -
2	Signal +	Excitation +
3	Signal -	Excitation -
4		Signal +

## 4 Channel Charge Input

## CHG Module

### DESCRIPTION

The CHG Module provides 4 input channels for detecting the charge levels generated by piezoelectric sensors that are typically used to measure acceleration, force and pressure. These are most suited to high temperature, low mass and high accuracy applications.

### TYPES

1. CHG42 with a 24-bit ADC and the following sampling limits:
  - $\leq 102.4 \text{ kHz} / \text{channel}$  for all channels

### WARNING:

When using Endevco cables it is recommended to remove the rubber o-ring on the CHG Module 10-32 connector as this could cause an intermittent electrical connection between the pin on the cable and the Module connector.

# chapter four

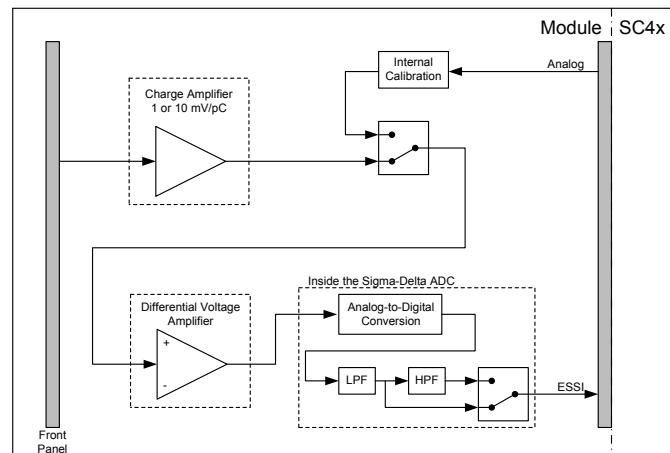
## CHG42



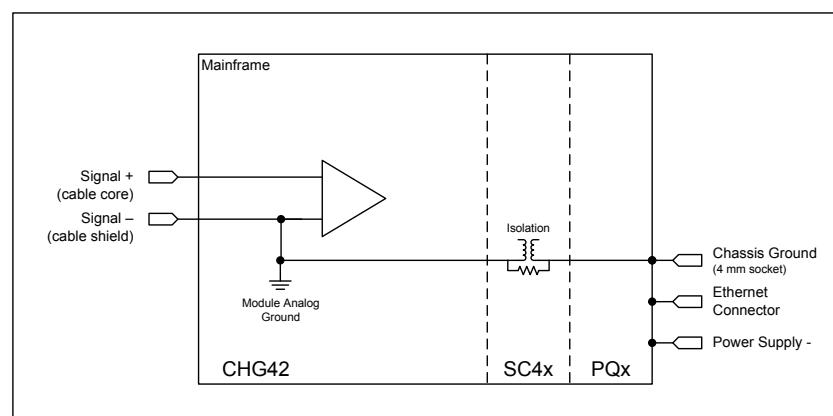
### NOTE:

Do not use the 100 mV range at high Module temperatures. Please refer to Charge Amplifier Offset specifications.

### CHG42 Functionality per Channel



### CHG42 Grounding Diagram



# getting to know the PAK MKII

## CHG42 Features

Parameter	Value
Module Connector	10-32 Microdot Female
Channels	4 input
Interface	For piezoelectric sensors
Charge Amplifier Sensitivity	1 mV/pC and 10 mV/pC
Voltage Amplifier Range	±100 mV, ±1 V, ±10 V (peak)
Input Charge Range	±10 000 pC (peak)
Charge Amplifier Offset	10 mV @ 40°C 30 mV @ 50°C 70 mV @ 60°C
Low Frequency Cut-Off	-3 dB at 0.016 Hz (sensitivity 10 mV/pC) -3 dB at 0.160 Hz (sensitivity 1 mV/pC)
Maximum Sampling Rate per Channel (fs)	102.4 kHz
Other Sampling Rates	Available through digital LP filters and decimation
Onboard ADC	4x sigma-delta
Resolution	16/24-bit
Digital HP Filter <small>Note 1</small>	-3 dB at 1 Hz, -0.1 dB at 6.5 Hz (fs ≤ 48 kHz), -3 dB at 2 Hz, -0.1 dB at 13 Hz (fs = 96 kHz) Filter scales with sampling rate
Digital LP Filter <small>Note 1</small>	Passband = 0.45 * fs Stopband = 0.55 * fs Passband ripple = ±0.001 dB (fs ≤ 48 kHz), ±0.003 dB (fs = 96 kHz) Stopband attenuation = 110 dB (fs ≥ 48 kHz) Stopband attenuation = 80 dB (fs < 48 kHz)
Optional Programmable Digital IIR Filter	Band pass/stop: 6 dB/octave High/Low pass: 12 dB/octave
SNR (fs = 48 kHz) <small>Note 3, 4, 11</small>	141 dB (±10 V), 136 dB (±1.0 V), 118 dB (±100 mV)
THD (fs = 48 kHz) <small>Note 3, 5, 11</small>	100 dB (±10 V), 107 dB (±1.0 V), 88 dB (±100 mV)

# chapter four

## CHG42 Features continued

Parameter	Value	
<b>SFDR<sub>IV</sub></b> (fs = 48 kHz) Note 3, 6, 11, 12	114 dB ( $\pm 10$ V), 123 dB ( $\pm 1.0$ V), 123 dB ( $\pm 100$ mV)	
<b>SFDR<sub>10V</sub></b> (fs = 48 kHz) Note 3, 6, 11, 13	134 dB ( $\pm 10$ V), 143 dB ( $\pm 1.0$ V), 143 dB ( $\pm 100$ mV)	
<b>SFDR<sub>H</sub></b> (fs = 48 kHz) Note 3, 7, 11, 12	103 dB ( $\pm 10$ V), 112 dB ( $\pm 1.0$ V), 92 dB ( $\pm 100$ mV)	
<b>Crosstalk</b> (fs = 48 kHz) Note 3, 8, 11	99 dB ( $\pm 10$ V), 98 dB ( $\pm 1.0$ V), 88 dB ( $\pm 100$ mV)	
<b>Noise Floor</b> (fs = 48 kHz) Note 3, 9, 11, 12	-126 dB ( $\pm 10$ V), -141 dB ( $\pm 1.0$ V), -143 dB ( $\pm 100$ mV)	
<b>Range Accuracy</b> Note 10, 11	1 mV/pC Sensitivity	0.16% ( $\pm 10$ V), 0.19% ( $\pm 1.0$ V), 0.16% ( $\pm 100$ mV)
	10 mV/pC Sensitivity	0.27% ( $\pm 1.0$ V), 0.23% ( $\pm 100$ mV)
<b>Phase Accuracy</b>	< 0.5 ° at 10 kHz	
<b>Module Calibration</b>	Internal amplitude and phase calibration	
<b>Protection</b>	2.2 kΩ series (inline)	
<b>Galvanic Isolation</b>	50 V	
<b>TEDS</b>	Not supported	

The different parameter values mentioned in the features table are all software-selectable.

*Note 1:* Digital filters form part of the onboard ADC. Channels 1 and 2 are converted by the 2-channel sigma-delta ADC and thus share the same HP and LP filter setup. The same is true for channels 3 and 4.

*Note 2:* Measured with maximum input signal.

*Note 3:* Measured after Module auto calibration has been applied.

*Note 4:* Signal to Noise Ratio (SNR): The ratio of the rms signal amplitude to the rms noise value excluding harmonics. Input signals are 7.5 V<sub>amplitude</sub> ( $\pm 10$  V Range), 750 mV<sub>amplitude</sub> ( $\pm 1$  V Range) and 75 mV<sub>amplitude</sub> ( $\pm 100$  mV Range) @ 1 kHz.

*Note 5:* Total Harmonic Distortion (THD): The ratio of the root-sum-squares of the first 10 harmonic amplitudes to the fundamental signal amplitude. Input signals are 7.5 V<sub>amplitude</sub> ( $\pm 10$  V Range), 750 mV<sub>amplitude</sub> ( $\pm 1$  V Range) and 75 mV<sub>amplitude</sub> ( $\pm 100$  mV Range) @ 1 kHz.

*Note 6:* Spurious Free Dynamic Range (SFDR): The ratio of the full scale input to the amplitude of the largest spurious spectral component (Remaining channels are terminated with a 1 nF capacitor.).

*Note 7:* Spurious Free Dynamic Range (SFDR<sub>H</sub>): The ratio of the fundamental signal amplitude to the amplitude of the highest peak including the

# getting to know the PAK MKII

## CHG42 Features continued

first and all other harmonics. Measurement bandwidth: 100 Hz to  $f_s / 2$ . Input signals are 7.5 V<sub>amplitude</sub> ( $\pm 10$  V Range), 750 mV<sub>amplitude</sub> ( $\pm 1$  V Range) and 75 mV<sub>amplitude</sub> ( $\pm 100$  mV Range) @ 1 kHz.

**Note 8:** Crosstalk: Signal is played into a channel while the remaining channels are terminated with a 1 nF capacitor. The crosstalk is the ratio of the fundamental signal amplitude of the input channel to the signal amplitude at the fundamental frequency on the remaining channels. Input signals are 7.5 V<sub>amplitude</sub> ( $\pm 10$  V Range), 750 mV<sub>amplitude</sub> ( $\pm 1$  V Range) and 75 mV<sub>amplitude</sub> ( $\pm 100$  mV Range) @ 1 kHz.

**Note 9:** Noise Floor: The rms noise value specified in dB when the inputs are terminated with a 1 nF capacitor.

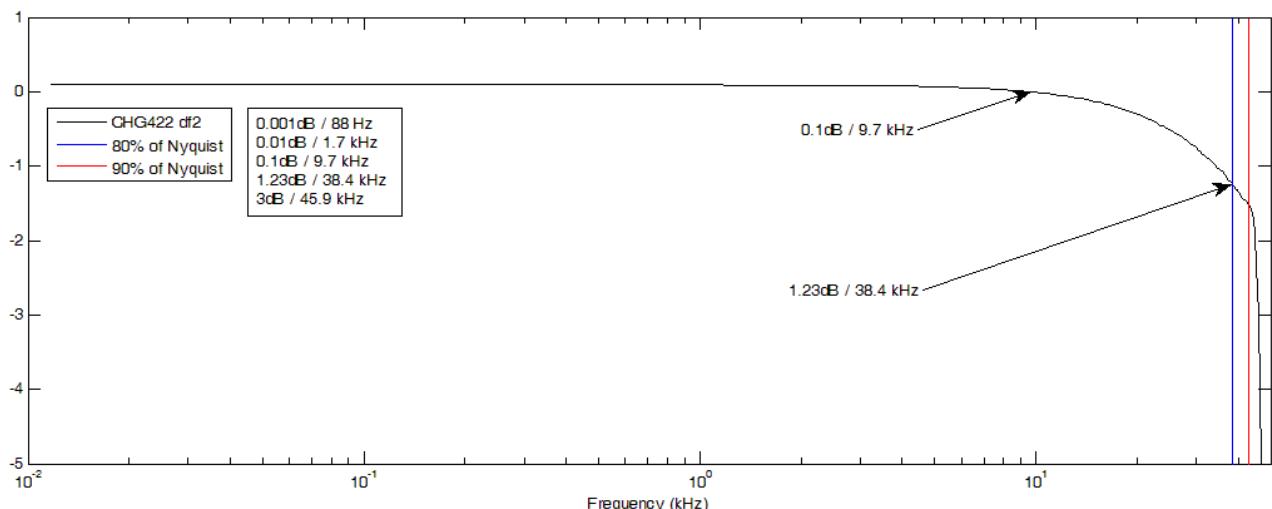
**Note 10:** Range Accuracy measured at 1 kHz.

**Note 11:** Listed values are typical measurement values.

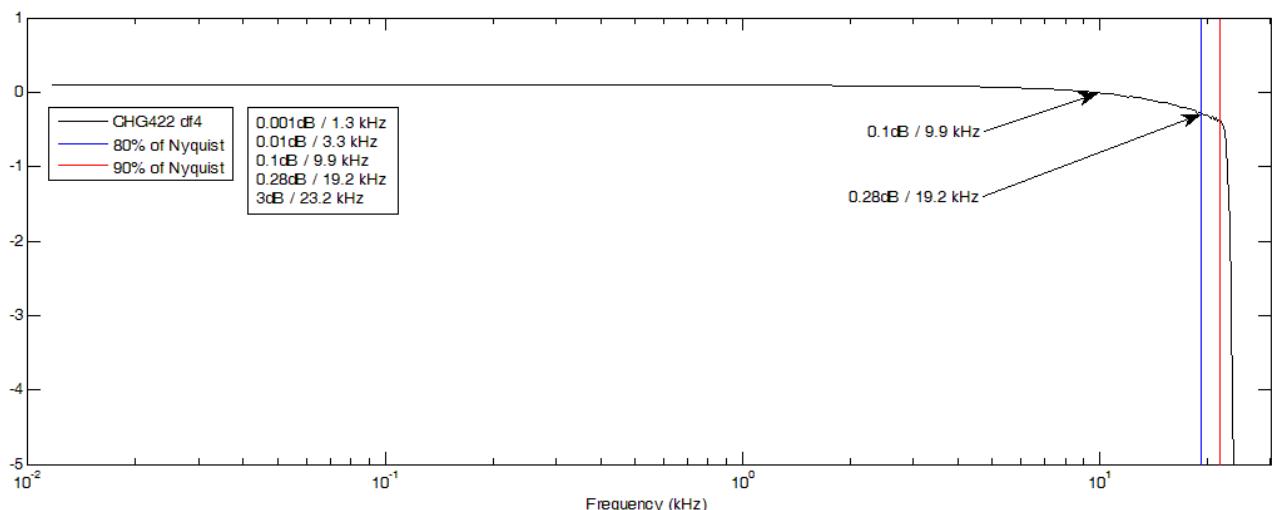
**Note 12:** 0 dB is equal to 1 V.

**Note 13:** 0 dB is equal to 10 V.

## Frequency Response Analysis



**Notes:** Nyquist frequency is 48 kHz. 0 dB equals 7.5 Vpp.



**Notes:** Nyquist frequency is 24 kHz. 0 dB equals 7.5 Vpp.

## DCH Module

## 2 Channel Differential Charge Input

### DESCRIPTION

The DCH42S Module provides 2 channels for measuring differential piezoelectric sensor signals at 204.8 kSa/s. It features two sensitivity settings, two time constant settings and a single ended mode for single ended piezoelectric signals.

The maximum input range is 50 000 pC<sub>pk</sub> in Differential Mode and 100 000 pC<sub>pk</sub> in Single Ended Mode. The module benefits from internal calibration of the three voltage gain ranges ( $\pm 100 \text{ mV}_{\text{pk}}$ ,  $\pm 1 \text{ V}_{\text{pk}}$  and  $\pm 10 \text{ V}_{\text{pk}}$ ). Measurement accuracy in Differential Mode is better than 1%.

### TYPES

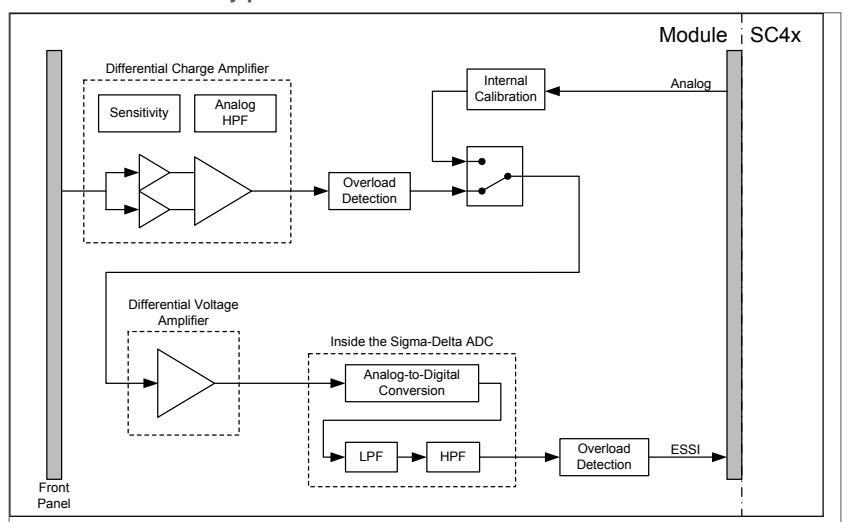
1. DCH42S with a 24-bit ADC and the following sampling limits:
  - $\leq 204.8 \text{ kHz} / \text{channel}$  for all channels

# getting to know the PAK MKII



DCH42S

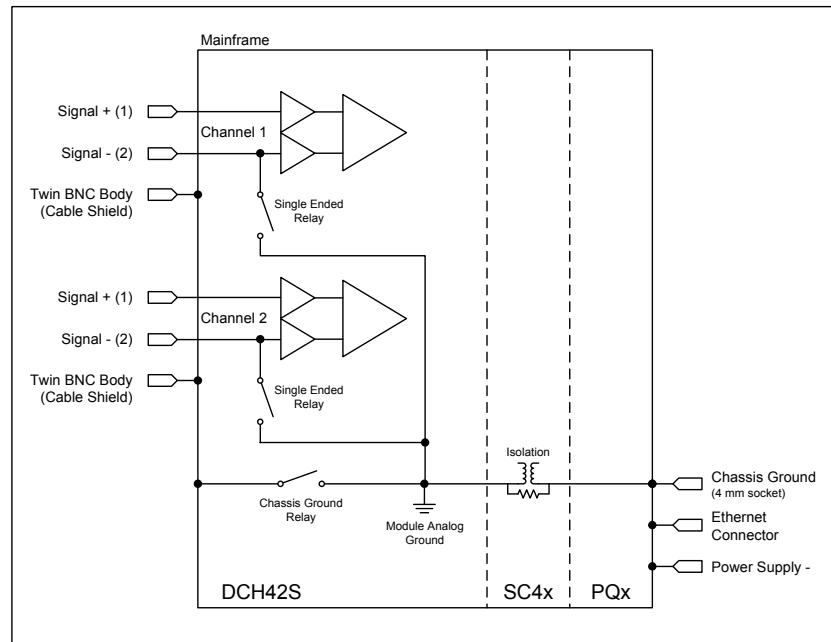
## DCH42S Functionality per Channel



# chapter four

## DCH42S continued

DCH42S Grounding Diagram



Note: It is possible to have the cable shield connected to the Twin BNC connector body, and thus the PAK MKII chassis.

PAK Ground Setting	Chassis Ground Relay	Single Ended Relay
<b>Single Ended Mode</b>		
Differential	Open	Open
Diff. (analog to system ground)	Closed	Open
<b>Differential Mode</b>		
Module Ground	Open	Closed
System Ground	Closed	Closed

# getting to know the PAK MKII

## DCH42S Specifications

Function	Value
Differential Mode Accuracy	< 1%

Conditions:

- Measured at a  $4\sigma$  confidence level
- Following the required 1 hour warm-up period of the PAK MKII
- Module Temperature of  $47^{\circ}\text{C} \pm 5^{\circ}\text{C}$
- $T_A$  : ambient temperature
- 1 Year Specifications of the Agilent 34410A are used

## DCH42S Features

Parameter	Value							
Module Connector	Amphenol 31-2225 Twin BNC							
Channels	2 inputs							
Interface	For differential and single ended piezoelectric sensors							
	Single Ended Mode				Differential Mode			
Input Charge Range	100 000 pC <sub>pk</sub>				50 000 pC <sub>pk</sub>			
Charge Amplifier Sensitivity (mV/pC)	0.1		1		0.2		2	
Charge Amplifier Sensitivity (pC/mV)	10		1		5		0.5	
Time Constant (seconds)	1	10	0.1	1	1	10	0.1	1
Analog HPF -3 dB (Hz)	0.16	0.016	1.6	0.16	0.16	0.016	1.6	0.16
Voltage Amplifier Range	±100 mV, ±1 V, ±10 V (peak)							
Maximum Sampling Rate per Channel (fs)	204.8 kHz							

# chapter four

## DCH42S Features continued

Parameter	Value				
Other Sampling Rates	Available through digital LP filters and decimation				
Onboard ADC	Sigma-Delta				
Resolution	16/24-bit				
Digital HP Filter	Sampling Rate (fs) (Hz)	-3 dB (Hz)	-0.1 dB (Hz)		
	6400 – 51200	1	6.5		
	65536 – 102400	2	13		
	131072 – 204800	4	26		
	Filter scales with sampling rate				
Digital HP Filter	Passband	0.45 * fs			
	Stopband	0.55 * fs			
	Passband ripple	$\pm 0.005$ dB max			
	Stopband attenuation	100 dB min			
	Filter scales with sampling rate				
SNR	115 dB				
SINAD	80 dB				
THD	100 dB				
SFDR	105 dB				
Cross Talk	115 dB				
Module Calibration	Internal amplitude calibration of voltage amplifier				
Protection	1 k $\Omega$ series (inline)				

# getting to know the PAK MKII

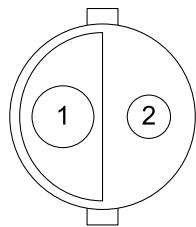
## DCH42S Features continued

Parameter	Value
Galvanic isolation	50 V
TEDS	Not supported

## CONNECTOR PIN DESCRIPTION

Pin 1: Signal positive

Pin 2: Signal negative



Pin definitions of a DCH42S module connector (when looking into the connector)

**DCH42S**  
continued

## TROUBLESHOOTING

### 1. Constant DC Offset

Ensure that the isolation resistances in the connector and cable are  $>1\text{ G}\Omega$ . This could be caused by cable failure or long term contamination of the connectors.

### 2. 50 Hz / 60 Hz Noise

Ensure that the shield did not break inside the Twin BNC plug on the cable.

## MIC Module

## 2 Channel Microphone Input

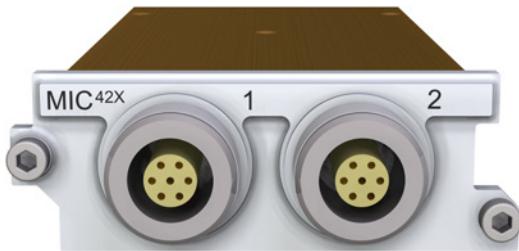
### DESCRIPTION

The MIC Module provides 2 input channels for measuring the analog audio signals generated by 2 microphones. The MIC Module provides excellent dynamic and low-noise performance required for audio measurements.

### TYPES

1. MIC42X with a 24-bit ADC and the following sampling limits:
  - $\leq 204.8 \text{ kHz} / \text{channel}$  for all channels

# getting to know the PAK MKII



**MIC42X**

This Module furthers the MIC42 and offers ICP® mode, signal integrity checking, signal overload detection, TEDS Class 1 and 2 as well as improved noise performance. It includes AC coupling and hardware gain stages for the measurement of small signals in the presence of large DC offsets.

Also included is voltage output, typically used for injecting test signals into microphone preamplifiers. Differential, or single-ended inputs cater for every need, while the  $\pm 14.5$  V preamplifier supply voltage provides for the latest B&K microphone preamplifiers.

The 24-bit ADC has excellent performance with a low passband ripple and a sharp roll-off for maximum useable bandwidth, and lowest stopband attenuation. The linearity of the ADC results in excellent phase performance, especially when paired with other 42 series Modules.

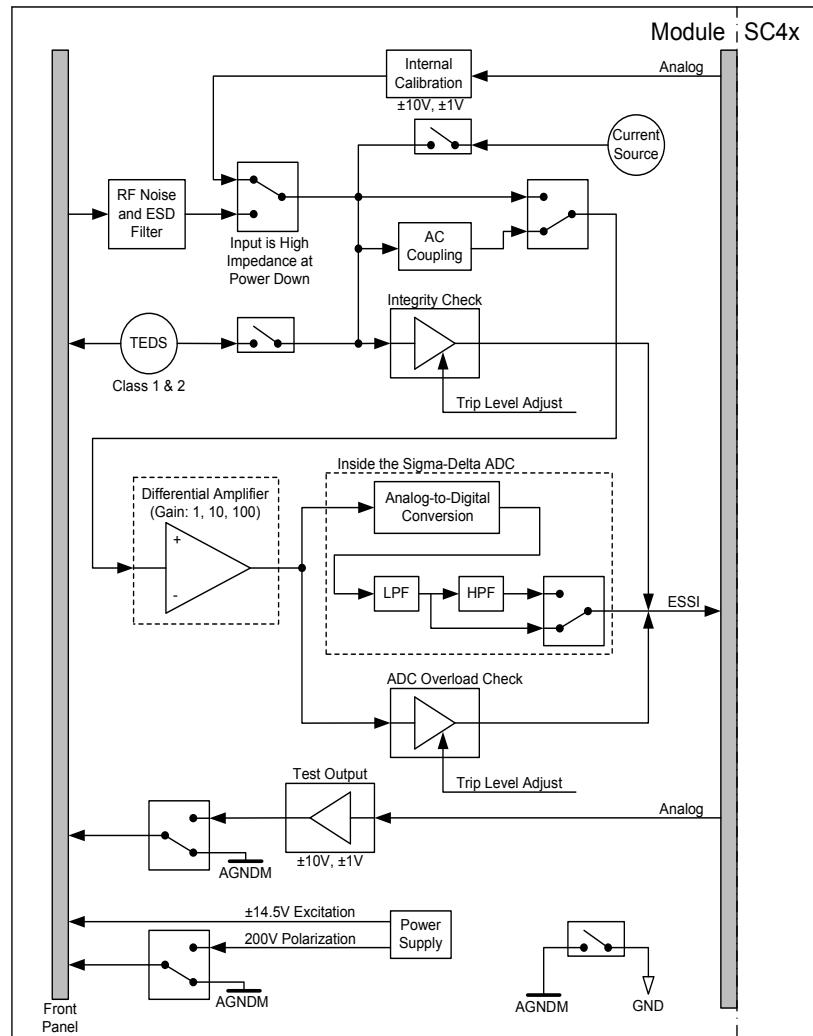
## CHANNEL FEATURES

1. Analog input (ALI) mode
2. ICP® mode with integrity checking
3. 200 V or 0 V Polarization voltage
4. High impedance input in power down
5. Hardware signal overload detection
6. Supports TEDS Class 1 and 2
7. AC and DC coupled mode in both differential and single-ended mode

# chapter four

## MIC42X continued

MIC42X Functionality per Channel



### DETAILED FEATURE DESCRIPTION

#### 1. Analog / Microphone Input Mode

In this mode the Module input is a voltage with the highest input range being  $\pm 12$  V. There are 3 hardware input ranges, namely  $\pm 12$  V,  $\pm 1.2$  V and  $\pm 120$  mV. Two different input biasing modes are available in this mode, namely differential and single-ended. In single-ended mode the negative input is connected directly to the ground (AGNDM) of the Module, in differential mode the inputs are equally biased to allow a fully differential signal. Both AC and DC coupling are available in this mode.

# getting to know the PAK MKII

## 2. ICP® Mode

A 4mA current is supplied as required by the ICP® sensors. In this mode AC coupling is always enabled, and all the hardware gain ranges are available. Note that the 4 mA current source has a compliance voltage of  $\pm 11$  V (22 V total).

## 3. AC/DC Coupling

AC/DC coupling is supported in both single-ended and differential input mode. When AC mode is enabled (selectable in ALI mode, always enabled for ICP® mode) the -3 dB cutoff frequency of the filter is approximately 0.16 Hz.

## 4. Pre-amplifier and Polarization Supply Voltage

The buffer amplifiers on the Module are powered by  $\pm 14.5$  V. The same  $\pm 14.5$  V is connected to positive and negative excitation pins on the Lemo connector for microphone power and excitation. The excitation voltage is always on and cannot be turned off. The microphone polarization voltage can be set to either +200 V or 0 V.

## 5. TEDS

The TEDS circuitry fully complies with the IEEE 1451.4 (V0.9, V1.0) standard. Microphones utilize pin 5 of the Lemo connector as a dedicated TEDS pin. Both class 1 and class 2 TEDS are supported. For ICP® sensors the positive input terminal (signal+) is connected to the TEDS I/O line and the negative terminal (signal-) is connected to the Module Ground (AGNDM).

## 6. High Impedance at Power Down

The Module will switch to a high impedance mode at power down.

## 7. ICP® Integrity Checking and Overvoltage Detection

In ICP® mode, the integrity checking circuit will detect the following errors:

- Short circuit between signal+ and signal- inputs
- Short circuit between signal- and ground (CGND or AGNDM)
- Open circuit between signal+ and signal- inputs

The overvoltage detection comparators will detect an overload condition at the ADC's inputs.

The overload detection level is adjustable via software.

## 8. AGNDM to GND Switch

When closed this switch connects AGNDM (isolated ground) to GND (non-isolated ground). GND is in turn connected to CGND (Chassis Ground). When open (default state) AGNDM is galvanically isolated from GND. The switch is software controlled.

## MIC42X

continued

# chapter four

## MIC42X Features

Parameter	Mode	Value
Module Connector		Lemo EGG.1B.307.CLN (Pin out for B&K Falcon pre-amplifier)
Channels		2 Input
Polarization Voltage		0 or 200 V $\pm 1\%$ (typical)
Pre-amplifier Excitation Voltage		$\pm 14.5$ V
Interface	ALI	Analog voltage sources
	ICP®	ICP® sensors, 4 mA excitation, 22 V compliance
Coupling	ALI	DC or AC
	ICP®	AC
AC Coupling	ICP®/ALI	-3 dB cutoff is 0.16 Hz
Input Bias	ALI	Differential, single-ended to Module Ground (isolated), single-ended to Chassis Ground (non-isolated)
	ICP®	Differential
Input Voltage Range		$\pm 12$ V, $\pm 1.2$ V, $\pm 120$ mV
Input Impedance		$2 \text{ M}\Omega    2.2 \text{ nF}$ (Differential Input Mode) $1 \text{ M}\Omega    2.2 \text{ nF}$ (Single-Ended Input Mode)
DC Offset <small>Note 2, 10</small>	ICP®/ALI	900 $\mu\text{V}(\pm 12 \text{ V})$ , 900 $\mu\text{V}(\pm 1.2 \text{ V})$ , 900 $\mu\text{V}(\pm 120 \text{ mV})$
Maximum Sampling Rate per Channel (fs)		204.8 kHz
Other Sampling Rates		Available through digital LP filters and decimation
Onboard ADC		2x Sigma-Delta
Resolution		24 bit
Digital HP Filter <small>Note 1</small>		-3 dB at 1 Hz, -0.1 dB at 6.5 Hz (fs=48 kSa/s, 96 kSa/s, 192 kSa/s) Filter scales with sampling rate

# getting to know the PAK MKII

## MIC42X Features continued

Parameter	Mode	Value
<b>Digital LP Filter</b> Note 1		Passband = $0.45^*fs$ Stopband = $0.55^*fs$ Passband ripple = $\pm 0.001$ dB ( $fs \leq 48$ kHz) $\pm 0.003$ dB ( $fs = 96$ kHz) $\pm 0.007$ dB ( $fs = 192$ kHz) Stopband attenuation = 120 dB ( $fs \geq 48$ kHz) Stopband attenuation = 80 dB ( $fs < 48$ kHz)
<b>Optional Programmable Digital IIR Filter</b>		Band pass/stop: 6 dB/Octave High/Low pass: 12 dB/Octave
<b>SNR</b> ( $fs = 48$ kHz) Note 2, 3, 10		150 dB ( $\pm 12$ V), 146 dB ( $\pm 1.2$ V), 134 dB ( $\pm 120$ mV)
<b>THD</b> ( $fs = 48$ kHz) Note 2, 4, 10		101 dB ( $\pm 12$ V), 103 dB ( $\pm 1.2$ V), 106 dB ( $\pm 120$ mV)
<b>SFDR<sub>IV</sub></b> ( $fs = 48$ kHz) Note 2, 5, 10, 12		131 dB ( $\pm 12$ V), 146 dB ( $\pm 1.2$ V), 152 dB ( $\pm 120$ mV)
<b>SFDR<sub>I0V</sub></b> ( $fs = 48$ kHz) Note 2, 5, 10, 13		151 dB ( $\pm 12$ V), 166 dB ( $\pm 1.2$ V), 172 dB ( $\pm 120$ mV)
<b>SFDR<sub>H</sub></b> ( $fs = 48$ kHz) Note 2, 6, 10, 12		103 dB ( $\pm 12$ V), 104 dB ( $\pm 1.2$ V), 108 dB ( $\pm 120$ mV)
<b>Crosstalk</b> ( $fs = 48$ kHz) Note 2, 7, 10		113 dB ( $\pm 12$ V), 126 dB ( $\pm 1.2$ V), 131 dB ( $\pm 120$ mV)
<b>Noise Floor</b> ( $fs = 48$ kHz) Note 2, 8, 10, 12		-135 dB ( $\pm 12$ V), -151 dB ( $\pm 1.2$ V), -159 dB ( $\pm 120$ mV)
<b>Range Accuracy</b> Note 9, 10		0.02% ( $\pm 12$ V), 0.04% ( $\pm 1.2$ V), 0.12% ( $\pm 120$ mV)
<b>Phase Accuracy</b>		< 0.2° at 10 kHz
<b>Module Calibration</b>		Internal amplitude and phase calibration
<b>Test Voltage Output</b>		Supplied from front panel connector pin 1
<b>Protection</b>		2 kV ESD
<b>Galvanic Isolation</b>		50 V
<b>TEDS</b> Note 11		IEEE 1451.4 V0.9, V1.0 Class 1 and Class 2

# chapter four

## MIC42X Features continued

The different parameter values mentioned in the features table are all software-selectable.

*Note 1:* Digital filters form part of the onboard ADC. Channels 1 and 2 are converted by the 2-channel sigma-delta ADC and thus share the same HP and LP filter setup.

*Note 2:* Measured after Module auto calibration has been applied.

*Note 3:* Signal to Noise Ratio (SNR): The ratio of the rms signal amplitude to the rms noise value excluding harmonics. Input signals are  $7.5 \text{ V}_{\text{amplitude}}$  ( $\pm 12 \text{ V Range}$ ),  $750 \text{ mV}_{\text{amplitude}}$  ( $\pm 1.2 \text{ V Range}$ ) and  $75 \text{ mV}_{\text{amplitude}}$  ( $\pm 120 \text{ mV Range}$ ) @ 1 kHz.

*Note 4:* Total Harmonic Distortion (THD): The ratio of the root-sum-squares of the first 10 harmonic amplitudes to the fundamental signal amplitude. Input signals are  $7.5 \text{ V}_{\text{amplitude}}$  ( $\pm 12 \text{ V Range}$ ),  $750 \text{ mV}_{\text{amplitude}}$  ( $\pm 1.2 \text{ V Range}$ ) and  $75 \text{ mV}_{\text{amplitude}}$  ( $\pm 120 \text{ mV Range}$ ) @ 1 kHz.

*Note 5:* Spurious Free Dynamic Range (SFDR): The ratio of the full scale input to the amplitude of the largest spurious spectral component (Inputs terminated with a short circuit. Measurement bandwidth: 100 Hz to fs / 2 excluding harmonics).

*Note 6:* Spurious Free Dynamic Range (SFDR<sub>H</sub>): The ratio of the fundamental signal amplitude to the amplitude of the highest peak including the first and all other harmonics. Measurement bandwidth: 100 Hz to fs / 2. Input signals are  $7.5 \text{ V}_{\text{amplitude}}$  ( $\pm 12 \text{ V Range}$ ),  $750 \text{ mV}_{\text{amplitude}}$  ( $\pm 1.2 \text{ V Range}$ ) and  $75 \text{ mV}_{\text{amplitude}}$  ( $\pm 120 \text{ mV Range}$ ) @ 1 kHz.

*Note 7:* Crosstalk: Signal is played into a channel while the remaining channels are short circuited. The crosstalk is the ratio of the fundamental signal amplitude of the input channel to the signal amplitude at the fundamental frequency on the remaining channels. Input signals are  $7.5 \text{ V}_{\text{amplitude}}$  ( $\pm 12 \text{ V Range}$ ),  $750 \text{ mV}_{\text{amplitude}}$  ( $\pm 1.2 \text{ V Range}$ ) and  $75 \text{ mV}_{\text{amplitude}}$  ( $\pm 120 \text{ mV Range}$ ) @ 1 kHz.

*Note 8:* Noise Floor: The rms noise value specified in dB when the inputs are terminated with a short circuit.

*Note 9:* Range Accuracy measured at 1 kHz.

*Note 10:* Listed values are typical measurement values.

*Note 11:* TEDS V1.0 available with firmware upgrade.

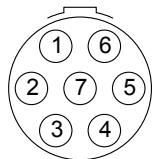
*Note 12:* 0 dB is equal to 1 V.

*Note 13:* 0 dB is equal to 10 V.

# getting to know the PAK MKII

## CONNECTOR PIN DEFINITIONS

Microphone manufacturers use their own pin definitions for microphone cables that connect their pre-amplifiers to instrumentation systems. The MIC Module was designed to be compatible with the B&K pre-amplifiers. Take care on the pin definitions when a different microphone pre-amplifier is used.



Pin definitions of a MIC42X Module 7-pin Lemo connector (when looking into the connector).

## MIC42X

continued

Pin	Function		
Mode	Microphone	ALI	ICP®
1 - Output	Microphone Calibration Output	-	-
2 - Input	Signal Ground (AGNDM in single-ended mode)	Signal- Input (AGNDM in single-ended mode)	Signal- Input (AGNDM in single-ended mode)
3 - Output	Polarization Voltage	-	-
4 - Input (Input/Output)	Signal+ Input	Signal+ Input (TEDS)	Signal+ Input 4 mA source (TEDS)
5 - Input/Output	TEDS	-	-
6 - Output	Positive Excitation Voltage	-	-
7 - Output	Negative Excitation Voltage	-	-

### NOTE:

A patch cable (010K) with broken shield is available. This cable could help to reduce noise in situations where the microphone measurement is sensitive to the PAK MKII grounding setup.

# chapter four

## Comparison of Pin Definitions for different Manufacturers with MIC Module

Pin Number	MIC Module	MTG MV 204	MTG MV 203	Norsonic 1201	GRAS 16 AJ	B&K 2669 L&C Lemo 0B
Pin 1:	Calibration Output Note 1	Heater supply	Heater supply	Heater supply	Not used	Calibration Input
Pin 2:	Signal ground Note 2	Microphone housing	Microphone housing	Signal ground	Signal ground	Signal ground
Pin 3:	Polarization Voltage Note 3	Free	Polarization voltage 200 V	Polarization voltage 200 V	Polarization voltage 200 V	Polarization voltage 200 V
Pin 4:	Signal In Note 4	Signal out	Signal out	Signal out	Signal out	Signal out
Pin 5:	TEDS Note 5	V2 Supply 28 V	V2 Supply 28 V	V1 Supply 15 V	Not used	Not connected
Pin 6:	Excitation Positive Note 6	V1 Supply 28...130 V	V1 Supply 28...130 V	Power supply positive 15...120 V ( $\pm 15$ to $\pm 60$ V)	Power supply positive 28...120 V	Power supply positive 28...120 V ( $\pm 14$ to $\pm 60$ V)
Pin 7:	Excitation Negative Note 6	0 V	0 V	Power supply negative / ground ( $\pm 15$ to $\pm 60$ V)	Power Ground	Power supply negative / ground ( $\pm 14$ to $\pm 60$ V)

MTG: Microtech Gefell GmbH, Germany

Norsonic: Norsonic AS, Norway

GRAS: G.R.A.S. Sound & Vibration A/S, Denmark

B&K: Brüel&Kjaer Sound & Vibration Measurement A/S, Denmark

**Note 1:** The calibration pin is a voltage output pin for the MIC42X. As such, when using the MTG and Nortronik microphone preamplifiers the corresponding pin should be disconnected in the cable connector to prevent a short circuit in the MIC42X calibration output .

**Note 2:** In single-ended mode this pin is internally connected to signal ground. In differential mode this pin is not connected to signal ground and becomes the negative input of the differential amplifier.

**Note 3:** The polarization voltage pin of the MIC42X is compatible with all microphone pre-amplifiers. The MIC Module is capable of switching this voltage off.

**Note 4:** This is the positive signal input pin of the MIC42X Module in both single-ended and differential mode.

**Note 5:** This pin is the TEDS micro-LAN pin of the MIC42X. The TEDS functionality is supported by certain B&K microphone pre-amplifiers. For the MTG and Nortronik microphone pre-amplifiers, the corresponding pin should be disconnected from the cable connector.

**Note 6:** These pins are designed as a dual power supply for a microphone pre-amplifier. All the mentioned manufacturers' microphone preamplifiers are capable of functioning with dual supplies. It has been confirmed that the microphone pre-amplifiers will function correctly at the  $\pm 14.5$  V (+29 V) supply of the MIC42X.

# getting to know the PAK MKII

## 4 Channel Analog Output

## ALO Module

---

### DESCRIPTION

The ALO4x Module provides 4 output channels for generating analog signals. The signals can be streamed down from PAK Software, or basic signals (square, sine, triangular, white noise, etc.) can be generated by the SC4x card.

Each channel may be configured to generate a different frequency and waveform with an output impedance per channel of  $10\ \Omega$ .

### TYPES

1. ALO42S

# chapter four

## ALO42S



### NOTE:

The ALO42S requires an SC42S to achieve 204.8 kSa/s.

The ALO42S provides:

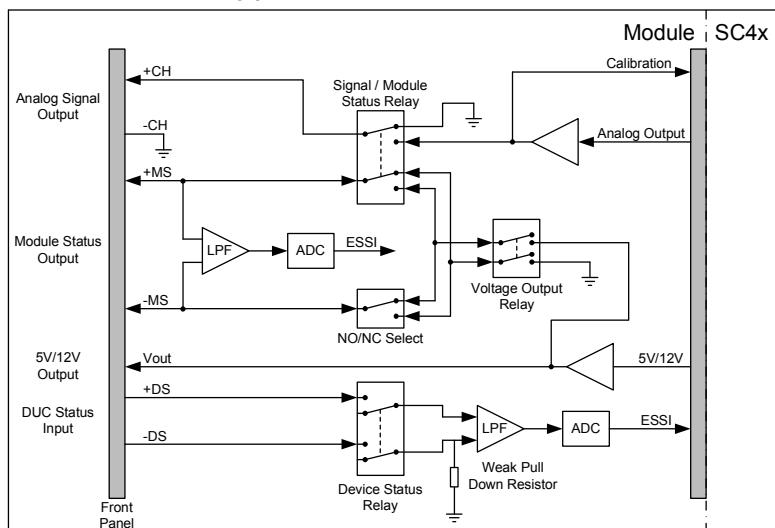
1. 24-bit 204.8 kSa/s on all 4 channels simultaneously
2. High signal quality
3. Safety features (for future use)

The ALO42S Module makes its own Module Status (MS) available to the Device Under Control (DUC). The DUC can detect if the ALO42S Module Status goes bad and then handle the fault condition safely. The ALO42S Module can also monitor the DUC on the DUC status input pins.

### NOTE:

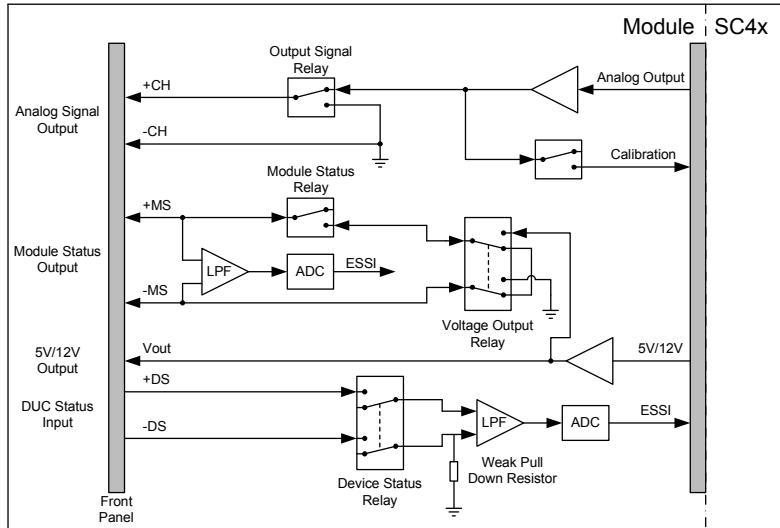
The ALO42S2 has been replaced by the ALO42S3.

### ALO42S2 Functionality per Channel



# getting to know the PAK MKII

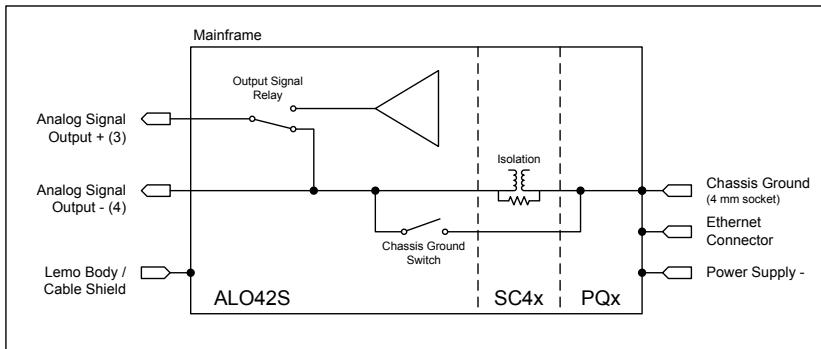
## ALO42S3 Functionality per Channel



## NOTE:

The ALO42S3 has the Module Status Relay separated from the Output Signal Relay. This allows the Module Status Relay to trigger immediately upon a failure, while the PAK MKII attempts to fade out the Analog Output Signal in a controlled manner.

## ALO42S Grounding Diagram

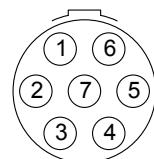


# chapter four

## ALO42S

continued

### CONNECTOR PIN DEFINITION



Pin definitions for ALO42S (when looking into the connector)

#### NOTE:

The QBNC11 SubModule is available to convert the signals to 4 BNC connectors.

Pin Number	Definition
1	Module Status Output +
2	DUC Status Input +
3	Analog Signal Output +
4	Analog Signal Output -
5	DUC Status Input -
6	Module Status Output -
7	5 V/12 V

Signal Pairs	
Module Status Output +	Module Status Output -
DUC Status Input +	DUC Status Input -
Analog Signal Output +	Analog Signal Output -
5 V/12 V	Analog Signal Output -

# getting to know the PAK MKII

## ALO42S Features

Parameter	Value
Module Connector	Lemo EHG.0B.307
Channels	4 Channels each with: <ul style="list-style-type: none"> <li>• Analog Signal Output (Pins 3 &amp; 4)</li> <li>• Module Status Output (Pins 1 &amp; 6)</li> <li>• Device Under Control Status Input (Pins 2 &amp; 5)</li> <li>• 5V/12V DC Voltage Output (Pins 7 &amp; 4)</li> </ul>
Galvanic Isolation	50 V
Protection	ESD & EMI
Output Voltage Range	±10 V
Sampling Rate	204.8 kSa/s
Sampling Resolution	24 bits
Output Impedance	10 Ω
Output Current	30 mA (max)
Bandwidth -0.1 dB Note 1, 2	20 kHz
Bandwidth -0.3 dB Note 1, 2	35 kHz
SFDR <sub>H</sub> Note 1, 2, 3, 4	114 dB
THD Note 1, 2, 4, 5	107 dB
SNR Note 1, 2, 4, 6	125 dB
FFT Noise Floor Note 1, 2, 4, 7	-136 dB
Crosstalk Note 8	122 dB
SC Generated Signals	Square Sine Triangular DC White noise

The different parameter values mentioned in the features table are all software-selectable.

# chapter four

## ALO42S Features continued

Note 1: ALO42S generating a 1 kHz 1 V amplitude signal at DF = 2, MSR 192000.

Note 2: 0 dB = 1 V amplitude.

Note 3: Spurious Free Dynamic Range ( $SFDR_H$ ): The ratio of the fundamental signal amplitude to the amplitude of the highest peak including the first and all other harmonics. Measurement bandwidth 20 Hz to 48 kHz.

Note 4: Measured using ICP Module in 1.5 V differential range at DF = 2, MSR 192000.

Note 5: Total Harmonic Distortion (THD): The ratio of the root-sum-squares of the harmonic amplitudes to the fundamental signal amplitude.

Note 6: Signal to Noise Ratio (SNR): The ratio of the RMS signal amplitude to the RMS noise value excluding harmonics.

Note 7: FFT Noise Floor is defined as the FFT processing gain added to the SNR.

Note 8: The crosstalk is measured by generating a 1 kHz signal on one channel, and measuring its presence on any other channel which is generating a 0 V signal.

Parameter	Module Status Output
Module Status Options	Relay (recommended) / DC Voltage Output
Module Status Good	Closed relay / DC Voltage output
Module Status Bad	Open relay / No voltage output
Input Voltage Range	0 V to 24 V
Output Voltage	5 V or 12 V (15 mA max)

Parameter	DUC Status Input
Input Voltage Range	0 V to 24 V
Sampling Rate	15.6 kSa/s
Sampling Resolution	12 bits
Bandwidth (-3 dB)	15.9 kHz

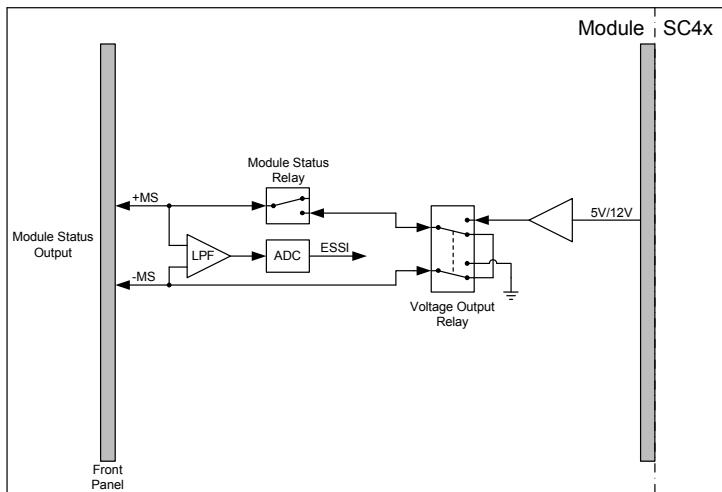
Parameter	5V/12V DC Voltage Output
Output Voltage	5 V or 12 V
Output Current	15 mA

# getting to know the PAK MKII

## MODULE STATUS

The Module Status (MS) of the ALO42S is available. The Device Under Control (DUC) can monitor the MS and perform a controlled shutdown if the ALO42S indicates that a fault condition occurred.

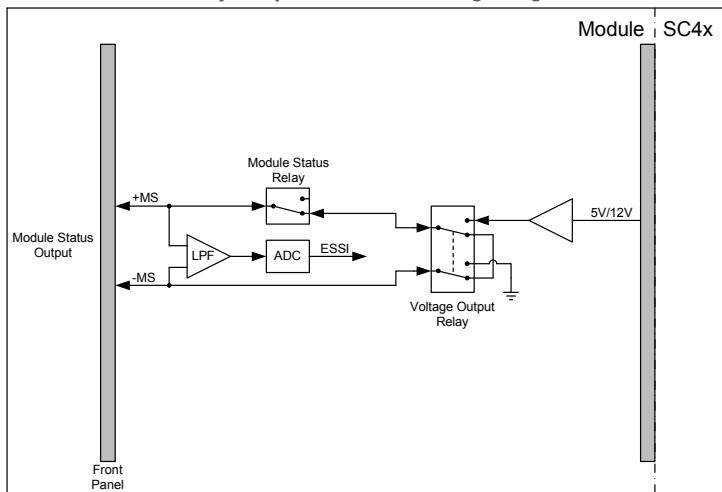
### Module Status: Default Condition (Fault or MS bad)



## ALO42S

continued

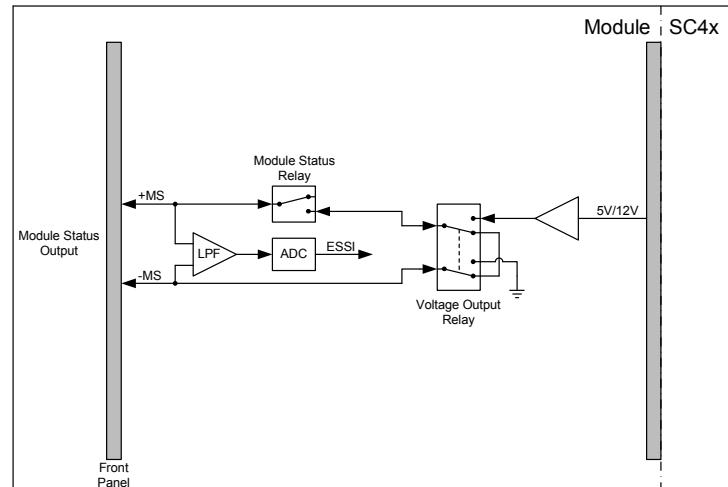
### Module Status: Relay Output Mode indicating MS good



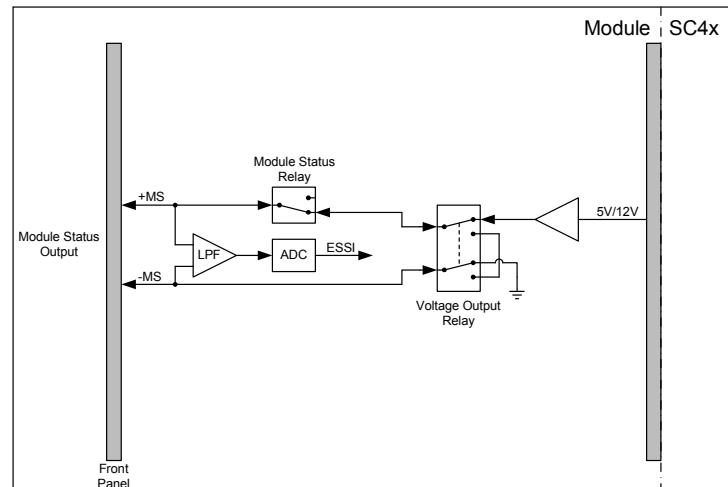
# chapter four

ALO42S  
continued

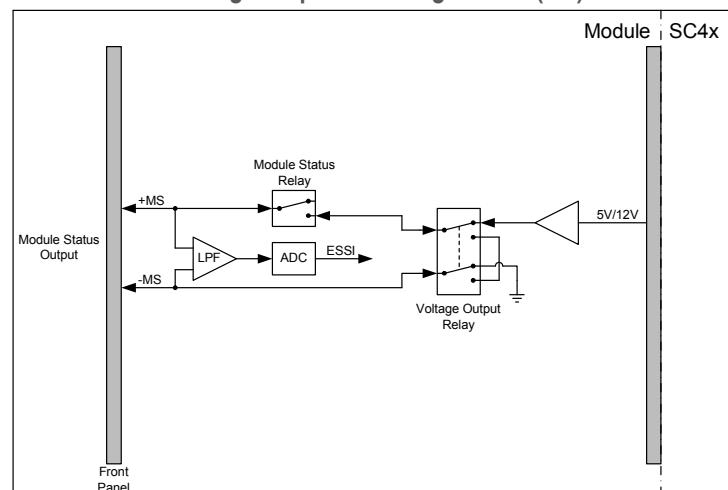
Module Status: Relay Output Mode indicating MS bad



Module Status: Voltage Output indicating MS good (choose 5 V or 12 V)



Module Status: Voltage Output indicating MS bad (0 V)

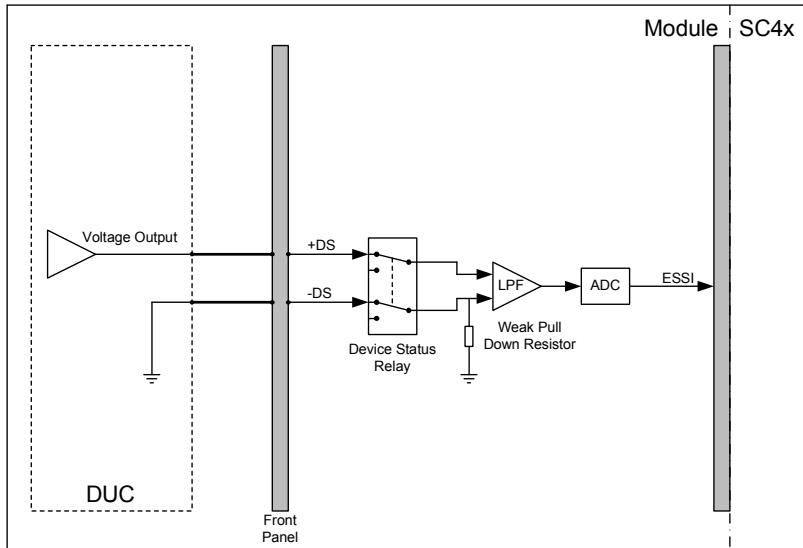


# getting to know the PAK MKII

## DEVICE STATUS

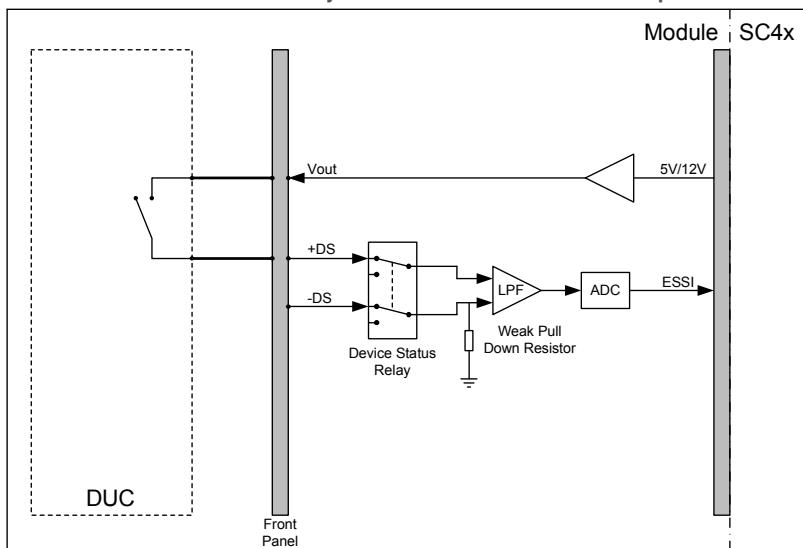
The device status of the DUC is monitored by the ALO42S Module.

### Device Status: DUC with a Voltage Output



**ALO42S**  
continued

### Device status: DUC with a relay needs the ALO42S 5V/12V output



## DAR Module

## 4 Channel Digital Audio Receiver

---

### NOTE:

- When both inputs of the DAR Module are allocated to a test, the frame rate for the inputs must be the same.
- When only one S/PDIF or AES3 signal will be received by a DAR Module during a test, it must be connected to input 1.

---

### DESCRIPTION

The DAR Module is able to receive 2 S/PDIF or AES3 digital audio streams. Each signal consists of a 2-channel pair (a left and right channel). In other words, the DAR Module has 4 input channels with the left channel of input 1 equal to the DAR Module channel 1 and the right channel of input 2 equal to the DAR Module channel 4.

Popular digital audio frame rates (96, 88.2, 48 and 44.1 kHz) are all supported. The following channel modes (which can be selected on a per-Module basis) exist:

1. *4CH mode* (4 Channel mode): S/PDIF or AES3 inputs 1 and 2 (channels 1 to 4) of the DAR Module support a maximum frame rate of 48 kHz.
2. *2CH mode* (2 Channel mode): S/PDIF or AES3 input 1 (channels 1 and 2) of the DAR Module supports a maximum frame rate of 96 kHz; channels 3 and 4 must be disabled.

### TYPES

1. DAR42 – with Lemo connectors

## 4 Channel Digital Audio Receiver

### DAR Module

continued

#### SYNC

The DAR42 Module transmits a synchronization (SYNC) signal from the front panel that will enable external digital audio transmitters to synchronize their digital audio transmission to the PAK MKII sample clock. If the digital audio signal received by the DAR Module is not synchronized to the PAK MKII sample clock, the following conditions may occur due to small differences in the digital audio transmitter and receiver clock frequencies:

1. *Underrun*: Transmitter clock frequency lower than PAK MKII sample clock frequency; the DAR Module forces synchronization to the PAK MKII sample clock by inserting zero-value samples as required
2. *Overrun*: Transmitter clock frequency higher than PAK MKII sample clock frequency; the DAR Module forces synchronization to the PAK MKII sample clock by rejecting samples when necessary

**The following SYNC signals can be provided by the DAR Module and are selectable by software:**

1. Word Clock
2. AES3 (sometimes referred to as AES/EBU) digital audio signal

The Word Clock is a TTL square wave signal with a duty cycle of 50 %. The positive clock edge indicates the start of the PAK MKII sample period.

## DAR Module

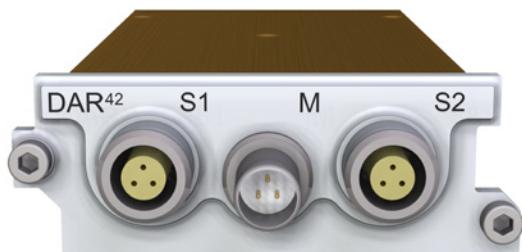
continued

**The AES3 signal has the following properties:**

1. Data is fixed at 0.
2. User and validity bits are fixed at 0.
3. Channel status information is implemented according to the “minimum” implementation as specified in the AES3 standard, which specifies that bit 0 of the channel status block is set to 1 for each channel. The rest of the channel status block is fixed at 0 except for the sampling frequency field (bits 6 and 7) that is set to the current AES3 frame rate.

After power-up or system reset the SYNC will be disabled. Smooth transition (no short pulses) occurs when switching between different SYNC signals. The SYNC signals of different DAR Modules in adjacent SC4x Module slots and even on separate SC4x boards are synchronized to each other in terms of frequency and phase.

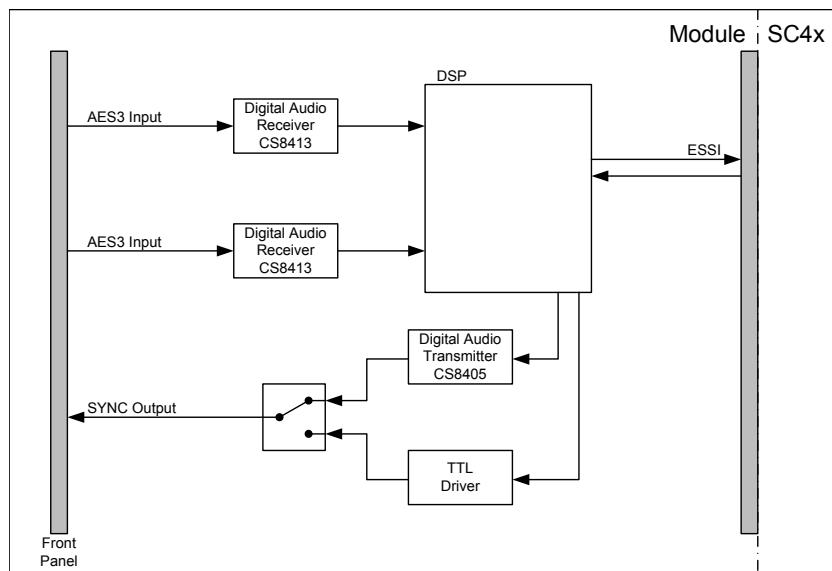
# getting to know the PAK MKII



DAR42

The DAR42 Module inputs comply with the professional interface specification of the digital audio standard. It is able to receive 2 AES3 digital audio streams. Each signal consists of a 2-channel pair (a left and right channel). The channel status, User and validity information of each AES3 signal are ignored – only the data section of each sub-frame will be passed on as a data sample to the rest of the PAK MKII system.

## DAR42 Module Functionality



# chapter four

## DAR42 Module AES3 Input Features

Parameter	Mode	Value
Module Connector		Lemo EGG.0B.303.CLN
Channel		2 inputs
Interface		AES3
Termination		110 Ω
Differential Input Voltage Range		200 mVp-p minimum
Common Mode Input Range		±7 V
Frame Rate	4CH mode	44.1, 48 kHz
	2CH mode	44.1, 48, 88.2, 96 kHz
Sample Width		16/20/24-bit
Protection		2 kV ESD
Galvanic Isolation		50 V, through capacitive coupling
Word Clock Delay Note 1		30 ns (maximum)
AES3 Delay Note 2		600 ns (typical)

The different parameter values mentioned in the features table are all software-selectable.

**Note 1:** The delay between the start of the PAK MKII sample period and a Word Clock positive edge.

**Note 2:** The delay between the start of the PAK MKII sample period and an AES3 frame start.

# getting to know the PAK MKII

## DAR42 Module SYNC Output Features

Parameter	Mode	Value
Module Connector		Lemo FAG.0B.303.CLA
Channel		1
Interface	Word Clock	TTL low-impedance output, single-ended
	AES3	AES3 transformer-coupled
Voltage Output	Word Clock	5.5 V (peak-to-peak, cable unterminated)
	AES3	3.5 V (peak-to-peak, cable unterminated)
Termination	Word Clock	75 Ω
	AES3	110 Ω
Frequency Range Note 1	Word Clock	44.1, 48, 88.2, 96 kHz
	AES3	44.1, 48 kHz
Protection		2 kV ESD
Galvanic Isolation	Word Clock	No
	AES3	50 V, through transformer coupling

The different parameter values mentioned in the features table are all software-selectable.

*Note 1:* The SYNC frequency or frame rate depends on the frame rate selected for the S/PDIF inputs. When the S/PDIF frame rate is 44.1 or 88.2 kHz, the available Word Clock frequencies are 44.1 and 88.2 kHz and the available AES3 frame rate is 44.1 kHz. When the S/PDIF frame rate is 48 or 96 kHz, the available Word Clock frequencies are 48 and 96 kHz and the available AES3 frame rate is 48 kHz.

# chapter four

## DAR42

continued

### CONNECTOR PIN DEFINITIONS

The Lemo connector pins of DAR Input1 and DAR Input 2 in the figure below are defined in differential mode as follows:

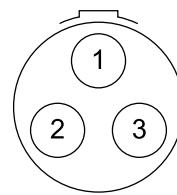
- Pin 1: Not connected
- Pin 2: Signal
- Pin 3: Signal

The Lemo connector pins of DAR Output 1 in the figure below are defined as follows for the TTL interface:

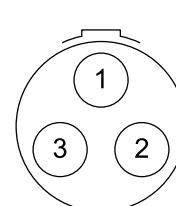
- Pin 1: Not connected
- Pin 2: Signal
- Pin 3: Ground

The Lemo connector pins of DAR Output 1 in the figure below are defined as follows for the AES3 interface:

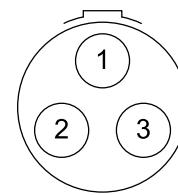
- Pin 1: Not connected
- Pin 2: Signal
- Pin 3: Signal



Input 1



Output 1



Input 2

**DAR42 Module pin definitions for the 3-pin Lemo connectors (when looking into the connectors)**

# getting to know the PAK MKII

## CONNECTING THE AES3 AND SYNC SIGNALS

When considering digital audio signals normally within the MHz range, the cable and termination impedances become important in ensuring the connection at maximum distance between digital audio transmitters and receivers is of a high standard. For shorter distances the exact matching of impedances becomes less crucial and the AES3 and SYNC connections should still work correctly with mismatched cable-, connector- and termination impedances. Note that a heavily distorted SYNC signal (due to mismatched impedances) may induce jitter into the digital audio transmitters.

The Lemo connectors on the DAR42 Module front panel must first be converted to the correct XLR or BNC connectors, to be compatible with the standard AES3 and Word Clock cables respectively. The required patch cables should be included with the received Module.

### AES3 to AES3

- Use standard AES3 audio cable with  $110 \Omega$  impedance and XLR connectors
- A Lemo-to-XLR (AES3 Input) patch cable must be used to connect the male XLR connectors from the AES3 transmitter to the input Lemo connector of the DAR42
- The Lemo pin 1 connector on the DAR42 Module is not connected, since it is recommended to only ground the cable shield at the AES3 transmitter side in order to prevent ground loops

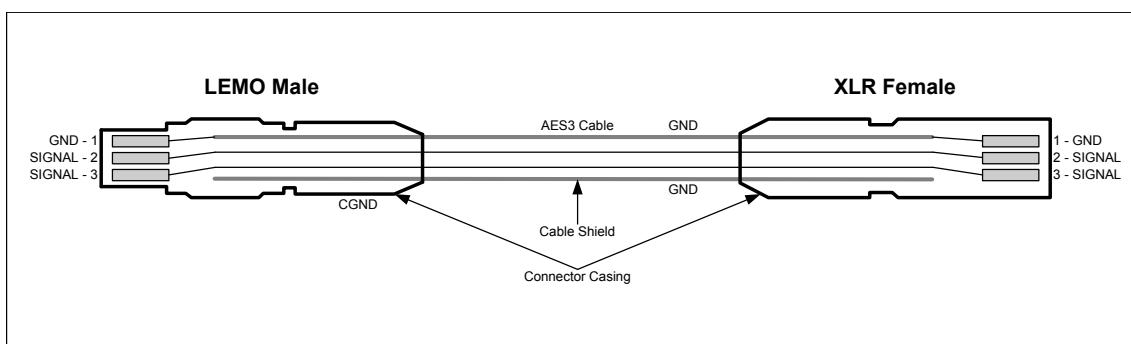
## DAR42

continued

## WARNING:

In order to prevent damage to the Module and / or degraded performance, do NOT use custom made patch cables.

### DAR42 Lemo-to-XLR Patch Cable for AES3 Input



# chapter four

## DAR42

continued

### NOTE:

The coaxial cable shield must be connected to DAR42 Module Ground (GND) and NOT the Lemo connector casing. There must be no contact between the coaxial cable shield and the Lemo connector casing.

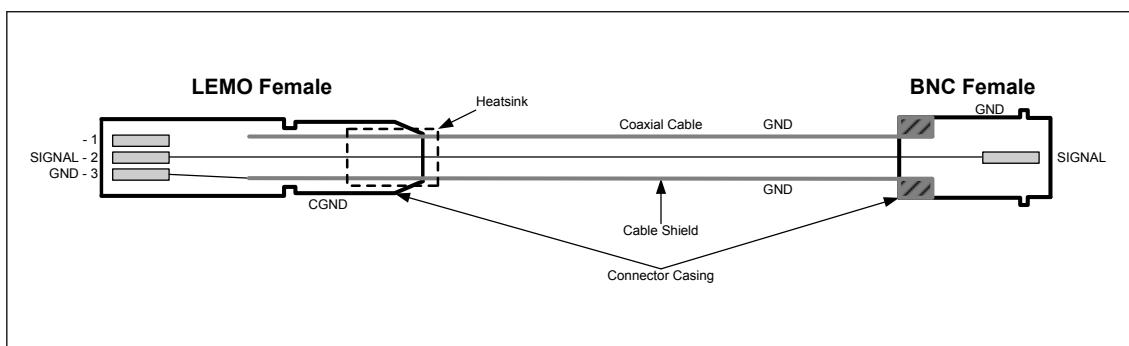
### S/PDIF to AES3

- An S/PDIF-to-AES3 converter, with  $75\ \Omega$  to  $110\ \Omega$  impedance matching, can be used to convert from an S/PDIF to an AES3 interface. The converter must not attenuate the S/PDIF digital audio signal
- The format of the received digital audio signal (consumer or professional) is ignored by the DAR42 Module
- It is recommended to attach the S/PDIF-to-AES3 converter to the digital audio transmitter S/PDIF output
- Should cable be required to transfer the S/PDIF signal (for instance when the converter is located close to the DAR42 Module input), use coaxial cable with  $75\ \Omega$  impedance
- The S/PDIF output impedance of a digital audio transmitter should be  $75\ \Omega$

### Word Clock SYNC

- When connecting the Word Clock to the Word Clock input of external digital audio transmitters, use coaxial cable with  $75\ \Omega$  impedance
- A Lemo-to-BNC patch cable must be used to connect the BNC female connector to the Lemo output connector of the DAR42
- The Word Clock is terminated with  $75\ \Omega$  on the DAR42 Module. This means that one end of the Word Clock cable must be located near the DAR42 Module (less than 0.5 m) with the other end of the cable terminated with  $75\ \Omega$  as well. The same Word Clock can be distributed to more than one digital audio transmitter's Word Clock input

### DAR42 Lemo-to-BNC Patch Cable for Word Clock Output



# getting to know the PAK MKII

## AES3 SYNC

- Use standard AES3 audio cable with  $110 \Omega$  impedance and XLR connectors
- A Lemo-to-XLR (AES3 Output) patch cable must be used to connect the female XLR connector from the AES3 SYNC receiver to the output Lemo connector of the DAR42
- The patch cable shield is not connected to DAR42 Module Ground but to the PAK MKII Chassis Ground via the Lemo connector casing. Therefore, it is suggested that the cable shield not be grounded at the AES3 SYNC receiver

## ADDITIONAL EXTERNAL CABLE REQUIREMENTS

If a cable with XLR connectors is used to connect between a DAR42 patch cable and external digital audio equipment, then this cable must have the following features:

- The XLR connectors must be XLR Female on one (TX) side and XLR Male on the other (RX) side
- The cable must be shielded and have one twisted pair inside
- The cable impedance must be  $110 \Omega$
- Pin 1 of each of the two XLR connectors must be connected to its cable shield as well as its connector casing

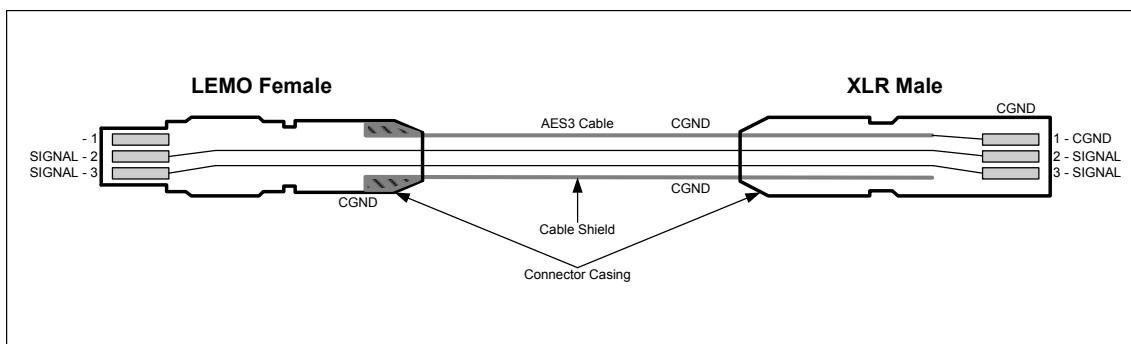
Any deviation from the above requirements may result in poor performance, ground loops or diminished EMC function. For short lengths of cable (i.e. up to 3 m), transmission will still be successful even if cables which do not meet all these requirements exactly are used.

Similarly, when a Word Clock signal is transmitted from the DAR Module to external digital audio equipment and cable lengths are long, it is required that a coaxial cable of  $75 \Omega$  impedance is used that has  $75 \Omega$  impedance BNC connectors.

## DAR42

continued

## DAR42 Lemo-to-XLR Patch Cable for AES3 Output



# chapter four

## CAN Module

## Dual independent CAN

### DESCRIPTION

The CAN Module provides an interface to connect to up to 2 independent Controller Area Networks (CAN). CAN is a robust differential serial communications protocol that is based on a multi-master bus configuration and is commonly used within automotive and general industrial environments. The CAN network consists of a single cable terminated at each end with terminating resistors (typically  $120\ \Omega$ ) with CAN nodes connected at non-fixed locations along the cable.

Each node usually contains a transceiver to convert differential CAN bus signal levels to normal bit stream levels. The bit stream is transmitted or received by a CAN Controller which acts as the CAN protocol handler of the node. Information is transmitted on the CAN bus using messages with the format defined by the CAN specification. These messages are referred to as CAN messages.

The CAN Module contains two channels that are implemented by its firmware to act as inputs or outputs, depending on the Module type (channel 1 – input/output 1; channel 2 – input/output 2).

### FEATURES

- Conformance with ISO 11898
- Conformance with CAN 2.0A and B which support 11-bit and 29-bit identifiers
- Each CAN input is galvanically isolated from the other CAN input as well as the rest of the PAK MKII
- Each CAN message received and accepted by the CAN Module will be time stamped in order to synchronize the received CAN messages with the rest of the measurement data

# getting to know the PAK MKII



CAN42

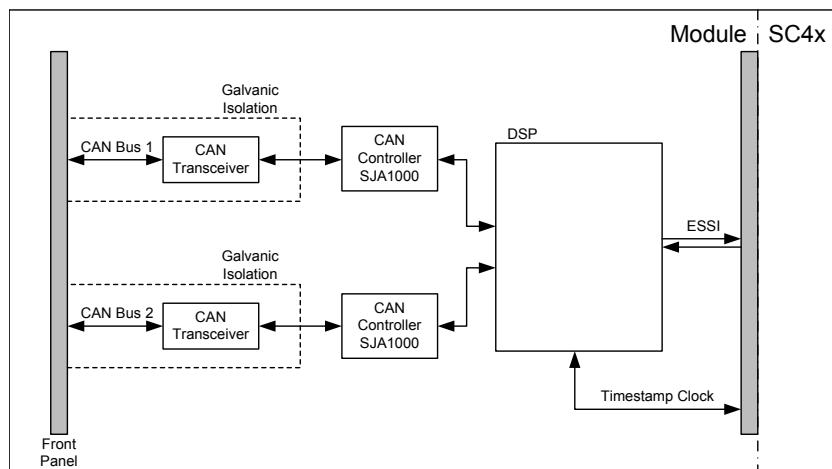
- Individually configurable identifier list per channel to provide acceptance filtering for all CAN messages received from the CAN bus
- Standard (11-bit) and Extended (29-bit) identifiers are supported
- Data and remote frames are supported

## TYPES

### 1. CAN42

The CAN42 Module can be configured to both transmit and receive messages (act as an active node), or to only receive messages (act as a passive node). The following figures and tables provides further insight into the CAN Module functionality and specifications.

### CAN Module Functionality



# chapter four

## CAN42 Features

Parameter	Value
Module Connector	RJ45 Female
Channels	2
CAN Bus Interaction Note 1	Passive and active mode supported
Interface	ISO 11898
Termination	None
CAN Transceiver	TJA1040
CAN Controller	SJA1000
CAN Controller Clock Frequency	16 MHz
CAN Bit Rate Range Note 2	10 kbit/s to 500 kbit/s (2 channels simultaneously) 1 Mbit/s (only channel 1)
Timestamp Resolution Note 3	5 µs to 7.8125 µs
Galvanic Isolation	50 V

The different parameter values mentioned in the features table are all software-selectable.

*Note 1:* Passive mode – messages are only received (without interacting with other nodes on bus). Active mode – messages are both transmitted and received.

*Note 2:* If the bus load on a 1 Mbit/s CAN bus increases to above 64 % for a period longer than 640 µs, the current CAN Module firmware may reject the CAN message due to internal throughput limitations.

*Note 3:* The timestamp clock is derived from the same SC4x clock reference as used by the SC4x for analog-to-digital conversion. Therefore, the timestamp resolution varies according to the sampling rates set for the other Modules in the same SC4x.

# getting to know the PAK MKII

## SJA1000 Bus Timing Register Values

CAN Bus Bit Rate	Bus Timing Registers		Description Note 1
	BTR0	BTR1	
10 kbit/s	0x31	0x1C	BRP = 49, SJW = 0 (1 $t_{scl}$ ), TSEG1 = 0xC (13 $t_{scl}$ ), TSEG2 = 0x1 (2 $t_{scl}$ ), Single sample point at 87.5 %
50 kbit/s	0x09	0x1C	BRP = 9, SJW = 0 (1 $t_{scl}$ ), TSEG1 = 0xC (13 $t_{scl}$ ), TSEG2 = 0x1 (2 $t_{scl}$ ), Single sample point at 87.5 %
100 kbit/s	0x03	0x2F	BRP = 3, SJW = 0 (1 $t_{scl}$ ), TSEG1 = 0xF (16 $t_{scl}$ ), TSEG2 = 0x2 (3 $t_{scl}$ ), Single sample point at 85 %
125 kbit/s	0x03	0x1C	BRP = 3, SJW = 0 (1 $t_{scl}$ ), TSEG1 = 0xC (13 $t_{scl}$ ), TSEG2 = 0x1 (2 $t_{scl}$ ), Single sample point at 87.5 %
250 kbit/s	0x01	0x1C	BRP = 1, SJW = 0 (1 $t_{scl}$ ), TSEG1 = 0xC (13 $t_{scl}$ ), TSEG2 = 0x1 (2 $t_{scl}$ ), Single sample point at 87.5 %
500 kbit/s	0x00	0x1C	BRP = 0, SJW = 0 (1 $t_{scl}$ ), TSEG1 = 0xC (13 $t_{scl}$ ), TSEG2 = 0x1 (2 $t_{scl}$ ), Single sample point at 87.5 %
1 Mbit/s	0x00	0x14	BRP = 0, SJW = 0 (1 $t_{scl}$ ), TSEG1 = 0x4 (5 $t_{scl}$ ), TSEG2 = 0x1 (2 $t_{scl}$ ), Single sample point at 75 %

Note 1:  $t_{scl}$  = CAN system clock period.

This period is derived from the SJA1000 clock frequency and the value of the BTR0 prescaler (1  $t_{scl}$  = 1 Time Quantum).

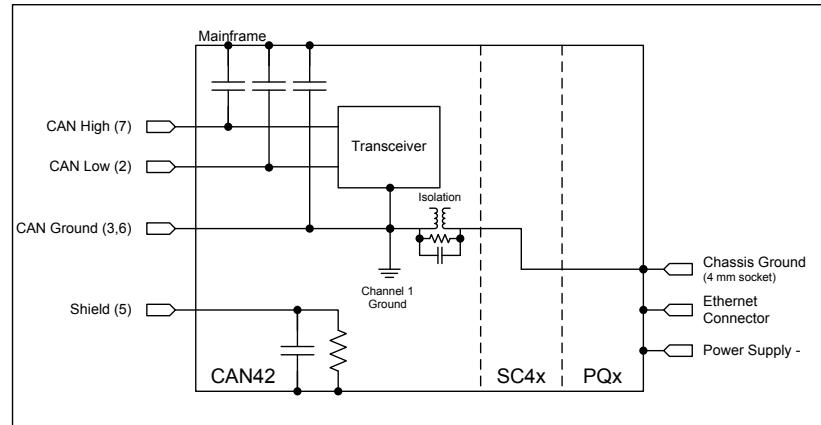
# chapter four

## CAN42 continued

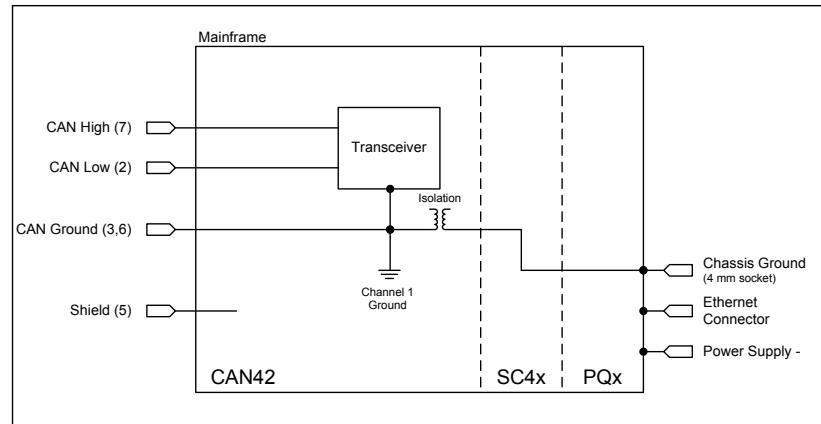
### NOTE:

As indicated in the figure, the CAN Ground pin of each node must be connected together and grounded to earth potential at a single point.

CAN42 Build A Grounding Diagram

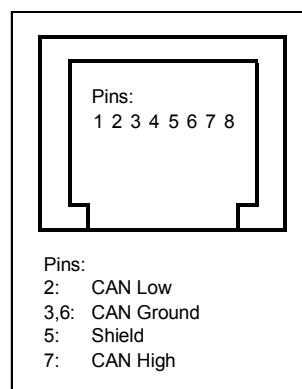


CAN42 Build B Grounding Diagram



### PIN DEFINITIONS

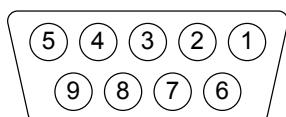
The CAN42 bus signals for each channel are available through an 8-pin RJ45 female connector with the pins defined below. All the other pins are not connected on the printed-circuit board.



Pin definitions of a CAN Module RJ45 connector (when looking into the connector)

# getting to know the PAK MKII

The connector is not pin compatible with the standard CAN RJ45 connector pin out. An adapter cable must be used with a CAN Module when interfacing to an external CAN network. For example when using 9-pin D-sub connectors to connect nodes on the CAN network, a RJ45 to 9-pin D-sub cable (as shown in the following section) can be used to connect the correct pins from the CAN Module to a CAN 9-pin D-sub connector. The pin numbering of a typical CAN female 9-pin D-sub connector is shown below.



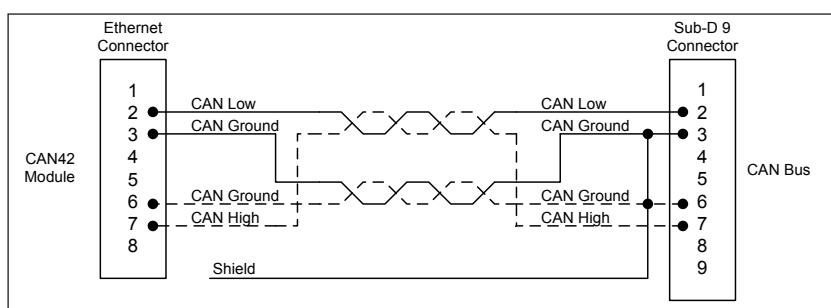
Pin definitions of a CAN 9-pin D-sub female connector (when looking into the connector)

## PINS

- |   |             |
|---|-------------|
| 1: Reserved   | 2: CAN Low  |
| 3: CAN GND  | 4: Reserved |
| 5: CAN Shield   | 6: CAN GND  |
| 7: CAN High   | 8: Reserved |
| 9: CAN V+ (Optional power on the CAN bus cable network – NOT implemented on the CAN4x Module) |             |

## CAN4X MODULE CABLE

The CAN4x Module was originally supplied with a green cable. This has been replaced with a blue cable with better EMI properties. CAN42 hardware build B (and newer) also has improved EMI properties.



Blue CAN4x Cable

## CAN BUS SETUP

The figure below shows a typical CAN bus setup. The network topology as defined by ISO 11898 is a single line structure terminated at both ends with a single termination resistor (typically  $120 \Omega$ ). This single line structure or CAN bus line has a maximum length which is determined by various factors such as the CAN bus bit rate. Note the difference between CAN bus line and stub cable.

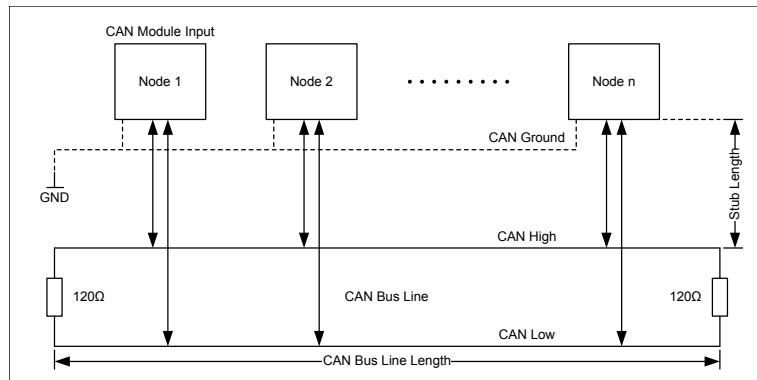
## CAN42

continued

# chapter four

## CAN42 continued

Typical CAN bus network setup



Some typical values for the maximum CAN bus line length related to the CAN bus bit rate are provided in the table.

Recommended Maximum CAN Bus Line Lengths

Bit Rate (kbit/s)	Bus Length (m)
1000	30
500	100
250	250
125	500

Multiple nodes can be connected to the bus via unterminated drop cables or stub cables. As indicated in the figure, the CAN Ground pin of each node must be connected together and grounded to earth potential at a single point. This is to ensure that the CAN High and CAN Low signals are all referenced to the same ground potential. To minimize reflections and standing waves which adversely affect signal integrity, the stub cable lengths must be kept as short as possible, the cable tail lengths should not be the same and the nodes on the network should also not be spaced equally. ISO 11898 specifies stub cable lengths (not bus lengths) of 0.3 m for a CAN bus operating at 1000 kbit/s, but this limitation is not always practical. Luckily receiver hysteresis and the synchronization rules of the CAN protocol allows for longer stub cable lengths. The maximum stub cable lengths are essentially determined by the bit timing parameters, the CAN bus line length and the accumulated stub cable length. The NXP CAN transceiver application note (see NXP's website) gives us rule-of-thumb formulas that can be used to specify the upper limit for the stub cable length and the upper limit for the cumulative stub cable length:

# getting to know the PAK MKII

$$L_U < t_{PROPSEG} - (50 \times t_p)$$

$$\sum_{i=1}^n L_{U_i} < t_{PROPSEG} - (10 \times t_p)$$

$t_{PROPSEG}$	The propagation segment of the bit period
$t_p$	Being the specific line delay per length unit (e.g. 5 ns/m)
$L_U$	Representing the length of the unterminated cable
$\sum_{i=1}^n L_{U_i}$	Cumulative stub cable length

## CAN42

continued

Please note that the actual propagation delay on the bus line should be calculated as the total CAN bus line length plus all stub cable lengths. This effectively leads to a reduction of the maximum CAN bus line length at a given bit rate. If the above recommendations are adhered to, the probability of reflection problems is considered to be fairly low. As an example:

Network bit rate	500 kbit/s
$t_{PROPSEG}$	$12 \times 125 \text{ ns} = 1500 \text{ ns}$
$t_p$	5 ns/m

Then an unterminated stub cable length of less than 6 m should be used, and the cumulative stub cable length should be less than 30 m for a propagation segment length of 1500 ns.

## WSB Module

## 4 Channel Wheatstone Bridge Input

### DESCRIPTION

The WSB Module provides 4 input channels for measuring analog signals from deflection bridge sensors (referred to as bridges below). Examples include LVDT, RVDT, synchro/resolvers, strain gauges, rope transducers, load cells, pressure sensors, etc. The main features of this Module are:

1. Resistive and inductive bridges
2. Full, half and quarter bridges
3. External and internal sensing
4.  $120\ \Omega$  and  $350\ \Omega$  bridges
5. Programmable DC excitation per channel (AC excitation only applicable to WSB42)
6. Module and bridge calibration

### TYPES

1. WSB42 with a 24-bit ADC and the following sampling limits:
  - $\leq 204.8\ \text{kHz}$  (24-bit) / channel for two channels
  - $\leq 204.8\ \text{kHz}$  (16-bit) / channel for all channels
  - $\leq 102.4\ \text{kHz}$  (24-bit) / channel for all channels

# getting to know the PAK MKII

## CALIBRATION METHODS

The WSB Module provides the following calibration methods:

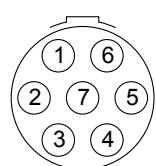
1. Bridge Balancing (for DC excitation only).
2. Bridge Calibration (for resistive bridges only). An internal calibration shunt resistor is available for bridge calibration. This resistor can be shunted on the Module between the Sense+ and Signal- lines.
3. Excitation Calibration. The WSB Module can utilize either external or internal sensing to measure and regulate the excitation voltage it supplies to a bridge. External sensing refers to a measurement setup where two additional wires (referred to as sense wires) are connected from the bridge to the WSB Module connector in order to allow the WSB Module to sense the excitation voltage at the bridge. This will enable the WSB Module to provide a more accurate excitation to the bridge especially when a long cable is used to connect the bridge to the WSB Module. Internal sensing refers to a measurement setup where no sense wires are connected between the bridge and the WSB Module. The excitation voltage can now only be measured on the Module. The WSB42 also has the ability to acquire the sense signal.
4. A quarter bridge completion resistor on the WSB Module can be selected as either 120 Ω or 350 Ω.

## CONNECTOR PIN DEFINITIONS

The WSB Module contains 4 Lemo connectors at the front panel (one connector per channel).

The pins for each connector are defined as follows:

- Pin 1: Excitation+
- Pin 2: Sense+
- Pin 3: Signal+
- Pin 4: Signal-
- Pin 5: Sense-
- Pin 6: Excitation-TEDS Return
- Pin 7: TEDS



Pin definitions of a WSB module 7-pin Lemo connector (when looking into the connector)

## WSB Module

continued

# chapter four

## CABLE INFORMATION

The table provides information for constructing a cable that can be used to connect an external deflection bridge sensor to an input of the WSB Module.

### WSB Module Cable and Connector Information

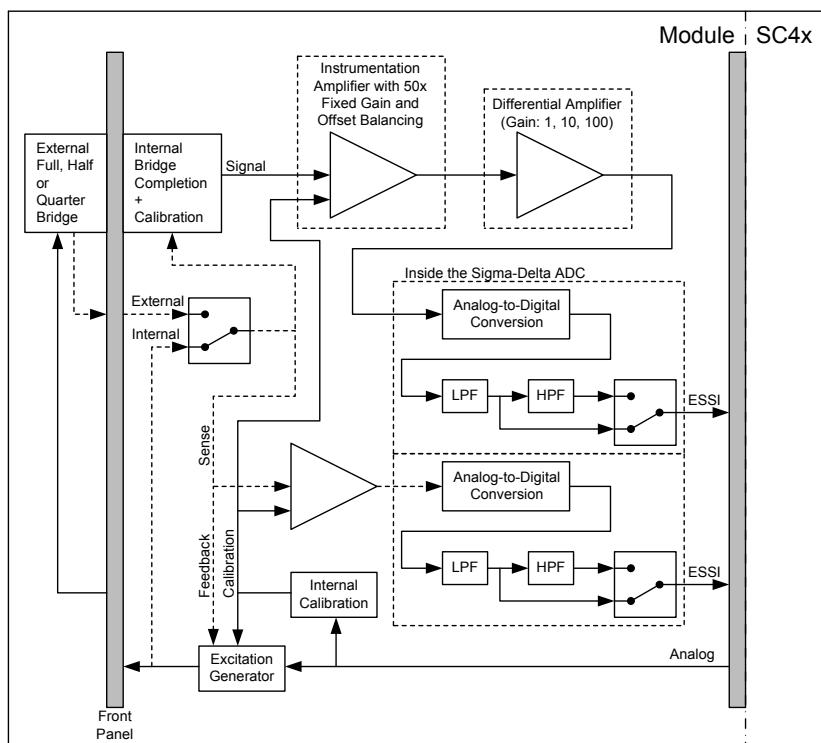
Parameter	Value		
Cable	CDT Nordic 0062743 (OD 4.6 mm)		
Connector	Lemo FGG.0B.307 CYCD52Z + GMA.0B.045.RA		
Connections	Cable Wire	Connector Pin	Pin Definition
	Twisted Pair 1	Brown	1
		Red	6
	Twisted Pair 2	Orange	2
		Yellow	5
	Twisted Pair 3	Green	3
		Blue	4
	Black	7	TEDS
	Screen	Connector Shell	Chassis Ground

# getting to know the PAK MKII



WSB42

## WSB42 Functionality per Channel



Each bridge and sense signal has a maximum sampling rate of 204.8 kHz. The sense signals can be used internal to the PAK MKII to fine tune the excitation voltage.

The excitation frequency must be the same for all channels of a WSB Module that utilizes AC excitation

The different modes and parameter values mentioned in the specifications table are all software-selectable. This includes the afore-mentioned calibration methods (these methods are carried out on a per-channel basis)

# chapter four

## WSB42 Specifications

### DC and AC Accuracy

Function	Range	Input Voltage	Error Specification ( $\pm$ % of range) $T_A = 23^\circ\text{C} \pm 5^\circ\text{C}$
DC Voltage	2 mV	2 mV	8.550
	20 mV	20 mV	0.600
	200 mV	200 mV	0.600
AC Voltage	2 mV	2 mV	3.460
	20 mV	20 mV	0.910
	200 mV	200 mV	0.900

Conditions:

- Within 30 minutes after “self calibration”
- Following the required 1 hour warm-up period of the PAK MKII
- Module Temperature of  $55^\circ\text{C} \pm 7^\circ\text{C}$
- $T_A$  : ambient temperature
- 90 Day Specifications of the Agilent 34410A are used

### Excitation Voltage Specifications

Function	Range	Error Specification ( $\pm$ % of range) $T_A = 23^\circ\text{C} \pm 5^\circ\text{C}$
DC Voltage	1 V	0.5
	2 V	0.4
	5 V	0.3

Conditions:

- Within 30 minutes after “self calibration”
- Following the required 1 hour warm-up period of the PAK MKII
- Module Temperature of  $55^\circ\text{C} \pm 7^\circ\text{C}$

# getting to know the PAK MKII

## WSB42 Specifications continued

- $T_A$  : ambient temperature
- 90 Day Specifications of the Agilent 34410A are used

### Bandwidth Specifications

The published attenuation values include the errors made during the measurement (DMM measurement errors) as well as errors made with the RMS calculation and represents the attenuation relative to the input voltage.

#### Bandwidth specification for a 204800 Hz sampling rate

Passband characteristics ( $f_s = 204800$ Hz)					
Parameter	Frequency (Hz)	Frequency Specification (Hz)		Attenuation (dB) $T_A = 23^\circ\text{C} \pm 5^\circ\text{C}$	
		Min	Max	Min	Max
Passband	100	-	100.01	-	0.029
	1000	-	1000.05	-	0.029
	51100	-	51103	-	0.200
	90000	-	90005	-	0.440
	95000	-	95005	-	0.560
	100500	-	100505	-	3.990
	106000	106000	-	14.800	-

Conditions:

- Within 30 minutes after “self calibration”
- Following the required 1 hour warm-up period of the PAK MKII
- Module Temperature of  $55^\circ\text{C} \pm 7^\circ\text{C}$
- $T_A$  : ambient temperature
- 90 Day Specifications of the Agilent 34410A are used

# chapter four

## WSB42 Specifications continued

Bandwidth specifications for a 102400 Hz sampling rate

Passband characteristics (fs = 102400 Hz)					
Parameter	Frequency (Hz)	Frequency Specification (Hz)		Attenuation (dB) $T_A = 23^\circ\text{C} \pm 5^\circ\text{C}$	
		Min	Max	Min	Max
Passband	100	-	100.01	-	0.029
	1000	-	1000.05	-	0.029
	25500	-	25502	-	0.064
	46600	-	46603	-	0.136
	47500	-	47503	-	0.200
	50150	-	50153	-	2.840
	53000	53000	-	16.900	-

Conditions:

- Within 30 minutes after “self calibration”
- Following the required 1 hour warm-up period of the PAK MKII
- Module Temperature of  $55^\circ\text{C} \pm 7^\circ\text{C}$
- $T_A$  : ambient temperature
- 90 Day Specifications of the Agilent 34410A are used

# getting to know the PAK MKII

## WSB42 Specifications continued

### Bandwidth specifications for a 51200 Hz sampling rate

Passband characteristics ( $f_s = 51200$ Hz)					
Parameter	Frequency (Hz)	Frequency Specification (Hz)		Attenuation (dB) $T_A = 23^\circ\text{C} \pm 5^\circ\text{C}$	
		Min	Max	Min	Max
Passband	100	-	100.01	-	0.029
	1000	-	1000.05	-	0.029
	25500	-	25502	-	0.064
	46600	-	46603	-	0.136
	47500	-	47503	-	0.200
	50150	-	50153	-	2.840
	53000	53000	-	16.900	-

Conditions:

- Within 30 minutes after “self calibration”
- Following the required 1 hour warm-up period of the PAK MKII
- Module Temperature of  $55^\circ\text{C} \pm 7^\circ\text{C}$
- $T_A$  : ambient temperature
- 90 Day Specifications of the Agilent 34410A are used

# chapter four

## WSB42 Features

Parameter	Mode	Value
Module Connector		Lemo EHG.0B.307.CLN
Channels		4 input
Bridge Configuration		Full, half or quarter
Bridge Type		Resistive or inductive
Quarter Bridge Completion Resistor		120 Ω or 350 Ω (internal to Module)
Calibration Shunt Resistor Note 12	Internal Sense	100 kΩ (maximum tolerance of 0.1 %)
	External Sense	100 kΩ (maximum tolerance of 0.1 %)
Excitation Frequency		DC to 5 kHz
Excitation Voltage Range		0 V to ±2.5 V (providing 0 V to 5.0 V across the bridge)
Excitation Current		200 mA (maximum)
Sense Options		External or internal
Input Voltage Range		±250 mV, ±25 mV, ±2.5 mV
Maximum Common Mode Voltage		±5 V
Bridge Balancing	DC excitation	±0.25 V (maximum)
Maximum Sampling Rate per Channel (fs)		204.8 kHz (per bridge or sense signal)

# getting to know the PAK MKII

## WSB42 Features continued

Parameter	Mode	Value
<b>Maximum Sampling Rate per Module</b>		409.6 kHz (Note 1)
<b>Other Sampling Rates</b>		Available through digital LP filters and decimation
<b>Onboard ADC</b>		8x sigma-delta
<b>Resolution</b>		16/24-bit
<b>Digital HP Filter</b>		-3 dB at $(21e-6 * fs)$ Hz, -0.1 dB at $(135e-6 * fs)$ Hz Filter scales with sampling rate for $fs \geq 48$ kHz
<b>Digital LP Filter</b>		Passband = $0.45 * fs$ Stopband = $0.55 * fs$ Passband ripple = $\pm 0.005$ dB, Stopband attenuation = 110 dB ( $fs \geq 48$ kHz) Stopband attenuation = 80 dB ( $fs < 48$ kHz)
<b>Optional Programmable Digital IIR Filter</b>		Band pass/stop : 6 dB/octave High/Low pass: 12 dB/octave
<b>SNR</b> ( $fs = 48$ kHz) Note 2, 3, 9		122 dB ( $\pm 250$ mV)
<b>THD</b> ( $fs = 48$ kHz) Note 2, 4, 9		89 dB ( $\pm 250$ mV)
<b>SFDR<sub>IV</sub></b> ( $fs = 48$ kHz) Note 2, 5, 9, 10		118 dB ( $\pm 250$ mV)
<b>SFDR<sub>10V</sub></b> ( $fs = 48$ kHz) Note 2, 5, 9, 11		138 dB ( $\pm 250$ mV)
<b>SFDR<sub>H</sub></b> ( $fs = 48$ kHz) Note 2, 6, 9, 10		94 dB ( $\pm 250$ mV)
<b>Crosstalk</b> ( $fs = 48$ kHz) Note 2, 7, 9		103 dB ( $\pm 250$ mV)
<b>Noise Floor</b> ( $fs = 48$ kHz) Note 2, 8, 9, 10		-133 dB ( $\pm 250$ mV)
<b>DC Offset</b> Note 2, 9		7 $\mu$ V ( $\pm 250$ mV)

# chapter four

## WSB42 Features continued

Parameter	Mode	Value
Phase Accuracy		0.2° at 10 kHz
Protection		2 kV ESD
Galvanic Isolation		50 V
TEDS		Support for IEEE 1451.4 Class 1

The different parameter values mentioned in the features table are all software-selectable.

*Note 1:* The WSB42 Module supports 819.2 kSa/s at 16-bit resolution when used in an SC42.

*Note 2:* Measured after Module auto calibration has been applied.

*Note 3:* Signal to Noise Ratio (SNR): The ratio of the rms signal amplitude to the rms noise value excluding harmonics. Input signals are 145 mV<sub>amplitude</sub> ( $\pm 250$  mV Range), 14.5 mV<sub>amplitude</sub> ( $\pm 25$  mV Range) and 1.45 mV<sub>amplitude</sub> ( $\pm 2.5$  mV Range) @ 1 kHz.

*Note 4:* Total Harmonic Distortion (THD): The ratio of the root-sum-squares of the first 10 harmonic amplitudes to the fundamental signal amplitude. Input signals are 145 mV<sub>amplitude</sub> ( $\pm 250$  mV Range), 14.5 mV<sub>amplitude</sub> ( $\pm 25$  mV Range) and 1.45 mV<sub>amplitude</sub> ( $\pm 2.5$  mV Range) @ 1 kHz.

*Note 5:* Spurious Free Dynamic Range (SFDR): The ratio of the full scale input to the amplitude of the largest spurious spectral component (Inputs terminated with a short circuit. Measurement bandwidth: 100 Hz to  $f_s / 2$  excluding harmonics).

*Note 6:* Spurious Free Dynamic Range (SFDR<sub>H</sub>): The ratio of the fundamental signal amplitude to the amplitude of the highest peak including the first and all other harmonics. Measurement bandwidth: 100 Hz to  $f_s / 2$ . Input signals are 145 mV<sub>amplitude</sub> ( $\pm 250$  mV Range), 14.5 mV<sub>amplitude</sub> ( $\pm 25$  mV Range) and 1.45 mV<sub>amplitude</sub> ( $\pm 2.5$  mV Range) @ 1 kHz.

*Note 7:* Crosstalk: Signal is played into a channel while the remaining channels are short circuited. The crosstalk is the ratio of the fundamental signal amplitude of the input channel to the signal amplitude at the fundamental frequency on the remaining channels. Input signals are 145 mV<sub>amplitude</sub> ( $\pm 250$  mV Range), 14.5 mV<sub>amplitude</sub> ( $\pm 25$  mV Range) and 1.45 mV<sub>amplitude</sub> ( $\pm 2.5$  mV Range) @ 1 kHz.

*Note 8:* Noise Floor: The rms noise value specified in dB when the inputs are terminated with a short circuit.

*Note 9:* Listed values are typical measurement values.

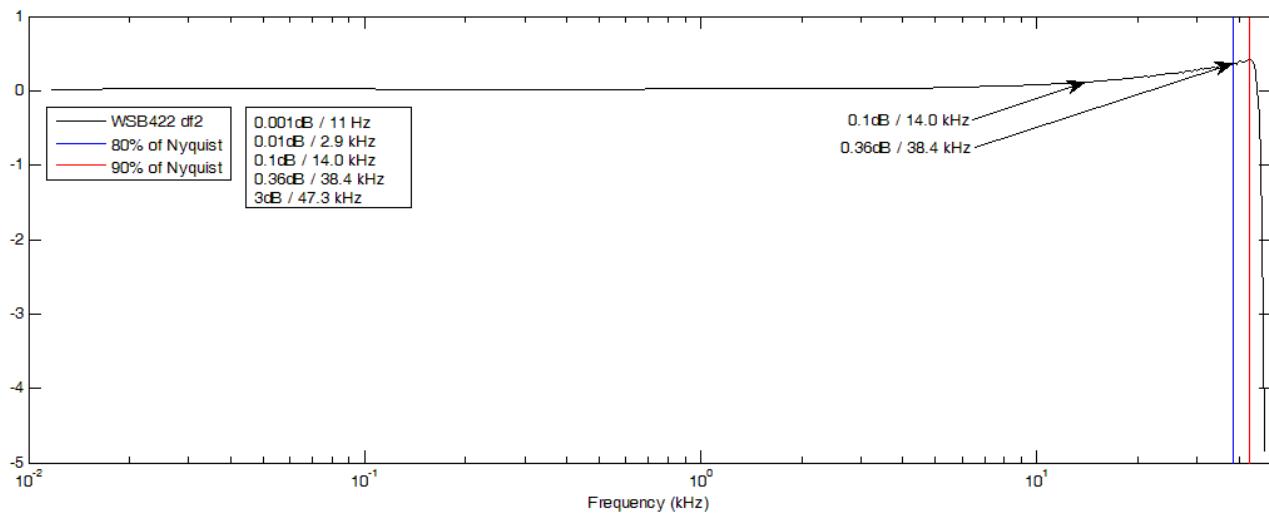
*Note 10:* 0 dB is equal to 1 V.

*Note 11:* 0 dB is equal to 10 V.

*Note 12:* For WBS42 Modules up to and including WSB424, shunt resistors only work in full bridge mode.

# getting to know the PAK MKII

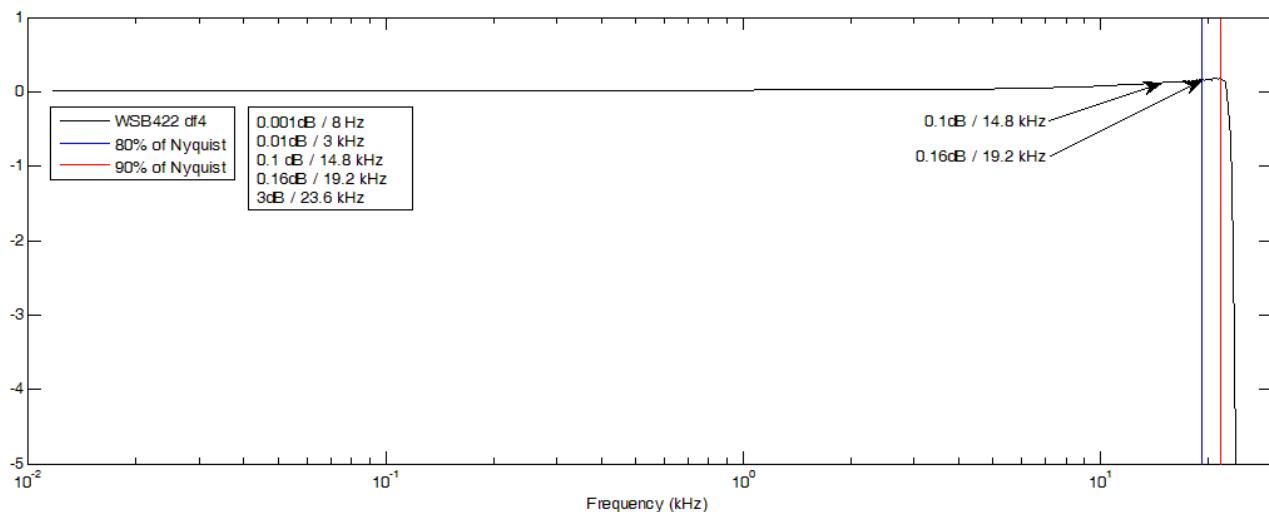
## Frequency Response Analysis



### Notes:

Nyquist frequency is 48 kHz.

0 dB equals 145 mVpp.



### Notes:

Nyquist frequency is 24 kHz.

0 dB equals 145 mVpp.

# chapter four

## WSB42

continued

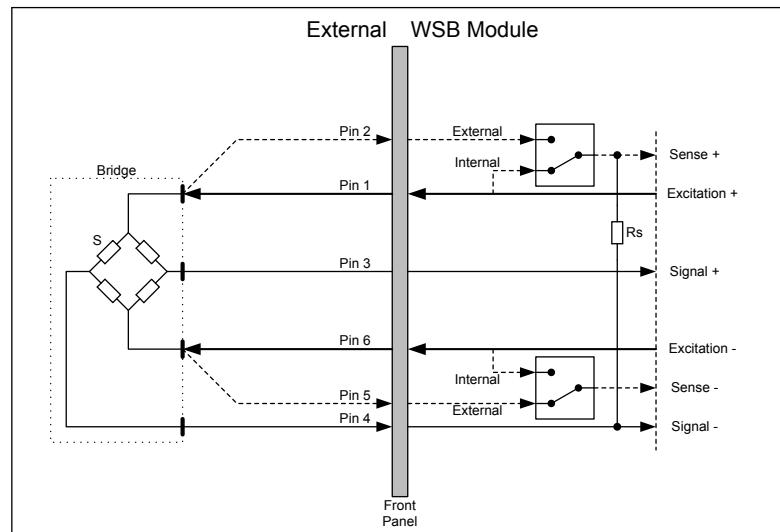
S = sensor  
Rs = calibration shunt resistor

### BRIDGE CONFIGURATIONS AND CONNECTIONS

The figures below show full, half and quarter bridge configurations for the WSB Module and a bridge located externally to the Module.

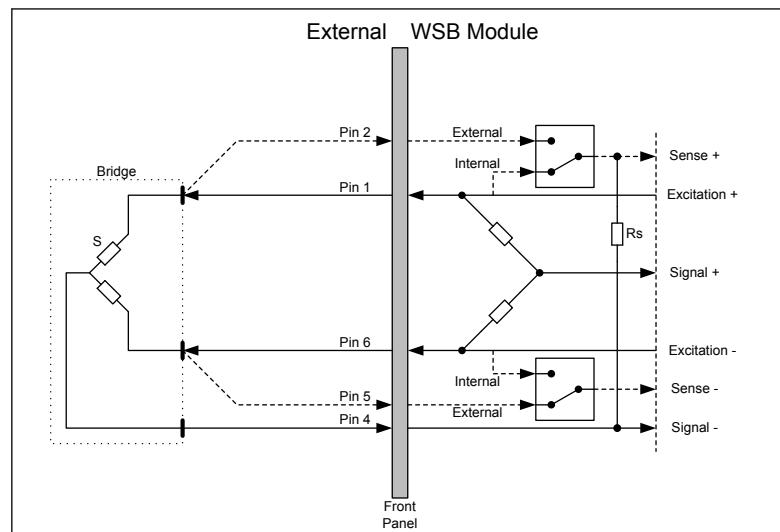
External connections and internal full bridge completion per WSB Module channel (6-wire bridges can be used with external sensing and 4-wire bridges with internal sensing).

#### Full Bridge Functionality



External connections and internal half bridge completion per WSB Module channel (5-wire bridges can be used with external sensing and 3-wire half bridges with internal sensing)

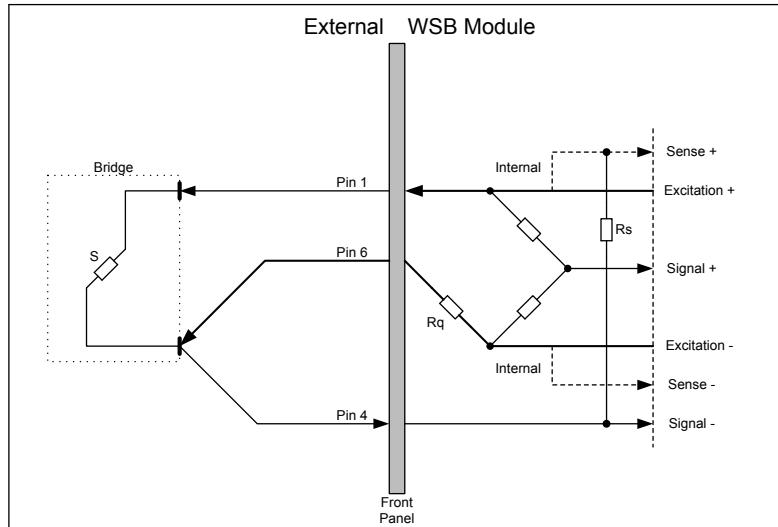
#### Half Bridge Functionality



# getting to know the PAK MKII

External connections and internal quarter bridge completion per WSB Module channel (3-wire quarter bridges can be used with internal sensing)

## Quarter Bridge Functionality



## WSB42

continued

S = sensor

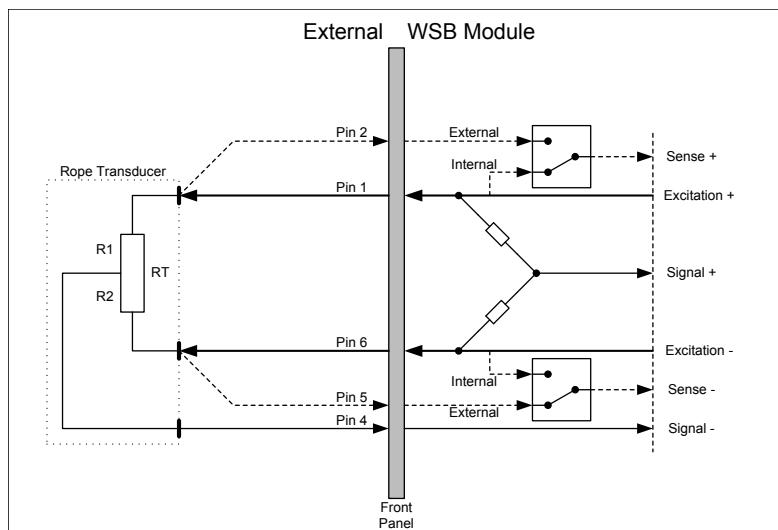
Rq = quarter bridge completion resistor

## USING A ROPE TRANSDUCER

The figure and descriptions below detail the connections between a WSB Module and a rope transducer.

External connections to a rope transducer and internal half bridge completion per WSB Module channel (5-wire and 3-wire rope transducers)

## Rope Transducer Functionality



The rope transducer's potentiometer is such that  $RT = R1 + R2$ . In terms of displacement, this is equal to  $LT = L1 + L2$ . Also  $L1/LT = R1/RT$  (1)

# chapter four

## WSB42

continued

### USING A ROPE TRANSDUCER (continued)

Now for the bridge above: if  $V_{in}$  is defined as the voltage difference between Signal+ and Signal- (in other words, the input voltage) and  $V_{exc}$  is defined as the voltage difference between Excitation+ and Excitation- (in other words, the excitation voltage), then the following equation holds:

$$V_{in} = V_{exc} (R1/RT - \frac{1}{2}) \quad (2)$$

When (1) is substituted into (2) we get

$$L1/LT = V_{in}/V_{exc} + \frac{1}{2} \quad (3)$$

The only restriction with the above configuration is that  $V_{in}$  must stay within range of the input amplifier. Hence  $V_{exc}$  is limited as follows:

WSB42 Modules:  $V_{exc} = 500$  mV

This should however not be a problem as  $V_{in}$  is normally a great deal lower in the case of a strain gauge bridge amplifier.

## 8 Channel Thermocouple/ Pt100 Input

### THM Module

---

#### DESCRIPTION

The THM Module provides 8 input channels for measuring temperature signals with thermocouples and Pt100 sensors. Besides Pt100 sensors E-, J-, K-, T- and U-type thermocouples are supported.

#### TYPES

There is a single THM Module type, that being:

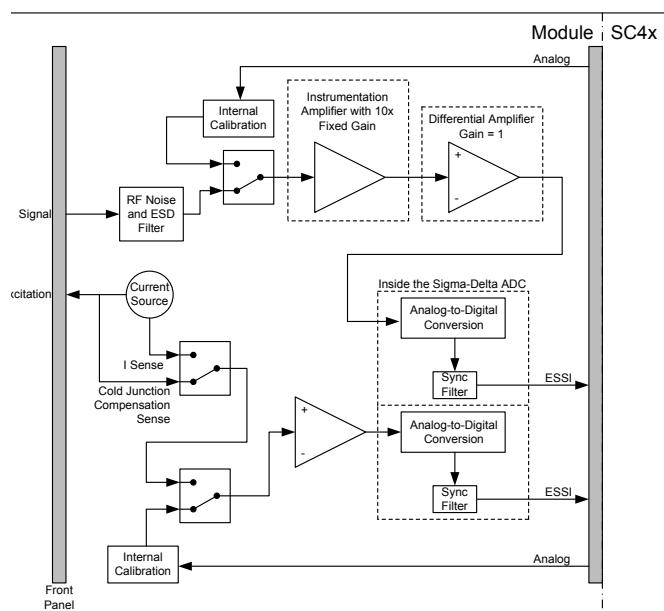
1. THM42

# chapter four

## THM42



### THM42 Functionality per Channel



# getting to know the PAK MKII

## THM42 Specifications

### Accuracy with THME10 SubModule

Function	Simulated Input (°C)	Min (°C)	Typical (°C)	Max (°C)
Temperature (°C)	-85	-86.2	-84.8	-83.1
	-45	-46.2	-44.7	-43.2
	0	-1.1	0.3	1.7
	200	199.1	200.3	201.7
	400	399.2	400.4	401.7
	600	599.2	600.4	601.7
	780	779.2	780.5	781.9

### Accuracy with THMP10 SubModule

Function	Simulated Input (°C)	Min (°C)	Typical (°C)	Max (°C)
Temperature (°C)	-190	-191.1	-190.6	-190.0
	-100	-101.2	-100.7	-100.0
	0	-1.3	-0.7	0.1
	250	248.3	249.3	250.3
	450	447.9	449.3	450.7
	650	647.7	649.4	651.0
	800	797.3	799.5	801.5

Conditions:

- Within 30 minutes after “self calibration”
- Following the required 1 hour warm-up period of the PAK MKII
- Module Temperature of  $45^{\circ}\text{C} \pm 7^{\circ}\text{C}$

# chapter four

## THM42 Features

Parameter	Value
Module Connector	Lemo EHG.0B.307.CLN
Channels	8 input (4 groups of 2 channel pairs, 2 channels per connector)
Input Modes	Thermocouple and Pt100
Sensors	Any combination of thermocouple and Pt100 but the same type of sensor must be used for each channel pair
Linearization	Thermocouple linearization for types: Iron/Constantan (J, Fe-CuNi), Chromel®/Alumel® (K, NiCr-NiAl), Copper/Constantan (T, Cu-CuNi)
Excitation	0.5 mA Excitation current for Pt100 and cold-junction-compensation. Monitored internally for drift and offset errors
Input Voltage Range	±250 mV
Maximum Common Mode Voltage	±4 V
Maximum Sampling Rate Per Channel (fs)	6.4 kHz
Maximum Sampling Rate per Module	51.2 kHz
Other Sampling Rates	Available through digital LP filters and decimation
Onboard ADC	8x sigma-delta for measurement and 2x sigma delta for thermocouple cold-junction compensation and Pt100 excitation current monitoring
Resolution	24-bit
SNR (fs = 24 kHz) Note 1, 2, 8	121 dB (±250 mV)
THD (fs = 24 kHz) Note 1, 3, 8	99 dB (±250 mV)

# getting to know the PAK MKII

## THM42 Features continued

Parameter	Value
<b>SFDR<sub>IV</sub></b> (fs = 24 kHz) Note 1, 4, 8, 9	133 dB ( $\pm 250$ mV)
<b>SFDR<sub>10V</sub></b> (fs = 24 kHz) Note 1, 4, 8, 10	153 dB ( $\pm 250$ mV)
<b>SFDR<sub>H</sub></b> (fs = 24 kHz) Note 1, 5, 8, 9	104 dB ( $\pm 250$ mV)
<b>Crosstalk</b> (fs = 24 kHz) Note 1, 6, 8	108 dB ( $\pm 250$ mV)
<b>Noise Floor</b> (fs = 24 kHz) Note 1, 7, 8, 9	143 dB ( $\pm 250$ mV)
<b>Protection</b>	2 kV ESD
<b>SubModules</b>	Cable between Module and sensor wire with housing containing TEDS, cold-junction-compensation and sensor connector. Color coded according to thermocouple type
<b>Module Calibration</b>	Internal amplitude and phase calibration
<b>TEDS</b>	Support for IEEE 1451.4 Class 2

The different modes and parameter values mentioned in the features table are all software-selectable.

*Note 1:* Measured after Module auto calibration has been applied.

*Note 2:* Signal to Noise Ratio (SNR): The ratio of the rms signal amplitude to the rms noise value excluding harmonics. Input signals are  $\pm 125$  mV<sub>amplitude</sub> ( $\pm 250$  mV Range) @ 1 kHz.

*Note 3:* Total Harmonic Distortion (THD): The ratio of the root-sum-squares of the first 10 harmonic amplitudes to the fundamental signal amplitude. Input signals are  $\pm 125$  mV<sub>amplitude</sub> ( $\pm 250$  mV Range) @ 1 kHz.

*Note 4:* Spurious Free Dynamic Range (SFDR): The ratio of the full scale input to the amplitude of the largest spurious spectral component (Inputs terminated with a short circuit. Measurement bandwidth: 100 Hz to  $f_s / 2$  excluding harmonics).

*Note 5:* Spurious Free Dynamic Range (SFDR<sub>H</sub>): The ratio of the fundamental signal amplitude to the amplitude of the highest peak including the first and all other harmonics. Measurement bandwidth: 100 Hz to  $f_s / 2$ . Input signals are  $\pm 125$  mV<sub>amplitude</sub> ( $\pm 250$  mV Range) @ 1 kHz.

*Note 6:* Crosstalk: Signal is played into a channel while the remaining channels are short circuited. The crosstalk is the ratio of the fundamental signal amplitude of the input channel to the signal amplitude at the fundamental frequency on the remaining channels. Input signals are  $\pm 125$  mV<sub>amplitude</sub> ( $\pm 250$  mV Range) @ 1 kHz.

*Note 7:* Noise Floor: The rms noise value specified in dB when the inputs are terminated with a short circuit.

*Note 8:* Listed values are typical measurement values.

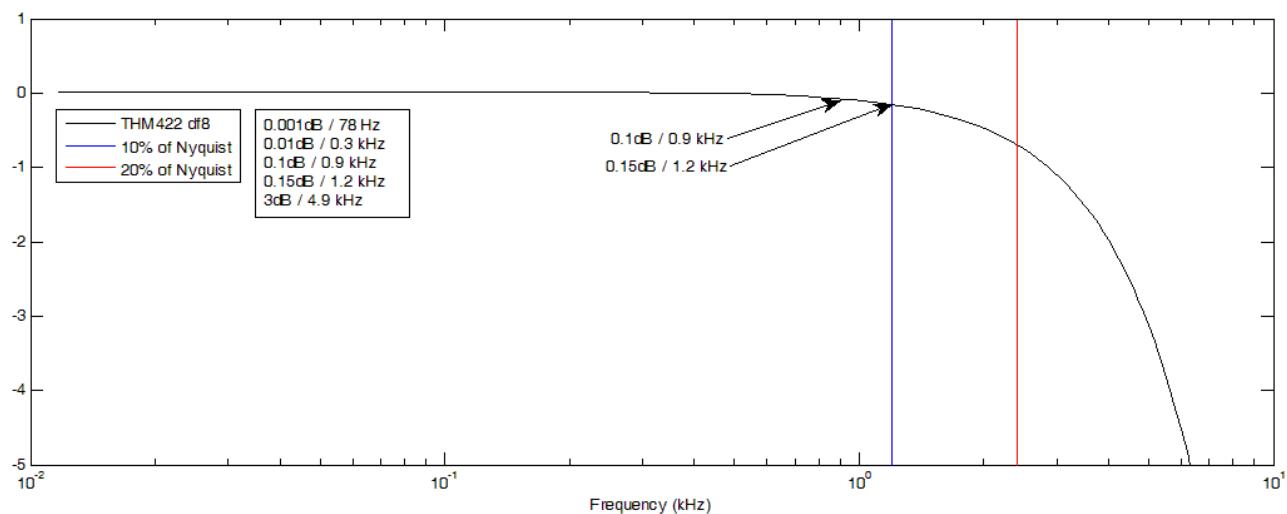
# chapter four

## THM42 Features continued

Note 9: 0 dB is equal to 1 V.

Note 10: 0 dB is equal to 10 V.

## Frequency Response Analysis



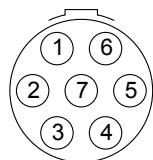
# getting to know the PAK MKII

## CONNECTOR PIN DEFINITIONS

The THM Module contains 4 Lemo connectors at the front panel (two channels per connector).

The pins for each connector are defined as follows:

- Pin 1: IN0-
- Pin 2: IN1-
- Pin 3: Excitation
- Pin 4: AGND
- Pin 5: IN1+
- Pin 6: IN0+
- Pin 7: SubModule ID



Pin definitions of a THM Module 7-pin Lemo connector (when looking into the connector)

**THM42**

continued

# chapter four

## THM42

sensor configurations  
and sensor technology

### NOTE:

To ensure that the THM Module functions correctly, the User is strongly urged not to change any SubModule connected to a THM Module during a measurement. All SubModules must be connected to the THM Module before the measurement starts.

### SENSOR CONFIGURATIONS AND SUBMODULE CONNECTIONS

There are 5 different SubModules to be used with THM42 Modules. These are the following:

1. THMS
2. THMP
3. THME
4. THMJ
5. THMK
6. THMT
7. THMU

Each THM42 Module can accommodate up to 4 SubModules. 2 sensors can be connected to the other end of the THMS, THMP, THMJ, THMK and THMT SubModules, resulting in a total sensor count of 8 sensors per Module. Both thermocouples and Pt100 sensors can be used with the SubModules. J-, K- and T-type thermocouples are supported.

### SENSOR TECHNOLOGY

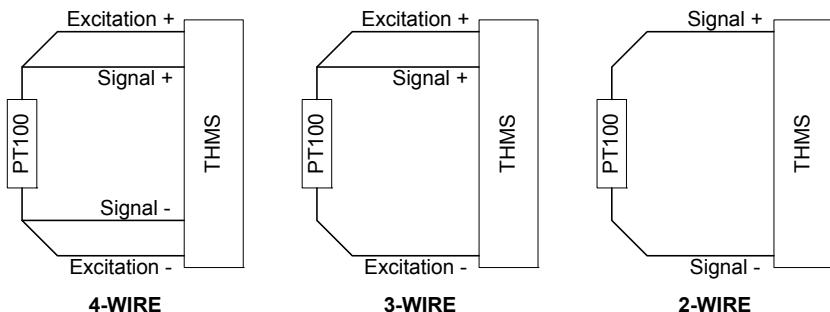
Thermocouple wires are color coded to reflect both the thermocouple type and to make a distinction between the positive and negative conductors. More than one standard exists therefor. The table below shows the wire colors for J-, K- and T-thermocouples as specified in the IEC, ASTM and DIN standards.

Pt100 sensors are more accurate and stable than thermocouples. Although they have a measurement range from -200 °C to 850 °C, they are typically only used up to temperatures of 600 °C. Thermocouples on the other hand are inexpensive and rugged and more immune to shock and vibration. They also tend to have faster response times compared to Pt100 sensors. The basic properties relating to each of the supported thermocouple types are shown in the table.

Pt100 sensors are available in 2-wire, 3-wire or 4-wire varieties. How to connect any of these sensor types to a THMS SubModule is shown in the diagrams of the three different sensor configurations. Thermocouples always have only two wires and are therefore not included in the figure.

# getting to know the PAK MKII

## 3 possible Configurations for Pt100 Sensors



## THM42

sensor configurations  
and sensor technology  
continued

## J-, K-, T- and E-type Thermocouple Properties

ANSI Type	Positive Lead Material	Negative Lead Material	Typical Range (°C)	Approximate Sensitivity ( $\mu\text{V}/^\circ\text{C}$ )	Features
J (Fe-CuNi)	Iron	Constantan	0 to 750	55	<ul style="list-style-type: none"> <li>Medium to high temperature</li> <li>Inexpensive</li> <li>Suitable for reducing environments</li> </ul>
K (NiCr-NiAl)	Chromel®	Alumel®	-200 to 1250	40	<ul style="list-style-type: none"> <li>General purpose</li> <li>High temperature</li> <li>Fairly inexpensive</li> <li>Suitable for oxidizing environment</li> </ul>
T (Cu-CuNi)	Copper	Constantan	-200 to 350	43	<ul style="list-style-type: none"> <li>General purpose</li> <li>Low temperature</li> <li>Moisture tolerant</li> </ul>
E (NiCr-CuNi)	Chromel®	Constantan	-200 to 900	68	<ul style="list-style-type: none"> <li>General purpose</li> <li>Low and medium temperature</li> <li>Highest sensitivity</li> </ul>

## Thermocouple Wire Colors as specified in the IEC, ASTM and DIN Standards

Type	IEC			ASTM			DIN		
	(+)	(-)	Connector	(+)	(-)	Connector	(+)	(-)	Connector
J (Fe-CuNi)	Black	White	Black	White	Red	Black	Red	Blue	Blue
K (NiCr-NiAl)	Green	White	Green	Yellow	Red	Yellow	Red	Green	Green
T (Cu-CuNi)	Brown	White	Brown	Blue	Red	Blue	Red	Brown	Brown
E (NiCr-CuNi)	Purple	White	Purple	Purple	Red	Purple	Red	Black	Black

# chapter four

## GPS Module

## GPS Receiver

### DESCRIPTION

The GPS Module provides a GPS receiver unit which interfaces to an external GPS antenna. The GPS Module generates valuable positioning information that is synchronized to other measurement data acquired from the PAK MKII.

### TYPES

There is a single GPS Module type, that being:

1. GPS42

### LED INTERPRETATION

The status of the LED located at the module front panel can be described as follows:

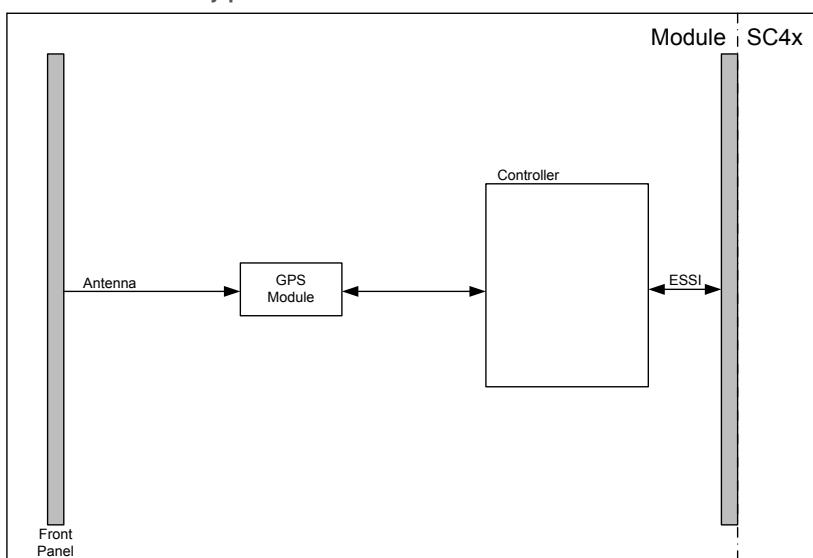
- LED blinking: 2D/3D fix, more than 3 satellites visible

# getting to know the PAK MKII



GPS42

## GPS42 Functionality per Channel



# chapter four

## GPS42 Features

Parameter	Description
Number of Channels	1
Antenna Voltage	3.3 V or 5 V
Input Connector	SMA
Receiver Type	L1 frequency, C/A Code, 16 Channels
Max Update Rate	4 Hz
Accuracy (SA off) Note 1	Position: 4.0 m CEP (Note 2), 5.0 m SEP (Note 3) Position DGPS/SBAS: <2.0 m CEP, 3.0 m SEP
Acquisition Time	Cold Start: 45 s, Warm Start: 38 s, Hot Start: < 8 s
Available Protocols	NMEA
Operational Limits	Altitude: < 18000 m, Velocity < 515 m/s
Available Baud Rates	9600
Specified Antenna	ANN-ST-0-005-0 GPS antenna from u-blox AG, Switzerland (Note 4)
Time-stamping of received GPS time and position data	5 µs

The different modes and parameter values mentioned in the features table are all software-selectable.

*Note 1:* SA: Selective Availability

*Note 2:* CEP: Circular Error Probability, the radius of a horizontal circle, centered at the antenna's true position, containing 50% of the fixes.

*Note 3:* SEP: Spherical Error Probability, the radius of a sphere, centered at the true position, contains 50% of the fixes.

*Note 4:* ANN-ST-0-005-0: Active GPS Antenna, with 5 m cable and an SMA connector.

# getting to know the PAK MKII

## IRIG and External/Internal GPS Receiver

### IRG Module

#### DESCRIPTION

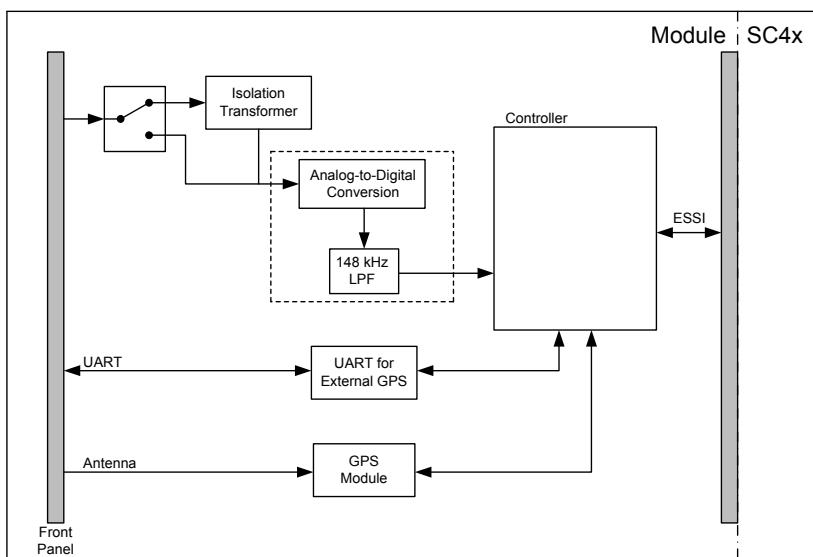
The internal GPS has the same specifications as the GPS Module. The external GPS function and IRIG receiver function is given in the following tables. The IRIG Receiver generates valuable timing information that is synchronized to other measurement data acquired from the PAK MKII.

#### TYPES

There is a single IRG Module type, that being:

1. IRG42

#### IRG42 Functionality per Channel



# chapter four

## IRG42



### IRG42 - External GPS Features

Parameter	Description
Number of Channels	1 x RS232
Supply Voltage	5 V, 1 A (max)
Input Connector	Lemo EHG.0B.307
Available Baud Rates	9600

### IRG42 - IRIG Features

Parameter	Description	
Number of Channels	1	
Input Connector	SMB	
IRIG Format Support <small>Note 1: The identification that follows was taken from the IRIG Standard 200-95.</small>	A003	1000pps, PWM-DC-Signal, no carrier BCD time of year, SBS time of day
	A133	1000pps, AM-Sine wave signal, 10 kHz carrier frequency BCD time of year, SBS time of day
	B003	100pps, PWM-DC-Signal, no carrier BCD time of year, SBS time of day
	B123	100pps, AM-Sine wave signal, 1 kHz carrier frequency BCD time of year, SBS time of day
DC Input Impedance	100 Ω	

Note 1: The identification that follows was taken from the IRIG Standard 200-95.

# getting to know the PAK MKII

## Interface to an EtherCAT® network

## ECT Module

### DESCRIPTION

The ECT Module adds functionality to the PAK MKII system which enables it to acquire data from networked EtherCAT® slave devices. The data acquired is synchronous with the highly-accurate EtherCAT® system time, and is presented along with informative variable parameters such as the denominator/numerator SI units, scaling factors etc. This functionality represents a ‘passive mode’ of operation in which the primary goal is to monitor variables external to the PAK MKII system.

### TYPES

There is a single EtherCAT Module type, that being:

1. ECT42

# chapter four

## ECT42



### SPECIFICATIONS

- Supports slave-to-slave communication (Passive mode)
- Time stamping of data in ubiquitous 64-bit EtherCAT® system time
- Full duplex 100-BASE-TX (100 Mbit/s) in upstream and downstream directions, with galvanic isolation on each interface
- Distributed clocks synchronized to an absolute maximum error of 100 ns
- Supports hot-connect and slave alias addressing for high availability
- Cycle times across the entire EtherCAT® network less than 100 µs
- M12 connectors for IP67 conformance
- Supports CANopen over EtherCAT® (CoE) and Service Delivery Object (SDO) access for extensibility
- Slave Information Interface (SII) implemented for device description
- Conforms to EtherCAT® standards (IEC61158, ISO 15745-4, SEMI E54.20)

### IN-SYSTEM OPERATION

A typical mode of operation is described in the block diagram below.

1. The XML descriptions of the slave devices on the network are processed by the master, and the EtherCAT® network is brought online
2. The output variables from other slave nodes are then mapped to the inputs of the ECT42 Module

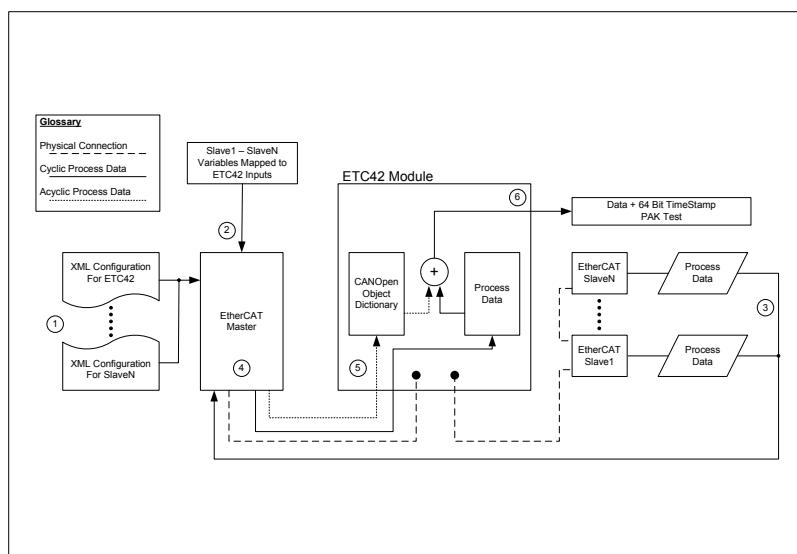
# getting to know the PAK MKII

3. As slave devices become operational, their output data is validated, and is made available on the network
  4. Cyclic data transfer of data from networked slaves to the ECT42 Module is effected by the master forwarding the process data as defined by the slave-to-slave mappings
  5. Acyclic data transfer of parameter data corresponding to the networked slave devices is brought about by the master through writing the relevant entries in the DS404 object dictionary
  6. The cyclic data is presented along with the corresponding parameter data from the object dictionary, as well as the 64-Bit EtherCAT® system timestamp within PAK
- Distributed clocks are supported by the Module and handled entirely by the EtherCAT® Master. If used and activated, the master will ensure that all the nodes are in sync.

## ECT42

continued

### ECT42 In-System Operation



### FUNCTIONALITY

The Module interfaces with the EtherCAT® network by means of two M12 connector ports, although for a basic network architecture only one port needs to be connected to the EtherCAT® network. A Lemo connector is also present through which the Module can be programmed within the PAK MKII system using JTAG. The EtherCAT® network is isolated from the Module by means of magnetics/transformers. Each port has a dedicated Ethernet PHY which is in turn connected to a PAK MII interface of the EtherCAT® ET1100 ASIC.

# chapter four

## ECT42 continued

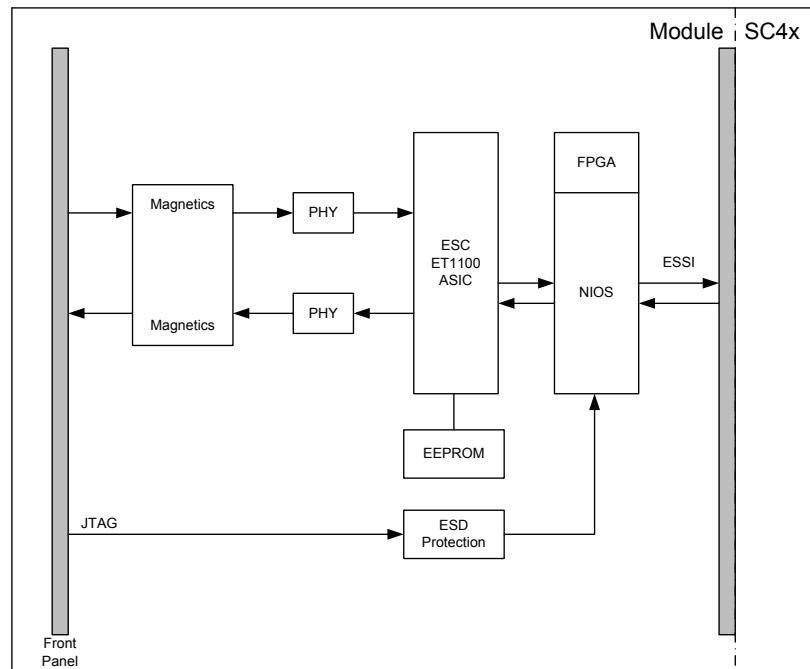
### The ET1100 ASIC

The ET1100 ASIC (application specific integrated circuit) is responsible for managing the communication path between the EtherCAT® fieldbus itself and the slave application. The primary functions of the ET1100 ESC (EtherCAT® Slave Controller) are thus to implement EtherCAT® MAC (Medium Access Control) functionality which includes real-time frame processing and address translation from the logical address space used by the master device, to the physical address space on the slave devices themselves. A 16 bit parallel asynchronous microcontroller interface exists between the ASIC and the FPGA. An EEPROM connected to the ET1100 stores the start-up device information for the slave device (this is programmed by the EtherCAT® master over the network).

### The Cyclone III FPGA and NIOS

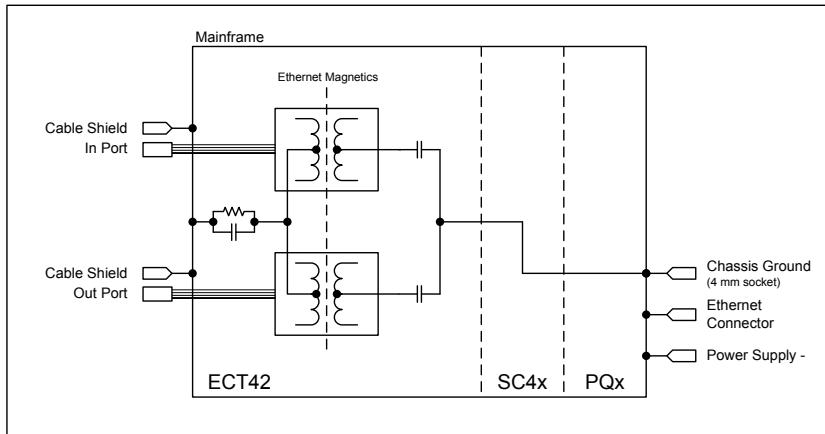
A Cyclone III FPGA (field programmable gate array) has been implemented on the Module in order to realize the slave application. This FPGA supports the implementation of a NIOS II processor onboard, which was used to implement the control, SC communications and application layer functionality. The main interface between the Module and the SC4x bus has been realized using the ESSI (Enhance Synchronous Serial Interface) communication lines. This interface is the means by which test data is streamed from the Module.

### ECT42 Functionality Diagram



# getting to know the PAK MKII

## ECT42 Grounding Diagram



**ECT42**  
continued

## ECT42 Features

Parameter	Value	Comments
Module Connectors	2x ERNI M12 Connectors (234041)	IP67 compliant
Physical Channel Configuration	Flexible, topology dependent.	
Logical Channel Configuration	Flexible. Provision for up to 40 32-bit Float input channels currently	Configurable at run time
EtherCAT® Compliance	IEC 61158, ISO 15745-4, SEMI E54.20	
Operational Modes	Passive Mode data acquisition. Full EtherCAT® state machine	
EtherCAT® Controller	ET1100	
EtherCAT® Controller Clock Accuracy	15 ppm	RX queue delay of 0 (<20 ppm)
Typical Synchronization Accuracy	10-20 ns	
Effective Bit Rate	135-400 kB/s	Dependent on input configuration

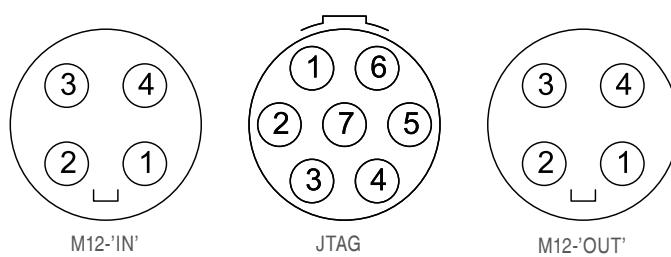
# chapter four

## ECT42

continued

### CONNECTOR INFORMATION / PIN DEFINITIONS

- Two connectors on Module front panel marked 'IN' and 'OUT'.
- Network topology determines the need for downstream link on 'OUT' port.
- Both connectors represent full duplex 100 Mbit/s links to an upstream/downstream device on the network.
- Lemo connector for JTAG configuration of controller in the field.



Pin Number	Definition
M12 'IN' and 'OUT' 1	Ethernet TX+
M12 'IN' and 'OUT' 2	Ethernet RX+
M12 'IN' and 'OUT' 3	Ethernet TX-
M12 'IN' and 'OUT' 4	Ethernet RX-
Lemo 1	2.5 V Input (Programmer)
Lemo 2	JTAG - TCK
Lemo 3	JTAG - TMS
Lemo 4	JTAG - TDO
Lemo 5	JTAG - TDI
Lemo 6	Ground (Programmer)
Lemo 7	Not Connected

# getting to know the PAK MKII

## Interface to FlexRay™ network

## FLX Module

### DESCRIPTION

The FLX Module provides an interface to connect to a FlexRay™ network. FlexRay™ is a very fast, deterministic, and fault-tolerant protocol that could satisfy the speed, reliability, and safety requirements of such applications as brake-by-wire and steer-by-wire. The protocol provides flexibility and determinism by combining scalable static and dynamic message transmission.

The protocol supports:

- Fault-tolerant clock synchronization (global time base)
- Collision-free bus access
- Guaranteed message latency
- Message oriented addressing via identifiers
- Scalable system fault-tolerance (single or dual channels).
- Physical layer error containment via an independent Bus Guardian on each channel.

A typical FlexRay™ system consists of either a single or dual channel network, each channel has its own cable terminated at the end with terminating resistors (typically  $110\ \Omega$ ). FlexRay™ nodes are connected at non-fixed locations along the cables (see supported network topologies).

Each node usually contains one transceiver per channel to convert differential FlexRay™ bus signal levels to normal bit stream levels. The bit stream is transmitted or received by a FlexRay™ Communications Controller (FCC) which acts as the FlexRay™ protocol handler of the node. Information is transmitted on the FlexRay™ bus using messages with the format defined by the FlexRay™ specification. These messages are referred to as FlexRay™ messages. The FLX Module contains two dependent FlexRay™ channel interfaces to support either the single channel or dual channel topologies. The MFR4310 communication controller and TJA1080 transceivers are used on the FLX Module. It supports the transmission and reception of FlexRay™ messages over a FlexRay™ network with selectable bit rates of 2.5, 5, 8 or 10 Mbit/s. The FLX Module supports independent channel filtering and provides status and error information to the User.

### NOTE:

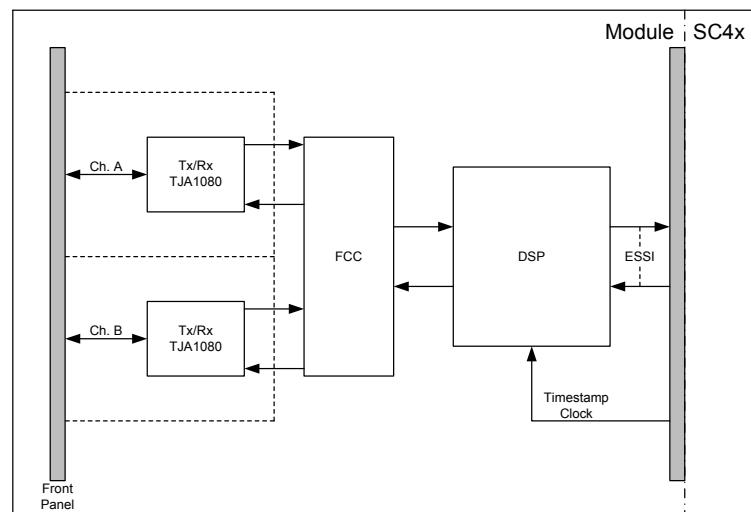
The FLXB10 and FLXB20 SubModules are used to connect the FLX Module to a FlexRay™ network.

# chapter four

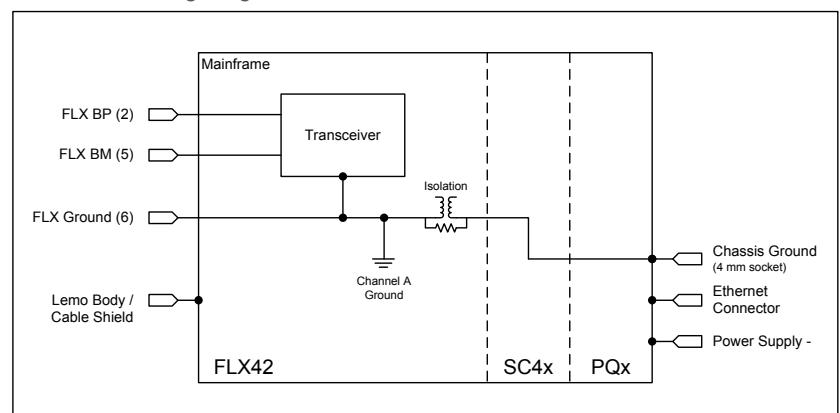
## FLX42



FLX42 Functionality Diagram



FLX42 Grounding Diagram



# getting to know the PAK MKII

More features of the FLX Module include:

- Conformance with FlexRay™ Protocol Specification V2.1A.
- FlexRay™ Electrical Physical Layer Specification V2.1A.
- Each FLX interface is galvanically isolated from the PAK MKII.
- Each FLX message received and accepted by the FLX Module will be time stamped in order to synchronize the received FLX messages with the rest of the measurement data.
- Individually configurable FlexRay™ Frame ID, Channel ID and Cycle Count filtering per channel.

## FLX42

continued

### FLX42 Features

Parameter	Value
Module Connectors	Lemo EHG.0B.307
Channel Configuration	2 dependent channels – Dual Channel Device or Single Channel Device (connector 2 disabled)
Operational Modes	Listen-Only Mode / Operational Mode / Self-Test Mode
FlexRay™ Compliance Note 1	FlexRay™ Protocol Specification V2.1A. FlexRay™ Electrical Physical Layer Specification V2.1A
Termination	FLX420 - None (Use FLXB10) FLX421 - Software selectable (Use FLXB20)
FlexRay™ Transceivers	NXP TJA1080
FlexRay™ Controller	Freescale MFR4310
FlexRay™ Controller Clock Frequency	40 MHz
FlexRay™ Bit Rate Range	2.5, 5, 8 or 10 Mbit/s
Timestamp Resolution Note 2	38 ns - 60 ns
Galvanic Isolation	50 V
Operational Temperature	-25 °C to 80 °C

The different modes and parameter values mentioned in the features table are all software-selectable.

*Note 1:* The Module was designed according to the mentioned specifications, currently no compliance tests have been attempted.

*Note 2:* The timestamp clock is derived from the same SC4x clock reference as used by the SC4x for analog-to-digital conversion. Therefore, the timestamp resolution varies according to the sampling rates set for the other Modules in the same SC4x.

# chapter four

## FLX42

continued

### FLEXRAY™ CHANNEL DEVICE CONFIGURATION

The FLX42 Module can be configured and used in the following device configuration modes:

#### Single Channel Device Configuration

It will function as a device that only has one FlexRay™ port. Connector 1 of the FLX42 Module can be connected to either channel A or channel B of the FlexRay™ network. The connected channel must be specified (either channel A or B) in the node parameters and receive FIFO parameters when allocating and configuring the Module.

**IMPORTANT:** In this configuration, connector 2 of the Module must not be connected!

#### Dual Channel Device Mode:

The FLX42 will function as a device with two FlexRay™ ports. Connector 1 of the FLX42 Module must be connected to channel A, and connector 2 must be connected to channel B of the FlexRay™ network.

### FLX42 OPERATIONAL MODES

The FLX42 Module must be configured to operate in either of the following operational modes:

#### Listen-Only Mode

The FLX42 Module will passively listen on the network and capture all messages as configured by the receive filters. The TJA1080 transceiver (one per FlexRay™ channel) is configured to prevent all transmissions from the FLX42 FlexRay™ controller.

#### Operational Mode

The FLX42 Module will actively participate in the network communication by not only capturing messages, but also transmitting messages sent to the FlexRay™ controller's transmit buffer via the API. Currently only one transmit buffer is supported per Module. The TJA1080 transceiver (one per FlexRay™ channel) is configured to allow reception and transmission of FlexRay™ messages. In this mode the Module may also be used to start up a FlexRay™ cluster.

#### Self-Test Mode

Simulation data will be generated on the Module DSP and streamed to the API as if the Module was capturing messages from a network. The FlexRay™ controller will be kept in HALT mode and thus will not affect any connected networks. The Self-Test mode is available for both Single- and Dual Channel device configuration.

# getting to know the PAK MKII

## SUPPORTED NETWORK TOPOLOGIES

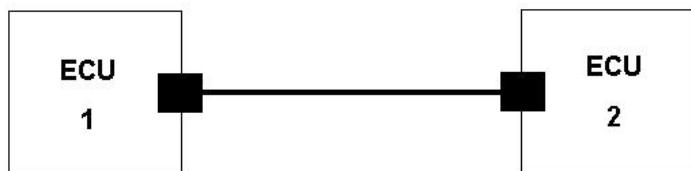
The Electrical Physical Layer (EPL) Specification 2.1 Rev. A specifies various network topologies for a FlexRay™ communication network. The FLX Module is compatible with the following network topologies (note that the termination is application specific, more details available from specification):

- Point-to-point (both terminated).
- Passive Star (furthest points terminated).
- Passive Linear Bus (furthest points terminated).
- Active Star (all terminated).
- Cascaded Active Star (furthest points terminated).
- Hybrid Technologies (application specific termination).

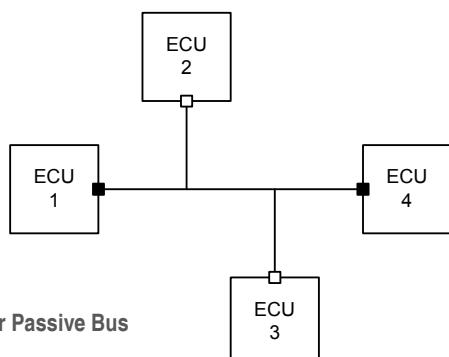
The following list of figures illustrate the above mentioned topology types. Note that the solid black square on a node indicates termination at that node. The empty squares indicate no termination.

## FLX42

continued



Example of Point-to-Point



Example of Linear Passive Bus

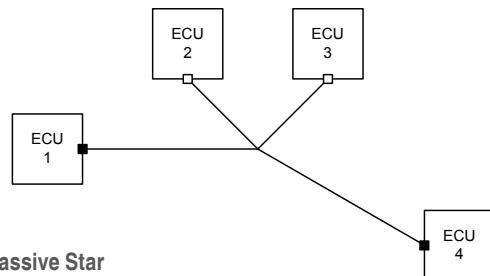
# chapter four

## FLX42

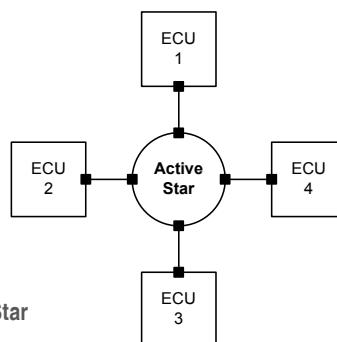
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### NOTE:

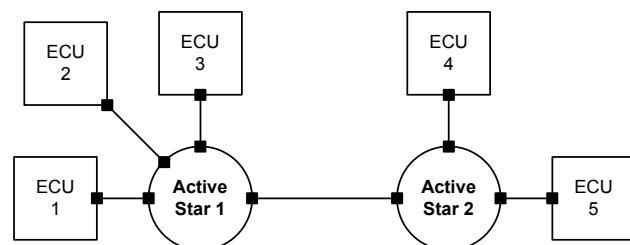
The FLXB10 and FLXB20 SubModules are used to connect the FLX Module to a FlexRay™ network.



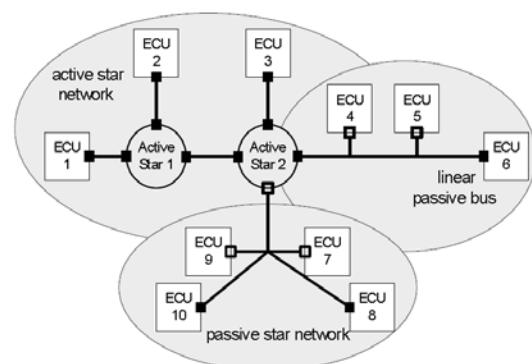
Example of Passive Star



Example of Active Star



Example of Cascaded Active Star

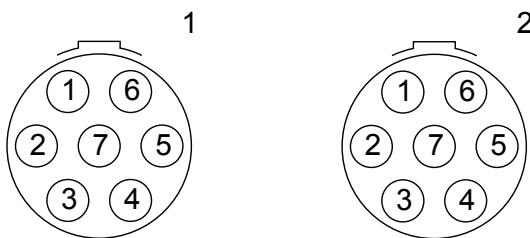


Example of Hybrid Technologies

# getting to know the PAK MKII

## CONNECTORS

The front view of the FLX Module is illustrated in the following figure. It has two Lemo EHG.0B.307 connectors marked as connectors 1 and 2. In Dual Channel Device configuration connector 1 corresponds to FlexRay™ Channel A, and connector 2 corresponds to FlexRay™ Channel B. In Single Channel Device configuration, connector 2 must not be connected and connector 1 serves as either Channel A or Channel B, depending on the node configuration settings.



**FLX42 Module connector pin layout (when looking into the connectors)**

## PIN DEFINITION

- Pin 1 – Reserved (Do not connect)
- Pin 2 – FLX Bus Plus
- Pin 3 – Reserved (Do not connect)
- Pin 4 – Reserved (Do not connect)
- Pin 5 – FLX Bus Minus
- Pin 6 – FLX Ground (to be connected to external network ground, isolated from PAK MKII)
- Pin 7 - Reserved (Do not connect)

The FLXB10 and FLXB20 SubModules can be used to connect the FLX42 module to a FlexRay™ network.

## FLX42

continued

# chapter four

**SubModules**      **Personalize sensors**

---

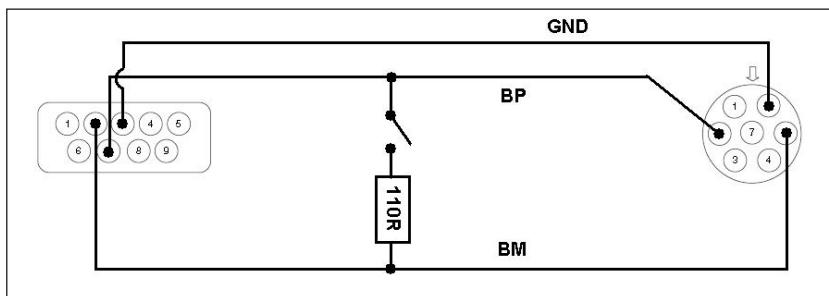
# getting to know the PAK MKII



## FLXB10

The Lemo connectors of the FLX42 Module must first be converted to the correct interface before it can be used on a FlexRay™ network. The FLXB10 and FLXB20 SubModules are used for this purpose. The FLXB10 SubModule is a Lemo to 9-pin D-sub connection cable (0.3m) that gives the user the option to terminate the cable at the FLX42 Module side with a  $110\ \Omega$  resistance. This SubModule is intended for use with FLX42 Module builds which has no internal termination selection circuitry (Identified as FLX420 in the Web Server). Its aluminum enclosure can be opened to allow the user to set or remove the termination via jumper connectors. The printing on the enclosure can be used to indicate the state of termination of the SubModule without opening the lid. See the supported network topologies section above for information about FlexRay™ network termination. The following figure illustrates the function of the FLXB10 cable.

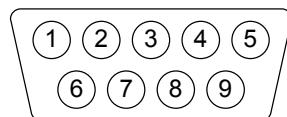
### Functional Illustration of the FLXB10 SubModule



# chapter four

## FLXB10 continued

The pin configuration of the 9-pin D-sub connector:

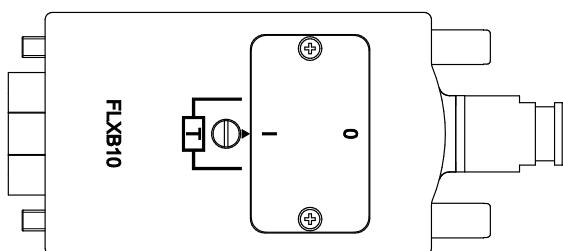
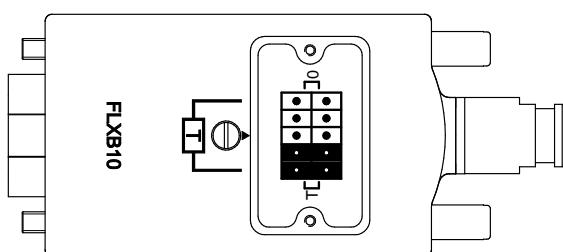
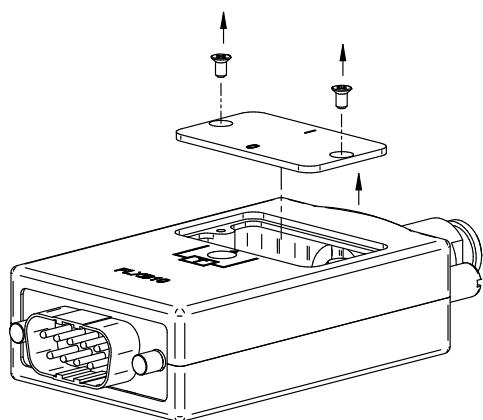


- Pin 1: Not connected
- Pin 2: FLX Bus Minus
- Pin 3: FLX Ground (network ground or common ground)
- Pin 4: Not connected
- Pin 5: Chassis ground (cable shield) - not used
- Pin 6: Optional FLX Ground – not used
- Pin 7: FLX Bus Plus
- Pin 8: Not connected
- Pin 9: VBAT – not used

# getting to know the PAK MKII

## HOW TO SET FLXB10 CABLE TERMINATION:

1. To enable termination, remove the two small screws on the printed side of the FLXB10 enclosure. Remove the lid to gain access to the jumpers.
2. Holding the enclosure in the same orientation as in the picture, insert two jumpers (they bridge from left to right) on the middle connector as indicated. The termination side of the middle connector is indicated with a 'T' on the printed circuit board.
3. Put the lid back on the enclosure, making sure that the printed 'I' on the lid is next to the printed arrow of the enclosure, and put the screws back in.
4. To test if the cable is terminated correctly, there should be a  $110 \Omega$  resistance between pins 2 and 7 of the 9-pin D-sub connector.



## FLXB10

continued

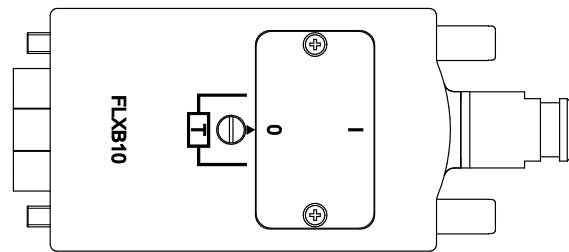
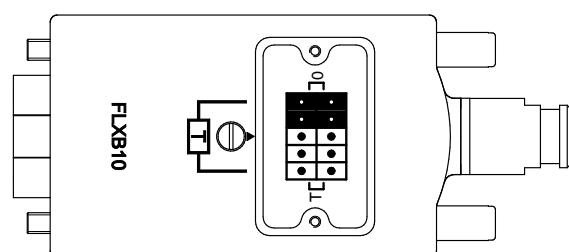
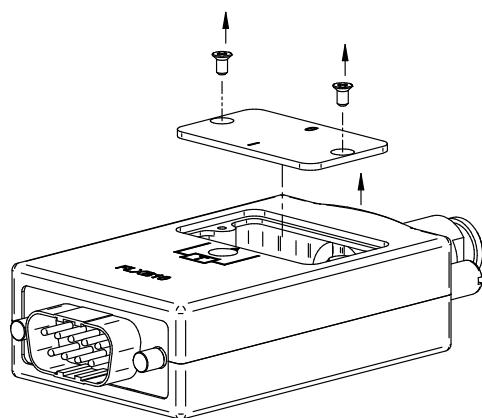
# chapter four

## FLXB10

continued

### HOW TO REMOVE FLXB10 CABLE TERMINATION:

1. Remove the two small screws on the printed side of the FLXB10 enclosure. Remove the lid to gain access to the jumpers.
2. Holding the enclosure in the same orientation as in the picture, move the two jumpers (they bridge from left to right) on the middle connector as indicated, from the 'T' side to the 'O' side on the printed circuit board.
3. Put the lid back on the enclosure, making sure that the printed 'O' on the lid is next to the printed arrow of the enclosure, and put the screws back in.
4. To test if the cable termination is removed, there should be an open circuit between pins 2 and 7 of the 9-pin D-Sub connector.



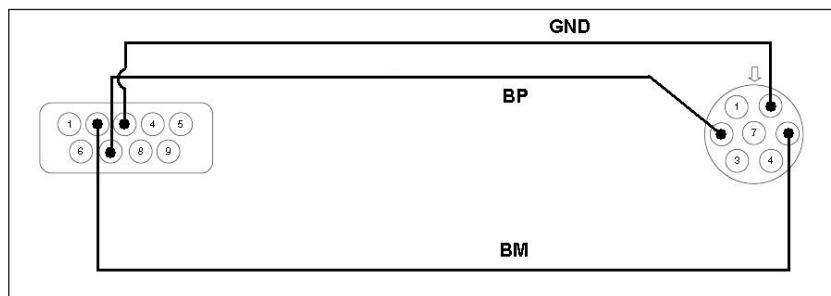
# getting to know the PAK MKII



## FLXB20

The Lemo connectors of the FLX42 Module must first be converted to the correct interface before it can be used on a FlexRay™ network. The FLXB10 and FLXB20 SubModules are used for this purpose. The FLXB20 is just a Lemo to 9-pin D-sub connection cable (3m). This SubModule is intended for use with FLX42 Module builds which has internal termination selection circuitry (identified as FLX421 and FLX422 in the Web Server). See the supported network topologies section above for information about FlexRay™ network termination. The following figure illustrates the function of the FLXB20 cable.

### Functional Illustration of the FLXB20 SubModule



The pin configuration of the 9-pin D-sub connector is the same as with the FLXB10.

# chapter four

## QBNC11



The Quad BNC (QBNC) is a Sub Module that is used to split signals from a 7-pin Lemo connector to 4 BNC connectors. A sticker on top indicates with which Modules the QBNC is compatible, and how the signals are mapped.

### QBNC11 specifications

QBNC11			
		ALO42S	ICM42S
BNC 1	Center pin	Analog Signal Output +	CH1 Monitor +
	Shield*	Analog Signal Output -	CH1 Monitor -
BNC 2	Center pin	Module Status Output +	CH2 Monitor +
	Shield	Module Status Output -	CH2 Monitor -
BNC 3	Center pin	DUC Status Input +	CH3 Monitor +
	Shield	DUC Status Input -	CH3 Monitor -
BNC 4	Center pin	5V / 12V Ouput +	CH4 Monitor +
	Shield*	5V / 12V Ouput -	CH4 Monitor -

\*Note that the shield of BNC 1 and BNC 4 are connected together as the 7 Lemo connector signals must be converted to 8 BNC connector signals.

# getting to know the PAK MKII



## THM SubModules

### DESCRIPTION

The THM SubModules are used with the THM42 module.

### TYPES

There are 7 THM SubModules, that being:

1. THMS
2. THMP
3. THME
4. THMJ
5. THMK
6. THMT
7. THMU

# chapter four

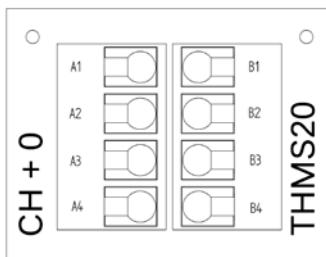
The THMS provides screw terminal connectors for connection of all supported thermocouple types and PT100 sensors. The two thermocouples connected to the SubModule should be of the same type. The THM42 module can however support any combination of different SubModules simultaneously.

## The THMS provides the following functions:

1. General-purpose screw terminal connectors for connection to any of the supported sensor types
2. Regular measurements of the thermocouple junction temperatures for cold-junction-compensation
3. TEDS functionality for reading sensor URN (Unique Registration Number)
4. TEDS functionality for SubModule identification.

The figure below shows a simplified drawing of the THMS front panel and screw input terminal connectors. Pin numbers A1 through B4 are not printed on the actual front panel and are for illustration of the connection procedure only.

On the front panel “CH +0” refers to the first channel (A). The connector to the right is used for second channel (B). The two dots in the top corners indicate the locations of the first pin for each sensor. Pin numbers then follow in numerical order up to pin 4.



THMS front panel and screw terminal input connectors (version 1)

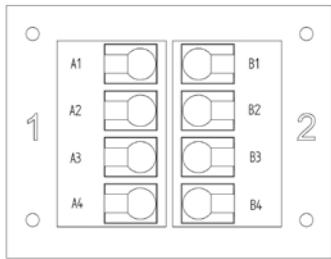
The following figure shows a drawing of the THMS front panel and screw terminal input connectors for newer versions of the THMS. Once again, pin numbers A1 through B4 are not printed on the actual front panel and are shown here for illustration of the connection procedure only.



## THMS

### connection information

# getting to know the PAK MKII



THMS front panel and screw terminal input connectors (version 2)

## THMS

connection information  
continued

### NOTE:

It is important to note that the use of 2-wire and 3-wire Pt100 sensors is not recommended due to an increase in measurement errors brought about by the lead resistance.

### Connections between 2 Thermocouple/Pt100 Sensors and a THMS

Pin Number	Function	Sensor Type Note 1			
		Thermocouple	Pt100 (4-wire)	Pt100 (3-wire)	Pt100 (2-wire)
A1	Excitation0+	NC	Positive current lead of first Pt100	Positive current lead of first Pt100	Jumper between pins A1 and A2 Note 2
A2	Signal0+	Positive lead of first thermocouple	Positive signal lead of first Pt100	Positive signal lead of first Pt100	Positive signal lead of first Pt100
A3	Signal0-	Negative lead of first thermocouple	Negative signal lead of first Pt100	Negative signal lead of first Pt100	Negative signal lead of first Pt100
A4	Excitation0-	NC	Negative current lead of first Pt100	Jumper between pins A3 and A4 Note 2	Jumper between pins A3 and A4 Note 2
B1	Excitation1+	NC	Positive current lead of second Pt100	Positive current lead of second Pt100	Jumper between pins B1 and B2 Note 2
B2	Signal1+	Positive lead of second thermocouple	Positive signal lead of second Pt100	Positive signal lead of second Pt100	Positive signal lead of second Pt100
B3	Signal1-	Negative lead of second thermocouple	Negative signal lead of second Pt100	Negative signal lead of second Pt100	Negative signal lead of second Pt100
B4	Excitation1-	NC	Negative current lead of second Pt100	Jumper between pins B3 and B4 Note 2	Jumper between pins B3 and B4 Note 2

Note 1: NC means no connection.

Note 2: This connection is not made by the THMS internally and must therefore be made by the User externally.

# chapter four

## Connections between 1 Thermocouple/Pt100 Sensor and Channel 1 of the THMS

Pin Number	Function	Sensor Type Note 1			
		Thermocouple	Pt100 (4-wire)	Pt100 (3-wire)	Pt100 (2-wire)
A1	Excitation0+	NC	Positive current lead of Pt100	Positive current lead of Pt100	Jumper between pins A1 and A2 Note 2
A2	Signal0+	Positive lead of thermocouple	Positive signal lead of Pt100	Positive signal lead of Pt100	Positive signal lead of Pt100
A3	Signal0-	Negative lead of thermocouple	Negative signal lead of Pt100	Negative signal lead of Pt100	Negative signal lead of Pt100
A4	Excitation0-	NC	NC	NC	NC
B1	Excitation1+	NC	NC	NC	NC
B2	Signal1+	NC	NC	NC	NC
B3	Signal1-	NC	NC	NC	NC
B4	Excitation1-	NC	Negative current lead of Pt100	Jumper between pins A3 and B4 Note 2	Jumper between pins A3 and B4 Note 2

Note 1: NC means no connection.

Note 2: This connection is not made by the THMS internally and must therefore be made by the User externally.

# getting to know the PAK MKII

Connections between 1 Thermocouple/Pt100 Sensor and Channel 2 of the THMS

Pin Number	Function	Sensor Type Note 1			
		Thermocouple	Pt100 (4-wire)	Pt100 (3-wire)	Pt100 (2-wire)
A1	Excitation0+	NC	Positive current lead of Pt100	Positive current lead of Pt100	Jumper between pins A1 and B2 Note 2
A2	Signal0+	NC	NC	NC	NC
A3	Signal0-	NC	NC	NC	NC
A4	Excitation0-	NC	NC	NC	NC
B1	Excitation1+	NC	NC	NC	NC
B2	Signal1+	Positive lead of thermocouple	Positive signal lead of Pt100	Positive signal lead of Pt100	Positive signal lead of Pt100
B3	Signal1-	Negative lead of thermocouple	Negative signal lead of Pt100	Negative signal lead of Pt100	Negative signal lead of Pt100
B4	Excitation1-	NC	Negative current lead of Pt100	Jumper between pins B3 and B4 Note 2	Jumper between pins B3 and B4 Note 2

Note 1: NC means no connection.

Note 2: This connection is not made by the THMS internally and must therefore be made by the User externally.

# chapter four

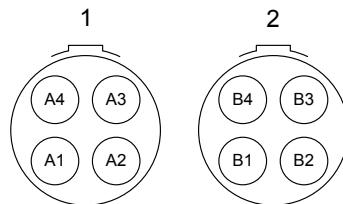


**THMP**  
connection information

The THMP SubModule accepts only Pt100 sensors and provides the following functions:

1. 2 4-pin Lemo EGG.0B.304.CLN connectors for connection to Pt100 sensors.
2. A return path for the excitation current if only one sensor per SubModule is used.
3. TEDS functionality for reading sensor URN (Unique Registration Number)
4. TEDS functionality for SubModule identification.

## THMP Front Panel and Lemo Input Connectors



## Connections between Pt100 Sensors and a THMP

Pin Number	Function	Pt100 (4-wire)
A1	Excitation0+	Positive current lead of first Pt100
A2	Signal0+	Positive signal lead of first Pt100
A3	Signal0-	Negative signal lead of first Pt100
A4	Excitation0-	Negative current lead of first Pt100
B1	Excitation1+	Positive current lead of second Pt100
B2	Signal1+	Positive signal lead of second Pt100
B3	Signal1-	Negative signal lead of second Pt100
B4	Excitation1-	Negative current lead of second Pt100

# getting to know the PAK MKII

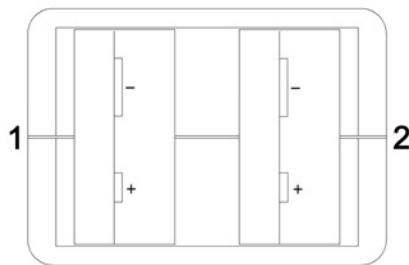
## THME, THMJ, THMK, THMT AND THMU CONNECTION INFORMATION

These SubModules accept E-, J-, K-, T-, and U-type thermocouples, respectively, and provide the following functions:

1. Two dedicated, miniature thermocouple connectors which are color-coded according to the thermocouple type
2. Regular measurements of the thermocouple junction temperatures for cold-junction-compensation
3. TEDS functionality for reading sensor URN (Unique Registration Number)
4. TEDS functionality for SubModule identification.

The figure below shows the THME, THMJ, THMK, THMT or THMU front panel with thermocouple input connectors. The positive thermocouple lead should be connected to the smaller terminal and the negative lead to the larger terminal.

## THME, THMJ, THMK, THMT or THMU Front Panel with Thermocouple Input Connectors



## THME, THMJ, THMK, THMT and THMU

connection information



# chapter four

## ICPM SubModules



### DESCRIPTION

The ICPM SubModule takes the form of a breakout box which is screwed on top of any PAK MKII Mainframe. The ICPM SubModule provides 2 DB50 connectors for 32 ICP channels. Each DB50 connector interfaces to 16 ICP input channels. No more than 2 ICPM SubModules can be stacked on top of the PAK MKII Mainframe.

### TYPES

Two ICPM SubModule types exist, namely:

1. ICPM10 which allows one to connect two DB50 connectors to 32 ICP42 channels with SMB connector cables.
2. ICPM10S which allows one to connect two DB50 connectors to 32 ICP42S channels with 3-pin LEMO connector cables.



# getting to know the PAK MKII

## ICPM Parameters

Parameter	ICPM10	ICPM10S
<b>Input Connectors</b>	2 input DB50 right-angle female connectors	
<b>Cables</b>	32 (50 cm) 2-wire cables	
<b>Output connectors</b>	32 3-pin male Lemo connector outputs	32 SMB connector outputs
<b>Jumper shunts</b>	32 shield jumper shunts	

## ICPM SubModule DB50 Pin-Outs

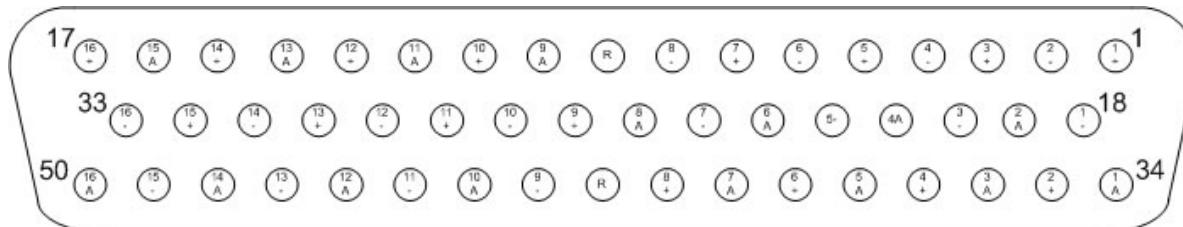
DB50 1 pin	Description	DB50 2 pin	Description
1	channel 1 +	1	channel 17 +
2	channel 2 -	2	channel 18 -
3	channel 3 +	3	channel 19 +
4	channel 4 -	4	channel 20 -
5	channel 5 +	5	channel 21 +
6	channel 6 -	6	channel 22 -
7	channel 7 +	7	channel 23 +
8	channel 8 -	8	channel 24 -
9	No connect	9	No connect
10	channel 9 shield	10	channel 25 shield
11	channel 10 +	11	channel 26 +
12	channel 11 shield	12	channel 27 shield
13	channel 12 +	13	channel 28 +
14	channel 13 shield	14	channel 29 shield
15	channel 14 +	15	channel 30 +
16	channel 15 shield	16	channel 31 shield
17	channel 16 +	17	channel 32 +
18	channel 1 -	18	channel 17 -
19	channel 2 shield	19	channel 18 shield
20	channel 3 -	20	channel 19 -
21	channel 4 shield	21	channel 20 shield
22	channel 5 -	22	channel 21 -
23	channel 6 shield	23	channel 22 shield
24	channel 7 -	24	channel 23 -
25	channel 8 shield	25	channel 24 shield

# chapter four

## ICPM SubModule DB50 Pin-Outs continued

DB50 1 pin	Description	DB50 2 pin	Description
26	channel 9 +	26	channel 25 +
27	channel 10 -	27	channel 26 -
28	channel 11 +	28	channel 27 +
29	channel 12 -	29	channel 28 -
30	channel 13 +	30	channel 29 +
31	channel 14 -	31	channel 30 -
32	channel 15 +	32	channel 31 +
33	channel 16 -	33	channel 32 -
34	channel 1 shield	34	channel 17 shield
35	channel 2 +	35	channel 18 +
36	channel 3 shield	36	channel 19 shield
37	channel 4 +	37	channel 20 +
38	channel 5 shield	38	channel 21 shield
39	channel 6 +	39	channel 22 +
40	channel 7 shield	40	channel 23 shield
41	channel 8 +	41	channel 24 +
42	No connect	42	No connect
43	channel 9 -	43	channel 25 -
44	channel 10 shield	44	channel 26 shield
45	channel 11 -	45	channel 27 -
46	channel 12 shield	46	channel 28 shield
47	channel 13 -	47	channel 29 -
48	channel 14 shield	48	channel 30 shield
49	channel 15 -	49	channel 31 -
50	channel 16 shield	50	channel 32 shield

## NUMBERING OF THE DB50 PINS FOR EACH DB50 CONNECTOR

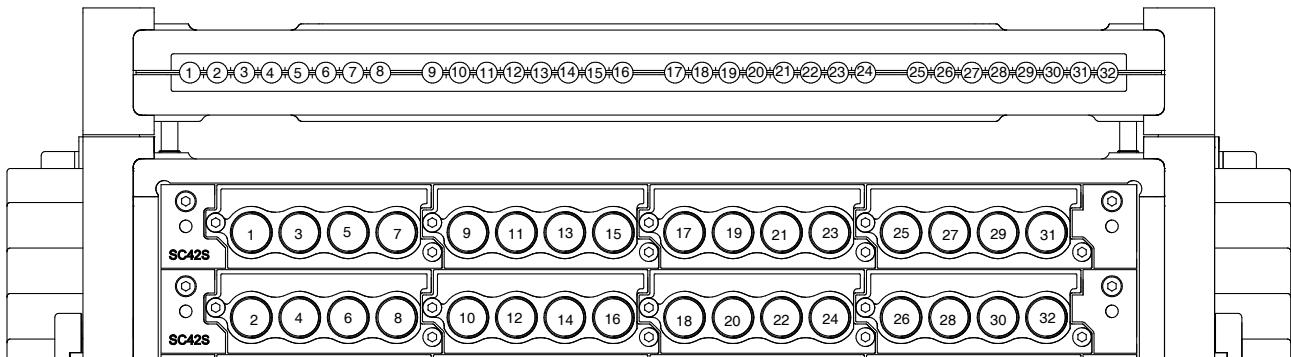


DB-50 pinout diagram

# getting to know the PAK MKII

## INTERFACING THE ICPM SUBMODULE TO THE PAK MKII

There are 32 cables that are fed out of the ICPM SubModule enclosure. These cables connect to ICP modules on the front end of the PAK MKII. Each ICPM SubModule is able to interface 32 channels to the front end of the PAK MKII, which corresponds to 2 fully populated SC42x cards. The channel numbers on the front end of the PAK MKII Mainframe are shown in the figure below. These channel numbers correspond to the channel numbers on the DB50 connectors situated on the front end of the ICPM SubModule enclosure.



ICPM10 Channel numbers

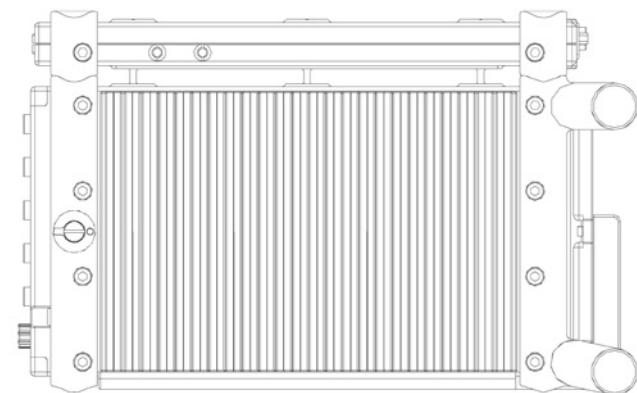
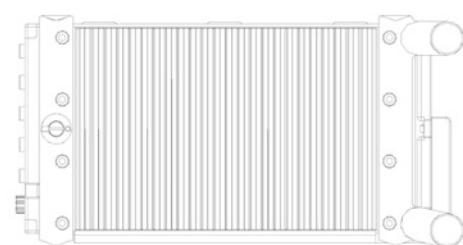
## MOUNTING THE ICPM SUBMODULE ON TOP OF THE PAK MKII

The ICPM SubModule should be mounted on top of the PAK MKII and fastened with 6 M3x4 cap screws into the 6 threaded female fastening points. The cap screws should be fastened with a 2.5 mm hexagon socket. This type of mounting will connect the CGND of the PAK MKII to the CGND of the ICPM SubModule enclosure. The figures on the following pages show a side view of the ICPM SubModule being mounted on top of the PAK MKII enclosure. A 2.5 mm hexagon socket key must be used to fasten the 6 M3x4 cap screws to a torque of 50 cNm (centi-Newton-meter) as illustrated in the figures on the following pages. A second ICPM SubModule can be mounted on top of the first ICPM SubModule to interface an additional 32 channels to the PAK MKII front end. A 2.5 mm socket key must then be used to fasten the inserts of the second ICPM SubModule to the first ICPM SubModule to a torque of 35 cNm. To loosen the second ICPM SubModule, use a 3.2 mm angle open end FACOM wrench to hold the bottom ICPM SubModule insert in place. Use a 2.5 mm socket key to loosen the top insert.

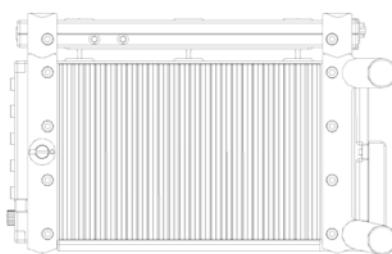
# chapter four

## ICPM10 continued

1

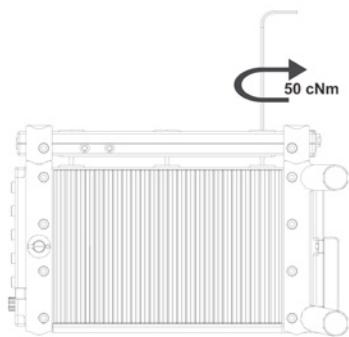


2

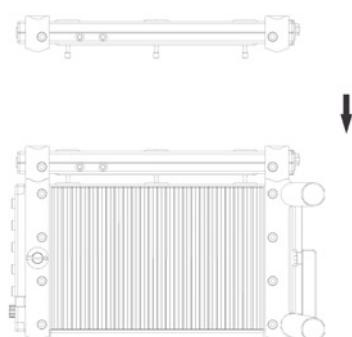


# getting to know the PAK MKII

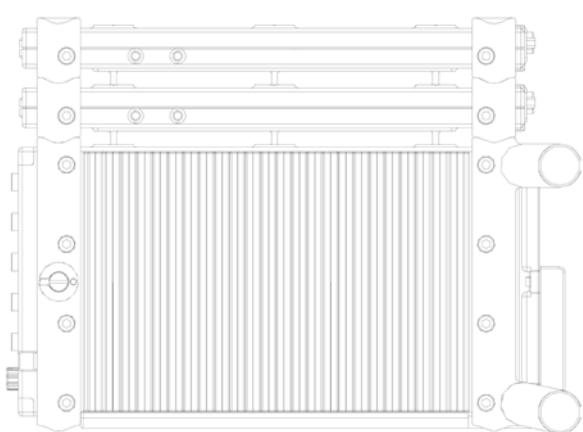
3



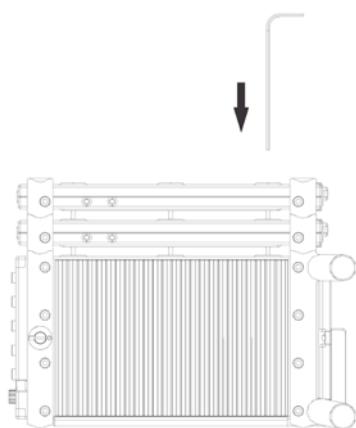
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5



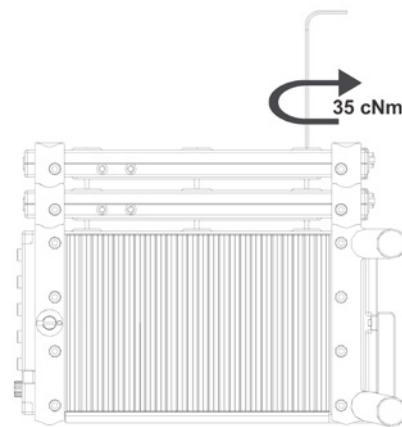
6



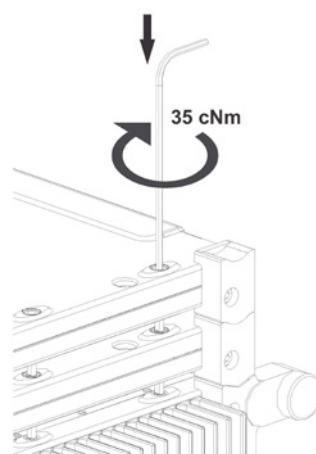
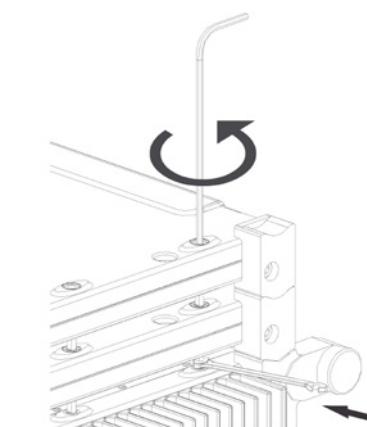
# chapter four

## ICPM10 continued

7

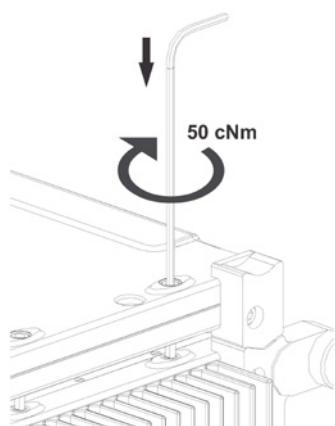


8



# getting to know the PAK MKII

9



## ICPM10

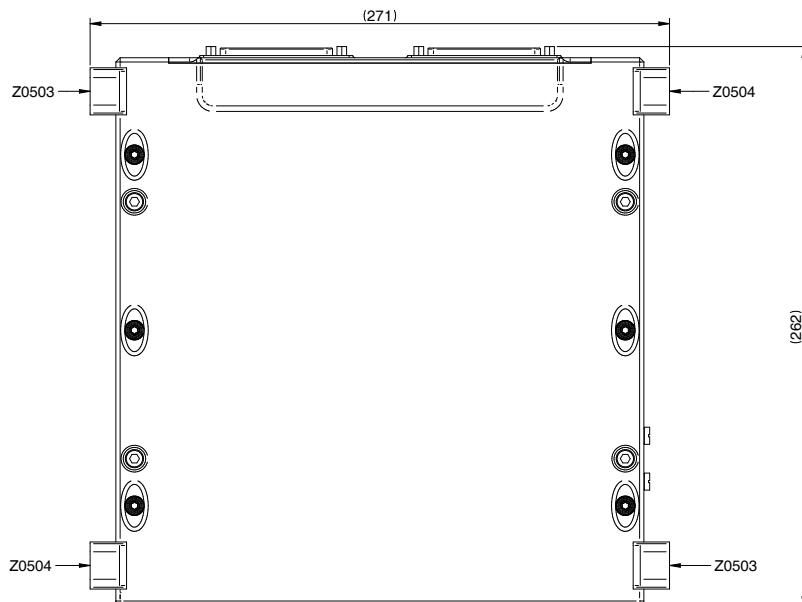
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### ASSEMBLY AND JUMPER SETTINGS

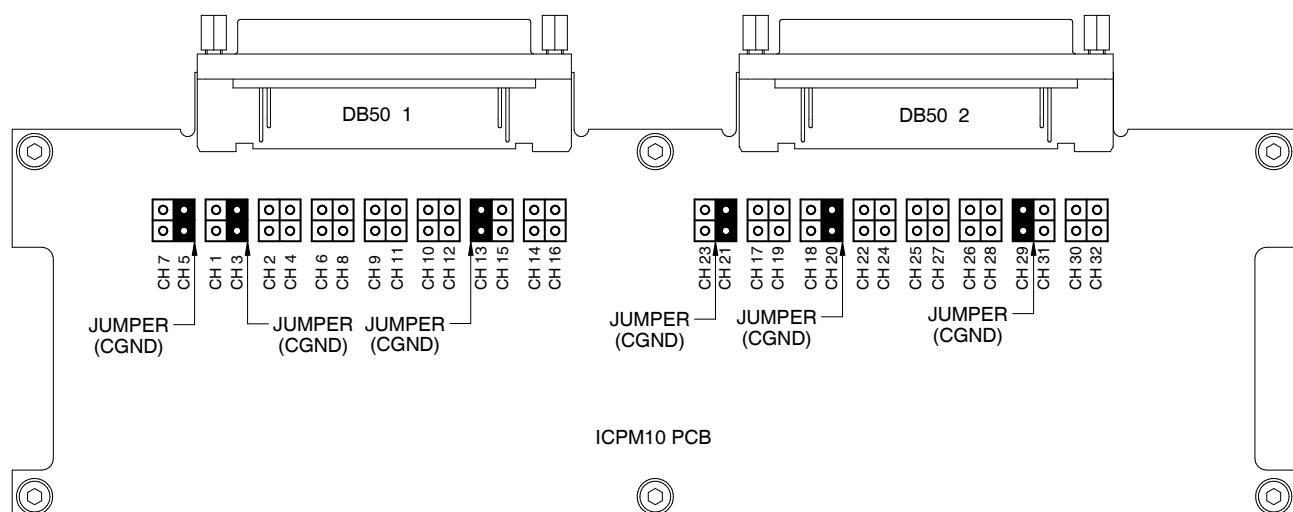
The following procedure must be followed in order to connect/disconnect the shield pins of the DB50 connectors to CGND.

1. Unfasten the 6 M3x4 cap screws on the ICPM SubModule top cover plate using a 2.5 mm hexagon socket key. Remove the ICPM SubModule from the PAK MKII.
2. Loosely unfasten the 2 rear DB50 M3x6 cap screws to the bottom cover plate using a 2.5 mm hexagon socket key on the ICPM SubModule. DO NOT unfasten completely.
3. Unfasten the 4 feet M5x8 cap screws using a 4 mm hexagon socket key. Note that there are two different types of feet, namely Z0503 and Z0504 (see figure ICPM10 ENCLOSURE TOP VIEW). The matching feet should be assembled diagonally to each other.
4. Unfasten the 4 M5x8 cap screws on the ICPM SubModule top cover plate using a 4 mm hexagon socket key, and slowly remove the top cover plate. Once the top cover plate is removed the ICPM SubModule PCB should be visible. The shield jumpers can be placed or removed with tweezers for each channel on the ICPM SubModule PCB (figure ICPM10 PCB (JUMPER SETTING)). The jumper shunts connect the DB50 shield pins to CGND. The jumper shunts are not connected to the negative signal. The channel number for each shield pin is indicated on the ICPM SubModule PCB alongside the jumper pins. Two jumper shunts can be connected per connector header. The jumper should be placed over the two pins with tweezers.
5. Once the jumpers have been set as desired, place the top cover plate back on to the ICPM SubModule.
6. Fasten the 4 M5x8 cap screws on the ICPM SubModule top cover plate using a 4 mm hexagon socket key.
7. Fasten the 2 M3x6 cap screws on the rear DB50 cover using a 2.5 mm hexagon socket key.
8. Fasten the 4 feet M5x8 cap screws using a 4 mm hexagon socket key.
9. Finally, fasten the ICPM SubModule to the top of the PAK MKII Mainframe with the 6 M3x4 cap screws using a 2.5 mm hexagon socket key.

# chapter four



ICPM10 ENCLOSURE TOP VIEW



ICPM10 PCB (JUMPER SETTING)

## getting to know the PAK MKII



### ICTV11

The ICTV11 is used to protect the ICT42 Module's tacho inputs from excessively high voltages. These may occur when inductive devices are discharged or when measuring close to high voltage circuitry.

The SubModule contains high energy overvoltage dissipation devices. These devices limit the output voltage to reasonable values which will not destroy the internal circuitry of the ICT42 Modules.

A BNC connector is provided on the SubModule to interface to the appropriate tacho sensor. The SubModule connects to the ICT42 Module through a 300 mm fly-lead ending with a 4 way Lemo FGG 0B connector.

# chapter four

Accessories

Enhance the PAK MKII

# getting to know the PAK MKII

The MiniTerminal is a remote interactive User interface that allows additional interaction between the User and PAK software. The MiniTerminal connects to the VME Controller via a serial cable supplied with the MiniTerminal. This is useful in scenarios where it is difficult or unsafe for the User to physically reach the PAK MKII User interface.

## MiniTerminal

### TYPES

The MiniTerminal hardware versions are categorized by its capability to support in-field firmware upgrades through its serial cable. The hardware versions that support it are called type MT11b, and those who don't are called type MT11a. The following table outlines the differences between the different hardware versions.

Hardware version	Supports firmware upgrade	Firmware type	Connector type	Buttons	Display size	Status LEDs	Cable length	Voltage input
MT100, MT110	No	MT11a	2 x RJ9	6	Normal	3	2 m	5V
MT111	Yes	MT11b	2 x RJ9	6	Normal	3	2 m	5V
MT123	Yes	MT11b	2 x 7-pin LEMO	7 (Note 1)	Large	3	2 to 5 m (Note 2)	5V to 12V

*Note 1:* The seventh button is used to remotely switch on the latest PQ30 MKII systems, when power or battery power is present. Just press and hold the seventh button until the PAK MKII switches on.

*Note 2:* The brightness level will be limited by the MiniTerminal if not connected to a PQ30 controller card. Readability is not compromised due to larger display size.

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## MiniTerminal continued

### NOTE:

1. Do not connect/disconnect the MiniTerminal to/from the PAK MKII while the PAK MKII is booting. Booting as it is referred to here refers to the period from when the PAK MKII is powered-up (or reset) until `Idle...` or `Idle` appears on the PAK MKII display.
2. Power to the MiniTerminal will not be toggled when the PAK MKII User interface command `SYSRST?` or `RST?` is executed. To recycle power to the MiniTerminal, the PAK MKII must be powered down and powered up again. The PAK MKII will perform its MiniTerminal detection procedure only once per PAK MKII power-up/down cycle.
3. For mounting the MT11 on a tripod an “1/4-20 UNC” screw on the back of the MT11 exists.



MiniTerminal versions with normal display size



MiniTerminal versions with larger display size

### CONNECTING THE MINITERMINAL TO THE PAK MKII

To connect the MiniTerminal to the PAK MKII, use the supplied serial cable and insert one end into any one of the two connectors of the MiniTerminal, and the other end into the PAK MKII “SER1/2” port (7-pin Lemo for a PQ12, PQ20, PQ30, PQ30S or VS20x).

### MINITERMINAL DETECTION BY THE PAK MKII

The MiniTerminal receives its power through the serial cable. Connect the MiniTerminal to the PAK MKII either when the PAK MKII is powered-down or after the PAK MKII has booted (`Idle...` or `Idle` appears on the PAK MKII display). Note that since the MiniTerminal is autodetected by the PAK MKII, the MiniTerminal may be connected at any time after the PAK MKII has booted.

The MiniTerminal detection procedure consists of the following:

1. Step 1: When the MiniTerminal receives power, it will first boot up and when complete, clear the LEDs and write its firmware version to the display. Note that if an error occurred while upgrading the MiniTerminal, the display and LEDs will remain off when the MiniTerminal is connected to the PAK MKII. When this error state is detected by the PAK MKII, it will attempt to perform the upgrade procedure to repair the MiniTerminal. The upgrade procedure will be discussed in the steps below.
2. Step 2: As soon as the PAK MKII has booted, it will begin to periodically test whether a MiniTerminal is connected.
3. Step 3: When a MiniTerminal is detected, the PAK MKII will clear the display and set

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LED 2 (amber). Please note that previous versions of the PAK MKII firmware would at this point request from the User to select the MiniTerminal mode. In such a case, the User should just select "PAK". As long as the same PAK MKII Controller card is used, the request will not appear on subsequent occasions when the MiniTerminal is detected by the PAK MKII.

4. Step 4: The PAK MKII will now determine if the MiniTerminal supports upgrading of its firmware and, if true, determine whether the current firmware executing on the MiniTerminal is the same as that stored on the PAK MKII. If the MiniTerminal firmware version is different, the PAK MKII will perform the upgrade procedure to upgrade the firmware stored on the MiniTerminal. If the firmware is the same or the MiniTerminal does not support upgrading, continue at step 8.
5. Step 5: When the upgrade procedure starts, the MiniTerminal display and LEDs will be off (it will appear as if the MiniTerminal was powered-down). The message `Wait:UMT` or `:UMT` will appear on the PAK MKII display. The upgrade process may take up to 20 seconds.
6. Step 6: If `Reboot` or `boot` appears on the PAK MKII display, it means that the upgrade procedure was successful and that power to the MiniTerminal must be recycled for the new firmware to execute. Continue once again at step 1 of the detection procedure.
7. Step 7: If `UMTerror` or `err` appears on the PAK MKII display, it means an error occurred during the upgrade procedure. If step 1 is performed again, the MiniTerminal display and LEDs will remain off. To recover the MiniTerminal from this error state, firstly disconnect the MiniTerminal and only reconnect it to the PAK MKII after the PAK MKII has booted. If the PAK MKII detects the MiniTerminal in its error state, the PAK MKII will perform the upgrade procedure again. Continue at step 5.
8. Step 8: LED 2 (amber) will be cleared and LED 3 (green) set when the PAK MKII has completed the detection procedure and is ready for normal operation. The display will also be off.

After the MiniTerminal is detected by the PAK MKII, the upgrade procedure will be repeated if PAK software upgrades the PAK MKII with new MiniTerminal firmware. As mentioned previously during the upgrade procedure, the MiniTerminal display and LEDs will be off and the message `Wait:UMT` or `:UMT` will appear on the PAK MKII display.

## MiniTerminal continued

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## SeatFrame

The SeatFrame allows PAK MKII front ends to be mounted together with a notebook onto a car seat.

### NOTE:

The SeatFrame can only be used together with the Mainframes MF02, MF03, MF04 and MF06.

### FEATURES

1. Consists of machined aluminum
2. Side feet can be adjusted in width to suit the seat
3. Can be disassembled and folded for easy transportation
4. Equally suited for both left hand and right hand drive vehicles
5. Multiple settings and adjustments allows the notebook to be placed in the position that best suits the User

### TYPES

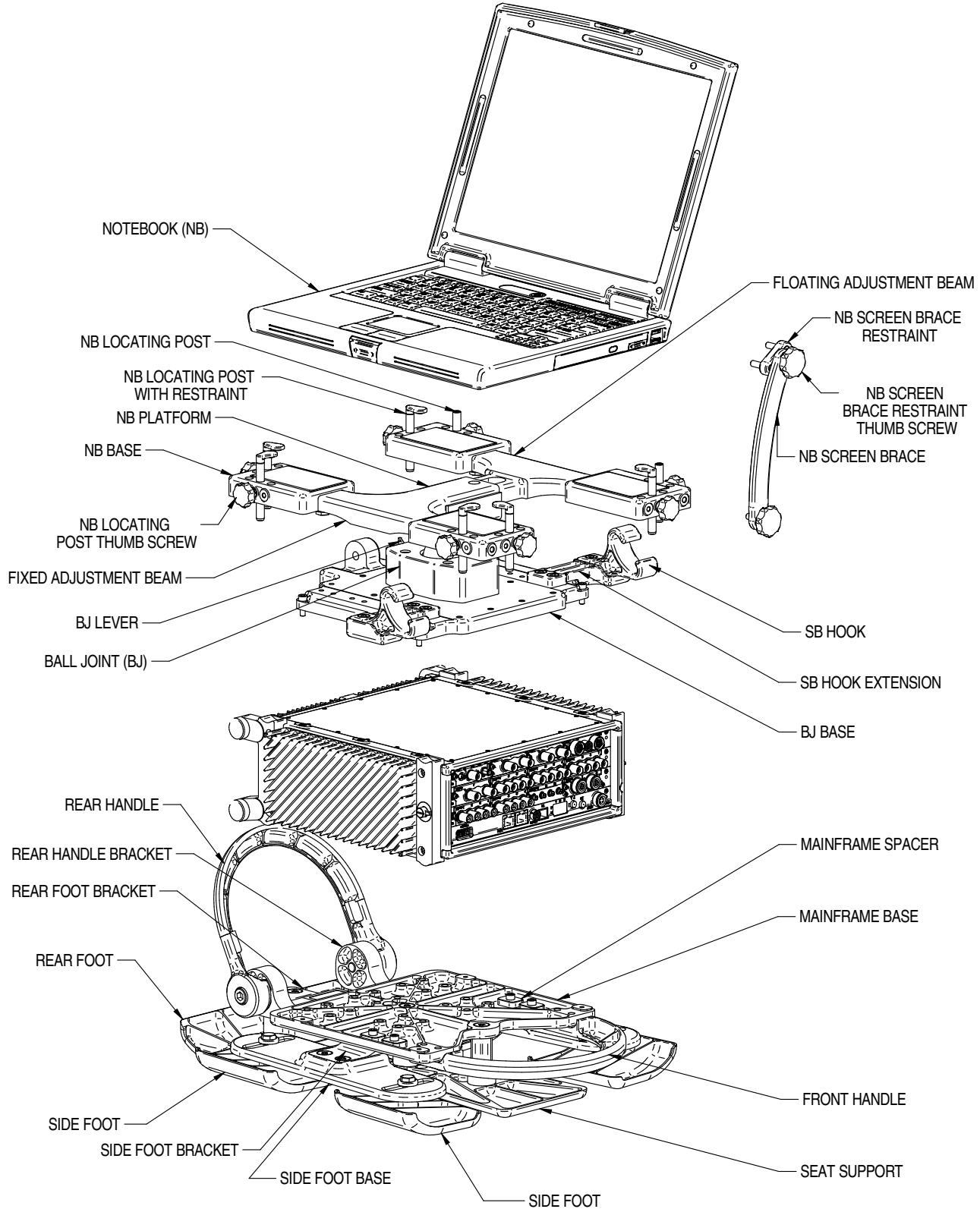
The following SeatFrame versions exist:

1. SF10



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## GLOSSARY OF SEATFRAME TERMS



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## Fitting a PAK MKII (MF02, MF03 or MF04 without fans) to a Seat- Frame

### Preparing to fit a MF02, MF03 or MF04 Mainframe without fans

1. When mounting a MF02 or MF03 Mainframe to the SeatFrame, loosen the Mainframe Spacers from its placeholders using a 4 mm Allen key.
2. Place the spacers in the 4 outer positions as shown in step 2.
3. Place the Mainframe on the Mainframe Base of the SeatFrame.

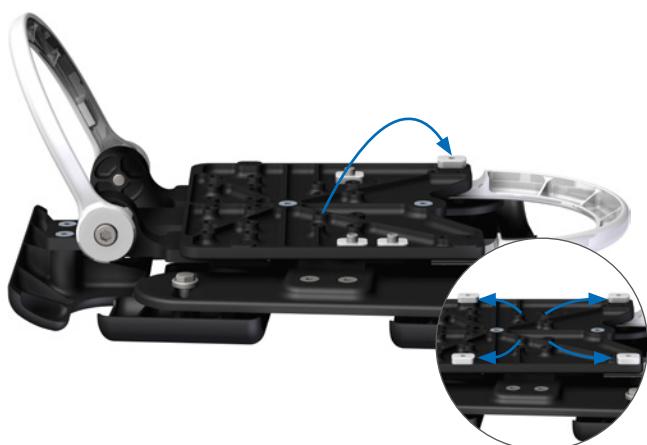
### NOTE:

Spacers are required as these mainframes do not have plenum covers.

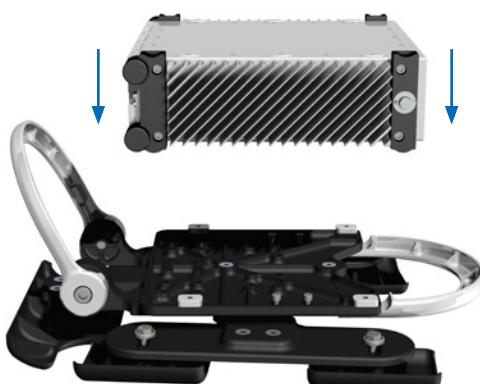
1



2



3



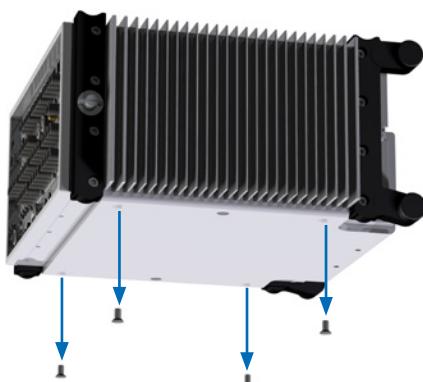
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1



Fitting  
a PAK MKII  
(MF04 or MF06  
with fans) to a  
SeatFrame

2



Preparing to fit a MF04 or MF06  
Mainframe with fans

1. When mounting a MF04 or MF06 Mainframe to the SeatFrame, fasten the Mainframe Spacers in its placeholders using a 4 mm Allen key.
2. Temporarily remove the 4 M5 screws holding the Plenum Cover at the bottom of the Mainframe.
3. Place the Mainframe on the Mainframe Base of the SeatFrame.

3



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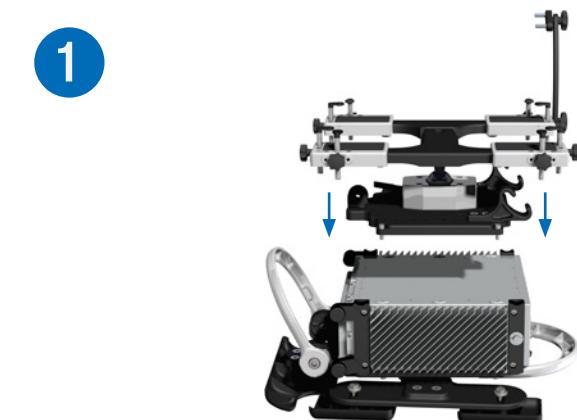
## Securing a Mainframe to the SeatFrame

1. Tighten the Mainframe to the Mainframe Base using M5 captive screws provided and a 8 mm Spanner in the 4 positions provided.



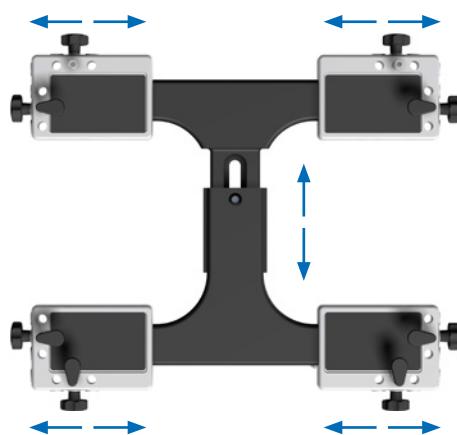
## Fastening the Notebook Platform with Ball Joint Base to Mainframe

1. Place the Notebook Platform with Ball Joint Base on top of the Mainframe.
2. Fasten the Ball Joint Base to the Mainframe using the M5x16 cap screws provided and a 4 mm Allen key in the 4 positions provided.



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1



## Adjusting the Notebook Platform to fit Notebook Size

2



1. The Notebook Platform is adjustable in the horizontal and vertical directions.
2. Loosen the M8 bolts under the 4 Notebook Bases with a 13 mm Spanner.

Move the Notebook Bases to accommodate Notebook length.  
Loosen the M8 bolts under the Notebook Platform with a 13 mm Spanner.

Move the Floating Adjustment Beam to accommodate Notebook width.

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## Securing the Notebook to the Notebook Base

1. Place the Notebook on the Notebook Platform.
2. Insert the Notebook Locating Post into the Notebook Base.

Tighten the locating pin thumb screw by hand.

Repeat this on all 8 Notebook Posts on each of the 4 Notebook Bases.



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1



## Securing the Notebook Screen

1. Attach the Notebook Screen Brace to the Notebook Platform by using the thumb screw provided.
2. To support the screen, pivot the Screen Brace Restraint to clamp the screen and fasten it using the Screen Brace Restraint thumb screw.



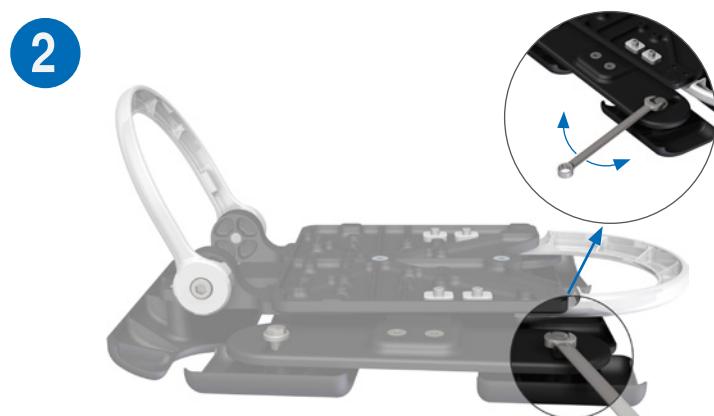
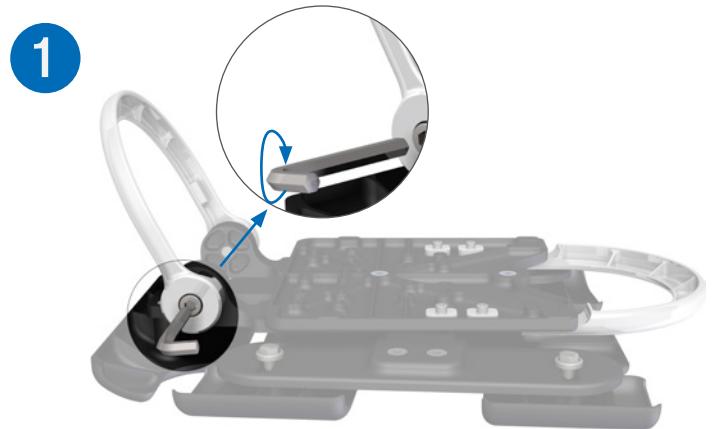
2



# chapter four

## Situational Adjustments

1. To support the angle of the Seat Back Rest, adjust the rear handle using a 8 mm Allen key to loosen and fasten the M10 cap screw.
2. Adjust side feet back and forth to fit the shape of the car seat comfortably using a 13 mm spanner.
3. Move the Ball Joint Leaver to the right and turn the notebook platform to the desired position. Toggle the Ball Joint Leaver again to fix the position.



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1



## Situational Adjustments

2



1. Depending on the Notebook size, the Notebook may interfere with a Safety Belt Hook.  
2. Should this occur, screw on the Safety Belt Hook extension using the M6 screws provided and a 5 mm Allen key.

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## CE Compliance

### NOTE:

CE compliance applies only to the PAK MKII components listed in the adjacent table.

CE marking on the PAK MKII indicates compliance to the EMC Directive (89/336/EEC) and Low Voltage Directive (73/23/EEC).

Under the EMC Directive the PAK MKII was tested to fulfill the following requirement:

- SABS IEC 61326-1 Minimum Requirements (Electrical equipment for measurement, control and laboratory use – EMC requirements)

In fulfilling this requirement the PAK MKII was tested against the following standards:

1. Emissions (each component is classified as Class A or B in the table below):
  - SABS CISPR 22 (Information technology equipment – Radio disturbance characteristics – Limits and methods of measurement)
2. Immunity:
  - IEC 61000-4-2 (Electrostatic discharge immunity test)
  - IEC 61000-4-3 (Radiated, radio-frequency, electromagnetic field immunity test)
  - IEC 61000-4-4 (Electrical fast transient/burst immunity test)
  - IEC 61000-4-5 (Surge immunity test)
  - IEC 61000-4-6 (Immunity to conducted disturbances, induced by radio-frequency fields)
3. The PAK MKII was tested to fulfill the following requirement under the Low Voltage Directive:
  - SABS IEC 61010-1 (Safety requirements for electrical equipment for measurement, control, and laboratory use – General requirements)

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## CE-compliant PAK MKII Components

Parameter	Component	Comment (Note 1)
Mainframes	MF02 (M515)	Class B
	MF03 (M381)	Class B
	MF04 (M386)	Class B
	MF06 (M382)	Class B
	MF10 (M395)	Class B
VMEbus boards	PQ12, PQ20	Class B
	SC42, SC42S	Class B
	PQ30	Class B
	SL21	Class A
Modules	ICP42, ICP42S	Class B, Note 2
	ICP42B	Class A
	ICM42S	Class A
	ICT42, ICT42S	Class B, Note 2
	ALO42S	Class B
	MIC42X	Class B
	CHG42	Class B, Note 2
	DCH42S	Class B, Note 2
	CAN42	Class B
	DAR42	Class A, Note 2, Build C only
	WSB42	Class B
	THM42	Class B
	ECT42	Class B
	FLX42	Class B
	IRG42	Class B
	GPS42	Class B
MiniTerminal	MT11	Class B

Note 1: For a complete PAK MKII system to be Class B, all of its components must be Class B.

Note 2: Only compliant if the length of any cable connected to the Module is less than 30 m.

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