United International University
QUEST FOR EXCELLENCE

CSE 1326: Digital Logic Design Lab
Decoders

United International University

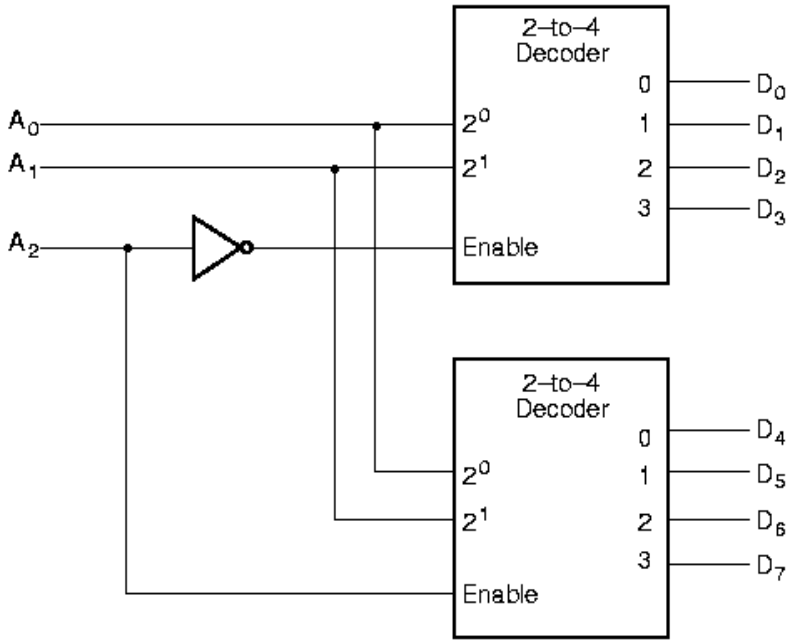
What to do (skip grayed colored ones)

1. Implementation: Implement 3-to-8 line decoder using
   a) Basic gates, AND gate with more inputs - Non-hierarchical
   b) Decoder and two-input AND gates - Hierarchical (LS)
   c) 2-to-4 line decoders with enable (Both TB and LS)
2. Application: Implement combinational circuits (functions) using decoder and basic gates

   $F = M_1 . M_3 . M_6 . M_7$

What To Do (1c)

1c) Implement a 3-to-8 line decoder using 2-to-4 line decoders with enable (see below) – Both TB and LS.



IC: 74139 dual 2-to-4 Decoder

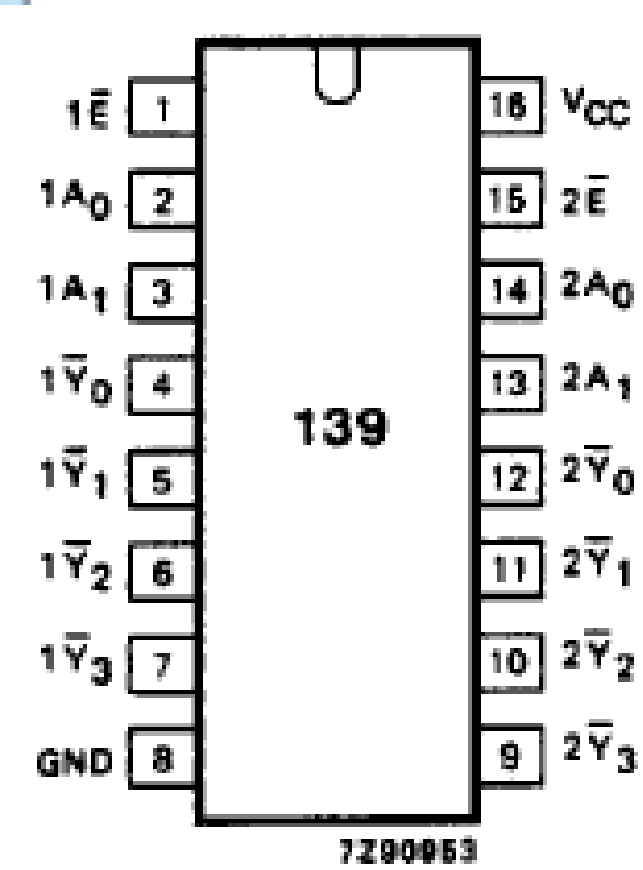
Function Table of 74LS139

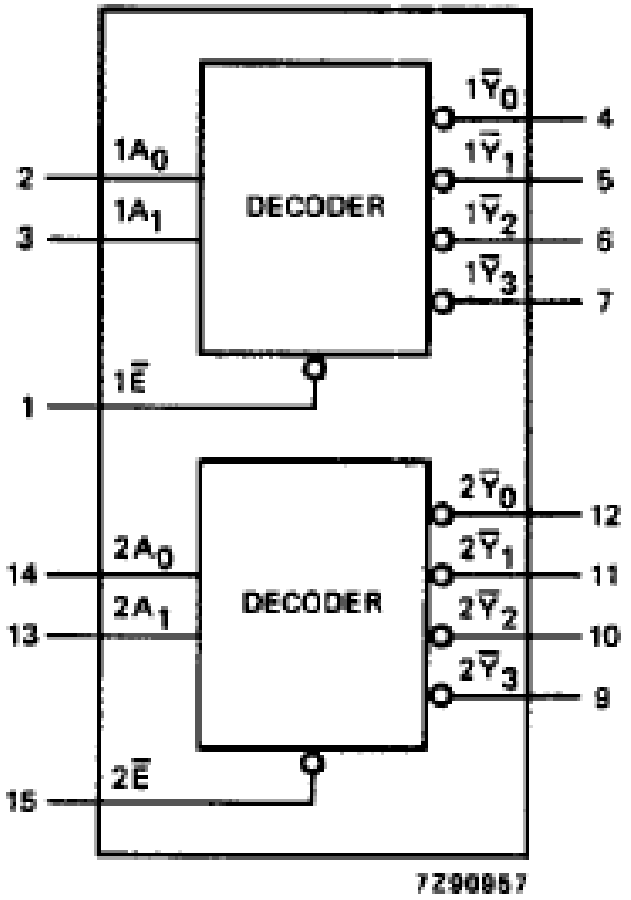
INPUTS			OUTPUTS			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

1 = High, 0 = Low, X = don't care

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{E}$, $2\overline{E}$	enable inputs (active LOW)
2, 3	$1A_0$, $1A_1$	address inputs
4, 5, 6, 7	$1\overline{Y}_0$ to $1\overline{Y}_3$	outputs (active LOW)
8	GND	ground (0 V)
12, 11, 10, 9	$2\overline{Y}_0$ to $2\overline{Y}_3$	outputs (active LOW)
14, 13	$2A_0$, $2A_1$	address inputs
16	V_{CC}	positive supply voltage

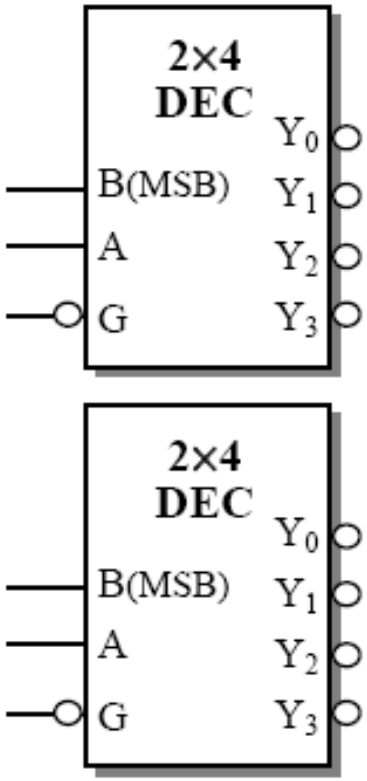
Functional/Pin Diagram

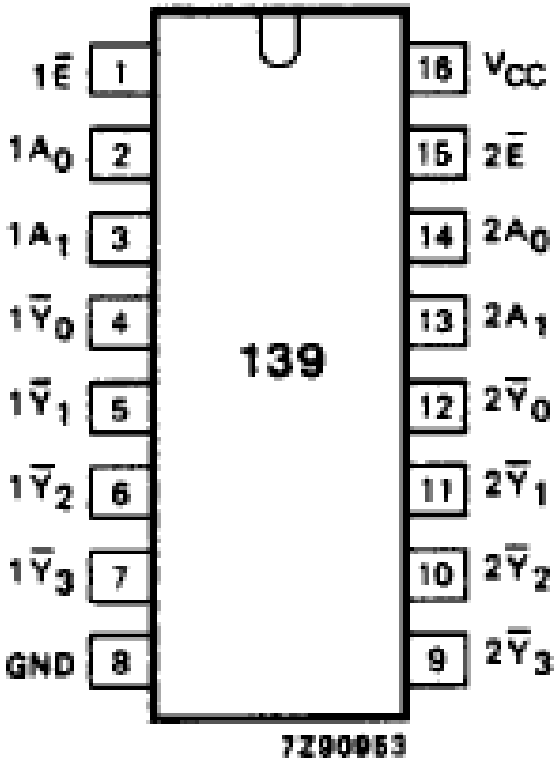




Implement a 3-to-8 line Decoder

- Following that pattern complete this connection using 74139, note the pin numbers





What To Do (2)

2. Application: Implement combinational circuits (functions) using decoder and basic gates.

$$F = M_1 . M_3 . M_6 . M_7$$

a) For trainer board, use the circuit in 1c.
b) For LS, use SOM, F=m0+m2+m4+m5

- Active-low decoders generate maxterms.
- If you have a product of maxterms equation for a function, you can easily use a active-low decoder and AND gates to implement that function.
- But, in logisim, there is no Active-low decoder. What can we do?

Writing Report (skip grayed colored ones)

1. Pin diagram of 74139 (with two 2-to-4 decoders inside).
2. Logic diagram of 3-to-8 line decoder implementation
   a) Basic gates, non-hierarchical (AND gate more inputs)
   b) Basic gates, hierarchical (Decoder and AND gate – two inputs)
   c) 2-to-4 line decoders with enable
3. Logic diagram of realizing combinational circuits using 3-to-8 line decoder

   $F = M_1 . M_3 . M_6 . M_7$
4. Answer the question: How to use the 3-to-8 line decoder (the one you have designed with two 2-to-4 line decoders) for implementing the following function?

   $F = m_0 + m_4 + m_5 + m_7$