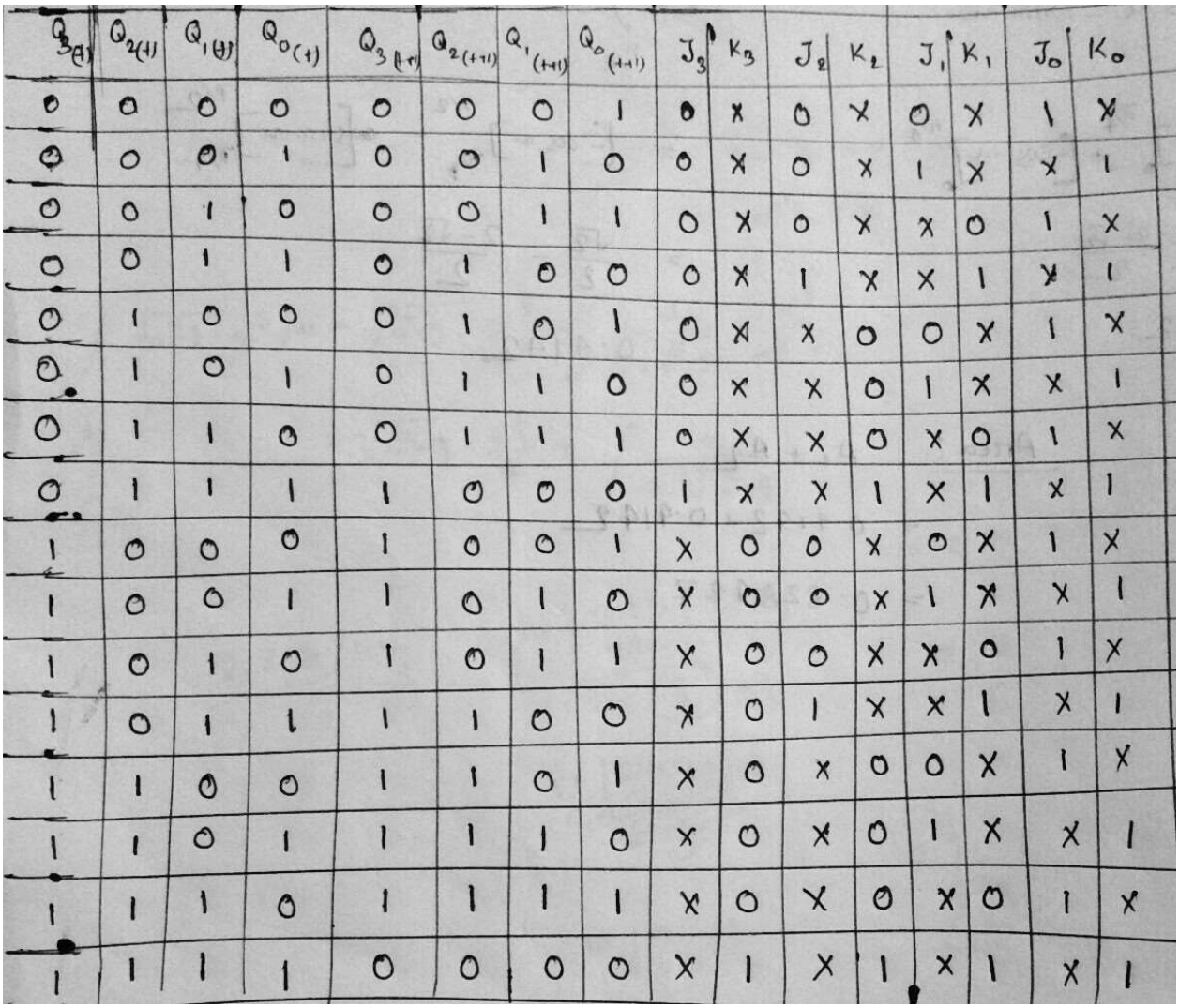
Objective:

Design a BCD to 7-Segment Decoder using Logisim to create a digital circuit that takes Binary Coded Decimal (BCD) input and converts it into the corresponding output to drive a 7-segment display. Demonstrate the ability to use logical gates and components effectively to achieve accurate BCD to 7-segment decoding, showcasing a clear understanding of digital circuit design principles and the functionality of 7-segment displays.

Truth Table of Ripple Counter :

0<1<2<3<4<5<6<7<8<9<10<11<12<13<14<15



$Q_{3(t)}$	$Q_{2(t)}$	$Q_{1(t)}$	$Q_{0(t)}$	$Q_{3(t+1)}$	$Q_{2(t+1)}$	$Q_{1(t+1)}$	$Q_{0(t+1)}$	J_3	K_3	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	0	0	0	1	0	X	0	X	0	X	1	X
0	0	0	1	0	0	1	0	0	X	0	X	1	X	X	1
0	0	1	0	0	0	1	1	0	X	0	X	X	0	1	X
0	0	1	1	0	1	0	0	0	X	1	X	X	1	X	1
0	1	0	0	0	1	0	1	0	X	X	0	0	X	1	X
0	1	0	1	0	1	1	0	0	X	X	0	1	X	X	1
0	1	1	0	0	1	1	1	0	X	X	0	X	0	1	X
0	1	1	1	1	0	0	0	1	X	X	1	X	1	X	1
1	0	0	0	1	0	0	1	X	0	0	X	0	X	1	X
1	0	0	1	1	0	1	0	X	0	0	X	1	X	X	1
1	0	1	0	1	0	1	1	X	0	0	X	X	0	1	X
1	0	1	1	1	1	0	0	X	0	1	X	X	1	X	1
1	1	0	0	1	1	0	1	X	0	X	0	0	X	1	X
1	1	0	1	1	1	1	0	X	0	X	0	1	X	X	1
1	1	1	0	1	1	1	1	X	0	X	0	X	0	1	X
1	1	1	1	0	0	0	0	X	1	X	1	X	1	X	1

Figure 1 : Truth Table of 4 bit Ripple Counter

K map of ALL Flip Flops input output:

Q_3Q_2 \ Q_1Q_0	$Q_1'Q_0'$ 00	$Q_1'Q_0$ 01	Q_1Q_0 11	Q_1Q_0' 10
$Q_3'Q_2'$ 00	0	1	3	2
$Q_3'Q_2$ 01	4	5	1 7	6
Q_3Q_2 11	X 12	X 13	X 15	X 14
Q_3Q_2' 10	X 8	X 9	X 11	X 10

$J_3: Q_2 Q_1 Q_0$

Q_3Q_2 \ Q_1Q_0	$Q_1'Q_0'$ 00	$Q_1'Q_0$ 01	Q_1Q_0 11	Q_1Q_0' 10
$Q_3'Q_2'$ 00	X 0	X 1	X 3	X 2
$Q_3'Q_2$ 01	X 4	X 5	X 7	X 6
Q_3Q_2 11	X 12	X 13	1 15	X 14
Q_3Q_2' 10	8	9	11	10

$K_3: Q_2 Q_1 Q_0$

Q_3Q_2 \ Q_1Q_0	$Q_1'Q_0'$ 00	$Q_1'Q_0$ 01	Q_1Q_0 10	Q_1Q_0' 10
$Q_3'Q_2'$ 00	0	1	1 3	2
$Q_3'Q_2$ 01	X 4	X 5	X 7	X 6
Q_3Q_2 10	X 12	X 13	X 15	X 14
Q_3Q_2' 10	8	9	1 11	10

$J_2: Q_1 Q_0$

	00	01	10	10
00	X 0	X 1	X 3	X 2
01	4	5	1 7	6
11	12	13	1 15	14
10	X 8	X 9	X 11	X 10

$K_2: Q_1 Q_0$

Q_3Q_2 \ Q_1Q_0	$Q_1'Q_0'$ 00	$Q_1'Q_0$ 01	Q_1Q_0 11	Q_1Q_0' 10
$Q_3'Q_2'$ 00	1 0	X 1	X 3	X 2
$Q_3'Q_2$ 01	X 4	X 5	X 7	X 6
Q_3Q_2 11	X 12	X 13	X 15	X 14
Q_3Q_2' 10	X 8	X 9	X 11	X 10

$J_1: Q_0$

Q_3Q_2 \ Q_1Q_0	$Q_1'Q_0'$ 00	$Q_1'Q_0$ 01	Q_1Q_0 11	Q_1Q_0' 10
$Q_3'Q_2'$ 00	X 0	X 1	1 3	2
$Q_3'Q_2$ 01	X 4	X 5	1 7	6
Q_3Q_2 11	X 12	X 13	1 15	14
Q_3Q_2' 10	X 8	X 9	1 11	10

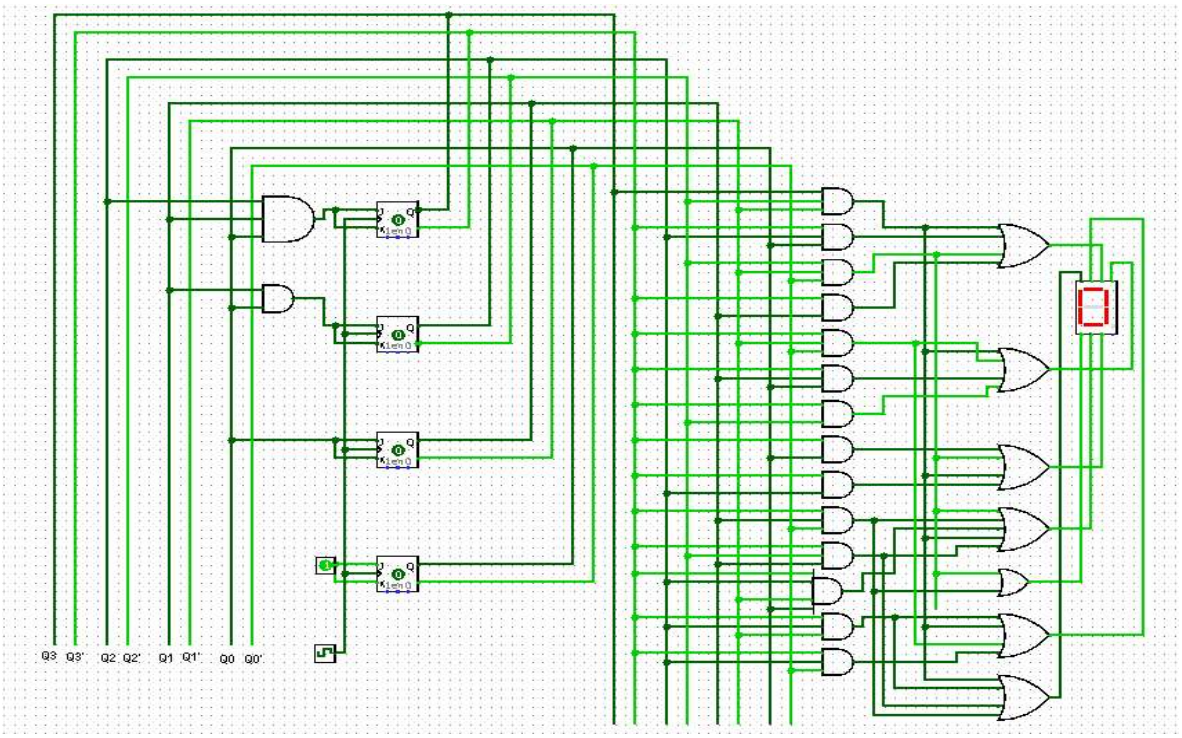
$K_1: Q_0$

Q_3Q_2 \ Q_1Q_0	$Q_1'Q_0'$ 00	$Q_1'Q_0$ 01	Q_1Q_0 11	Q_1Q_0' 10
$Q_3'Q_2'$ 00	1 0	X 1	X 3	1 2
$Q_3'Q_2$ 01	1 4	X 5	X 7	1 6
Q_3Q_2 11	1 12	X 13	X 15	1 14
Q_3Q_2' 10	1 8	X 9	X 11	1 10

$J_0: 1$

Q_3Q_2 \ Q_1Q_0	$Q_1'Q_0'$ 00	$Q_1'Q_0$ 01	Q_1Q_0 11	Q_1Q_0' 10
$Q_3'Q_2'$ 00	X 0	1 1	1 3	X 2
$Q_3'Q_2$ 01	X 4	1 5	1 7	X 6
Q_3Q_2 11	X 12	1 13	1 15	X 14
Q_3Q_2' 10	X 8	1 9	1 11	X 10

$K_0: 1$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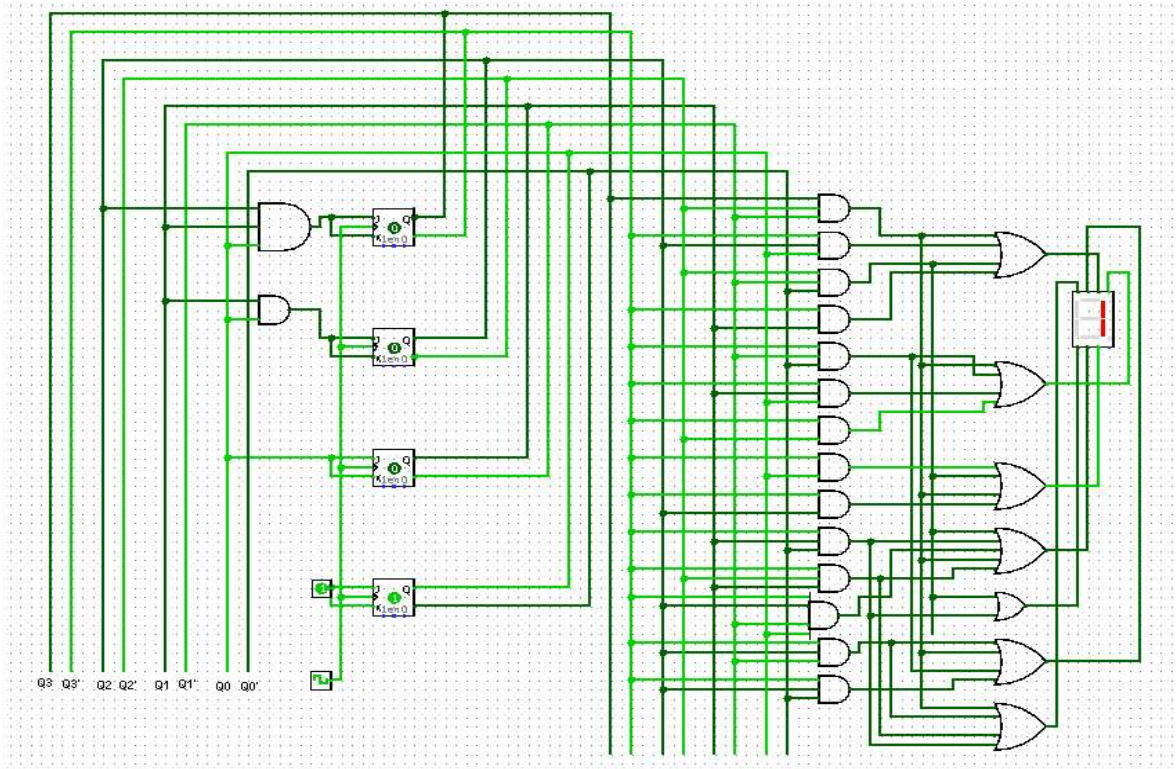
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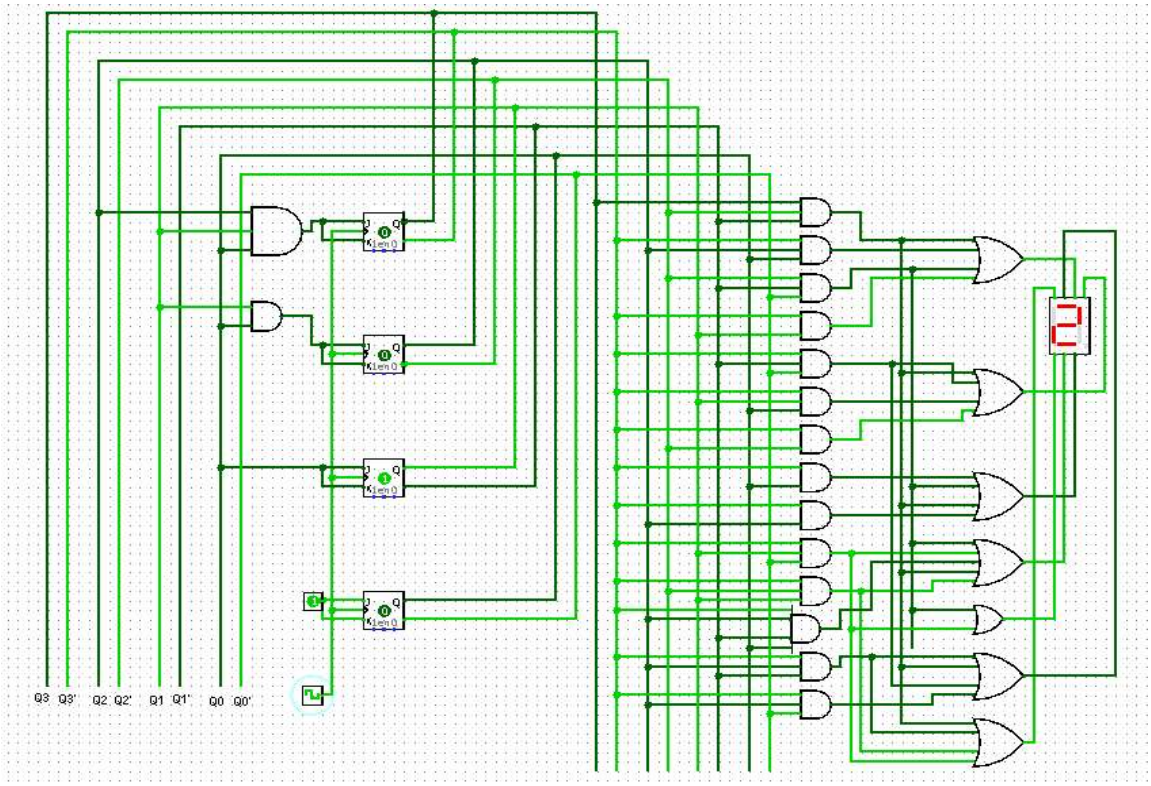
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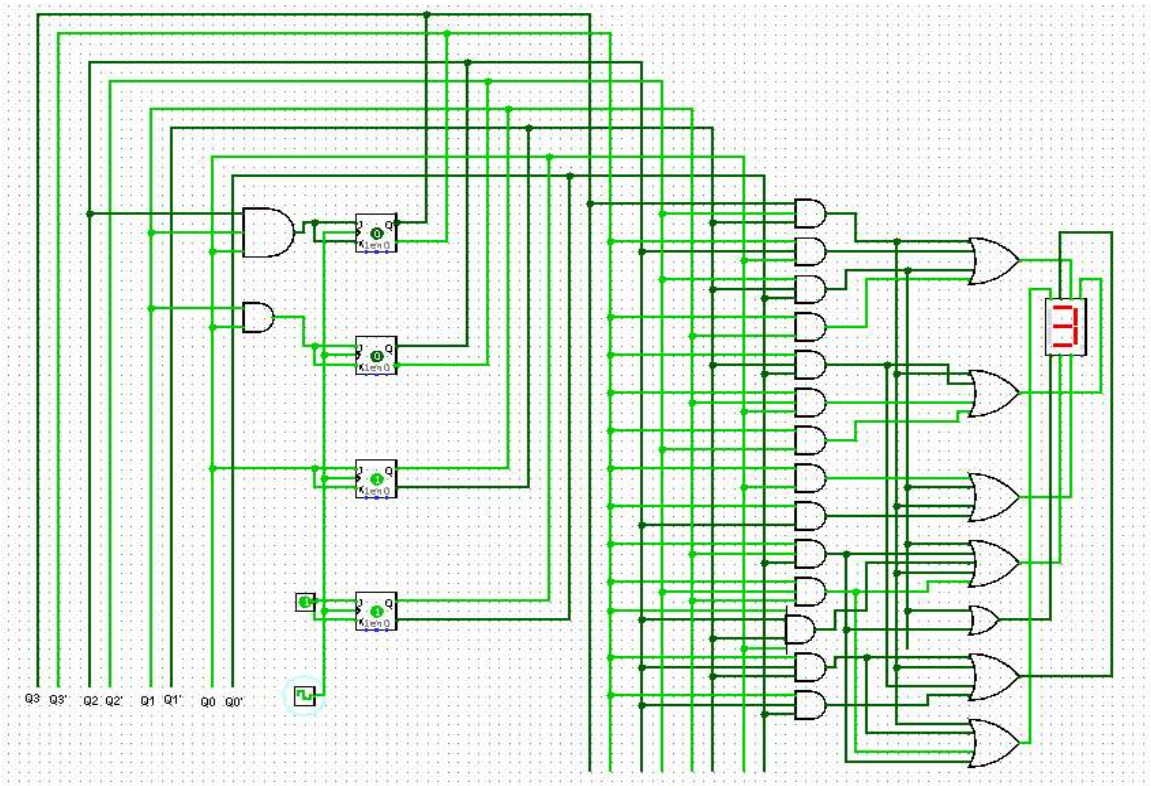
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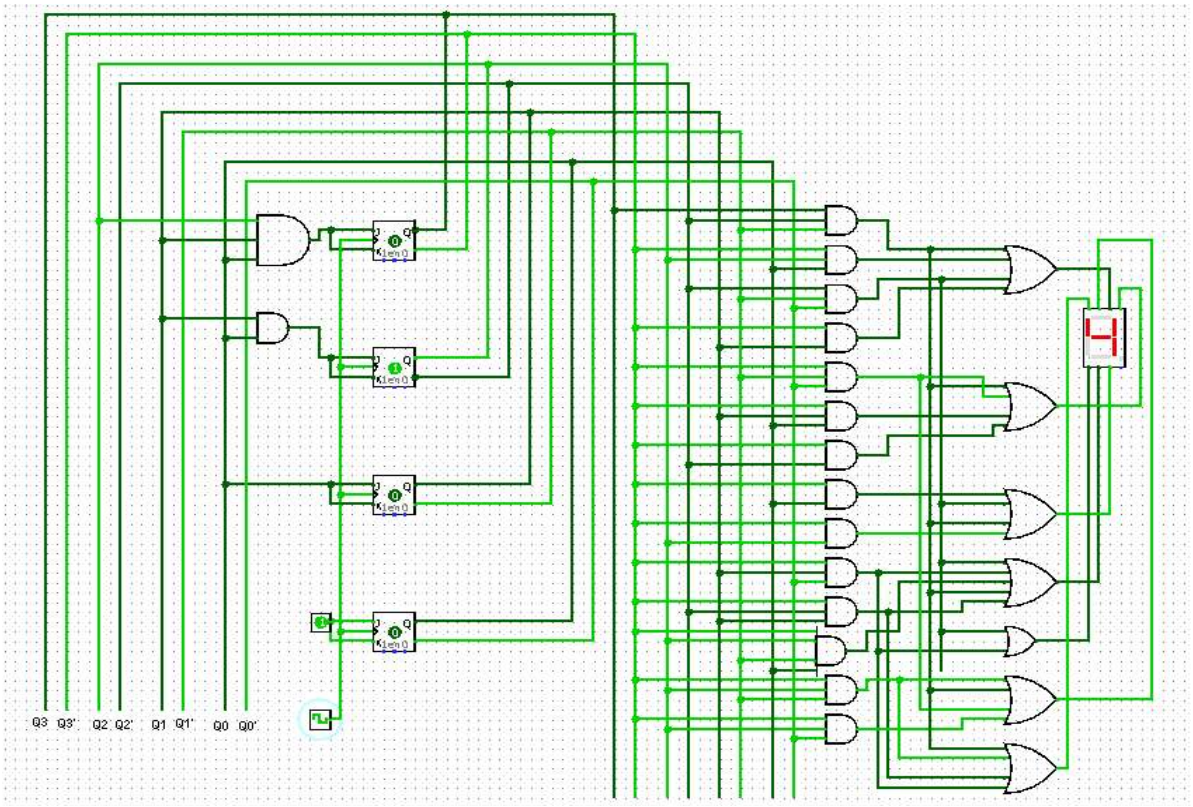
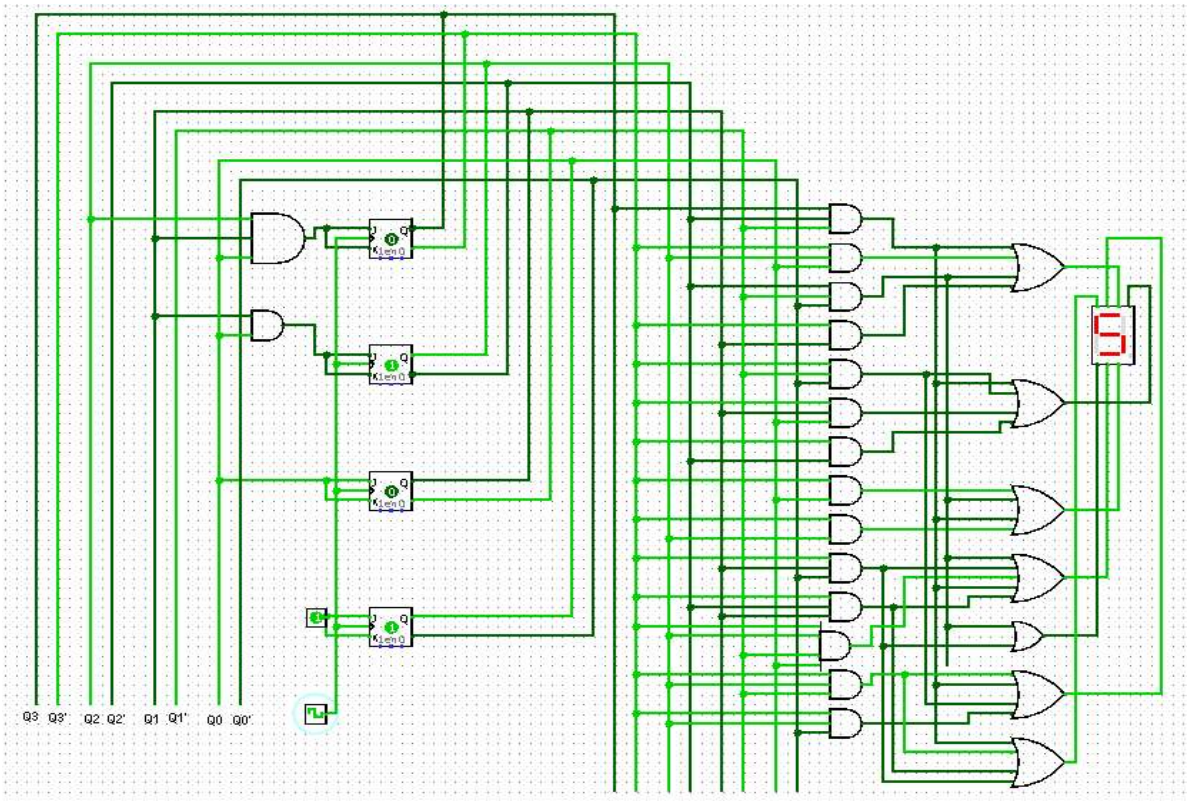

Q3 Q3' Q2 Q2' Q1 Q1' Q0 Q0'
4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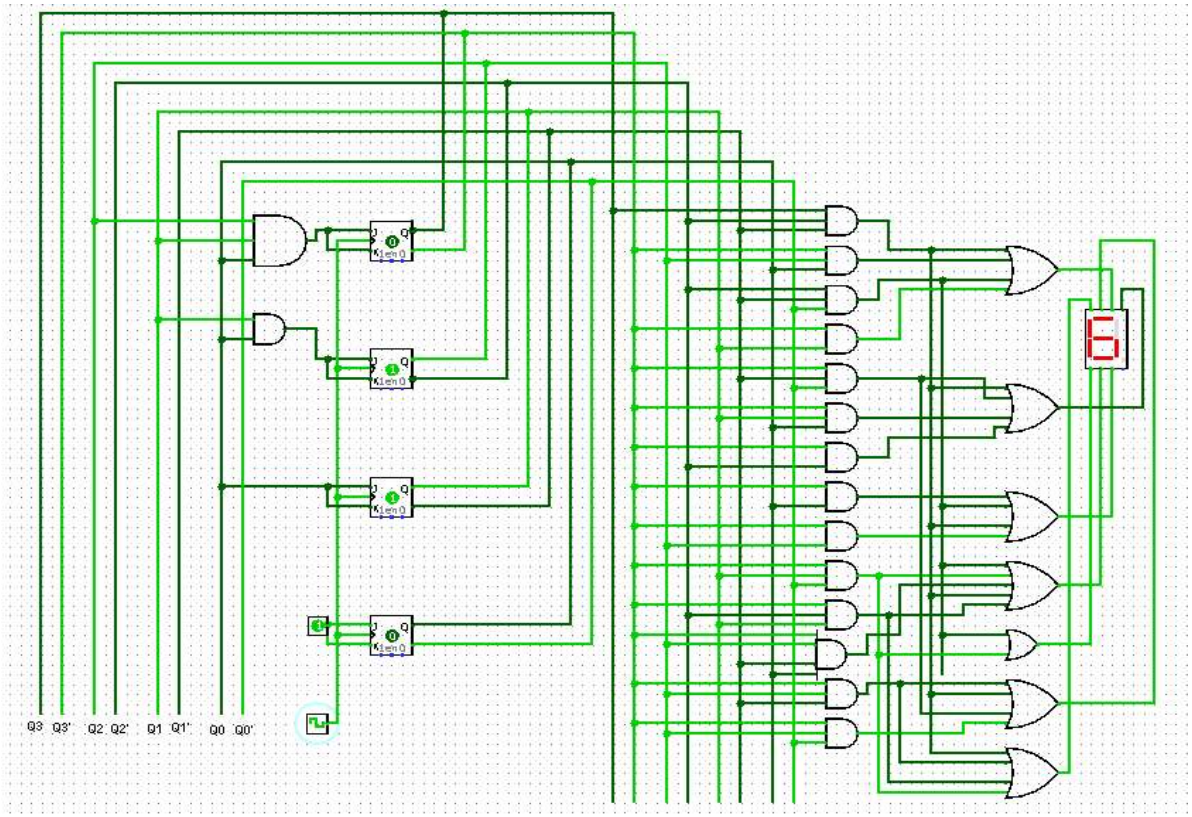
5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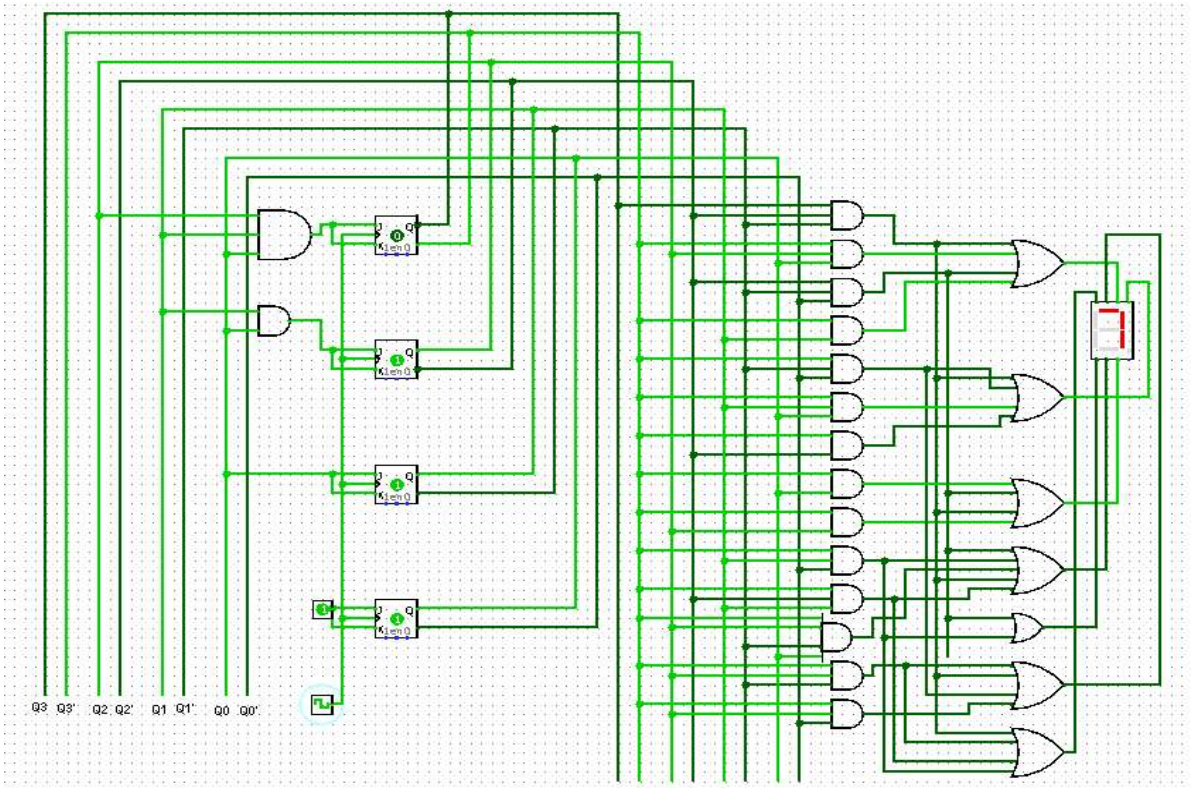
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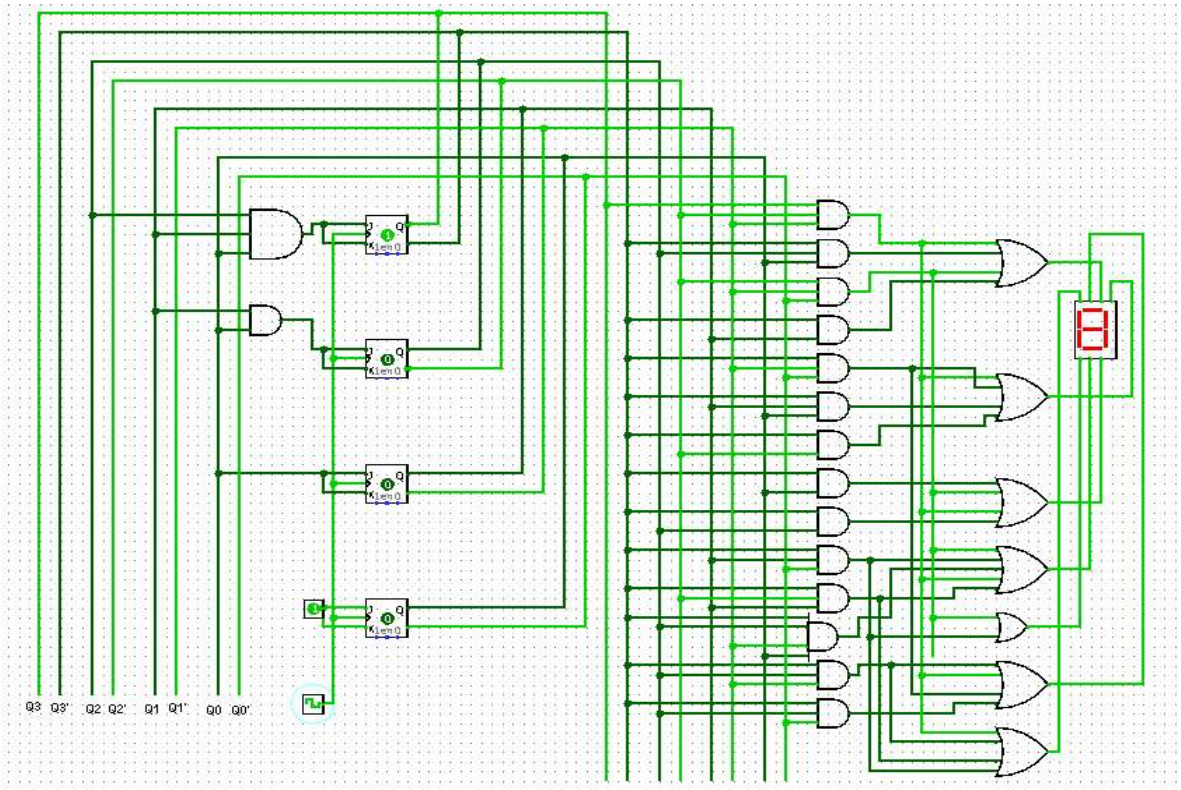
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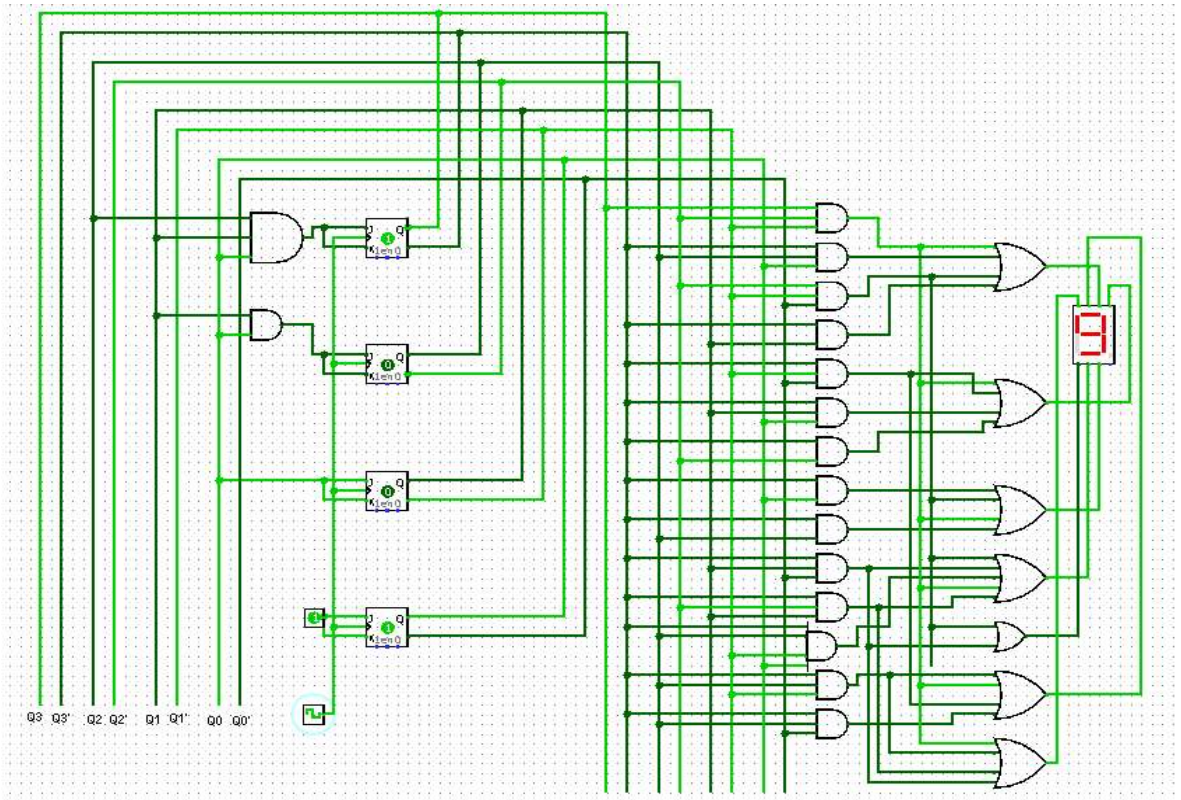
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