



United International University
QUEST FOR EXCELLENCE



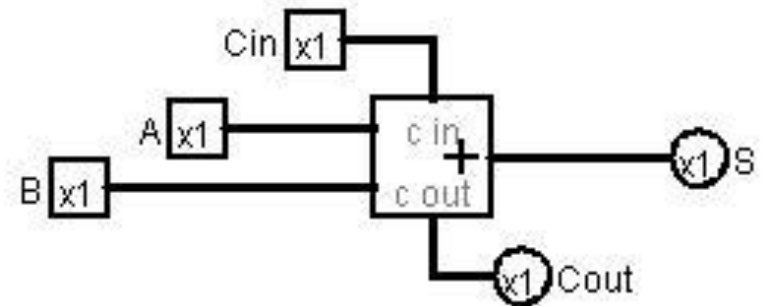
CSE 1326: Digital Logic Design Lab Implementing Full Adder

United International University

What to do

- (1) Implement a 1-bit full-adder using XOR gates.

Cin	A	B	Cout	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



- C_{in} is X
- A is Y
- B is Z

$$S = \overline{X}\overline{Y}Z + \overline{X}Y\overline{Z} + X\overline{Y}\overline{Z} + XYZ$$

$$C = XY + XZ + YZ$$

What to do (contd.)

- First, simulate a one-bit Full-Adder (FA) in logisim using “adder”. Get the truth table. Find expressions for S and Cout
- Previous equations can be transformed to the following forms:

$$S = (X \oplus Y) \oplus Z$$

$$C = XY + Z(X \oplus Y)$$

- Implement 1-bit FA using xor and verify it in both logisim and trainer-board

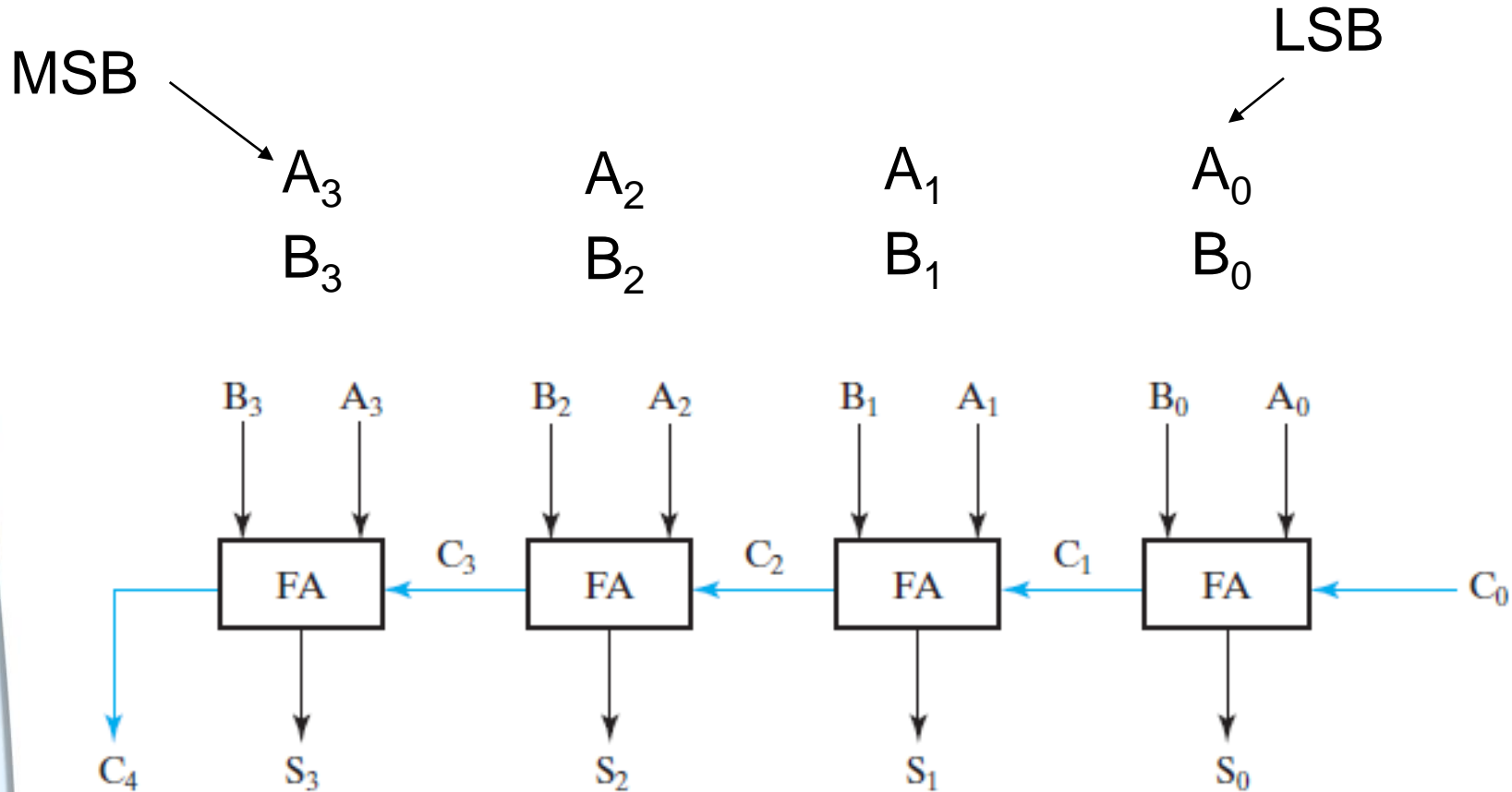
What to do (contd.)

- (2) In Logisim (only), add two digits (e.g., 8 and 9) using
 - a) Four 1-bit full adders
 - b) Two 2-bit full adders
 - c) One 4-bit full adder

Add Two Digits (Supplementary)

	MSB							LSB
		A_3	A_2	A_1	A_0			
		B_3	B_2	B_1	B_0			
Carry		?	?	1	?			
A ($A_3 A_2 A_1 A_0$) = 9		1	0	0	1			
B ($B_3 B_2 B_1 B_0$) = 7		0	1	1	1			
		?	?	?	?			0
	C_{out}	S_3	S_2	S_1	S_0			

Add Two Digits (Supplementary)



- C_{in} or C_0 is provided in LSB stage

Writing Report

- The report should contain
 - Truth table for 1-bit full adder
 - Circuit diagram of 1-bit full adder using XOR (S and Cout)
 - Logisim circuit designs for adding two digits that uses
 - 4 1-bit full adders
 - 2 2-bit full adders
 - 1 4-bit full adder