



### CSE 1326: Digital Logic Design Lab Basic Logic Gates and ICs

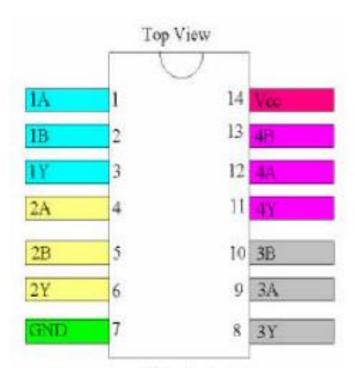
**United International University** 



- Objective & What to do
  - To know the basic gates below and related ICs
  - Verify those gates using logisim and trainer board.
  - 74LS00 Quad 2-Input NAND gate
  - 74LS02 Quad 2-Input NOR gate
  - 74LS04 Quad 2-Input NOT gate
  - 74LS08 Quad 2-Input AND gate
  - 74LS32 Quad 2-Input OR gate
  - 74LS86 Quad 2-Input XOR

### An IC





## OR, AND

OR	The output is active high if any one of the input is in active high state, Mathematically,  Q = A+B	<b>A</b> 0 0 1 1	<ul><li>B</li><li>0</li><li>1</li><li>0</li><li>1</li></ul>	Output Q  0  1  1	A OR	7432 1 VCC 14 2 VCC 14 13 3 12 4 11 5 0 9 7 GND 8
	The output is active high only if both the inputs are in active high state,	<b>A</b> 0	<b>B</b>	Output Q		7408 1 VCC 14 2 13
AND	Mathematically,  Q = A.B	0	1	0	AB AND AB	3 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
		1	0	0		7 GND 8

# NOT, NOR

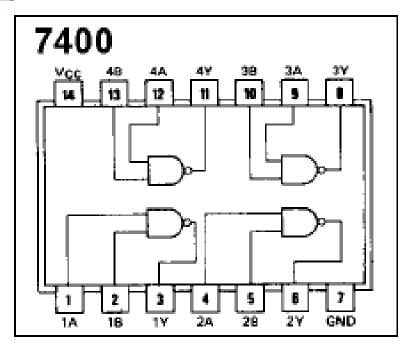
NOT	In this gate the output is opposite to the input state, Mathematically, $Q = \overline{A}$	<b>A</b> 0 1		Output Q  1 0	A \(\overline{\text{NOT}}\)	7404 1 VCC 14 2 13 3 12 4 11 5 10 6 9 7 GND 8
	The output is active high only if both the inputs are in active low state, Mathematically,	<b>A</b> 0	<b>B</b> 0	Output Q		7402 1 VCC 14 2 VCC 14
NOR	$\mathbf{Q} = \overline{\mathbf{A} + \mathbf{B}}$	0	1	0	A NOR	
		1	0	0		6 9 7 GND 8

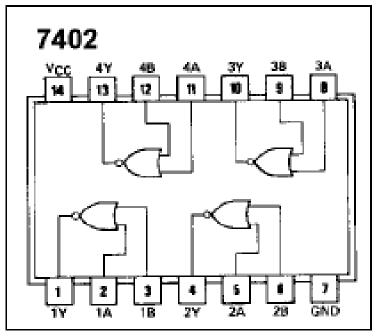
### NAND, EXOR

		The output is active high	A	В	Output Q		7400
		only if any one of the					1 VCC 14
		input is in active low state, Mathematically,	0	0	1		
	NAND	, sauce, 1/14/11/11/11/11/11/11/11/11/11/11/11/11	0	1	1	A 35	
	MAND	$Q = \overline{A.B}$				NAMO	
			1	0	1		
							7 GND Y
			1	1	0		
			1				
1		The output is active high	A	В	Output Q		7486
/		The output is active high only if any one of the		В	Output Q		7486
		only if any one of the input is in active high		<b>B</b>	Output Q		7486
		only if any one of the	A				
7		only if any one of the input is in active high state, Mathematically,	A				
	EXOR	only if any one of the input is in active high	<b>A</b> 0	0	0	A ASB	
	EXOR	only if any one of the input is in active high state, Mathematically,	<b>A</b> 0	0	0	A ASE	
	EXOR	only if any one of the input is in active high state, Mathematically,	<b>A</b> 0 0	0	0	A ASB	

### NAND, NOR



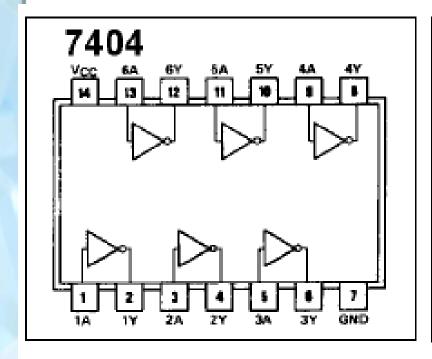


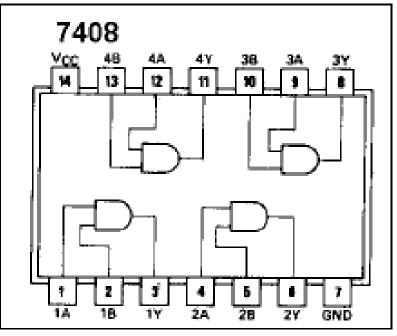


2 INPUT NAND GATE

2 INPUT NOR GATE

### NOT, AND

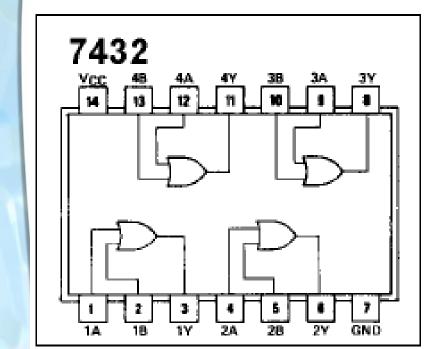


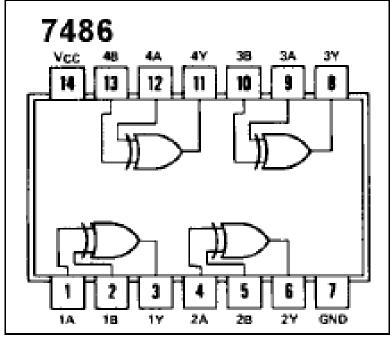


NOT GATE

2 INPUT AND GATE

### OR, XOR





2 INPUT OR GATE

2 INPUT XOR GATE



No Report for Lab One!!!