United International University

Computer Science and Engineering

Group No: 6

Course No: CSE1326

Course Title: Digital Logic Design Laboratory

Exp. No: 6

Name of the Exp. "Ripple counter"

Students No: 011213193

Date of Performance: 07/09/2022

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Objectives:

Implementing Ripple counters: 4-bit downward counter using

1. +ve edge D flip-flop

2. -ve edge J-K flip-flop

Components used:

1. D Flip-flop IC - 7474

2. JK Flip-flop IC - 7476

3. Clock

4. Logisim Software

5. Trainer Board

Theory:

A ripple counter is an asynchronous counter where only the first flip-flop is clocked by an external clock. All subsequent flip-flops are clocked by the output of the preceding flip-flop. Asynchronous counters are also called ripple-counters because of the way the clock pulse ripples it way through the flip-flops.

The MOD of the ripple counter or asynchronous counter is 2^n if n flip-flops are used. For a 4-bit counter, the range of the count is 0000 to 1111 (2^4-1). A counter may count up or count down or count up and down depending on the input control. The count sequence usually repeats itself. When counting up, the count sequence goes from 0000, 0001, 0010, ... 1110 , 1111 , 0000, 0001, ... etc. When counting down the count sequence goes in the opposite manner: 1111, 1110, ... 0010, 0001, 0000, 1111, 1110, ... etc.

The complement of the count sequence counts in reverse direction. If the uncomplemented output counts up, the complemented output counts down. If the uncomplemented output counts down, the complemented output counts up.

There are many ways to implement the ripple counter depending on the characteristics of the flip flops used and the requirements of the count sequence.

Clock Trigger: Positive edged or Negative edged

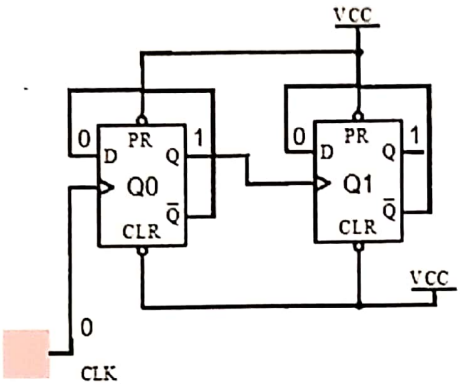
JK or D flip-flops

Count Direction: Up, Down, or Up/Down

Asynchronous counters are slower than synchronous counters because of the delay in the transmission of the pulses from flip-flop to flip-flop. With a synchronous circuit, all the bits in

the count change synchronously with the assertion of the clock. It can be implemented using D-type flip-flops or JK-type flip-flops.

The circuit below uses 2 D flip-flops to implement a divide-by-4 ripple counter ($2^n = 2^2 = 4$). It counts down.



STATE TABLE

COUNT	Q1	Q0
3	1	1
2	1	0
1	0	1
0	0	0

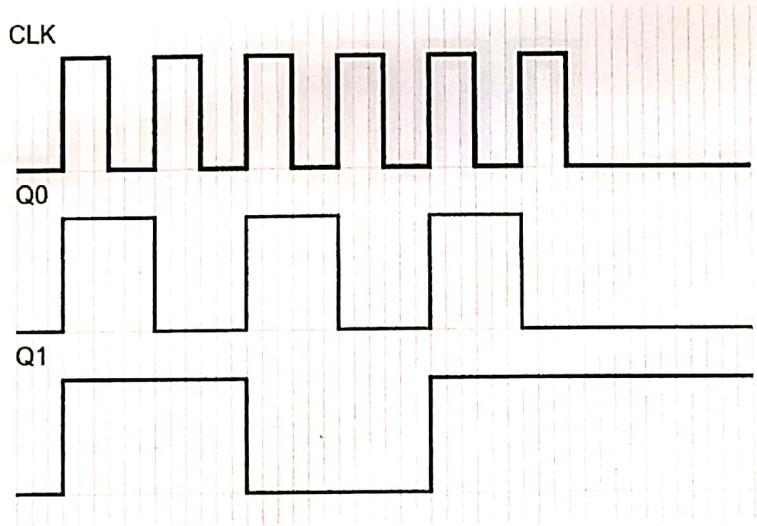


Fig-1: Block diagram of a ripple counter

Problem/Design Solve Procedure:

Logisim software is used to solve different types of counters using D flip-flop and JK flip-flop.

(1)

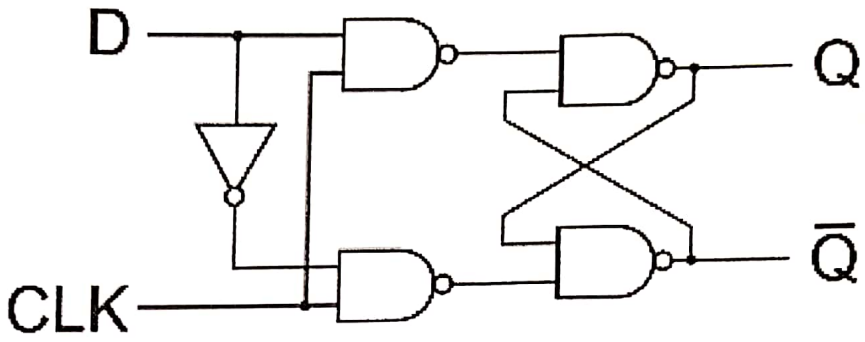


Fig-2: Gate diagram of D Flip-flop IC

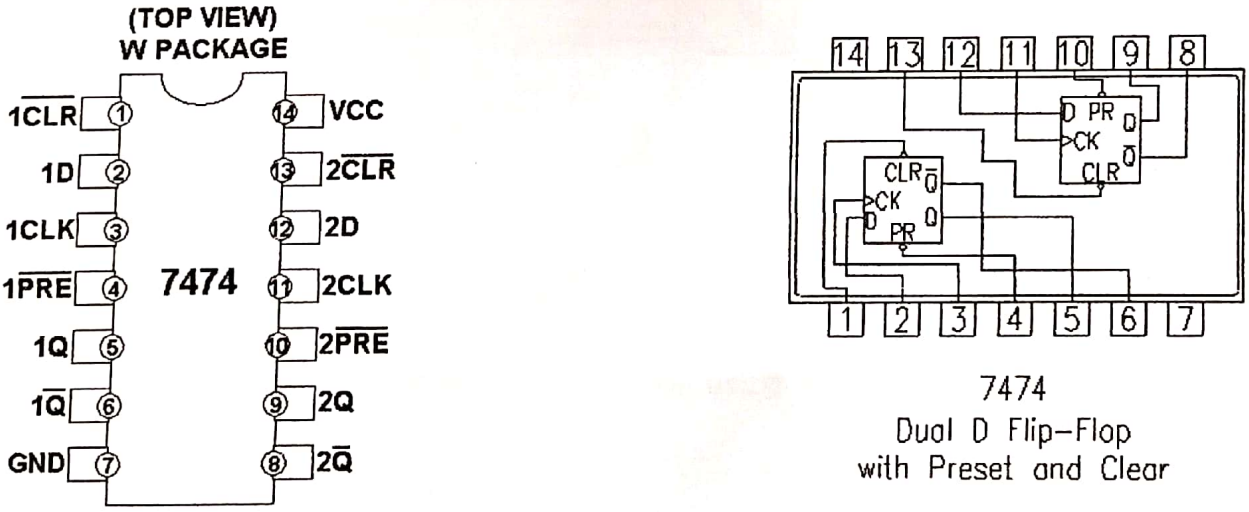


Fig-3: Pin Diagram of D Flip-flop

(2)

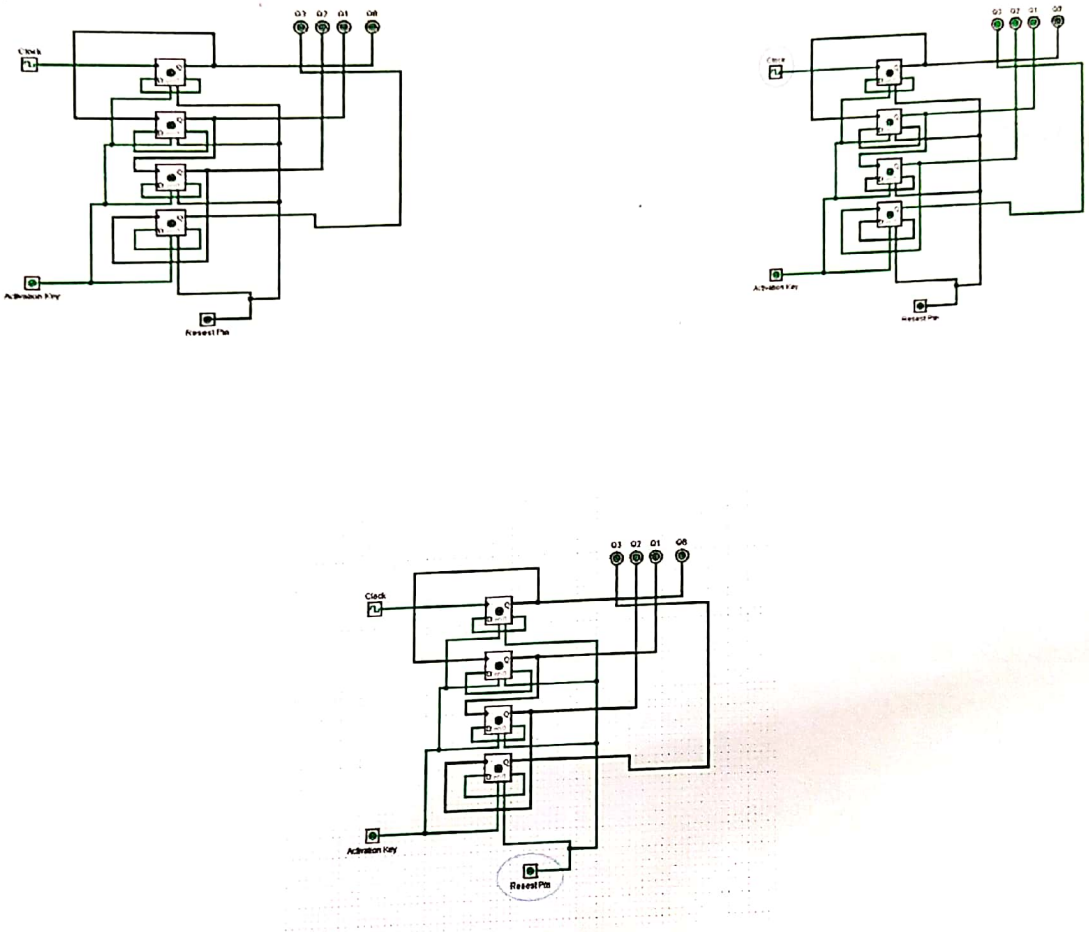


Fig-4: 4-Bit downward counter using +ve DFF

Fig-4 is representing a 4-Bit downward ripple counter using +ve D flip-flop. It can count 0 to 15 in reverse order. Here is a clock that is handling the entire thing and also a reset pin to reset the circuit from any number. +ve means when clock is 1 it will be performing. Here is using 4 D flip-flop for 4-Bit counter. Every FF's output is performing as next DFF's clock input till the last. Here is an activation key to active the circuit. If the activation key is off the circuit will

not work even though we triggered the clock. Every DFF's Q' is represented DFF's input. It will active when Q is off. Q is also used for showing the output.

(3)

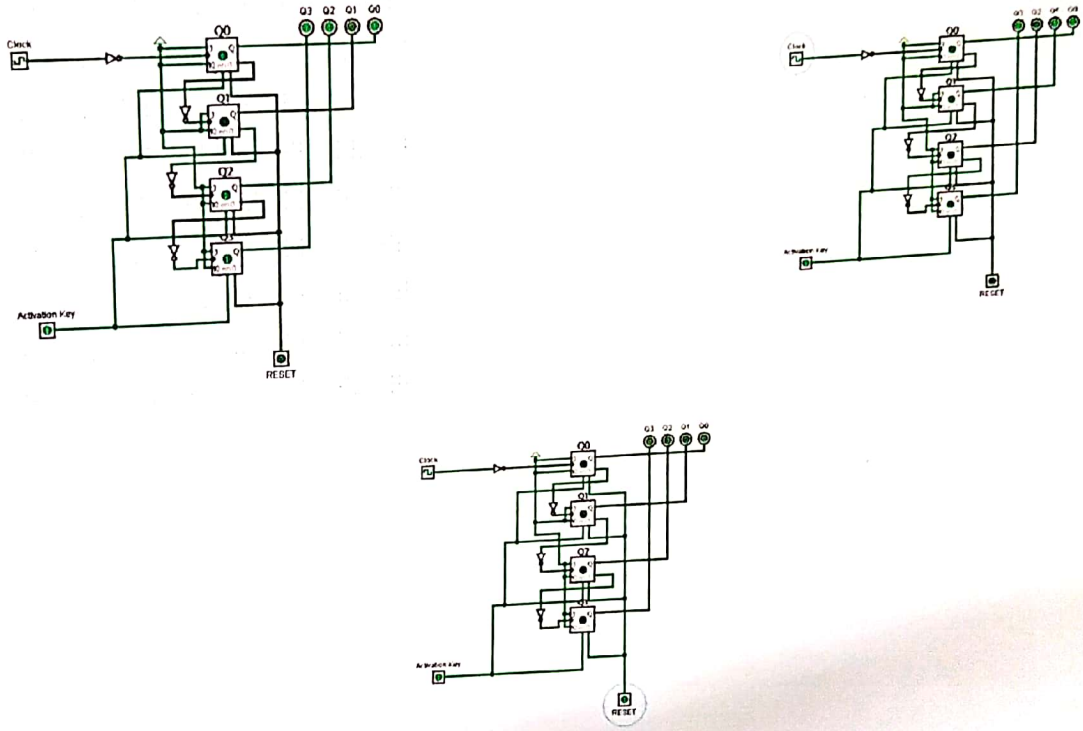


Fig-5: 4-Bit downward counter using -ve J-K FF

Fig-5 is representing a 4-Bit downward ripple counter using -ve J-K flip-flop. -ve means when clock is triggered in negative the outputs will be toggled. Here is an activation key to active the circuit and a reset key to reset the circuit. If we triggered the reset button the circuit will be changed and value transformed into 0000. The clock is attached with NOT game so it is representing -ve edge that I said before. The logic of J-K input is always 1. The wire is connected with "power" which is an amazing feature of Logisim. The "power" wire's value is always 1. Every FF's Q' is connected with next FF's clock with a NOT gate and Q3 Q2 Q1 Q0 is representing the outputs.

Discussion:

I have learnt how to perform ripple counters throughout this experiment. Such as how to use Logisim software, how to implements different bits of counters using different types of flip-flops, how to implement a circuit diagram of 3-bit upward ripple counter using DFF, 4-bit downward ripple counter using J-K FF etc. During the implementation the Flip-flop was taken from memory and wires were attached very carefully. I have faced some problems in when I draw 4-bit downward ripple counter using J-K flip-flop , it was so confusing to placement the outputs. It wastes so many times, had to make me overthink and circuits were not working in proper way etc. But later it has been solved.