



United International University
QUEST FOR EXCELLENCE



CSE 1326: Digital Logic Design Lab

Basic Logic Gates and ICs

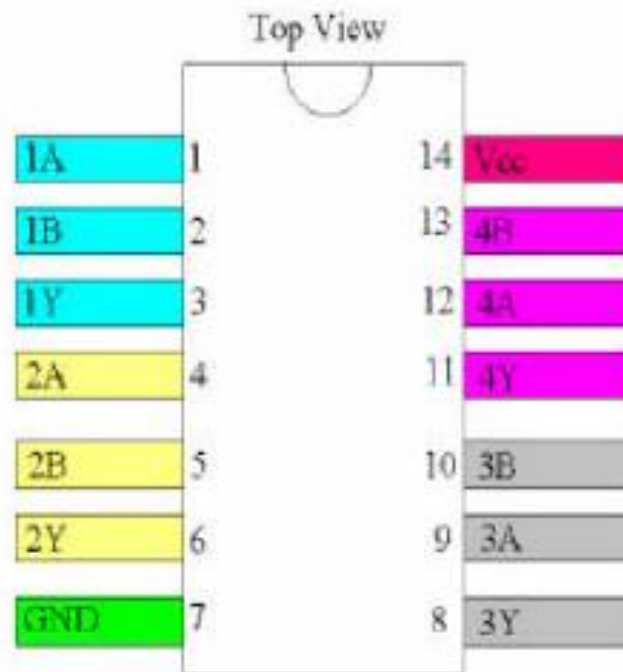
United International University

Basic Gates and ICs

- Objective & What to do
 - To know the basic gates below and related ICs
 - Verify those gates using logisim and trainer board.
- 74LS00 Quad 2-Input NAND gate
- 74LS02 Quad 2-Input NOR gate
- 74LS04 Quad 2-Input NOT gate
- 74LS08 Quad 2-Input AND gate
- 74LS32 Quad 2-Input OR gate
- 74LS86 Quad 2-Input XOR

An IC

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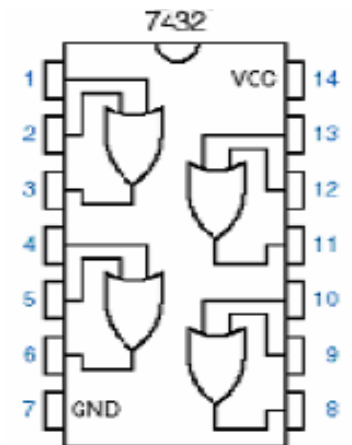
OR, AND

OR

The output is active high if any one of the input is in active high state, Mathematically,

$$Q = A + B$$

A	B	Output Q
0	0	0
0	1	1
1	0	1
1	1	1

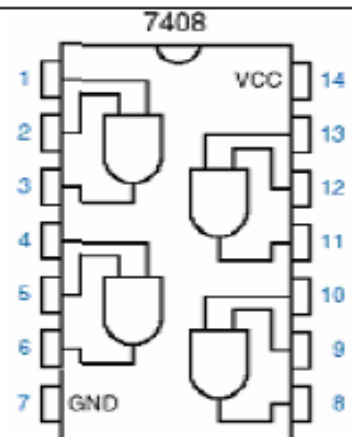


AND


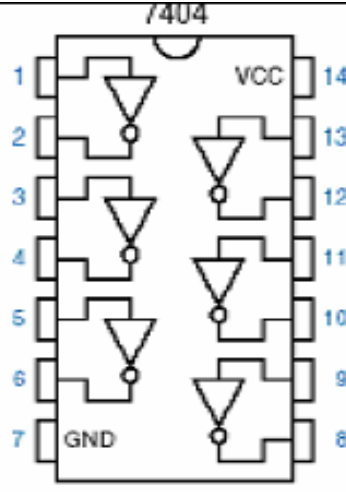

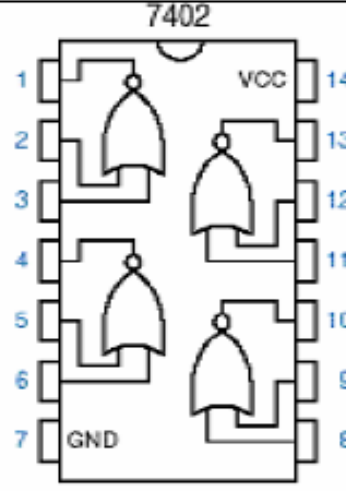
The output is active high only if both the inputs are in active high state, Mathematically,

$$Q = A \cdot B$$


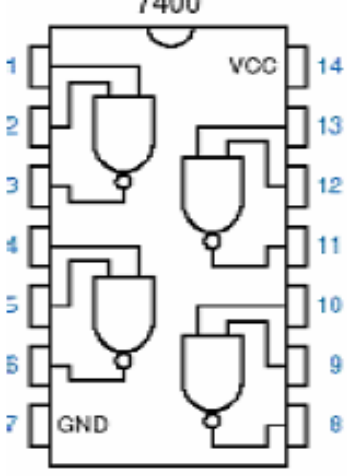

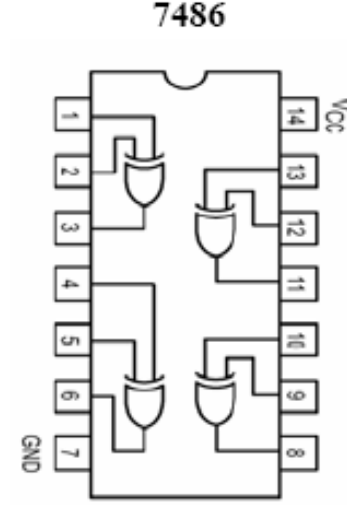
A	B	Output Q
0	0	0
0	1	0
1	0	0
1	1	1



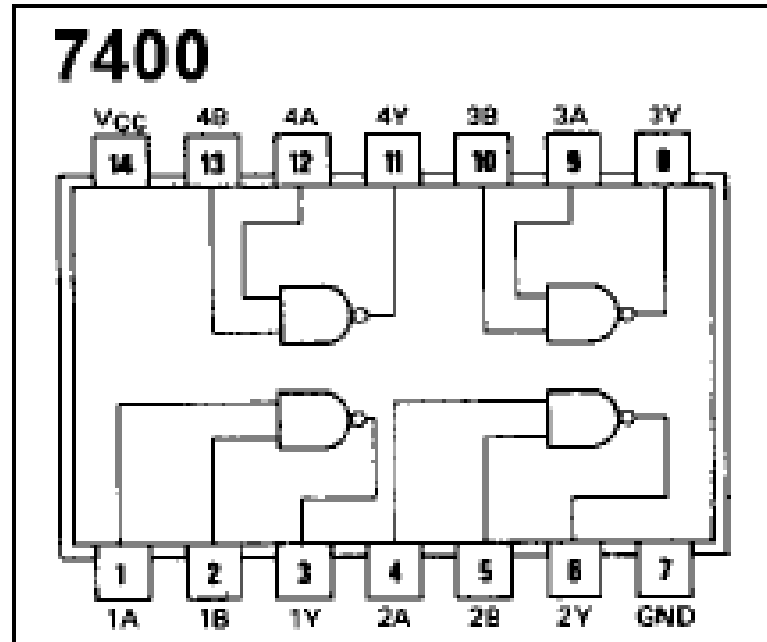
NOT, NOR

NOT	<p>In this gate the output is opposite to the input state, Mathematically,</p> $Q = \overline{A}$	<table><tr><th>A</th><th>Output Q</th></tr><tr><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td></tr></table>	A	Output Q	0	1	1	0											
A	Output Q																		
0	1																		
1	0																		
NOR	<p>The output is active high only if both the inputs are in active low state, Mathematically,</p> $Q = \overline{A+B}$	<table><tr><th>A</th><th>B</th><th>Output Q</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>	A	B	Output Q	0	0	1	0	1	0	1	0	0	1	1	0		
A	B	Output Q																	
0	0	1																	
0	1	0																	
1	0	0																	
1	1	0																	

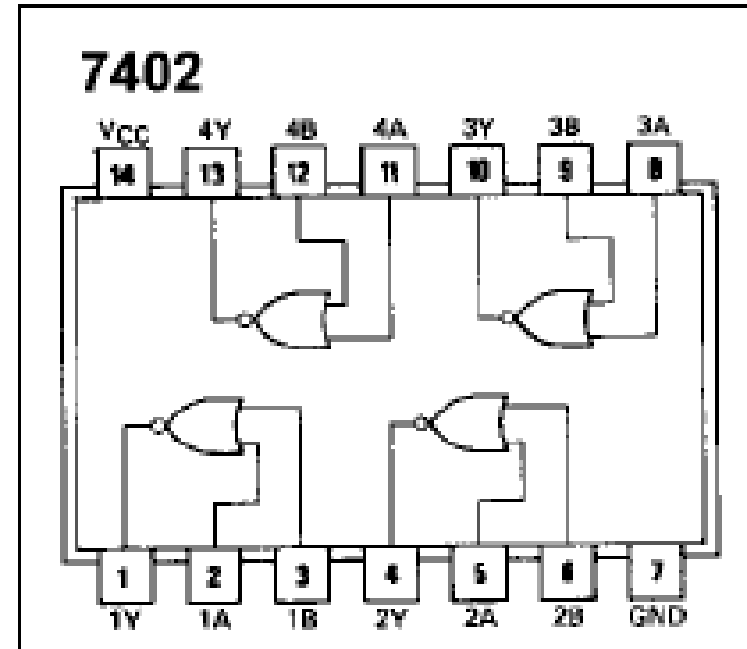
NAND, EXOR

<p>NAND</p>	<p>The output is active high only if any one of the input is in active low state, Mathematically,</p> $Q = \overline{A \cdot B}$	<p>A</p> <p>0</p> <p>0</p> <p>1</p> <p>1</p>	<p>B</p> <p>0</p> <p>1</p> <p>0</p> <p>1</p>	<p>Output Q</p> <p>1</p> <p>1</p> <p>1</p> <p>0</p>		
<p>EXOR</p>	<p>The output is active high only if any one of the input is in active high state, Mathematically,</p> $Q = A \oplus B$	<p>A</p> <p>0</p> <p>0</p> <p>1</p> <p>1</p>	<p>B</p> <p>0</p> <p>1</p> <p>0</p> <p>1</p>	<p>Output Q</p> <p>0</p> <p>1</p> <p>1</p> <p>0</p>		

NAND, NOR

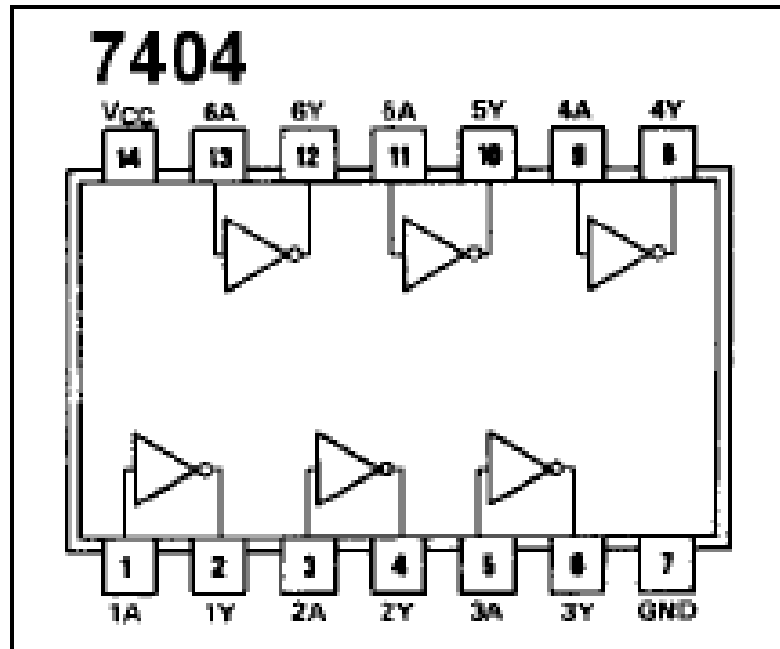


2 INPUT NAND GATE

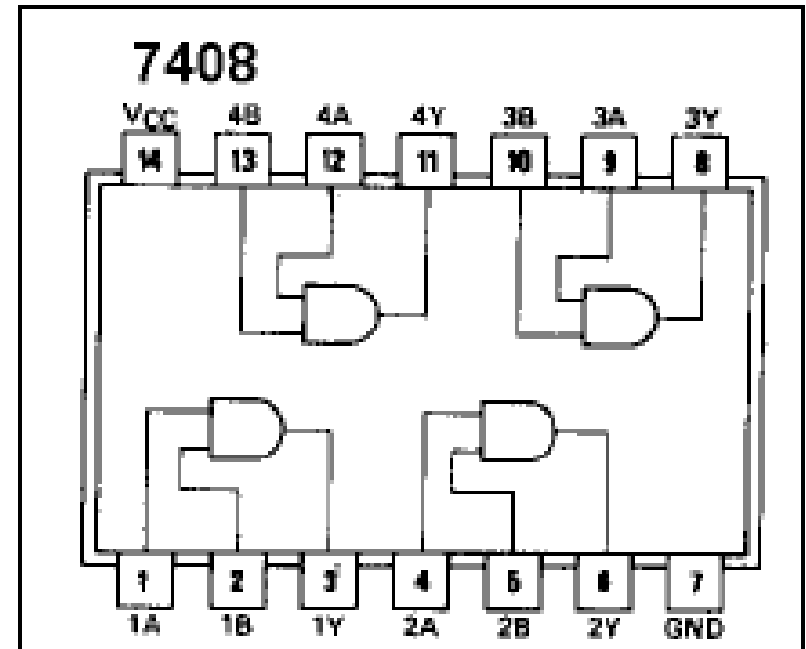


2 INPUT NOR GATE

NOT, AND

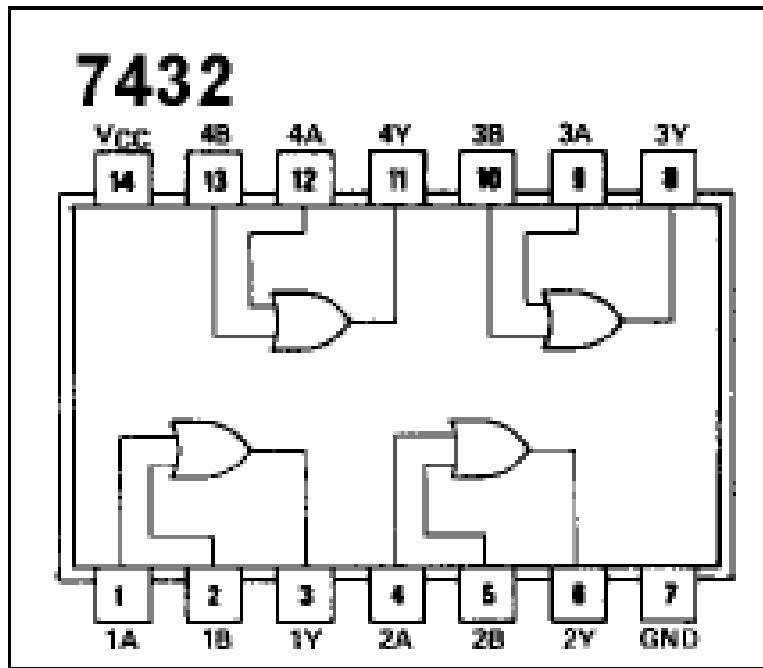


NOT GATE

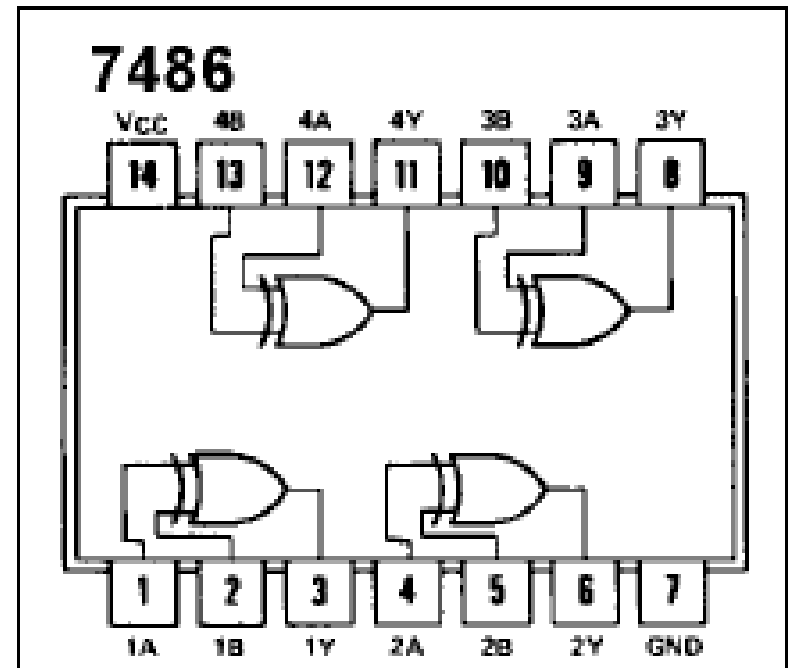


2 INPUT AND GATE

OR, XOR



2 INPUT OR GATE



2 INPUT XOR GATE

- No Report for Lab One!!!