DTB Command Line Commands

DTB Connection

scan	list USB IDs of connected DTBs
open [*usbid*]	Open DTB access
close	Close DTB access
flush	Flush communication buffer
init	Set DTB to default state
exit	Exit comand interpreter
welcome	test connection (LED blinking)
setled *led*	Set LED status

led	LED4	LED3	LED2	LED1

info	Show detailed version info
version, ver	Show software version
rpcinfo	Show RPC version and commands
rpclink	Check if DTB commands available and link
help	Shows a short command list

Delay

cdelay *n*	Wait for *n* clock cycles
udelay *us*	Wait for *us* microseconds
mdelay *ms*	Wait for *ms* milliseconds

ROC/Module Signal

clkmode *mode*	Set CLK signal mode
ctrmode *mode*	Set CTR signal mode
sdamode *mode*	Set SDA signal mode
tinmode *mode*	Set TIN signal mode

mode
0 = normal mode
1 = constant low
2 = constant high
3 = pseudo random pattern (not yet implemented)

clk *delay* [*duty*]	Set CLK signal delay
ctr *delay* [*duty*]	Set CTR signal delay
sda *delay* [*duty*]	Set SDA signal delay
tin *delay* [*duty*]	Set TIN signal delay

delay Delay in 1/20 clock cycles (1.25 ns @ 40 MHz)

duty Adjust falling edge position in 1/20 clock cycles (optional parameter, default 0)

clklvl amplitude	Set CLK signal amplitude
ctrlvl amplitude	Set CTR signal amplitude
sdalvl amplitude	Set SDA signal amplitude
tinlvl amplitude	Set TIN signal amplitude

amplitude Signal amplitude: 0...15

Pattern Generator PG

pgset *step pattern delay* Add entry in PG memory

step PG memory address (0...255)

pattern

sync	rest	resr	cal	trg	tok

delay Delay to next pattern in clock cycles (0 = stop) to 255

pgsingle	Start single sequence
pgloop *period*	Start loop with period *period* in clock cycles
pgtrig	Enable start with external triggers
pgstop	Stop PG (after pgloop or pgtrig)

Example:
Set up tpical readout sequence

pgset 0 b101000	10	Pulse SYNC and RESR and wait for 10 clock cycles
pgset 1 b000100	120	Pulse CAL and wait for 120 clock cycles
pgset 2 b000010	16	Pulse TRG and for 16 clock cycles
pgset 3 b000001	0	Pulse TOK and finish sequence
pgloop 1000		Run in loop with 1000 clock cycles period
pgstop		Stop PG

ROC Power, ROC control

pon	Switch on VD and VA and all ROC signals
poff	Switch off VD and VA and all ROC signals
vd *mv*	Set VD to *mv* millivolts
va *mv*	Set VA to *mv* millivolts
id *ma*	Set VD current limits to *ma* milliamps
ia *ma*	Set VA current limit to *ma* milliamps
getvd	Show VD voltage
getva	Show VA voltage
getid	Show VD current
getia	Show VA current
reson	Activate ROC reset line
resoff	Desactivate ROC reset line
hvon	Apply bias viltage to sensor
hvoff	Remove bias voltage from sensor
rocaddr *addr*	Set hard-wired ROC address to *addr*

ROC Programming

select *addr*	Select ROC address range for commands
dac *dacnr value*	Program DAC
vana *value*	Set vana DAC
vtrim *value*	Set vtrim DAC
vthr *value*	Set vthr DAC
vcal *value*	Set vcal DAC
wbc *value*	Set WBC
ctl *value*	Set control register
cole *range*	Enable columns
cold *range*	Disable columns
pixe *x y trim*	Enable pixel field and set trimming value to *trim*
pixd *x y*	Disable pixel field
cal *x y*	Set calibrate pulses to pixel field
cald	Disable all calibrate pulses
mask	Mask all double columns and pixels

Digital Signal Probe

d1 *source*	Assign signal source to D1 output
d2 *source*	Assign signal source to D2 output

source		
	0 = GND	10 = CTR
	1 = CLK	11 = TIN
	2 = SDA	12 = TOUT
	3 = send	13 = clk_present
	4 = pg_tok	14 = clk_good
	5 = pg_trg	15 = adc_send
	6 = pg_cal	16 = CRC
	7 = pg_res	
	8 = pg_rest	
	9 = pg_sync	

Analog Signal Probe

a1 *source*	Assign signal source to A1 output
a2 *source*	Assign signal source to A2 output

source		
	0 = TIN	4 = CLK
	1 = SDATA1	5 = SDA
	2 = SDATA2	6 = TOUT
	3 = CTR	7 = GND

Data Aquisition DAQ

dopen *size*	Open DAQ and assign memory *size* = size of buffer (# samples)
dclose	Close DAQ and free buffer
dstart	Enable data flow
dstop	Disable data flow
dsize	Show DAQ buffer fill state
dread	Read DAQ buffer and interpret as digital data
dreada	Read DAQ buffer and interpret as analog data
adcena	Enable ADC channel for DAQ
adcdis	Disable ADC channel for DAQ
deser *mode*	Configure DESER160 for DAQ

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