AN1326
APPLICATION NOTE

L6565 QUASI-RESONANT CONTROLLER

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A variable frequency version of flyback converter, commonly known as Quasi-resonant (QR) ZVS flyback, is largely used in certain applications, such as SMPS for TV, though it is well suited for other applications too.

This peculiar topology features several merits. Besides the others, which will be highlighted in the text, one of them is to be a simple derivative of the standard square-wave flyback, well known to every SMPS designer.

After deriving the equations governing QR ZVS flyback topology and dealing with the related issues, ST's L6565, a PWM controller specifically designed to fit this particular topology, will be presented and its internal functions discussed in details.

Some clues on the design based on this device will be provided and, finally, a design example will be given that will show how easy and cost-effective such L6565-based systems are.

INTRODUCTION

Over the past two decades plenty of resonant and quasi-resonant converters have been developed and proposed as an answer to the difficulties raised by square-wave converters, especially those related to their parasitic elements. The basic idea is to put these parasitics in use.

The core of both classes of converters is a tank circuit. Unlike resonant converters, where it takes part actively in the power conversion process, quasi-resonant converters use the tank circuit only to create either a zero-voltage or a zero-current condition for the power switch, to turn on or turn off respectively.

The existing types of quasi-resonant converters can be then classified as either Zero-Voltage Switching turn-on (ZVS) or Zero-Current Switching turn-off (ZCS) converters.

In ZVS converters the power switch is dynamically connected in parallel to the tank circuit. The superposition of the resonant voltage across the tank circuit (and the switch, while it is in off state) on the DC input voltage generates the zero-voltage condition for the switch to turn on. Conversely, in ZCS converters the power switch is connected in series to the tank circuit. The superposition of the resonant current flowing through the tank circuit (and the switch, while it is in on state) on the normal current flow generates the zero-current condition for the switch to turn off.

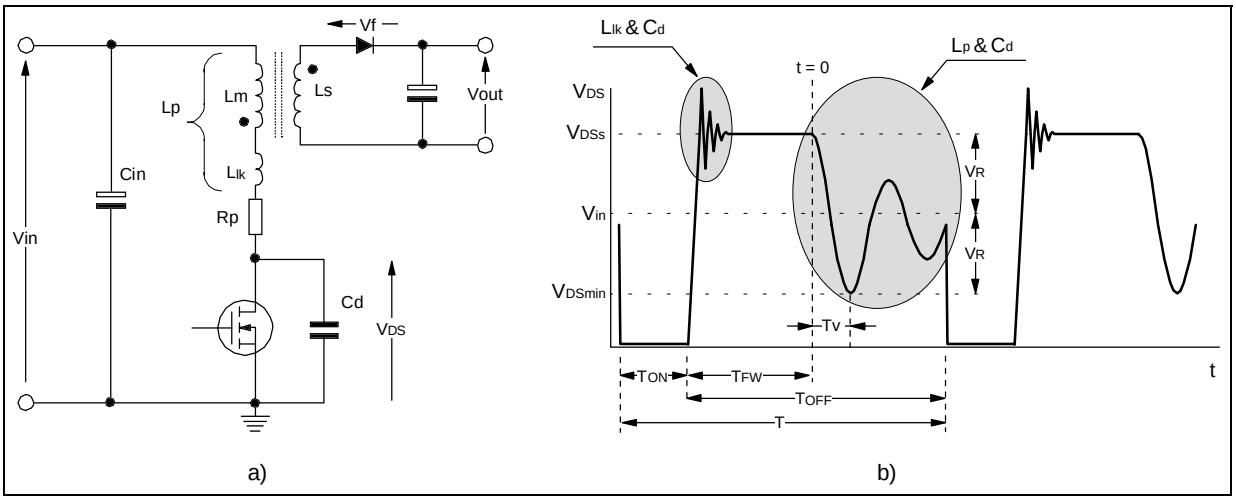
An interesting property of quasi-resonant converters is that they will be turned back into a normal square-wave converter if the tank circuit is removed. Vice versa, a quasi-resonant converter can be obtained starting from a normal square-wave topology.

QR ZVS FLYBACK TOPOLOGY

In principle there are many ways to make a quasi-resonant (QR) ZVS flyback converter, but most of them are not suitable for offline applications because of the too high voltages involved. With the above-mentioned property in mind, it is possible to derive a QR version starting from a standard square-wave flyback power stage and pointing out its major parasitic elements, as illustrated in figure 1.

L_{lk} is the leakage inductance, which represents the magnetic flux generated by the primary winding and not coupled to the secondary. It stores energy that will not be delivered to the secondary and that needs to be transferred or dissipated elsewhere. Besides, it prevents a portion of the energy stored in the mutual inductance L_m (which is perfectly coupled to the secondary) from being transferred to the secondary and delays the energy transfer process. The energy stored in L_{lk} is the cause of the large overvoltage spike on the MOSFET's drain at turn-off.

Figure 1. Flyback power stage with major parasitics (a) and V_{DS} waveform with fixed frequency, DCM (b).



C_d is the total capacitance of the drain node. It is the sum of the MOSFET's C_{oss}, transformer intrawinding capacitance, stray capacitance due to the layout of the circuit (e.g. a heatsink) as well as other contributions reflected from the secondary side, such as an R-C damper on the rectifier diode.

Actually, C_{oss} is modulated by the drain voltage but the variation becomes significant at very low V_{DS} values and the impact is however limited. Therefore, it is possible to assume for C_{oss} the value specified usually at V_{DS} = 25V by manufacturers.

C_d is discharged inside the MOSFET as it is turned on, thus causing a current spike. This spike not only gives origin to additional losses in the MOSFET but may also cause noise problems, especially in case of current mode control and under light load conditions.

R_p is the resistance of the primary side mesh, mostly located in the primary winding. It is important to notice that the resistance of the primary winding has to account not only for the ohmic resistance of the wire but also for the high frequency effects in copper (skin and proximity), the magnetic material losses (hysteresis and eddy currents) and radiation.

At least a couple of tank circuits can be then identified in the schematic, whose effect is conspicuous on the drain voltage waveform in Discontinuous Conduction Mode (DCM) operation (see figure 1b).

The first one shows up after the overvoltage spike at MOSFET turn-off and is due to the resonance of L_{lk}, just demagnetized, with C_d. The drain voltage falls in under dumped fashion from the peak to the settling value:

$$V_{DSs} = V_{in} + V_R = V_{in} + n \cdot (V_{out} + V_f) \qquad (1)$$

where V_{in} is the DC input voltage, V_R the so-called reflected voltage, n the primary-to-secondary turn ratio, V_{out} the regulated output voltage of the converter and V_f the forward drop across the secondary rectifier.

The second tank circuit, made up of L_p and C_d, resonates as the secondary winding has run dry of energy, thus the secondary rectifier no longer conducts, and both windings are open. In principle, it is an RLC circuit and the drain voltage follows the natural evolution of such circuit starting from the condition of C_d charged at V_{DSs} @ t = 0 (see waveform in figure 1b). R_p is normally by far less than the critical damping impedance of the tank circuit, thus the equation describing the under-damped evolution of the drain voltage is:

$$V_{DS}(t) \approx V_{in} + V_R \cdot e^{-\alpha \cdot t} \cdot \cos(2 \cdot \pi \cdot f_r \cdot t)$$

where:

$$\alpha = \frac{R_p}{2 \cdot L_p}, \qquad (2)$$

$$f_r = \frac{1}{2 \cdot \pi \cdot \sqrt{L_p \cdot C_d}} \qquad (3)$$

are the decay factor and the resonance frequency, respectively.

The first valley of the resonance occurs at t = T_v, where T_v can be derived from:

$$\cos(2 \cdot \pi \cdot f_r \cdot T_v) = -1 \Rightarrow T_v = \frac{1}{2 \cdot f_r} = \pi \cdot \sqrt{L_p \cdot C_d}\,; \qquad (4)$$

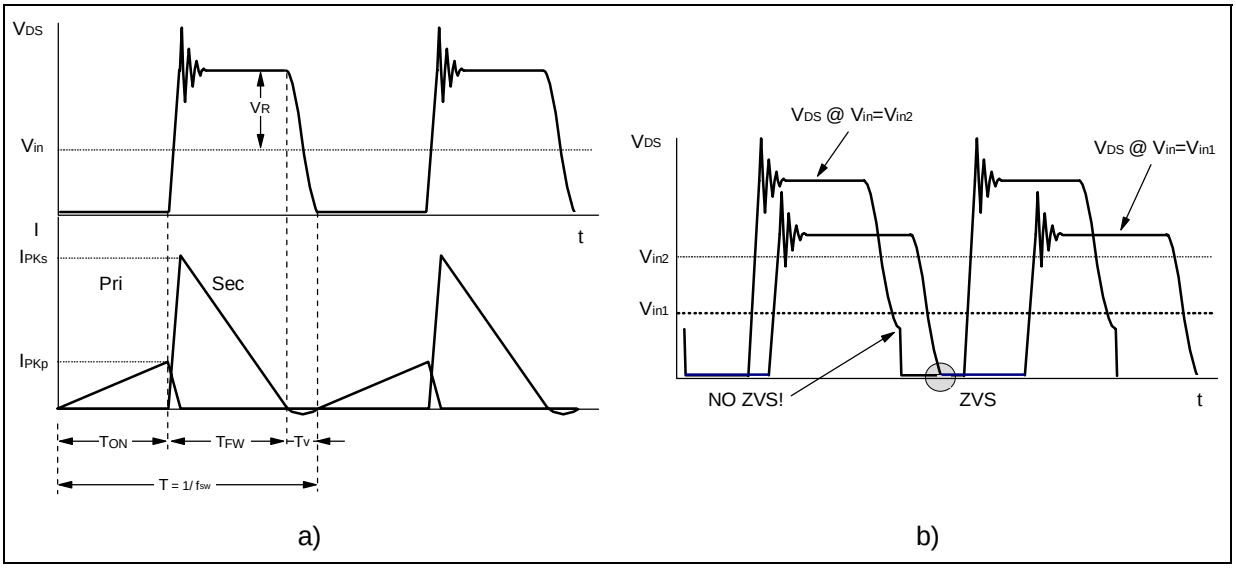
At that point, the drain voltage experiences an absolute minimum, given by $V_{DSmin} \approx V_{in} - V_R$ with good approximation ($e^{-\alpha \cdot Tv} \approx 1$). Therefore, a zero-voltage condition can be generated provided that:

Very Important in Determining the Turns Ration and Maximum Duty Cycle

$$V_{DSmin} \leq 0 \Rightarrow V_R \geq V_{in} \qquad (5)$$

and, if the system is controlled so that the MOSFET is switched on as the drain voltage reaches either zero or the minimum of the first valley, a QR ZVS converter will be obtained. The resulting waveforms are shown in figure 2.

Figure 2. (a) Typical QR waveforms; (b) How V_{in} affects ZVS conditions.



It is worthwhile noticing that the operation of the tank circuit depends only on circuit parameters and not on the operating conditions of the converter. The input voltage just impacts on the zero-voltage condition, as stated by eqn. 5 and shown in figure 2b.

The key point to generate such kind of functionality is to synchronize MOSFET's turn-on to the transformer demagnetization after an appropriate delay (T_v), which can be done just by detecting the negative-going portion of $V_{DS}(t)$. Therefore, in principle, any PWM controller with synchronization capability can be used to control this kind of converter. The L6565, in particular, is provided with a dedicated pin (ZCD) that allows doing the job with a very simple interface, just one resistor.

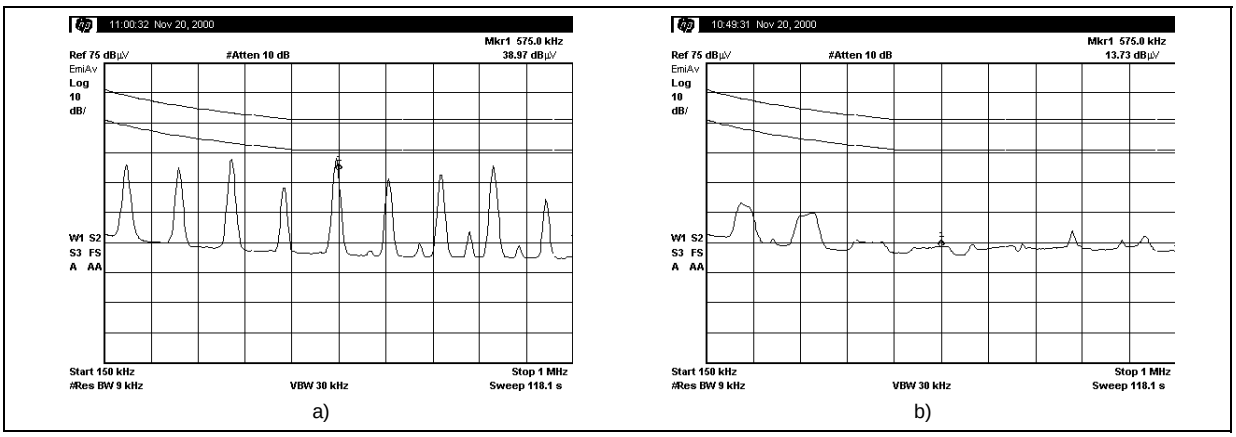
Variable frequency operation - as a result of input voltage and/or output current changes - is inherent in such functionality. The system works close to the boundary between DCM and CCM (Continuous Conduction Mode) operation of the transformer. This is what is otherwise called TM (Transition Mode) operation. The shorter T_v is, compared with the ON and OFF times of the MOSFET, the closer to TM the operation will be. Hence this QR ZVS flyback converter can be identified with the TM flyback converter mentioned in [1], as well as with the well-known self-oscillating flyback or Ringing Choke Converter (RCC).

As opposed to fixed-frequency standard flyback converter, this approach to quasi-resonance has several advantages.

The main benefit probably concerns conducted EMI emissions. In mains operated applications, due to the ripple appearing across the input bulk capacitor, the switching frequency is modulated at twice the mains frequency f_L, with a depth depending on the ripple amplitude. This causes the spectrum to be spread over frequency

bands, rather than being concentrated on single frequency values. Especially when measuring conducted emissions with the average detection method, the level reduction can be of several dBµV. Figure 3 shows a comparison made on the same L6565-based SMPS, fixed frequency first and then QR-operated. It is then possible to reduce the size and the cost of the EMI filter.

Figure 3. Conducted EMI (average detection): a) fixed-frequency operation; b) QR operation.



Another important benefit is a high safety degree under short circuit conditions: since the conduction cycles of the MOSFET are inhibited until the transformer is fully demagnetized, flux runaway and, therefore, transformer saturation are not possible. Moreover, as during a short circuit the demagnetization voltage is very low, the system will be led to work at a very low frequency, with a very small duty cycle. As a result, the power that the converter will be able to carry is very low.

Additionally, QR approach makes use of the otherwise undesirable parasitic drain capacitance to generate a zero-voltage condition that minimizes turn-on losses of the MOSFET. An external capacitor may be added in parallel to the MOSFET or across the primary winding. This will reduce the impact that the spread of the parasitic C_d has on f_r, smooth the negative-going edge of the drain voltage after transformer's demagnetization (in the interests of EMI) and reduce the dV/dt at turn-off, with the benefit of lower turn-off losses and EMI generation.

Finally, the way the system processes power does not change, thus designer's experience with standard flyback can be fully exploited and there is very little additional know-how needed. Advantages and Disadvantage are Discussed here

To complete the picture, it must be said that there are also some drawbacks. The system actually works in DCM, thus currents' peak and RMS values are quite high: this will result mainly in higher conduction losses in the MOSFET and greater high frequency losses in the transformer. This suggests not using this approach for power levels above 120-150W in wide range mains applications and above 200 W with European mains. Furthermore, the high operating frequency when the converter is lightly loaded partly cancels the advantages of the ZVS in terms of power losses. Finally, while in a standard flyback the design can be optimized in order for a 600V-rated MOSFET to be used in European or wide range mains applications, optimizing the design in a QR system will likely lead to the use of a more expensive 800 V-rated MOSFET.

In the following, the topology's operation will be discussed in details and a set of equations useful for the design will be given. Then the use of the L6565, a PWM controller specific for this particular topology, will be discussed in details. Finally, an application (an SMPS for TV) will be developed and the evaluation result of its prototype, as well as some significant waveforms, will be presented.

QR OPERATION: TIMING AND ENERGETIC RELATIONSHIPS

To generate the equations governing the operation of a QR ZVS flyback converter, with the aim of providing a design method, some simplifying assumptions will be made:

1) Fall and rise times of both voltage and current waveforms are negligible.
2) Transformer's non-idealities will be neglected (no delay in the primary-to-secondary energy transfer, peak secondary current proportional to the primary one depending on primary-to-secondary turn ratio n).
3) The system is controlled so that the time elapsed from transformer's demagnetization to MOSFET's turn-on is kept equal to T_v, eqn. (4), under all operating conditions.

That being stated, it will be useful to refer to the simplified schematic of figure 4 as well as the waveforms of figure 2. The ON-time of the MOSFET is expressed by:

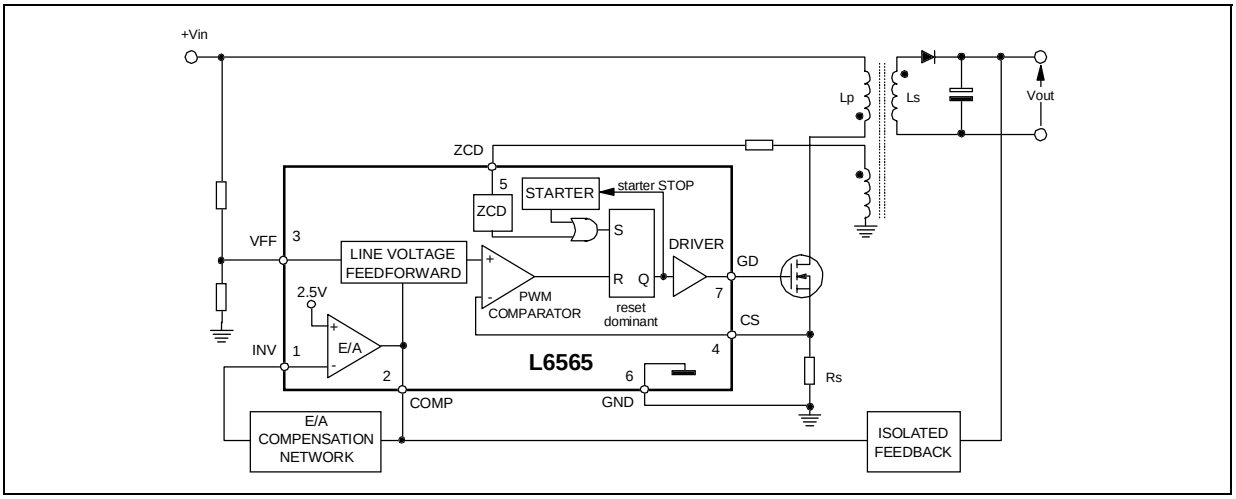
$$T_{ON} = \frac{L_p \cdot I_{PKp}}{V_{in}} \quad (6)$$

After T_{ON} has elapsed the MOSFET is turned off and energy is transferred to the secondary winding. The time needed for the discharge of this energy to the output, referred to as "freewheeling time", will be:

$$T_{FW} = \frac{L_s \cdot I_{PKs}}{V_{out} + V_f} = \frac{\frac{L_p}{n^2} \cdot (n \cdot I_{PKp})}{V_{out} + V_f} = \frac{L_p \cdot I_{PKp}}{V_R}, \quad (7)$$

where L_S is the inductance of the secondary winding and I_{PKs} the peak secondary current.

Figure 4. Block diagram of an L6565-based QR ZVS flyback converter.



The total conversion cycle period T_{SW} is the sum of T_{ON}, T_{FW} and T_v, and the switching frequency is:

$$f_{SW} = \frac{1}{T_{SW}} = \frac{1}{T_{ON} + T_{OFF} + T_v}. \quad (8)$$

Since the system actually works in DCM, the peak primary current is related to the input power of the converter, P_{in} (more precisely, to transformer's input power), according to the well-known relationship:

$$P_{in} = \frac{1}{2} \cdot L_p \cdot I_{PKp}^2 \cdot f_{SW}. \quad (9)$$

By substituting (4), (6) and (7) in (8) and combining with (9), the switching frequency can be expressed as a function of the characteristic parameters of the circuit (L_p, V_R, f_r) and of the operating conditions (P_{in}, V_{in}). The result can be conveniently expressed in the following terms:

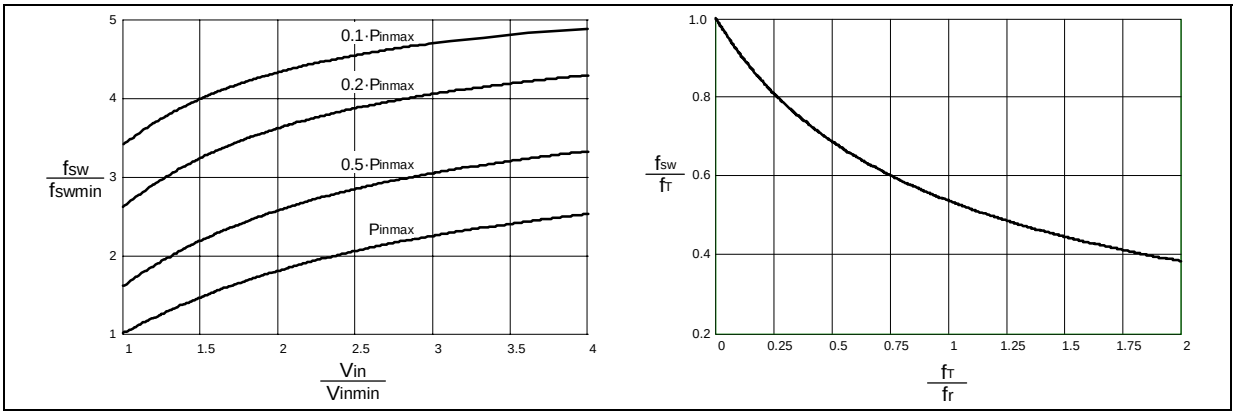
$$f_{SW} = \frac{2 \cdot f_T}{1 + \frac{f_T}{f_r} + \sqrt{1 + 2 \cdot \frac{f_T}{f_r}}}, \quad (10)$$

where:

$$f_T = \frac{1}{2 \cdot P_{in} \cdot L_p \cdot \left(\frac{1}{V_{in}} + \frac{1}{V_R}\right)^2} \quad (11)$$

is the "transition frequency", that is the frequency the system would work at if $f_r \rightarrow \infty \Rightarrow T_v = 0$, which would occur if $C_d = 0$. The name comes from the fact that this frequency is characteristic of TM operation.
Actually, in case $f_T << fr$, it is possible to estimate f_{sw} by using eqn. (11) instead of the more complex formula (10). The two quantities become more and more different as the ratio f_T / f_r increases (see the right diagram of figure 5), that is as the delay T_v becomes a significant portion of the switching period T_{sw}.

Figure 5. Switching frequency vs. operating conditions (left) and f_{sw} vs. f_T (right) relationships



The switching frequency f_{sw} changes with the operating conditions in so far as the transition frequency f_T changes, as shown in the left diagram of figure 5. Eqn. (11) shows that the minimum value of f_{sw}, f_{swmin}, which is usually a design constraint, will be reached at maximum input power (P_{inmax}) when the input voltage V_{in} is at its minimum, V_{inmin}. Being the converter operated from the AC mains, V_{inmin} is the valley voltage across the input bulk capacitor. Therefore, to fulfill the design requirement concerning the minimum operating frequency, the primary inductance L_p will be selected not exceeding the following upper limit:

$$L_{pmax} = \frac{1}{\left[\sqrt{2 \cdot P_{in\ max} \cdot f_{sw\ min}} \cdot \left(\frac{1}{V_{in\ min}} + \frac{1}{V_R}\right) + \pi \cdot f_{sw\ min} \cdot \sqrt{C_d}\right]^2}, \qquad (12)$$

The equations that provide the quantities of interest in the design of a QR ZVS flyback converter can be easily derived considering that the system is inherently of DCM type, although working at a frequency subject to change with the operating conditions. Table 1 summarizes these relationships.

Table 1. Main Electrical Quantities in QR ZVS Flyback Converters

	Parameter	Primary Side	Secondary Side
1	Duty Cycle	$D = \frac{1}{V_{in}} \cdot \sqrt{2 \cdot P_{in} \cdot L_p \cdot f_{sw}}$	$D' = \frac{1}{V_R} \cdot \sqrt{2 \cdot P_{out} \cdot L_p \cdot f_{sw}}$
2	Peak Current	$I_{PKp} = \sqrt{\frac{2 \cdot P_{in}}{L_p \cdot f_{sw}}}$	$I_{PKs} = \frac{2 \cdot I_{DCs}}{D'}$
3	DC Current	$I_{DCp} = \frac{1}{2} \cdot I_{PKp} \cdot D$	$I_{DCs} = \frac{P_{out}}{V_{out}}$
4	Total RMS Current	$I_{RMSp} = I_{PKp} \cdot \sqrt{\frac{D}{3}}$	$I_{RMSs} = I_{PKs} \cdot \sqrt{\frac{D'}{3}}$
5	AC RMS Current	$I_{ACp} = \sqrt{I_{RMSp}^2 - I_{DCp}^2}$	$I_{ACs} = \sqrt{I_{RMSs}^2 - I_{DCs}^2}$
6	Peak Voltage	$V_{PKDS} = V_{in} + V_R + V_{spike}$	$V_{REV} = V_{out} \cdot \left(1 + \frac{V_{in}}{V_R}\right)$
7	Switching frequency modulation depth	$\frac{\Delta f_{sw}}{f_{sw}} = \frac{2 \cdot f_r - f_{sw}}{2 \cdot f_r + f_{sw}} \cdot \frac{2 \cdot V_R}{V_R + V_{in}} \cdot \frac{\Delta V_{in}}{V_{in}}$	

Once the switching frequency has been found from (10), or simply from (11) if that is the case, all of the quantities listed in the table can be easily calculated. Obviously, current stresses will be calculated at minimum input voltage and maximum load, while voltage stresses will be calculated at maximum input voltage.

P_{out} is the power delivered to the load, while the input power P_{in} that appears explicitly or not in all of the relationships should be the one processed by the primary side of the transformer. This is the sum of the power coming out of the secondary side, that lost inside the transformer due to copper and ferrite losses and the one not transferred (and mostly dissipated in a clamping circuit) because of the leakage inductance. A transformer efficiency η_t could be estimated, such that:

$$P_{in} = \frac{P_{out} \cdot \left(1 + \frac{V_f}{V_{out}}\right)}{\eta_t} \qquad (13)$$

The efficiency η_t is usually quite high, typically 92 to 98%, depending on transformer's size and construction technique. If at design-time the designer feels more confident of estimating converter's overall efficiency η rather than transformer's η_t, Pin can be considered as the input power of the converter, that is the ratio of P_{out} to η, with acceptable approximation.

QR OPERATION: CONVERTER'S POWER CAPABILITY AND L6565'S LINE FEEDFORWARD FUNCTION

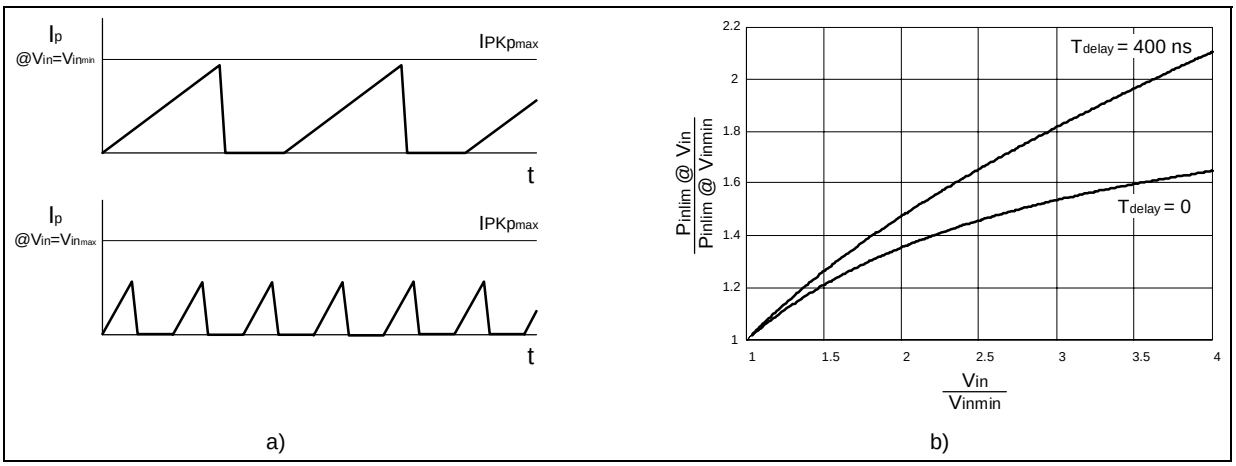
Current-mode control will be used, thus the maximum power that the system is able to deliver to the output (P_{inlim}), that is its power capability, is controlled by means of pulse-by-pulse current limitation. This is usually done by clamping the control voltage that programs the peak primary current I_{PKp} at a fixed value V_{csx}, in this way limiting the maximum peak primary current I_{PKpmax}.

In fixed-frequency DCM flyback converters, this provides a power capability that, ideally, is independent of the input voltage V_{in}. Actually, there is a slight dependence due to the internal propagation delay of the controller and the MOSFET's turn-off delay (200 to 500 ns overall).

Differently, in QR ZVS flyback even in the ideal case of no delay, power capability strongly depends on the input voltage. In wide-range mains applications this can be an issue.

The situation is illustrated in figure 6a. The upper trace shows the primary current waveform at minimum input voltage: the peak current is close to the maximum, thus just a small extra output power will trip the current limitation circuit. The lower trace shows the primary current waveform under the same load conditions at maximum input voltage. Being the switching frequency higher, then the peak current will be lower: a much larger power will be allowed to pass before pulse-by-pulse limitation is tripped.

Figure 6. a) Primary current at min. and max. input voltage; b) Power capability vs. input voltage

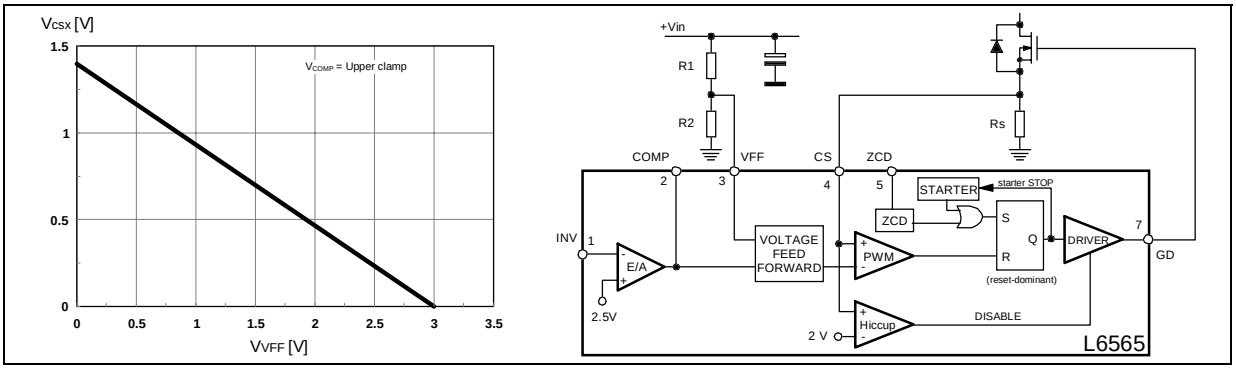


The effect of such delay is shown in figure 6b, where P_{inlim} vs. V_{in} is shown for both zero and 400 ns delay in a typical design (V_{in} = 100 to 400V; P_{inlim} = 125W, f_{swmin} = 100 kHz, L_p = 110µH, V_R = 150V, C_d = 1.5nF).

Even ideally (T_{delay} = 0), at 400V input the power throughput that trips the pulse-by-pulse current limitation is about 1.65 times higher than what needed at 100V. Accounting for the delay the limit rises at 2.11 times.

To overcome this problem, the L6565 has the Line Feedforward function available. It acts on the clamp level of the control voltage V_{csx}, that is on the overcurrent setpoint, so that it is a function of the converter's input voltage, sensed through a dedicated pin (#3, VFF): the higher the input voltage, the lower the setpoint. The diagram of figure 7a shows the relationship between the voltage at the pin VFF and V_{csx} (with the error amplifier saturated high in the attempt of keeping output voltage regulation). The schematic in figure 7b shows how the function is included in the control loop.

Figure 7. a) Overcurrent setpoint vs. VFF voltage; b) Line Feedforward function block



Quantitatively, the maximum power capability P_{inlim} can be expressed by means of eqns. (6), (7) and (8), in which $I_{PKp} = I_{PKpmax}$, substituted in (9):

$$P_{in\ lim} = \frac{1}{2} \cdot L_p \cdot \frac{I_{PKp\ max}^2}{I_{PKp\ max} \cdot L_p \cdot \left(\frac{1}{V_{in}} + \frac{1}{V_R}\right) + T_v} . \qquad (14)$$

Ideally, the maximum peak primary current I_{PKpmax} (which should slightly exceed the value derived from line 2 in table 1 @ $V_{in} = V_{inmin}$) would be equal to V_{csx}/Rs, however the internal propagation delay as well as the MOSFET's turn-off delay, has to be accounted for. This causes the actual I_{PKpmax} to exceed the ideal value by an amount proportional to the input voltage:

$$I_{PKp\ max} = \frac{V_{csx}}{Rs} + \frac{V_{in}}{L_p} \cdot T_{delay} . \qquad (15)$$

The Line Feedforward block combines the voltage at pin VFF (proportional to the converter's input voltage) with the E/A output, thus determining the internal reference (V_{cs}) for the PWM comparator, according to the following relationship:

$$V_{cs} = 0.16 \cdot (V_{COMP} - 2.5) \cdot (3 - V_{VFF}) \qquad (16)$$

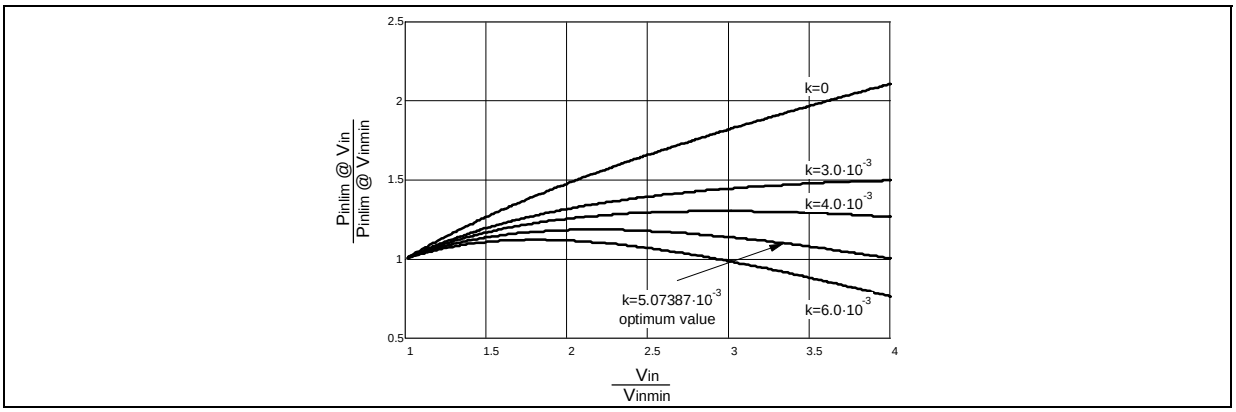
Note that in this equation V_{COMP} is ≥ 2.5V and V_{VFF} is ≤ 3V. Ideally, if either $V_{COMP} = 2.5$ or $V_{VFF} = 3$ the result is $V_{cs} = 0$, which forces the L6565 to stop switching. Actually eqn. (16) is not very accurate when either V_{COMP} or V_{VFF} get close to their respective limits: the effect of offsets and some non-linearity becomes significant. Thus the real $V_{cs} = 0$ condition and the switching halting may occur for values of V_{COMP} slightly below 2.5V and values of V_{VFF} slightly above 3V

The overcurrent setpoint (V_{csx}), graphically illustrated in the diagram of figure 7a, can be found considering the error amplifier at the limit of its linear dynamics ($V_{COMP} \cong 5.4V$). The resulting analytical V_{csx} vs. V_{VFF} relationship is:

$$V_{csx} = 0.467 \cdot (3 - V_{VFF}) = 0.467 \cdot (3 - k \cdot V_{in}), \qquad (17)$$

where k is the divider ratio R2/(R1+R2).
If this function is not needed for any reason, e.g. because of a narrow input voltage range, the pin will be grounded. The overcurrent setpoint will be set at $V_{csx} = 1.4V$ regardless of the converter's input voltage.

Figure 8. Correction characteristics of Line Feedforward



The diagram of figure 6b, as well as equations 14 and 15, shows a non-linear relationship between P_{inlim}, V_{in} and V_{csx}, hence the linear correction (17) will not result in a perfect compensation. A considerable reduction of the power capability change over the input voltage range will be achieved anyway.

Figure 8 shows the effect of the compensation circuit on the converter's power capability for different values of k (a T_{delay} of 400 ns is assumed) in the typical design previously considered.

The optimum value of k, k_{opt}, which minimizes the power capability variation over the input voltage range, could be found by combining equations 14, 15 and 17, imposing that the value of P_{inlim} is the same at the extremes of the input voltage range and solving for k. However, the value of the sense resistor Rs, which appears in (15), is a function of k_{opt} in turn. The exact calculation is very complex, and non-idealities shift the actual optimum value from the theoretical one. It is therefore more practical to provide a first cut value, simple to be calculated. Then, Rs will be chosen on this basis and k_{opt} found empirically.

A great simplification comes from assuming $T_v = 0$ (exact TM operation) and $T_{delay} = 0$; k_{opt} will then be:

$$k_{opt} = 3 \cdot \frac{V_R}{V_{in\,min} \cdot V_{in\,max} + (V_{in\,min} + V_{in\,max}) \cdot V_R} \tag{18}$$

With $k = k_{opt}$, the maximum value of P_{inlim}, reached at:

$$V_{in} = V_{inx} = \sqrt{V_R \cdot \left(V_R + \frac{3}{k_{opt}}\right)} - V_R\,, \tag{19}$$

exceeds P_{inlim} @ $V_{in} = V_{inmin}$ (= P_{inlim} @ $V_{in} = V_{inmax}$) by about 20%. It is worthwhile pointing out that, for given input voltage range and delay, this result does not depend on the specific design, only k_{opt} changes.

The value of Rs, can be determined from (15), again with $T_{delay} = 0$, resulting in:

$$Rs = 0.467 \cdot \frac{3 - k_{opt} \cdot V_{inmin}}{I_{PKpmax}}. \tag{20}$$

The approximate calculation yields a value of kopt equal to $3.913 \cdot 10^{-3}$, about 23% less than the exact value $5.074 \cdot 10^{-3}$. It can be a useful rule of thumb to use the value resulting from (18) increased by 20% as the starting point.

After choosing Rs, the value of k_{opt} can be fine-tuned experimentally to minimize converter's power capability changes over the input voltage range. To do so, it is necessary to check the power level where the converter loses regulation just at minimum and maximum input voltage and adjust k (e.g. using a trimmer) so as to make them equal. This could require, in turn, a modification of Rs, because the power level achieved in the previous step is slightly higher or lower than the target, thus some iteration might be needed. The values of R1 and R2 will be high enough to minimize the power dissipated on them, especially if there are requirements on the converter's efficiency under light load or no-load conditions.

The small-signal control-to-output-gain of the Line Feedforward block, needed for stability analysis, can be determined by differentiation of the large-signal model (16) and considering that $V_{VFF} = k_{opt} \cdot V_{in}$:

$$G_{FF} = \frac{\hat{v}_{cs}}{\hat{v}_{COMP}} = 0.16 \cdot (3 - k_{opt} \cdot V_{in}) \tag{21a}$$

Line Feedforward improves also the input ripple rejection ability of the system and limits the variation of the gain-bandwidth product of the small-signal control-to-output transfer function with the input voltage (see APPENDIX).

The small-signal line-to-output gain of the block is found again by differentiation of (16):

$$G'_{FF} = \frac{\hat{v}_{cs}}{\hat{v}_{in}} = -0.16k_{opt}(V_{COMP} - 2.5) = -\frac{k_{opt}}{3 - k_{opt} \cdot V_{in}} V_{cs}. \quad (21b)$$

QR OPERATION: BEHAVIOR UNDER SHORT CIRCUIT CONDITIONS

As previously said, a QR flyback converter operates safely under short circuit conditions at the output. The reason of that is that any new conduction of the MOSFET is inhibited as long as the transformer is not fully demagnetized. Equation 7, which is here recalled:

$$T_{FW} = \frac{L_P \cdot I_{PKp}}{V_R} = \frac{L_P \cdot I_{PKp}}{n \cdot (V_{out} + V_f)},$$

shows that, as the overload is progressively increased, the demagnetization time T_{FW} gets longer and longer: I_{PKp} is kept constant by the pulse-by-pulse limitation and the output voltage drops because the system is out of regulation. However, if T_{FW} exceeds the period T_{START} of the internal starter, the MOSFET will be switched on before the demagnetization is complete. In some cases, before $T_{FW} > T_{START}$, the reflected voltage V_R can be so low that the oscillation on the ZCD pin can no longer arm the internal circuit.

Whichever condition is met first, the converter will be forced to work at the frequency of the internal starter ($1/T_{START}$) and, likely, in CCM. Flux runaway, though now theoretically possible, is however extremely unlikely. Referring to [2] for the details of the calculations, the flux runaway condition for a dead short at the output is:

$$\frac{n \cdot V_f}{V_{in} + V_f} \leq \frac{T_{ONmin}}{T_{START}} \cong 10^{-3},$$

which is very tough to meet in normal offline applications, as one can easily see by using sensible values for n, V_{in} and V_f. T_{ONmin} is the minimum ON-Time that the L6565 can provide because of its internal delays and MOSFETS's Turn-Off delay, usually around 300-400ns.

To guarantee the operation described so far, the L6565 blanks the ZCD input for some time (3.5 µs min.) after the MOSFET has been turned off. In this way, situations like the one shown in figure 9a, relevant to a short circuit in a 50W converter using a controller not provided with this safety feature, are prevented. In that picture it is possible to see that the system is detecting the demagnetization of the leakage inductance and not that of the primary inductance. This causes a very high frequency operation - instead of a very low one - that has led to transformer saturation: the primary current reaches a peak of 8A in 400 ns with a slope pointing out only 15 µH inductance (the overcurrent setpoint was 2A, the primary inductance was 400 µH).

Figure 9. Short circuit waveforms in a system a) without ZCD blanking; b) with ZCD blanking

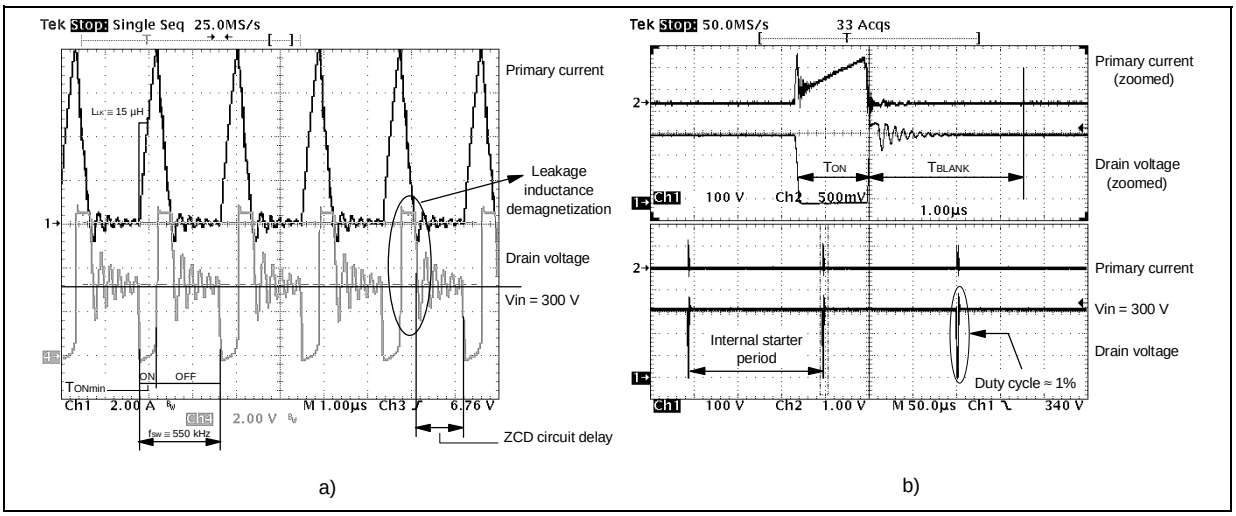


Figure 9b shows instead the operation previously described, allowed by the L6565, where the converter works at the frequency of the internal starter with a duty cycle of about 1%.

Dangerous short circuit conditions occur when there is an isolation failure on the secondary winding, e.g. due to a damaged wire coating, or when the secondary diode fails short (typical of axial diodes). Both of these failures reflect a short circuit to the transformer's primary side while the MOSFET is turned on [2]. The primary current rate of rise is then limited only by the leakage inductance of the transformer, like in figure 9a. If not properly handled, this very likely leads to the destruction of the system.

To protect the converter in the event of such failure, a comparator (shown in fig. 7b) senses the voltage on the current sense input and disables the gate driver if this voltage exceeds the 2nd level OCP, fixed at 2V. To re-enable the driver, first the IC must be turned off and then restarted: in other words, the Vcc voltage must fall below the UVLO threshold and then exceed again the start-up threshold.

With the gate driver disabled the quiescent current of the IC is unchanged and, since no energy is coming from the self-supply circuit, the Vcc capacitor will be discharged below the UVLO threshold after some time (see pin 8 in "L6565 pin usage" section). Then the device will initiate a new start-up cycle. This will result in a low-frequency intermittent operation (Hiccup-mode operation), with very low stress on the power circuit.

QR OPERATION: HIGH SWITCHING FREQUENCY AT LIGHT LOAD AND L6565'S FREQUENCY FOLDBACK FUNCTION

Equations (6) and (7) show that T_{ON} and T_{FW} can be however short if I_{PKp} (i.e. the load) tends to zero, in which case $f_T \rightarrow \infty$ and $f_{sw} \rightarrow 2 \cdot fr$. Although in the real-world operation the maximum switching frequency would be significantly lower than this theoretical limit, it could be of some hundred kHz and cause a considerable efficiency drop. This is why the L6565 has been provided with the Frequency Foldback function.

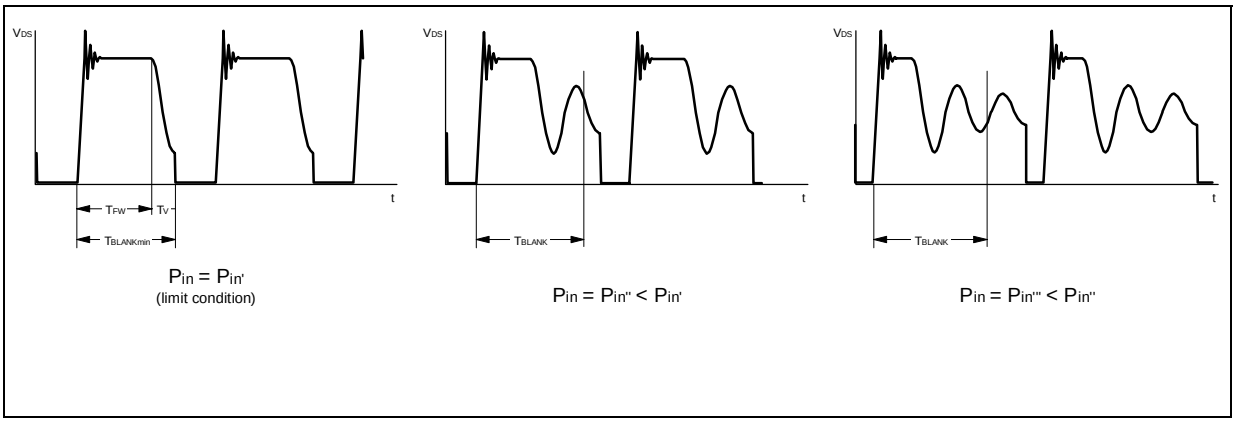
In principle, this function lies in putting a limit to the minimum OFF-time of the switch [3]. The blanking time of the ZCD circuit, used for safe operation under short circuit conditions and mentioned in the previous section, serves this purpose as well. Therefore, the QR operation considered so far will be maintained as long as:

$$T_{FW} + T_V \geq T_{BLANKmin}, \qquad (22)$$

where $T_{BLANKmin}$ is the aforesaid minimum blanking time (3.5 µs) of the Zero Current Detector (ZCD) circuit. The maximum operating frequency will then not exceed:

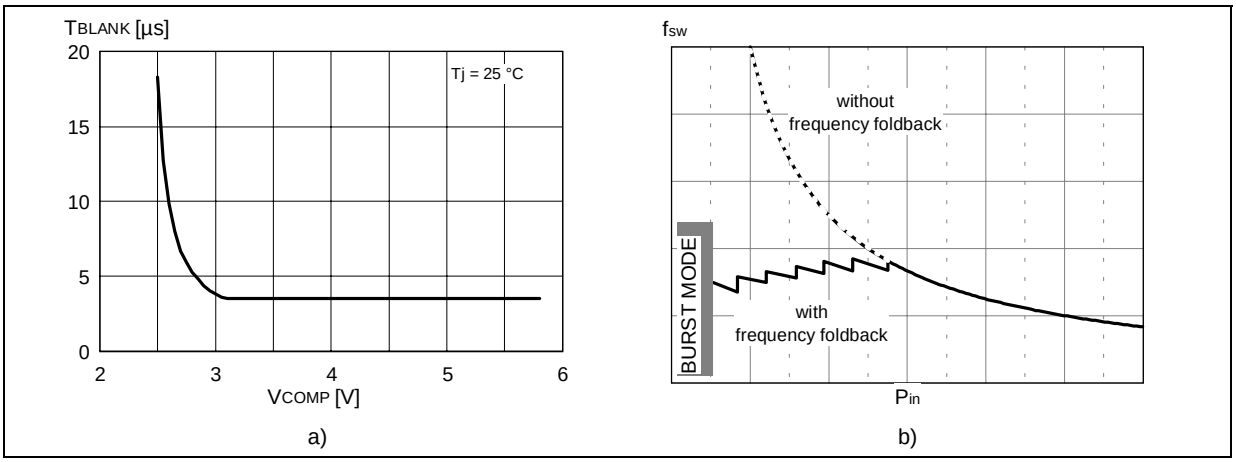
$$f_{swmax} = \frac{1}{T_{BLANKmin} \cdot \left(1 + \frac{V_R}{V_{in}}\right) - T_v \cdot \frac{V_R}{V_{in}}}.$$

Figure 10. Frequency foldback: ringing cycle skipping as the load is progressively reduced



If the load current and the input voltage are such that the condition (22) is not fulfilled, the system will enter the "Frequency Foldback" mode, a sort of "ringing cycle skipping" illustrated schematically in figure 10.

Figure 11. a) ZCD blanking time vs. error amplifier output voltage; b) qualitative frequency trend



Any negative-going edge of the voltage at pin 5 that occurs during the blanking time is ignored; the first negative-going edge after T_{BLANK} has elapsed will trigger the ZCD circuit and determine MOSFET's turn-on.

The peculiarity of the Frequency Foldback function, however, is that the duration of T_{BLANK} is a function of the error amplifier output V_{COMP}, as shown in the diagram of figure 11a. The lower the load is, the lower V_{COMP} will be and this, in turn, leads to a longer T_{BLANK}. Therefore, more and more ringing cycles will be skipped and the operating frequency will gradually decay, as shown qualitatively in the diagram of figure 11b.

While the Frequency Foldback is active, uneven switching cycles may be observed, due to the fact that the OFF-time of the MOSFET is allowed to change with discrete steps ($2 \cdot T_V$), while the OFF-time needed for cycle-by-cycle energy balance may fall between two contiguous steps. One or more longer switching cycles will be then compensated by one or more shorter ones, and vice versa. This phenomenon is absolutely normal and there is no appreciable effect on the performance of the converter and its output voltage.

When the load is low enough, so many ringing cycles and will be skipped that their amplitude becomes very small and they can no longer arm the ZCD circuit (see pin 5 in "L6565 pin usage" section). In that case, after some time the ZCD circuit is idle, the internal starter of the IC will be activated, resulting in burst-mode operation: a series of few switching cycles spaced out by long periods (400µs typ.) where the MOSFET is in OFF state.

Actually the operation at very light load can be more complex than so far described: another mechanism may be involved that interacts with the blanking time of the ZCD circuit.

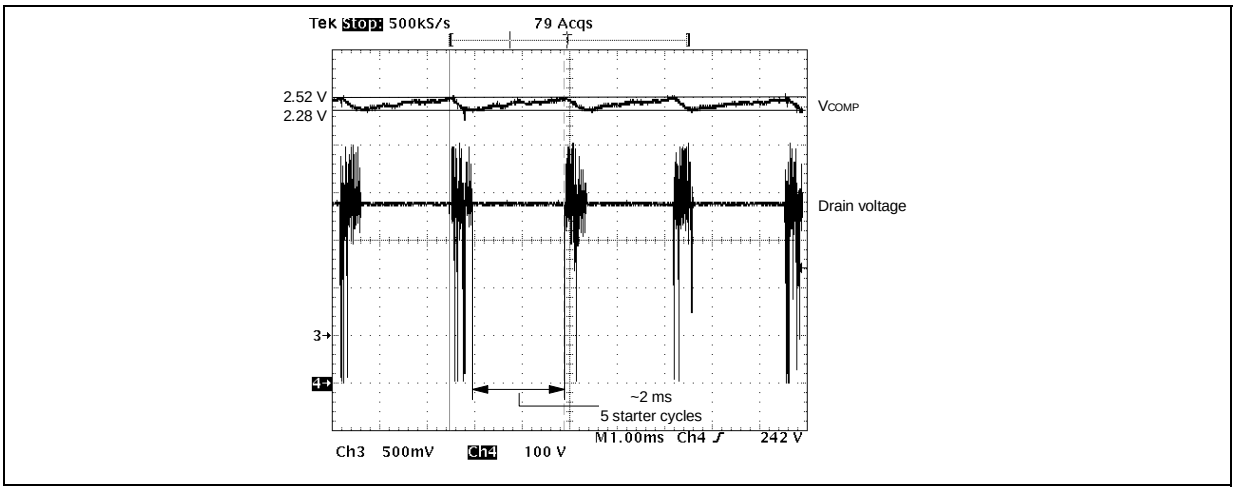
To explain this mechanism it is useful to recall eqn. (16), which provides the output of the Line Feedforward block (i.e. the internal reference for the PWM comparator): it states that, if the voltage V_{COMP} is 2.5V (or lower), the output V_{cs} is zero and the L6565 stops switching.

Depending on parameters such as the input voltage, the residual load (i.e. resistors of the output divider, opto-coupler bias, dummy load resistors, etc.) and the transformer's primary inductance, at very light load it is possible to hit the minimum ON-time ($T_{ONmin} \approx 400$ ns) of the L6565 and, despite the long switch OFF-times imposed by the ZCD blanking, the energy delivered each cycle may exceed the short-term demand from the load. This excess energy causes the output voltage to increase a little and the control loop to react by lowering V_{COMP} until $V_{cs} = 0$ and switching is stopped, to maintain the long-term energy balance. The output voltage will now slowly decay and the control loop will react by increasing V_{COMP}. Switching will be re-enabled as the $V_{cs} = 0$ condition is removed, but will actually restart as the first starter pulse comes after re-enabling. Also in this case the result will be burst-mode operation.

At most, the burst repetition rate can be as high as the starter frequency but, depending on the converter's output capacitance, the residual load and the control loop response, one or even more starter cycles may be skipped, giving origin to a burst repetition rate submultiple of the starter frequency. This latter behavior is shown in fig. 12.

As compared to a burst-mode operation occurring at the starter frequency, there is usually no special advantage in this starter cycle skipping mode, since the duration of each burst is longer and the average number of switching cycles per second, which the light-load losses are related to, does not change much.

Figure 12. Burst-mode at very light load: starter cycle skipping



QR ZVS FLYBACK: DESIGN CONSIDERATIONS

- *Minimum switching frequency selection.* With the aim of minimizing transformer's size, f_{swmin} should be as high as possible. A high f_{swmin}, besides increasing losses, reduces the load range where the converter works in QR, that is, frequency foldback and, eventually, burst mode will occur at higher load currents (which, however, might be desirable). Often, the choice is influenced by EMI considerations too.
- *Reflected voltage selection.* In order to extend the input voltage range where the ZVS condition (5) is met, the reflected voltage should be as high as possible. The upper limit to V_R is usually determined by MOSFET's voltage rating. The selection of V_R affects also many important parameters and electrical quantities of the converter, as summarized in table 2. The designer should trade off these sometimes contrasting requirements one against the other to find the optimum solution for their specific application.

Table 2. Effect of V_R selection on converter's performance

Increasing (⇑) VR results in:	
Parameter	**Change**
Transformer's primary inductance	⇑
Minimum required Transformer's Area Product	⇑
Drain Ringing Frequency	⇓
Switching frequency	⇑(*)
Peak and RMS primary current	⇓
Peak and RMS secondary current	⇑
MOSFET's conduction losses	⇓
MOSFET's turn-on losses	⇓
MOSFET's total losses	⇓ (**)
Secondary rectifier(s) losses	⇑
Maximum drain peak voltage	⇑
Maximum secondary rectifier(s) reverse voltage	⇓
(*) For a given f_{swmin}, the rate of rise vs. V_{in} and I_{out} increases; (**) At high input voltage; at low input voltage V_R has little effect.	

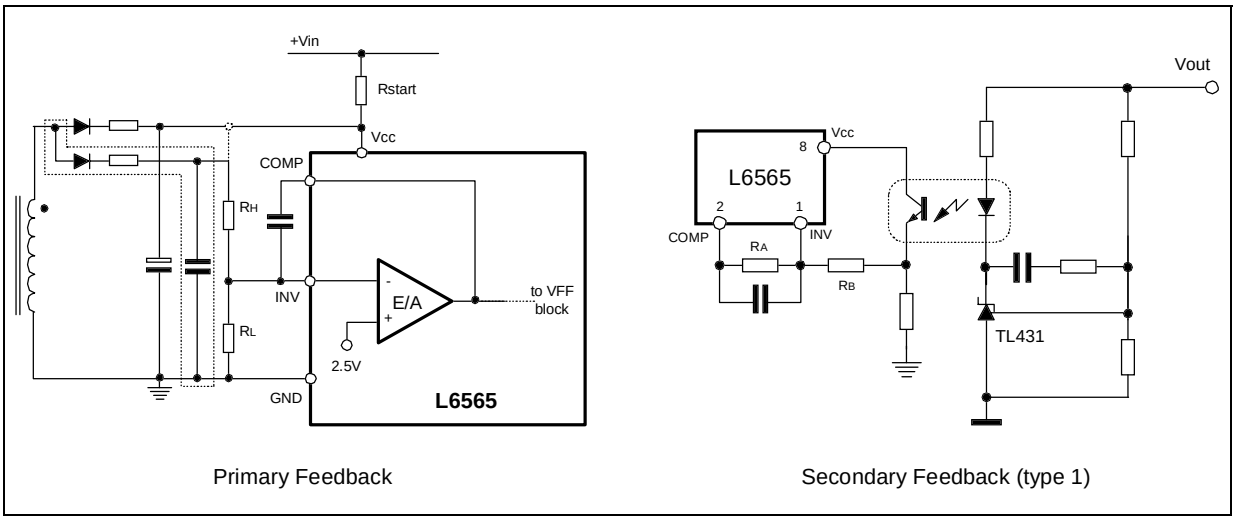
- *Transformer design.* Once the electrical specification of the transformer has been defined (the primary inductance is found from (12), the primary-to-secondary turn ratio from $n = V_R / (V_{out} + V_f)$, the peak and RMS currents from table 1, at minimum input voltage), the design of the transformer is carried out just like for any fixed-frequency DCM flyback transformer. Refer to [4] for a handy design procedure. Also the considerations about its construction are exactly the same.

L6565 PIN USAGE

Pin 1 (INV). It is the inverting input of the E/A. This pin can be used in case of both primary and secondary feedback technique, as shown in figure 13.

The circuit for primary feedback shown in figure 13 is recommended when the extremely low consumption before start-up of the L6565 is to be fully exploited. The parts in the shaded region can be omitted and the resistor divider (R_L and R_H) that sets the output voltage be connected directly to the Vcc rail. Of course, in this case the consumption of R_L and R_H will be accounted for when designing the start-up circuit (see pin 8).

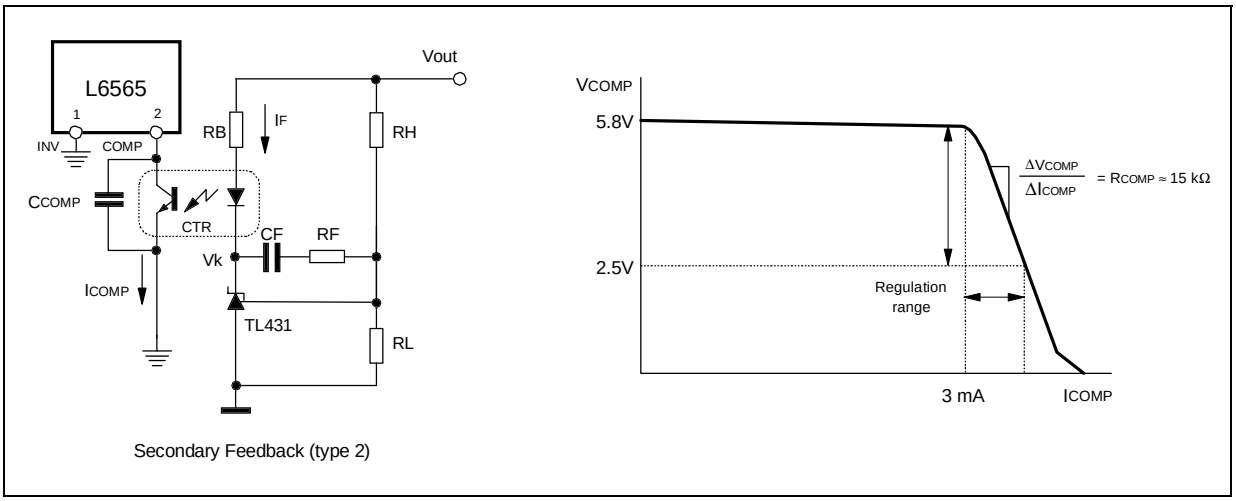
Figure 13. Use of L6565's error amplifier



In case of the secondary feedback configuration shown in figure 13, the L6565's error amplifier is used as an op-amp in inverting configuration, with a gain fixed by the ratio R_A/R_B. The internal reference is not involved in the output voltage setting (this is done at the secondary side by the TL431); it just sets the quiescent point of the circuit. The resistors will be selected keeping in mind that the current capability of the E/A must not be exceeded and the gain must be large enough to account for the entire E/A's dynamics.

Pin 2 (COMP). E/A output. Usually, this pin is used for the compensation of the voltage control loop and the relevant network is connected between this pin and INV (#1), as shown in the schematics of figure 13. Compensation networks from this pin to ground are not effective since the E/A is a voltage mode type (with low output impedance).

Figure 14. Use of pin COMP to directly modulate the duty cycle in secondary feedback



In a different type of secondary feedback, shown in figure 14, the pin INV is grounded and the E/A of the L6565 (which is therefore unbalanced high) is used as a current source. The characteristic of this current source is shown in figure 14 too: the voltage V_{COMP} is changed (and the duty cycle controlled) by modulating the current I_{COMP} sunk from the pin within the regulation range. In this region, a change of I_{COMP} causes a change of V_{COMP} corresponding to a resistance $R_{COMP} \approx 15\ k\Omega$. Forcing pin COMP below 2.25V will cause the L6565 to stop switching. Anyway, it is recommended to take the pin to GND not directly, but through a 390 to 470Ω resistor.

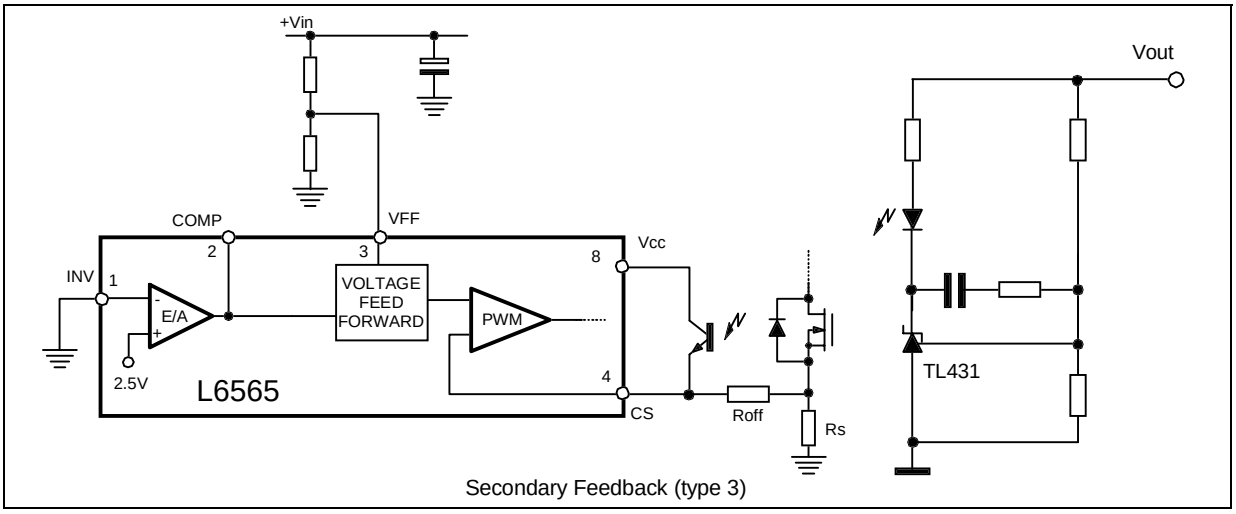
Pin 3 (VFF). Line feedforward input. Typically, a resistor divider connected as shown in figure 7 applies to this pin a voltage proportional to the converter's input voltage. Its determination is dealt with in the paragraph describing of the Line Feedforward function.

A small capacitor (typically from 1 to 10 nF), connected between pin 3 and ground is usually recommended to filter out any noise that may be coupled with the pin (which is a high impedance point).

Pin 4 (CS). Inverting input of the PWM comparator. Through this pin, the L6565 reads the instantaneous inductor current, converted to a proportional voltage by the external sense resistor (Rs). As this signal crosses the threshold set by the output of the Line Feedforward block, the PWM latch is reset and the power MOSFET is turned off. The MOSFET stays in OFF-state until the PWM latch is set again either by an appropriate signal on the ZCD pin (see pin 5 description) or by the internal starter in the absence of that. An internal circuit ensures that the PWM latch cannot be set until the signal on the pin CS has disappeared.

The current sense pin can be used in a particular arrangement of the feedback loop shown in figure 15. In this circuit the optocoupler provides output voltage regulation by modulating the current injected into the offset resistor Roff, depending on the information coming from the secondary side, and changing the dynamics allowed to the signal across the sense resistor.

Figure 15. Secondary feedback arrangement suggested for synchronized mode operation



The E/A of the L6565 is not used at all for regulation and stays unbalanced high. This feedback arrangement is recommended when the device is required to work in synchronized mode and not as a QR controller. In fact, being the E/A output saturated high, the blanking time of the ZCD is fixed at $T_{BLANKmin} = 3.5\ \mu s$, thus allowing the IC to be synchronized up to frequencies over 250 kHz, regardless of the line/load conditions.

Pin 5 (ZCD). Input to the Zero Current Detector circuit. Transformer demagnetization will be sensed through the auxiliary winding that powers the IC: in fact the voltage developed by this windings is an exact replica of the drain voltage, scaled down by the primary-to-auxiliary winding turn ratio m (see timing diagram (a) in fig. 16a).

The ZCD circuit is negative-going edge triggered: when the voltage on the pin falls below 1.6V it sets the PWM latch and the MOSFET is turned on. However, to do so, the circuit must be first armed: prior to falling below 1.6V, the voltage on pin 5 must experience a positive-going edge exceeding 2.1V (typically due to MOSFET's turn-off in QR operation). This function is realized with a comparator with hysteresis and a monostable that is positive-going edge triggered, as shown in the block diagram of figure 16. The relevant signals are shown in the timing diagram a) of figure 16. The ZCD circuit is blanked for some time after MOSFET's turn-off, so that any negative-going edge occurring before this time has elapsed is ignored (see "Frequency Foldback"). This is illustrated in the timing diagram of figure 17.

Figure 16. ZCD pin internal block diagram and operation

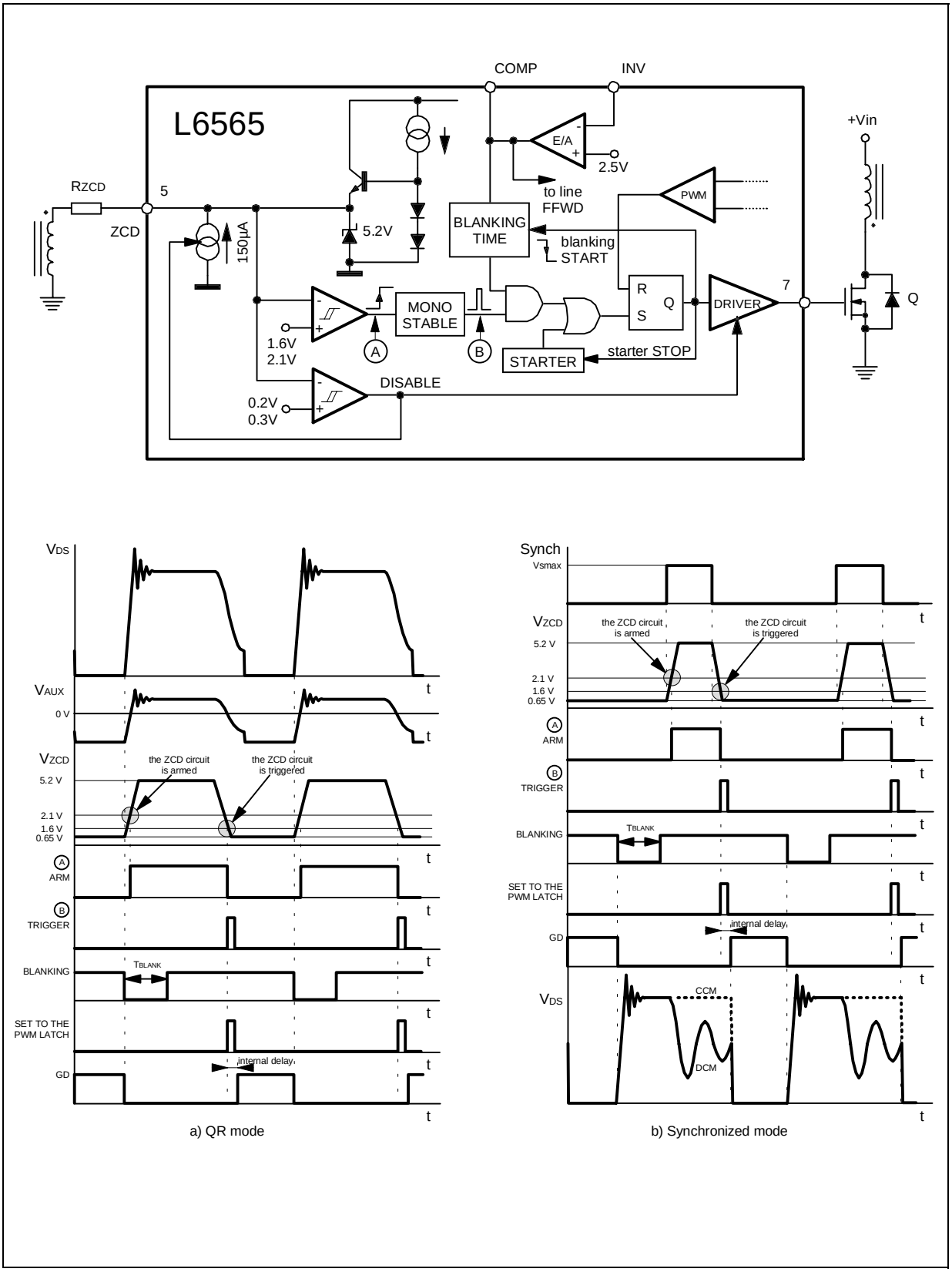
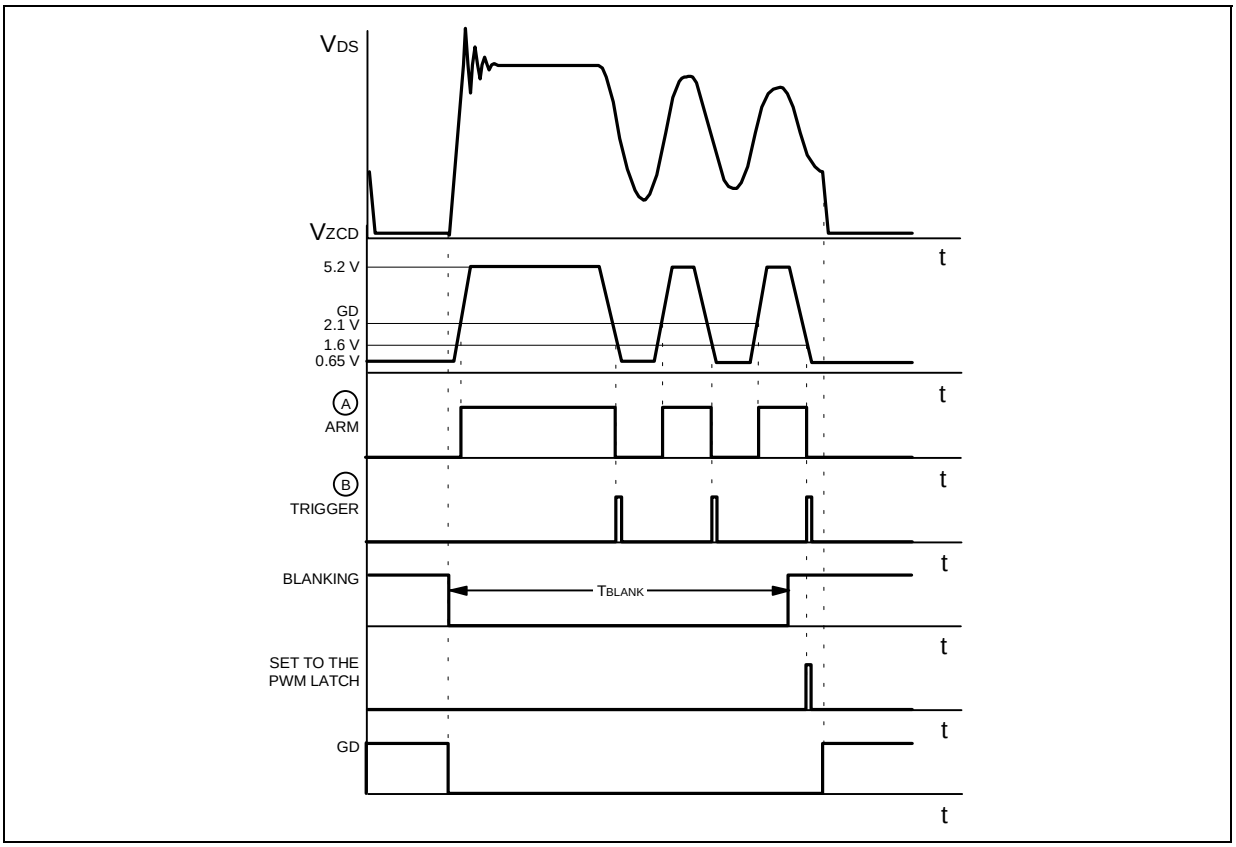


Figure 17. Frequency Foldback: timing diagram showing ZCD operation at light load



To minimize the external interface with the synchronization source (whether it is the auxiliary winding or an independent clock), the voltage at the pin is both top and bottom limited by a double clamp. The upper clamp is typically located at 5.2V, while the lower clamp is at one VBE above zero. The interface will then be made by just one resistor that has to limit the current sourced by and sunk from the pin within the rated capability of the internal clamps (3 mA min. each). To select its value, one should consider the worst condition that occurs while the MOSFET is in ON-state at maximum input voltage. The minimum resistance value will then be:

$$R_{ZCDmin} = \frac{\frac{V_{in\ max}}{m} + 1}{3} \quad [k\Omega]$$

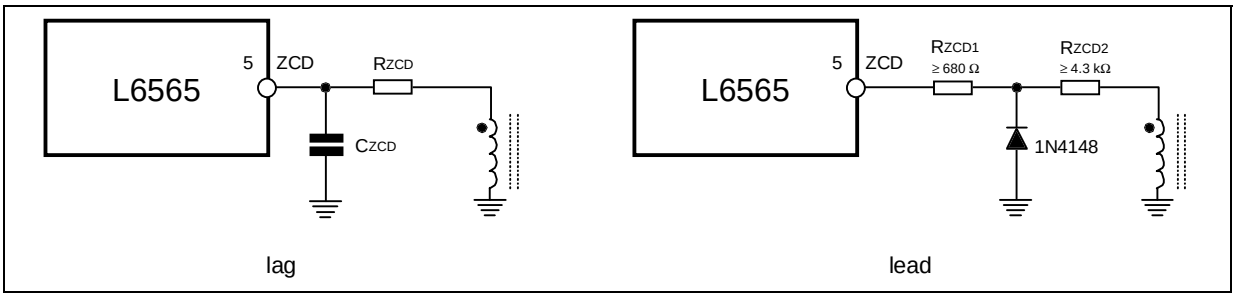
considering the maximum lower clamp level (1V) and the minimum source capability of the pin (3 mA).

The value can be experimentally adjusted to fine tune the ZCD circuit delay so as to make it equal to T_v and optimize MOSFET's turn-on. A higher resistance provides a longer delay and vice versa. However, values over 100 to 150 kΩ have little effect on the delay and, on the other hand, sometimes the minimum resistor value R_{ZCDmin} still provides too long a delay.

In case of need, either of the two circuits shown in figure 18 can be used to extend the adjustment range of the ZCD circuit delay. In the lag circuit C_{ZCD} is usually a few pF capacitor; its value can be increased according to the need. In the lead circuit the diode limits the negative voltage at -1V, worst case. From the above formula, the minimum standard value for R_{ZCD1} is 680Ω. Now R_{ZCD2} must be such that the total resistance from the pin ZCD to ground is over 5kΩ, otherwise the L6565 could not start-up. At any rate, the current sunk from the pin while the MOSFET is in OFF-state must never exceed the rated capability, then also the following condition must be met:

$$R_{ZCD2} > \frac{\frac{V_R}{m} - 4.7}{3} - R_{ZCD1} \quad [k\Omega]$$

Figure 18. Circuits to extend the adjustment range of the ZCD circuit delay



If the pin is driven by an external signal, the L6565 will be synchronized to (the negative-going edges of) that signal. To work properly, its period must be greater than the ZCD blanking time, its high level V_{smax} greater than 2.1V and its low level V_{smin} lower than 1.6V.

With reference to the timing diagram b) in figure 16, the minimum limiting resistor will be either:

$$R_{ZCDmin} = \frac{V_{s\,max} - 4.7}{3}\ [k\Omega] \quad \text{or} \quad R_{ZCDmin} = \frac{V_{s\,min} + 1}{3}\ [k\Omega]$$

whichever is greater (provided V_{smax} is greater than 4.7V and V_{smin} less than 1V).

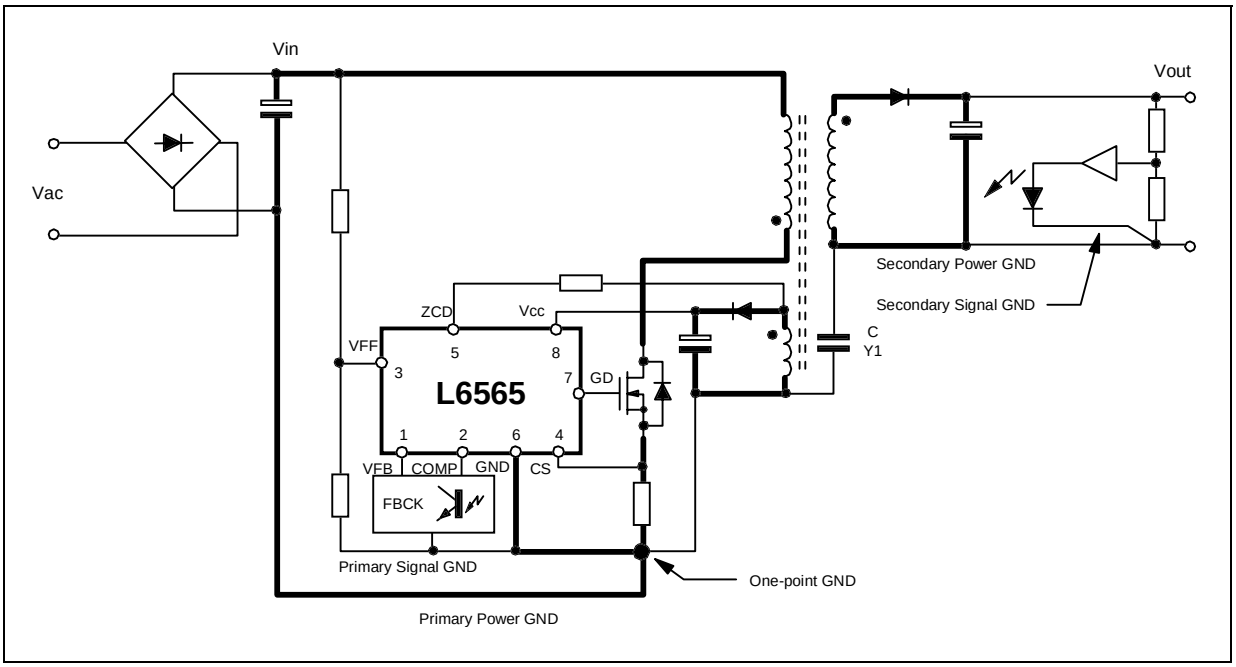
This pin develops a disable function too. The device will be shut down if the voltage at the pin is forced externally below 150mV. To do so, the capability (10mA max.) of the lower clamp has to be exceeded. Any small signal NPN can be used to do the job.

The IC restarts when the external pull-down is removed (provided its Vcc is still above the UVLO), since an internal 150µA pull-up generator, active only while the IC is disabled, lets the voltage go up. The current consumption during shutdown is reduced at about 1.4mA.

Pin 6 (GND). Ground. This pin acts as the current return for both the signal internal circuitry and for the gate drive current. When layouting the printed circuit board, these two paths should run separately, as shown in the schematic of figure 19.

The bold traces carry pulsed high current so they should be as short and fat as possible in the PCB. This will keep both resistive and inductive effects to a minimum, in favor of efficiency as well as radiated RFI.

Figure 19. Recommended ground routing in an L6565-based QR ZVS flyback

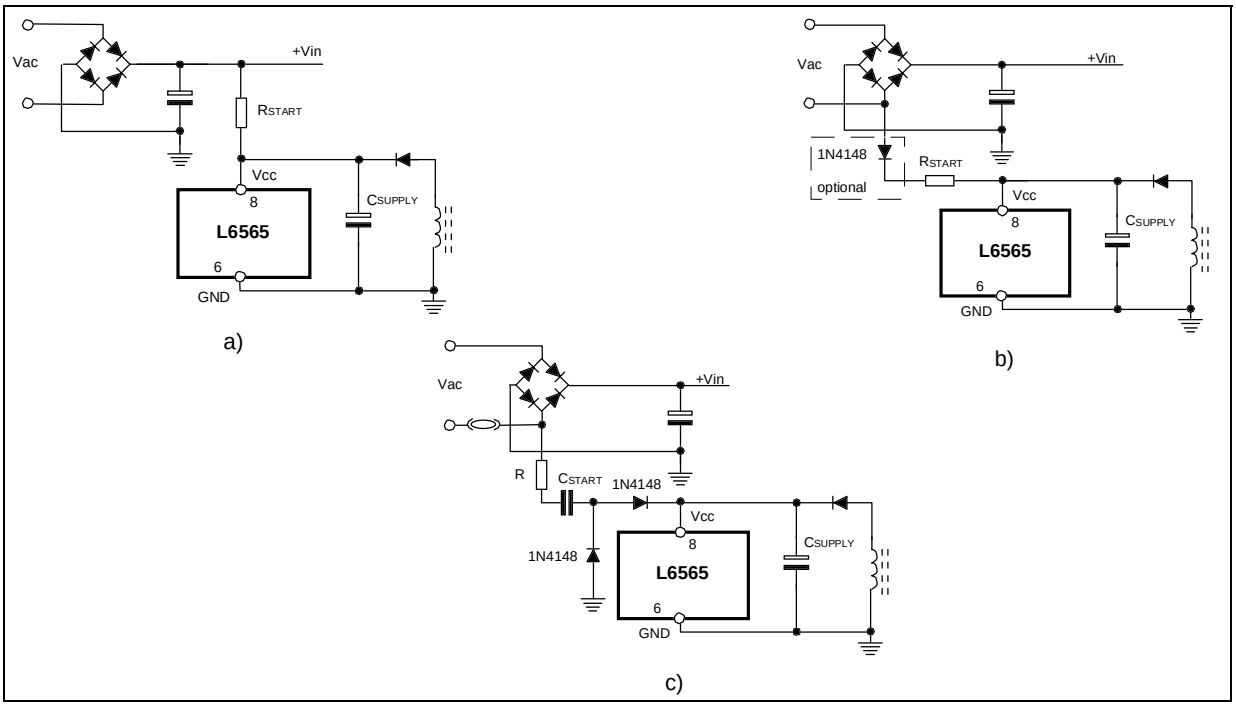


Pin 7 (GD). Gate driver output. It is able to drive an external MOSFET with 400mA source and sink capability. The driver is made up of a totem pole with a low side NDMOS. Its inherent body diode avoids the use of an external diode to prevent excessive negative voltages on the pin due to parasitic ringing.

To avoid undesired switch-on of the external MOSFET, because of some leakage current when the supply of the chip is below the UVLO threshold, an internal pull-down circuit holds the pin low. This circuit guarantees 1 V maximum on the pin (@ I_{sink} = 5mA), with Vcc ≥ 4V. This allows omitting the "bleeder" resistor connected between the gate and the source of the external MOSFET used for this purpose.

Pin 8 (Vcc). IC's supply pin. This pin will be externally connected to the start-up circuit (usually one resistor, R_{START}, connected as shown in figures 20a,b and to the self-supply circuit (aux. winding, diode and C_{SUPPLY}).

Figure 20. Start-up circuit configurations



An additional film capacitor (0.1 or 0.22 µF typically), placed as close the IC's pins as possible, can be used for filtering out the noise due to layout issues.

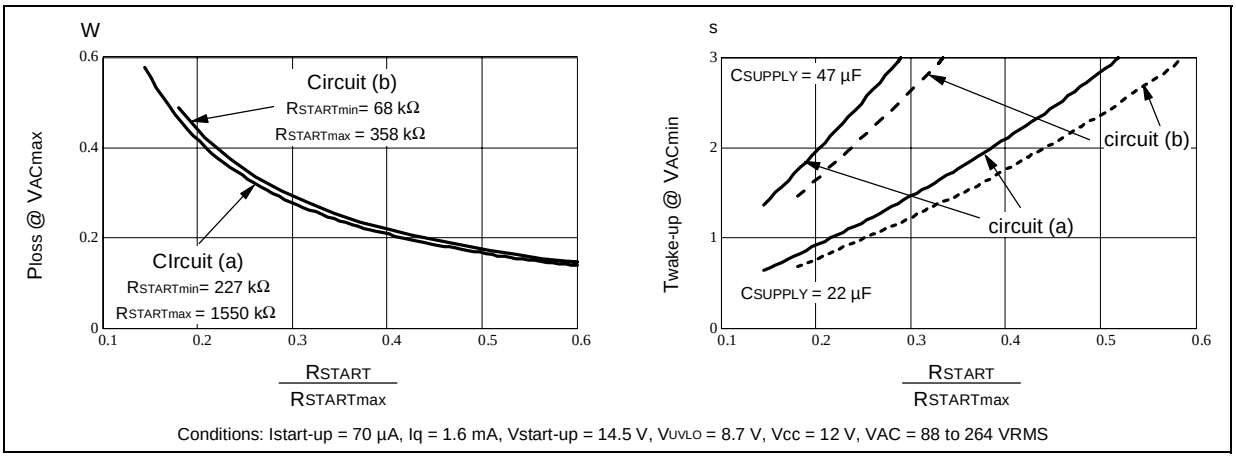
To start the L6565, the V_{cc} voltage must exceed the start-up threshold. Below this value the device is inactive and consumes less than 70µA from the pin, 45µA typically. This allows the use of a high value R_{START} (in the hundreds kΩ), or a charge pump circuit, which reduces power consumption and optimizes system efficiency at light load, especially in wide range mains applications.

In principle, to make sure that the IC can start up even with the minimum line voltage (V_{ACmin}), there is a maximum value for R_{START}. In practice, however, to get an acceptable wake-up time (i.e. the time needed for the V_{cc} voltage to reach the start-up threshold of the IC), R_{START} needs to be quite lower than this limit.

Figure 21 shows the power consumption of the start-up circuits a) and b) at maximum line voltage when the device is running, and the typical wake-up time, that is the time needed for the Vcc voltage to reach the start-up threshold at minimum line voltage, for different values of R_{START} (normalized to its maximum value).

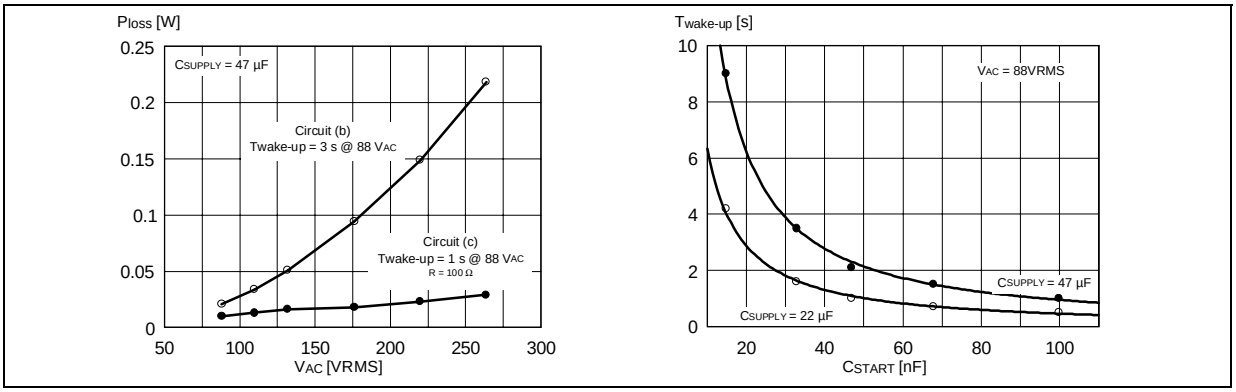
A minimum value for R_{START} (see Fig. 21 - left) is required to allow the IC to restart after the driver has been disabled by a 2nd level OCP intervention (e.g. resulting from a shorted secondary diode). If a resistance lower than this limit is used, at high line the IC might not restart because the current coming from R_{START} exceeds the IC consumption (1.6mA min.) and keeps the V_{cc} voltage above the UVLO threshold. Of course this feature can be used the other way round, to turn the Hiccup-mode behavior of the 2nd OCP threshold into a latched one.

Figure 21. Typical power consumption and wake-up time for the start-up circuits a) and b)



The start-up circuit c) is a small charge pump. It allows faster wake-up times, compared to circuits a) and b), with very low power dissipation. The wake-up time depends on the value of C_{START}, a high-voltage capacitor that can be a low-quality one since it is operated at low frequency and carries very little current. Figure 22 shows the typical wake-up time for different values of C_{START} and the consumption vs. the line voltage. For reference, the consumption of circuit b - but with a much longer wake-up time - is shown too.

Figure 22. Typical power consumption and wake-up time for the start-up circuit of figure 20c



The above-mentioned considerations that lead to a minimum value for R_{START} in circuits a) and b) here put a limit of 85nF to the maximum value of C_{START} (the current delivered by the pump is $\sqrt{2} \cdot V_{AC} \cdot f_L \cdot C_{START}$). The series resistor R limits the charge/discharge peak current of C_{START}. It may range from few units to some kΩ without affecting the wake-up time significantly; however, the dissipation will go up as R increases above some hundred ohms.

When operating, the current consumption (of the device only, not considering the gate drive current) rises to a value not exceeding 3.5mA. The device keeps on working as long as the supply voltage is over the UVLO threshold (10.3V max). If the Vcc voltage exceeds 18V (min.) an internal zener diode, 25mA rated, will be activated in order to clamp the voltage. In that case the consumption of the device will obviously increase.

A PRACTICAL QR ZVS FLYBACK DESIGN WITH THE L6565

As a reference design, a 50 W multioutput QR ZVS flyback converter for a 14" TV SMPS, based on the L6565, will be now presented.

Table 3 summarizes the electrical specification of the application, table 3 provides transformer's spec, and the electrical schematic is shown in figure 23 along with the relevant part values.

Table 3. L6565-based 50W QR SMPS for 14" TV: electrical specification

Input Voltage Range (V_{in})	88 to 264 Vac
Mains Frequency (f_L)	50/60 Hz
Maximum Output Power (P_{out})	51 W
Outputs	V_{out1} = 105 V ± 5% I_{out1}= 0.1 to 0.35 A $V_{ripple1}$ = 1%
	V_{out2} = 14 V ± 10% I_{out2} =0.1 to 1 A $V_{ripple2}$ = 1%
	V_{out3} = 5 V ± 5% I_{out3} = 50 mA $V_{ripple3}$ < 1%
Minimum Switching Frequency in Normal Mode	70 kHz
Target Efficiency (@ P_{out} = 50 W, V_{in} = 88÷264 Vac)	η > 80%
Maximum Input Power in Standby (@ P_{out} = 0.25 W on 5V output, V_{in} = 88÷264 Vac)	< 2 W

The minimum switching frequency (70 kHz @ V_{in} = 90V_{DC}) has been chosen trading off transformer's size against frequency-related losses. The reflected voltage is 140V, thus ZVS is achieved only when the converter is powered by the 110V mains. However, this value seems to provide a good compromise between capacitive and switching losses at 220V mains. An 800V MOSFET is used anyway to provide enough room for the leakage inductance voltage spike, in order to maximize energy transfer during its demagnetization.

The converter is started up with a dropping resistor (R1+R2) that draws current from the AC side of the bridge rectifier. This circuit dissipates only about 240mW @ 264 Vac thanks to the extremely low start-up current of the L6565. The worst-case wake-up time is 2.8s at 88 Vac and 0.7s at 264 Vac.

R3 and R4 compensate for the power capability change vs. the input voltage (Voltage Feedforward). A 1nF film capacitor bypasses any noise on pin #3 to ground.

Output voltage regulation is achieved with secondary feedback, type 1; Vout1 (105V), which must be tightly regulated, is directly under feedback and Vout2 (14V) is in tracking. The 5V output for the µP is linearly post-regulated from the 14V output to get a very clean voltage.

Figure 23. L6565-based 50W QR SMPS for 14" TV: electrical schematic

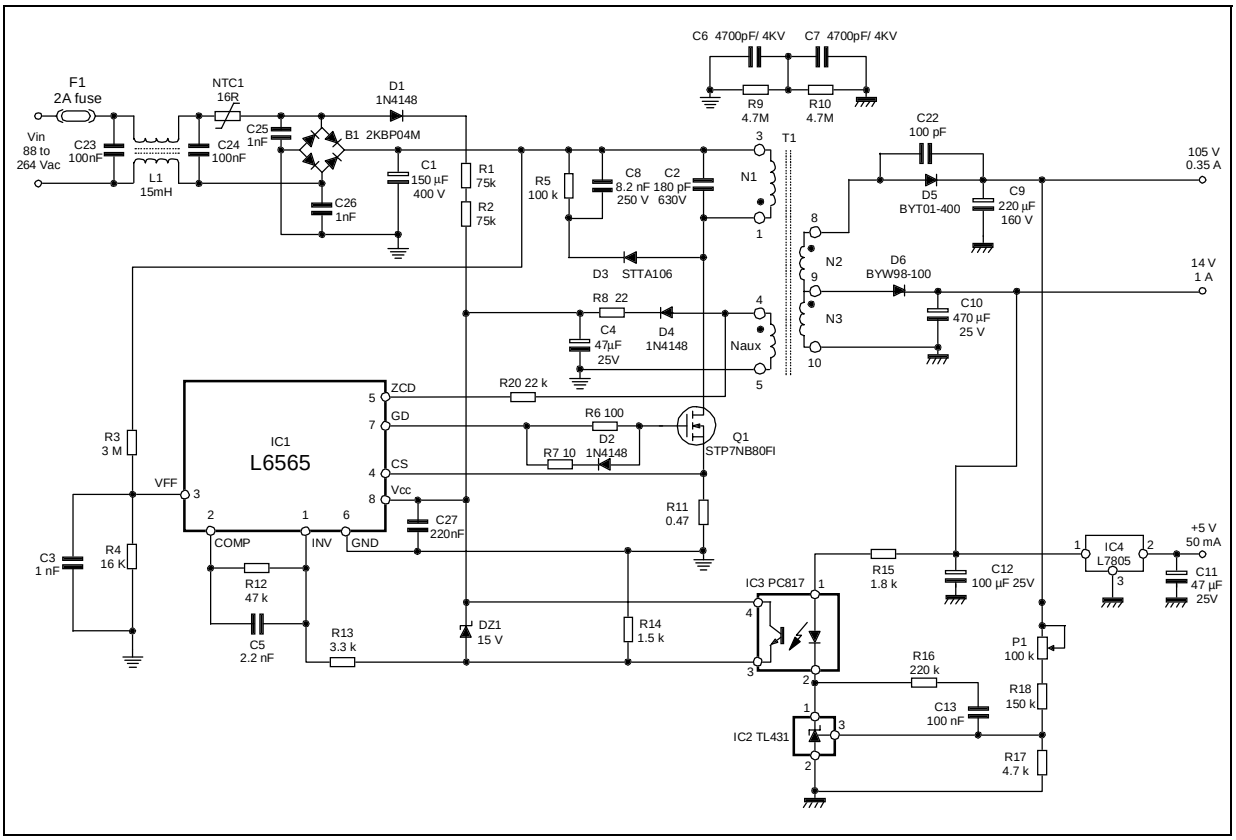


Table 4. L6565-based 50W QR SMPS for 14" TV: transformer specification

Core	ETD29/16/10, N67 Material or 3C85 or equivalent					
Bobbin	Horizontal mounting, 14 pins					
Air gap	≈ 1 mm for an inductance 1-3 of 285 µH					
Leakage inductance	< 8 µH					
Windings Spec & Build	Pin Start/End	Winding	Voltage	Wire	Turns	Notes
	1/2	Pri1	---	2xAWG28	24	
	8/9	Sec1	105	AWG28	31	
	9/10	Sec2	14	AWG28	5	
	2/3	Pri2	---	2xAWG28	24	
	4/5	Aux	14	AWG32	5	Evenly spaced

A protection against output overvoltages (OVP) due to the optocoupler's failure is realized with the zener diode DZ1. In case of failure the output voltage will not be out of control: the system will work with a primary voltage sensing feedback that regulates the outputs 10-15% higher than the nominal value.

A 180pF polypropylene capacitor has been added across the primary winding to optimize MOSFET's losses by a small snubbing effect on the drain voltage rate of rise.

The delay between transformer' s demagnetization and MOSFET's turn-on is adjusted by means of R20. The

final value of 22kΩ has been experimentally determined so as to achieve the optimum turn-on point after the addition of C2. Changing the value of C2 requires a different value of R20.

The following tables summarize some significant evaluation data of the prototype and the oscilloscope pictures show some significant waveforms under different operating conditions.

Table 5. L6565-based 50W QR SMPS for 14" TV: Full load measurements

V_{AC} [V]	88	110	132	176	220	264
P_{in} [W]	61.7	60.4	59.0	58.7	59.7	61.2
Vout [V]	105.0	105.0	105.0	105.0	105.1	105.1
	13.74	13.76	13.77	13.77	13.78	13.78
	4.995	4.995	4.995	4.995	4.995	4.995
P_{out} [W]	50.74	50.76	50.77	50.77	50.78	50.78
η [%]	82.2	84.0	86.0	86.5	85.1	83.0
Load conditions: 105V: 350mA; 14V: 1A; 5V: 50mA						

Table 6. L6565-based 50W QR SMPS for 14" TV: consumption from the mains in Standby

V_{AC} [V]	88	110	132	176	220	264
P_{in} [W]	1.17	1.20	1.24	1.37	1.45	1.60
Load conditions: 105V and 14V open; 5V: 50mA						

Table 7. L6565-based 50W QR SMPS for 14" TV: power capability

V_{AC} [V]	88	110	132	176	220	264
P_{inlim} [W]	86	92	96	98	95	90

Figure 24. Drain Voltage and Primary Current: Full load, V_{in} = 100 VDC (left), V_{in} = 380 VDC (right)

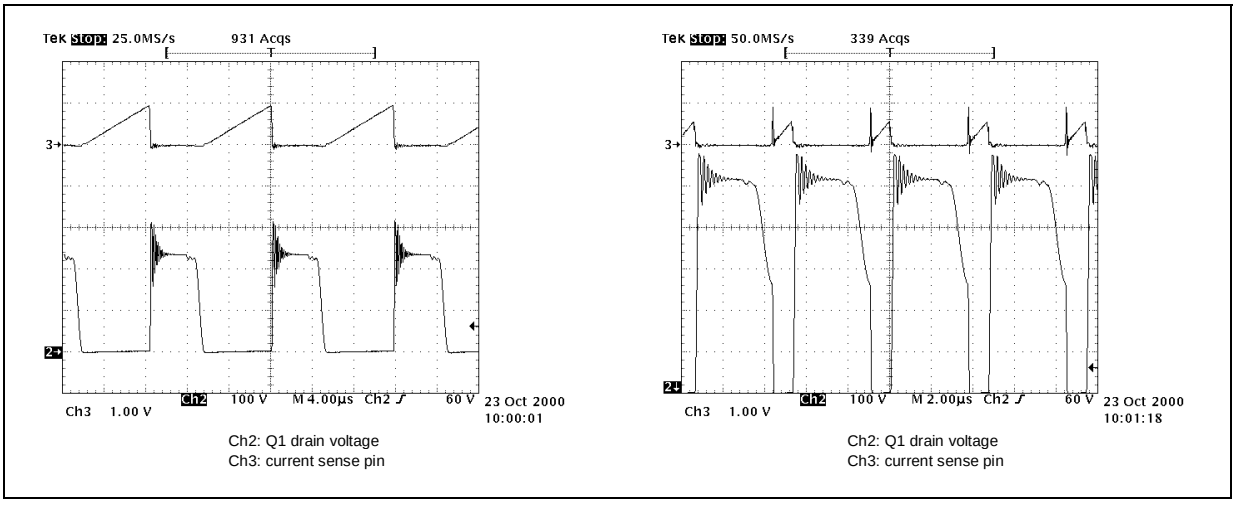
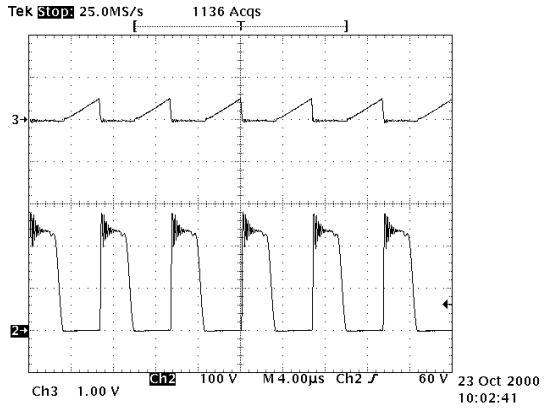
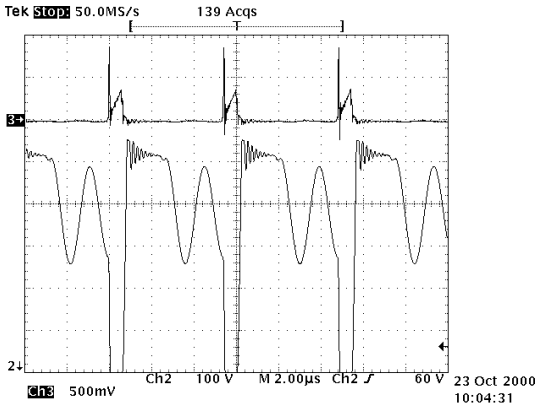


Figure 25. Drain Voltage and Primary Current: half load, V_{in} = 100 VDC (left), V_{in} = 380 VDC (right)

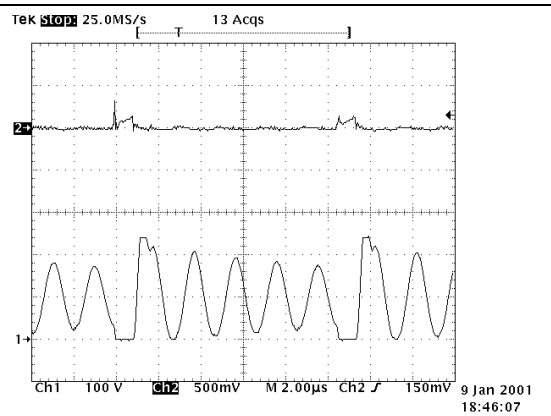


Ch2: Q1 drain voltage
Ch3: current sense pin

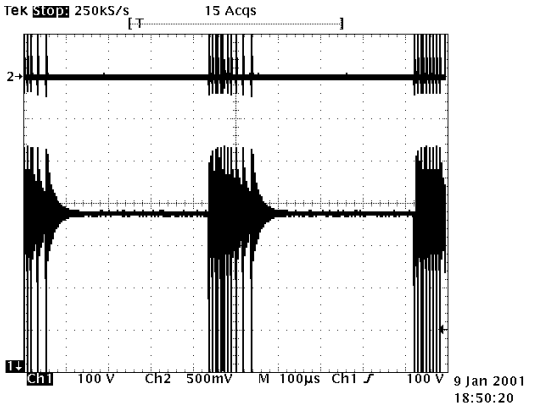


Ch2: Q1 drain voltage
Ch3: current sense pin

Figure 26. Drain Voltage and Primary Current: Standby, V_{in} = 100 VDC (left), V_{in} = 380 VDC (right)

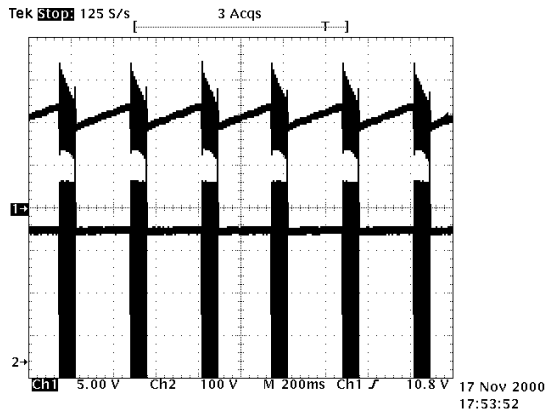


Ch1: Q1 drain voltage
Ch2: current sense pin

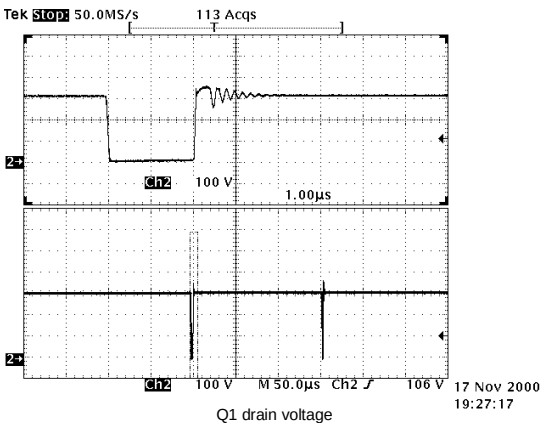


Ch1: Q1 drain voltage
Ch2: current sense pin

Figure 27. Short circuit on 105V output, V_{in} = 300 VDC: system running at the starter frequency

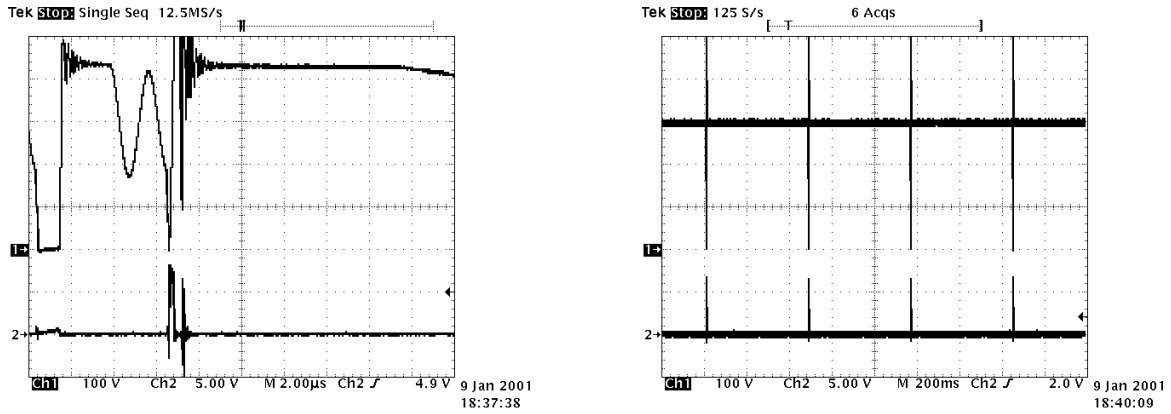


Ch1: Vcc (pin 8) voltage
Ch2: Q1 drain voltage



Q1 drain voltage
Lower screen: detail of a burst
Upper screen: detail of a single cycle

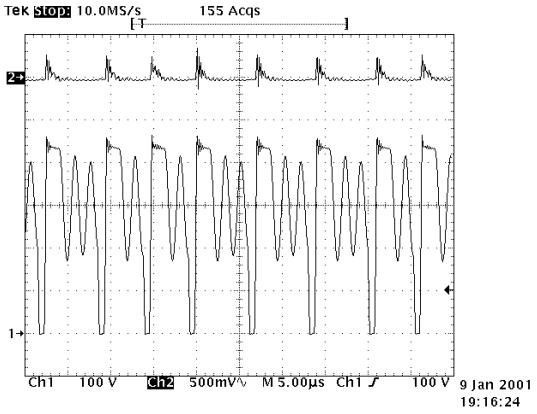
Figure 28. Short circuit of the output diode D5: detail of turn-on (left), Hiccup-mode operation (right).



Ch1: Q1 drain voltage
Ch2:current sense pin

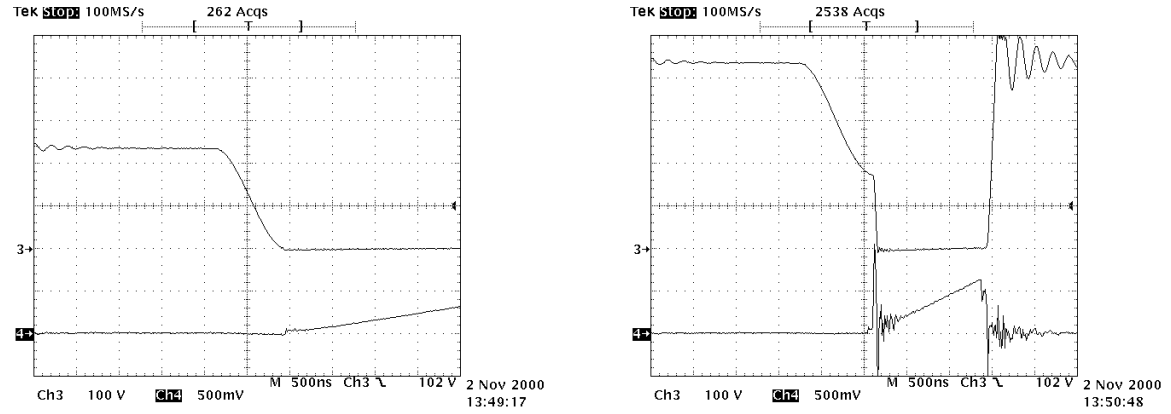
Ch1: Q1 drain voltage
Ch2:current sense pin

Figure 29. Uneven ringing cycle skipping during frequency foldback



Ch1: Q1 drain voltage
Ch2: 105 V output

Figure 30. Details of MOSFET turn-on; V_{in} = 100 V_{DC} (left) - ZVS, V_{in} = 300 V_{DC} (right) - no ZVS



Ch3: Q1 drain voltage
Ch4: current sense pin

Ch3: Q1 drain voltage
Ch4: current sense pin

CONCLUSIONS

After showing how it is possible to obtain a QR ZVS flyback converter suitable for offline applications from a standard fixed-frequency flyback converter, the many benefits and the few drawbacks resulting from this approach have been highlighted.

The equations governing the operation of such class of converters have been derived for design purposes and some details have been considered, resulting in some clues on their design. Details on how the L6565 and the functions it embeds are to be used are given. In particular, the Frequency Foldback and the Line Feedforward functions have been discussed.

A detailed pin-by-pin description of the IC has been provided, with some hints on pin usage. Finally, as an example, a 50W multioutput QR ZVS flyback converter for 14" TV SMPS, along with bench evaluation results and the most significant waveforms, has been presented.

REFERENCES

[1] "L6561-based Flyback Converters" (AN1060)

[2] "How to handle Short Circuit Conditions with ST's Advanced PWM Controllers" (AN1215)

[3] Y. Panov, M. Jovanovic, "Adaptive Off-Time Control For Variable-Frequency, Soft-Switched Flyback Converter At Light Loads", PESC 99. 30th Annual IEEE (1999 Volume 1)

[4] L. H. Dixon, Jr., "Filter Inductor and Flyback Transformer Design for Switching Power Supplies", Unitrode Switching Regulated Power Supply Design Seminar Manual, SEM-1000, 1994

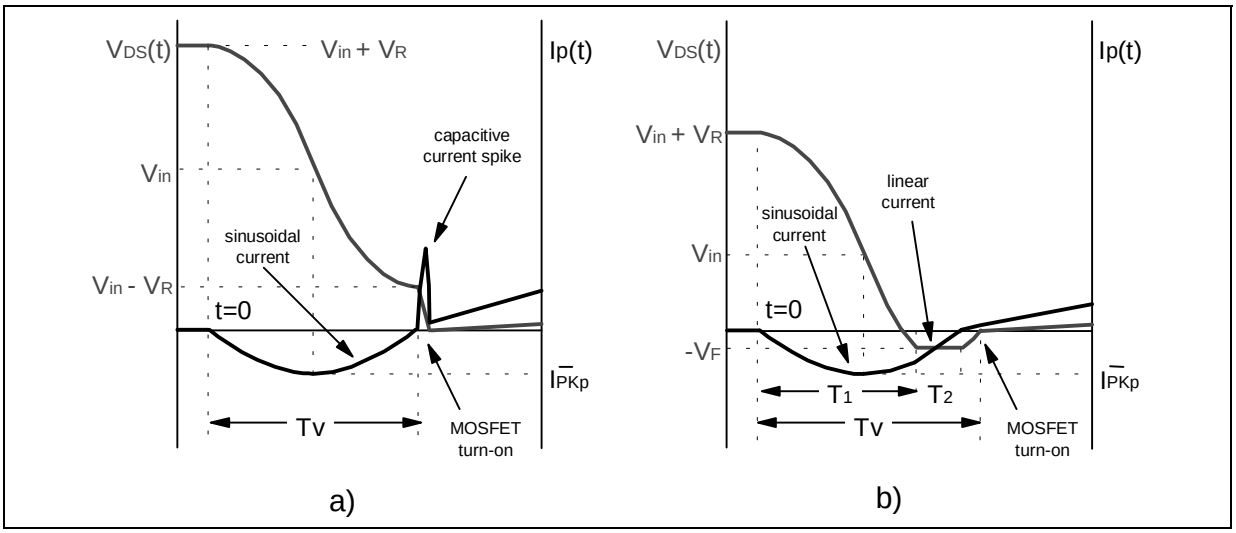
[5] J. Chen, R. Erickson, D. Maksimovic, "Averaged Switch Modeling of Boundary Conduction Mode DC-to-DC Converters", IECON '01. 27th Annual IEEE (2001 Volume 2)

APPENDIX

QR operation: MOSFET's turn-on

As can be noted in the detailed waveforms of figure 31, the primary current becomes negative during the dead time Tv. It is a portion of sinusoid since it is related to a resonance. This is due to the drain capacitance that is discharging, thus current comes out of the MOSFET's drain and charges the primary inductor L_p.

Figure 31. Details of MOSFET's turn-on in case of: (a) $V_{in} > V_R$, no ZVS, (b) $V_{in} < V_R$, ZVS



This being a reactive current, the associated power dissipation inside the MOSFET is ideally zero, negligible in practice. Some power is dissipated in the equivalent resistance of the primary winding, like in a standard flyback converter operated in DCM.

If the ZVS condition (5) is not satisfied, the residual drain voltage generates a current spike at MOSFET's turn-on (see figure 31a) due to the sudden discharge of C_d through MOSFET's $R_{ds(ON)}$. There is an associated loss that can be expressed as follows:

$$P_{cap} = \left[\frac{5}{6}\cdot C_{oss}\cdot (V_{in}-V_R)^{\frac{3}{2}} + \frac{1}{2}\cdot C_d\cdot (V_{in}-V_R)^2\right]\cdot f_{sw}, \quad (A1)$$

where C_{oss} is the MOSFET's drain-to-source capacitance specified at V_{DS} = 25V. The above formula takes the non-linear nature of C_{oss} into account ant assumes that the remaining part of C_d is linear.

When the ZVS condition is met, the loss quantified by equation A1 is zero but a power loss will be generated in the MOSFET if its body diode is injected. In order for that to happen, it is sufficient that the reflected voltage exceeds the input voltage by one diode drop (assume typically 1 V).

Figure 31b shows the situation in details. At the time T_1 the drain voltage reaches $-V_F$ and is clamped by the MOSFET's body diode. Then the current turns from sinusoidal to linear. It takes a time T_2 for the current to go to zero and the power dissipation occurs during this time. To simplify, C_{oss} modulation is ignored and V_F is neglected with respect to V_{in}. With these approximations, the estimated power loss will be:

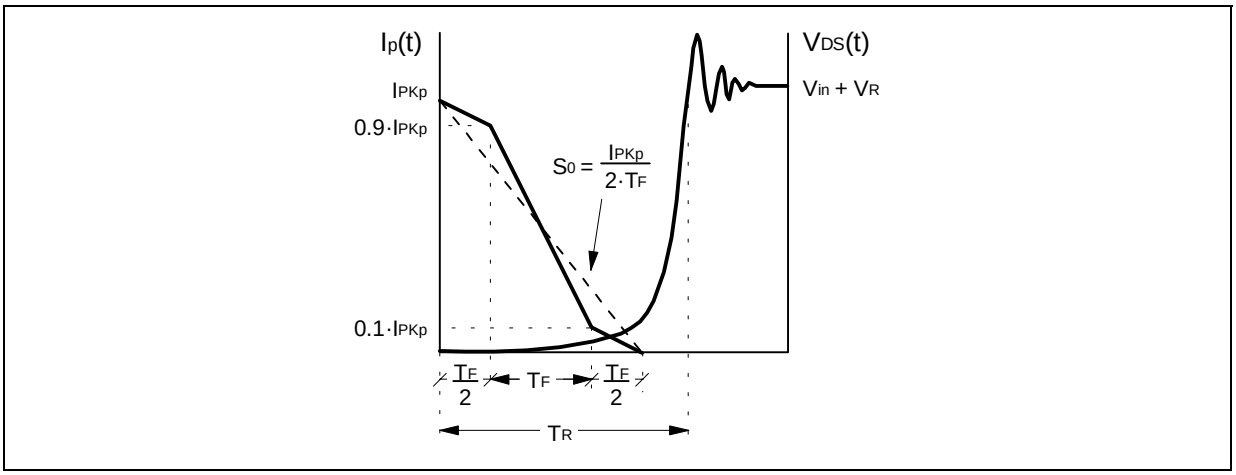
$$P_{diode} = V_F\cdot I_{DCdiode} = \frac{1}{2}\cdot V_F\cdot\frac{V_R^2 - V_{in}^2}{V_{in}}\cdot C_d\cdot f_{sw}$$

This dissipation usually amounts at some ten mW at minimum input voltage, which is the worst case. As a result, there is no point in complicating the control to turn-on the MOSFET exactly when the drain voltage crosses zero to avoid body diode injection. A fixed dead-time T_v is the optimum solution in most cases.

QR operation: MOSFET's turn-off

When the MOSFET is driven off, the drain current starts to decrease with a certain slope from its peak value I_{PKp}. The transformer's primary inductance acts almost as a current source, thus this current decrease is mirrored by a current increase through C_d. The drain voltage will rise until it reaches $V_{in} + V_R$, after that L_p becomes coupled with L_s and the voltage across L_m will be fixed at $V_{in} + V_R$. The drain voltage will increase further on because the leakage inductance L_{lk} is still charged with a current almost equal to I_{PKp} and has to be demagnetized. When L_{lk} has run dry the drain voltage will settle down to $V_{in} + V_R$ after some oscillations.

Figure 32. Details of MOSFET's turn-off: linear approximation of current falling edge.



With the approximation sketched in figure 32, the drain voltage evolution will be described by a sinusoid that, in

almost all practical cases, can be approximated by a parabola:

$$V_{DS}(t) = \frac{I_{PKp}}{4 \cdot T_F \cdot C_d} \cdot t^2$$

with a small error. T_F is the current fall time (defined as the time needed to the current to fall from 90% to 10% of its initial value) that can be deduced from the MOSFET's electrical specification.

The time T_R needed to the drain voltage to reach the level $V_{in} + V_R$, when the leakage inductance begins its demagnetization (practically, the drain voltage rise time), will be:

$$T_R = 2 \cdot \sqrt{\frac{T_F \cdot C_d \cdot (V_{in} + V_R)}{I_{PKp}}}$$

If C_d is such that $T_R > 2 \cdot T_F$, that is if:

$$C_d > \frac{T_F \cdot I_{PKp}}{V_{in} + V_R} \ ,$$

then the turn-off losses in the MOSFET will be given by:

$$P_{sw} = \frac{(T_F \cdot I_{PKp})^2}{6 \cdot C_d} \cdot f_{sw} \ . \quad \text{(A2)}$$

By inspection of (A1) and (A2) it is possible to see that there is an optimum value of C_d that minimizes MOSFET's total switching losses $P_{cap} + P_{sw}$. With some easy calculation it is possible to find:

$$C_{dopt} = \frac{1}{\sqrt{3}} \cdot \frac{T_F \cdot I_{PKp}}{V_{in} - V_R}$$

Usually, an external capacitor should be added to get such capacitance value.

However, this optimization is valid only under specific operating conditions, in terms of input voltage and load current. For example, optimizing losses for full load conditions will inevitably lead to higher losses at light load. This should be kept in mind when deciding whether to use or not the capacitor.

Another consideration could be that the addition of such capacitor could allow the designer to save the RCD (or zener) clamp for the leakage inductance spike. To be able to do this, the total drain capacitance has to meet the condition:

$$C_d > \frac{I_{PKp}^2 \cdot L_{lk}}{[V_{(BR)DSS} - V_{in} - V_R]^2} \quad \text{(A3)},$$

where $V_{(BR)DSS}$ is the breakdown voltage of the MOSFET. This condition should be evaluated under the worst-case conditions that are with the short circuit peak primary current and at the input voltage where the right side of (A3) reaches the maximum, which generally occurs at $V_{in} = V_{inmax}$.

Anyway, if used, it is advantageous to connect the external capacitor across the primary winding of the transformer: in this case its voltage rating needs to be greater than V_{inmax}, whereas it should be rated at least for $V_{inmax+}V_R$ if connected across the MOSFET. The effect on f_r and the drain voltage rise time will be the same.

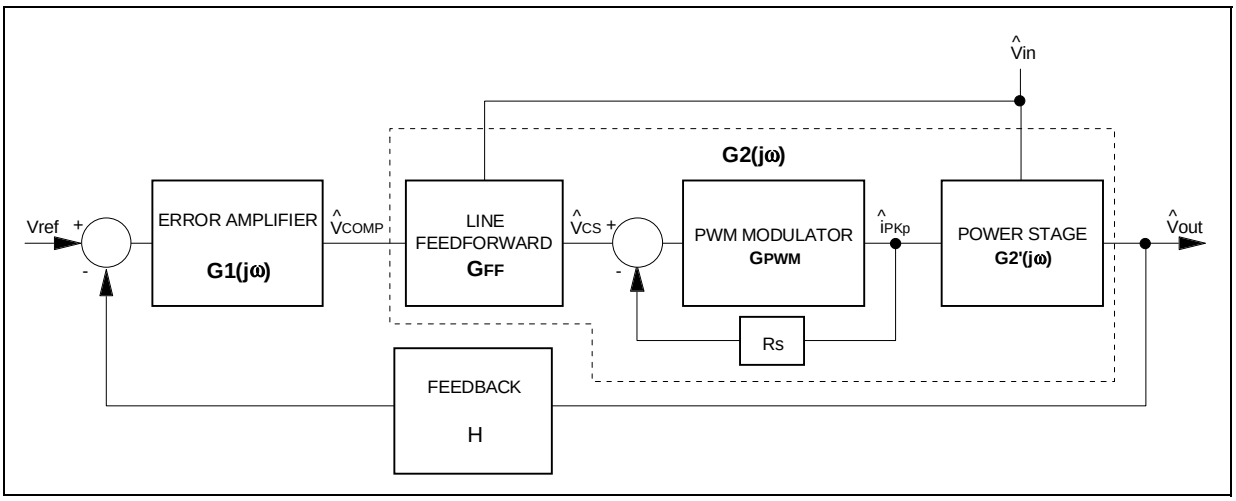
Small signal model of QR ZVS flyback and design of the feedback loop compensation

The control loop can be summarized as shown in figure 33, where each block is described by its transfer function in the complex frequency domain and represented by means of a Bode plot. The set PWM modulator + Power stage + Line Feedforward block is what, in control theory terminology, is called the "plant", while the compensated error amplifier is the "controller".

The task of the control loop design is to determine the transfer function G1(jω) of the error amplifier and define the relevant frequency compensation network. The objective of the design is to ensure that the resulting closed-

loop system will be stable and well performing in terms of regulation and dynamic response.

Figure 33. Control loop Block Diagram of an L6565-based QR ZVS flyback



To do so, it is necessary to determine first the transfer function of the plant G2(jω), in order to select an appropriate structure for G1(jω). The transfer function of the plant is defined by the control method (peak current mode), the topology of the converter (flyback) and its operating mode. For the sake of simplicity the operating mode will be considered an exact TM (transition Mode), neglecting the time Tv needed to achieve ZVS. An exact analysis considering also the dead time, besides being much heavier from the calculation point of view, would show that the difference is practically negligible at least at medium-heavy load.

G2(jω) can be factorized as the product of the gain of the Line Feedforward block (G_{FF}), the PWM modulator gain (G_{PWM}) and the power stage transfer function G2'(jω):

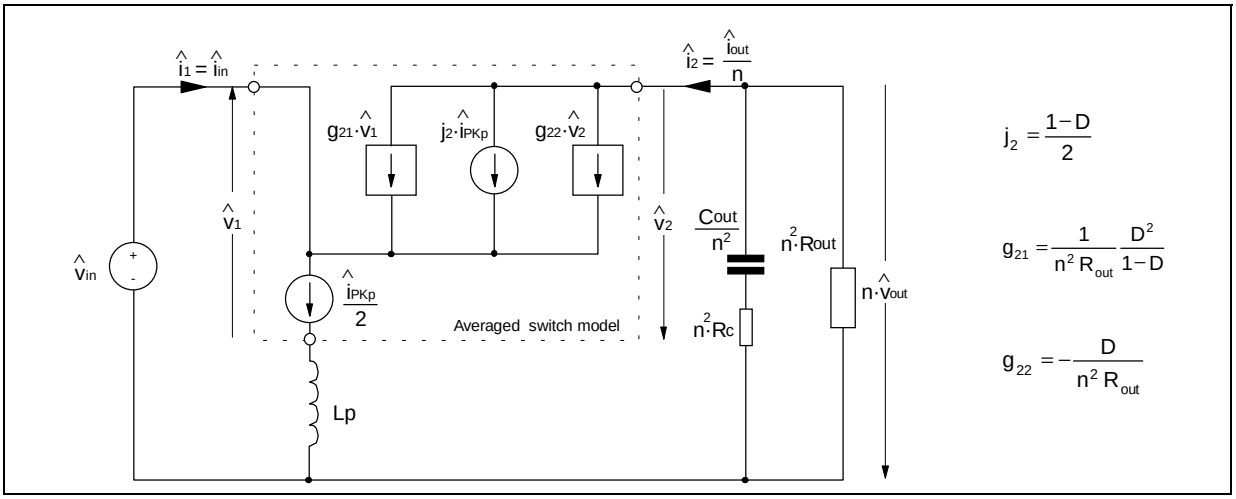
$$G2(j\omega) = G_{FF} \cdot G_{PWM} \cdot G2'(j\omega).$$

The expression of G_{FF} is given in (21a), while that of G_{PWM} is simply:

$$G_{PWM} = \frac{\hat{i}_{PKp}}{\hat{v}_{cs}} = \frac{1}{Rs}$$

As to the power stage, an analysis with the averaged switch model approach [5] leads to the small-signal model illustrated in figure 34.The resulting control-to-output transfer function G2'(jω) is:

Figure 34. Small-signal model of the QR ZVS power stage



$$G2'(j\omega) = \frac{\hat{v}_{out}}{\hat{i}_{PKp}} = \frac{n}{2}R_{out}\frac{1-D}{1+D}\frac{(1+j\omega R_c C_{out})\left(1-j\omega\frac{L_p}{n^2 R_{out}}\frac{D}{(1-D)^2}\right)}{1+j\omega\frac{R_{out}C_{out}}{1+D}}$$

which looks very much like the low-frequency approximation of the control-to-output transfer function of CCM flyback:

- the DC gain of the control-to-output transfer function is exactly half that of a CCM system;
- there is a low-frequency shifting pole exactly equal to that of a CCM system;
- the gain-bandwidth product is a function of the input-to-output voltage ratio only, like in CCM systems.
- there is a shifting RHP zero with the same expression as in a CCM system, but actually located at a higher frequency because of the smaller inductance; it is possible to show that:

$$f_{RHP} = \frac{1}{\pi D}f_{sw},$$

which is well above usual targets of the open-loop crossover frequency and therefore will be neglected for loop design purposes. If the crossover frequency is selected higher than $0.1f_{RHP}$ there will be some phase margin erosion that can be accounted for at design time.

Finally, the control-to-output transfer function G2(jω) will be:

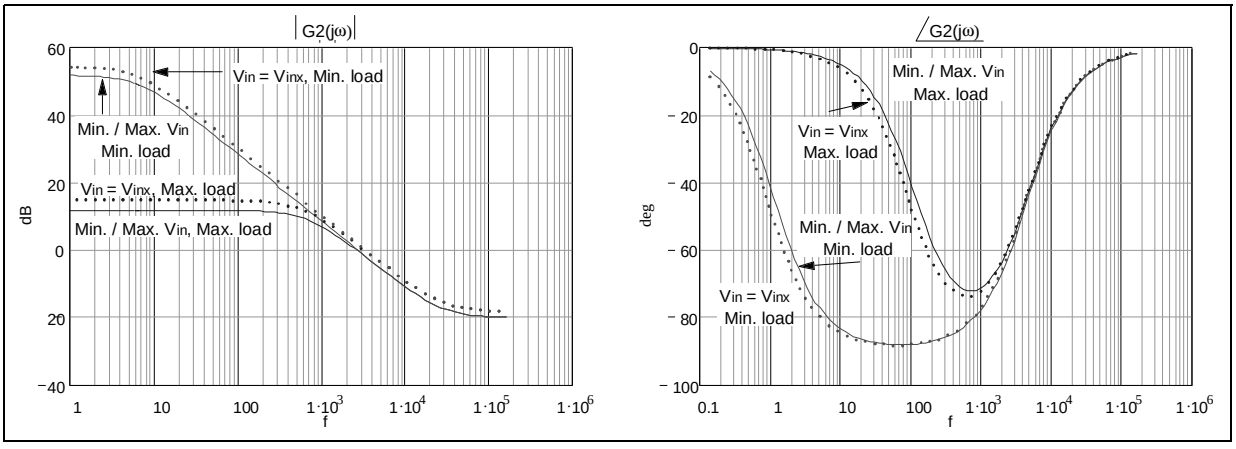
$$G2(j\omega) = \frac{\hat{v}_{out}}{\hat{v}_{COMP}} = \frac{n}{14}\frac{R_{out}}{Rs}(3-k_{opt}V_{in})\frac{1-D}{1+D}\frac{(1+j\omega R_c C_{out})}{1+j\omega\frac{R_{out}C_{out}}{1+D}},$$

being 0.14/2 = 0.07 ≅ 1/14.

It is worthwhile noticing that the Line Feedforward block affects the dependence of the control-to-output DC gain on the input voltage. Moreover, it is possible to prove also that it reduces the variation of the gain-bandwidth product of G2(jω) versus the input voltage exactly the same way it compensates converter's power capability. In case of optimum compensation, this means that it assumes the same values at the extremes values of Vin and reaches a maximum, 20% higher, for $V_{in} = V_{inx}$ given by (20). This is shown in figure 35 for the converter example considered in the text.

Although the crossover frequency of G2(jω) is maximum for $V_{in} = V_{inx}$ its increase is relatively small, then for design purposes it is still better to consider the condition $V_{in}=V_{inmin}$ where the RHP zero frequency is minimum and its effects are maximum.

Figure 35. Typical Bode plots of G2(jω) under different operating conditions



It is interesting to consider the audio susceptibility as well, that is the line-to-output transfer function, and see the effect of the Line feedforward block. The line-to-output transfer function of the power stage only, that is with the VFF pin grounded or kept at a fixed voltage, is:

$$\frac{\hat{v}_{out}}{\hat{v}_{in}} = \frac{1}{n}\frac{D^2}{1-D^2}\frac{1+j\omega R_c C_{out}}{1+j\omega\frac{R_{out}C_{out}}{1+D}}.$$

The gain of the voltage feedforward block with respect to the input voltage changes, G'_{FF}, is given by (21b). With reference to the small-signal model of figure 34, this means that the current generator $\frac{1}{2}\hat{i}_{PKp}$ is no longer independent (and cannot be opened) but is a function of $\hat{v}_{in}$. The resulting expression is:

$$\frac{\hat{v}_{out}}{\hat{v}_{in}} = \frac{1}{n}\frac{D^2}{1-D^2}\left(1-\frac{\alpha}{D}\right)\frac{(1+j\omega R_c C_{out})\left(1+j\omega\frac{L_p}{n^2 R_{out}}\frac{D}{(1-D)^2}\frac{\alpha}{D-\alpha}\right)}{1+j\omega\frac{R_{out}C_{out}}{1+D}}$$

where:

$$\alpha = \frac{k_{opt}V_{in}}{3-k_{opt}V_{in}}$$

The Line Feedforward then modifies the DC gain with an additional factor and adds a shifting zero. A simple inspection shows that the DC gain is positive for $\alpha<D$, negative for $\alpha>D$ and zero for $\alpha=D$, and that, at the same time, the additional zero disappears for $\alpha=D$, is an LHP zero for $\alpha<D$, an RHP zero for $\alpha>D$. It is possible to prove that α equals D (which nulls the DC gain and the zero location) for $V_{in} = V_{inx}$ given by (20).

Figure 36. Open-loop audio susceptibility: a) DC gain; b) 100 Hz gain

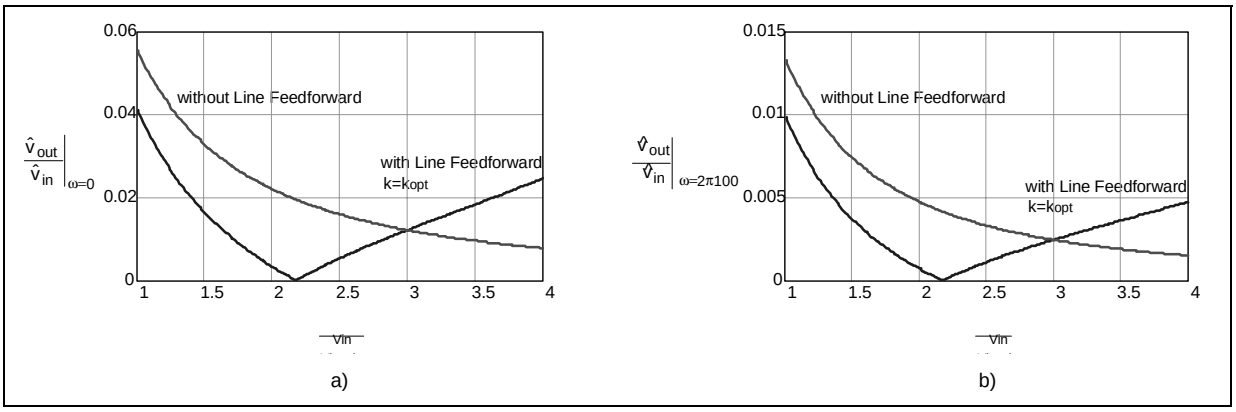
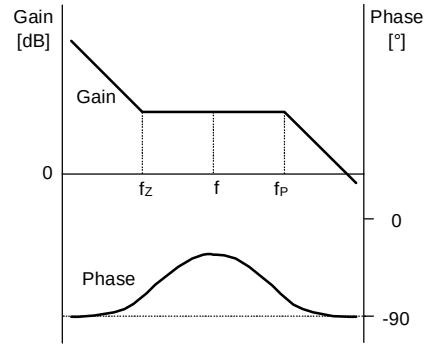


Figure 36 shows how the overall audio susceptibility @DC and @100 Hz change over the input voltage range, compared against the gain that would result with k=0, that is without Line Feedforward. It is possible to notice that in the lower input voltage range, that is for V_{in} a up to about $3 \cdot V_{inmin}$, the Line Feedforward reduces audio susceptibility, which results in a lower line-frequency ripple on the output. At high line the audio susceptibility is worse but this occurs where the input voltage ripple is low.

This kind of plant will be stabilized in closed-loop operation by what is commonly known as a Type 2 amplifier. Its transfer function G1(jω), which comprises a pole at the origin and a zero-pole pair, is defined as shown in fig. 37, where also its asymptotic Bode plot is illustrated.

Figure 37. Type 2 amplifier transfer function (Bode diagram and analytical expression)



$$G1(j\omega) = \frac{G1_0}{j\omega}\frac{1+\frac{j\omega}{\omega_Z}}{1+\frac{j\omega}{\omega_P}}$$

The main task of this correction is to reduce the phase lag of G2(jω) in the neighborhood of the crossover frequency. As usual, the target is specified in terms of desired crossover frequency (f_c, with $f_c < f_{swmin}/5$) and desired phase margin (Φ_m, with $\Phi_m > 45°$) of the global open loop gain.

The synthesis of G1(jω) can be done with the following step-by-step procedure:

a) Calculate the equivalent output resistance relevant to the full load output power P_{outmax}, $R_{out} = V^2_{out}/P_{outmax}$, the duty cycle D corresponding to $V_{in} = V_{inmin}$ and evaluate f_{RHP}. If f_c is greater than $0.1f_{RHP}$ define the quantity Φ_{m1} as:

$$\Phi_{m1} = 45\left(1 + Log\frac{f_c}{f_{RHP}}\right)$$

otherwise consider $\Phi_{m1} = 0$.

b) Calculate gain and phase of G2(jω) at the desired crossover frequency fc. That is:

$$G2_c = \left|G2(2\pi f_c)\right|,$$

$$\Phi 2_c = \frac{180}{\pi}\arg[G2(2\pi f_c)];$$

c) Calculate gain and phase of G1(jω) at $f = f_c$ in order for the overall open-loop gain to cross the 0 dB axis at $f = f_c$ with the phase margin Φ_m:

$$G1_c = \left|G1(2\pi f_c)\right| = \frac{1}{G2_c},$$

$$\Phi 1_c = \frac{180}{\pi}\arg[G1(2\pi f_c)] = -180 + (\Phi_m + \Phi_{m1}) - \Phi 2_c$$

d) Cancel the pole of G2(jω) by placing the zero of G1(jω) in the neighborhood:

$$f_Z = \frac{\omega_Z}{2\pi} = \frac{\alpha}{2\pi}\frac{1+D}{R_{out}C_{out}} \qquad \text{(tipically, } \alpha = 0.5 \text{ to } 5);$$

e) Place the pole of G1(jω) so as to get the desired phase margin:

$$f_P = \frac{\omega_P}{2\pi} \approx \frac{f_c}{\left|\tan\left(\frac{\pi}{180}\Phi 1_c\right)\right|};$$

f) Calculate the unity gain frequency $G1_0$:

$$G1_0 \approx 2\pi G1_c\frac{f_c f_Z}{f_P}.$$

The synthesis of G1(jω) is completed. Its practical implementation can be realized with the circuit of figure 14. Its transfer function is:

$$G1(j\omega) = \frac{\hat{v}_{COMP}}{\hat{v}_{out}} = \frac{\hat{v}_{COMP}}{\hat{i}_{COMP}}\frac{\hat{i}_{COMP}}{\hat{i}_F}\frac{\hat{i}_F}{\hat{v}_k}\frac{\hat{v}_k}{\hat{v}_{out}} = \frac{CTR_{max}R_{COMP}}{RB\ RH\ CF}\frac{1}{j\omega}\frac{1+j\omega(RH+RF)CF}{1+j\omega R_{COMP}C_{COMP}}, \quad (A4)$$

where CTR is optocoupler's Current Transfer Ratio. Table 8 gives the design relationships useful to derive the part values. $I_{COMPmax}$ is specified in the datasheet (5mA).

Table 8. G1(jω) implementation: part values of figure 14 schematic

Symbol	Definition
RL	Usually between 500Ω and 5 kΩ
RH	$RL\frac{V_{out}-V_{REF}}{V_{REF}}$ (the TL431 reference voltage V_{REF} is typically 2.5V)
RB	Less than $CTR_{min}\frac{V_{out}-3.5}{I_{COMPmax}}$ (assuming 1V drop across the opto's LED)
CF	$\frac{CTR_{max}R_{COMP}}{RB\ RH\ G1_0}$
RF	$\frac{1}{2\pi f_Z CF} - RH$
C_{COMP}	$\frac{1}{2\pi f_P R_{COMP}}$

The following condition should be met:

$$\frac{CTR_{max}}{CTR_{min}} \le G1_c\frac{\left|\tan\left(\frac{\pi}{180}\Phi 1_c\right)\right|}{R_{COMP}}\frac{V_{out}-3.5}{I_{COMPmax}} \quad (A5)$$

otherwise the resulting value for RF will be negative. This usually happens when the there is too high gain. If so, RB should be increased (within its limit) or an optocoupler with a narrower CTR_{min} - CTR_{max} spread should be selected.

It is also possible to reduce the gain by connecting a resistor RX in parallel to C_{COMP}. In fact, this resistor comes dynamically in parallel to R_{COMP}, thus reducing the equivalent value appearing at the numerator of the gain (A4). Equivalently, the denominator of the right-hand side of (A5) is reduced and the limit is increased. Moreover, since RX diverts part of the current sourced by the pin COMP, the opto coupler carries less current and a slightly higher bias resistor RB can be used, thus giving some extra gain reduction (in other words, the quantity $I_{COMPmax}$ in (A5) is reduced). Remember that, if the current flowing through the opto's LED and the TL431 is allowed to go below 1mA, an additional resistor should be connected form the output voltage rail to the cathode of the TL431 to guarantee sufficient bias to the TL431 itself.

To be able to exploit the full dynamics of the error amplifier under worst case conditions, RX should not be less than 4kΩ, which anyway reduces the gain by a factor 4.75 not considering the possible increase of RB.

If none of the above is possible, either a higher f_c or a lower Φ_m should be selected and the calculations from step a) to step f) redone.

Finally, it is worth reminding that this design procedure gives just first cut values that should be checked and adjusted after bench tests. In particular, it is recommended to measure the actual loop gain G2(jω) and not rely only upon the analytical model with its approximations, and the feedback network should be designed on the basis of the measured values of $G2_c$ and $\Phi 2_c$ rather than the computed values.