U_HDMI
HDMI.SchDoc

U_Ethernet
Ethernet.SchDoc

U_LED_SW_BUT
LED_SW_BUT.SchDoc

U_SYS_MAX10_CTRL
SYS_MAX10_CTRL.SchDoc

U_SOUND
SOUND.SchDoc

U_B13
B13.SchDoc

U_B14
B14.SchDoc

U_B15
B15.SchDoc

U_B16
B16.SchDoc

U_B34
B34.SchDoc

U_FPGA-CFG
FPGA-CFG.SchDoc

U_FPGA-MGT
FPGA-MGT.SchDoc

U_FPGA-PWR
FPGA-PWR.SchDoc

U_JOY
JOY.SchDoc

U_KEYBOARD
KEYBOARD.SchDoc

U_POWER
POWER.SchDoc

U_PowerMain
PowerMain.SchDoc

U_VGA
VGA.SchDoc

U_EXT_HEADER
EXT_HEADER.SchDoc

U_EXP_Slot
EXP_Slot.SchDoc

U_Floppy
Floppy.SchDoc

PM1 FIDU-DOT - small
PM2 FIDU-DOT - small
PM3 FIDU-DOT - small
PM4 FIDU-DOT - small
PM5 FIDU-DOT - small
PM6 FIDU-DOT - small

Serial1
Serial
Serialnumber 6,3 x 6.3mm

LOGO1
TE Logo PRINT Layer
LOGO PRINT

GND Mount.Hole 3.2mm
GND Mount.Hole 3.2mm
GND Mount.Hole 3.2mm
GND Mount.Hole 3.2mm
GND Mount.Hole 3.2mm
GND Mount.Hole 3.2mm

Design drawn by:	IG
Checked by:	MR
Assembly variant:	[No Variations]
Created by:	VariantCreatedBy
Modified by:	VariantModifiedBy
Modified at:	VariantDateModification

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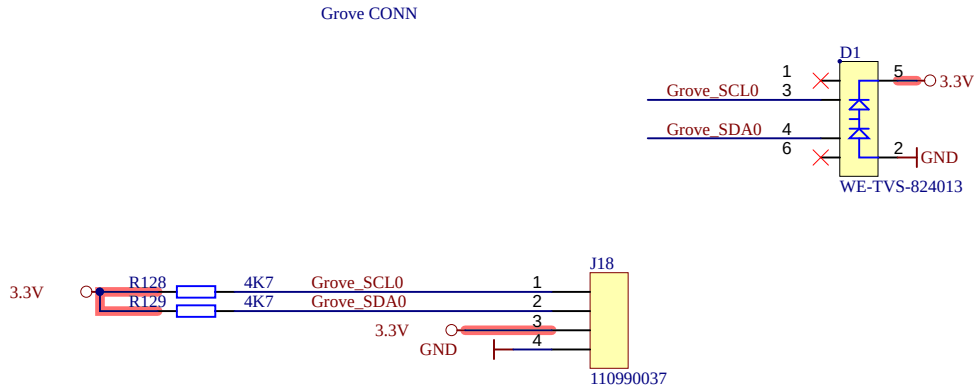
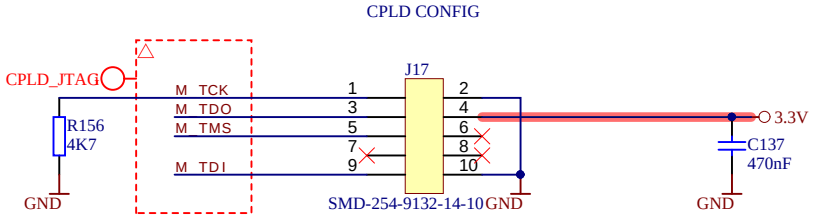
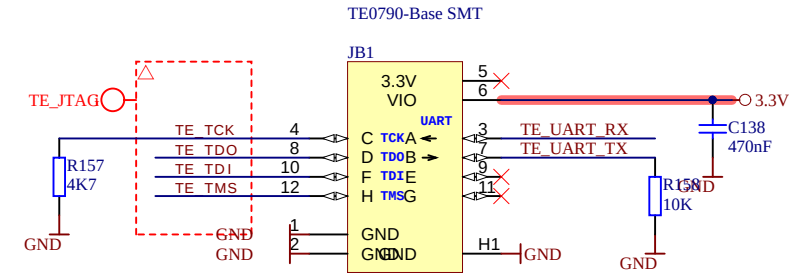
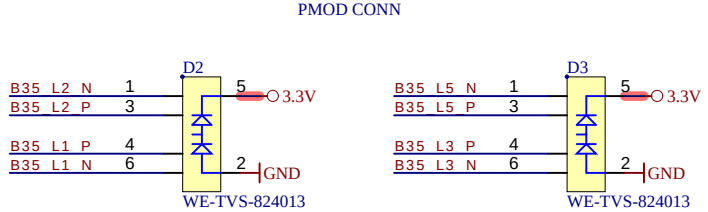
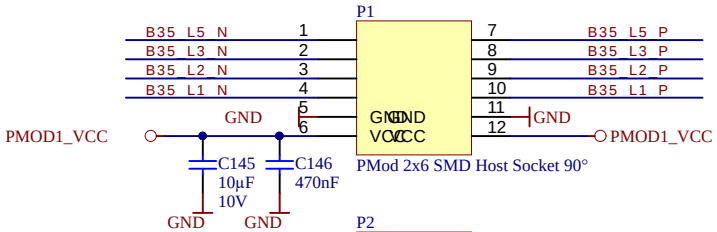
Title: MEGA65		
A4	Number: TE0765 [No Variations]	Rev. 03
Date: 2020-06-29	Copyright: Trenz Electronic GmbH	Page 1 of 23
Filename: TE0765.SchDoc		

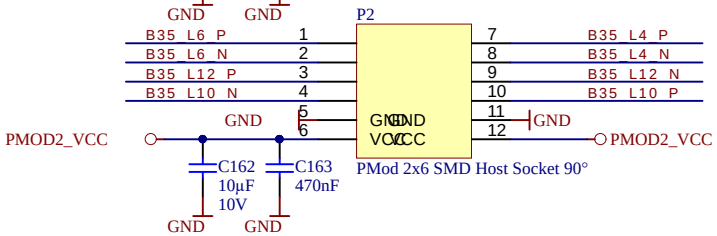


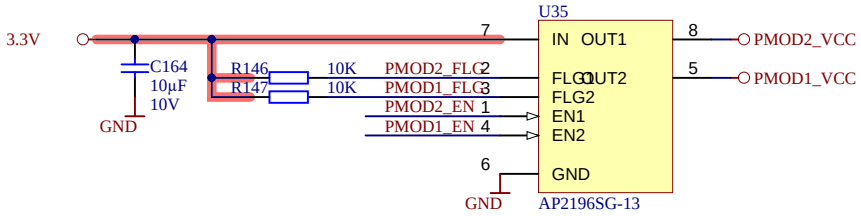












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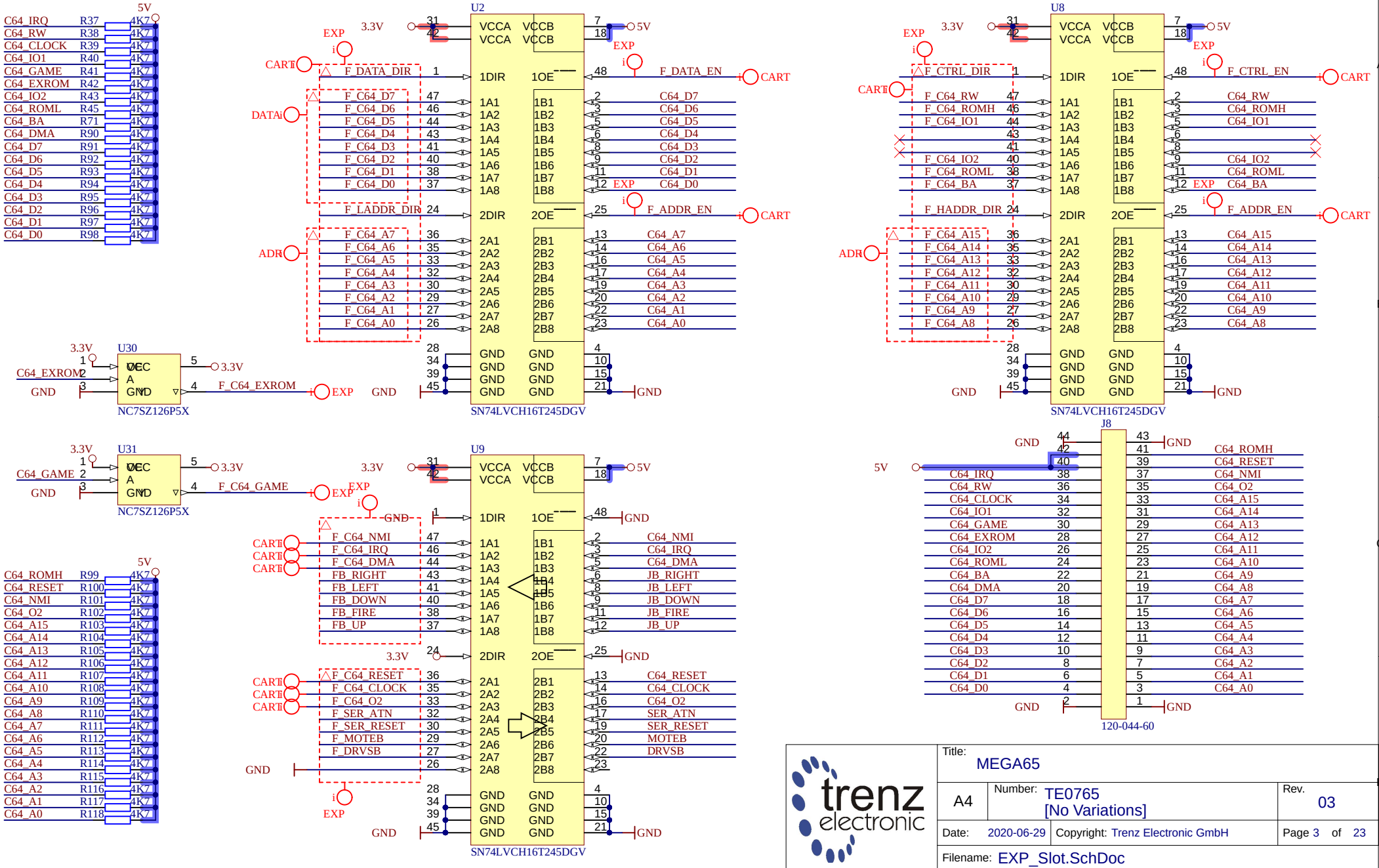
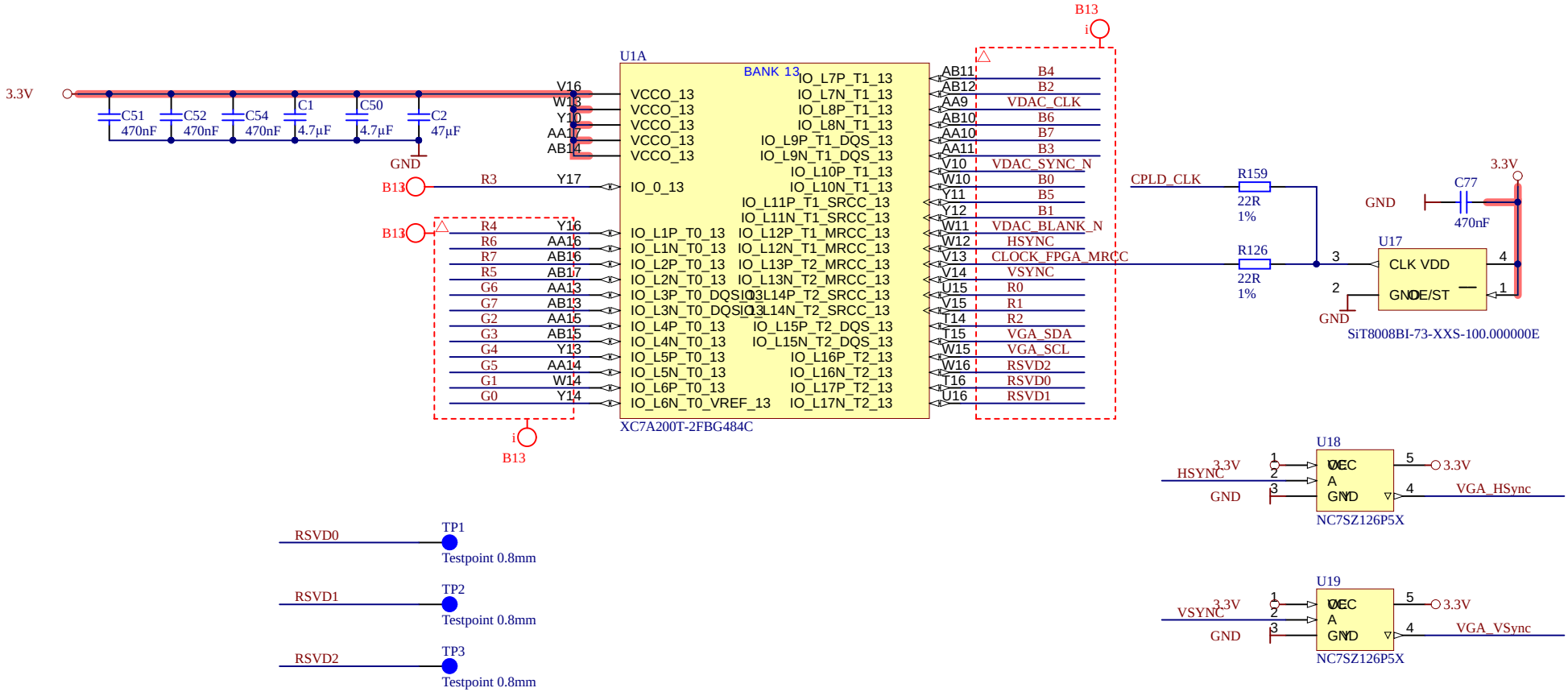
Title: MEGA65			
A4	Number: TE0765 [No Variations]		Rev. 03
Date: 2020-06-29	Copyright: Trenz Electronic GmbH		Page 2 of 23
Filename: EXT_HEADER.SchDoc			



trenz electronic	Title: MEGA65		
	A4	Number: TE0765 [No Variations]	Rev. 03
	Date: 2020-06-29	Copyright: Trenz Electronic GmbH	Page 3 of 23
	Filename: EXP_Slot.SchDoc		



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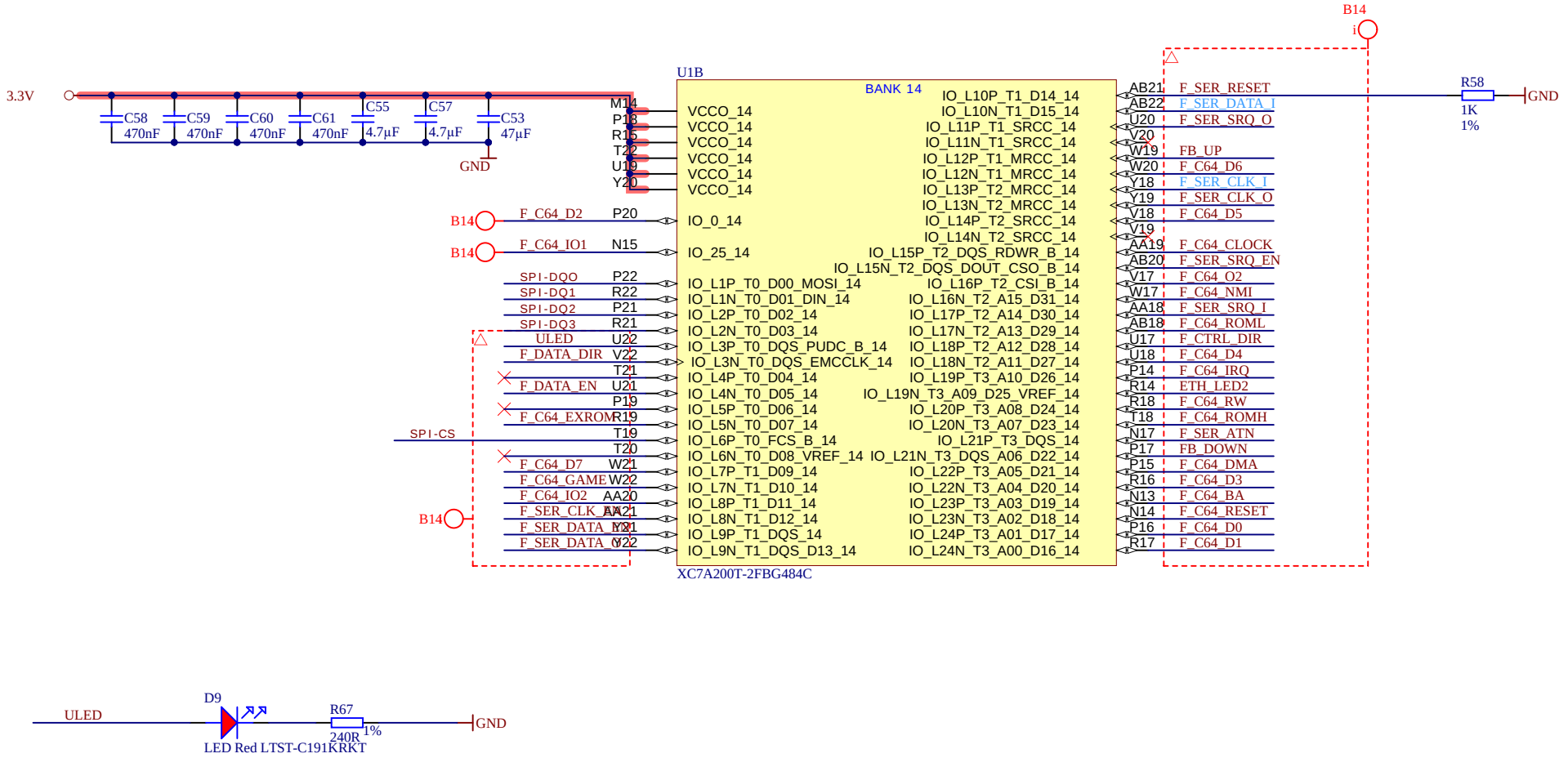
A4	Number: TE0765 [No Variations]		Rev. 03
Date: 2020-06-29	Copyright: Trenz Electronic GmbH		Page 4 of 23
Filename: B13.SchDoc			



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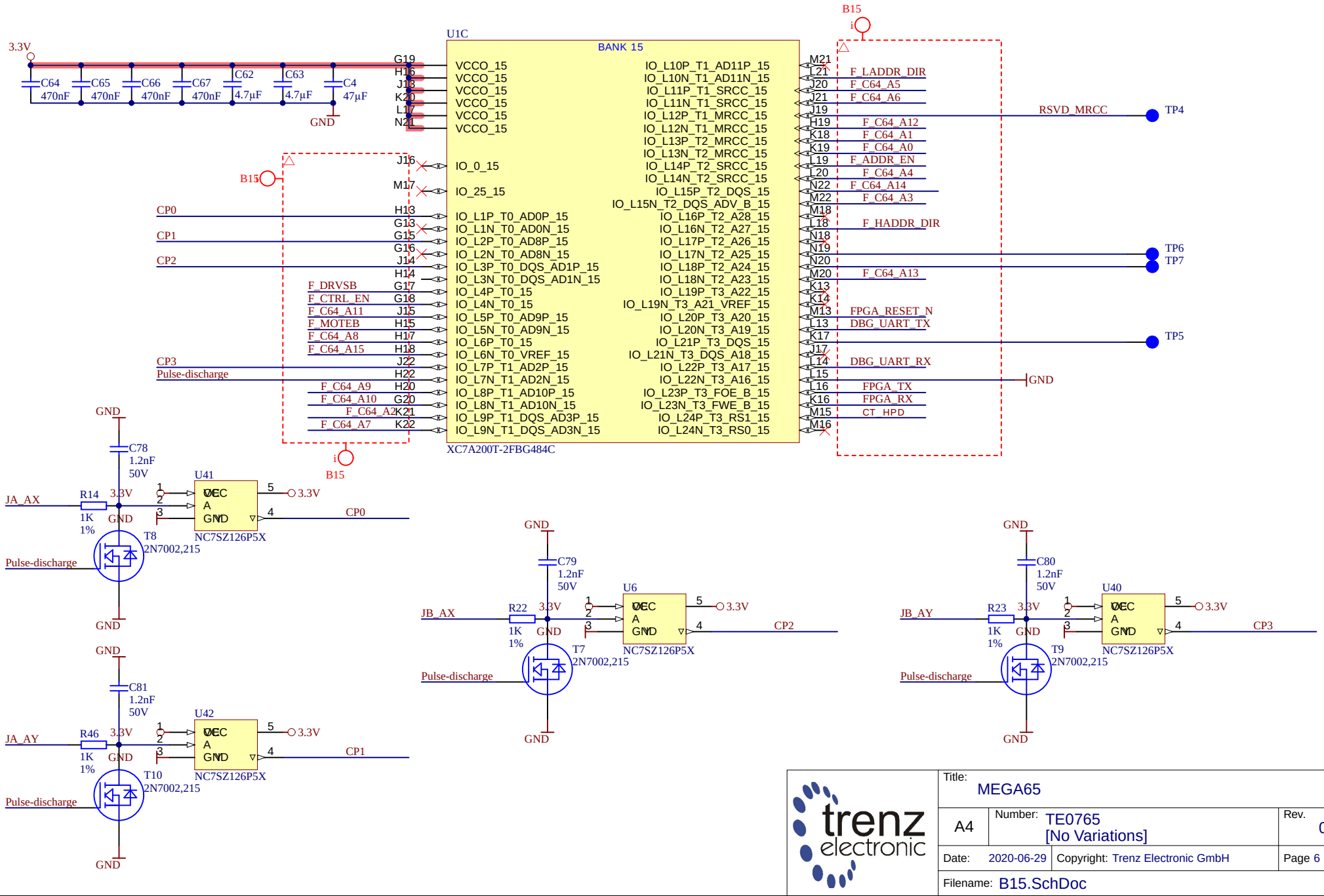
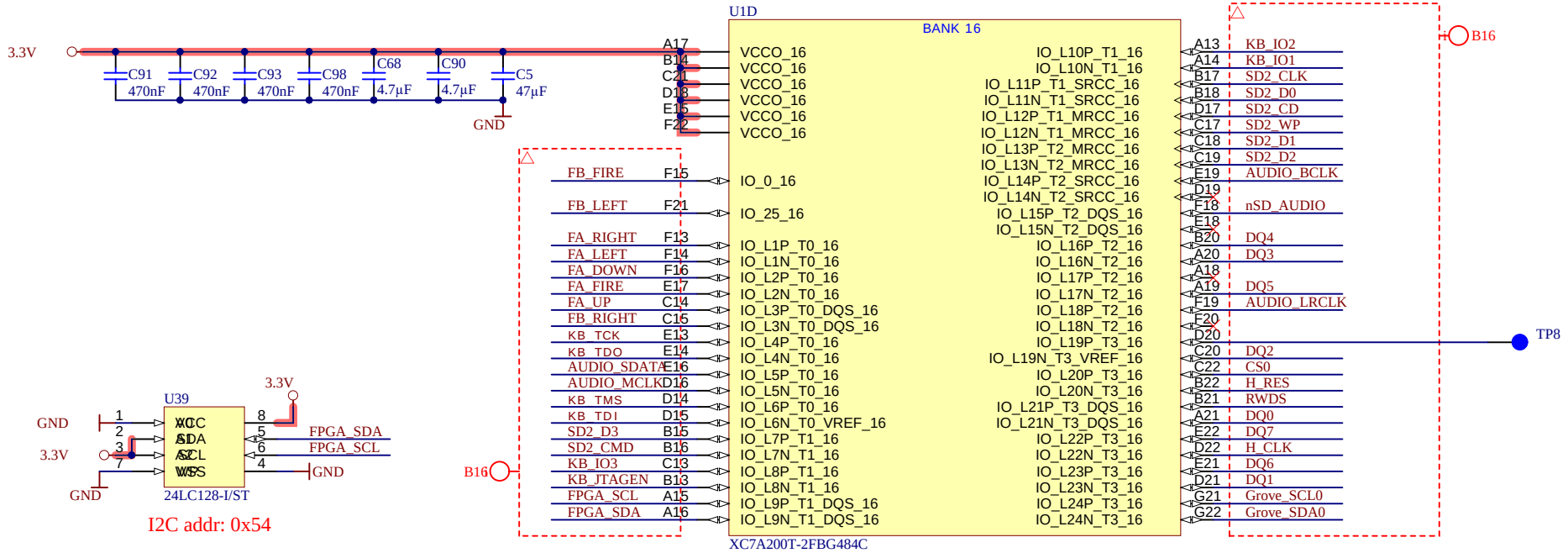
	Date: 2020-06-29	Copyright: Trenz Electronic GmbH	Page 5 of 23
	Filename: B14.SchDoc		



trenz electronic	Title: MEGA65		
A4	Number: TE0765 [No Variations]		Rev. 03
Date: 2020-06-29	Copyright: Trenz Electronic GmbH		Page 6 of 23
Filename: B15.SchDoc			



trenz electronic	Title: MEGA65		
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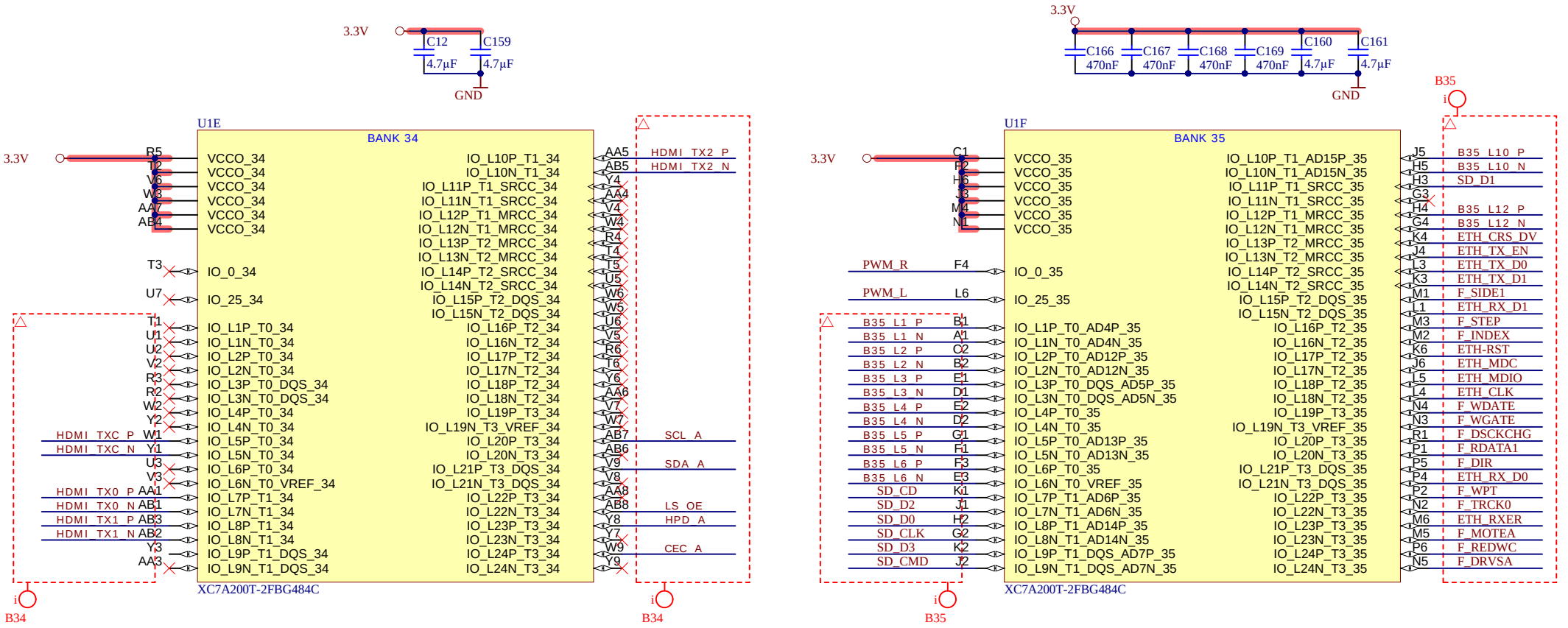
	Date: 2020-06-29	Copyright: Trenz Electronic GmbH	Page 7 of 23
	Filename: B16.SchDoc		



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Title: MEGA65			
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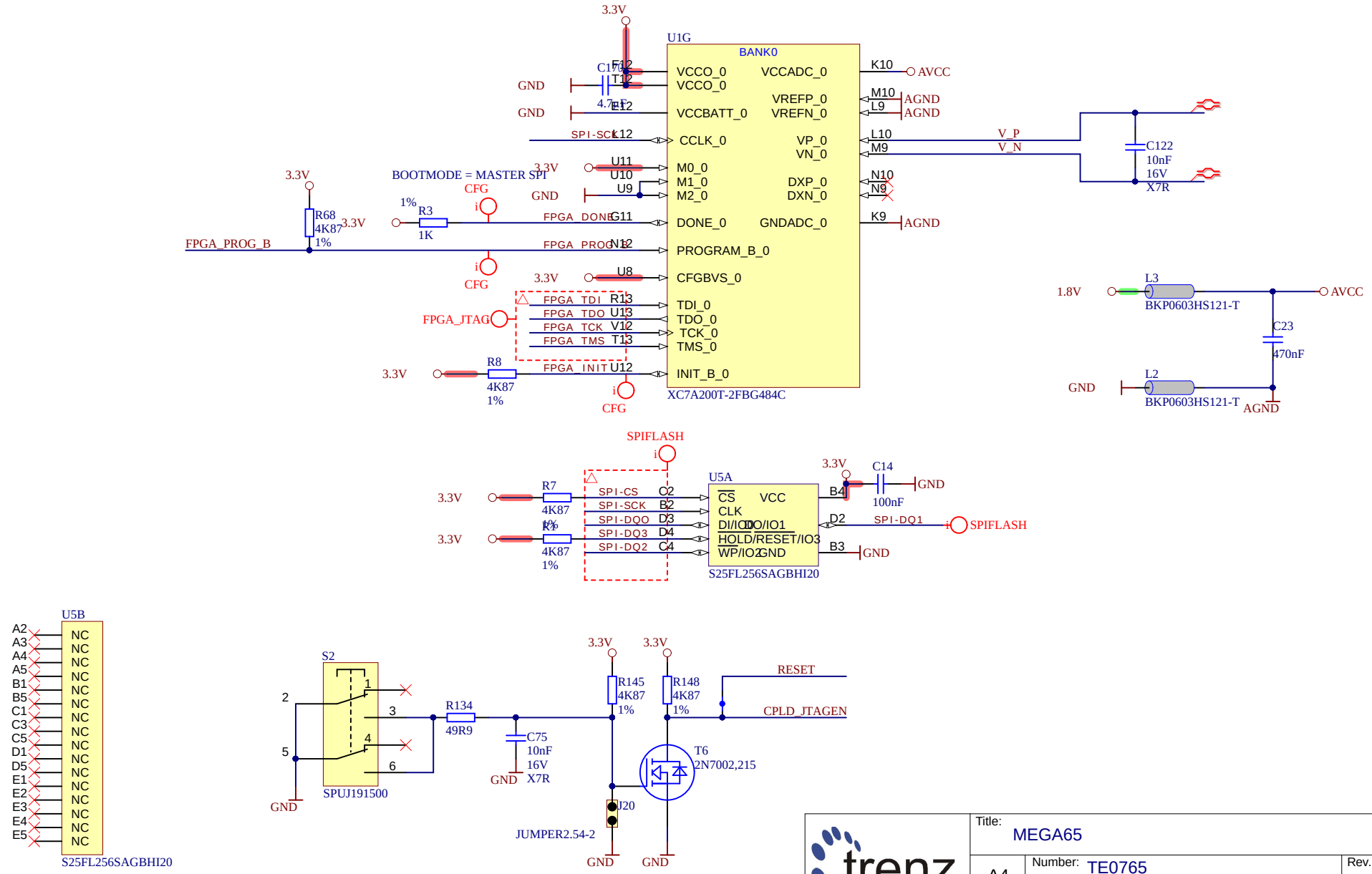
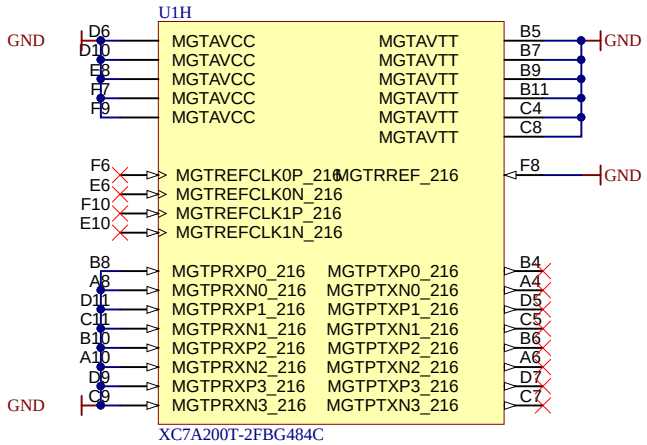
Date: 2020-06-29	Copyright: Trenz Electronic GmbH		Page 8 of 23
Filename: B34.SchDoc			



trenz electronic	Title: MEGA65		
	A4	Number: TE0765 [No Variations]	Rev. 03
	Date: 2020-06-29	Copyright: Trenz Electronic GmbH	Page 9 of 23
	Filename: FPGA-CFG.SchDoc		



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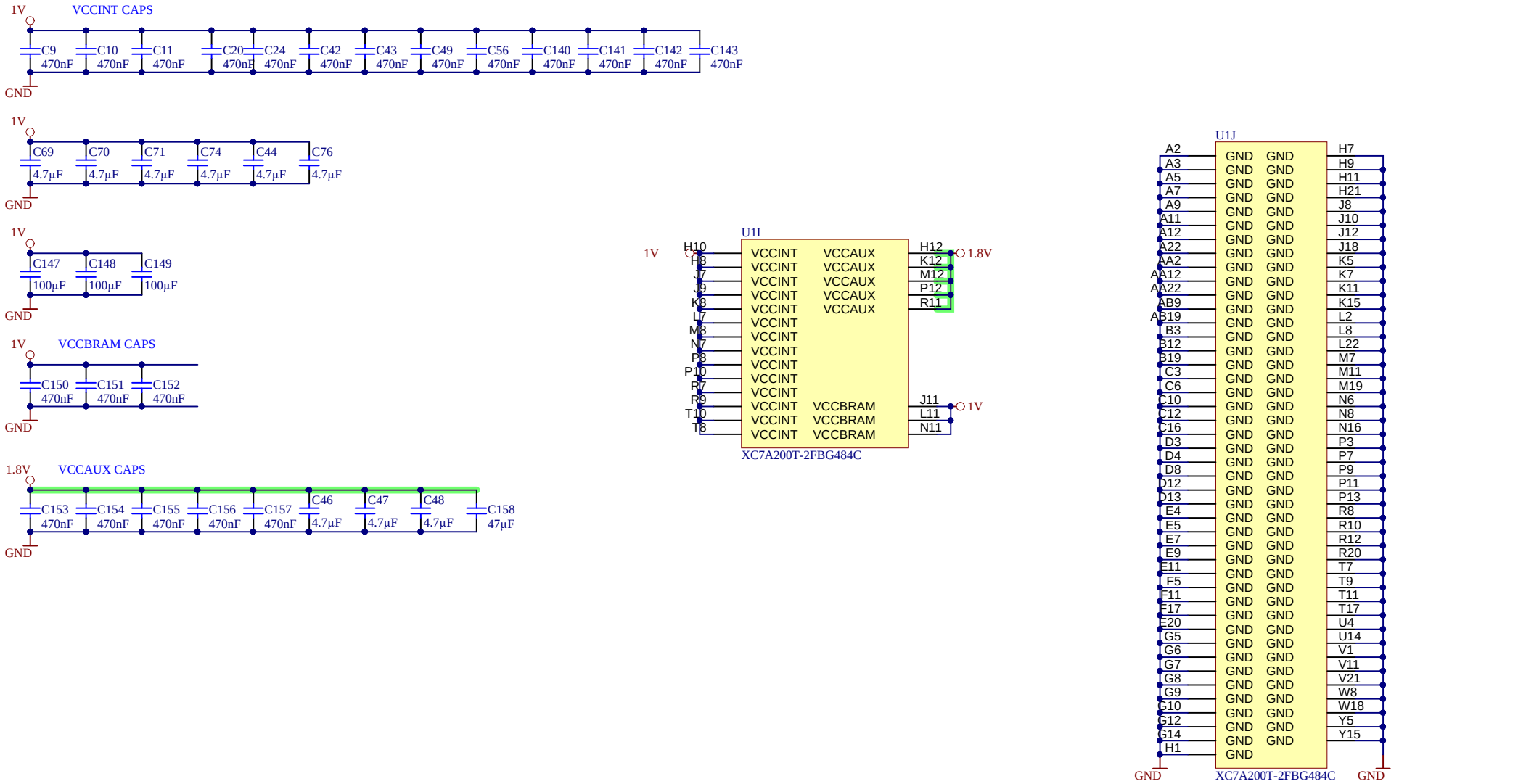
	Date: 2020-06-29	Copyright: Trenz Electronic GmbH	Page 10 of 23
	Filename: FPGA-MGT.SchDoc		



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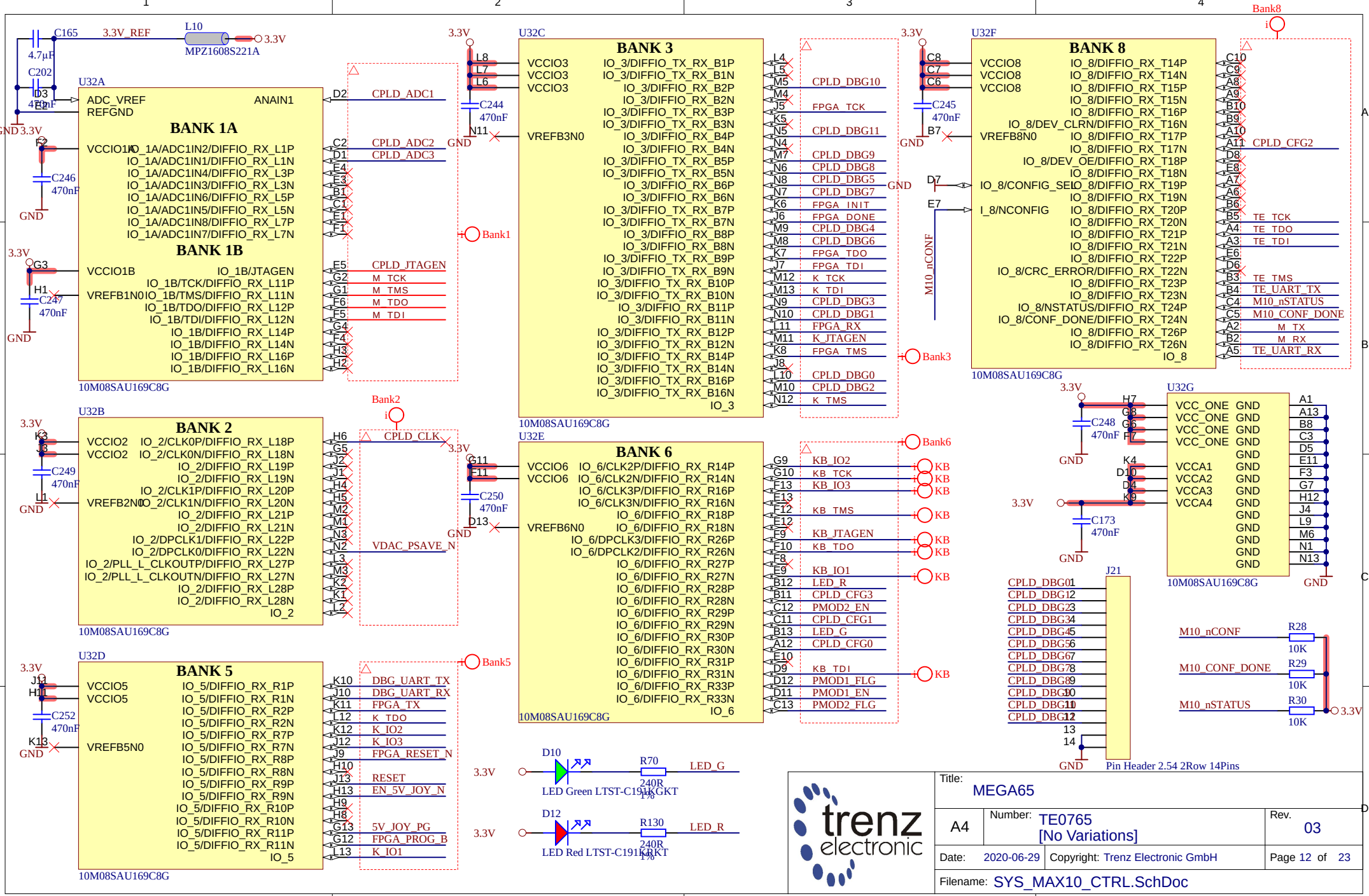
Title: MEGA65		
A4	Number: TE0765 [No Variations]	Rev. 03
Date: 2020-06-29	Copyright: Trenz Electronic GmbH	Page 11 of 23
Filename: FPGA-PWR.SchDoc		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4.7µF
C202
4.7µF
3.3V_REF
L10
MPZ1608S221A
3.3V
GND
U32A
ADC_VREF
REFGND
ANAIN1
BANK 1A
VCCIO1A
IO_1A/ADC1IN2/DIFFIO_RX_L1P
IO_1A/ADC1IN1/DIFFIO_RX_L1N
IO_1A/ADC1IN4/DIFFIO_RX_L3P
IO_1A/ADC1IN3/DIFFIO_RX_L3N
IO_1A/ADC1IN6/DIFFIO_RX_L5P
IO_1A/ADC1IN5/DIFFIO_RX_L5N
IO_1A/ADC1IN8/DIFFIO_RX_L7P
IO_1A/ADC1IN7/DIFFIO_RX_L7N
BANK 1B
VCCIO1B
IO_1B/JTAGEN
IO_1B/TCK/DIFFIO_RX_L11P
VREFB1N0
IO_1B/TMS/DIFFIO_RX_L11N
IO_1B/TDO/DIFFIO_RX_L12P
IO_1B/TDI/DIFFIO_RX_L12N
IO_1B/DIFFIO_RX_L14P
IO_1B/DIFFIO_RX_L14N
IO_1B/DIFFIO_RX_L16P
IO_1B/DIFFIO_RX_L16N
10M08SAU169C8G
C246
470nF
C247
470nF
CPLD_ADC1
CPLD_ADC2
CPLD_ADC3
CPLD_JTAGEN
M_TCK
M_TMS
M_TDO
M_TDI
Bank1
U32B
BANK 2
VCCIO2
IO_2/CLK0P/DIFFIO_RX_L18P
IO_2/CLK0N/DIFFIO_RX_L18N
IO_2/DIFFIO_RX_L19P
IO_2/DIFFIO_RX_L19N
IO_2/CLK1P/DIFFIO_RX_L20P
VREFB2N0
IO_2/CLK1N/DIFFIO_RX_L20N
IO_2/DIFFIO_RX_L21P
IO_2/DIFFIO_RX_L21N
IO_2/DPCLK1/DIFFIO_RX_L22P
IO_2/DPCLK0/DIFFIO_RX_L22N
IO_2/PLL_L_CLKOUTP/DIFFIO_RX_L27P
IO_2/PLL_L_CLKOUTN/DIFFIO_RX_L27N
IO_2/DIFFIO_RX_L28P
IO_2/DIFFIO_RX_L28N
IO_2
10M08SAU169C8G
C249
470nF
Bank2
CPLD_CLK
VDAC_PSAVE_N
U32D
BANK 5
VCCIO5
IO_5/DIFFIO_RX_R1P
IO_5/DIFFIO_RX_R1N
IO_5/DIFFIO_RX_R2P
IO_5/DIFFIO_RX_R2N
IO_5/DIFFIO_RX_R7P
VREFB5N0
IO_5/DIFFIO_RX_R7N
IO_5/DIFFIO_RX_R8P
IO_5/DIFFIO_RX_R8N
IO_5/DIFFIO_RX_R9P
IO_5/DIFFIO_RX_R9N
IO_5/DIFFIO_RX_R10P
IO_5/DIFFIO_RX_R10N
IO_5/DIFFIO_RX_R11P
IO_5/DIFFIO_RX_R11N
IO_5
10M08SAU169C8G
C252
470nF
DBG_UART_TX
DBG_UART_RX
FPGA_TX
K_TDO
K_IO2
K_IO3
FPGA_RESET_N
RESET
EN_5V_JOY_N
5V_JOY_PG
FPGA_PROG_B
K_IO1
Bank5
U32C
BANK 3
VCCIO3
IO_3/DIFFIO_TX_RX_B1P
IO_3/DIFFIO_TX_RX_B1N
IO_3/DIFFIO_RX_B2P
IO_3/DIFFIO_RX_B2N
IO_3/DIFFIO_TX_RX_B3P
IO_3/DIFFIO_TX_RX_B3N
VREFB3N0
IO_3/DIFFIO_RX_B4P
IO_3/DIFFIO_RX_B4N
IO_3/DIFFIO_TX_RX_B5P
IO_3/DIFFIO_TX_RX_B5N
IO_3/DIFFIO_RX_B6P
IO_3/DIFFIO_RX_B6N
IO_3/DIFFIO_TX_RX_B7P
IO_3/DIFFIO_TX_RX_B7N
IO_3/DIFFIO_RX_B8P
IO_3/DIFFIO_RX_B8N
IO_3/DIFFIO_TX_RX_B9P
IO_3/DIFFIO_TX_RX_B9N
IO_3/DIFFIO_TX_RX_B10P
IO_3/DIFFIO_TX_RX_B10N
IO_3/DIFFIO_RX_B11P
IO_3/DIFFIO_RX_B11N
IO_3/DIFFIO_TX_RX_B12P
IO_3/DIFFIO_TX_RX_B12N
IO_3/DIFFIO_TX_RX_B14P
IO_3/DIFFIO_TX_RX_B14N
IO_3/DIFFIO_TX_RX_B16P
IO_3/DIFFIO_TX_RX_B16N
IO_3
10M08SAU169C8G
C244
470nF
CPLD_DBG10
FPGA_TCK
CPLD_DBG11
CPLD_DBG9
CPLD_DBG8
CPLD_DBG5
CPLD_DBG7
FPGA_INIT
FPGA_DONE
CPLD_DBG4
CPLD_DBG6
FPGA_TDO
FPGA_TDI
K_TCK
K_TDI
CPLD_DBG3
CPLD_DBG1
FPGA_RX
K_JTAGEN
FPGA_TMS
CPLD_DBG0
CPLD_DBG2
K_TMS
Bank3
U32E
BANK 6
VCCIO6
IO_6/CLK2P/DIFFIO_RX_R14P
IO_6/CLK2N/DIFFIO_RX_R14N
IO_6/CLK3P/DIFFIO_RX_R16P
IO_6/CLK3N/DIFFIO_RX_R16N
IO_6/DIFFIO_RX_R18P
VREFB6N0
IO_6/DIFFIO_RX_R18N
IO_6/DPCLK3/DIFFIO_RX_R26P
IO_6/DPCLK2/DIFFIO_RX_R26N
IO_6/DIFFIO_RX_R27P
IO_6/DIFFIO_RX_R27N
IO_6/DIFFIO_RX_R28P
IO_6/DIFFIO_RX_R28N
IO_6/DIFFIO_RX_R29P
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IO_6/DIFFIO_RX_R31P
IO_6/DIFFIO_RX_R31N
IO_6/DIFFIO_RX_R33P
IO_6/DIFFIO_RX_R33N
IO_6
10M08SAU169C8G
C250
470nF
KB_IO2
KB_TCK
KB_IO3
KB_TMS
KB_JTAGEN
KB_TDO
KB_IO1
LED_R
CPLD_CFG3
PMOD2_EN
CPLD_CFG1
LED_G
CPLD_CFG0
KB_TDI
PMOD1_FLG
PMOD1_EN
PMOD2_FLG
Bank6
KB
D10
LED Green LTST-C191KGKT
R70
240R
1%
LED_G
D12
LED Red LTST-C191KRKT
R130
240R
1%
LED_R
U32F
BANK 8
VCCIO8
IO_8/DIFFIO_RX_T14P
IO_8/DIFFIO_RX_T14N
IO_8/DIFFIO_RX_T15P
IO_8/DIFFIO_RX_T15N
IO_8/DIFFIO_RX_T16P
IO_8/DEV_CLRN/DIFFIO_RX_T16N
VREFB8N0
IO_8/DIFFIO_RX_T17P
IO_8/DIFFIO_RX_T17N
IO_8/DEV_OE/DIFFIO_RX_T18P
IO_8/DIFFIO_RX_T18N
IO_8/CONFIG_SEL
IO_8/DIFFIO_RX_T19P
IO_8/DIFFIO_RX_T19N
I_8/NCONFIG
IO_8/DIFFIO_RX_T20P
IO_8/DIFFIO_RX_T20N
IO_8/DIFFIO_RX_T21P
IO_8/DIFFIO_RX_T21N
IO_8/DIFFIO_RX_T22P
IO_8/CRC_ERROR/DIFFIO_RX_T22N
IO_8/DIFFIO_RX_T23P
IO_8/DIFFIO_RX_T23N
IO_8/NSTATUS/DIFFIO_RX_T24P
IO_8/CONF_DONE/DIFFIO_RX_T24N
IO_8/DIFFIO_RX_T26P
IO_8/DIFFIO_RX_T26N
IO_8
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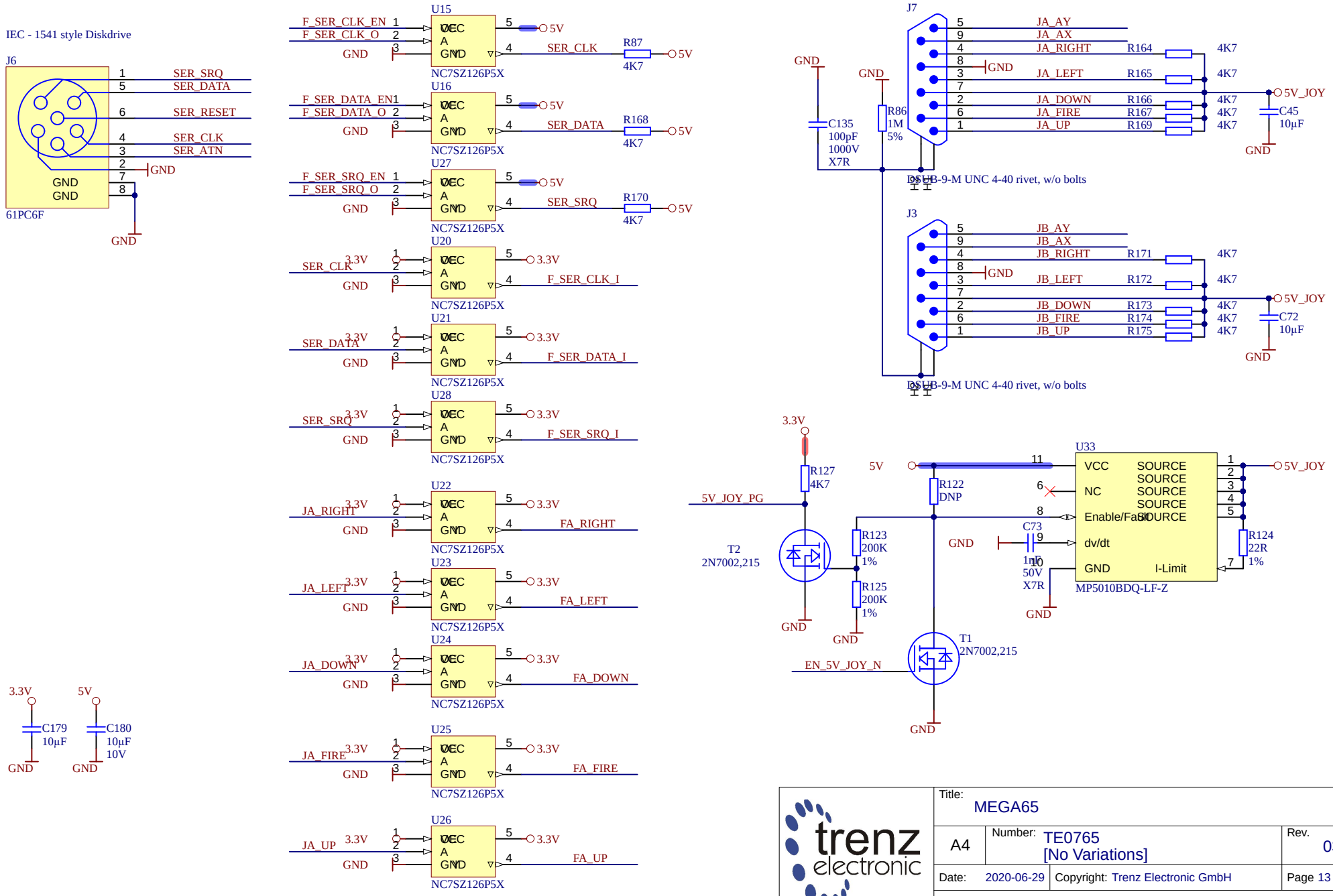
C245
470nF
M10_nCONF
CPLD_CFG2
TE_TCK
TE_TDO
TE_TDI
TE_TMS
TE_UART_TX
M10_nSTATUS
M10_CONF_DONE
M_TX
M_RX
TE_UART_RX
Bank8
U32G
VCC_ONE
VCCA1
VCCA2
VCCA3
VCCA4
GND
10M08SAU169C8G
C248
470nF
C173
470nF
J21
Pin Header 2.54 2Row 14Pins
CPLD_DBG0
CPLD_DBG1
CPLD_DBG2
CPLD_DBG3
CPLD_DBG4
CPLD_DBG5
CPLD_DBG6
CPLD_DBG7
CPLD_DBG8
CPLD_DBG9
CPLD_DBG10
CPLD_DBG11
CPLD_DBG12
R28
10K
R29
10K
R30
10K
M10_nCONF
M10_CONF_DONE
M10_nSTATUS
trenz electronic
Title: MEGA65
A4
Number: TE0765 [No Variations]
Rev. 03
Date: 2020-06-29
Copyright: Trenz Electronic GmbH
Page 12 of 23
Filename: SYS_MAX10_CTRL.SchDoc



Title: MEGA65			
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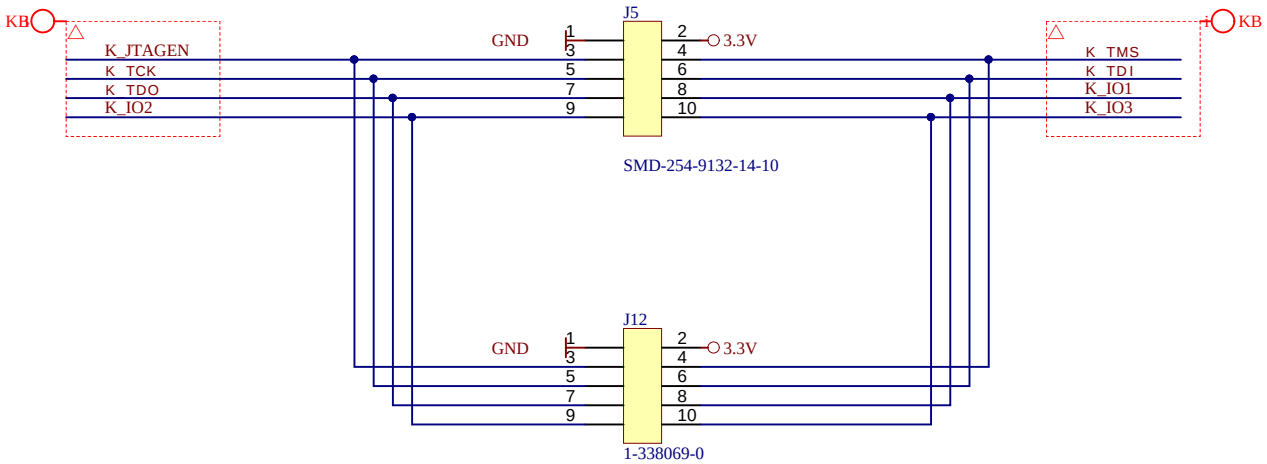
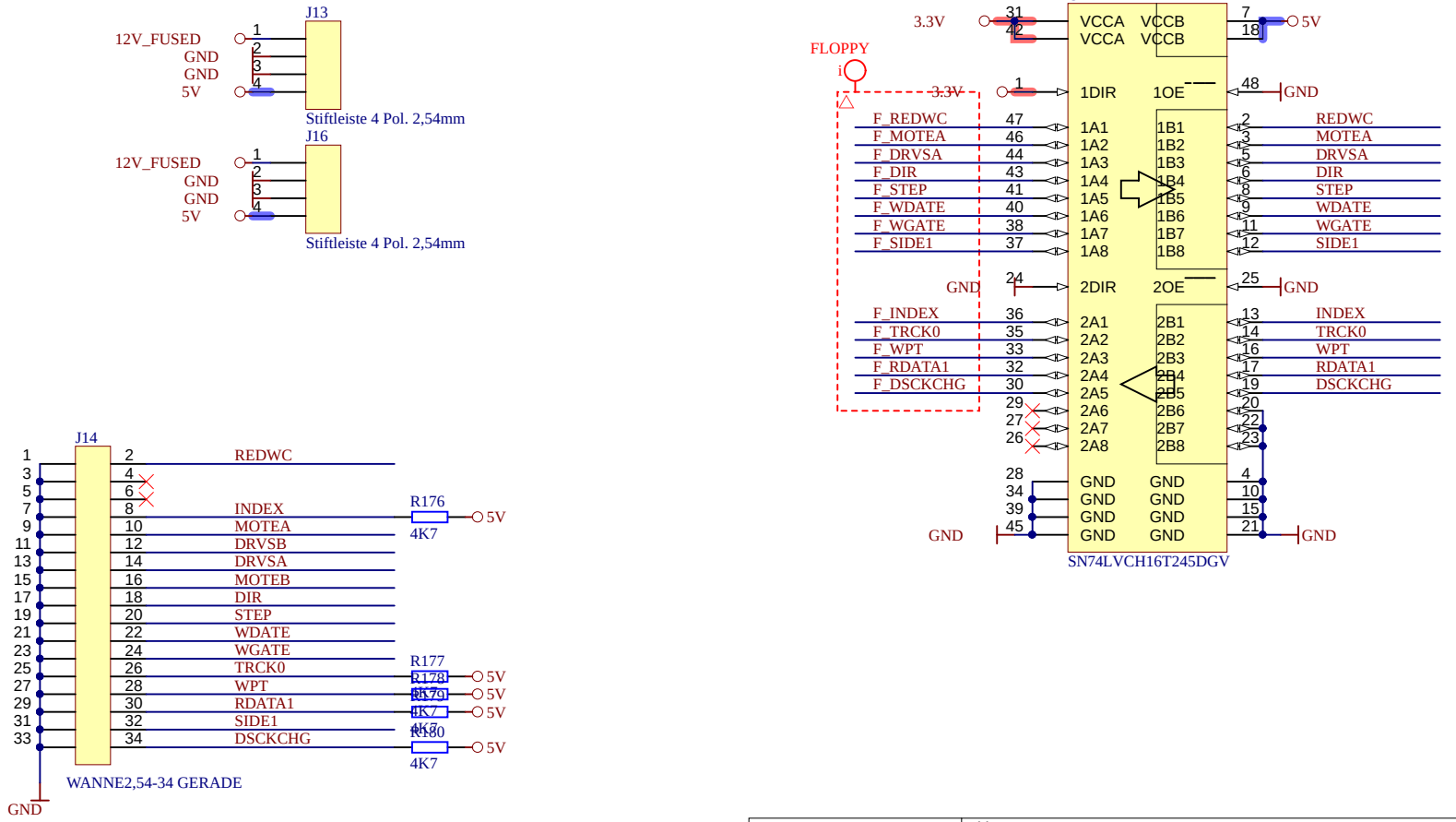
Date: 2020-06-29	Copyright: Trenz Electronic GmbH		Page 13 of 23
Filename: JOY.SchDoc			



trenz electronic	Title: MEGA65		
	A4	Number: TE0765 [No Variations]	Rev. 03
	Date: 2020-06-29	Copyright: Trenz Electronic GmbH	Page 14 of 23
	Filename: KEYBOARD.SchDoc		



trenz electronic	Title: MEGA65		
	A4	Number: TE0765 [No Variations]	Rev. 03
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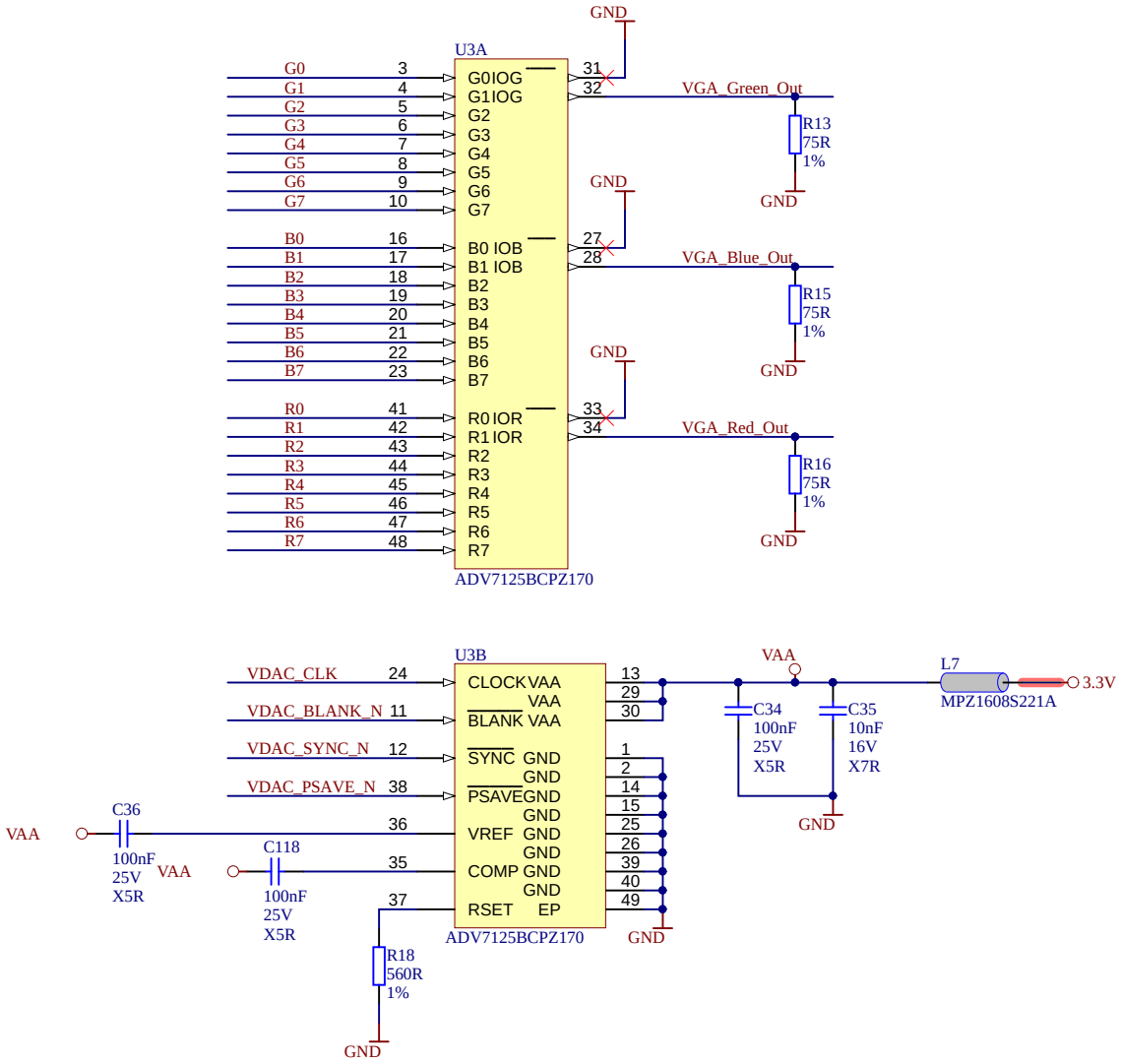
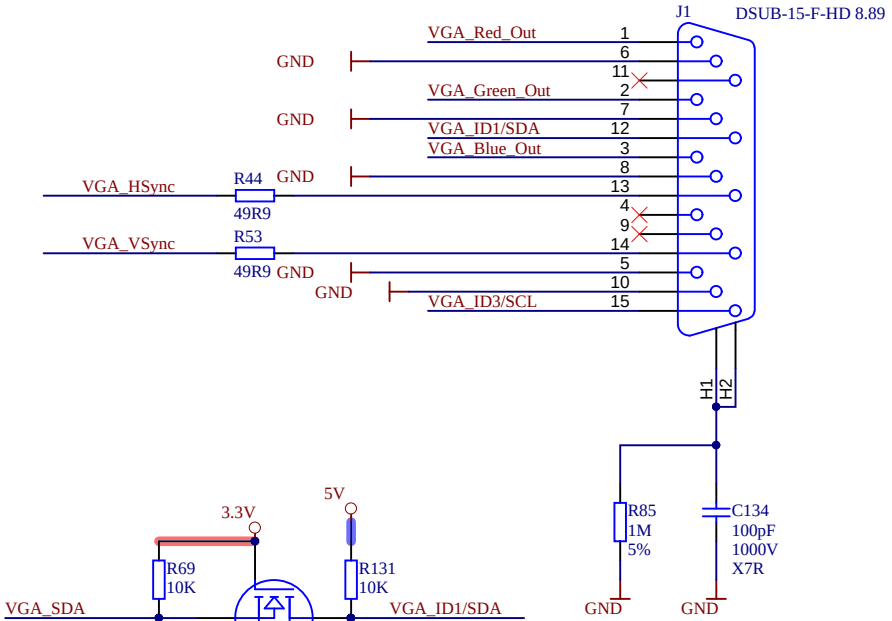
	Filename: Floppy.SchDoc		





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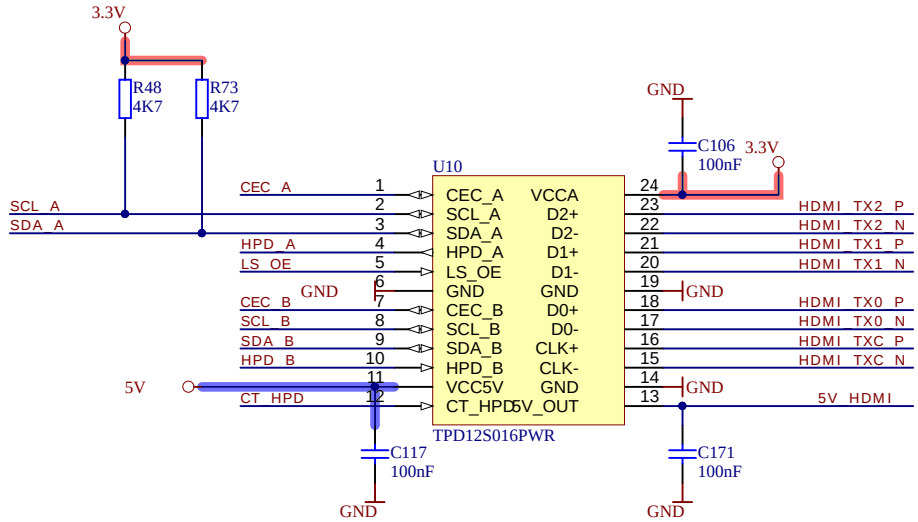
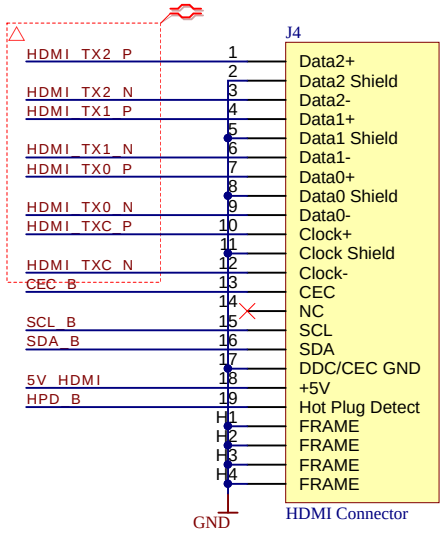
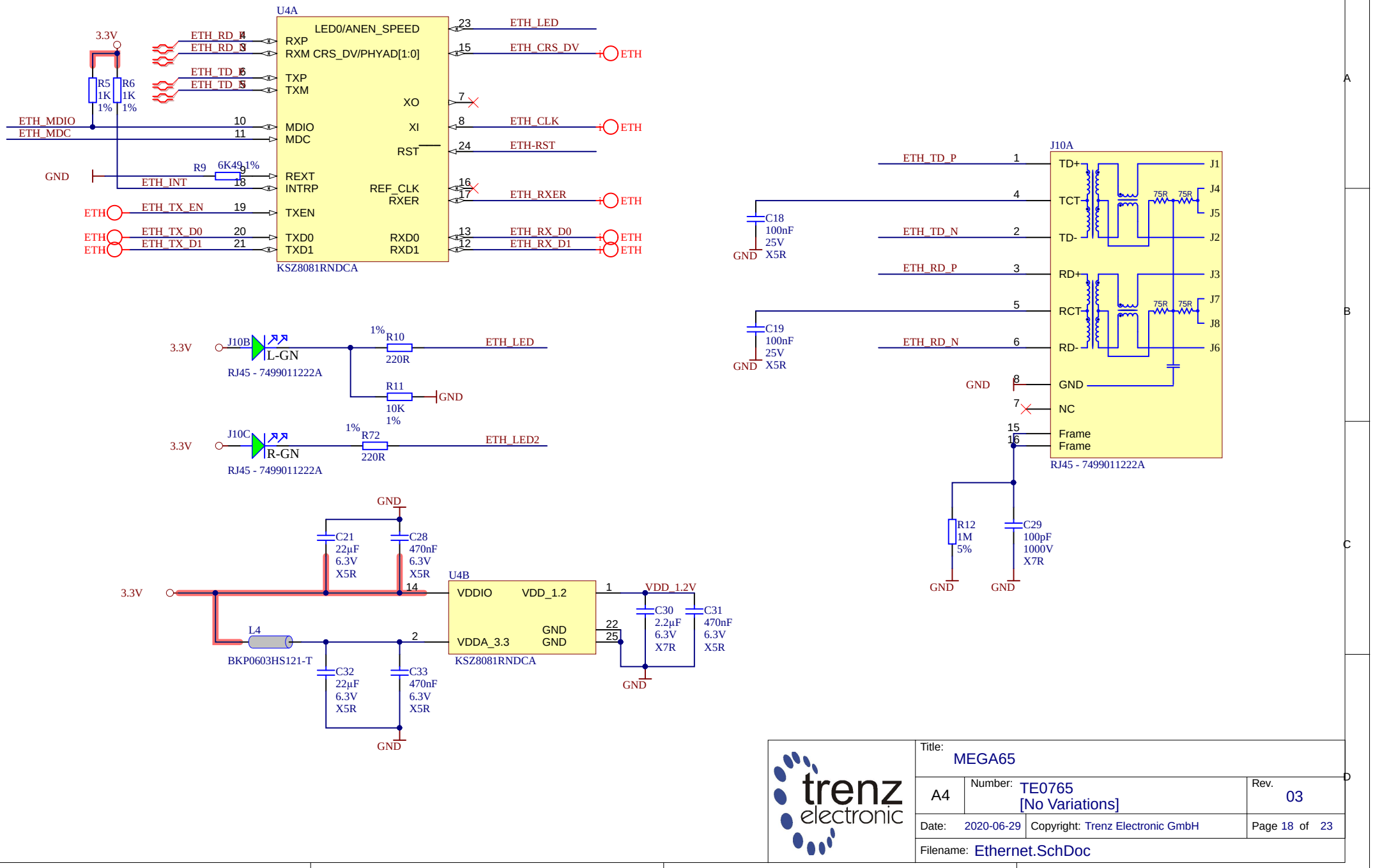
Title: MEGA65			
A4	Number: TE0765 [No Variations]		Rev. 03
Date: 2020-06-29	Copyright: Trenz Electronic GmbH		Page 16 of 23
Filename: VGA.SchDoc			





trenz electronic	Title: MEGA65		
	A4	Number: TE0765 [No Variations]	Rev. 03
	Date: 2020-06-29	Copyright: Trenz Electronic GmbH	Page 17 of 23
	Filename: HDMI.SchDoc		



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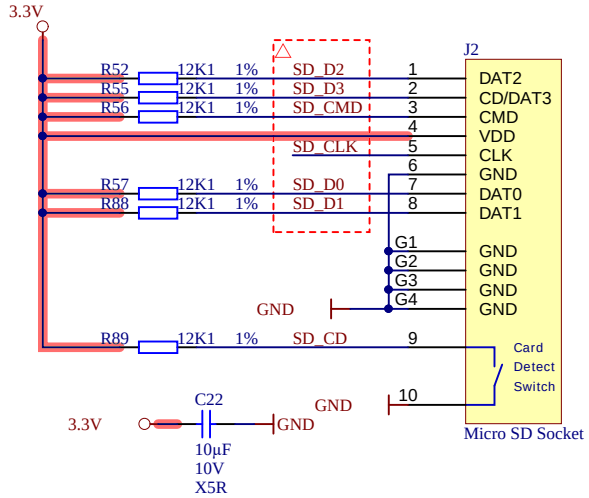
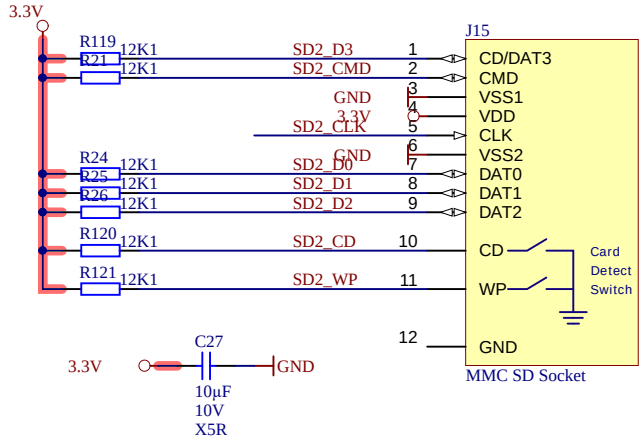
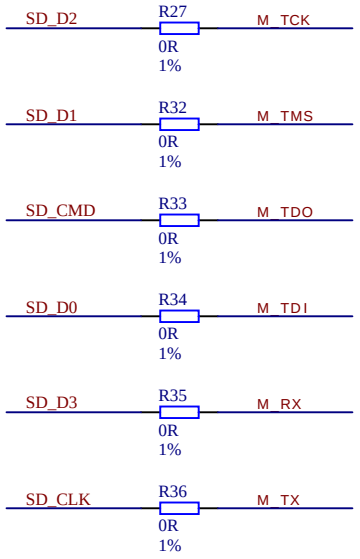
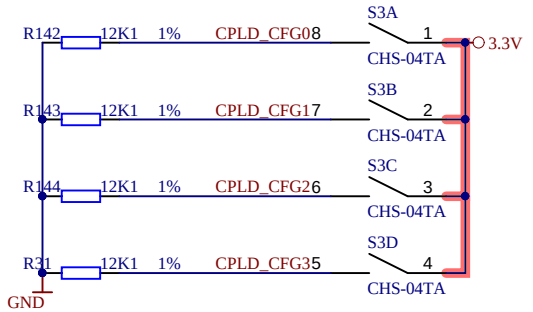
Date: 2020-06-29	Copyright: Trenz Electronic GmbH		Page 18 of 23
Filename: Ethernet.SchDoc			





http://linux-sunxi.org/MicroSD_Breakout





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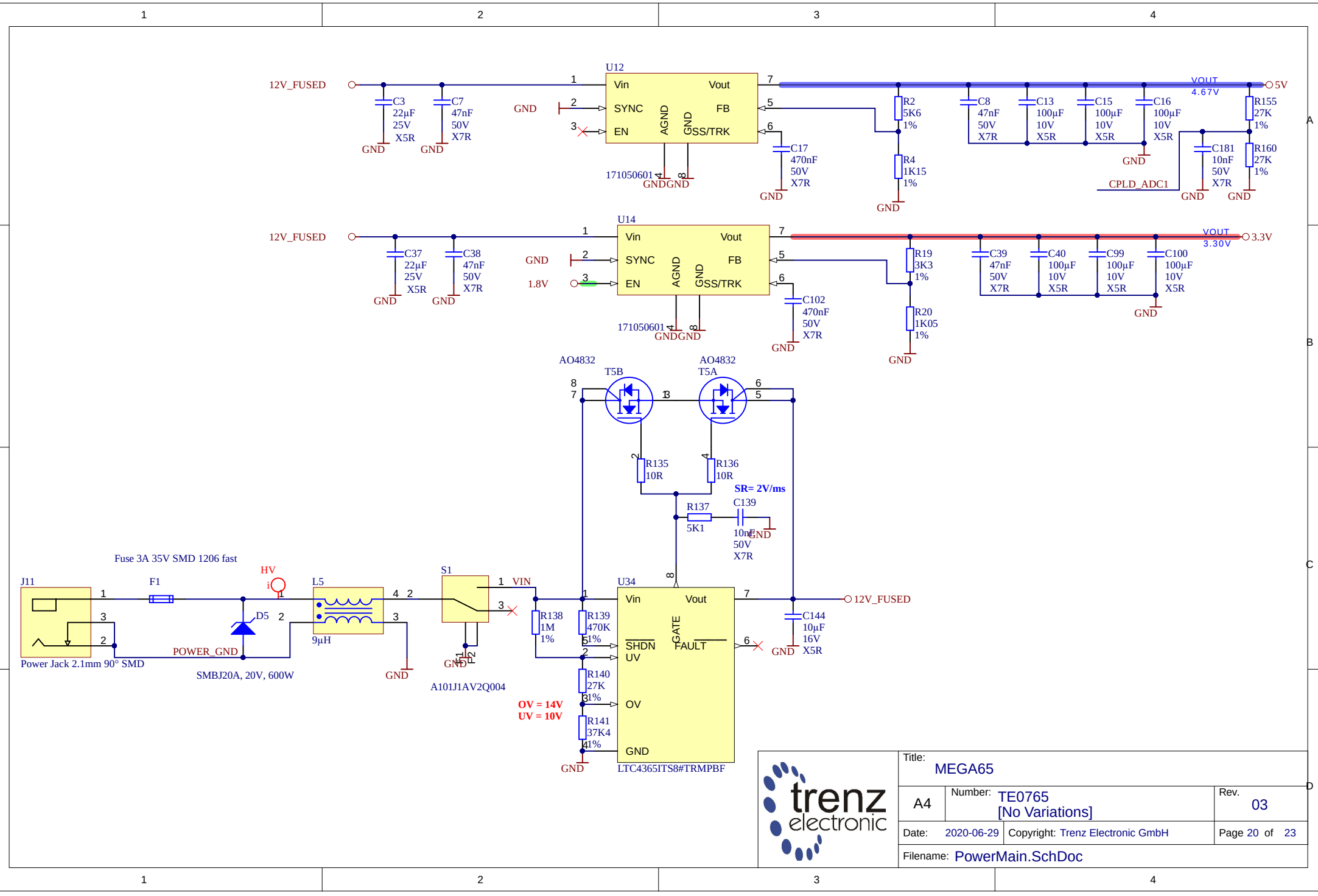
Date: 2020-06-29	Copyright: Trenz Electronic GmbH		Page 19 of 23
Filename: LED_SW_BUT.SchDoc			



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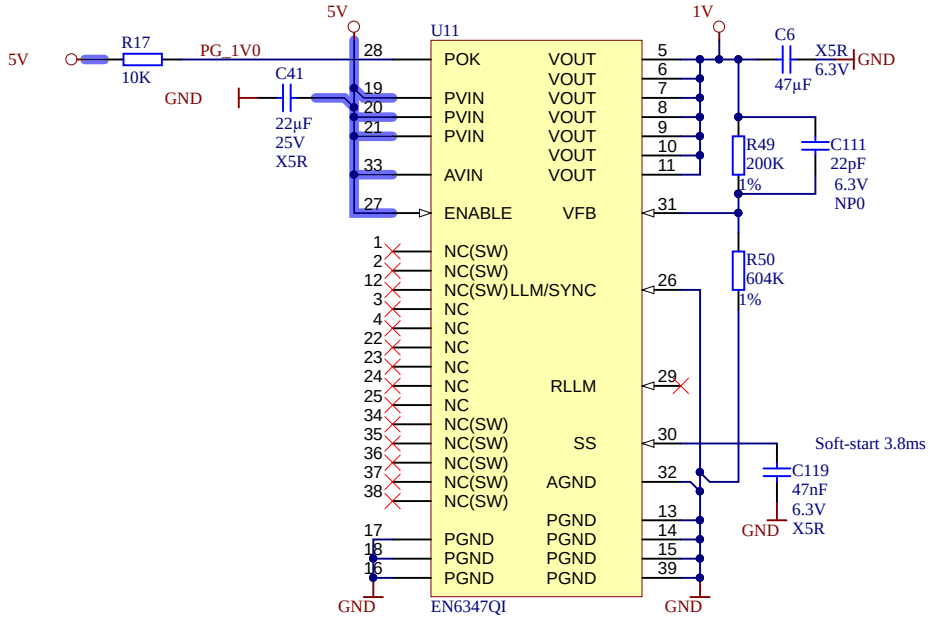
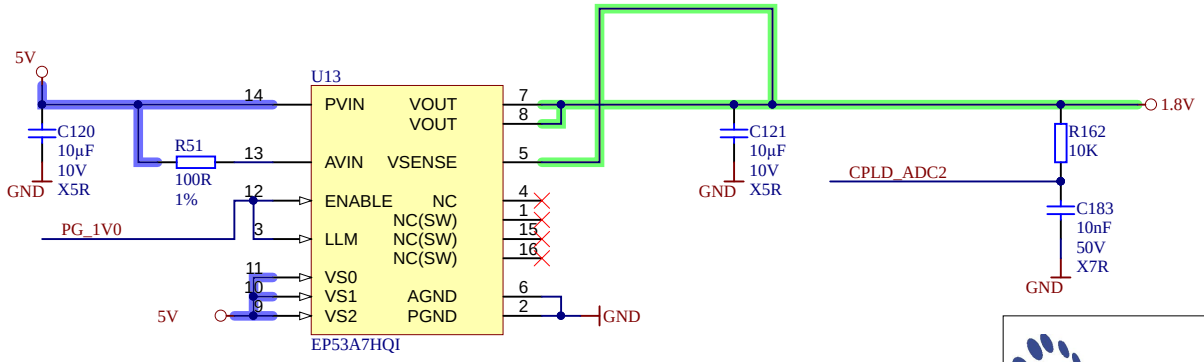
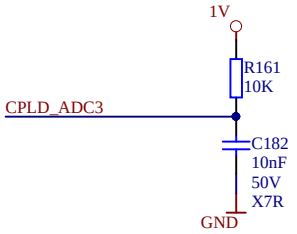
	Date: 2020-06-29	Copyright: Trenz Electronic GmbH	Page 20 of 23
	Filename: PowerMain.SchDoc		







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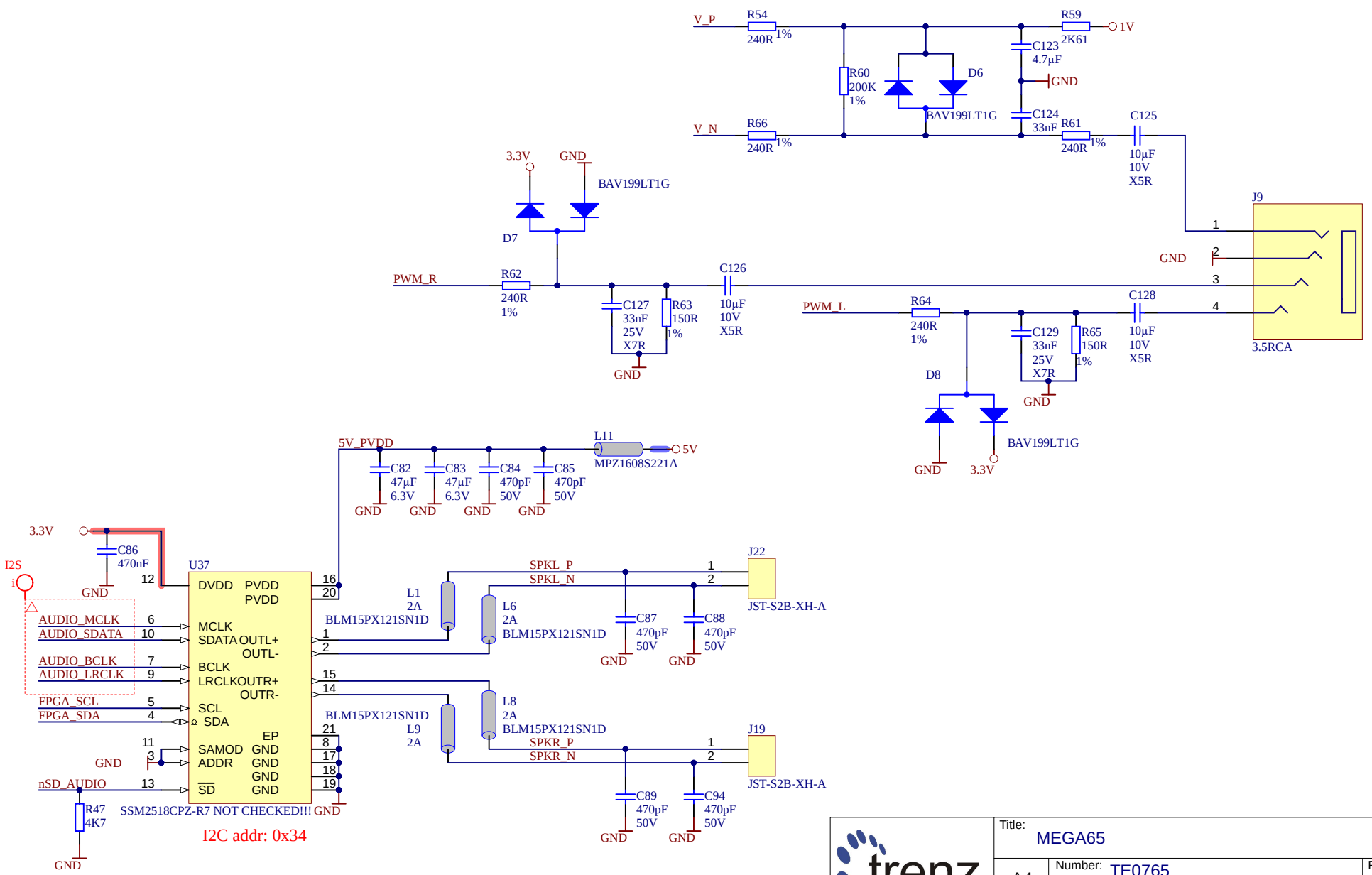
Date: 2020-06-29	Copyright: Trenz Electronic GmbH / TT		Page 21 of 23
Filename: POWER.SchDoc			



Title: MEGA65			
A4	Number: TE0765 [No Variations]		Rev. 03
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Filename: SOUND.SchDoc			

REVISION HISTORY

REV	Description	
-03	1. Added a VRP resistor on bank 65; 2. LDO U33 is changed on ADP7102ACPZ; 3. Signal FPGA IO0 is connected on AE18 pin of FPGA; 4. Signal DBG_LED3 is connected on AD18 pin of FPGA; 5. Signal MIO13_25 connected to J1 pin 33 instead MIO25. 6. Resistor R84 is removed; 7. LED D1 moved on edge of PCB; 8. Added THT testpoints J4 on CPLD_JTAGEN, R76 was removed; 9. Signals B49_XX_X are renamed in B88_XX_X; 10. C241 is changed on 1nF; 11. Length of CLK signals on RFADC and RFDAC are adjusted; 12. Wrong connection on U8 is fixed (PCB); 13. Wrong connection PGOOD1 pin of U7 is fixed;	IG

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Title: MEGA65		
A4	Number: TE0835 [No Variations]	Rev. 03
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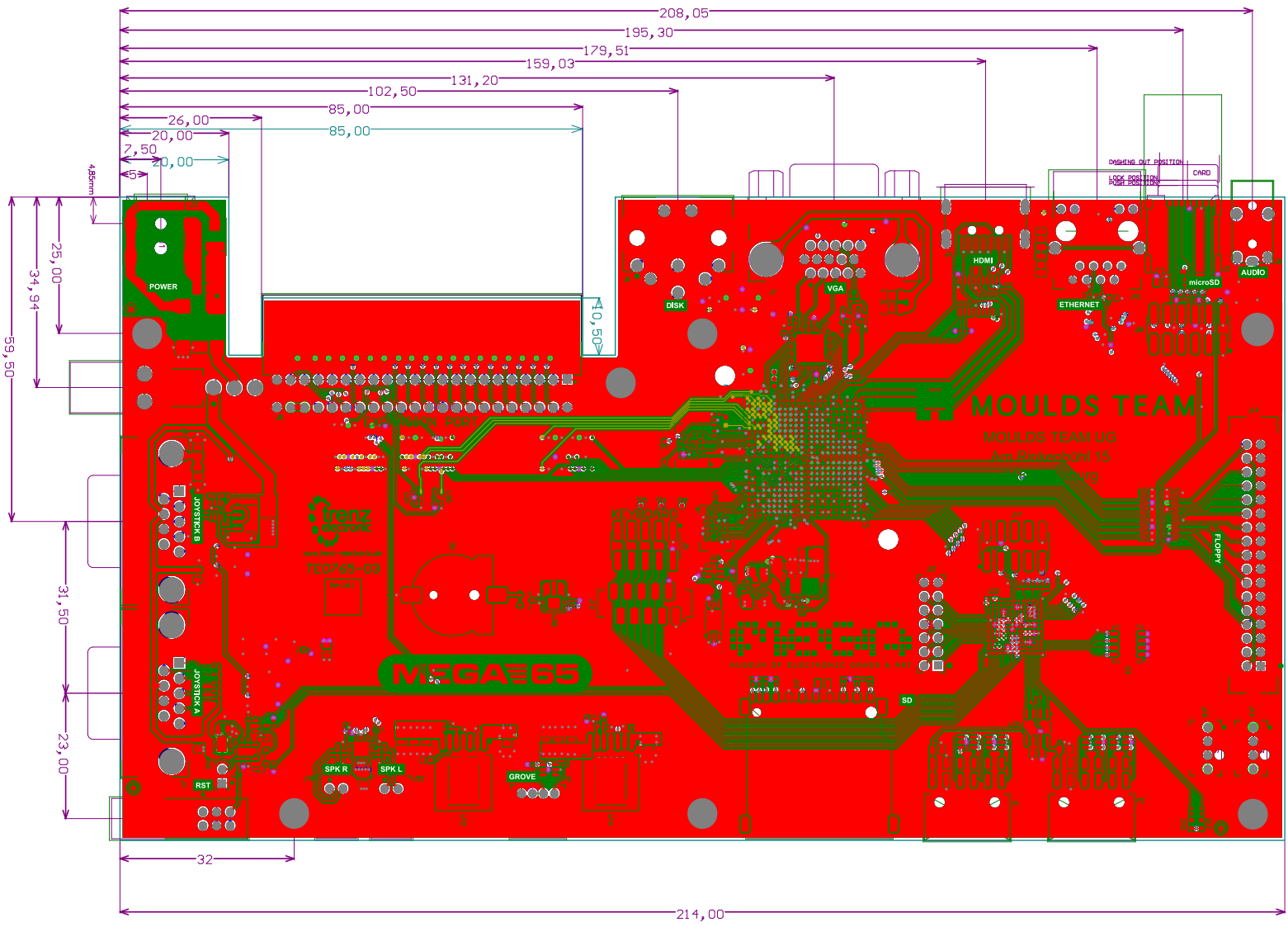
Filename: Revision_Changes.SchDoc		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32
214,00
POWER
DISK
VGA
HDMI
ETHERNET
microSD
AUDIO
CARD
EXPANSION PORT
JOYSTICK B
JOYSTICK A
KEYBOARD
FLOPPY
SD
SPK R
SPK L
GROVE
RST
MOULDS TEAM
MOULDS TEAM UG
Am Rinkenbühl 15
MEGA65
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