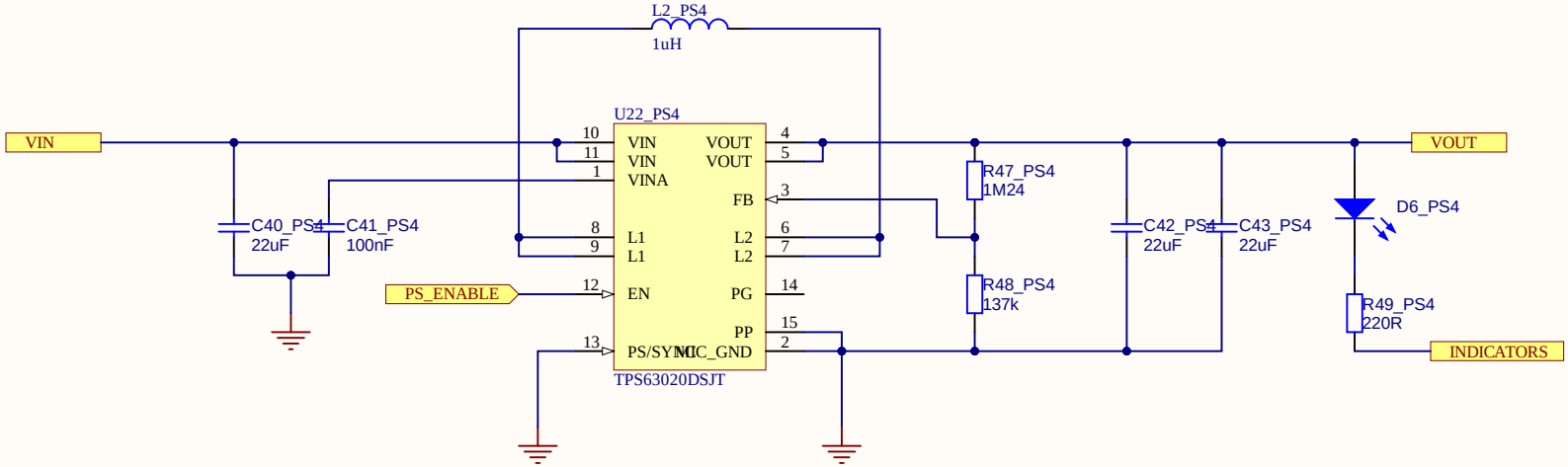
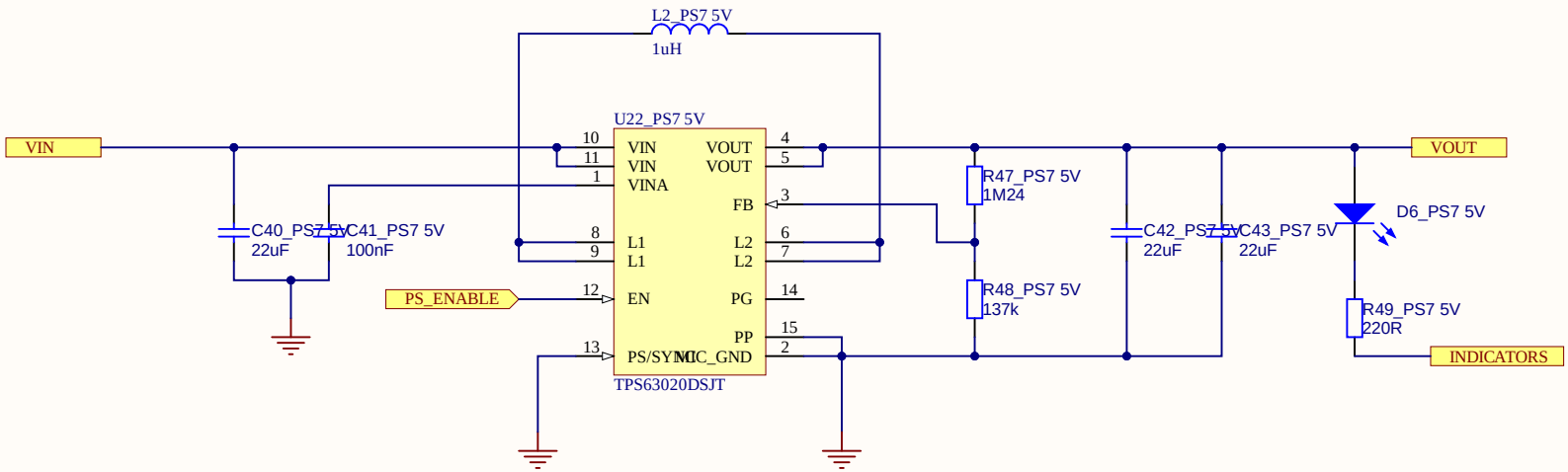
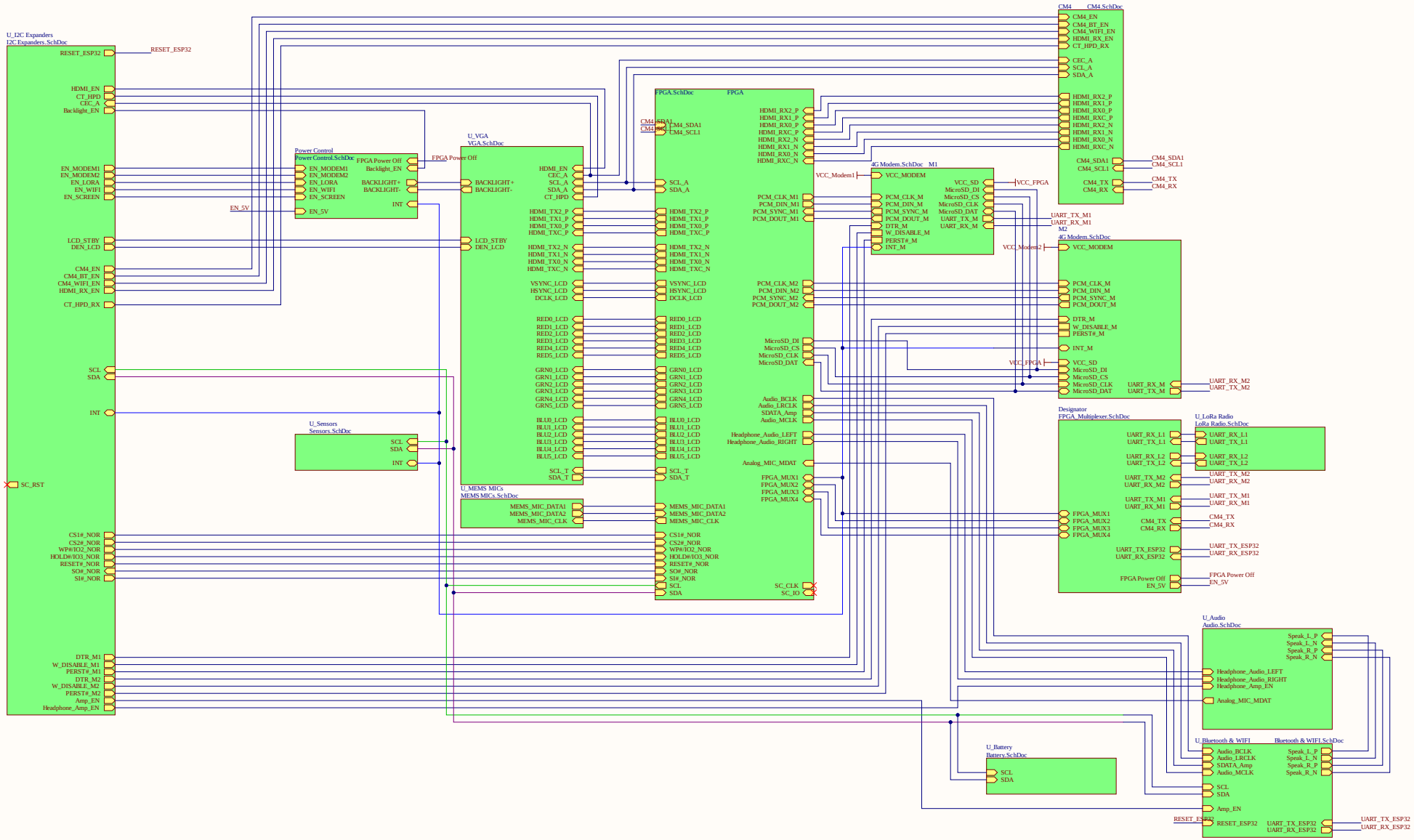


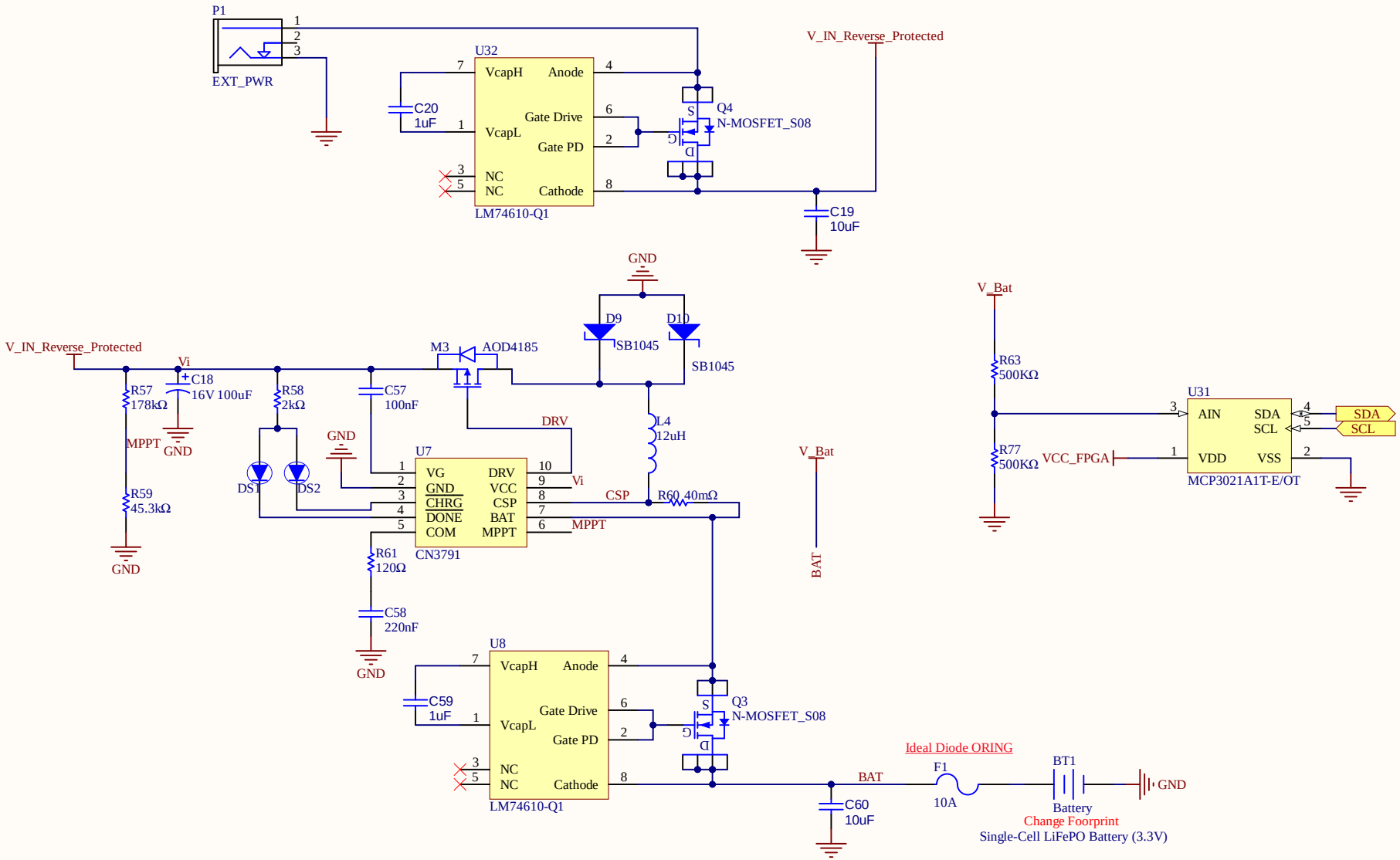
Title		
Size A4	Number	Revision
Date: 2.21.2022		Sheet of
File: D:\projects\..\PowerSupply5V.SchDoc		Drawn By:



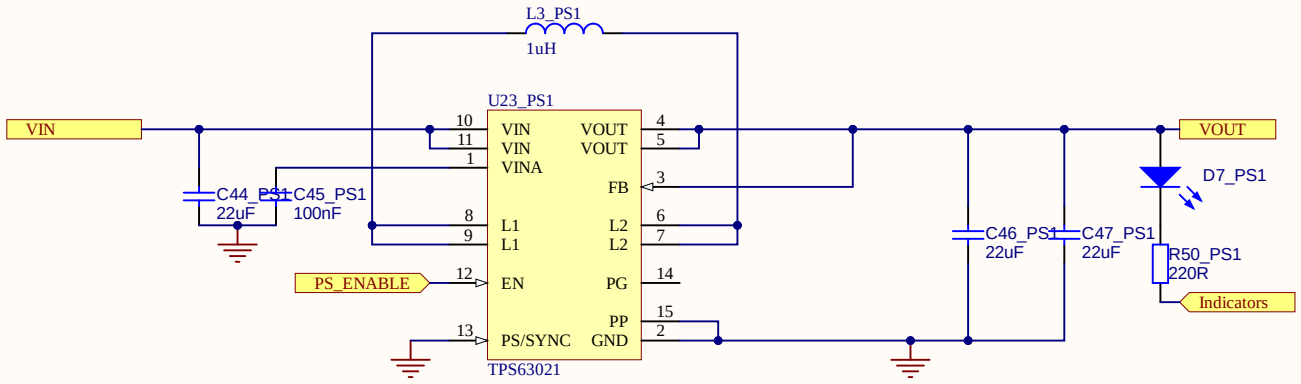
Title		
Size A4	Number	Revision
Date: 2.21.2022		Sheet of
File: D:\projects\..\PowerSupply5V.SchDoc		Drawn By:



Title	*Mega Phone*		*Flinders University College of Science & Engineering Engineering Services Room 3 1284 South Rd SA 5042*
Size: A2	Number: A4284	Revision: 1	
Date: 21.2.2022	Time: 8:55:58	Sheet 1 of 1	
File: D:\projects\Irnas\PCB_designs\Altium\megaphone-r2-nohistory\MEGAphone Overview.SchDoc			

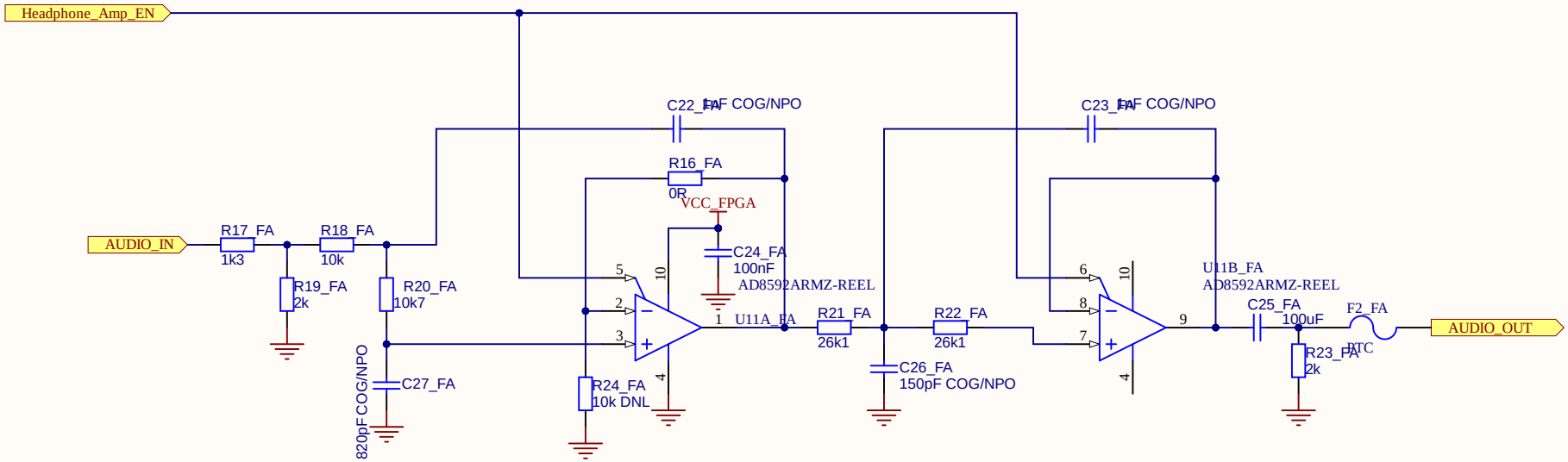


Title	TITLE		Flinders University College of Science & Engineering Engineering Services Room 3.22 1284 South Rd SA 5042
Size: A4	Number: A4	Drawn By: D Kleiss	
Date: 21.2.2022.	Revision: 1	Sheet 1 of 1	
File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\Battery.SchDoc			

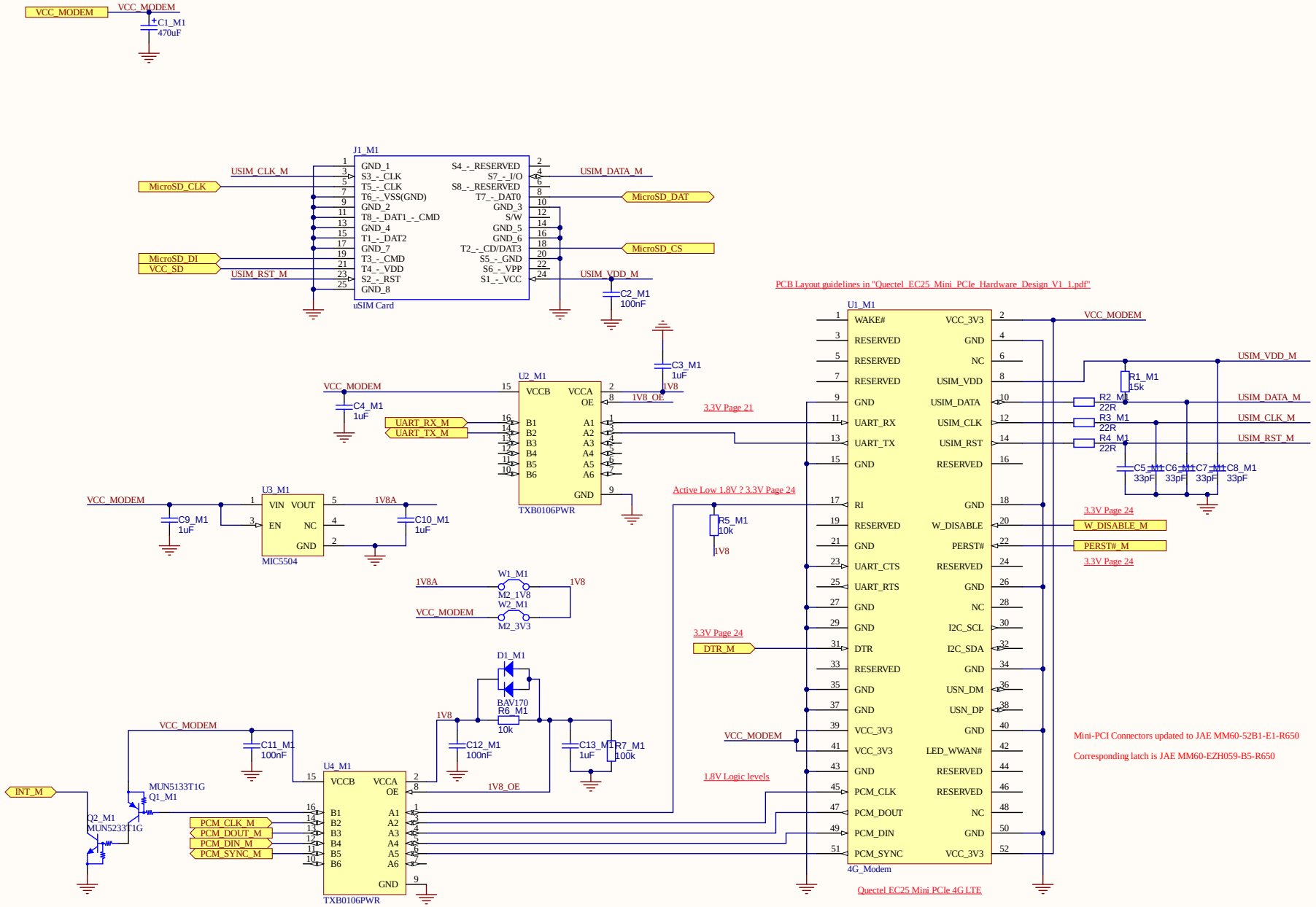


Title **TITLE**			*Flinders University* *College of Science & Engineering* *Engineering Services Room 3.22* *1284 South Rd* *SA 5042*
Size: A4	Number: A4	Drawn By: D Kleiss	
Date: 21.2.2022.	Revision: 1	Sheet 1 of 1	
File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\PowerSupply.SchDoc			

Sallen-Key Butterworth Low Pass 4th Order Filter

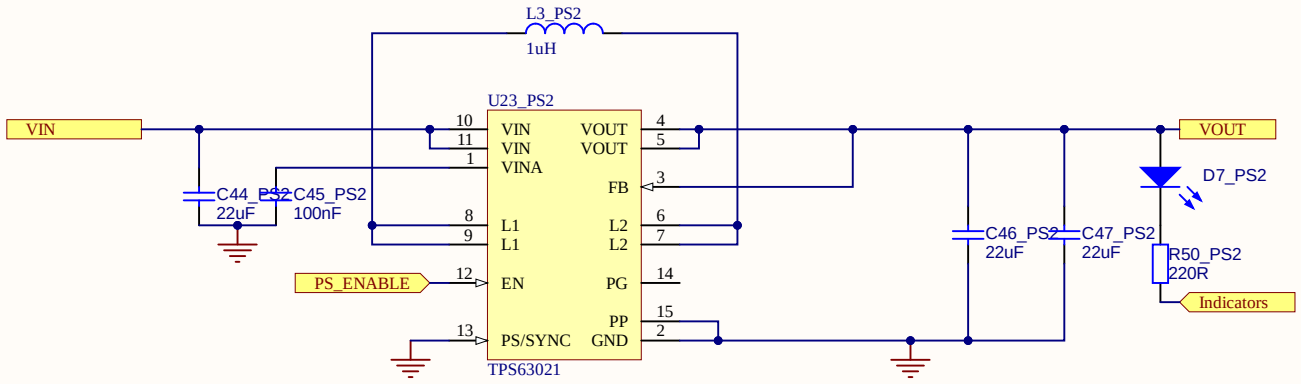


Title **TITLE**			*Flinders University* *College of Science & Engineering* *Engineering Services Room 3.22* *1284 South Rd* *SA 5042*
Size: A4	Number: A4	Drawn By: D Kleiss	
Date: 21.2.2022.	Revision: 1	Sheet 1 of 1	
File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\Headphone Filter.SchDoc			



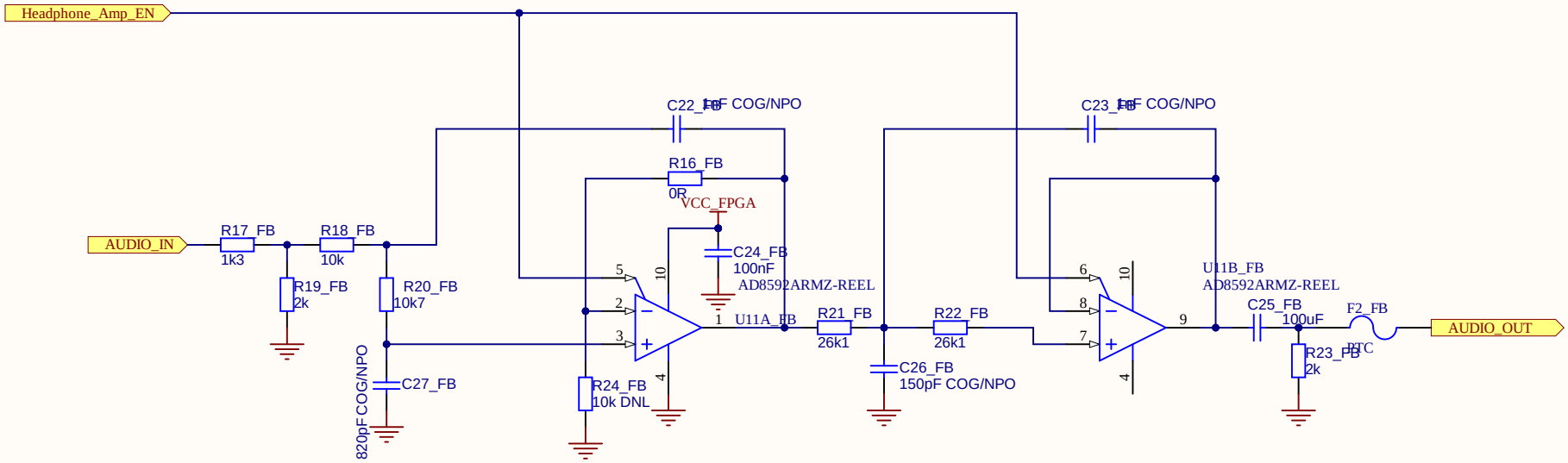
Title	TITLE		Flinders University College of Science & Engineering Engineering Services Room 3.22 Bedford Park SA SA 5042
Size: A3	Number: A4	Drawn By: D Kleiss	
Date: 21.2.2022.	Revision: 1	Sheet 1 of 1	
File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\4G Modem.SchDoc			

6 17
Lachlan McDonald

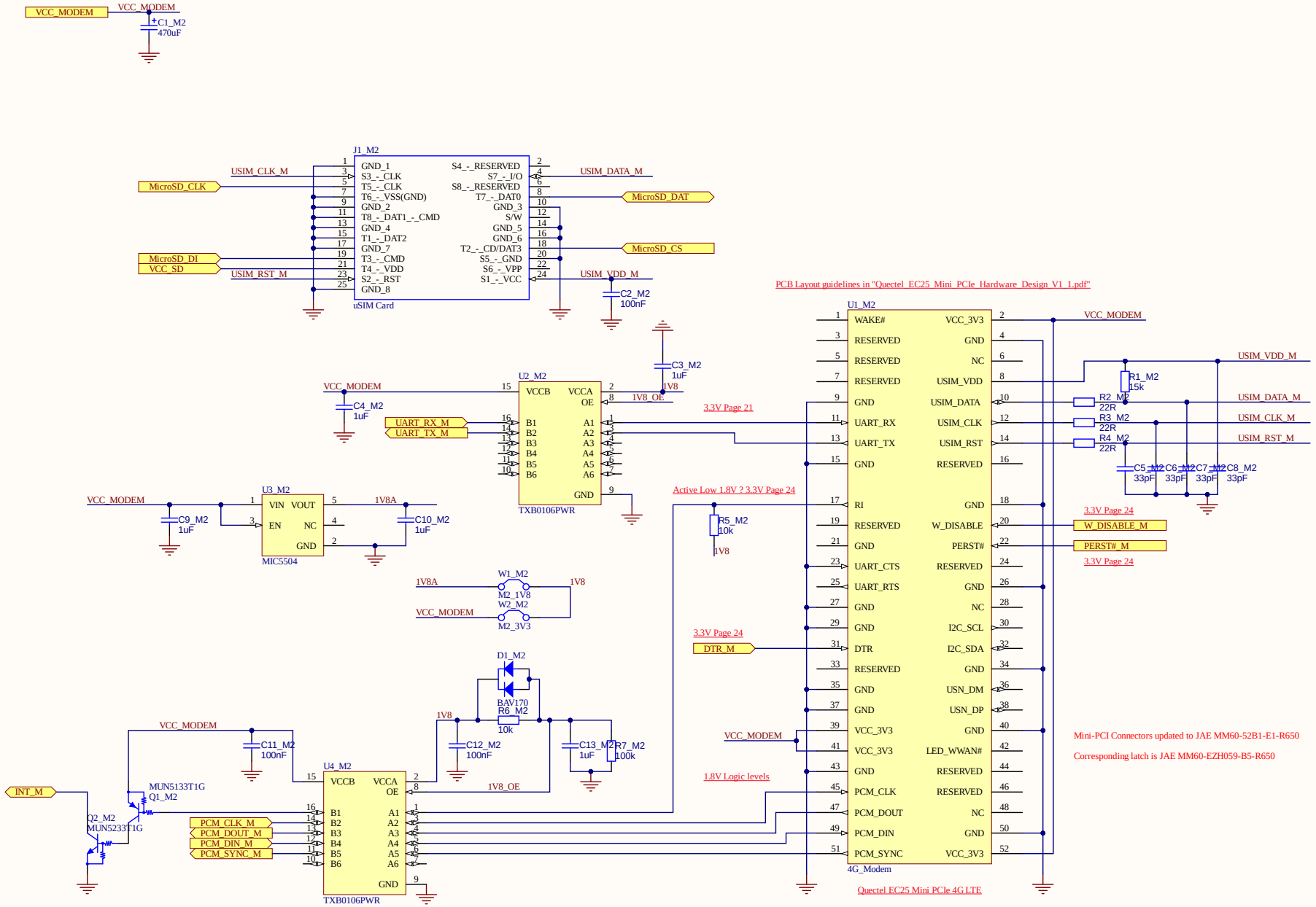


Title **TITLE**			*Flinders University* *College of Science & Engineering* *Engineering Services Room 3.22* *1284 South Rd* *SA 5042*
Size: A4	Number: A4	Drawn By: D Kleiss	
Date: 21.2.2022.	Revision: 1	Sheet 1 of 1	
File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\PowerSupply.SchDoc			

Sallen-Key Butterworth Low Pass 4th Order Filter

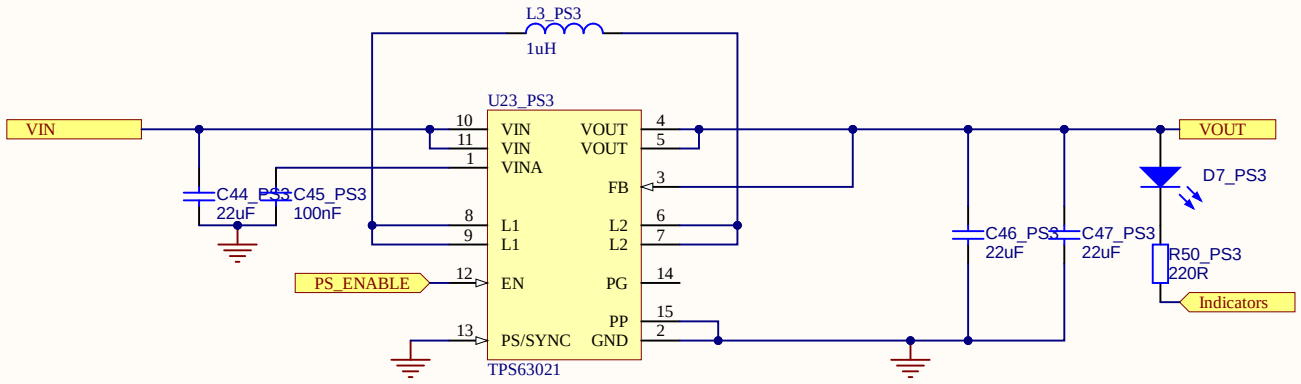


Title	TITLE		Flinders University College of Science & Engineering Engineering Services Room 3.22 1284 South Rd SA 5042
Size: A4	Number: A4	Drawn By: D Kleiss	
Date: 21.2.2022.	Revision: 1	Sheet 1 of 1	
File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\Headphone Filter.SchDoc			

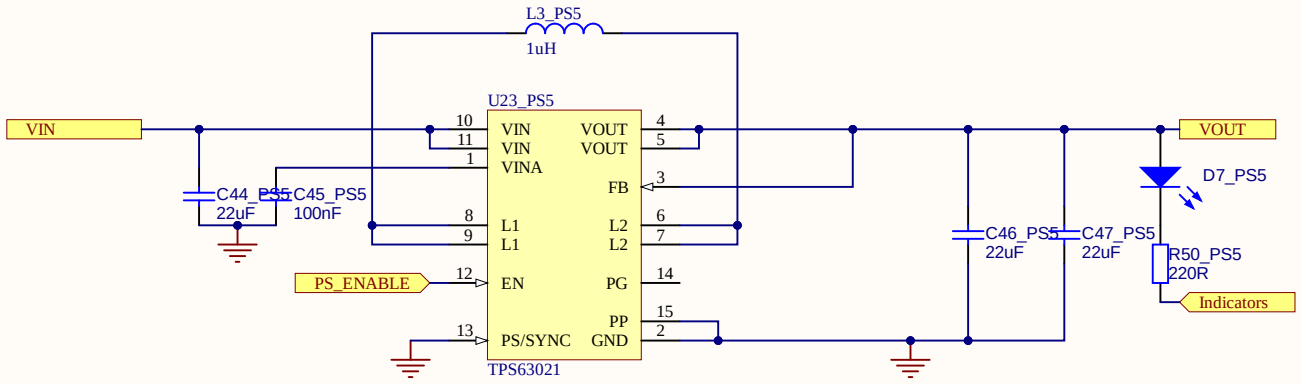


Title	TITLE		Flinders University College of Science & Engineering Engineering Services Room 3.22 Bedford Park SA SA 5042
Size: A3	Number: A4	Drawn By: D Kleiss	
Date: 21.2.2022.	Revision: 1	Sheet 1 of 1	
File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\4G Modem.SchDoc			

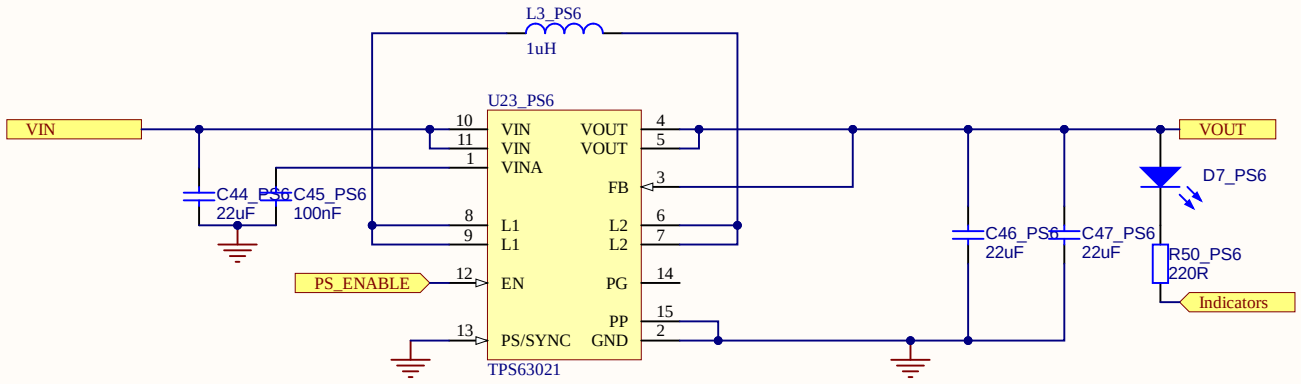
6 17
Lachlan McDonald



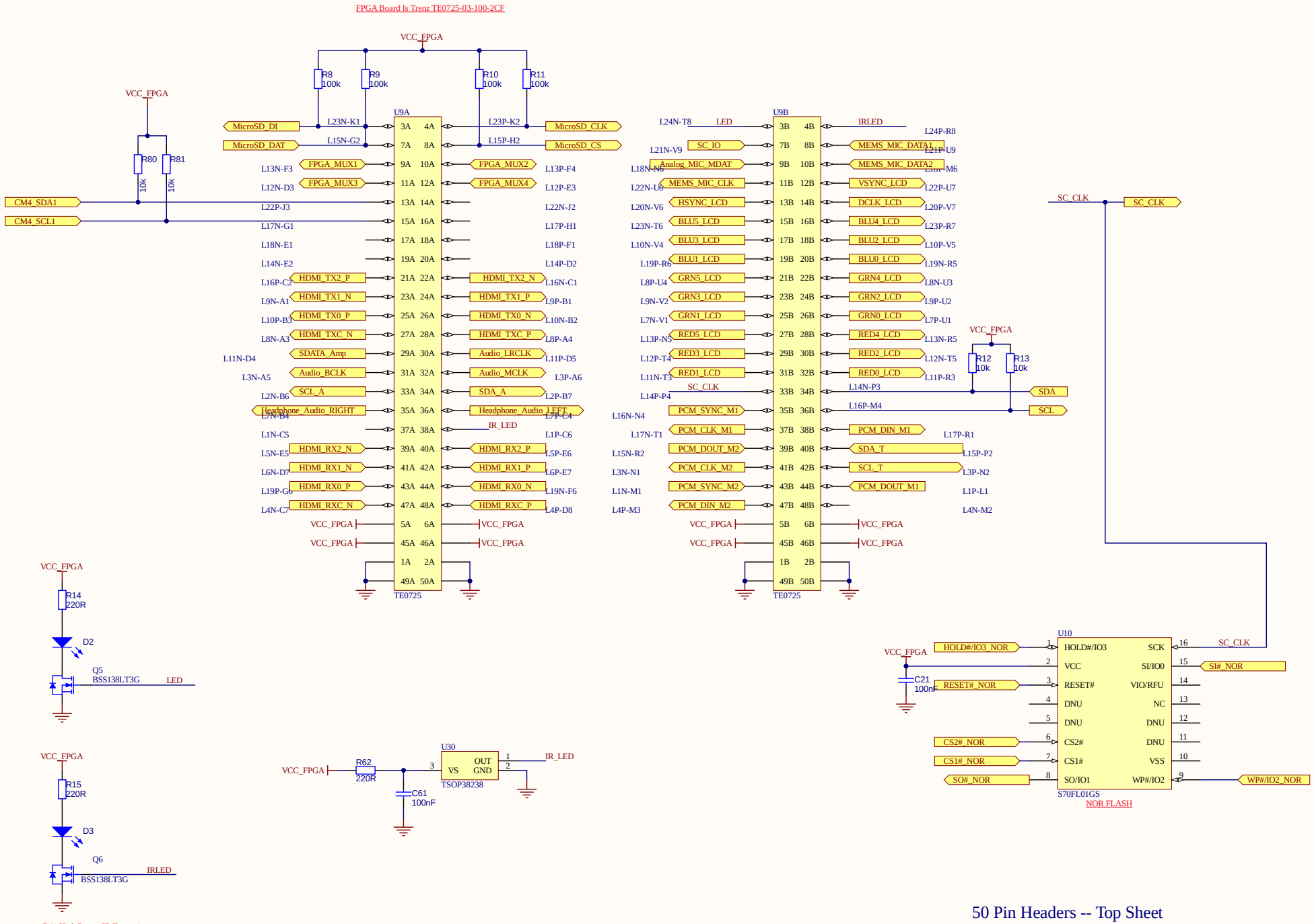
Title **TITLE**			*Flinders University* *College of Science & Engineering* *Engineering Services Room 3.22* *1284 South Rd* *SA 5042*
Size: A4	Number: A4	Drawn By: D Kleiss	
Date: 21.2.2022.	Revision: 1	Sheet 1 of 1	
File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\PowerSupply.SchDoc			



Title **TITLE**			*Flinders University* *College of Science & Engineering* *Engineering Services Room 3.22* *1284 South Rd* *SA 5042*
Size: A4	Number: A4	Drawn By: D Kleiss	
Date: 21.2.2022.	Revision: 1	Sheet 1 of 1	
File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\PowerSupply.SchDoc			



Title **TITLE**			*Flinders University* *College of Science & Engineering* *Engineering Services Room 3.22* *1284 South Rd* *SA 5042*
Size: A4	Number: A4	Drawn By: D Kleiss	
Date: 21.2.2022.	Revision: 1	Sheet 1 of 1	
File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\PowerSupply.SchDoc			



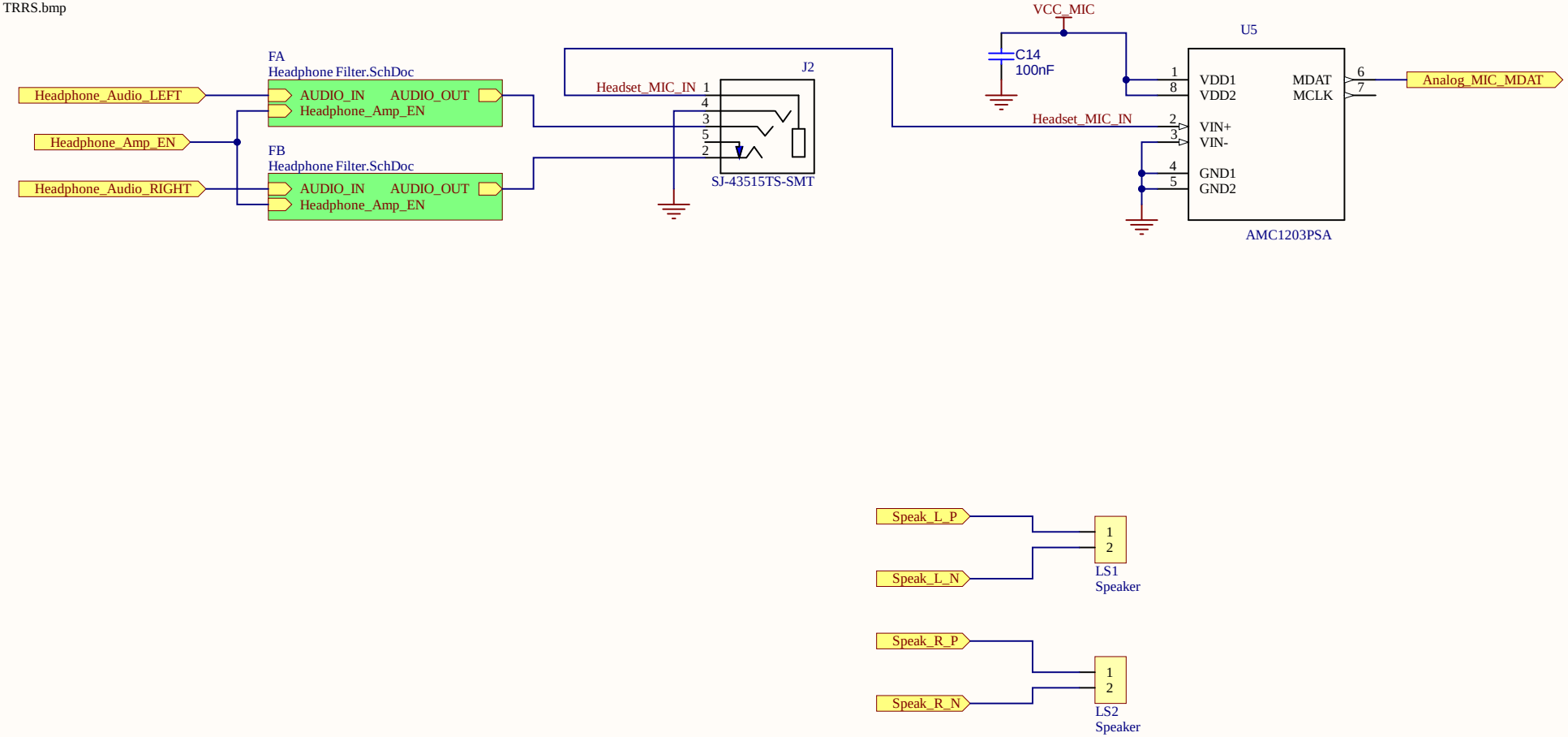
50 Pin Headers -- Top Sheet

Title	*MEGAPHONE FPGA*		
Size: A3	Number: *	Drawn By: *	
Date: 21.2.2022.	Revision: *	Sheet 2 of *	
File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\FPGA.SchDoc			

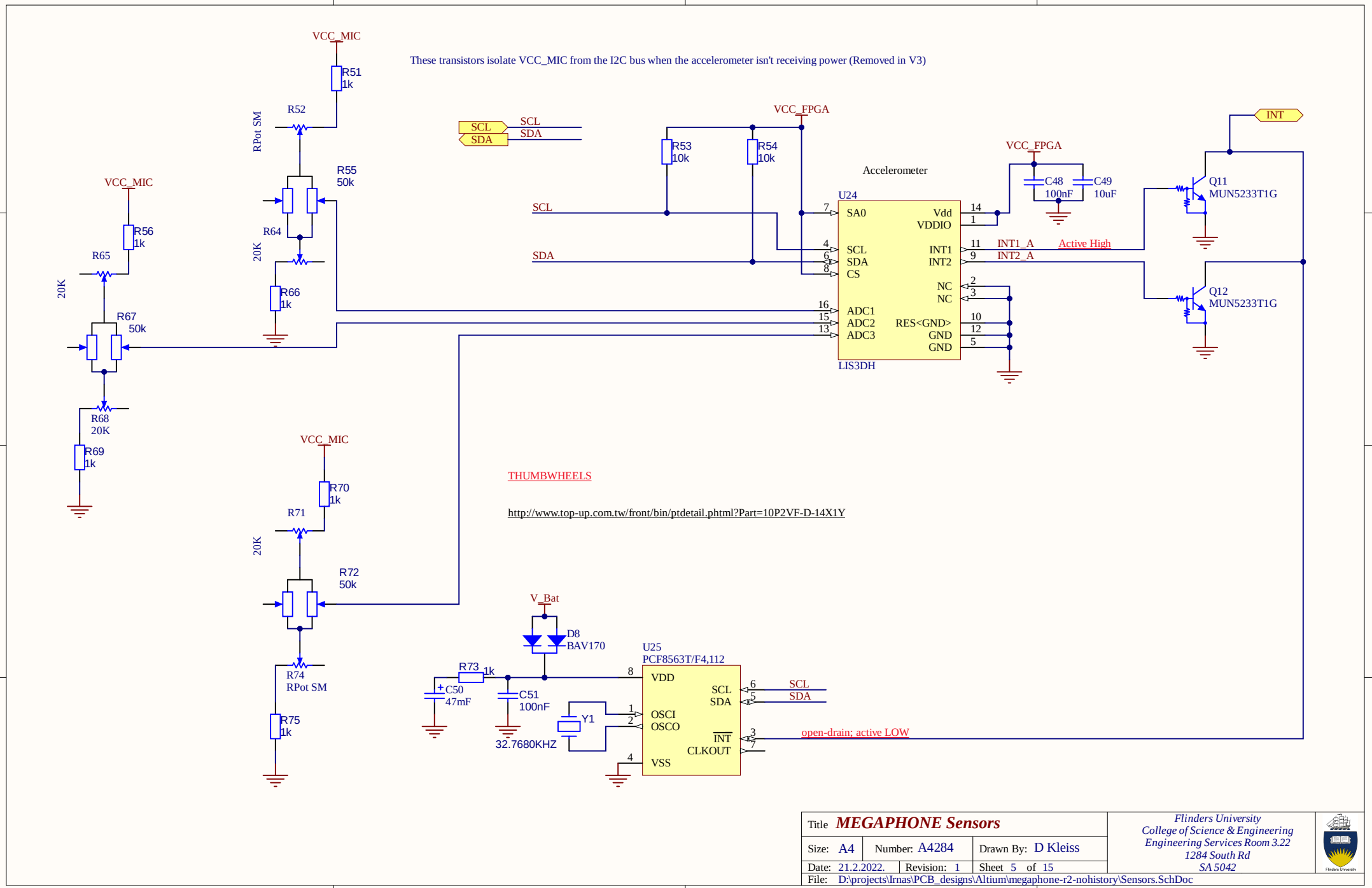
Bedford Park SA

Lachlan McDonald

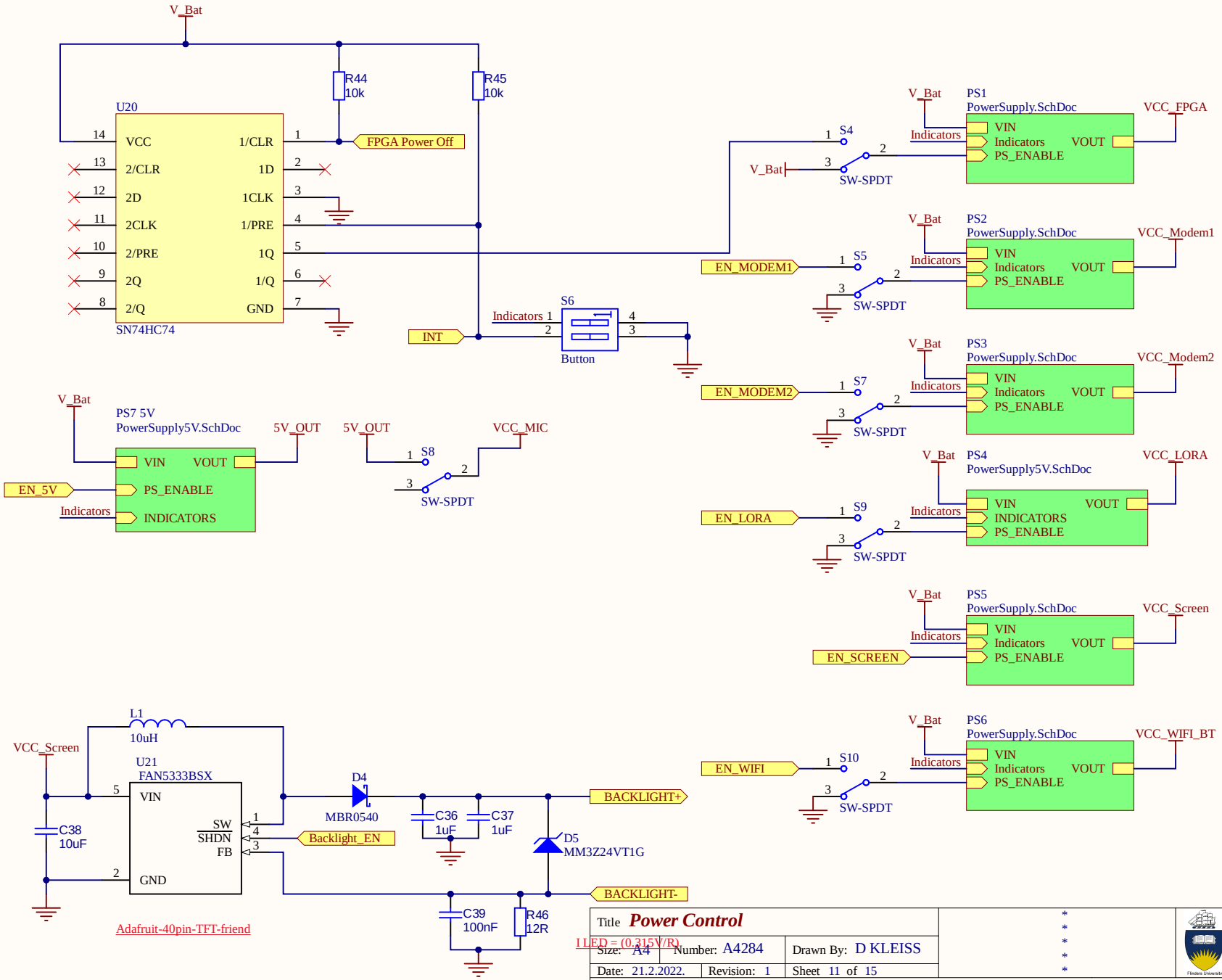
Cannot open file S:\CSE-CSEM esg\Electro Technical Team\Superceded\Documents\Altium\Step Models\Connectors\CUI\CUI_SJ-43515TS-SMT-TR\Mating TRRS.bmp

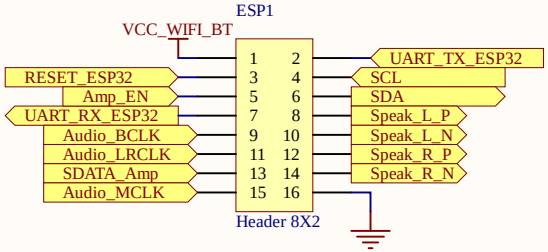


Title **AUDIO**			* * * * * 7 17
Size: A4	Number: *	Drawn By: D KLEISS	
Date: 21.2.2022.	Revision: 1	Sheet 3 of 15	
File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\Audio.SchDoc			

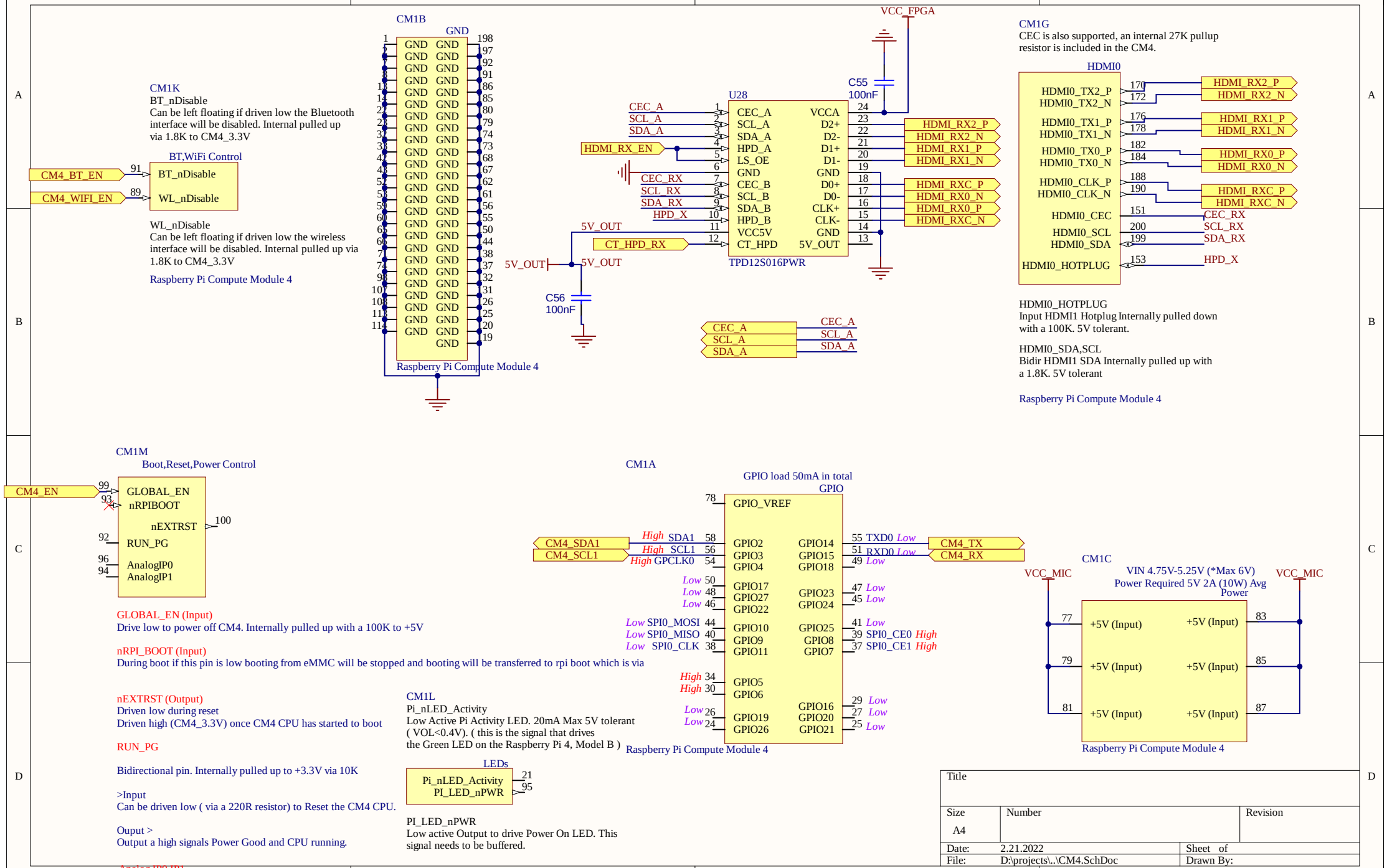


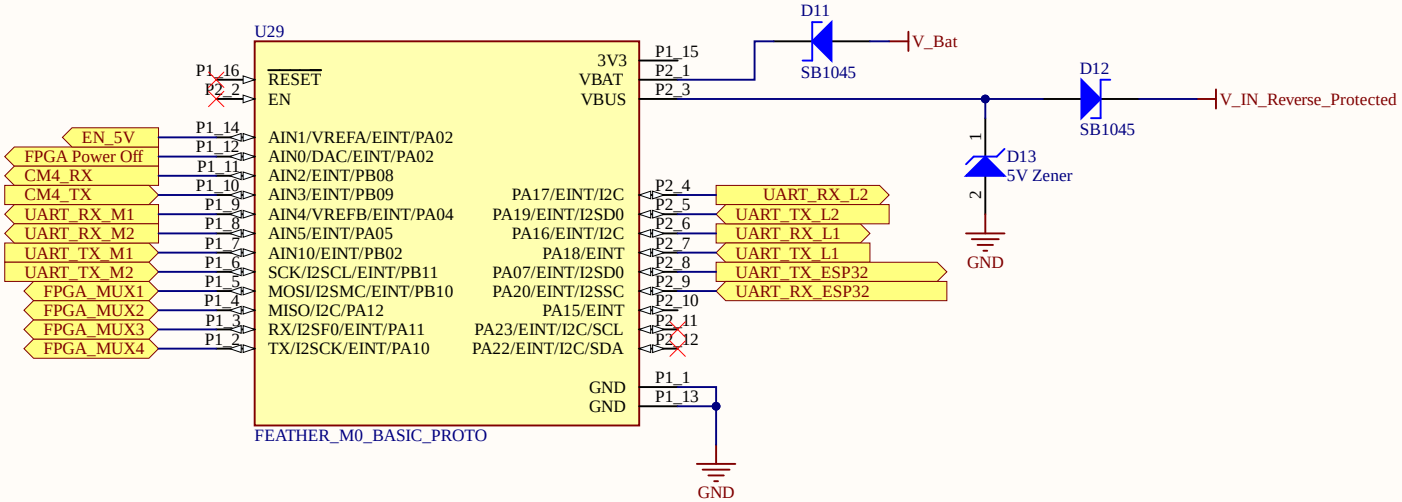
Title	**MEGAPHONE Sensors**		*Flinders University* *College of Science & Engineering* *Engineering Services Room 3.22* *1284 South Rd* *SA 5042*
Size: A4	Number: A4284	Drawn By: D Kleiss	
Date: 21.2.2022.	Revision: 1	Sheet 5 of 15	
File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\Sensors.SchDoc			


V_Bat
R44
10k
R45
10k
U20
SN74HC74
VCC
2/CLR
2D
2CLK
2/PRE
2Q
2/Q
1/CLR
1D
1CLK
1/PRE
1Q
1/Q
GND
FPGA Power Off
INT
Indicators
S6
Button
PS1
PowerSupply.SchDoc
VIN
Indicators
PS_ENABLE
VOUT
VCC_FPGA
S4
SW-SPDT
PS2
VCC_Modem1
EN_MODEM1
S5
PS3
VCC_Modem2
EN_MODEM2
S7
PS4
VCC_LORA
EN_LORA
S9
PS5
VCC_Screen
EN_SCREEN
PS6
VCC_WIFI_BT
EN_WIFI
S10
PS7 5V
PowerSupply5V.SchDoc
5V_OUT
EN_5V
INDICATORS
S8
VCC_MIC
L1
10uH
U21
FAN5333BSX
SW
SHDN
FB
C38
10uF
D4
MBR0540
C36
1uF
C37
1uF
Backlight_EN
BACKLIGHT+
D5
MM3Z24VT1G
BACKLIGHT-
C39
100nF
R46
12R
Adafruit-40pin-TFT-friend
I LED = (0.315V/R)
Title
Power Control
Size: A4
Number: A4284
Drawn By: D KLEISS
Date: 21.2.2022.
Revision: 1
Sheet 11 of 15
File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\Power Control.SchDoc

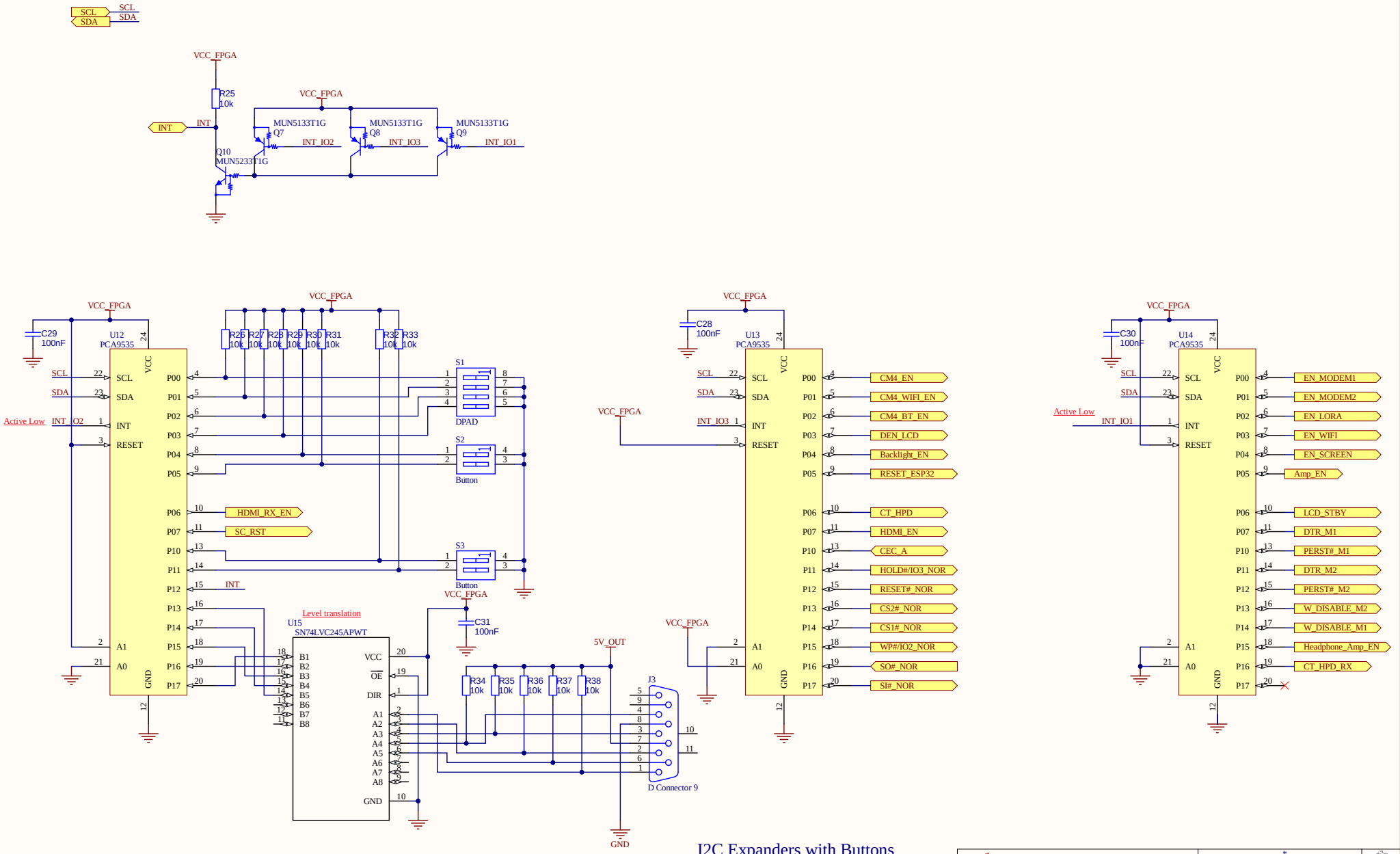


Title	***BLUETOOTH & WiFi***		* * * * * 9 17
Size: A4	Number: *	Drawn By: *	
Date: 21.2.2022.	Revision: *	Sheet * of *	
File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\Bluetooth & WIFI.SchDoc			Lachlan McDonald


CM1K
BT_nDisable
Can be left floating if driven low the Bluetooth interface will be disabled. Internal pulled up via 1.8K to CM4_3.3V
BT,WiFi Control
CM4_BT_EN
CM4_WIFI_EN
BT_nDisable
WL_nDisable
WL_nDisable
Can be left floating if driven low the wireless interface will be disabled. Internal pulled up via 1.8K to CM4_3.3V
Raspberry Pi Compute Module 4
CM1B
GND
Raspberry Pi Compute Module 4
VCC_FPGA
C55
100nF
U28
CEC_A
SCL_A
SDA_A
HDMI_RX_EN
CEC_RX
SCL_RX
SDA_RX
HPD_X
5V_OUT
CT_HPD_RX
CEC_A
SCL_A
SDA_A
HDMI_RX2_P
HDMI_RX2_N
HDMI_RX1_P
HDMI_RX1_N
HDMI_RXC_P
HDMI_RX0_N
HDMI_RX0_P
HDMI_RXC_N
TPD12S016PWR
C56
100nF
CM1G
CEC is also supported, an internal 27K pullup resistor is included in the CM4.
HDMI0
HDMI0_TX2_P
HDMI0_TX2_N
HDMI0_TX1_P
HDMI0_TX1_N
HDMI0_TX0_P
HDMI0_TX0_N
HDMI0_CLK_P
HDMI0_CLK_N
HDMI0_CEC
HDMI0_SCL
HDMI0_SDA
HDMI0_HOTPLUG
HDMI0_HOTPLUG
Input HDMI1 Hotplug Internally pulled down with a 100K. 5V tolerant.
HDMI0_SDA,SCL
Bidir HDMI1 SDA Internally pulled up with a 1.8K. 5V tolerant
Raspberry Pi Compute Module 4
CM1M
Boot,Reset,Power Control
CM4_EN
GLOBAL_EN
nRPIBOOT
nEXTRST
RUN_PG
AnalogIP0
AnalogIP1
GLOBAL_EN (Input)
Drive low to power off CM4. Internally pulled up with a 100K to +5V
nRPI_BOOT (Input)
During boot if this pin is low booting from eMMC will be stopped and booting will be transferred to rpi boot which is via
nEXTRST (Output)
Driven low during reset
Driven high (CM4_3.3V) once CM4 CPU has started to boot
RUN_PG
Bidirectional pin. Internally pulled up to +3.3V via 10K
>Input
Can be driven low (via a 220R resistor) to Reset the CM4 CPU.
Ouput >
Output a high signals Power Good and CPU running.
Analog IP0,IP1
Analog input of the MAX7704. Typically connected to CC pin of Type C power connector
Raspberry Pi Compute Module 4
CM1A
GPIO load 50mA in total
GPIO
GPIO_VREF
CM4_SDA1
CM4_SCL1
SDA1
SCL1
GPCLK0
GPIO2
GPIO3
GPIO4
GPIO17
GPIO27
GPIO22
SPI0_MOSI
SPI0_MISO
SPI0_CLK
GPIO10
GPIO9
GPIO11
GPIO5
GPIO6
GPIO19
GPIO26
GPIO14
GPIO15
GPIO18
GPIO23
GPIO24
GPIO25
GPIO8
GPIO7
GPIO16
GPIO20
GPIO21
TXD0
RXD0
CM4_TX
CM4_RX
SPI0_CE0
SPI0_CE1
Raspberry Pi Compute Module 4
CM1L
Pi_nLED_Activity
Low Active Pi Activity LED. 20mA Max 5V tolerant (VOL<0.4V). (this is the signal that drives the Green LED on the Raspberry Pi 4, Model B)
LEDs
Pi_nLED_Activity
PI_LED_nPWR
PI_LED_nPWR
Low active Output to drive Power On LED. This signal needs to be buffered.
Raspberry Pi Compute Module 4
CM1C
VCC_MIC
VIN 4.75V-5.25V (*Max 6V)
Power Required 5V 2A (10W) Avg Power
VCC_MIC
+5V (Input)
Raspberry Pi Compute Module 4
Title
Size
A4
Number
Revision
Date: 2.21.2022
Sheet of
File: D:\projects\..\CM4.SchDoc
Drawn By:



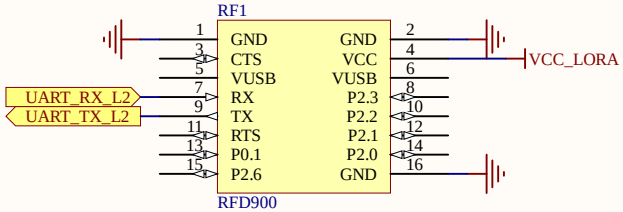
Title		
Size A4	Number	Revision
Date: 2.21.2022	Sheet of	
File: D:\projects\..\FPGA_Multiplexer.SchDoc	Drawn By:	

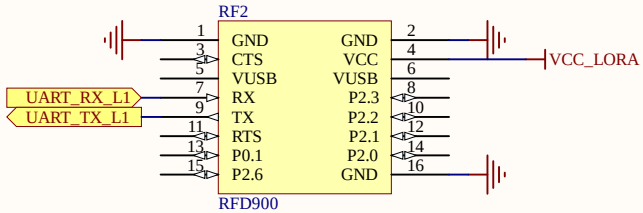


I2C Expanders with Buttons

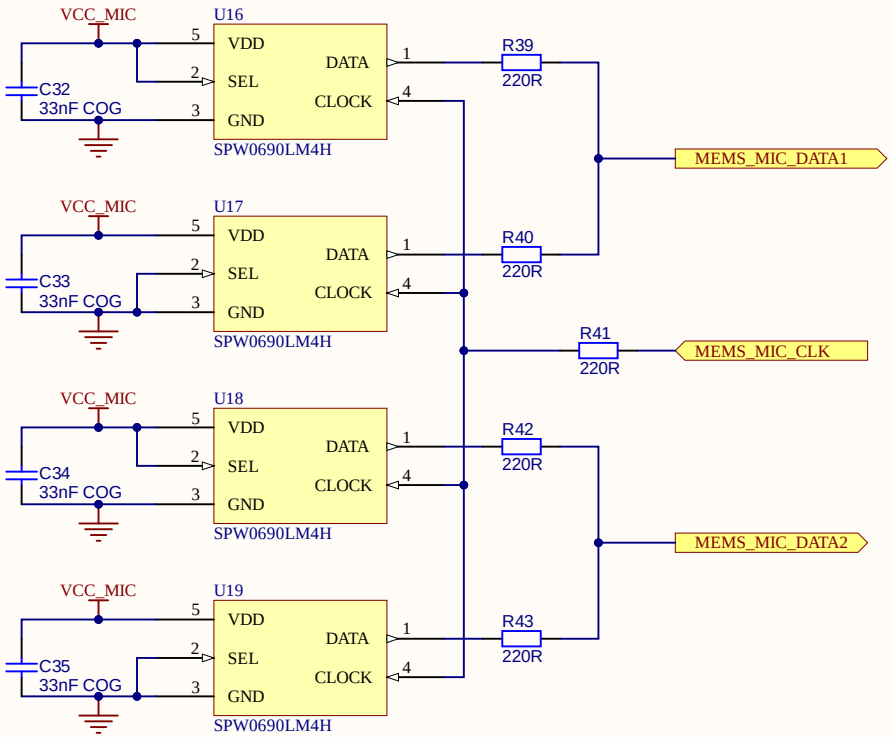
Title *			* * * Bedford Park SA *
Size: A3	Number: *	Drawn By: *	
Date: 21.2.2022.	Revision: *	Sheet * of *	
File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\I2C Expanders.SchDoc			

Lachlan Mitchell

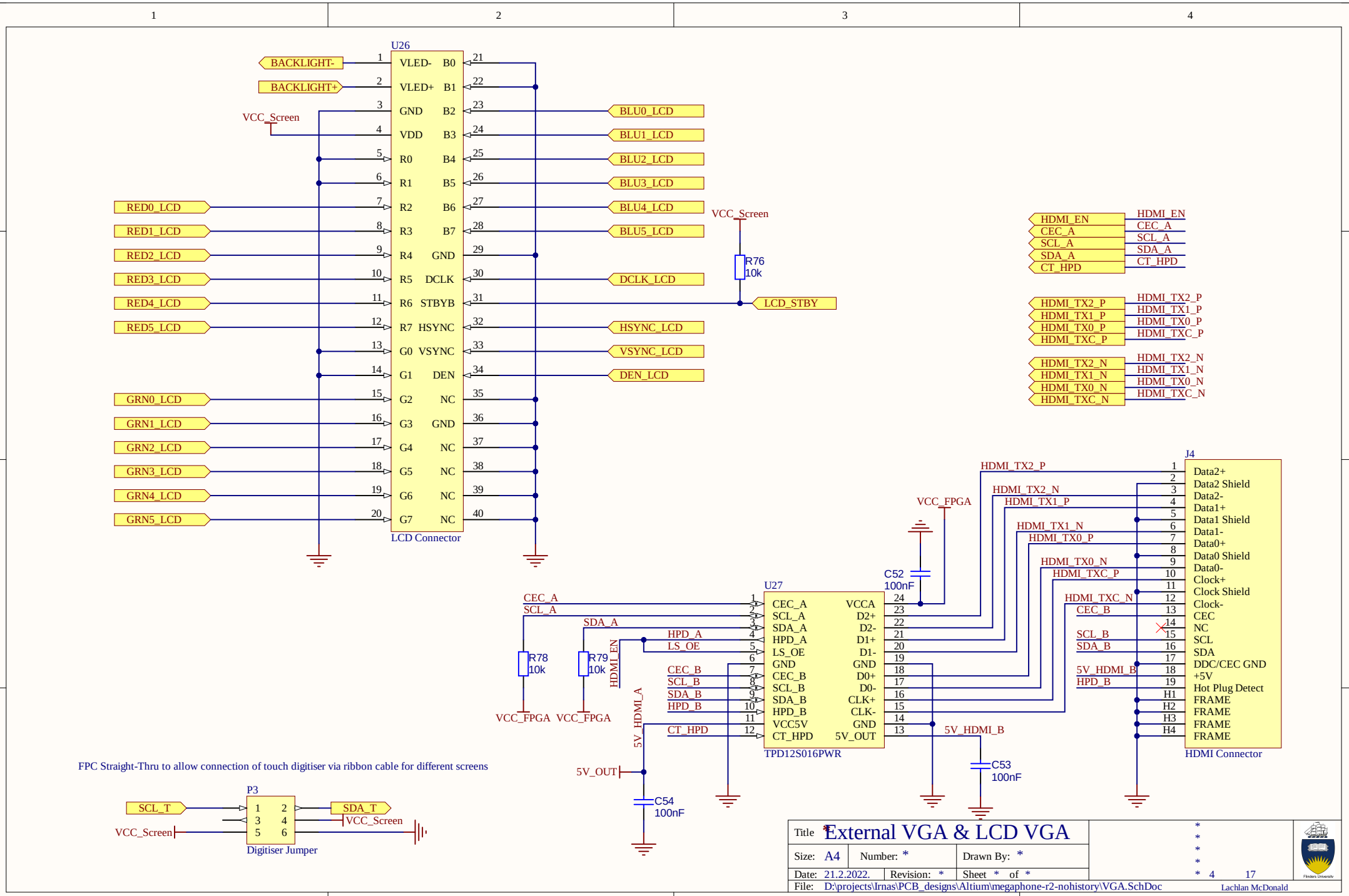


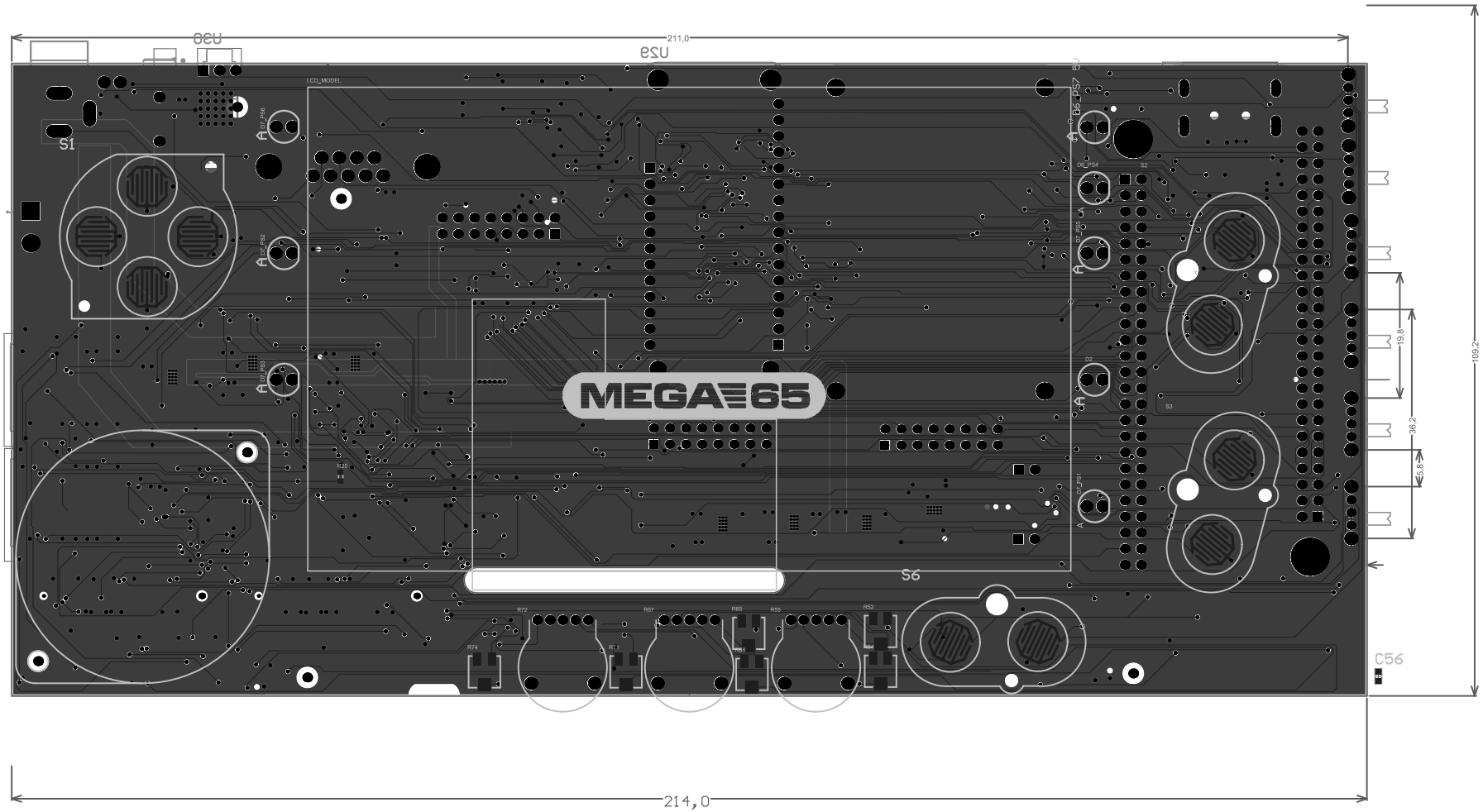


Title * LoRa Modules			* * * * *
Size: A4	Number: *	Drawn By: *	
Date: 21.2.2022.	Revision: *	Sheet * of *	11 17
File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\LoRa Radio.SchDoc			Lachlan McDonald



Title *			* * * * *
Size: A4	Number: *	Drawn By: *	
Date: 21.2.2022.	Revision: *	Sheet * of *	16 17
File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\MEMS MICs.SchDoc			Lachlan McDonald


U26
BACKLIGHT-
BACKLIGHT+
VCC_Screen
VLED- B0
VLED+ B1
GND B2
VDD B3
R0 B4
R1 B5
R2 B6
R3 B7
R4 GND
R5 DCLK
R6 STBYB
R7 HSYNC
G0 VSYNC
G1 DEN
G2 NC
G3 GND
G4 NC
G5 NC
G6 NC
G7 NC
BLU0_LCD
BLU1_LCD
BLU2_LCD
BLU3_LCD
BLU4_LCD
BLU5_LCD
DCLK_LCD
LCD_STBY
HSYNC_LCD
VSYNC_LCD
DEN_LCD
RED0_LCD
RED1_LCD
RED2_LCD
RED3_LCD
RED4_LCD
RED5_LCD
GRN0_LCD
GRN1_LCD
GRN2_LCD
GRN3_LCD
GRN4_LCD
GRN5_LCD
LCD Connector
R76
10k
HDMI_EN
CEC_A
SCL_A
SDA_A
CT_HPD
HDMI_TX2_P
HDMI_TX1_P
HDMI_TX0_P
HDMI_TXC_P
HDMI_TX2_N
HDMI_TX1_N
HDMI_TX0_N
HDMI_TXC_N
J4
Data2+
Data2 Shield
Data2-
Data1+
Data1 Shield
Data1-
Data0+
Data0 Shield
Data0-
Clock+
Clock Shield
Clock-
CEC
NC
SCL
SDA
DDC/CEC GND
+5V
Hot Plug Detect
FRAME
HDMI Connector
VCC_FPGA
C52
100nF
U27
VCCA
D2+
D2-
D1+
D1-
GND
D0+
D0-
CLK+
CLK-
5V_OUT
VCC5V
HPD_A
LS_OE
HPD_B
R78
10k
R79
10k
5V_HDMI_A
5V_HDMI_B
C53
100nF
C54
100nF
TPD12S016PWR
FPC Straight-Thru to allow connection of touch digitiser via ribbon cable for different screens
P3
SCL_T
SDA_T
Digitiser Jumper
Title External VGA & LCD VGA
Size: A4
Number: *
Drawn By: *
Date: 21.2.2022.
Revision: *
Sheet * of *
File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\VGA.SchDoc
Lachlan McDonald


211,0
214,0
109,2
19,8
36,2
5,8
LCD_MODEL
MEGA65
S1
S6
C56