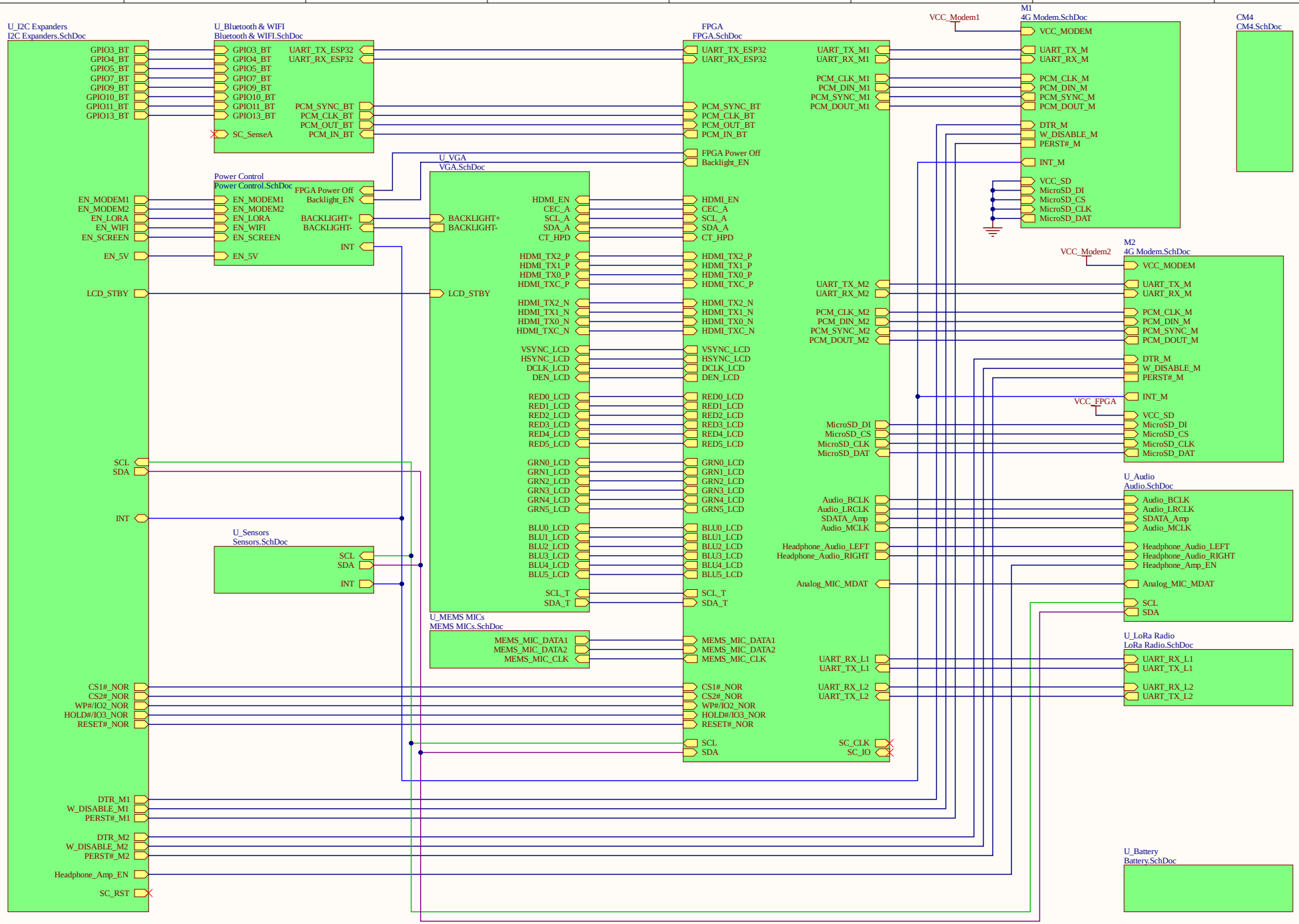
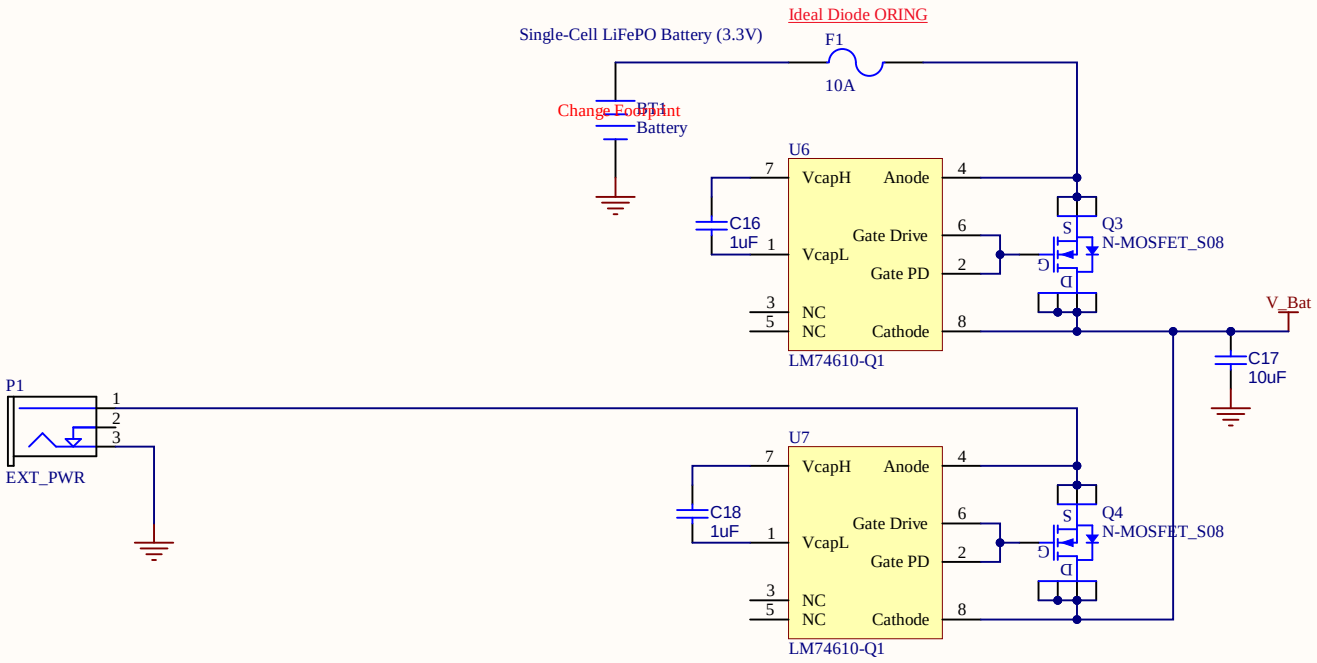
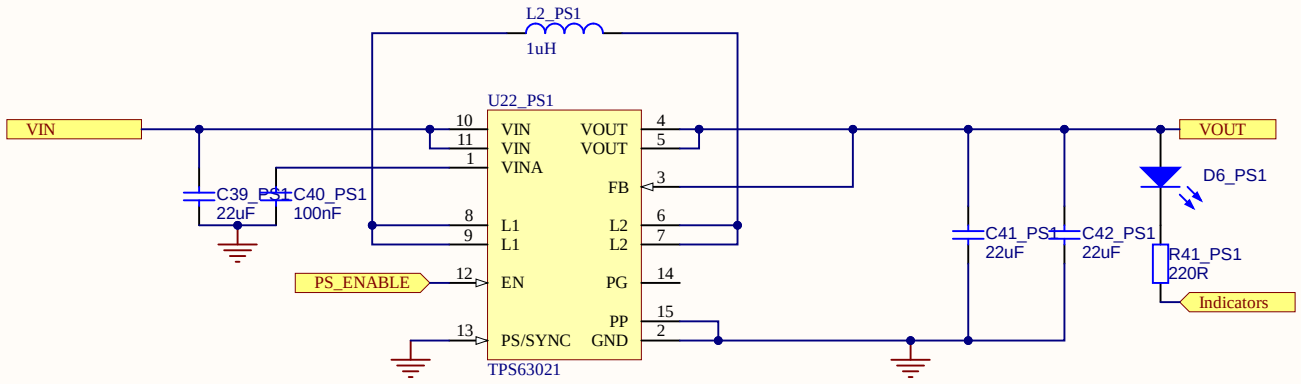



| | | | |
|---|---|---|---|
| Title | **Mega Phone** | | *Flinders University*<br>*College of Science & Engineering*<br>*Engineering Services Room 3.22*<br>*Bedford Park SA*<br>*SA 5042* |
| Size: A3 | Number: A4284 | Drawn By: D Kleiss | |
| Date: 10.3.2021. | Revision: 1 | Sheet 1 of 1 | |
| File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\MEGAphone Overview.SchDoc | | | |

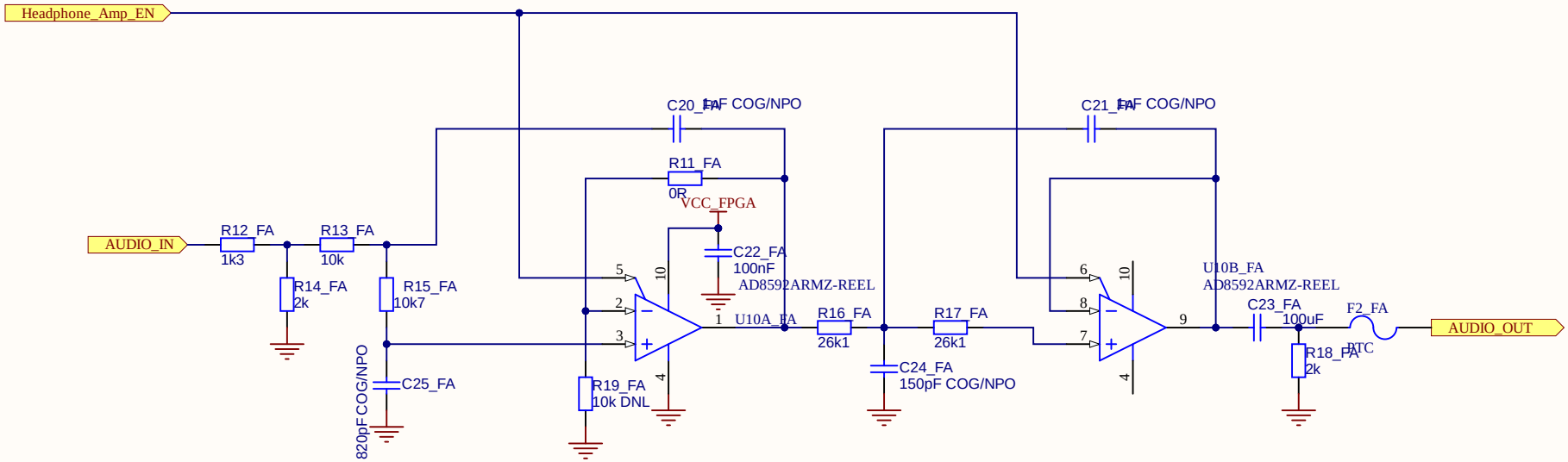



| | | | |
|---|---|---|---|
| Title | TITLE | | Flinders University<br>College of Science & Engineering<br>Engineering Services Room 3.22<br>1284 South Rd<br>SA 5042 |
| Size: A4 | Number: A4 | Drawn By: D Kleiss | |
| Date: 10.3.2021. | Revision: 1 | Sheet 1 of 1 | |
| File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\Battery.SchDoc | | | |

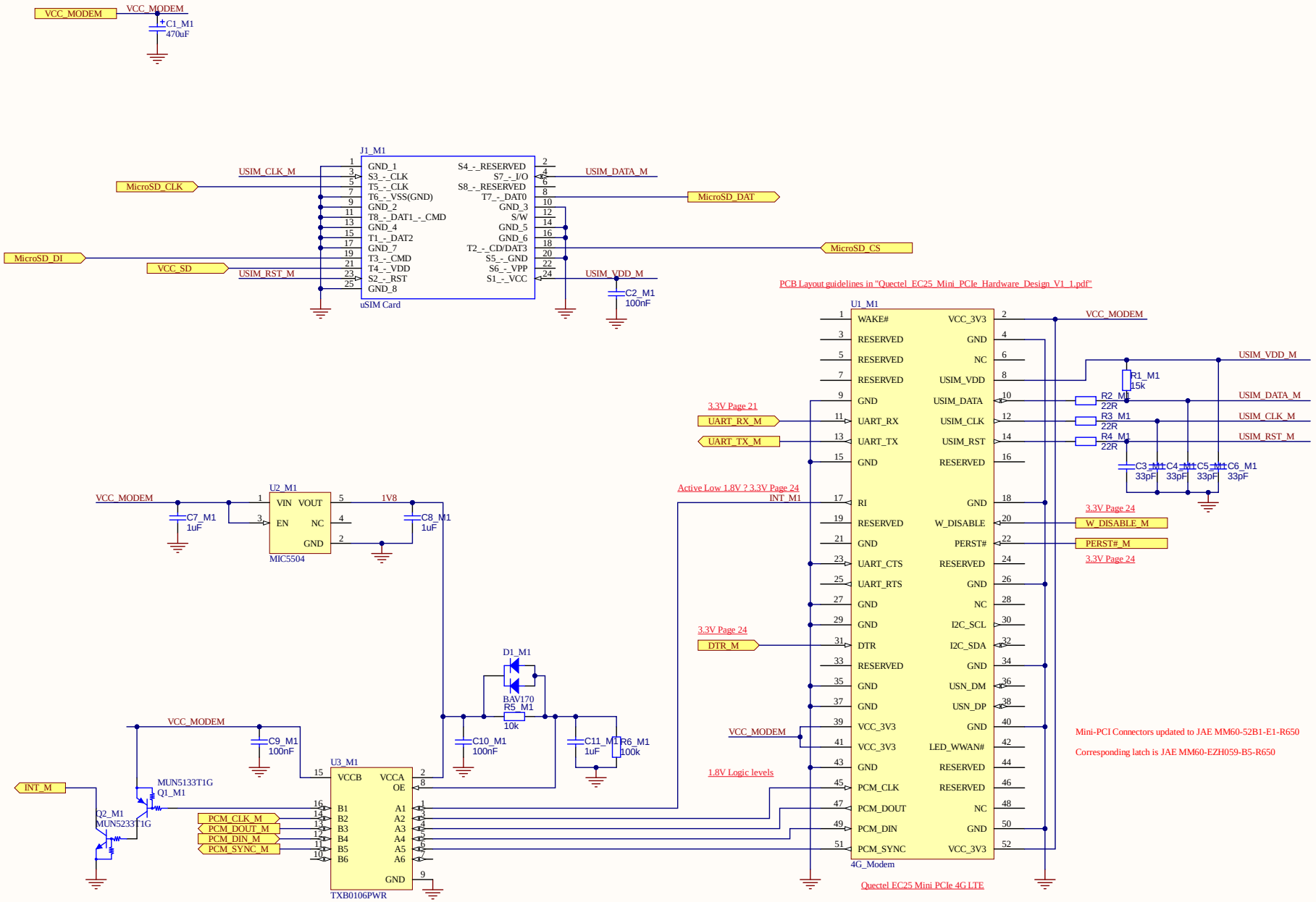



| | | | |
|---|---|---|---|
| Title **TITLE** | | | *Flinders University*<br>*College of Science & Engineering*<br>*Engineering Services Room 3.22*<br>*1284 South Rd*<br>*SA 5042* |
| Size: A4 | Number: A4 | Drawn By: D Kleiss | |
| Date: 10.3.2021. | Revision: 1 | Sheet 1 of 1 | |
| File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\PowerSupply.SchDoc | | | |

Sallen-Key Butterworth Low Pass 4th Order Filter

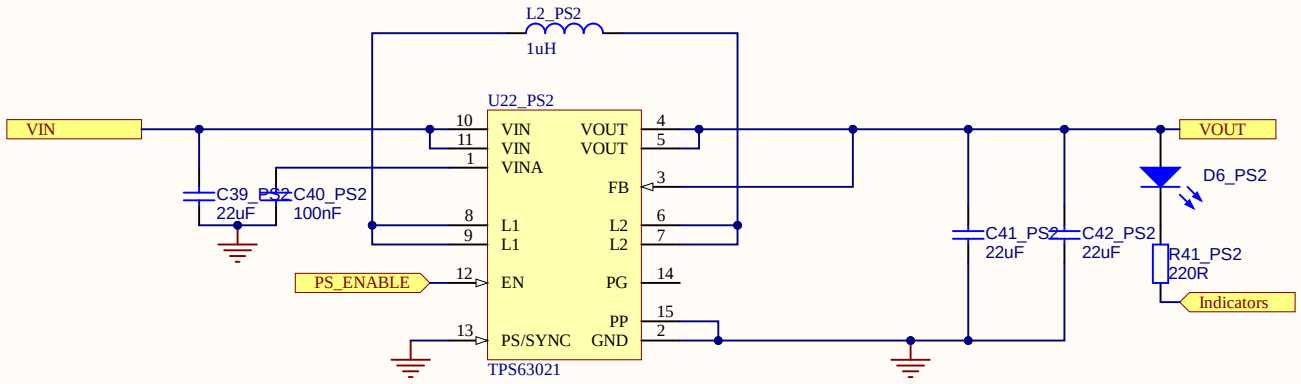



| | | | |
|---|---|---|---|
| Title | TITLE | | Flinders University<br>College of Science & Engineering<br>Engineering Services Room 3.22<br>1284 South Rd<br>SA 5042 |
| Size: A4 | Number: A4 | Drawn By: D Kleiss | |
| Date: 10.3.2021. | Revision: 1 | Sheet 1 of 1 | |
| File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\Headphone Filter.SchDoc | | | |



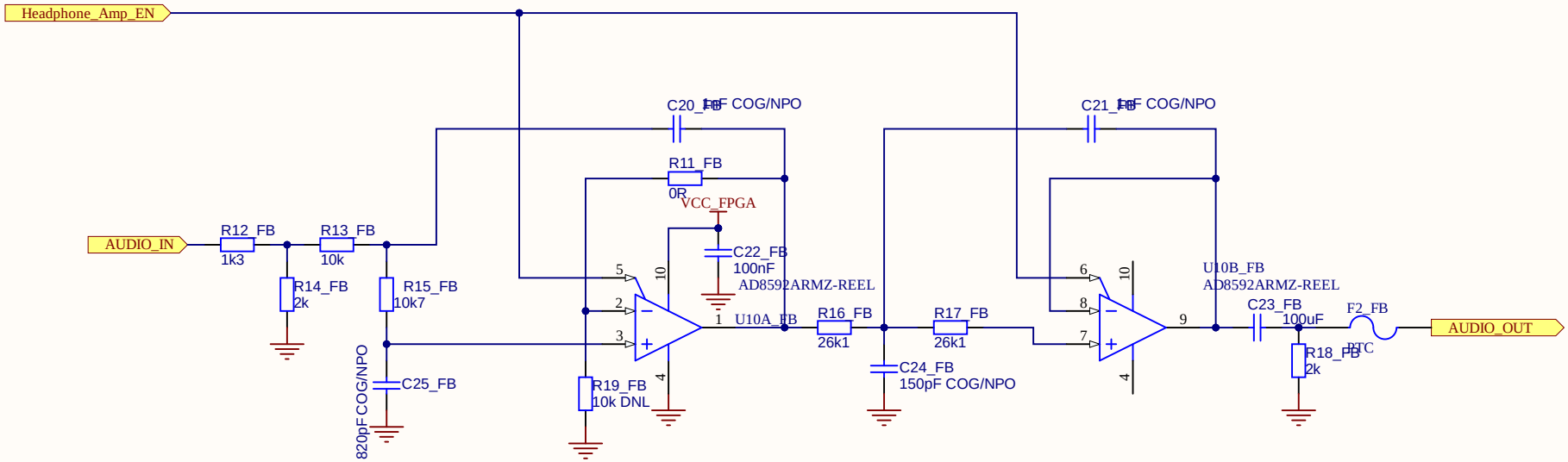

| | | | |
|---|---|---|---|
| Title | TITLE | | Flinders University<br>College of Science & Engineering<br>Engineering Services Room 3.22<br>Bedford Park SA<br>SA 5042 |
| Size: A3 | Number: A4 | Drawn By: D Kleiss | |
| Date: 10.3.2021. | Revision: 1 | Sheet 1 of 1 | |
| File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\4G Modem.SchDoc | | | |

6 17
Lachlan McDonald

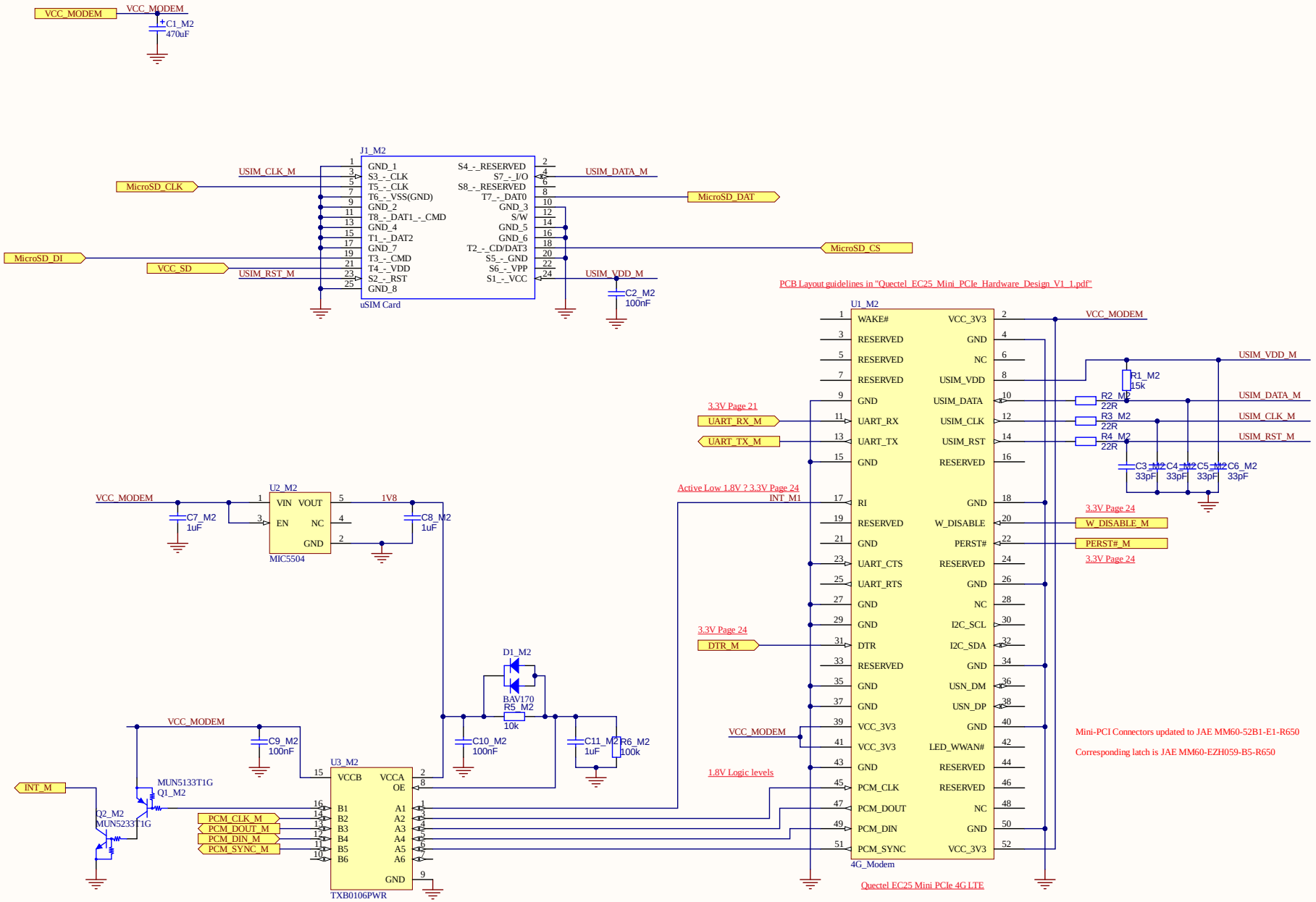



| | | | |
|---|---|---|---|
| Title **TITLE** | | | *Flinders University*<br>*College of Science & Engineering*<br>*Engineering Services Room 3.22*<br>*1284 South Rd*<br>*SA 5042* |
| Size: A4 | Number: A4 | Drawn By: D Kleiss | |
| Date: 10.3.2021. | Revision: 1 | Sheet 1 of 1 | |
| File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\PowerSupply.SchDoc | | | |

Sallen-Key Butterworth Low Pass 4th Order Filter

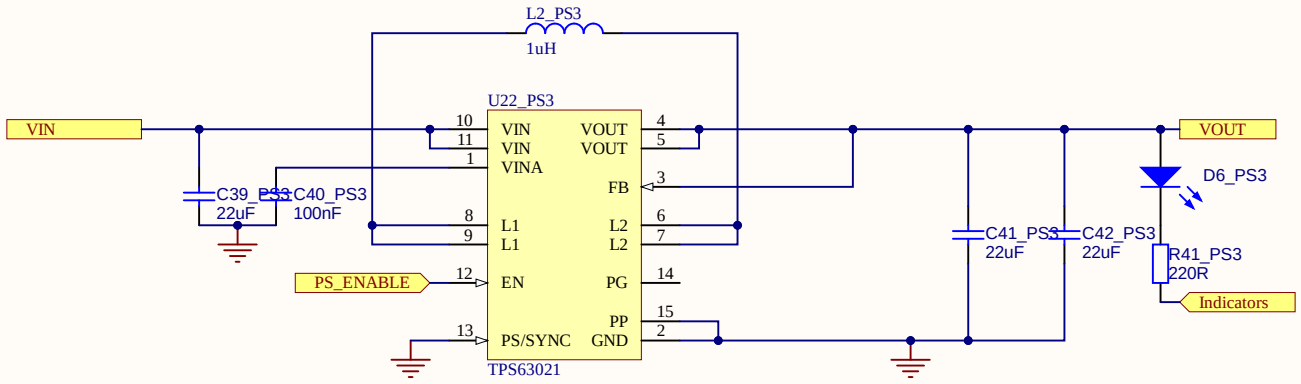



| | | | |
|---|---|---|---|
| Title | TITLE | | Flinders University<br>College of Science & Engineering<br>Engineering Services Room 3.22<br>1284 South Rd<br>SA 5042 |
| Size: A4 | Number: A4 | Drawn By: D Kleiss | |
| Date: 10.3.2021. | Revision: 1 | Sheet 1 of 1 | |
| File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\Headphone Filter.SchDoc | | | |

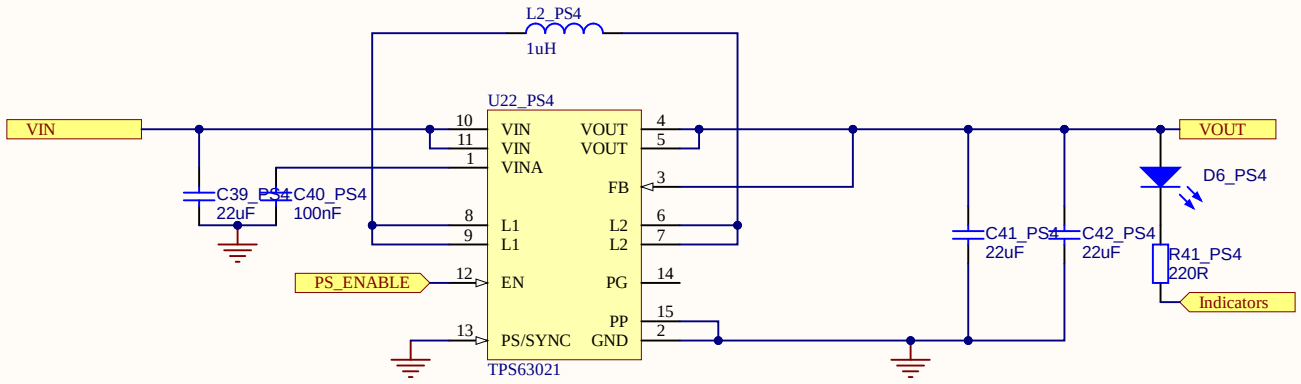



| | | | |
|---|---|---|---|
| Title | TITLE | | Flinders University<br>College of Science & Engineering<br>Engineering Services Room 3.22<br>Bedford Park SA<br>SA 5042 |
| Size: A3 | Number: A4 | Drawn By: D Kleiss | |
| Date: 10.3.2021. | Revision: 1 | Sheet 1 of 1 | |
| File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\4G Modem.SchDoc | | | |

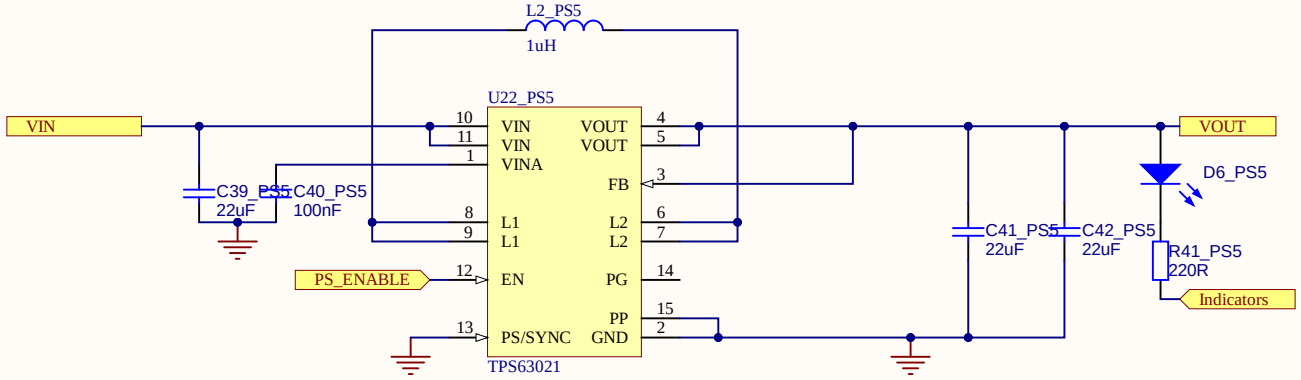
6 17
Lachlan McDonald



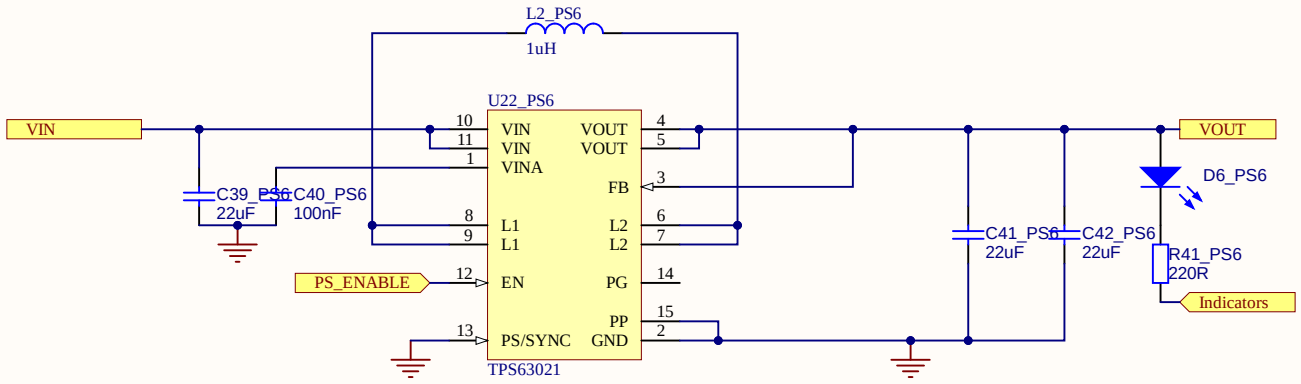

| | | | |
|---|---|---|---|
| Title **TITLE** | | | *Flinders University*<br>*College of Science & Engineering*<br>*Engineering Services Room 3.22*<br>*1284 South Rd*<br>*SA 5042* |
| Size: A4 | Number: A4 | Drawn By: D Kleiss | |
| Date: 10.3.2021. | Revision: 1 | Sheet 1 of 1 | |
| File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\PowerSupply.SchDoc | | | |




| | | | |
|---|---|---|---|
| Title **TITLE** | | | *Flinders University*<br>*College of Science & Engineering*<br>*Engineering Services Room 3.22*<br>*1284 South Rd*<br>*SA 5042* |
| Size: A4 | Number: A4 | Drawn By: D Kleiss | |
| Date: 10.3.2021. | Revision: 1 | Sheet 1 of 1 | |
| File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\PowerSupply.SchDoc | | | |

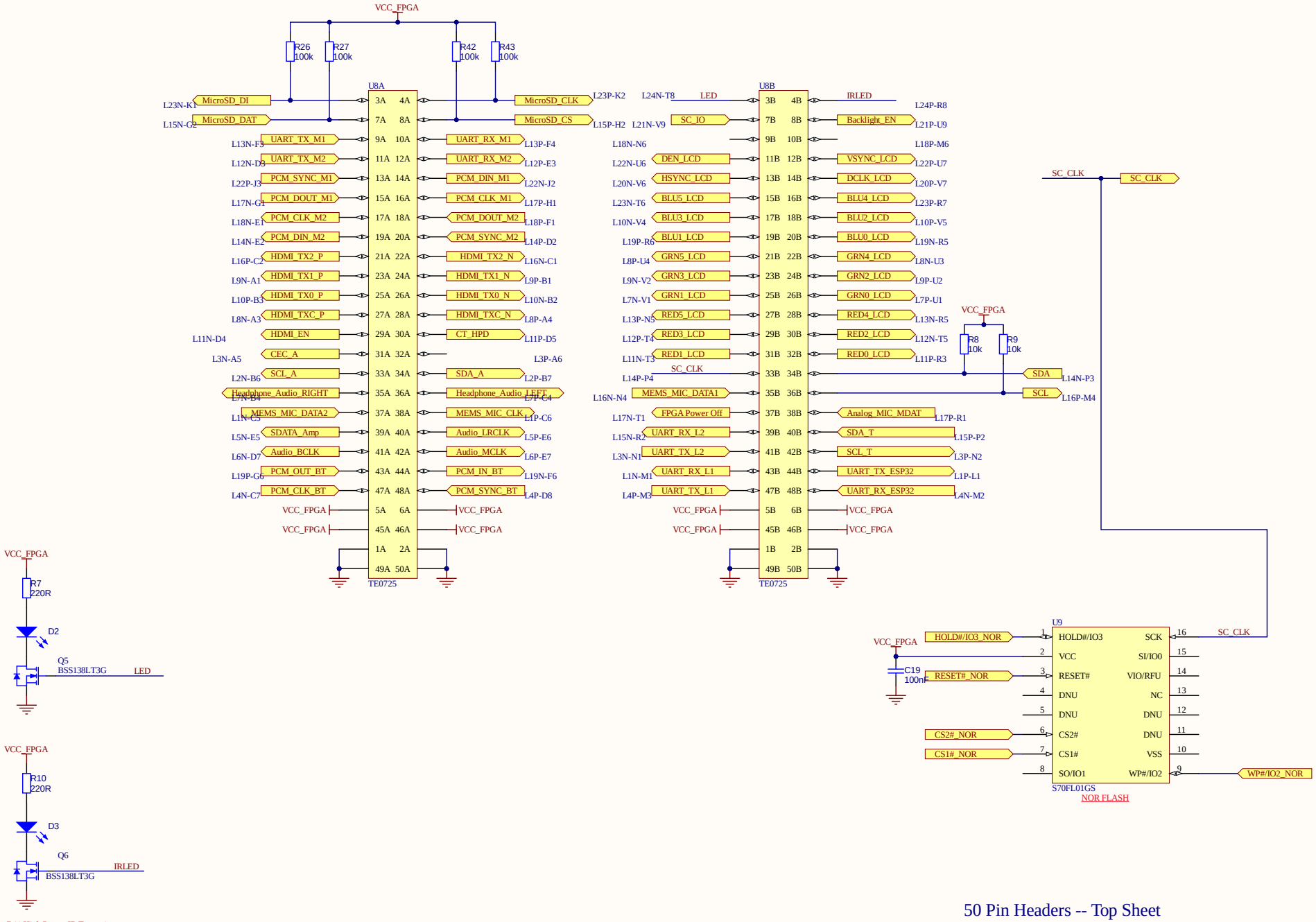



| | | | |
|---|---|---|---|
| Title **TITLE** | | | *Flinders University*<br>*College of Science & Engineering*<br>*Engineering Services Room 3.22*<br>*1284 South Rd*<br>*SA 5042* |
| Size: A4 | Number: A4 | Drawn By: D Kleiss | |
| Date: 10.3.2021. | Revision: 1 | Sheet 1 of 1 | |
| File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\PowerSupply.SchDoc | | | |




| | | | |
|---|---|---|---|
| Title **TITLE** | | | *Flinders University*<br>*College of Science & Engineering*<br>*Engineering Services Room 3.22*<br>*1284 South Rd*<br>*SA 5042* |
| Size: A4 | Number: A4 | Drawn By: D Kleiss | |
| Date: 10.3.2021. | Revision: 1 | Sheet 1 of 1 | |
| File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\PowerSupply.SchDoc | | | |

FPGA Board Is Trenz TE0725-03-100-2CF



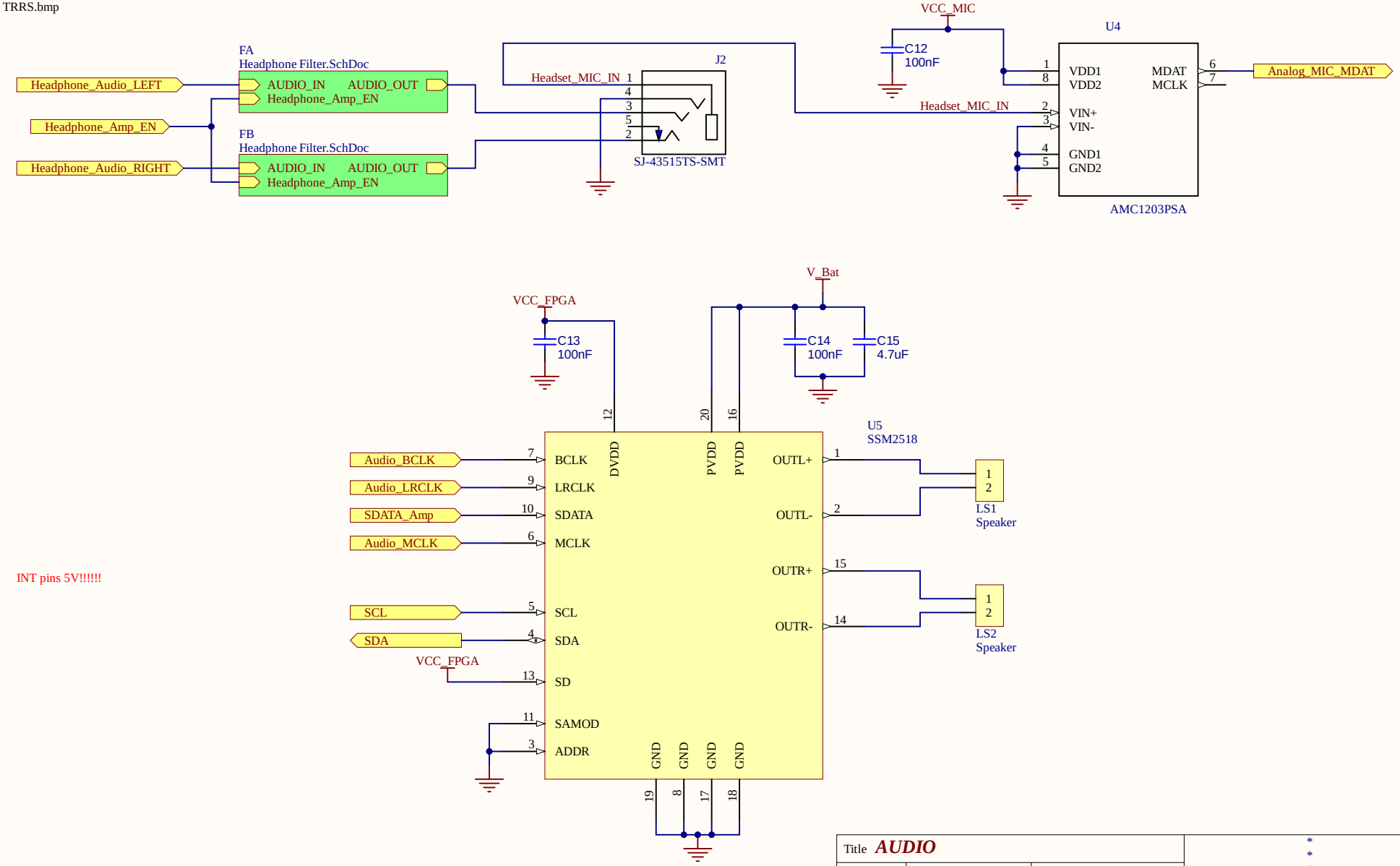

# 50 Pin Headers -- Top Sheet

| | | | |
|---|---|---|---|
| Title | *MEGAPHONE FPGA* | | |
| Size: A3 | Number: * | Drawn By: * | |
| Date: 10.3.2021. | Revision: * | Sheet 2 of * | |
| File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\FPGA.SchDoc | | | |

Bedford Park SA

Lachlan McDonald

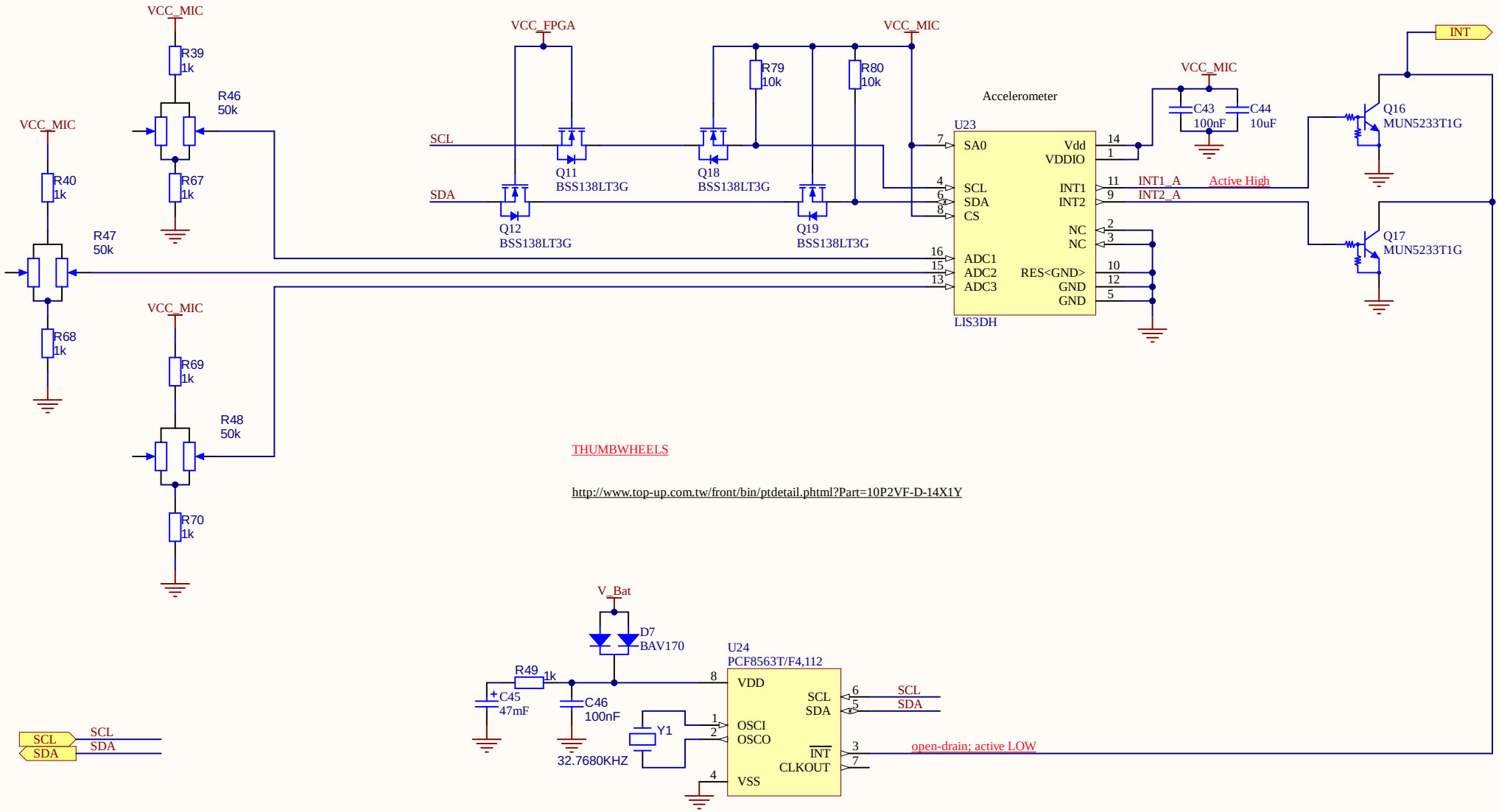
Cannot open file S:\CSE-CSEM esg\Electro Technical Team\Superceded\Documents\Altium\Step Models\Connectors\CUI\CUI_SJ-43515TS-SMT-TR\Mating TRRS.bmp



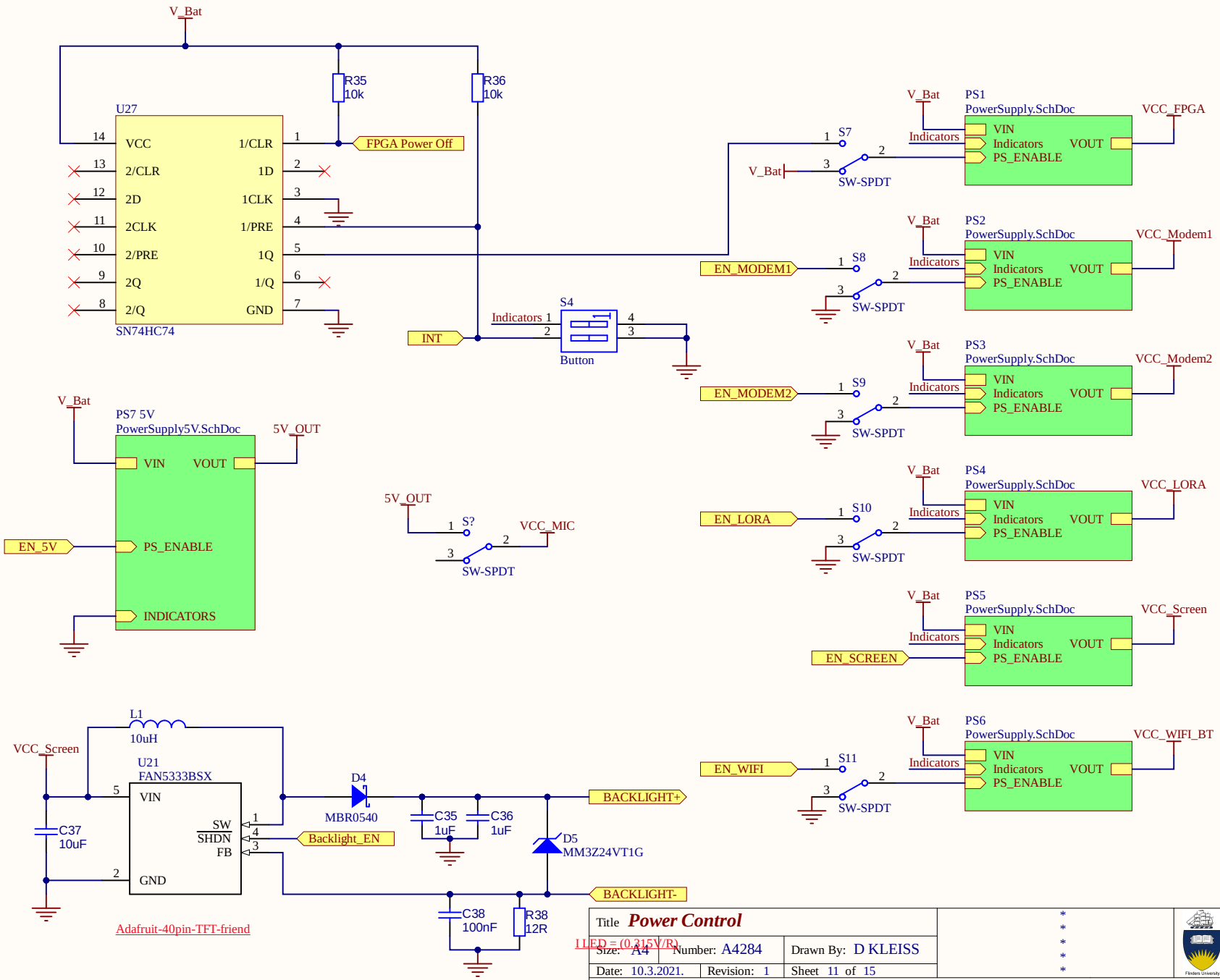

INT pins 5V!!!!!!

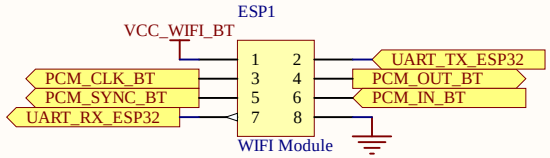
| | | | |
|---|---|---|---|
| Title **AUDIO** | | | * * * * * |
| Size: A4 | Number: * | Drawn By: D KLEISS | |
| Date: 10.3.2021. | Revision: 1 | Sheet 3 of 15 | 7 17 |
| File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\Audio.SchDoc | | | |

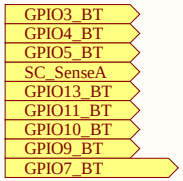
These transistors isolate VCC_MIC from the I2C bus when the accelerometer isn't receiving power



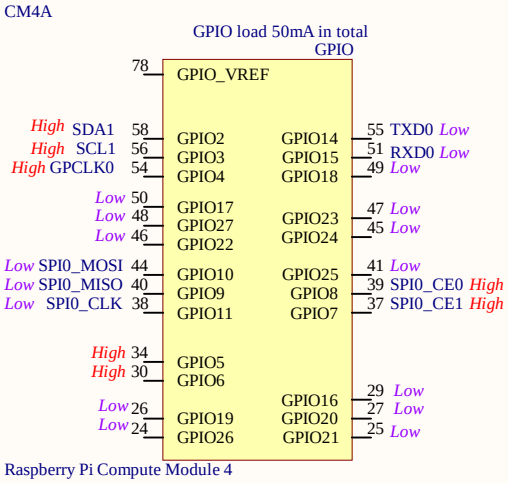

| | | | |
|---|---|---|---|
| Title | **MEGAPHONE Sensors** | | *Flinders University*<br>*College of Science & Engineering*<br>*Engineering Services Room 3.22*<br>*1284 South Rd*<br>*SA 5042* |
| Size: A4 | Number: A4284 | Drawn By: D Kleiss | |
| Date: 10.3.2021. | Revision: 1 | Sheet 5 of 15 | |
| File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\Sensors.SchDoc | | | |


V_Bat
R35
10k
R36
10k
U27
SN74HC74
VCC
2/CLR
2D
2CLK
2/PRE
2Q
2/Q
1/CLR
1D
1CLK
1/PRE
1Q
1/Q
GND
FPGA Power Off
INT
Indicators
S4
Button
PS1
PS2
PS3
PS4
PS5
PS6
PowerSupply.SchDoc
VIN
Indicators
VOUT
PS_ENABLE
VCC_FPGA
VCC_Modem1
VCC_Modem2
VCC_LORA
VCC_Screen
VCC_WIFI_BT
S7
S8
S9
S10
S11
SW-SPDT
EN_MODEM1
EN_MODEM2
EN_LORA
EN_SCREEN
EN_WIFI
PS7 5V
PowerSupply5V.SchDoc
5V_OUT
EN_5V
INDICATORS
S?
VCC_MIC
L1
10uH
U21
FAN5333BSX
SW
SHDN
FB
C37
10uF
D4
MBR0540
C35
1uF
C36
1uF
D5
MM3Z24VT1G
BACKLIGHT+
BACKLIGHT-
Backlight_EN
C38
100nF
R38
12R
Adafruit-40pin-TFT-friend
1 LED = (0.315V/R)
Title Power Control
Size: A4
Number: A4284
Drawn By: D KLEISS
Date: 10.3.2021.
Revision: 1
Sheet 11 of 15
File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\Power Control.SchDoc

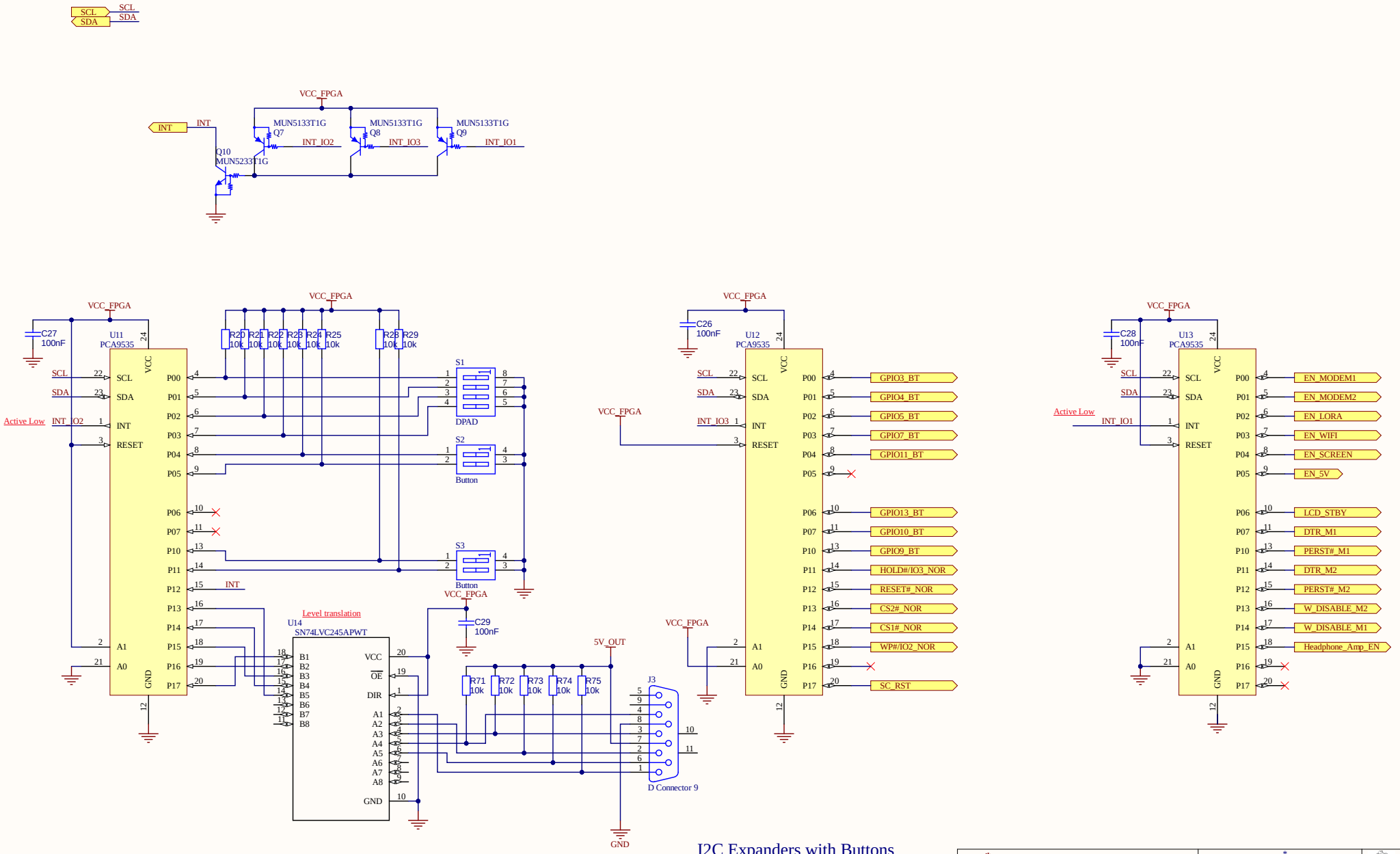



| | | | |
|---|---|---|---|
| Title | ***BLUETOOTH & WiFi*** | | * * * * * |
| Size: A4 | Number: * | Drawn By: * | |
| Date: 10.3.2021. | Revision: * | Sheet * of * | 9 17 |
| File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\Bluetooth & WIFI.SchDoc | | | Lachlan McDonald |



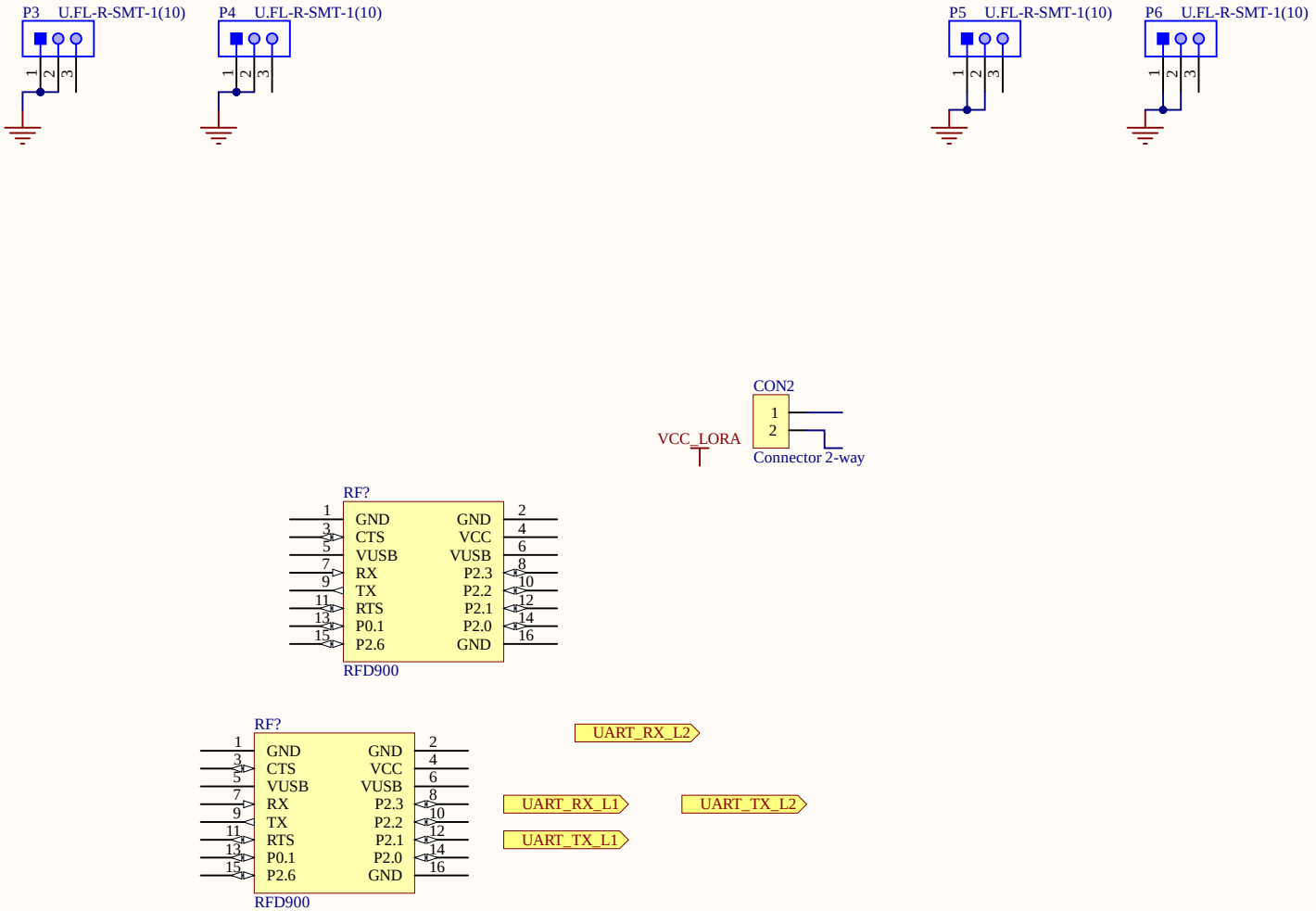

| Title | | |
|---|---|---|
| Size A4 | Number | Revision |
| Date: 3.10.2021 | | Sheet of |
| File: D:\projects\..\CM4.SchDoc | | Drawn By: |



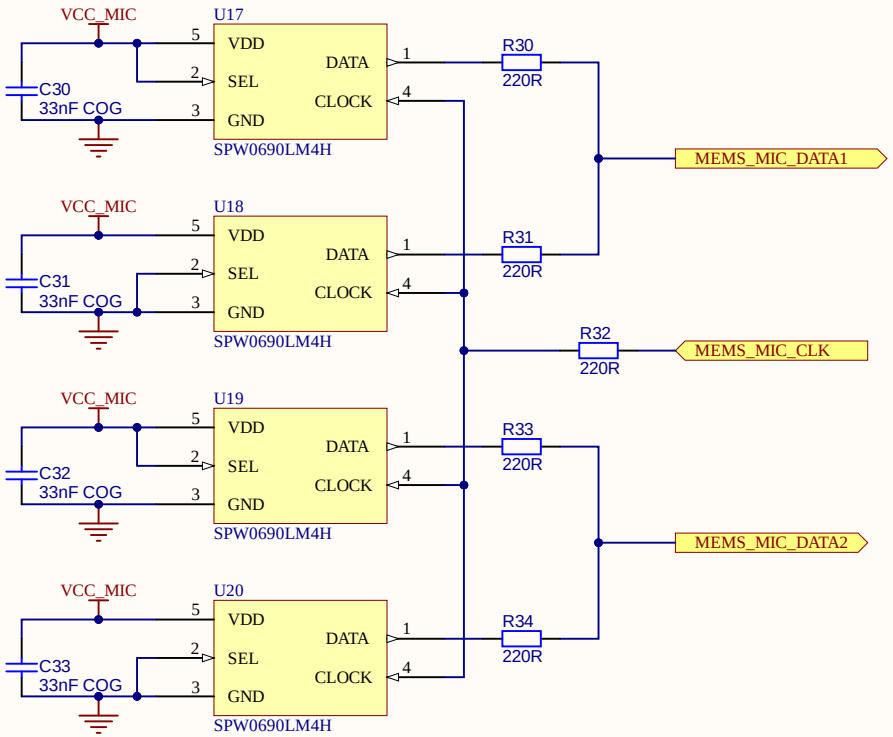

# I2C Expanders with Buttons

| | | | |
|---|---|---|---|
| Title * | | | * * * Bedford Park SA * |
| Size: A3 | Number: * | Drawn By: * | |
| Date: 10.3.2021. | Revision: * | Sheet * of * | |
| File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\I2C Expanders.SchDoc | | | |

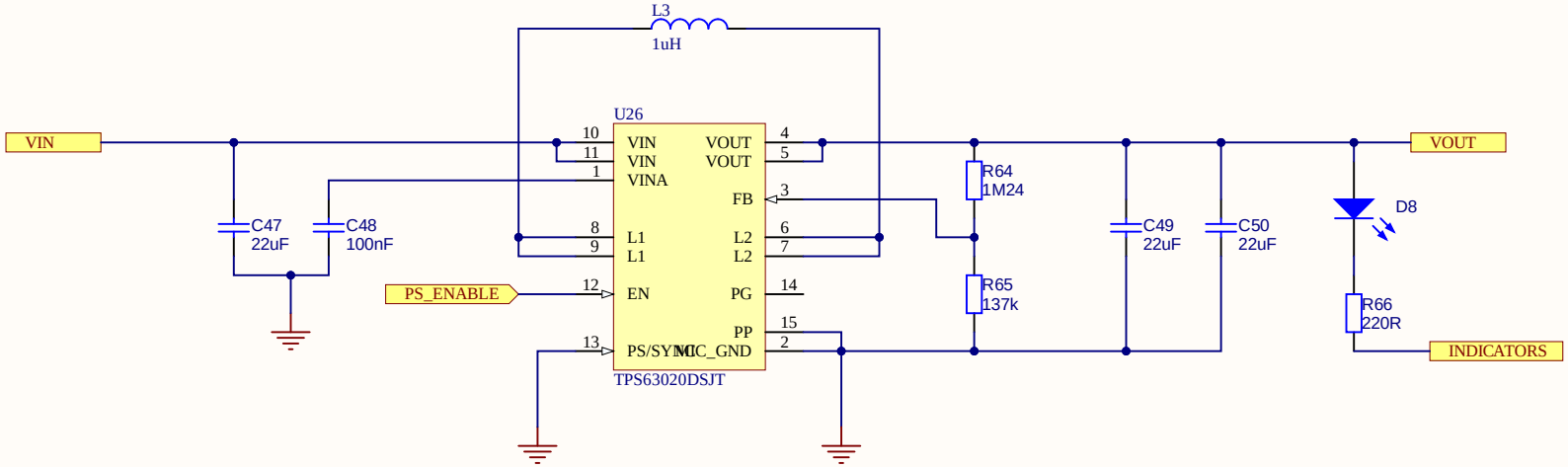
Lachlan Michell



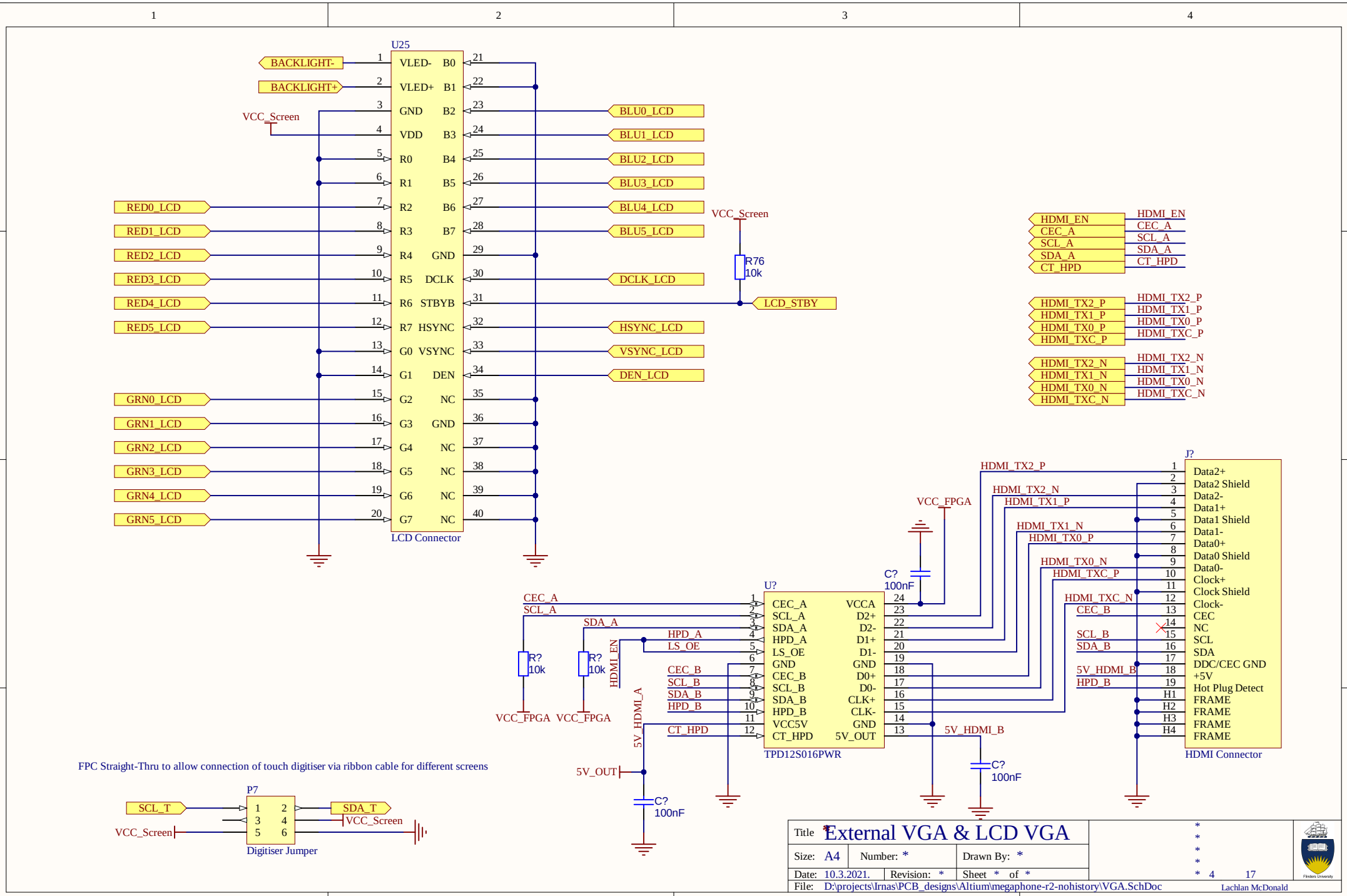

| | | | |
|---|---|---|---|
| Title * LoRa Modules | | | * * * * * |
| Size: A4 | Number: * | Drawn By: * | |
| Date: 10.3.2021. | Revision: * | Sheet * of * | 11 17 |
| File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\LoRa Radio.SchDoc | | | Lachlan McDonald |

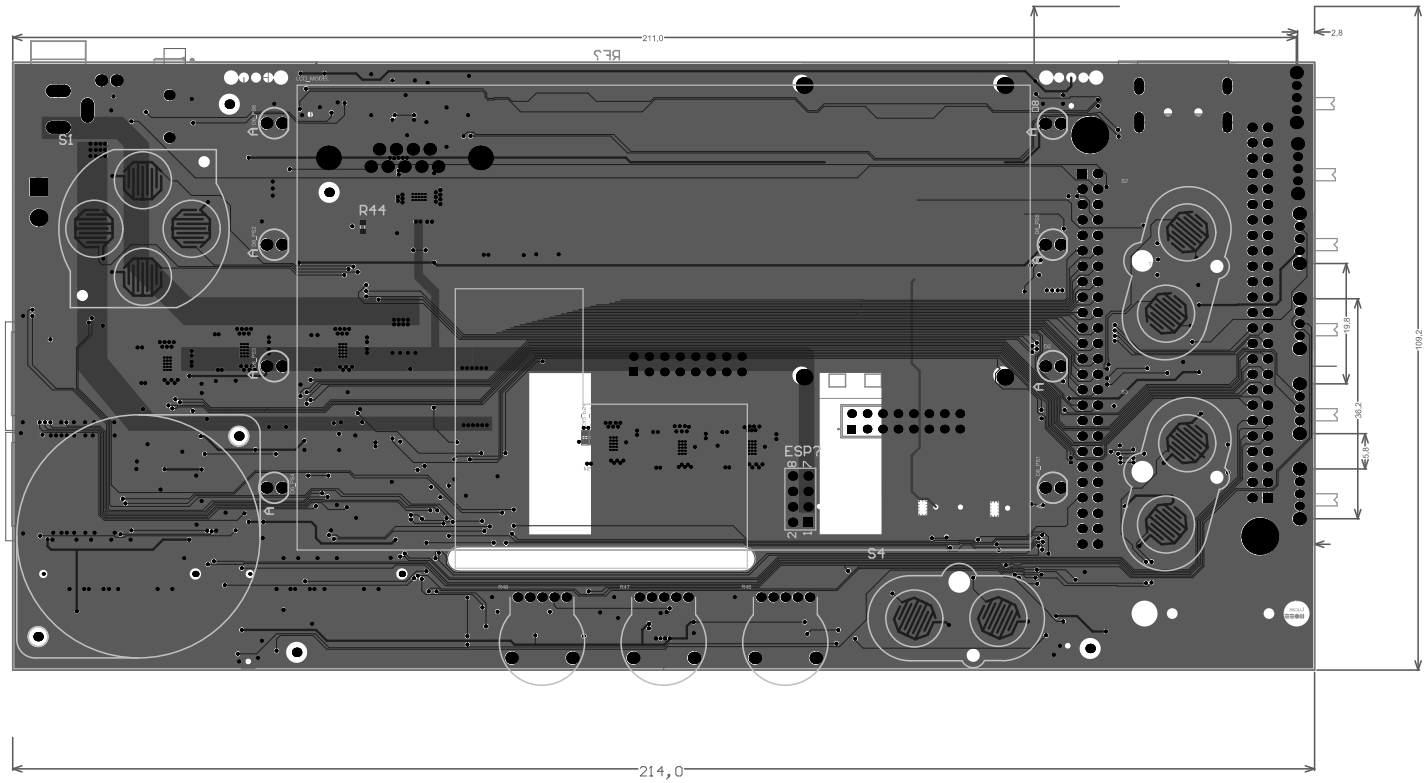


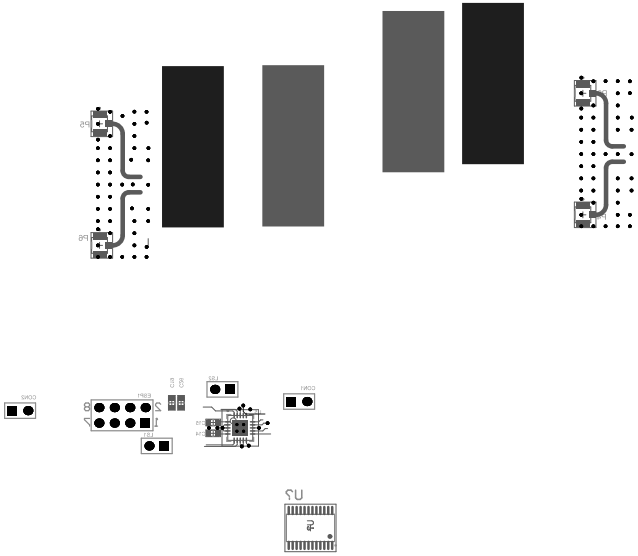

| | | | |
|---|---|---|---|
| Title * | | | * * * * * |
| Size: A4 | Number: * | Drawn By: * | |
| Date: 10.3.2021. | Revision: * | Sheet * of * | 16 17 |
| File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\MEMS MICs.SchDoc | | | Lachlan McDonald |




| Title | | |
|---|---|---|
| Size A4 | Number | Revision |
| Date: 3.10.2021 | | Sheet of |
| File: D:\projects\..\PowerSupply5V.SchDoc | | Drawn By: |


U25
BACKLIGHT-
BACKLIGHT+
VCC_Screen
VLED- B0
VLED+ B1
GND B2
VDD B3
R0 B4
R1 B5
R2 B6
R3 B7
R4 GND
R5 DCLK
R6 STBYB
R7 HSYNC
G0 VSYNC
G1 DEN
G2 NC
G3 GND
G4 NC
G5 NC
G6 NC
G7 NC
BLU0_LCD
BLU1_LCD
BLU2_LCD
BLU3_LCD
BLU4_LCD
BLU5_LCD
DCLK_LCD
LCD_STBY
HSYNC_LCD
VSYNC_LCD
DEN_LCD
RED0_LCD
RED1_LCD
RED2_LCD
RED3_LCD
RED4_LCD
RED5_LCD
GRN0_LCD
GRN1_LCD
GRN2_LCD
GRN3_LCD
GRN4_LCD
GRN5_LCD
LCD Connector
R76
10k
HDMI_EN
CEC_A
SCL_A
SDA_A
CT_HPD
HDMI_TX2_P
HDMI_TX1_P
HDMI_TX0_P
HDMI_TXC_P
HDMI_TX2_N
HDMI_TX1_N
HDMI_TX0_N
HDMI_TXC_N
J?
Data2+
Data2 Shield
Data2-
Data1+
Data1 Shield
Data1-
Data0+
Data0 Shield
Data0-
Clock+
Clock Shield
Clock-
CEC
NC
SCL
SDA
DDC/CEC GND
+5V
Hot Plug Detect
FRAME
FRAME
FRAME
FRAME
HDMI Connector
VCC_FPGA
C?
100nF
U?
CEC_A
SCL_A
SDA_A
HPD_A
LS_OE
GND
CEC_B
SCL_B
SDA_B
HPD_B
VCC5V
CT_HPD
VCCA
D2+
D2-
D1+
D1-
D0+
D0-
CLK+
CLK-
5V_OUT
TPD12S016PWR
R?
10k
HDMI_EN
5V_HDMI_A
5V_HDMI_B
5V_OUT
FPC Straight-Thru to allow connection of touch digitiser via ribbon cable for different screens
P7
SCL_T
SDA_T
VCC_Screen
Digitiser Jumper
Title External VGA & LCD VGA
Size: A4
Number: *
Drawn By: *
Date: 10.3.2021.
Revision: *
Sheet * of *
File: D:\projects\lrnas\PCB_designs\Altium\megaphone-r2-nohistory\VGA.SchDoc
4 17
Lachlan McDonald


211,0
2,8
109,2
19,8
38,2
5,0
214,0
S1
R44
ESP7
S4


MEGA65
MEGA65
U7