IIT BOMBAY — EE 101 QUIZ 3 — NOVEMBER 1, 2018

- You have **90 minutes** to answer the questions.
- Please write your **name** and **roll number** at appropriate places.
- Write the **key steps** of your solution of the problems in the space provided.
- You can solve the problems in the supplementary sheets provided but it will not be graded.

Name: Sample Solution Roll number: TA **Full Marks: 30**

Question	1	2	3	4	5	6	Total
Marks							

1. For the circuit shown in Figure 1, find the Thevenin voltage (V_{th}) and the Thevenin impedance (R_{th}) as seen from the terminals a and b. 4 marks

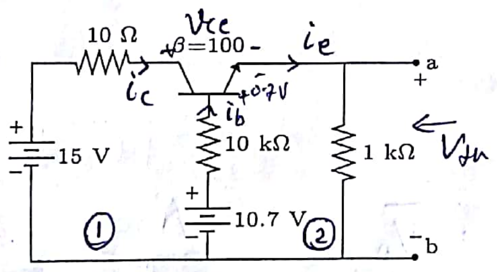


Figure 1: Circuit for Problem 1

Sol^n: Assume BJT is operating in active region $\therefore i_c = \beta i_b$

(a) KVL in loop ② (assume $V_{be} = 0.7V$)

1M $\begin{cases} 10.7 - i_b \cdot 10k - 0.7 - i_e \cdot 1k = 0 \\ \because i_e = (\beta+1) i_b \\ \therefore i_b = 90.09\ \mu A = \frac{10}{111}\ mA \end{cases}$

1M $\begin{cases} \therefore i_c = 9.009\ mA \ \&\ i_e = 9.099\ mA \\ \therefore V_{th} = i_e \times 1k\Omega = 9.099\ V \end{cases}$

With KVL in loop-①②, one can check that $V_{ce} \approx 5V$ i.e indeed BJT is operating in linear region.

(b) To determine R_{th}; lets find the i_{sc} short-circuit current across a-b terminals.

KVL in loop ② ($V_{BE} = 0.7V$)

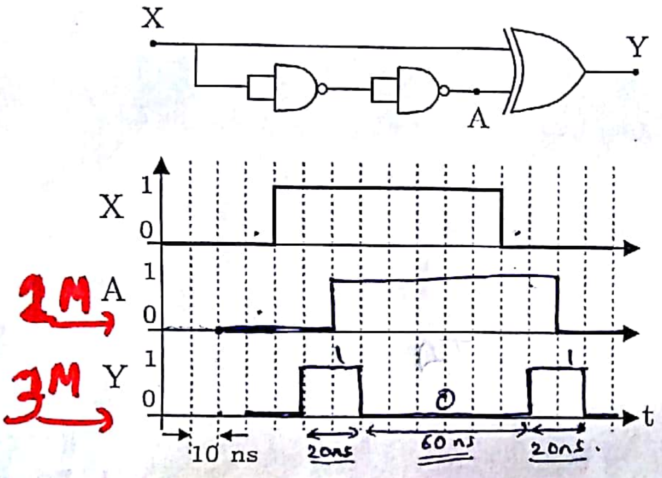
1M $\begin{cases} 10.7 - i_b \cdot 10k - 0.7 = 0 \\ \therefore \boxed{i_b = 1mA} \\ \therefore \boxed{i_c = 100\ mA} \ \&\ i_e = 101\ mA \end{cases}$

Note: $i_{sc} = i_e$ when a-b are shorted.

$\therefore$ 1M $\left\{ R_{th} = \frac{V_{th}}{i_{sc}} = 90.09\ \Omega. \right.$

Also for case(b) one can verify. $V_{ce} = 14V$ $\therefore$ BJT is still in active region.

2. For the circuit shown in Figure 2, the logic gates have a transport delay of 10 ns i.e. given an input, it takes 10 ns for the output to appear. For the input X whose waveform is as shown in Figure 2, draw the waveforms of A and Y and label appropriately. **5 marks**



→ Two NAND gates introduce a delay of 20ns.

→ XOR gate o/p appears after 10ns of input wave.

(Note: All logic gates shown here; have transport delay accounted.)

Figure 2: Circuit for Problem 2

3. For the circuit shown in Figure 3, the circuit parameters are $R_1 = 10\ \text{k}\Omega$, $R_2 = 5\ \text{k}\Omega$ and $C = 2\ \mu\text{F}$. Obtain the

- transfer function between the input (v_i) and the output (v_o),
- low frequency gain and high frequency gain of this block.

3+2=5 marks

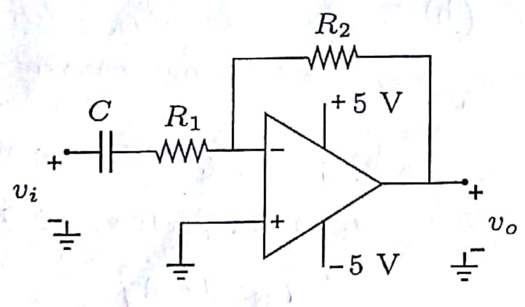
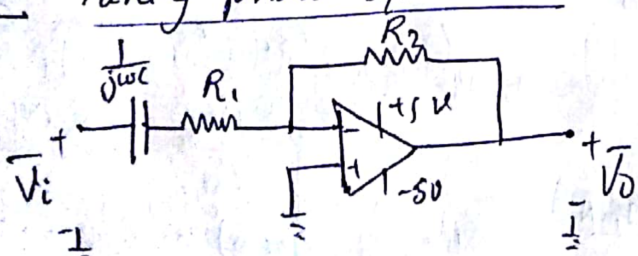


Figure 3: Circuit for Problem 3

Sol^n: Taking phasor equivalent :-



$$\therefore \frac{\bar{V_0}}{\bar{V_i}} = \frac{-R_2}{\left(R_1 + \frac{1}{j\omega C}\right)} \quad 3M$$

$$\therefore \frac{\bar{V_0}}{\bar{V_i}} = \left(\frac{-j\omega R_2 C}{1+j\omega C R_1}\right) = \frac{-j\omega 0.01}{(1+j\omega 0.02)}$$

$$\Rightarrow \text{Gain } G: \left|\frac{\bar{V_0}}{\bar{V_i}}\right| = \left|\frac{j\omega R_2 C}{1+j\omega C R_1}\right| \quad 2M$$

$G|_{\omega\to 0} = 0$ ← low frequency gain

Cont.

$G|_{\omega\to\infty} = \frac{CR_2}{CR_1} = 0.5$ ← high frequency gain

(Note: this behaves as high pass filter)

4. For the circuit shown in Figure 4, the voltage source $v_s(t)$ is a small amplitude sinusoidal signal of frequency 20 kHz. If the coupling capacitor (C_c) is 0.8 μF, find
   - quiescent value of collector to emitter voltage (V_{CE}) and base current (I_B),
   - small signal voltage gain $\left(A_v = \frac{|v_o|}{|v_s|}\right)$.

2+4=6 marks

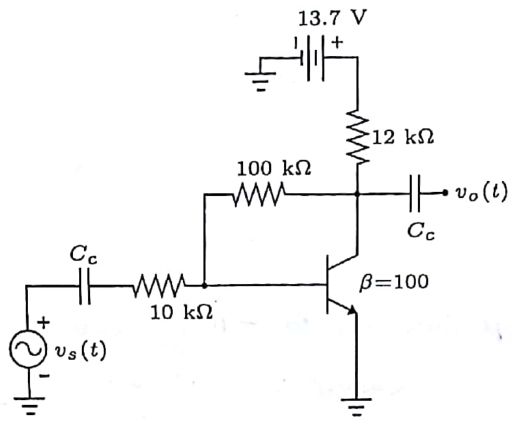
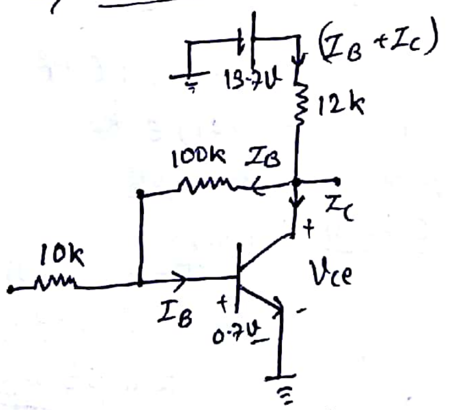


Figure 4: Circuit for Problem 4

Sol^n: (a) To determine V_{ce} & I_B using DC analysis.

⇒ Equivalent circuit is: (Assume $V_{BE} = 0.7V$)



Assume BJT is operating in linear region
$\therefore I_C = \beta I_B$.

1M KVL in outer loop:-

$13.7 - 12k(I_B + I_C) - 100k\, I_B - 0.7 = 0$

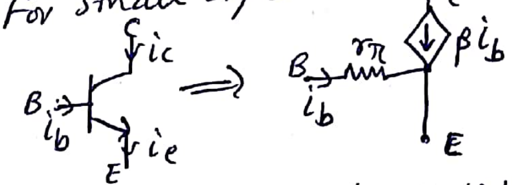
$13 = (1212k + 100k) I_B$

$\therefore I_B = \frac{13}{1312k} = \underline{9.9085\ \mu A}$.

1M $\therefore I_C = 100 \times I_B = \underline{0.9909\ mA}$

Also: $V_{ce} = 13.7 - 12k \cdot I_C + 12k\, I_B = 1.81V - 0.1189 = \underline{1.69V}$

(b) For small signal model:

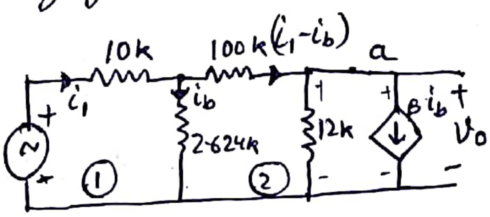


where $r_\pi = \frac{26mV}{I_B} = \underline{2.624\ k\Omega}$.

⇒ Coupling capacitor can be assumed to offer negligible reactance ∴ ignored.

CKTS: ⇒

1M



2M

⇒ KVL in ①
$V_i = 10k\, i_1 + 2.624\, i_b$ —①

⇒ KCL in node a
$i_1 - i_b = \left(\frac{V_o}{12k} + i_b \cdot \beta\right)$ —②

⇒ KVL in 1-2
$2.624k \cdot i_b - 100k(i_1 - i_b) = V_o$ —③

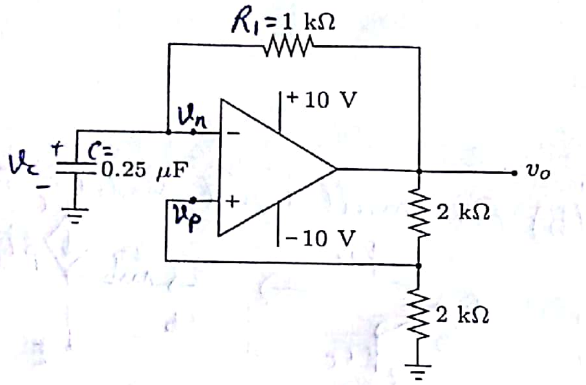
⇒ From eq^{n}② & eq^{n}③ we get.
$\boxed{i_b = 0.0852 i_1}$ —④

$\therefore V_o = -91.26k\, i_1$
& $V_i = \cancel{9.777}\ 10.224\, k \cdot i_1$ } using ①,③,④

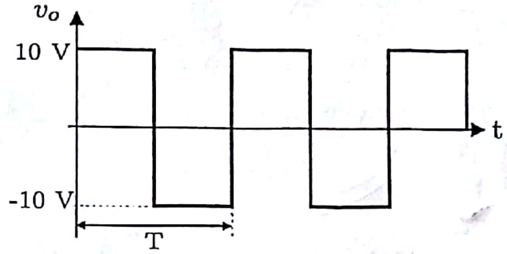
1M $\therefore A_v = \left|\frac{V_o}{V_i}\right| = 8.926$

Cont.

5. The circuit shown in Figure 5a is an oscillator whose output waveform is shown in Figure 5b. Determine the period of oscillation (T). 4 marks



(a) Circuit for Problem 5



(b) Waveform for Problem 5

Figure 5: Figures for Problem 5

Sol^n:

1M

→ v_p is $\frac{2k}{2k+2k} \times v_o = \frac{1}{2} v_o$

→ $v_n = v_c$ (value)

→ Assuming opamp to be ideal.

$\boxed{v_o = A(v_p - v_n)}$ ... $A \to \infty$ —①

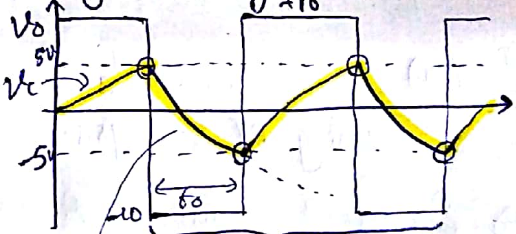
Since $\pm V_{cc} = \pm 10$ V is given; saturation hits the V_o to be bound between ± 10 V.

→ when $V_o = 10$ V; v_c is charging with +ve polarity.

→ Analysis → 2M

→ When v_c exceeds v_p (negligibly as well) O/p saturates to −10 V due to eq^n ①.

→ ∴ v_c ~~changes to~~ starts charging towards ~~→~~ −ve voltage. Waveforms can be as shown.



⇒ In general steady-state.

$$v_c = V_{final} + (V_{initial} - V_{final}) \cdot e^{-\frac{t}{RC}}$$

$$v_c = -10 + (5 - (-10)) e^{-\frac{t}{RC}}$$

when $v_c = -5$; v_o changes to +10 V

∴ $t_0 = R_1 C \ln(3)$. ∴ Time period

$T = R_1 C \ln(9)$

$= 549.3 \mu s$

≈ 0.55 ms

1M

6. Obtain the

(a) binary and decimal representation of $(FAB)_H$,

(b) decimal and hexadecimal representation of $(10101001)_2$,

(c) binary and hexadecimal representation of $(110)_{10}$.

2+2+2=6 marks

(a) $(FAB)_H = (1111\ 1010\ 1011)_2 = (4011)_{10}$

1M 1M

(b) $(1010\ 1001)_2 = (A9)_H = (169)_{10}$

1M 1M

(c) $(110)_{10} = (6E)_H = (0110\ 1110)_2$

1M 1M

The End.