



**MIDDLE EAST TECHNICAL UNIVERSITY**

**EE464- STATIC POWER CONVERSION-II**

**Hardware Project Final Report**

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## 1 Introduction

This report is prepared to provide design specifications, component selections, performance and computer simulations of the our isolated flyback converter design for the EE464 hardware project. All deliverables of the project which are isolated flyback converter, compensator, controller and thermal designs will be provided in this report.

There are mainly two different topologies and three different specs for each topology. As XXX we have chosen the Flyback 1 topology whose specs are listed below:

FLYBACK	Minimum Input Voltage (V)	24
	Maximum Input Voltage (V)	48
	Output Voltage (V)	15
	Output Power (W)	60
	Output Volt. Peak-to-Peak Ripple (%)	4
	Line Regulation (%)	2
	Load Regulation (%)	2

Figure 1: Design Specifications of the Flyback 1 Converter

Simplicity of less components, wide input voltage range and lower cost advantages of Flyback topology are the main reasons of our choice. Compact design and high power density is another benefits of the Flyback converter. Moreover, the Flyback converter offers higher efficiency in low voltage range. The Flyback 1 topology is preferred by taking all of these into account.

## 2 Isolated Flyback Converter Design and Component Selections

A Flyback converter has two kinds of operation modes ; continuous conduction mode (CCM) and discontinuous conduction mode (DCM). CCM and DCM have their own advantages and disadvantages, respectively.

A CCM flyback was preferred for this project for improved efficiency, reduced component stress and reduced filter size. A CCM flyback operation reduces peak currents, RMS currents, and switch loss. Therefore CCM is usually recommended for low voltage and high current output applications. However the main disadvantage of a CCM flyback is the lower control loop bandwidth due to a right-half plane zero (RHPZ) which can be solved by a compensator.

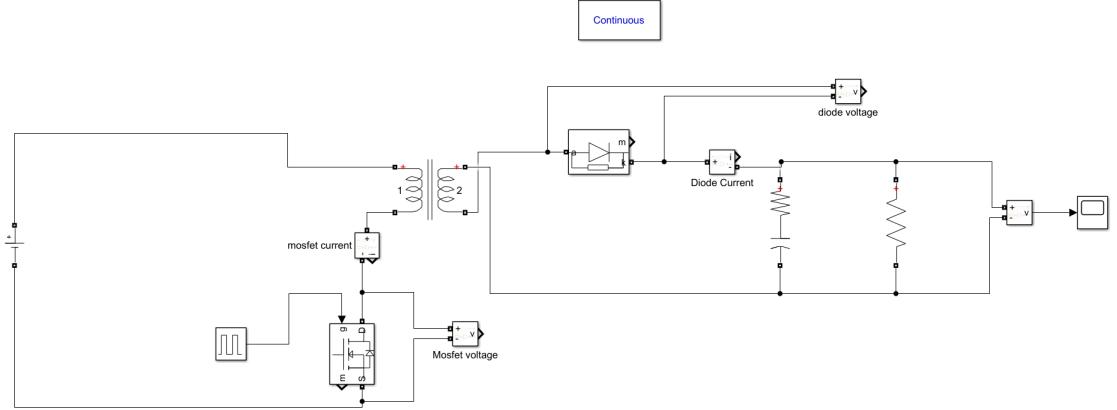


Figure 2: The framework design of Flyback converter.

Let's start by choosing turn ratio of transformer and estimated efficiency:

$$N = \frac{N_{primary}}{N_{secondary}} = 1.5$$

$$\eta = \frac{P_{out}}{P_{in}} \approx \%80$$

$$\text{Hence, } P_{in} = 75W$$

$$D_{max} = 0.5$$

$$V_D = 0.5 \text{ diode forward voltage}$$

$$N = \frac{N_1}{N_2} = \frac{V_{in,min} D_{max}}{(V_{out} + V_D)(1 - D_{max})} = 1.548$$

$$\frac{1 - D_{min}}{D_{min}} = \frac{V_{max}}{(V_{out} + V_D)n}$$

$$D_{min} = 0.326$$

## 2.1 Framework Design

Switched mode power supply (SMPS) design is inherently a very complex job requires many trade-off decisions and iterations with a lot of design parameters. In design process, we have comprehensively worked on literature and step-by-step notes. The framework of our design is build by following 3 steps:

1. Determine  $V_{Mosfet}$ :

$$V_{Mosfet} = V_{in,max} + n(V_{out} + V_D) \approx 72V$$

where  $V_D = \text{diode (schottky) voltage} = 0.5V$

2. Determine the transformer primary side inductance  $L_m$ :

$$L_m = \frac{(V_{DC,min}D_{max})^2}{2P_{in}f_sK}$$

where  $K = 0.3$  the ripple factor in full load and minimum input voltage condition

$$f_s = 40kHz$$

$$L_m = \frac{(24 * 0.5)^2}{2 * 75 * 4 * 10^4 * 0.3} \approx 78\mu H$$

Check CCM to DCM boundary:

$$(L_m)_{min} = \frac{(1 - D)^2 R}{2f} N^2 = 47.9\mu H$$

$$L_m > (L_m)_{min}$$

3. Determine the switch current rating:

$$I_{ds,peak} = I_{EDC} + \frac{\Delta I}{2}$$

$$I_{EDC} = \frac{P_{in}}{V_{in,min}D_{max}} = \frac{75}{24 * 0.5} = 6.25A$$

$$\Delta I = \frac{V_{in,min}D_{max}}{L_m f_s} = 3.84A$$

$$I_{ds,peak} = 8.2A$$

$$I_{ds,rms} = \sqrt{[3(I_{EDC})^2 + (\frac{\Delta I}{2})^2] \frac{D_{max}}{3}} = 4.49A$$

$$I_{Mosfet} = 8.5A$$

## 2.2 Transformer Design

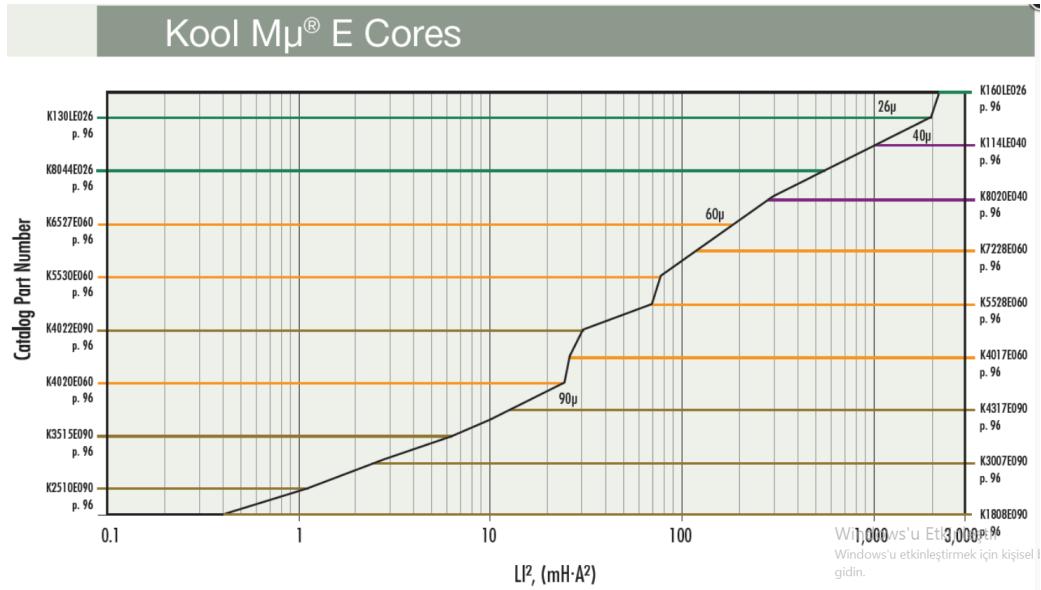


Figure 3:  $LI^2$  Characteristics of Kool Mu E Cores [1]

$$L_m I^2 = 78 * 10^{-3} (2.66)^2 = 0.554 mH \cdot A^2$$

From Figure 3 K2510E090 has been chosen

$$N_{pri} = \sqrt{\frac{L_{pri}}{A_L}} = \sqrt{\frac{78 \mu H}{92 nH/T^2}} = 29 \text{ turns}$$

Let's choose  $N_{pri} = 30$

Checking DC bias:

$$NI_{pri} = 30 * 2.66 = 79.8 A \cdot turns$$

For 78.8 A\*turns,  $A_L = 85 nH/T^2$

$$L = N^2 A_L = 30^2 * 85 = 76.5 \mu H$$

$$H = \frac{NI}{L_e} = \frac{30 * 2.66}{4.85} = 16.45 A \cdot turns/cm$$

$$B = 0.12 \text{ Tesla}$$

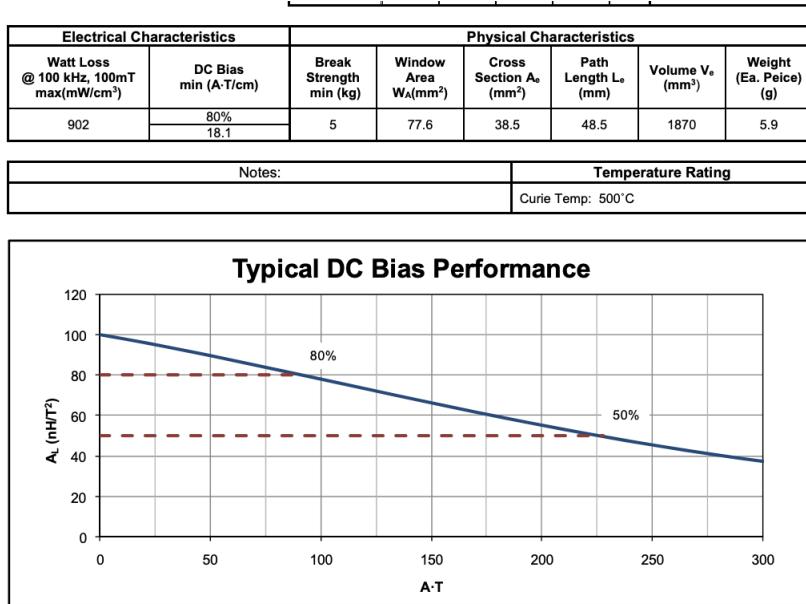


Figure 4: Electrical characteristic of K2510E090 core.

## DC Magnetization Curves

### Fit Formula

$$B = \left[ \frac{a + bH + cH^2}{1 + dH + eH^2} \right]^x \text{ Units: B in Tesla; H in A·Turns/cm}$$

where:

	$\mu$	$a$	$b$	$c$	$d$	$e$	$x$
Kool Mp <sup>®</sup>	14	1.105E-01	1.301E-02	6.115E-04	1.386E-01	5.735E-04	1.760
	26	1.008E-01	1.452E-02	7.846E-04	1.035E-01	7.573E-04	1.754
	40	5.180E-02	2.132E-02	7.941E-04	8.447E-02	7.652E-04	1.756
	60	5.214E-02	2.299E-02	8.537E-04	7.029E-02	8.183E-04	1.658
	75	4.489E-02	2.593E-02	7.949E-04	6.463E-02	7.925E-04	1.595
	90	4.182E-02	2.990E-02	7.824E-04	6.542E-02	7.669E-04	1.549
	125	1.414E-02	2.851E-02	1.135E-03	7.550E-02	1.088E-03	1.274

Figure 5: DC magnetization curve provided by producer.

$B = 0.176T$  according to provided equation in Figure 5.

Core Loss Density Curves					
Fit Formula					
$P = a(B^b)(f^c)$ (B in Tesla, f in kHz)					
	Perm	freq:	a	b	c
Kool Mp®	14 $\mu$	> 10kHz	21.49	1.000	1.33
	14 $\mu$	< 10kHz	40.18	1.000	1.22
	24 $\mu$ , 40 $\mu$	> 10kHz	45.48	1.774	1.46
	26 $\mu$ , 40 $\mu$	< 10kHz	170.17	1.774	1.03
	60 $\mu$	> 9kHz	62.65	1.781	1.36
	60 $\mu$	< 9kHz	136.93	1.781	1.12
	75 $\mu$ , 90 $\mu$	> 10kHz	146.81	2.022	1.33
	75 $\mu$ , 90 $\mu$	< 10kHz	338.51	2.022	1.05
	125 $\mu$	> 10kHz	71.93	1.928	1.47
	125 $\mu$	< 10kHz	228.46	1.928	1.05

Figure 6: Core loss density curve provided by producer.

$$P = 568.8 \text{mW/cm}^3$$

$$\text{Volume of selected core}=1.87 \text{cm}^3$$

$$\text{Therefore core loss}=568.8 * 1.87 = 1.063 \text{W}$$

## 2.3 Wire Selection

Skin effect and switching frequency are considered for wire selection. Therefore, possible maximum conductor cross section was chosen to avoid high ac resistance and losses, as seen in Figure 7.

AWG gauge	Conductor Diameter Inches	Conductor Diameter mm	Conductor cross section in mm <sup>2</sup>	Ohms per 1000 ft.	Ohms per km	Maximum amps for chassis wiring	Maximum amps for power transmission	Maximum frequency for 100% skin depth for solid conductor copper
0000	0.46	11.684	107	0.049	0.16072	380	302	125 Hz
000	0.4096	10.40384	84.9	0.0618	0.202704	328	239	160 Hz
00	0.3648	9.26592	67.4	0.0729	0.255512	283	190	200 Hz
0	0.3249	8.25246	53.5	0.0983	0.322424	245	150	250 Hz
1	0.2893	7.34822	42.4	0.1239	0.406392	211	119	325 Hz
2	0.2576	6.54304	33.6	0.1563	0.512664	181	94	410 Hz
3	0.2294	5.82676	26.7	0.197	0.64616	158	75	500 Hz
4	0.2043	5.18922	21.1	0.2485	0.81503	135	60	650 Hz
5	0.1819	4.62026	16.8	0.3133	1.027624	118	47	810 Hz
6	0.162	4.1148	13.3	0.3951	1.295928	101	37	1100 Hz
7	0.1443	3.66522	10.6	0.4982	1.634096	89	30	1300 Hz
8	0.1285	3.2639	8.37	0.6282	2.060496	73	24	1650 Hz
9	0.1144	2.90576	6.63	0.7921	2.598088	64	19	2050 Hz
10	0.1019	2.58826	5.26	0.9989	3.276392	55	15	2600 Hz
11	0.0907	2.30378	4.17	1.26	4.1328	47	12	3200 Hz
12	0.0808	2.05232	3.31	1.588	5.20864	41	9.3	4150 Hz
13	0.072	1.8288	2.63	2.003	6.56984	35	7.4	5300 Hz
14	0.0641	1.62814	2.08	2.525	8.282	32	5.9	6700 Hz
15	0.0571	1.45034	1.65	3.184	10.44352	28	4.7	8250 Hz
16	0.0508	1.29032	1.31	4.016	13.17248	22	3.7	11 k Hz
17	0.0453	1.15062	1.04	5.064	16.60992	19	2.9	13 k Hz
18	0.0403	1.02362	0.823	6.385	20.9428	16	2.3	17 kHz
19	0.0359	0.91186	0.653	8.051	26.40728	14	1.8	21 kHz
20	0.032	0.8128	0.519	10.15	33.292	11	1.5	27 kHz
21	0.0285	0.7239	0.412	12.8	41.984	9	1.2	33 kHz
22	0.0253	0.64516	0.327	16.14	52.9392	7	0.92	42 kHz
23	0.0226	0.57404	0.259	20.36	66.7808	4.7	0.729	53 kHz
24	0.0201	0.51054	0.205	25.67	84.1976	3.5	0.577	68 kHz

Figure 7: Wire gauge chart.

$$I_{pri}^{rms} = 4.52A$$

$$I_{sec}^{rms} = I_{ds}^{rms} \sqrt{\frac{1 - D_{max}}{D_{max}}} \frac{V_{RO}}{V_o + V_F}$$

$$V_{RO} = \frac{D_{max}}{1 - D_{max}} V_{in}^{min}$$

$$I_{sec}^{rms} = 6.67A$$

Choose  $J = 6A/mm^2$

$$A_{pri} = \frac{4.52}{6} \approx 0.76$$

$$A_{sec} = \frac{6.67}{6} \approx 1.11$$

Pick 3xAWG23 and 4xAWG22

$$k_u(\text{fill factor}) = \frac{3 * 0.259 * 30 + 4 * 0.327 * 20}{77.6} = \%64$$

$$MLT = \pi * (E + F)/2 = 39.3285mm \quad E \text{ and } F \text{ are the core parameters shown in Datasheet.}$$

$$Length \text{ primary} = 30 * 39.3285 = 11780mm$$

$$Length \text{ secondary} = 20 * 39.3285 = 786.57mm$$

$$R_{pri} = (66.78 * 1.18 * 10^{-3})/3 = 0.0262\Omega$$

$$R_{sec} = (52.9392 * 0.786 * 10^{-3})/4 = 0.0104\Omega$$

There is no need to calculate the AC resistances since skin effect is already considered during wire selection. In other words, it can be taken as same with the dc resistances by neglecting the proximity effect.

$$P_{cu} = I_{pri(rms)}^2 * R_{pri} + I_{sec(rms)}^2 * R_{sec} = 4.5222 * 0.0262 + 6.6732 * 0.0131 = 1.119W$$

## 2.4 Diode Selection

$$V_D = V_o + \frac{V_{in}^{max}(V_o + V_F)}{V_{RO}} \approx 47V$$

$$I_D^{rms} = I_{sec}^{rms} = 6.67A$$

## 2.5 Output Capacitor Selection

$$\Delta V_0 = \frac{I_o D_{max}}{C_o f_s} + \frac{I_{ds}^{peak} V_{RO} R_C}{V_o + V_F}$$

$$R_C = 15m\Omega$$

$\Delta V_o$  is desired %4 which is equal to 0.6V deviation

$$\text{Let's make a conservative selection } \Delta V_o = 0.35V \quad \Delta V_o = \frac{4 * 0.492}{C_o * 4 * 10^4} + \frac{8.2 * 24 * 0.015}{15.5}$$

$$0.35 = \frac{4.92 * 10^{-5}}{C_o} + 0.19$$

$$C_o = \frac{4.92 * 10^{-5}}{0.16}$$

$$C_o \approx 330\mu F$$

## 2.6 RC-Snubber Design

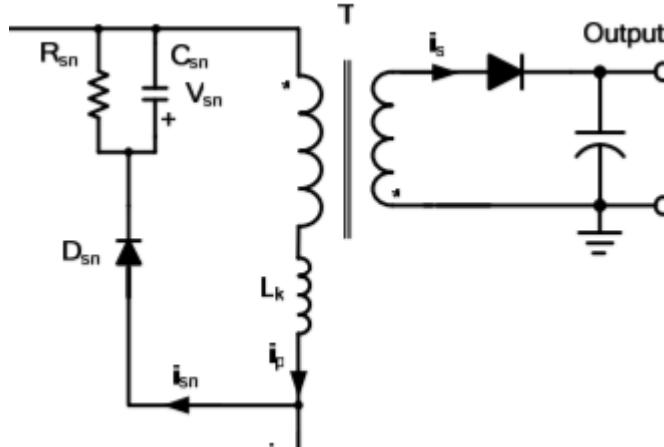


Figure 8: RCD snubber.

During the off time, additional voltage stress may occur on Mosfet (switch) due to leakage inductance of the transformer and they may damage the Mosfet. Therefore, a RCD snubber has designed to reduce that extra stress on Mosfet, shown in Figure 8. The components of that circuit depends on the primary leakage inductance, so they may be changed after measuring the leakage inductance in practice. For theoretical calculations, leakage inductance is taken as %1 of the primary inductance.

When the Mosfet turns off, current on the leakage inductance starts to flow through the RCD snubber and it suppress the voltage stress on that node due to ringing effect. To design RCD snubber, the steps are followed:

1. Measure leakage inductance \*Due to pandemic condition, we have used %1 of the magnetizing inductance  $L_m$ .

$$L_{leakage} = L_m * 0.01 = 0.7\mu H$$

2. Determine peak clamp voltage:

$$\begin{aligned}
 P &= \frac{1}{2} L I_{peak}^2 f_s \\
 P &= \frac{1}{2} * 7 * 10^{-7} (6.5)^2 * 4 * 10^4 \approx 0.6W \\
 V_f &= 70V \quad V_x = 70/3V \\
 P_{snubber}^{max} &= 0.6(1 + \frac{V_f}{V_x}) = 2.4W
 \end{aligned}$$

3. Selecting clamp resistor:

$$\begin{aligned}
 R &= \frac{2V_x T_s (V_f + V_x)}{L I_p^2} \\
 R &= \frac{2 * 23.3 * (93.3)}{7 * 10^{-7} * (6.5)^2 * 4 * 10^{-4}} \approx 3.67k\Omega
 \end{aligned}$$

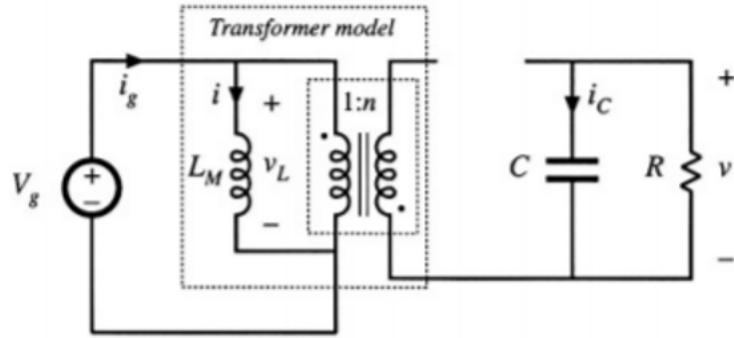
### 3 Compensator Design and Controller

#### 3.1 Compensator Design

To construct a compensator circuit for closed loop control, the transfer function of the circuit should be derived by using small-signal model of Flyback converter. In this process, super-position method has been used. Control-to-output transfer function of CCM Flyback is derived below:

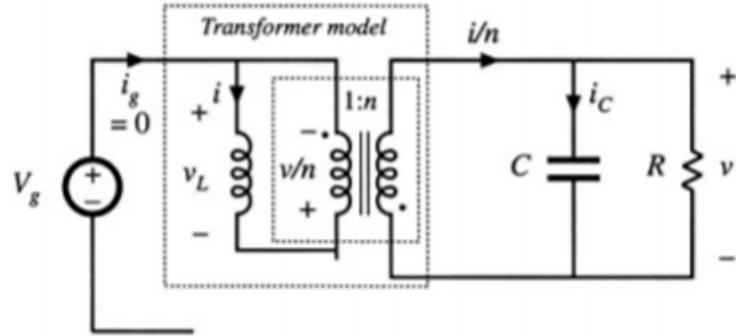
In order to achieve the small signal model of the flyback converter; capacitor current, inductor voltage and input current equations should be derived for both ON and OFF states of the switch.

1. Switch is OFF:



$$V_L = V_g i_c = -\frac{V}{R} i_g = I$$

2. Switch is ON:



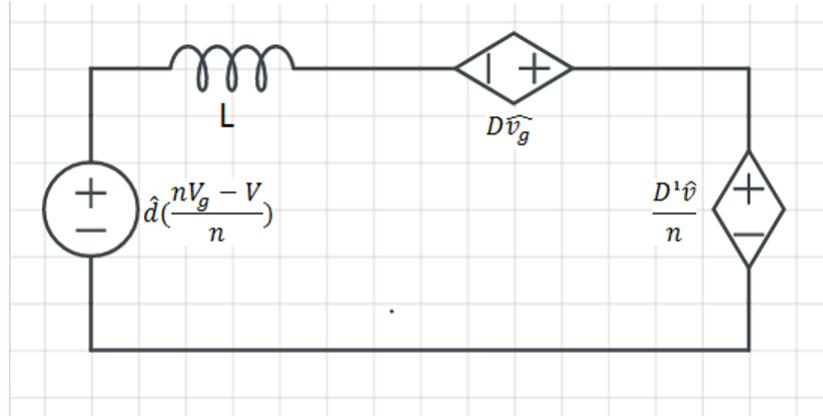
$$V_L = -\frac{V}{n} i_c = \frac{I}{n} - \frac{V}{R} i_g = 0$$

Averaging and Linearizing:

$$\begin{aligned} V_c &= V & V_L &= DV_g - \frac{D'V}{n} \\ i_c &= -\frac{DV}{R} + D'(-\frac{V}{R} + \frac{I}{n}) & i_g &= DI \end{aligned}$$

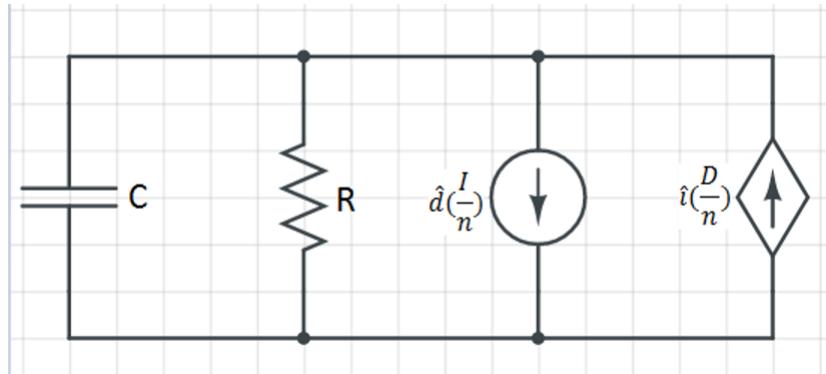
Considering AC perturbations following AC circuits are obtained.

3. Inductor voltage:



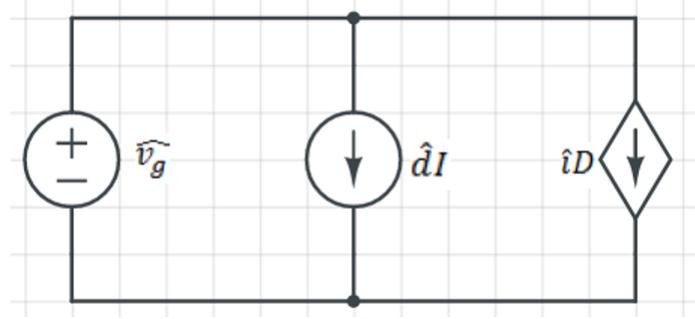
$$L \frac{d\tilde{v}_L}{dt} = D\tilde{v}_g + \tilde{d}V_g - \frac{D'\tilde{v} - \tilde{d}V}{n} = \tilde{d}\left(\frac{nV_g - V}{n}\right) + D\tilde{v}_g - \frac{D'\tilde{v}}{n}$$

4. Capacitor current:



$$\begin{aligned} C \frac{d\tilde{V}}{dt} &= -\frac{D\tilde{v} + \tilde{d}V}{R} - \frac{D'\tilde{v}}{R} + \frac{\tilde{d}V}{R} + \frac{D'\tilde{i}}{n} - \frac{\tilde{d}I}{n} \\ &= -\tilde{d}\frac{I}{n} - \frac{\tilde{v}}{R} + \tilde{i}\frac{D}{n} \end{aligned}$$

5. Input current:



$$\tilde{i}_g = \tilde{i}D + \tilde{d}I$$

Adding these three circuits one after another will result with :  
 L: magnetizing inductor      I: inductor current       $R_o n$ : diode resistor  
 V:output voltage       $V_g$ : input voltage

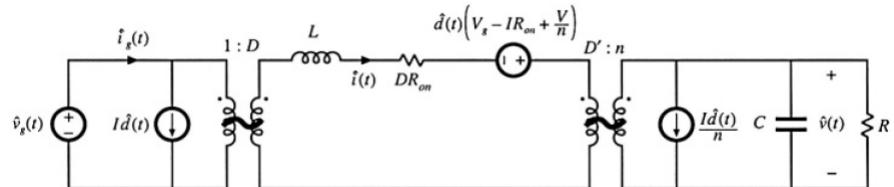
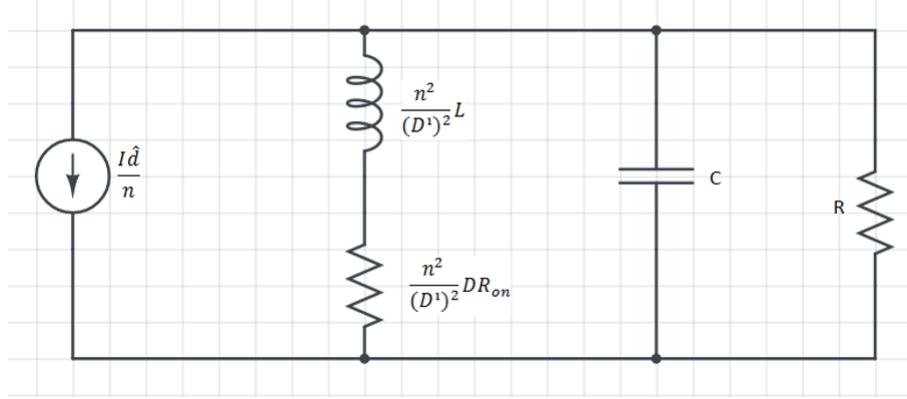


Figure 9: Small-signal ac equivalent circuit model of Flyback converter.

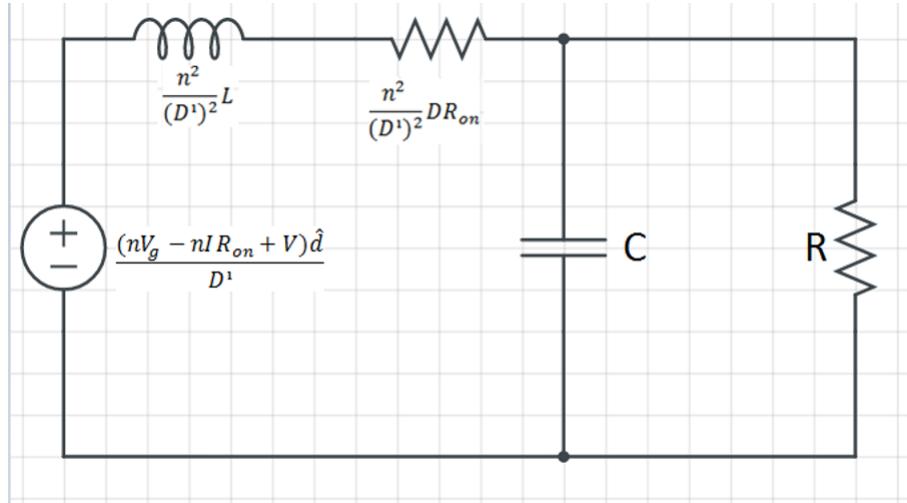
1. Killing current source:



$$\frac{\tilde{V}}{\tilde{d}} = \frac{(nV_g - nIR_{on} + V)}{D'} * \frac{R \parallel \frac{1}{sC}}{(sL + DR_{on}) \frac{n^2}{D'^2} + (R \parallel \frac{1}{sC})}$$

$$\frac{\tilde{V}}{\tilde{d}} = \frac{(nV_g - nIR_{on} + V)D'R}{n^2(sL + DR_{on})(sCR + 1) + D'^2R}$$

2. Killing voltage source ( $R_{on}$  is ignored for ideal case):



$$\begin{aligned}
\frac{V(s)}{d(s)} &= \frac{-I(sL)nR + D'R_nV_g + VD'R}{(sL + DR_{on})(sCR + 1)n^2 + RD'^2} \\
I &= \frac{I_s}{D'} \quad I_s = \frac{D}{D'}n \frac{V}{R} \\
V &= \frac{D}{D'}nV_g \quad I = \frac{D}{D'^2}n^2 \frac{V_g}{R} \\
\frac{V(s)}{d(s)} &= \frac{(\frac{-D}{D'^2}n^3(sL) + D'R_n + DnR)V_g}{(sL)(sCR + 1)n^2 + RD'^2} \\
\frac{V(s)}{d(s)} &= \frac{nV_g(-\frac{D}{(1-D)^2}n^2(sL) + R)}{s^2n^2RLC + sL_n^2 + R(1-D)^2} \\
\frac{V(s)}{d(s)} &= \frac{nV_g}{(1-D)^2} \frac{(-Dn^2sL + (1-D)^2)R}{s^2n^2RLC + sL_n^2 + R(1-D)^2} \\
&= \frac{nV_g}{(1-D)^2} \frac{(1 - \frac{s}{\frac{(1-D)^2}{Dn^2L}})}{(1 + \frac{s}{\frac{(1-D)^2R}{L_m^2}} + \frac{s^2}{\frac{(1-D)^2}{n^2LC}})}
\end{aligned}$$

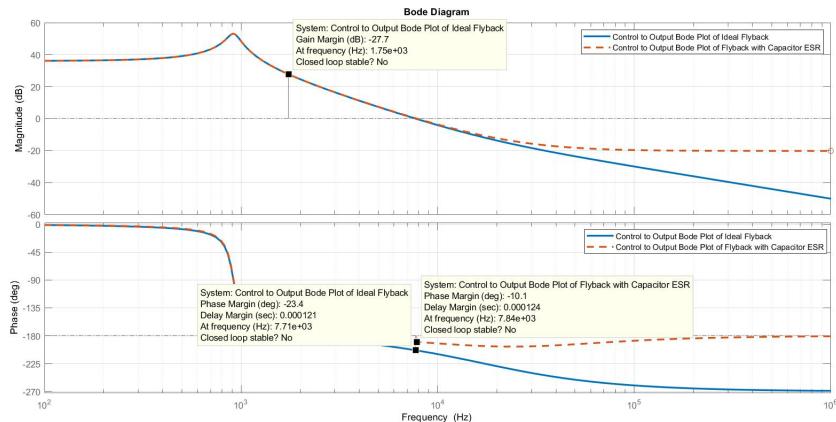


Figure 10: Control-to-output transfer function bode plots of the designed Flyback converter .

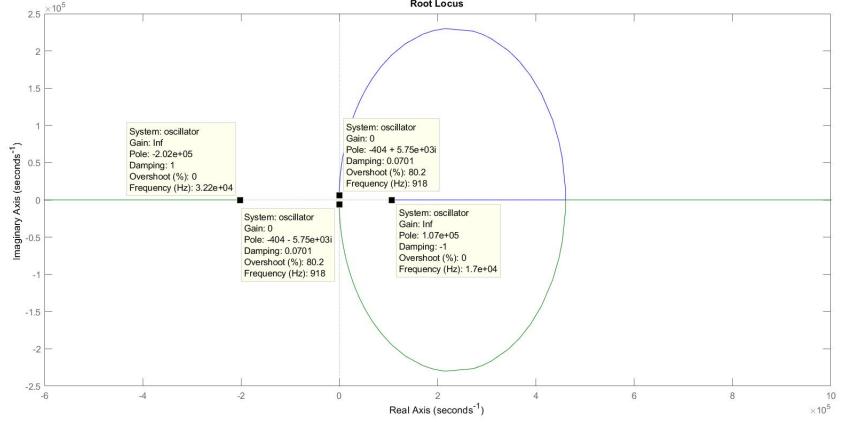


Figure 11: Root locus of the designed Flyback converter's control-to-output transfer function.

The open-loop characteristic of our Flyback converter and the zero/pole locations of the control-to-output transfer function of it are illustrated in Figure 10 and 11. Without a compensator, the design is not stable which can be observed from both root loci and negative phase margin. To achieve a stable closed-loop system, at least  $40^0 - 45^0$  phase margin is necessary. Moreover, ESR of the output capacitor is very important because it introduces an extra zero to system. In this respect, a Type-3 error amplifier is designed and implemented by following steps:

1. Assume  $V_{osc}^{peak} = 1.8V$
2. Select crossover frequency  $\frac{f_{sw}}{10} < f_c < \frac{f_{sw}}{5}$   
Let's choose it  $f_c = \frac{f_{sw}}{5} = 8kHz$ .

3. Location of poles and zeros:

$$f_{ESR} > \frac{f_{sw}}{2} > f_c > f_{LC} \quad \text{Type-3B}$$

$$f_{LC} = 918\text{Hz}$$

$$\frac{f_{sw}}{2} = 20\text{kHz}$$

$$f_{ESR} = 32.2\text{kHz}$$

$$f_{RHPZ} = 17\text{kHz}$$

$$f_c = 8\text{kHz}$$

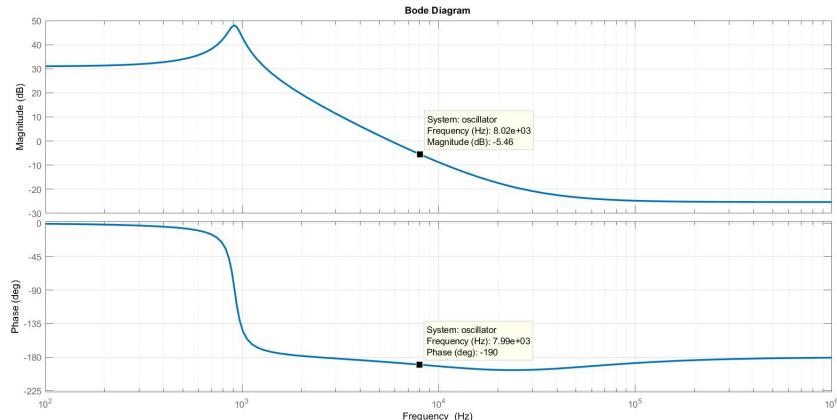


Figure 12: Bode plot of control-to-output transfer function, marked  $f_c$ .

4. Determine needed phase and gain at  $f_c$  from Figure 12:

at  $f_c = 8\text{kHz}$ :

$$\text{phase} = -190^0 \quad \text{gain} = -5.6\text{dB}$$

$$\Theta_{\text{compensator}} = 45 - (-190) = 235^0$$

$$\text{Gain}_{\text{compensator}} = 5.4\text{dB}(1.862)$$

5. Derive the Type-3B compensator' components by using K-method, as illustrated in Figure 13:

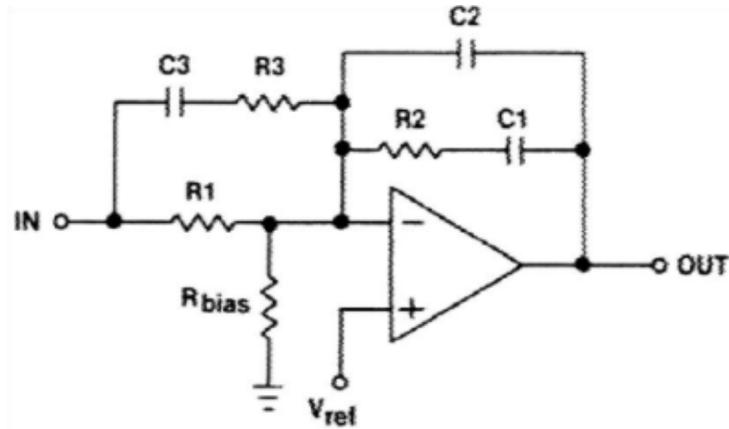


Figure 13: Schematic of the designed Type-3 compensator.

Start with  $R_1 = 1k\Omega$

$$R_2 = \frac{|G(jw_c)|}{\sqrt{K}} = \frac{1.862 * 1000}{\sqrt{42.21}} = 286 \approx 270\Omega$$

$$C_1 = \frac{\sqrt{K}}{w_c R_2} = \frac{\sqrt{42.21}}{2\pi * 8000 * 270} = 479 \approx 470\mu F$$

$$C_2 = \frac{1}{w_c R_2 \sqrt{K}} \approx 10nF$$

$$C_3 = \frac{\sqrt{K}}{w_c R_1} \approx 130nF$$

$$R_3 = \frac{1}{w_c \sqrt{K} C_3} \approx 30\Omega$$

$$V_{ref} = V_{out} \frac{R_{bias}}{R_{bias} + R_1}$$

$$2.5 = 15 * \frac{R_{bias}}{R_{bias} + 1000}$$

$$R_{bias} = 200\Omega$$

6. Derive transfer function of the compensator:

$$\begin{aligned}
 TF &= -\frac{R_1 + R_3}{R_1 R_3 C_2} * \frac{(s + \frac{1}{R_2 C_1})(s + \frac{1}{(R_1 + R_3)C_3})}{s(s + \frac{C_1 + C_2}{R_2 C_1 C_2})(s + \frac{1}{R_3 C_3})} \\
 &= -(3.43 * 10^6) * \frac{s^2 + 17.58 * 10^3 s + 76.5 * 10^6}{s^3 + 7.11 * 10^5 s^2 + 12.6 * 10^1 0s}
 \end{aligned}$$

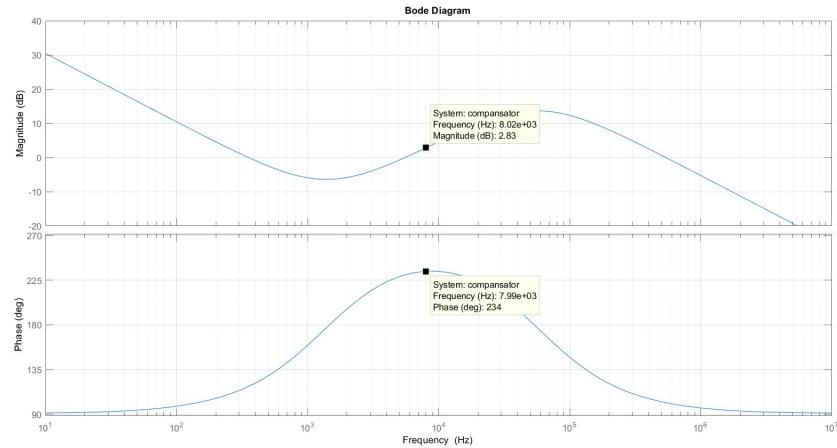


Figure 14: Bode plot of the designed Type-3B compensator.

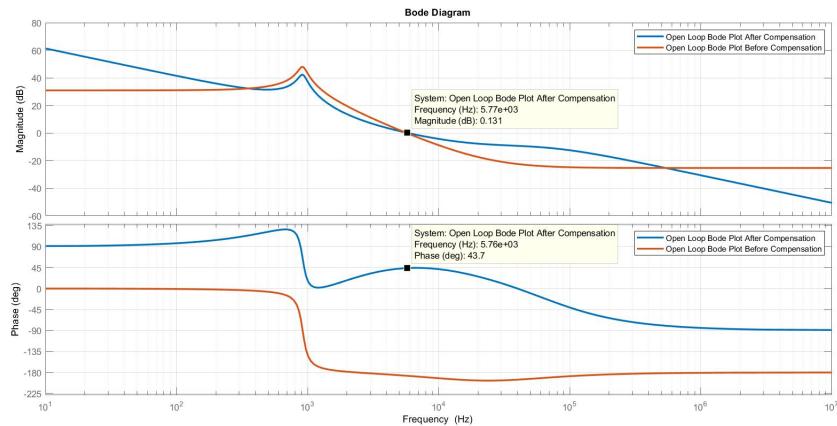


Figure 15: Bode plot of the Flyback converter with compensator.

With the designed Type-3B compensator, our system achieved  $\Phi_{margin} = 43.7^\circ$ , which ensures the system stability, and almost the desired crossover frequency, can be seen in Figure 14 and 15. The error of desired crossover frequency is the result of available components constrain.

### 3.2 Choosing Controller

## PWM Controller:

In order to make regulation for the output voltage, we need a some kind of feedback to some reference value, For that purpose, instead of using opamps to realize error amplifier, we have used “LT1246” PWM modulator. It has a wide range of oscillator frequency including the one that we have choose for the implementation which is 40kHz.

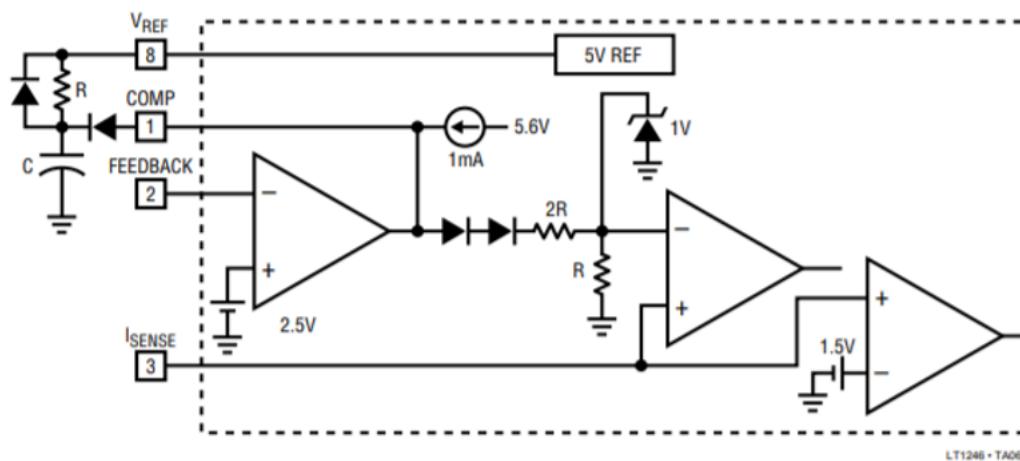


Figure 16: Error amplifier of the Lt1246.

It has its own internal error amplifier, which has a reference voltage of 2.5 Volt, therefore, in order to regulate 15 volt output voltage, we need to divide that value to be equal to 2.5 volt by creating voltage divider network. Also it has a "RT/CT" pin that can be connected to an "RC" circuit to adjusting its ramp waveform frequency.

## 4 Efficiency and Thermal Analysis

In power supply design, the electrical efficiency of the overall circuit and the junction temperature of semiconductor devices, which handle the conversion of power to a usable form, are very important points of design process.

MOSFET, diode and transformer losses are main elements of the scope of our

thermal design. Temperature of these components directly effect the performance of overall system, so we need to deal with it. To achieve better performance and thermal design, the thermal equivalent model is used, as illustrated in Figure 17 and 18.

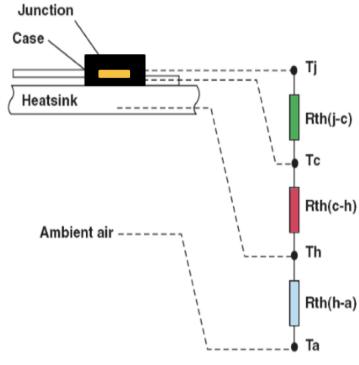


Figure 17: Thermal equivalent model of a semiconductor.

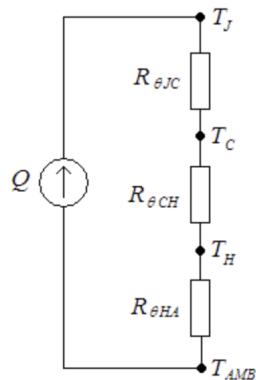


Figure 18: Electrical equivalent model of thermal model.

According to these models, two heat sinks were implemented to PCB design for Mosfet and secondary side diode.

#### 4.1 Mosfet Heatsink

Conduction and switching losses are two main components of Mosfet' losses which should be taken into account for heat sink selection. The characteristic of thermal resistance of Mosfet and operating temperature interval were found in datasheet. In Figure 18, current source represents dissipated total power on the semiconductor and can be derived for Mosfet as below:

$$\begin{aligned}
 P_{tot} &= P_{conduction} + P_{sw} \\
 P_{conduction} &= I_{ds,rms}^2 R_{ds,on} \\
 &= (4.5)^2 * 0.15 \approx 3.04W
 \end{aligned}$$

$R_{ds,on}$  depends on temperature, as seen in Figure 19, and operating junction temperature is chosen  $90^0$ .

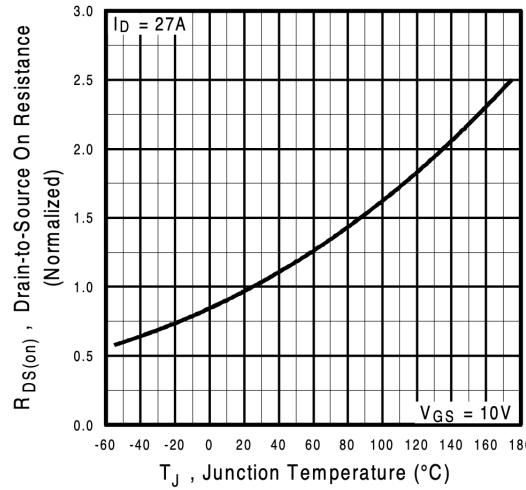


Figure 19:  $R_{ds}$  vs temperature characteristic of IRF540N.

$$\begin{aligned}
P_{sw} &= \frac{1}{2}(V_{ds}^{max} I_{ds}^{peak}) t_f f_s \\
&= \frac{1}{2} * (48 * 8.5) * 33 * 10^{-9} * 4 * 10^4 \approx 0.27W
\end{aligned}$$

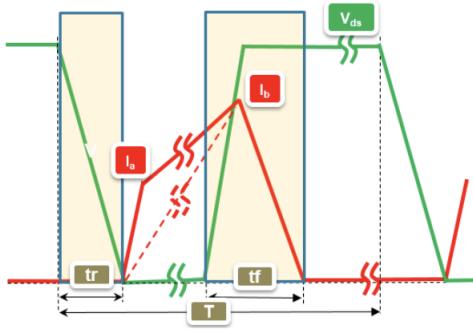


Figure 20: Inductive load switching.

$$\begin{aligned}
P_{tot} &= 3.04 + 0.27 = 3.31W \\
R_{j-c} &= 1.1C^0/W \quad R_{c-h} = 0.5C^0/W \\
T_{junction} - T_{ambient} &= P_{tot} * (R_{j-c} + R_{c-h} + R_{heatsink}) \\
(90^0 - 25^0) &= 3.31W * (1.6 + R_{heatsink}) \\
R_{heatsink} &= 18C^0/W
\end{aligned}$$

As seen in Figure 21, HSE-B20250-040H is chosen for perfect fit and desired thermal resistance at operating point. It is TO-220 package heatsink which directly fit our Mosfet with same package.

## PERFORMANCE CURVES

### HSE-B20250-040H

Power (W)	Heatsink Temperature Rise Above Ambient ( $\Delta T = Ths - Ta$ ) (°C)		
	Natural Conv.	200 LFM	400 LFM
0	0	0	0
1	19.57	4.28	3.44
2	35.77	8.76	6.98
3	49.68	13.06	10.36
4	62.71	17.44	13.88
5	74.79	21.93	17.35
6	85.46	26.39	20.74
7	97.48	30.77	24.33
8	108.09	35.20	27.77
9	117.16	39.64	31.31
10	127.50	43.98	34.86

Ths: "hot spot" temperature measured on the heatsink  
Ta: ambient temperature

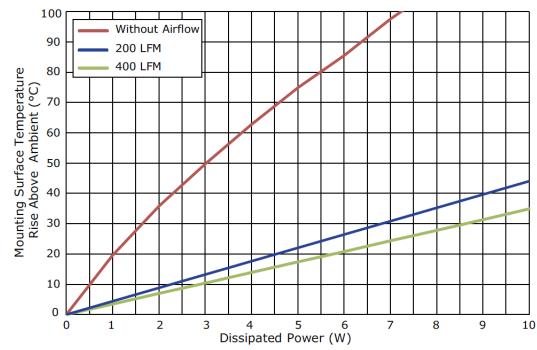


Figure 21: HSE-B20250-040H performance curve.

## 4.2 Diode Heatsink

To find the correct heatsink same procedure and models has followed as Mosfet. The diode can operate maximum 150° and we want to operate at 100°.

$$I_D \approx I_o = 4A \quad V_D = 0.47V \quad R_{on} = 0.0133\Omega$$

$$P_D = I_D * V_D + I^2 R_{on} = 2.12W$$

$$R_{j-c} = 1.5C^0/W$$

$$T_{junction} - T_{ambient} = P_{tot} * (R_{j-c} + R_{heatsink})$$

$$\frac{75}{2.12} - 1.5 = R_{heatsink}$$

$$= 33.87C^0/W$$

As seen in Figure 22, HSS-B20-0635H is chosen for perfect fit and desired thermal resistance at operating point. It is TO-220 package heatsink which directly fit our diode with same package.

## PERFORMANCE CURVES

### HSS-B20-0635H

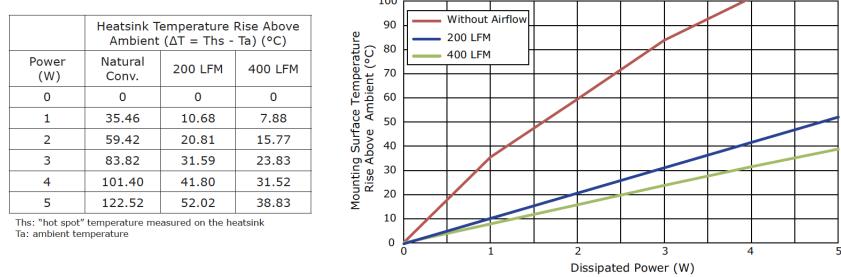


Figure 22: HSS-B20-0635H performance curve.

### 4.3 Transformer Losses

$$P_{core} = 568.8 \text{ mW/cm}^3$$

$$\text{Volume of selected core} = 1.87 \text{ cm}^3$$

$$\text{Therefore core loss} = 568.8 * 1.87 = 1.063 \text{ W}$$

$$P_{cu} = I_{pri(rms)}^2 * R_{pri} + I_{sec(rms)}^2 * R_{sec} = 4.5222 * 0.0262 + 6.6732 * 0.0131 = 1.119 \text{ W}$$

$$P_{transformer} = 2.27 \text{ W}$$

## 5 PCB Design

A printed circuit board (PCB) mechanically supports and electrically connects electrical or electronic components using conductive tracks, pads and other features etched from one or more sheet layers of copper laminated onto and/or between sheet layers of a non-conductive substrate. Components are generally soldered onto the PCB to both electrically connect and mechanically fasten them to it.

After the introduction, we are starting to mention about the process, challenges and solution of these challenges in flyback PCB design.

In this project, we have used Kicad pcb design tool to implement the design. Firstly all of the schematic of the circuit is implement by using the symbols. This process is important because we will next generate a netlist from these connections and later on, we will import this netlist in the PCB design layout.

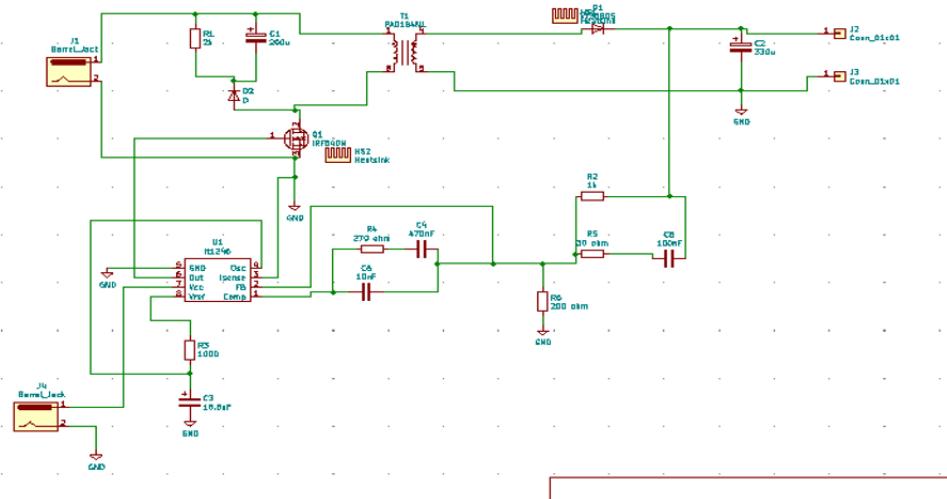


Figure 23: Schematic of the Flyback circuit.

As seen in Figure 23, all the connections between the components are done however, although it can not be understood from the figure, we have faced with several challenges in the implementation of this process because there isn't any LT1246 symbol in the Kicad libraries thus, we had to make it ourselves, for that purpose, Symbol editor tool of the kicad is utilized to create that symbol because we have the data sheet and we know how many pins that we need to create that block.

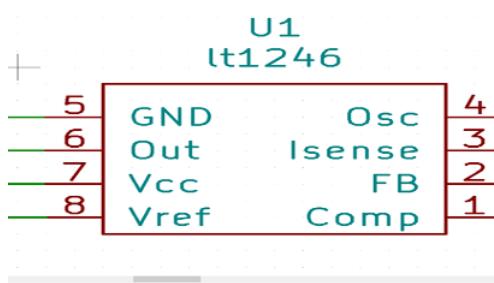


Figure 24: Symbol of the “LT1246” Controller IC.

After implementing the missing component symbol, placing resistor and capacitor symbols are straight forward. Therefore, in the next step, after completing the connections of the symbols, in the same page, we have started to assign footprints to symbols. And since, we have chosen nearly all of the components from digikey, this process was also straight forward but in order to assign a footprint to “Controller IC” we need to check its datasheet because there was

not recommended assignment for that component.

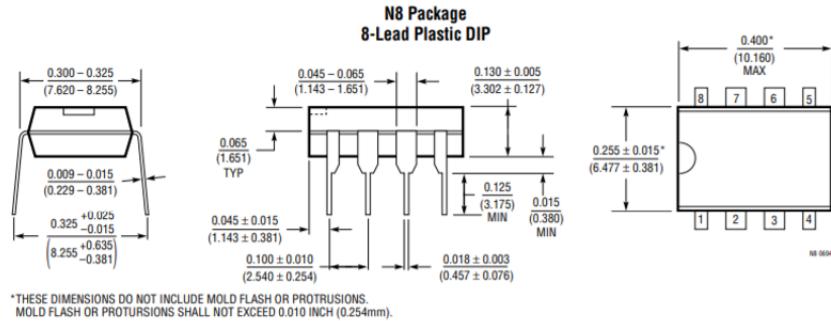


Figure 25: Package information of Lt1246.

In datasheet of that component, we have the package information and its package is common THT SO-DIP-8 package which can be seen for the most of the opamps, therefore it was available in the Kicad footprint library and it was assigned to that footprint.

After assigning of footprints, we have run the “electric rules checker” tool to see whether we can have any connection problems, after observing the checker, we have generated a netlist to export in to “layout” page.

In the second step, we were working on “PCB Layout” page to adjusting main PCB design, in that page we have created several types of tracks for the connection of the components in terms of how much current that these tracks will carry. In order to evaluate these track widths we have used “PCB track width calculator” webpage.

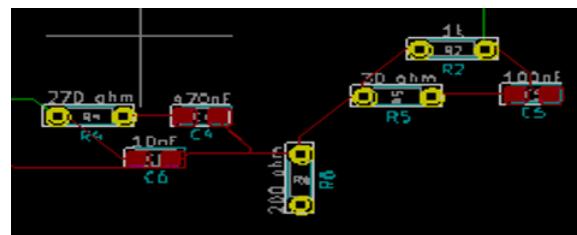


Figure 26: A view from the PCB layout page.

**Printed Circuit Board Width Tool**

This Javascript web calculator calculates the trace width for printed circuit board conductors for a given current using formulas from IPC-2221 (formerly IPC-D-275).

**Inputs:**

Current	1	Amps
Thickness	1	oz/ft <sup>2</sup> <input type="button" value="▼"/>

**Optional Inputs:**

Temperature Rise	10	Deg <input type="button" value="C"/> <input type="button" value="F"/>
Ambient Temperature	25	Deg <input type="button" value="C"/> <input type="button" value="F"/>
Trace Length	1	inch <input type="button" value="mm"/>

**Results for Internal Layers:**

Required Trace Width	0.781	mm <input type="button" value="in"/>
Resistance	0.0164	Ohms
Voltage Drop	0.0164	Volts
Power Loss	0.0164	Watts

**Results for External Layers in Air:**

Required Trace Width	0.300	mm <input type="button" value="in"/>
Resistance	0.0427	Ohms
Voltage Drop	0.0427	Volts
Power Loss	0.0427	Watts

Figure 27: Captured when the controller output to gate connection width calculated.

After calculating the track widths of all the connections, footprints are connected to each other. However, since the implementation of PCB design requires back and front copper layers, we have utilized from this process in several ways. For example since it is hard to jump a connection on another one in the PCB, we have used “back copper” layer for some connections to avoid wrong nodes and connections.

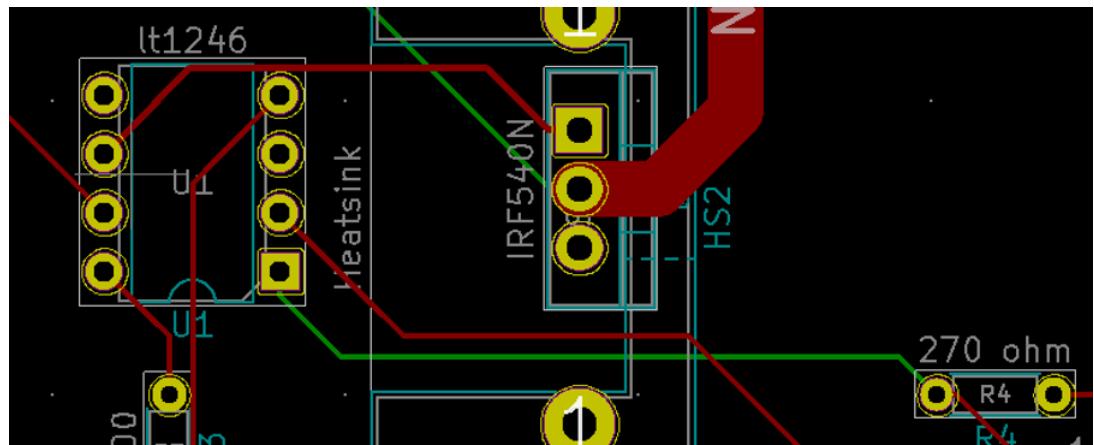


Figure 28: Illustration of back and front copper traces.

After checking the design warning and mistakes which is created by “design rules checker”, finally, we have connected all the grounds of the circuits by using front and copper layers. so, the layout process is completed.

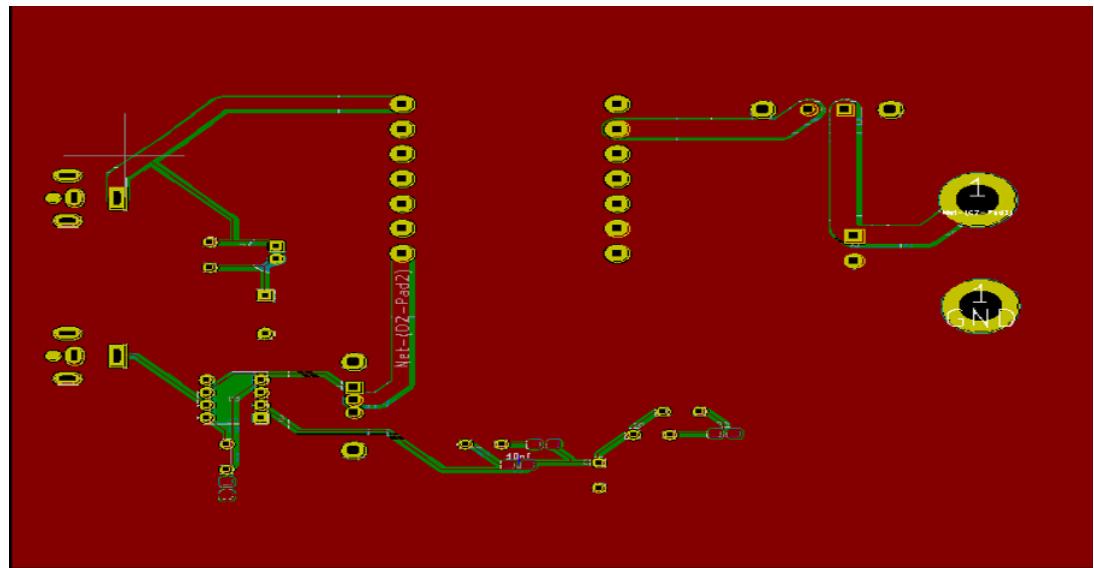


Figure 29: Final version of the PCB layout page.

After we have created all the layers inside the “Flyback” converter, next process is producing “gerber files” to make the PCB ready to be produced and it can be done using “plot” button of the PCB layout page and following several straightforward steps.

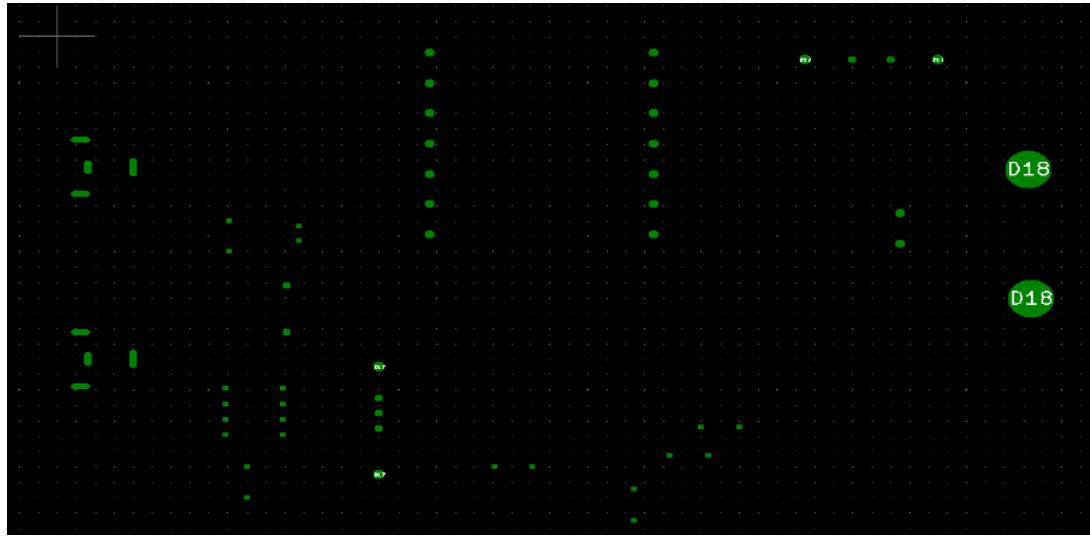


Figure 30: Opening “gerb view of drill files”.

Finally, we have taken a quote from the given website. (Bill of materials is on the github)

**Pricing And Build Time**

PCB Price	Price Comparison Matrix		
	Build Time	Qty	Total
<input checked="" type="checkbox"/> 6-7 days	1000	\$6781	

**Tip:**Final price can be negotiated.

Shipping Cost:

UNITED STATES OF AMERICA ▲ DHL ▼

**DHL** 5-7 Days , wt : 59.721 kg **\$506**

CHN Time Zone(GMT+8): 2020/6/25 4:32:43

Payment before 2020/06/25 06:00 (GMT+8 Only PCB)

Delivery time 2020/7/1 AM Estimation 2020/7/7

PCB Cost: US \$ 6781  
Shipping: US \$ 506  
**Total: US \$ 7287**

Email

## 5.1 3D Views of Design

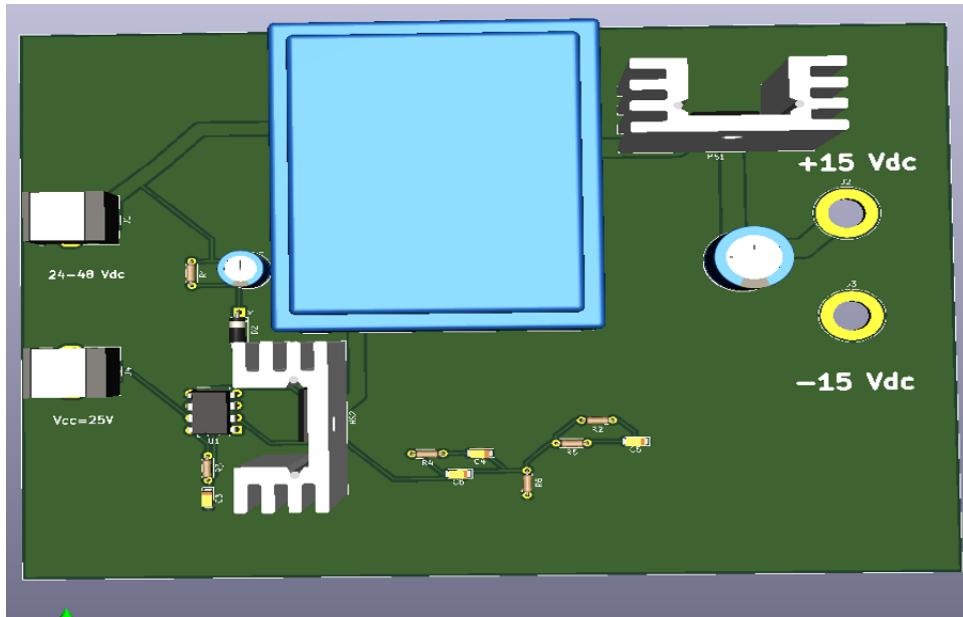


Figure 31: Top view of the circuit.

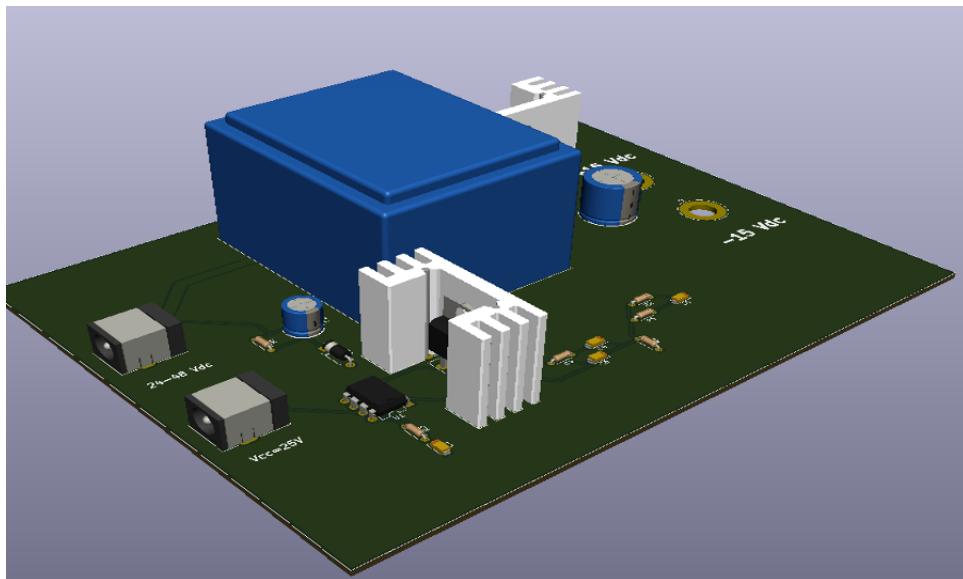


Figure 32: Side view of the circuit.

## 6 Test Results

### 6.1 Line Regulation

#### 6.1.1 With Controller

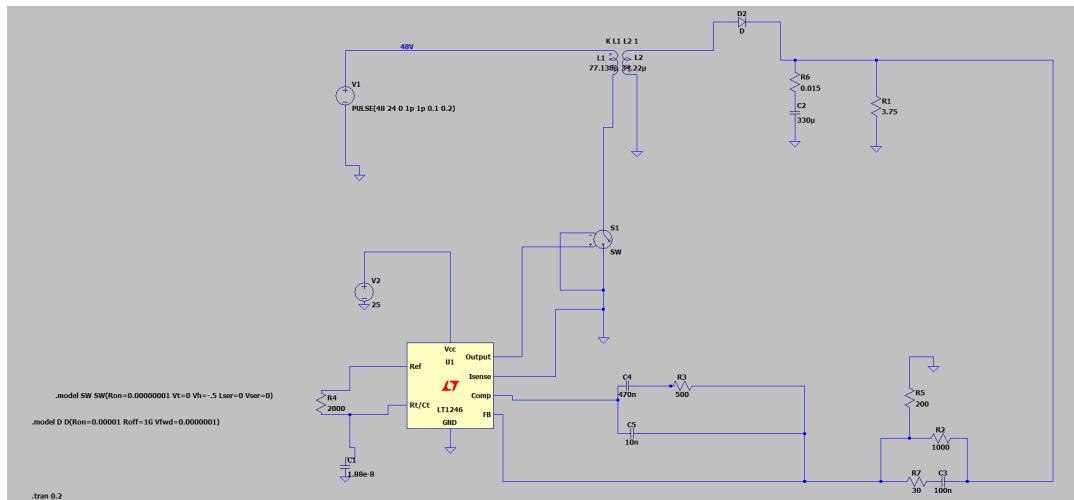


Figure 33: Circuit schematic of LtSpice model with controller.

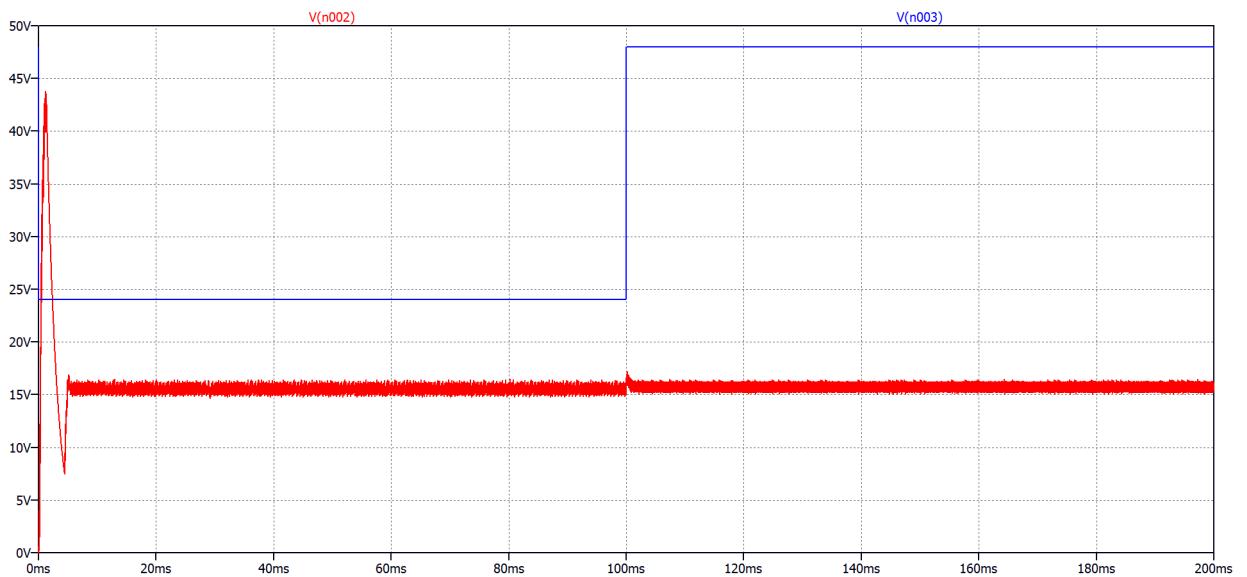


Figure 34: Output step response with controller.

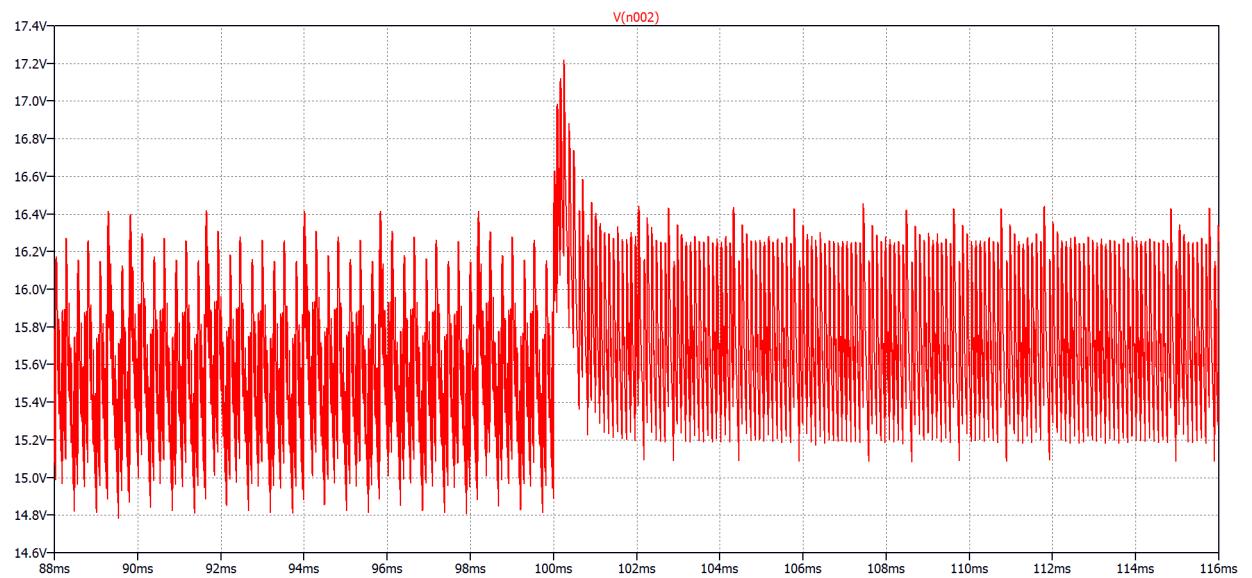


Figure 35: More detailed output step response with controller.

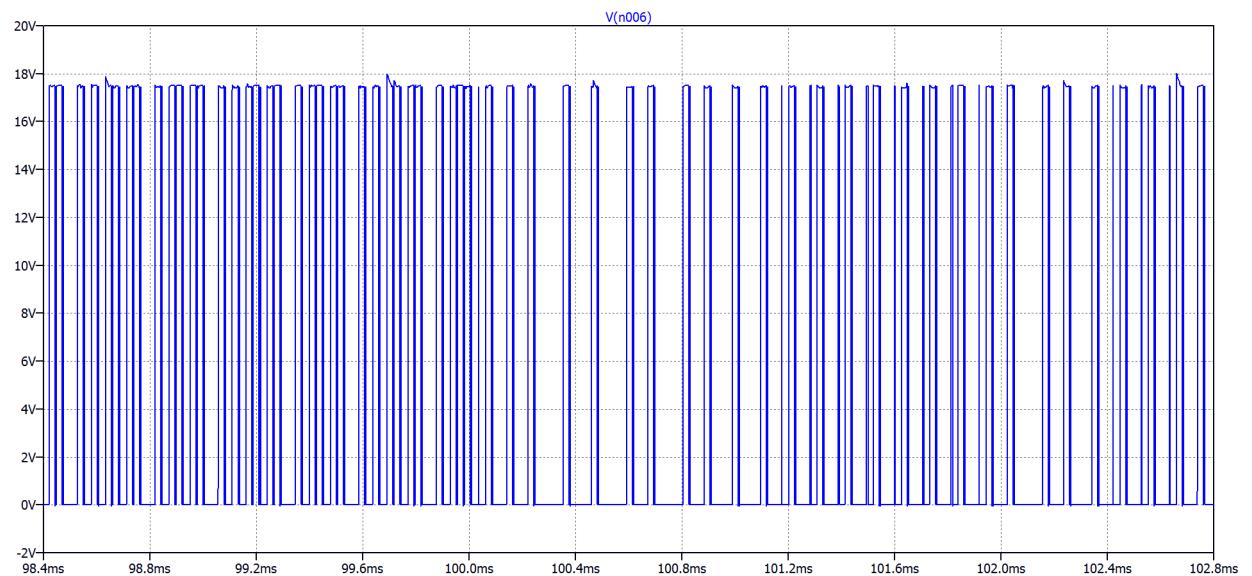


Figure 36: Duty cycle(gate signal) with controller.

### 6.1.2 Without Controller

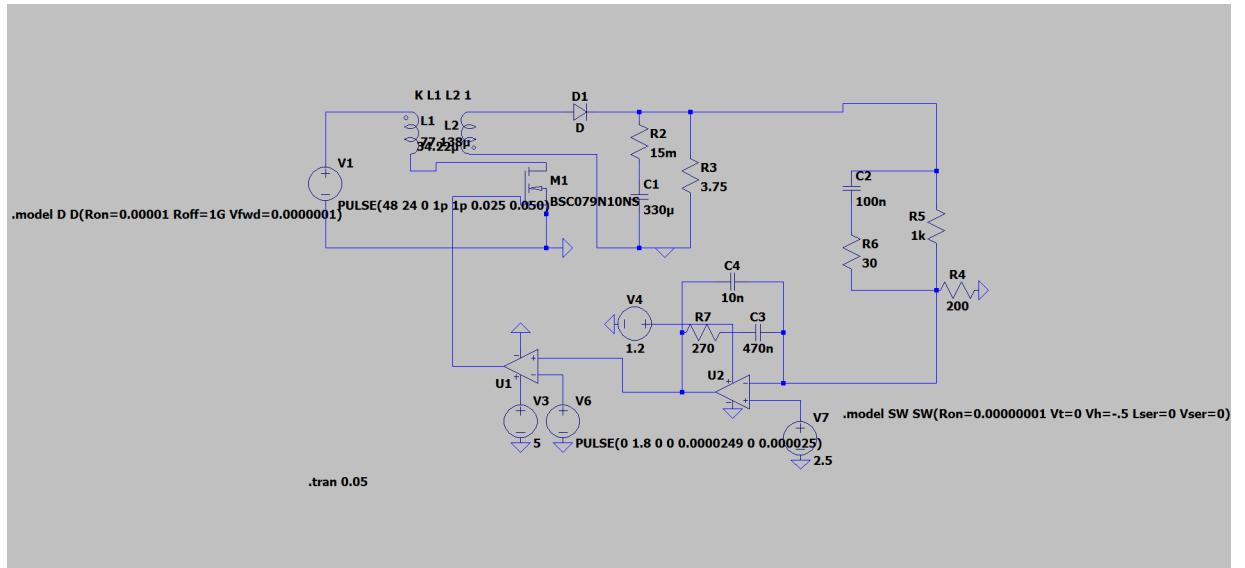


Figure 37: Circuit schematic of LtSpice model without controller.

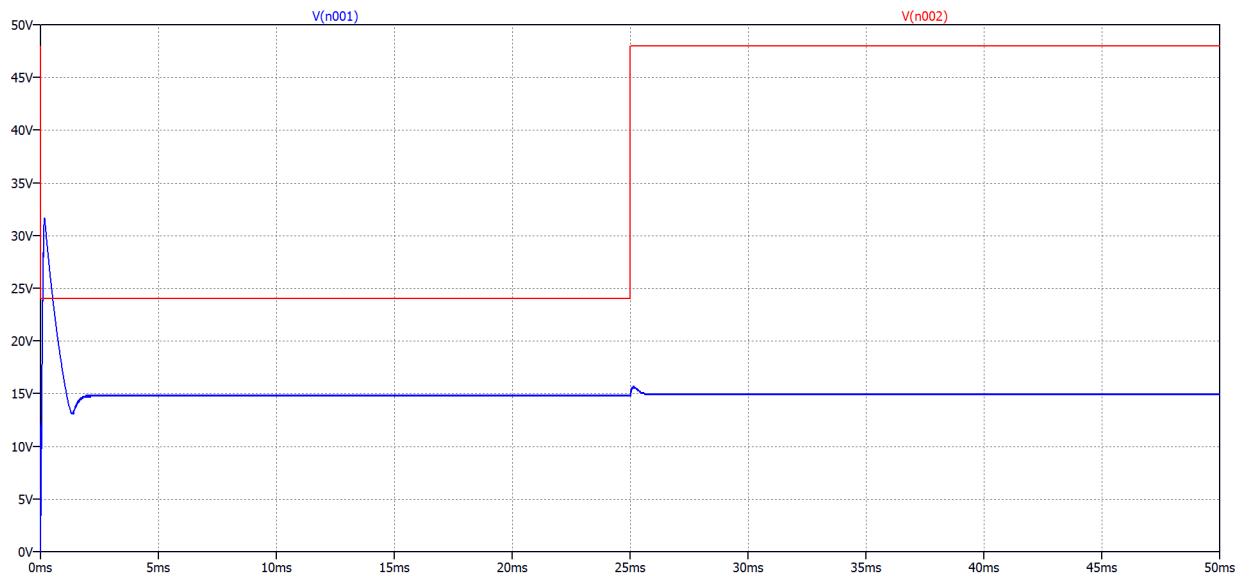


Figure 38: Output step response without controller.

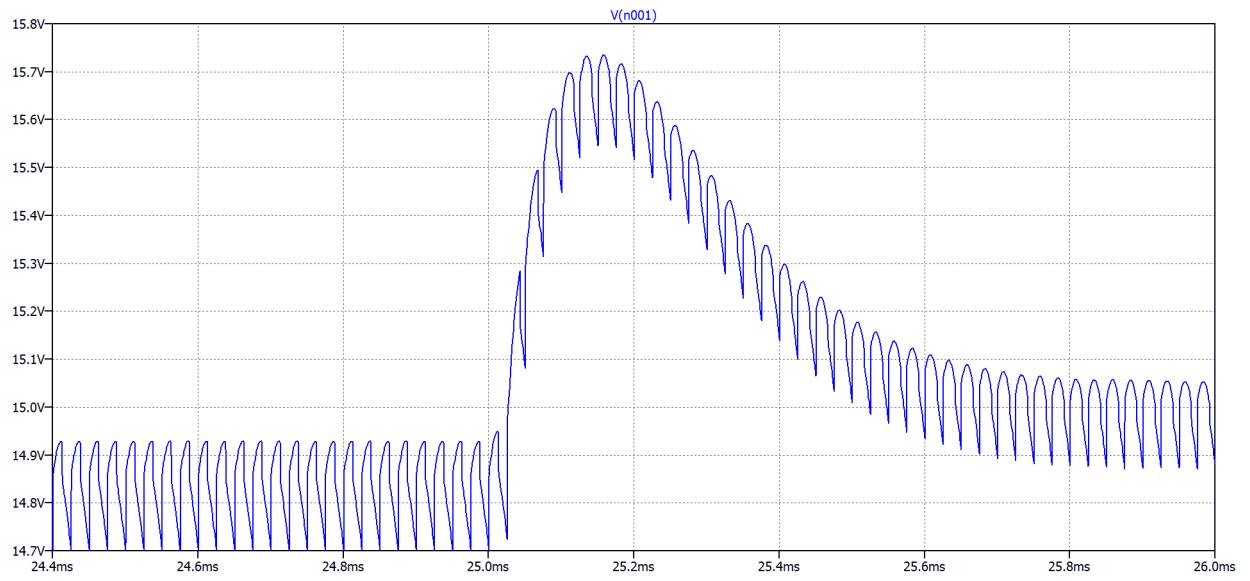


Figure 39: More detailed output step response without controller.

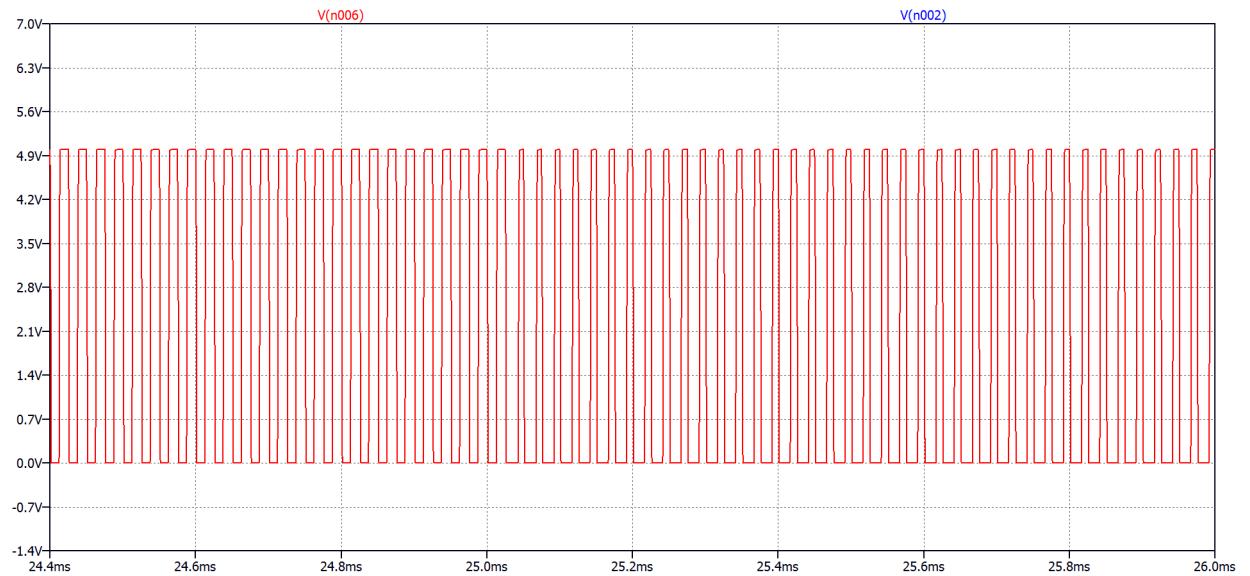


Figure 40: Duty cycle(gate signal) without controller.

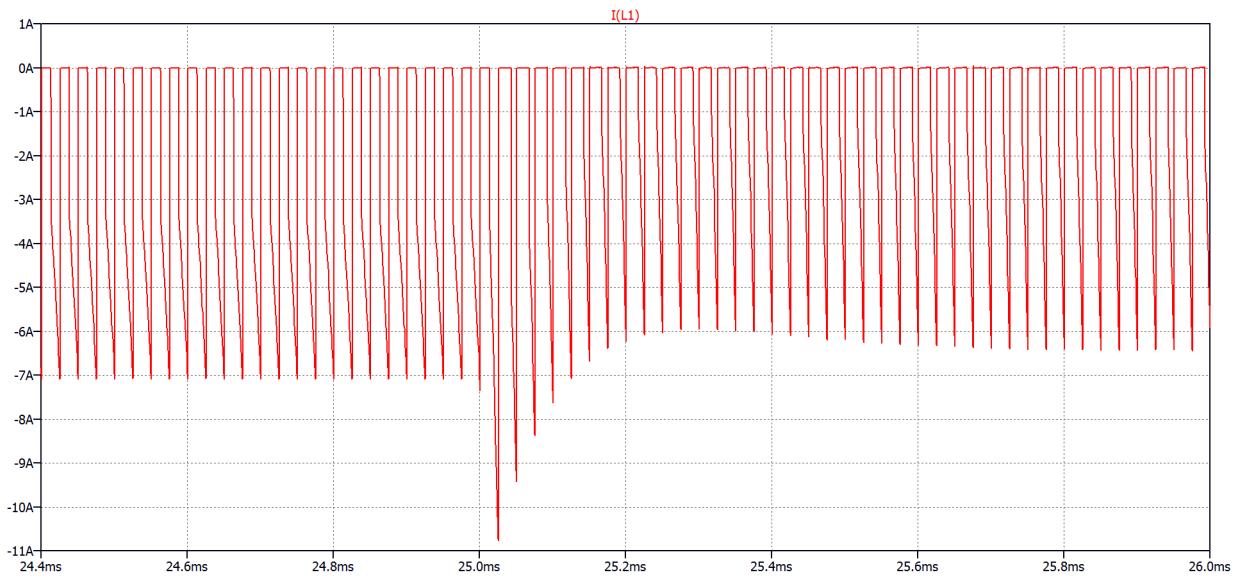


Figure 41: Primary inductance current without controller.

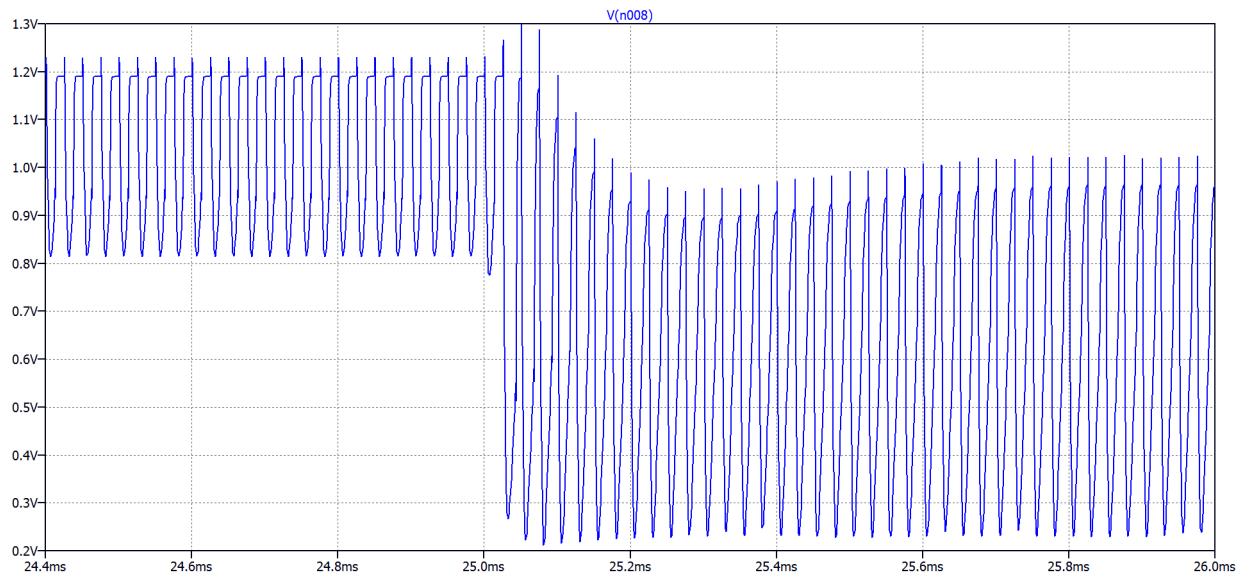


Figure 42: Error amplifier output without controller.

## 6.2 Load Regulation Test

In order to test the load regulation of the system we simply connect a parallel load with the same resistance to the output. Initially, circuit starts with full-load or half-load but since there is a switch which series with the additional load, we can control its existence in the circuit. in other words we can make “On” and “OFF” to the mosfet thus connecting and disconnecting the parallel resistance at the output.

### 6.2.1 Half load to full load

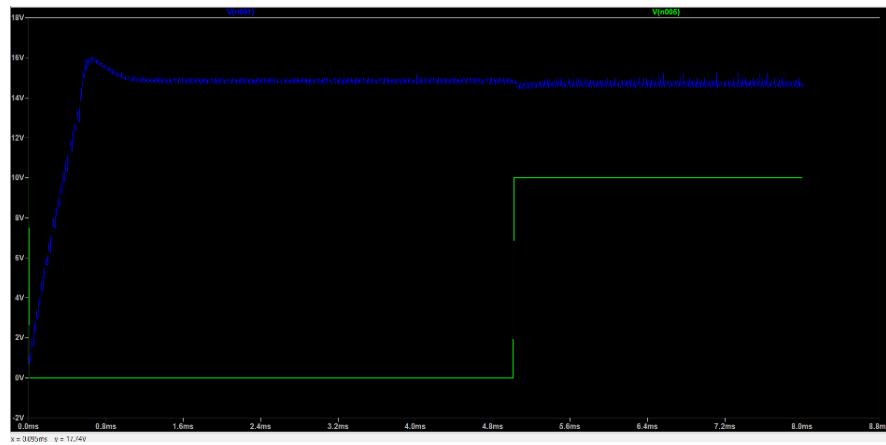


Figure 43: Half load to full load.

### 6.2.2 Full load to half load

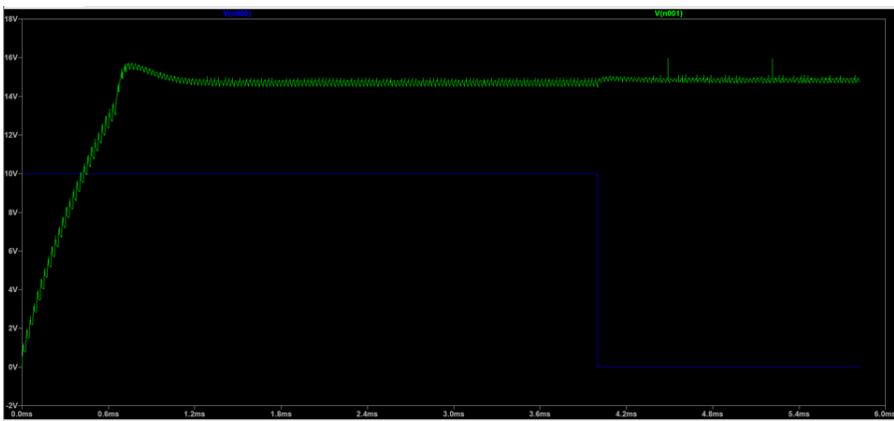


Figure 44: Full load to half load.

As we can see from the Figure 43 and 44, controller can react fastly and return the output voltage to its reference however returning may not be perfect since those controller are not perfect and are not linear in all the regions that the output value fallow.

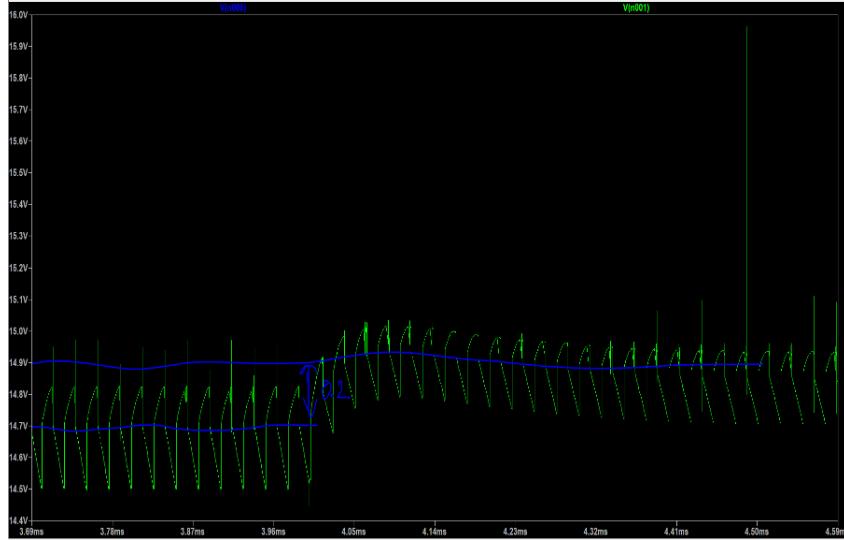


Figure 45: Measurement of the load regulation.

As can be seen from the Figure 43 and 44, difference between loads is 0.2 volt so,  $\frac{0.2}{15} = \%1.33$  load regulation which is under %2.

### 6.3 Open-loop Transfer Function Verification Test

In this test, the aim is verifying the analytically calculated transfer function by using a reliable software tool. For that purpose, we simply created a “Average Switch model” of the CCM flyback converter in the Matlab.

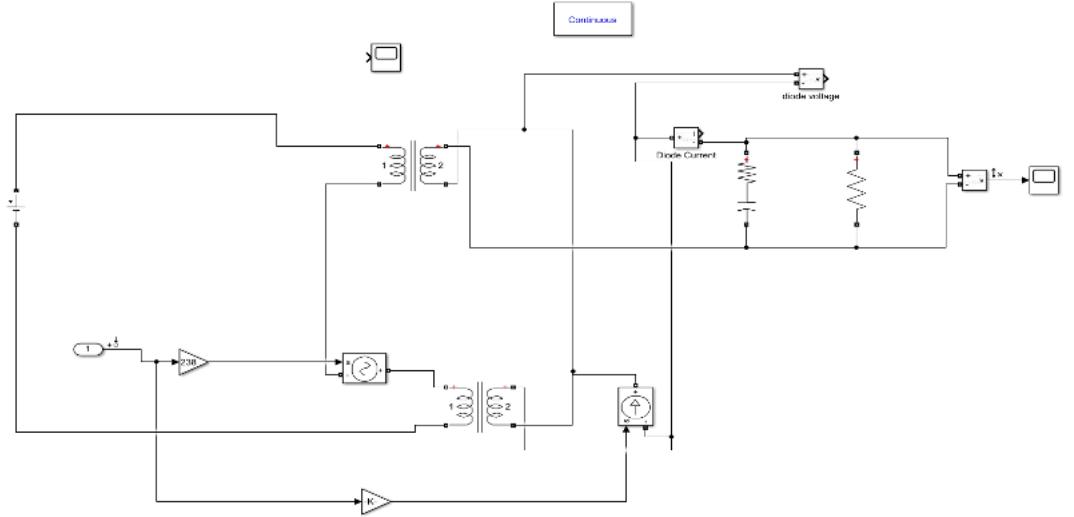


Figure 46: Average switch model of flyback converter.

By using that circuit, we just linearize the switch network which includes diode and mosfet however, there are still non-idealities in the circuit because we don't exclude input voltage in that circuit. However, linearizing those nonlinearities would become much easier compared to original circuit because linearizing duty cycle is much more harder.

Therefore, as we can understand we simply use linearizing tool of the matlab to extract bode plot and transfer function of the open-loop system.

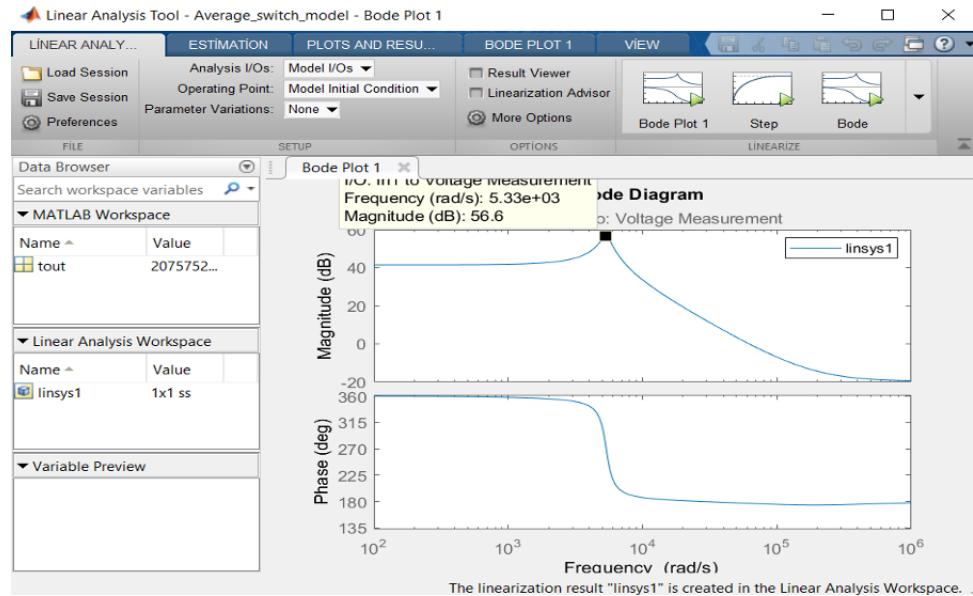


Figure 47: Bode plot of average switch network when  $V_{in} = 36V$ .

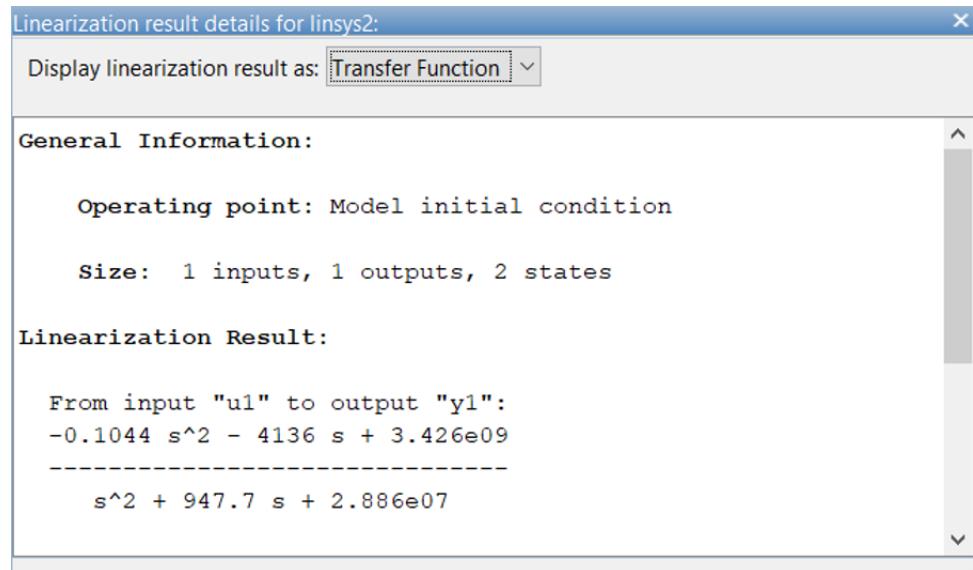


Figure 48: Extraction of transfer function from linearization tool.

As can be seen from the Figure 47 and 48, open-loop transfer functions are closely match with the analytical results.

## 6.4 Mosfet Temperature Test

In this test, we have tried to find the correct value of the mosfets junction and case temperature and comparing it with the analytical results, for that purpose, 24 volt input is given (to create worst case condition) and in lt spice there is a heat sink model which we can create the one that we choose in simulation environment. whole circuit is like below.

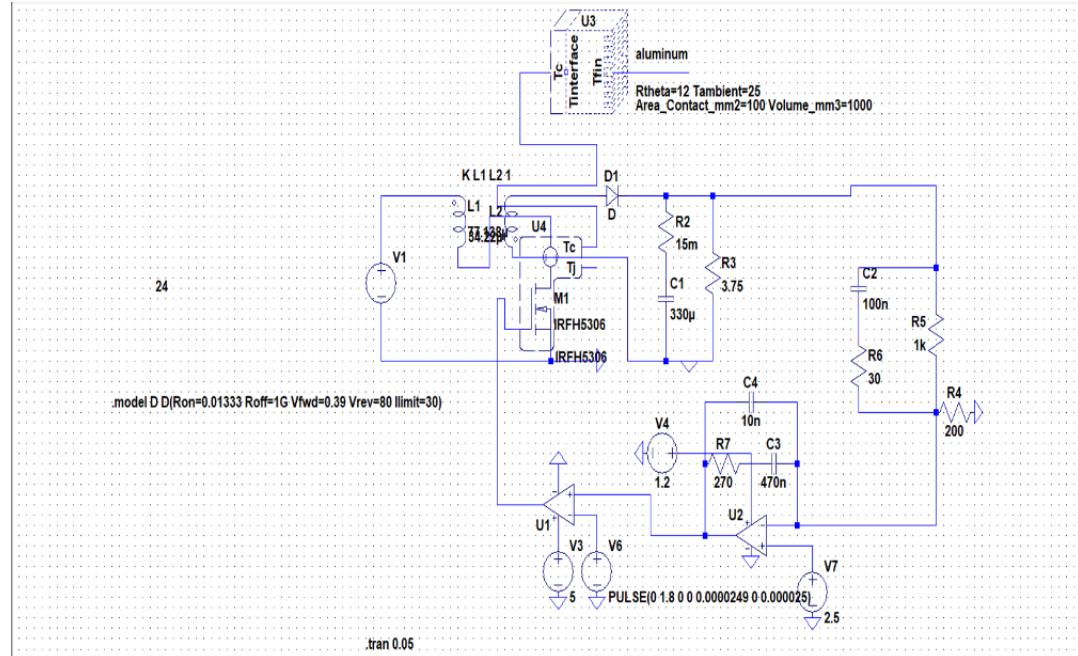


Figure 49: Thermal design simulation.

For that purpose, The junction to case and case junction resistances of the mosfer will be found which is similar to our mosfet, also, the found heatsink temperature resistance is also given.

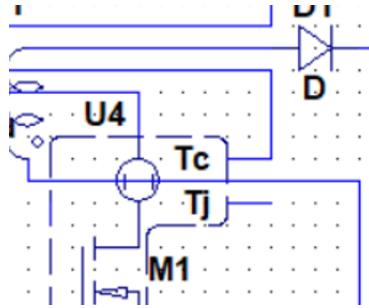


Figure 50: Tc junction.

From the above node( $T_j$ ), we have measured the combined temperature of the junction and results are as below.

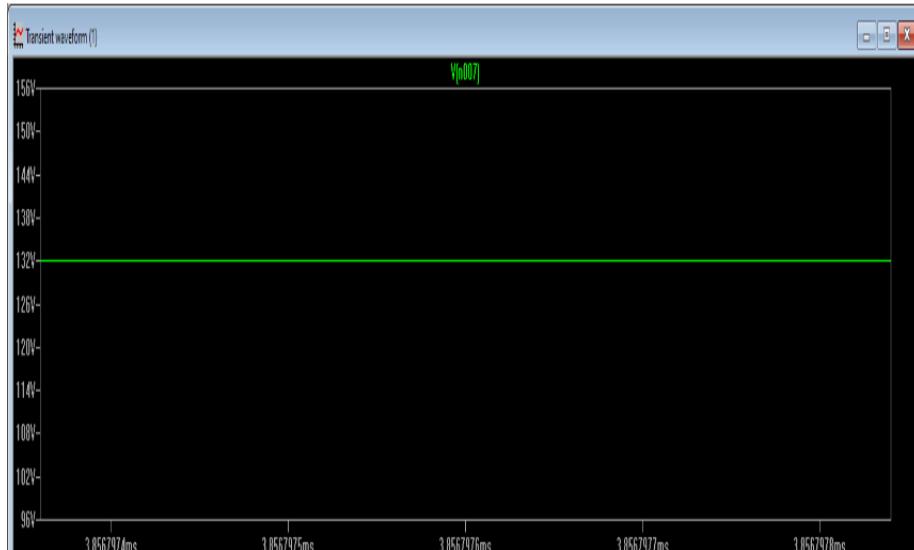


Figure 51: Junction temperature of the Mosfet.

## 6.5 Snubber Test

The test of the snubber circuit is made under the very detailed model of the Mosfet(IRF540N) to realize the real switching behaviour of the circuit together with the snubber circuit. Therefore, pre-calculated rise and fall time of the mosfet is realized by connected  $C_{ds}$  capacitor. Moreover, since we have variable input range the test is done under the worst case condition for the highest voltage stress of the mosfet that can happen  $V_{in} = 48$ .

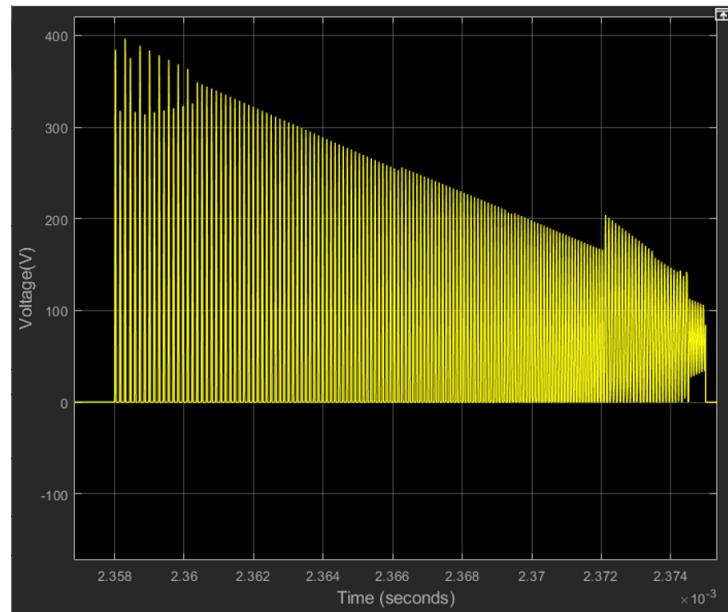


Figure 52: The voltage on switch without the snubber.

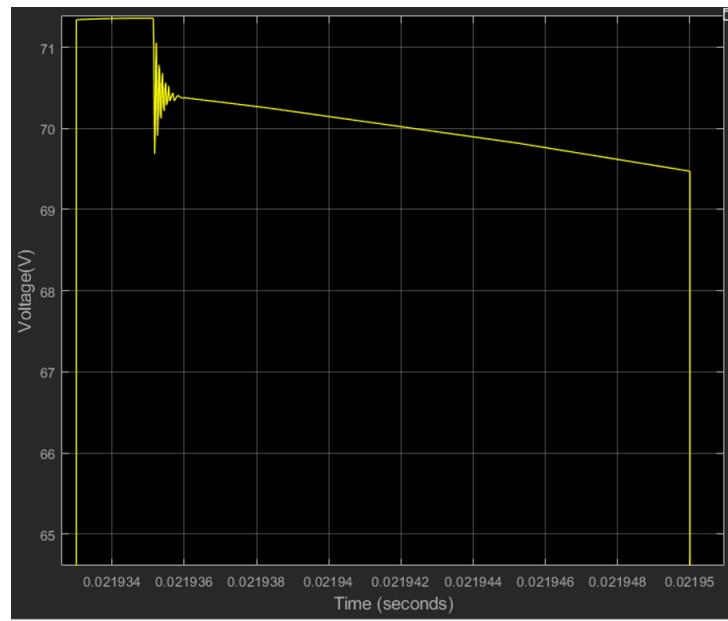


Figure 53: The voltage on switch with the snubber.

As can be seen from Figure 52 and 53, increase in the mosfet  $V_{ds}$  voltage is confined in small value thanks to voltage keeping behaviour of the snubber capacitor.

We have 100V rated mosfet(IRF540N) so it is clear that chosen component can withstand these conditions.

## 7 Bill of Materials

Q1	Package_TO_SOT_THT:T33A Id, 100V Vds, HEXF	Transistor_FET	IRF540NPBF	IRF540N	\$0.97	1
R1	Resistor_THT:R_Axial_D	Resistor	PR02000201001JR500	2k	\$0.04845	2
C1	Capacitor_THT:CP_Radi	Polarized capacitor	TVA1207.7	200u	\$1.60	1
D1	Package_TO_SOT_THT:T	Diode	VT3080S-E3/4W	VT3080S	\$1.29	1
C2	Capacitor_THT:CP_Radi	Polarized capacitor		330u	\$1.05	1
J1	Connector_BarrelJack:B	DC Barrel Jack	Connector	PJ-054	Barrel_Jack	\$0.81
U1	Package_DIP:DIP-8_W7	Controller IC	New_Library_0	LT1246CN8#PBF	lt1246	\$2.95
R3	Resistor_THT:R_Axial_D	Resistor	PR02000201001JR500	1k	\$0.04845	1
C3	Capacitor_THT:C_Disc_	Polarized capacitor	C0603C183K5RACTU	18.8nF	\$0.01472	1
T1	Transformer_THT:Transi	SMT Gate Drive Transf	Transformer	MadenTURKEY	0	
J2	Connector:Banana_Jack:	Generic connector, sing	Connector_Generic	symbolize Output Holes	Conn_01x01	
J3	Connector:Banana_Jack:	Generic connector, sing	Connector_Generic	symbolize Output Holes	Conn_01x01	
R2	Resistor_THT:R_Axial_D	Resistor	PR02000201001JR500	1k	\$0.04845	1
R5	Resistor_THT:R_Axial_D	Resistor	CFR-25JB-52-30R	30 ohm	\$0.1	1
C5	Capacitor_THT:C_Disc_	Unpolarized capacitor	GRM155R71C103KA01J	100nF	\$0.00238	1
			C0402C102K5RACTU			
C6	Capacitor_THT:C_Disc_	Unpolarized capacitor		10nF	\$0.0037	1
C4	Capacitor_THT:C_Disc_	Unpolarized capacitor	C0402C474K9PACTU	470nF	\$0.01176	1
R4	Resistor_THT:R_Axial_D	Resistor	CF14JT270R	270 ohm	\$0.00475	1
R6	Resistor_THT:R_Axial_D	Resistor	CF14JT200R	200 ohm	\$0.00475	1
D2	Diode_THT:D_A-405_P7	Diode	1N4007-T	D	\$0.19000	1
	Heatsink_Stone	Mechanical	HSE-B20250-040H	M	\$0.87	2

Figure 54: All components list.

### 7.1 Component Selection

#### 7.1.1 Power Handling Components

Mosfet:

As mentioned before, since rectifier operates in CCM. In order to reduce the conduction losses, a MOSFET having small ON resistance is selected. Maximum current flowing through the MOSFET is primary side peak current. Although considering RMS current is pretty enough during component selection, peak currents provides some margin and more reliable operation. Therefore,

$$I_{rated(Mosfet)} > I_{pri(peak)} = 6.6A$$

Voltage rating of the MOSFET is calculated as follows:

$$V_{rated(Mosfet)} = V_{in,max} + V_R + V_{spike}$$

Assuming expected maximum spike voltage is 30 % of maximum input voltage. Note that that spikes are decreased with a clamp circuit.

$$V_{rated(Mosfet)} = 48 + 31 + 14.4 = 93.4V$$

For that purpose, 100V 33A 0.044 ohm “IRF540NSPbF” .

Output Diode:

Similarly, in order to decrease the conduction losses, a schottky diode is chosen. and since it is fast recovery time its switching losses are also low.

$$V_{rated(diode)} = V_{out} + V_{in,max}N_{sec}N_{pri} = 39V$$

$$I_{rated(diode)} > I_{sec(peak)} = 11.32A$$

Secondary peak current is considered due to more reliable operation.

Moreover, 30% margin is added to voltage rating. At the end, a schottky diode whose ratings are over 50V and 22.32 A is selected. For this purpose, 80 V 30 A VT3080S is chosen. It's forward voltage drop is typically 0.5-0.6 V.

### 7.1.2 Snubber Components

Resistor:

Most critical component of the snubber is the resistor because it should dissipate the power which is coming from the leakage inductance. and in the snubber part finding required resistor is derived so, it is 2k ohm. and it since the voltage on the capacitor is around 20-22.5 V, it passes around 10 mA current continuously, so it dissipates about 0.2 watt power. in order to realize that operation, we choose “ PPC1.0KW-2TR-ND” 1 kohm but 2 in series, each one of them has power rating of 2W, so it can handle that operation.

Capacitor:

Capacitor value of the snubber is not that critical because as long as it can keep the voltage of itself during the switching period it means no matter the value, it can be useful in snubber circuit. Also, since it will be parallel to the primary winding during the “OFF” time of the mosfet it can bear the “Flyback” voltage so, for our circuit, its voltage rating should be around 20-25V for that purpose, we have chosen the “TVA207.7”  $200\mu F$  which has 25 Volt rating.

Diode:

Diode ratings are not that important for the current values because if we assume that there is zero average current passing through the capacitor average current passing through diode will be 10 mA but when it is off it can withstand  $V_{in} - V_{cap}(V_{flyback})$  = around 1.5 volt to 25.5 Volt to work properly, So, we choose, “1N4007” diode which has “1000 Vrrm” and “1 amp” average current rating.

### 7.1.3 Filter Components

Capacitor: Since rectifier is operating on DCM, and higher peak currents flow through the components, ESR of the capacitor becomes important.  $C_{cap} \gg I_{out}D_{max}f_{sw}V_{ripple}$ .

$N_{cp}$  is a value between 10-20, and allowable maximum ripple for that case is 0.6 V. Taking it as 10,

$$C_{min} = 9.3\mu F$$

Calculating maximum ESR:

$$ESR_{max} = V_{ripple}I_{sec(peak)} = 0.0268\Omega$$

$V_{rated(cap)} = V_{out} = 15V$  At the end, 50 V 330  $\mu F$  23m $\Omega$  aluminium electrolytic capacitor is chosen.

#### 7.1.4 Integrated Circuits

## PWM Controller:

In order to make regulation for the output voltage, we need a some kind of feedback to some reference value, For that purpose, instead of using opamps to realize error amplifier, we have used “LT1246” PWM modulator. It has a wide range of oscillator frequency including the one that we have choose for the implementation which is 40kHz.

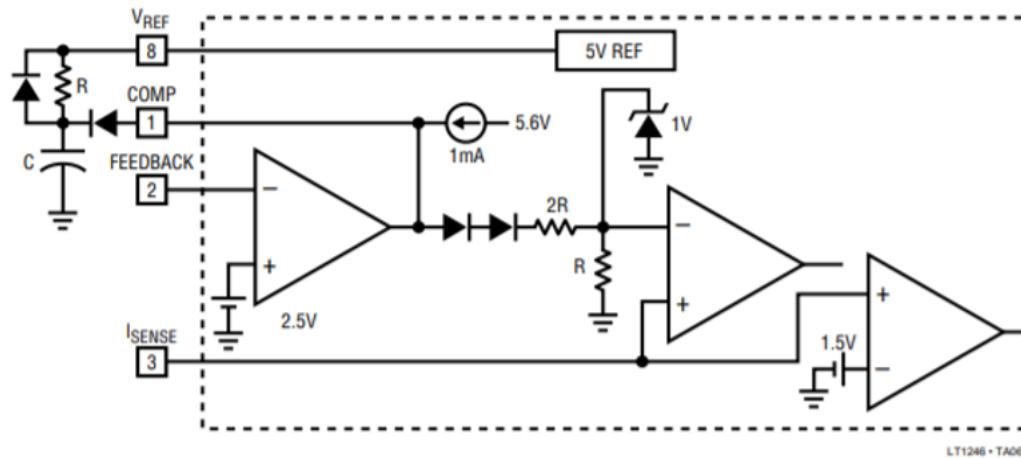


Figure 55: Error amplifier of the Lt1246.

It has its own internal error amplifier, which has a reference voltage of 2.5 Volt, therefore, in order to regulate 15 volt output voltage, we need to divide that value to be equal to 2.5 volt by creating voltage divider network. Also it has a "RT/CT" pin that can be connected to an "RC" circuit to adjusting its ramp waveform frequency.

### 7.1.5 Compensator Network

First of all, all of the component that are connected to this network is end up at the pins which are “FB” and “COMP” both of are input to the some operational amplifiers inside the controller therefore the current passing through these components is not among the selection considerations. However, during the start-up, the voltage on the output can reach the 45 volt therefore, their rating may be at least that value to guarantee the safe operation because we don’t have any isolation on the feedback side.

#### Voltage divider network:

This part is also included in compensation network it consists of two resistors which are 1k and 200 ohm. as we mention above, their current rating are not important. So, we choose “CF14JT200R” as 200 ohm and “PR02000201001JR500” as 1kohm.

#### Compensation network:

The components that are related to that part is derived in the “compensator” section. So in here we are just sharing the products as round values of previously calculated numbers. However, since there is no power handling and regulating high voltages (i.e output capacitor of circuit) all the capacitors are chosen as “Ceramic” capacitors.

470nF capacitor :C0402C474K9PACTU

10nF capacitor :GRM155R71C103KA01J

100nF capacitor :C0402C102K5RACTU

270  $\Omega$  resistor :CF14JT270R

30  $\Omega$ resistor : CFR-25JB-52-30R

#### 7.1.6 Oscillator

In the Oscillator part , choosing the component values as close as the founded values in the paper is really important because it determines our switching frequency. we have made this calculation using the given equations in the controller datasheet as below:

$$\text{Oscillator rise time: } t_r = 0.583RC$$

$$\text{Oscillator discharge time: } t_d = \frac{3.46RC}{0.0164R - 11.73}$$

$$\text{Oscillator period: } t_{osc} = t_r + t_d$$

So, in our case  $T_{osc} = 25\mu\text{sec}$  therefore equating this number to above formulas gives that :

$$R = 1k\Omega$$

$$C = 18.8nF (\text{choose it as } 18nF)$$

So the chosen components are as below:

$$R = (\text{PR02000201001JR500})$$

$$C = (\text{C0603C183K5RACTU})$$

## 8 Conclusion

In that project, a Flyback converter with certain specifications is designed. Before starting to the design process, a very comprehensive research has been done. All necessary points of the design is considered, and the best solution is tried to develop between countless trade-offs. Actually, these points are not just conceptual ideas but also the design arguments that are supported by very detailed simulation results. In simulation step, we have used many different software such as TINA, SIMPLIS, KicadAlso etc. Also, an excel sheet is formed to understand the trade-offs of the system better. Eventually, the design is successfully completed under the software tools which are mainly Simulink and LtSpice. This report gives an information about the what we have did during the semester for that project. It includes very detailed design information from circuit configurations to component selections and not only under the simulation environment but also it includes explanation of the producible PCB design that is created by us. Moreover, in the design part, we explain how we achieve the requirements of that topology how we overcome the challenges of the design and how much effort we make during the design process and in the test result part, we have showed that we did the job with all of the specifications and verify that this system is working as we have designed.

## 9 References

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