Appendix A: CPU Design PC_RST RF_EN RUN CLK MULT EN RUN_ind Z_FLAG ina AUTO MAN_CLK CLK CLR_ind LDQ A.M. ind PC_MUX_SEL[1..0 PC_RST SR SE PLUS1_SEL A_SEL[1..0 B_SEL[1..0 PC_EN MUL_SEL INST TYPE MUX SEL D_SEL[1_0 OAPI2_0 DATA_MEM_SEL WB_SEL UL_SE WR_EN INST REG EN counterchk[3.0] OUTBUT INSTR_MEM_ADDRESS[9.0] DUTPUT _____ Q_REG[7..0] PUTPUT RF_B_READ_PORT[7.0]

DATA_MEM_DATA_IN[15.0]

DATA_MEM_DATA_OUT[15.0]

DATA_MEM_DATA_OUT[15.0]