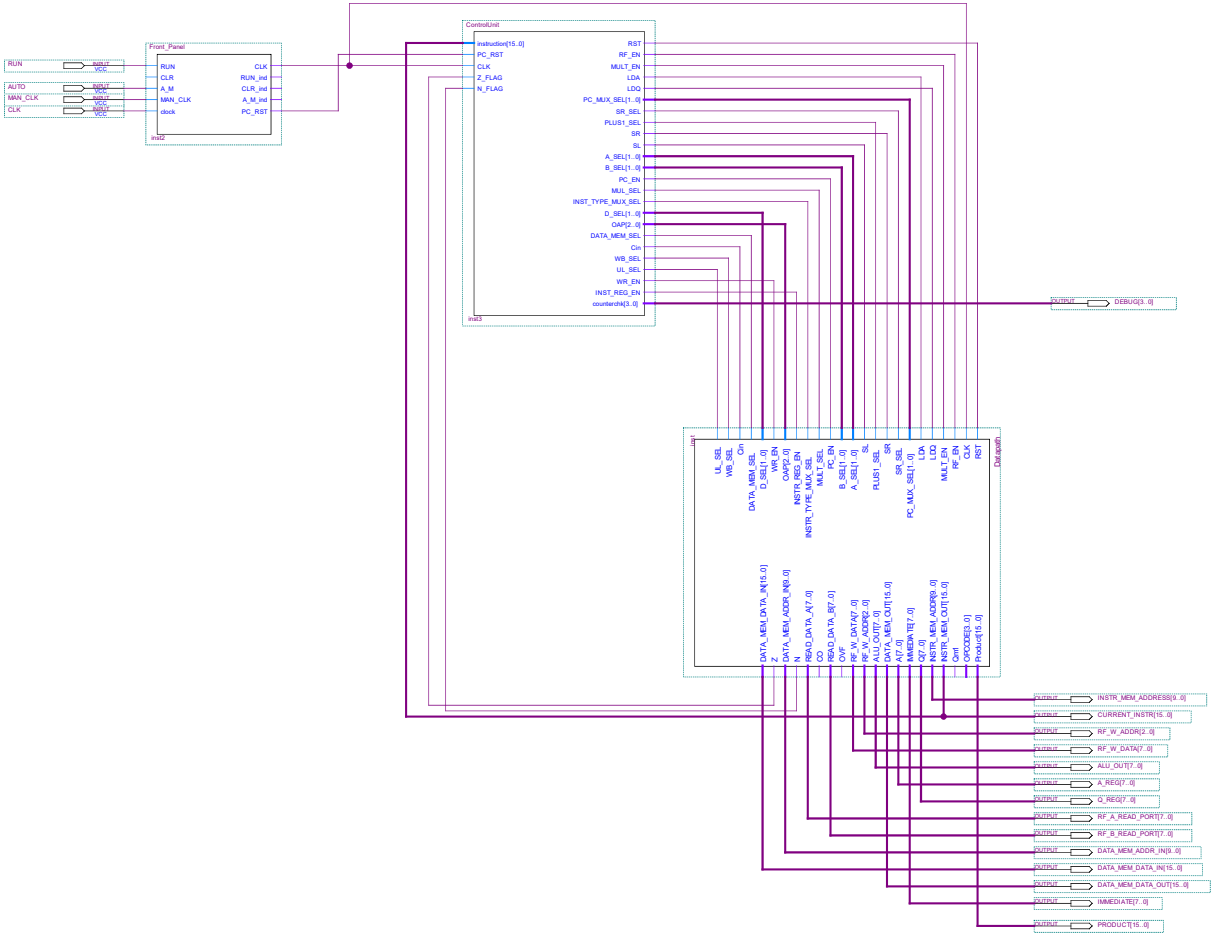
RUN
AUTO
MAN_CLK
CLK
INPUT
VCC
Front_Panel
RUN
CLR
A_M
MAN_CLK
clock
CLK
RUN_ind
CLR_ind
A_M_ind
PC_RST
inst2
ControlUnit
instruction[15..0]
PC_RST
CLK
Z_FLAG
N_FLAG
RST
RF_EN
MULT_EN
LDA
LDQ
PC_MUX_SEL[1..0]
SR_SEL
PLUS1_SEL
SR
SL
A_SEL[1..0]
B_SEL[1..0]
PC_EN
MUL_SEL
INST_TYPE_MUX_SEL
D_SEL[1..0]
OAP[2..0]
DATA_MEM_SEL
Cin
WB_SEL
UL_SEL
WR_EN
INST_REG_EN
counterclk[3..0]
inst3
OUTPUT
DEBUG[3..0]
inst
UL_SEL
WB_SEL
Cin
DATA_MEM_SEL
D_SEL[1..0]
WR_EN
OAP[2..0]
INSTR_REG_EN
INSTR_TYPE_MUX_SEL
MUL_SEL
PC_EN
B_SEL[1..0]
A_SEL[1..0]
SL
PLUS1_SEL
SR
SR_SEL
PC_MUX_SEL[1..0]
LDA
LDQ
MULT_EN
INST_REG_EN
RF_EN
CLK
RST
Datapath
DATA_MEM_DATA_IN[15..0]
Z
DATA_MEM_ADDR_IN[9..0]
N
READ_DATA_A[7..0]
CO
READ_DATA_B[7..0]
OVF
RF_W_DATA[7..0]
RF_W_ADDR[2..0]
ALU_OUT[7..0]
DATA_MEM_OUT[15..0]
A[7..0]
IMMEDIATE[7..0]
Q[7..0]
INSTR_MEM_ADDR[9..0]
INSTR_MEM_OUT[15..0]
Qm1
OPCODE[5..0]
Product[15..0]
OUTPUT
INSTR_MEM_ADDRESS[9..0]
CURRENT_INSTR[15..0]
RF_W_ADDR[2..0]
RF_W_DATA[7..0]
ALU_OUT[7..0]
A_REG[7..0]
Q_REG[7..0]
RF_A_READ_PORT[7..0]
RF_B_READ_PORT[7..0]
DATA_MEM_ADDR_IN[9..0]
DATA_MEM_DATA_IN[15..0]
DATA_MEM_DATA_OUT[15..0]
IMMEDIATE[7..0]
PRODUCT[15..0]