

**MIDDLE EAST TECHNICAL UNIVERSITY NORTHERN CYPRUS CAMPUS**

**ELECTRICAL AND ELECTRONICS ENGINEERING PROGRAM**

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**EEE 446 Computer Architecture**

**Lab Module 2**

**8-bit INTEGER ARITHMETIC PROCESSOR DATAPATH DESIGN**

Contents

[Objective 2](#_Toc36042286)

[AP datapath Simulations 3](#_Toc36042287)

[Multiplication Simulation 11](#_Toc36042288)

[State Diagram 13](#_Toc36042289)

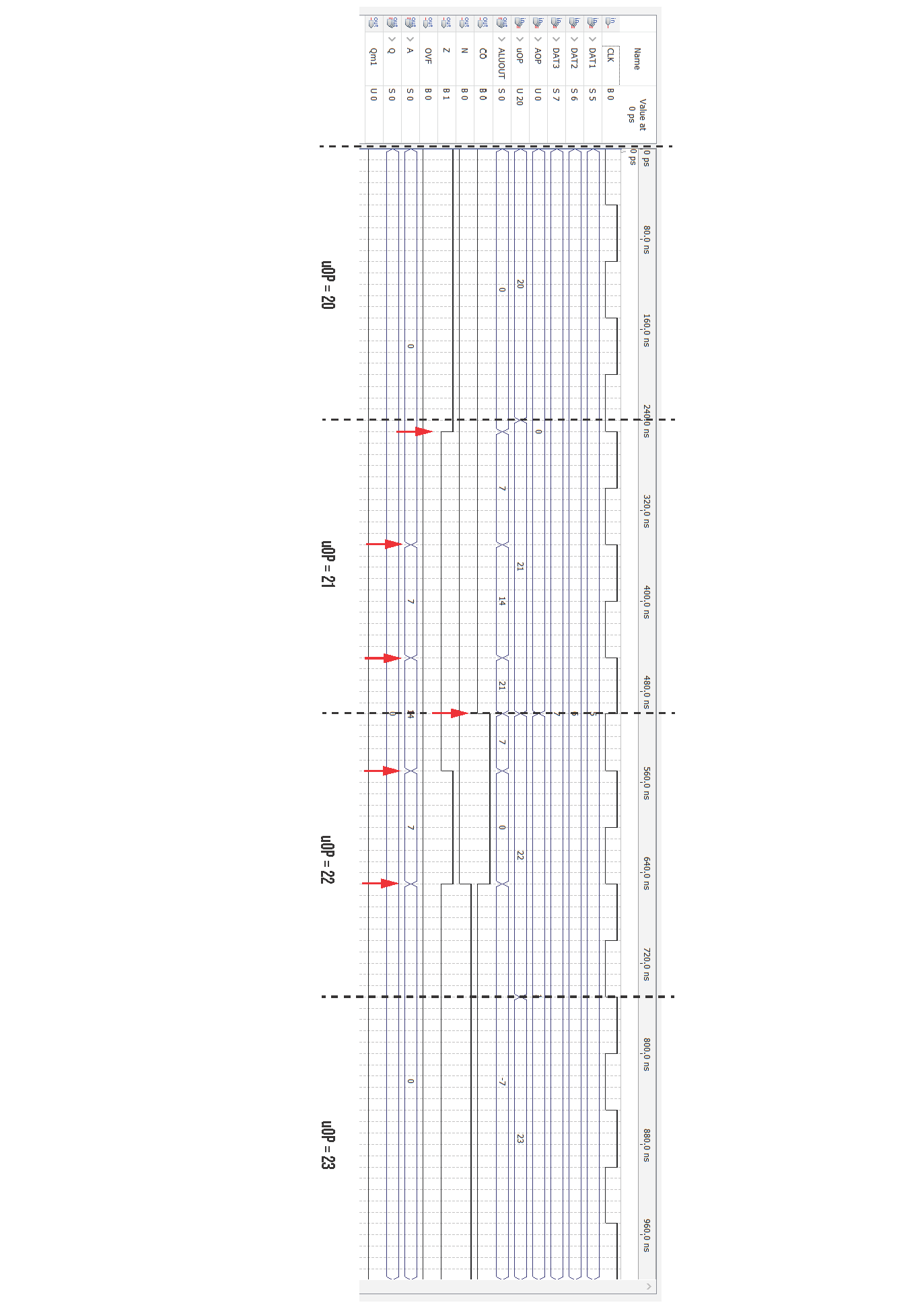
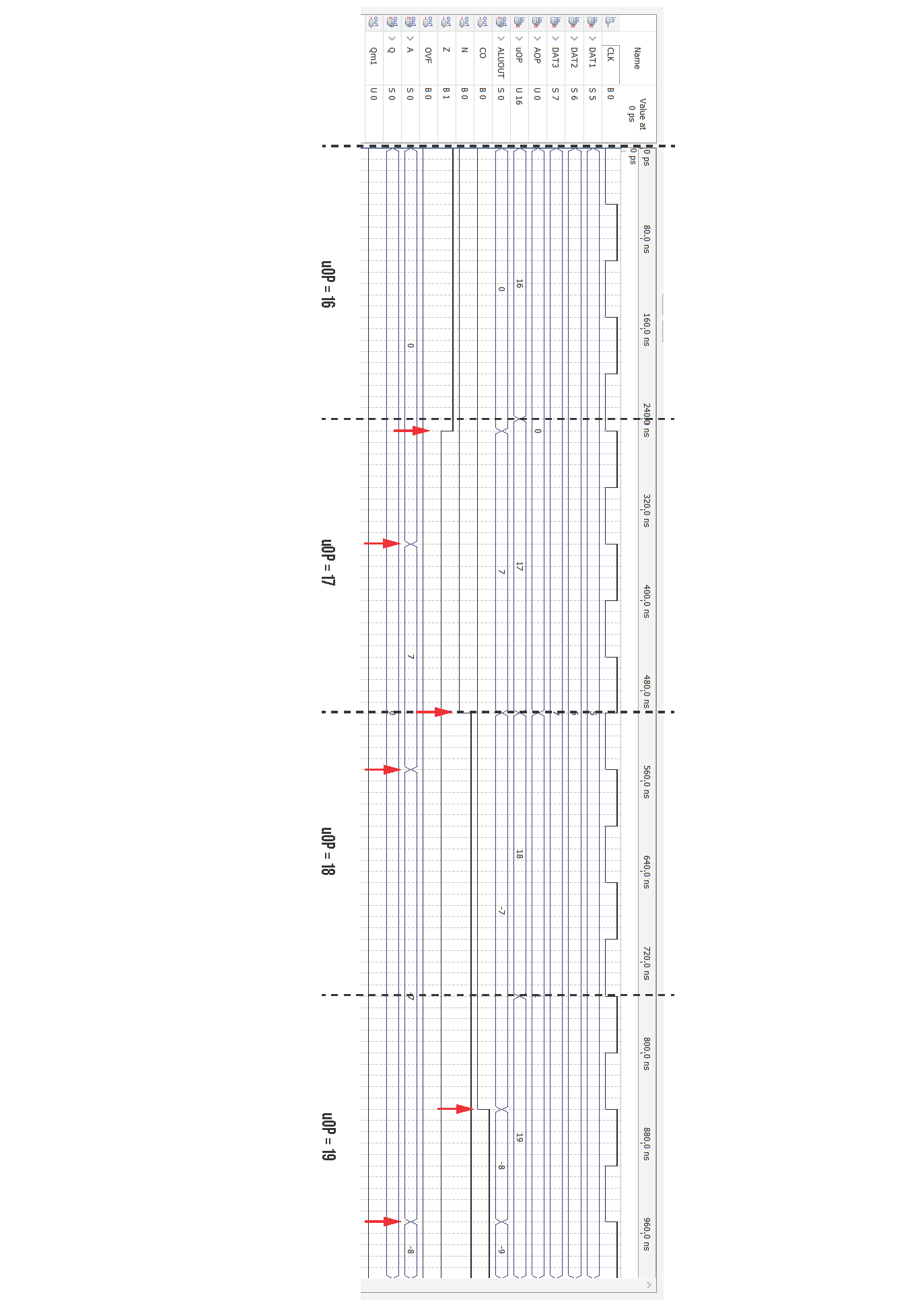
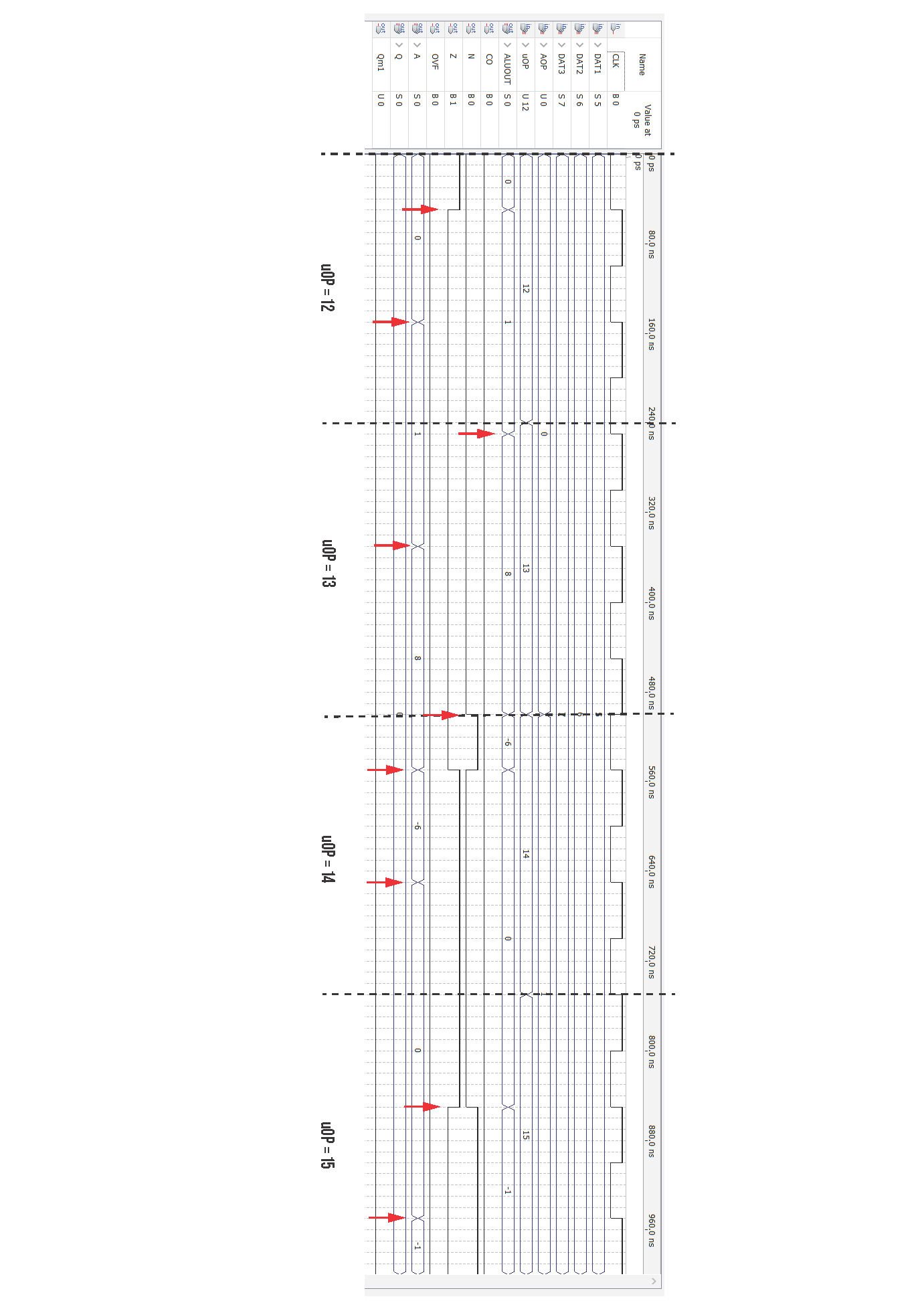
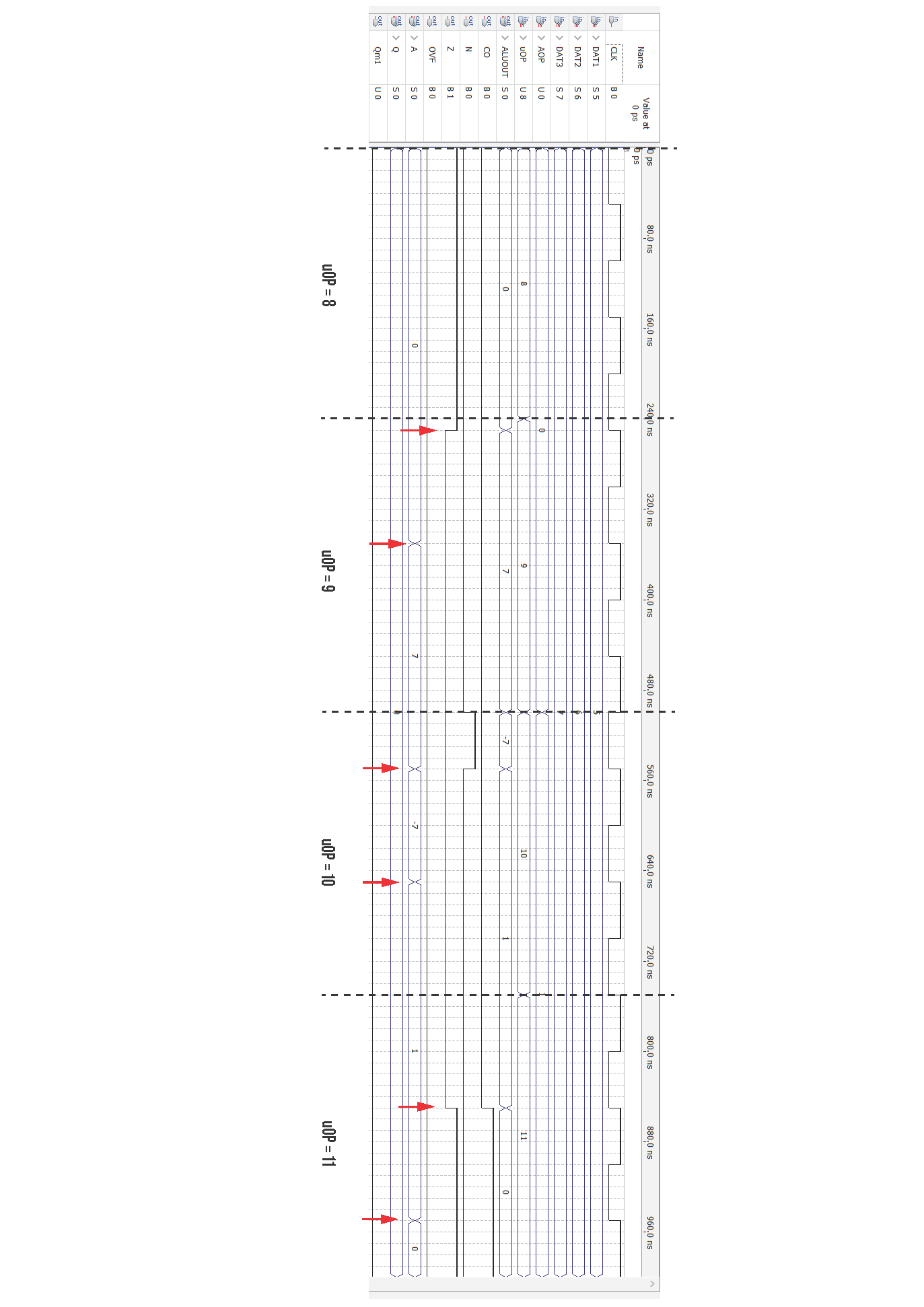
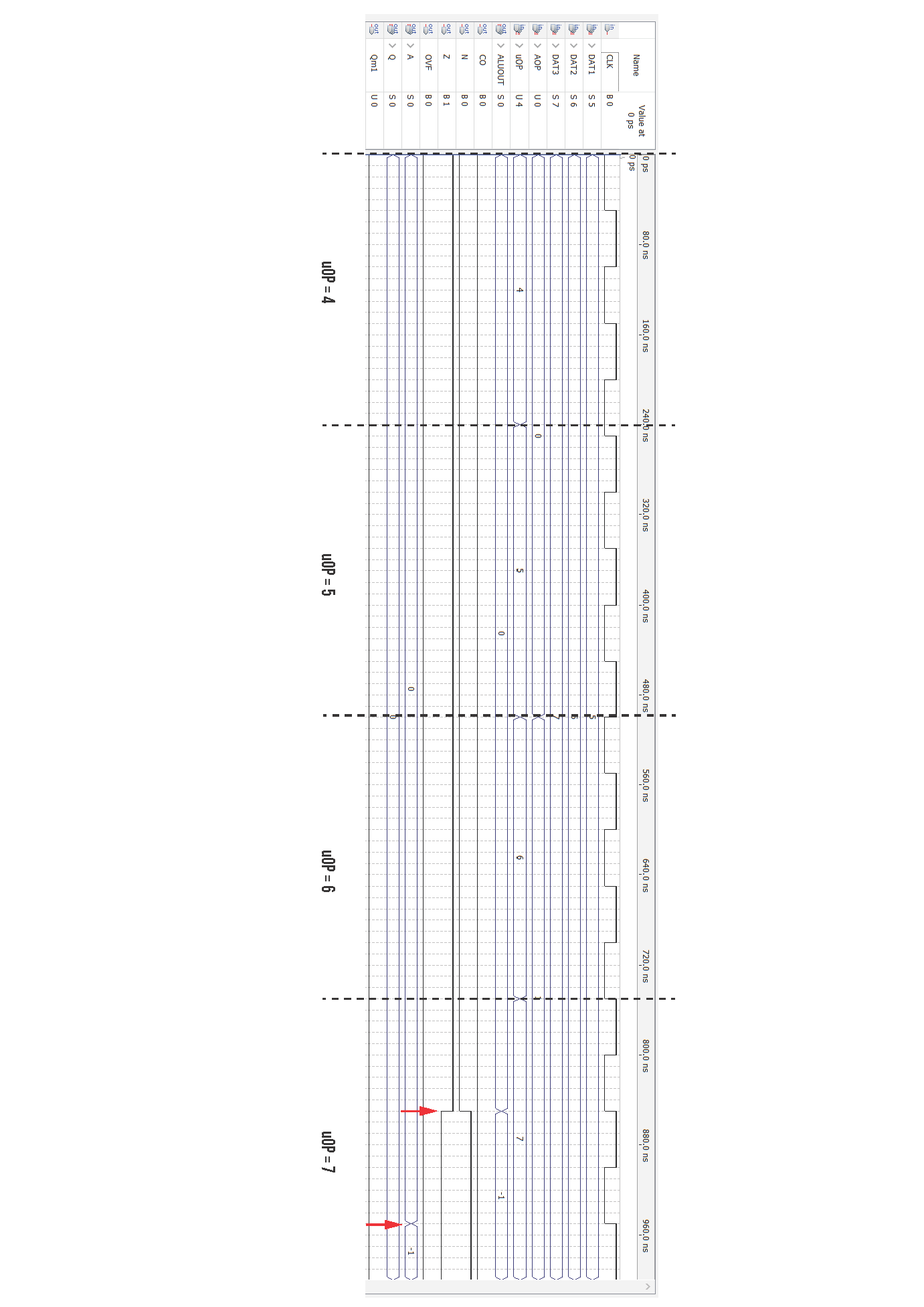
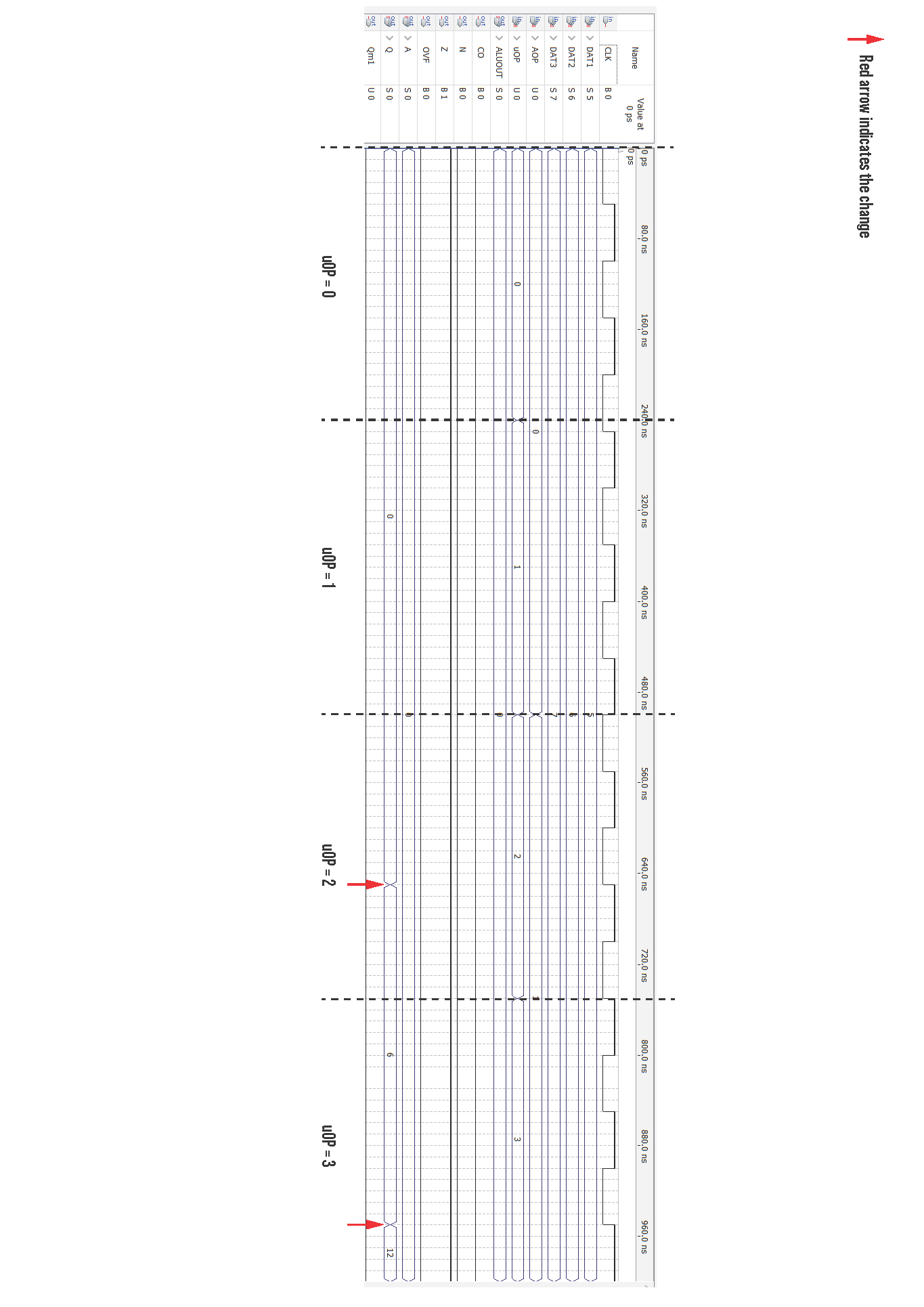
[Timing Analyzer Summary 15](#_Toc36042290)

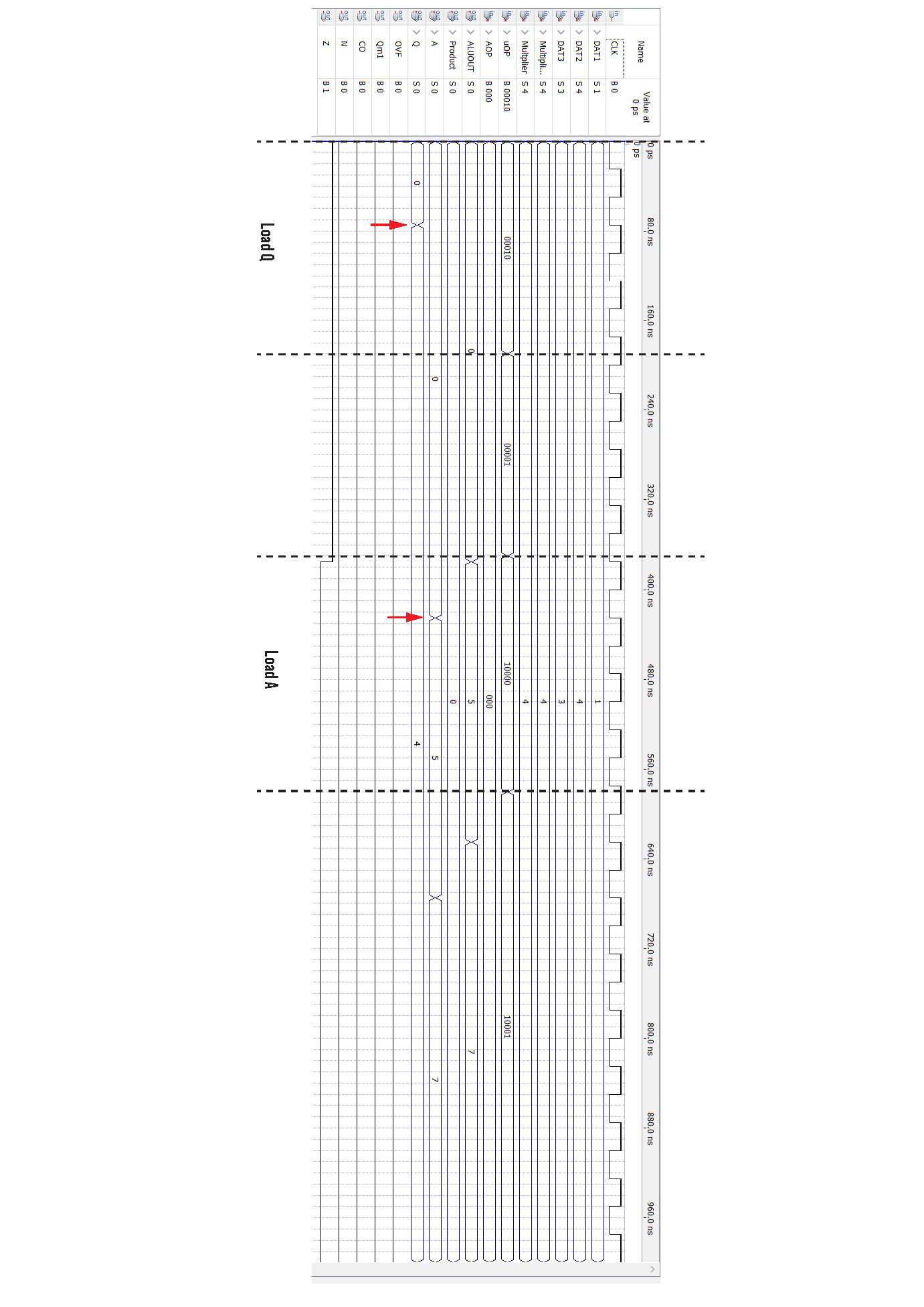
[Schematic Design Files 15](#_Toc36042291)

# Objective

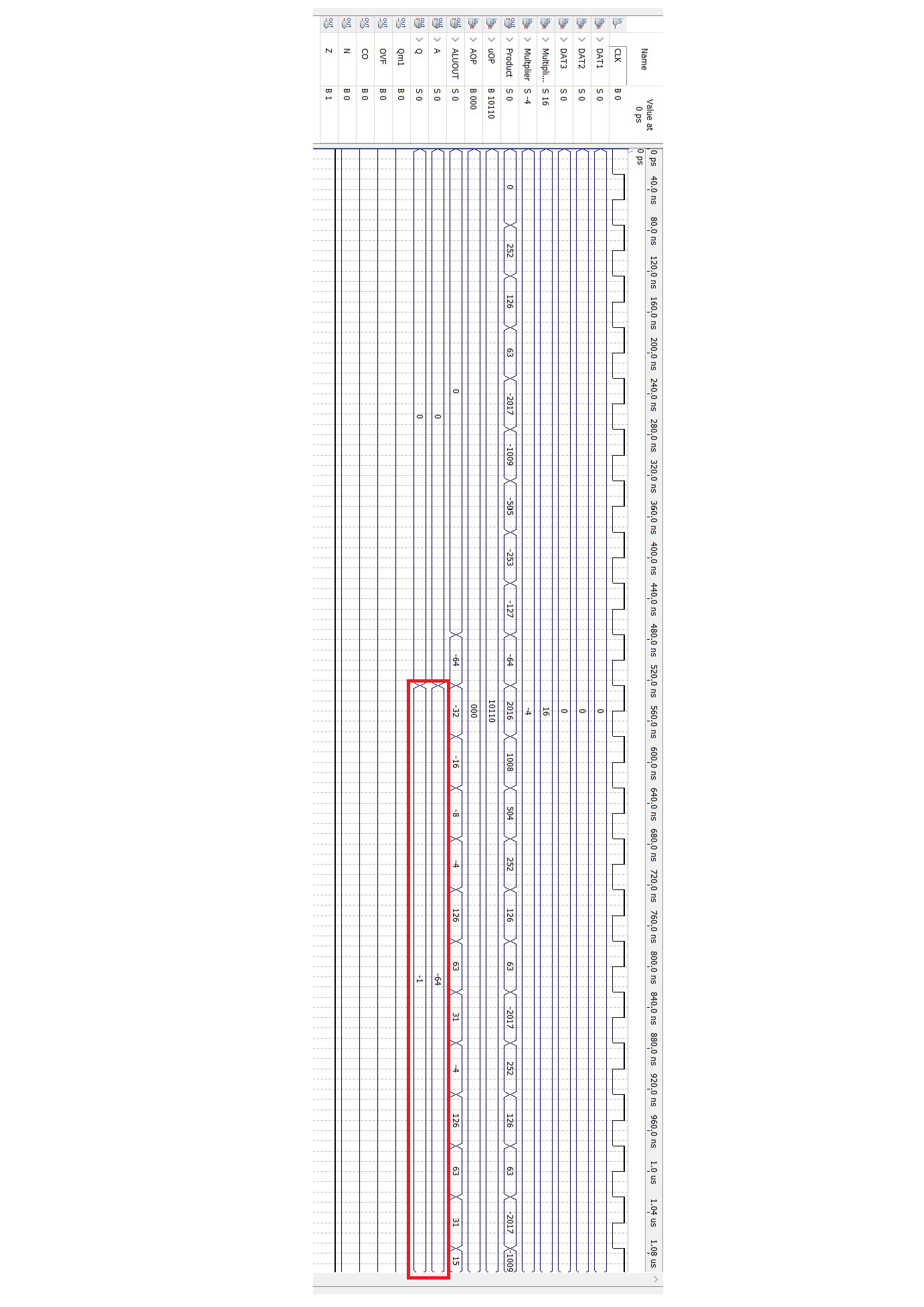
In this lab module, we were responsible for designing an 8-bit arithmetic processor (AP) and a control unit to implement the microinstructions associated with this arithmetic processor. The 8-bit arithmetic processor can do all the required operations specified by the lab manual. The control unit executes the micro-operations according to the uOP code assigned to each instruction. This will then be used later to build our multicycle machine after the ISA is designed to carry out the operations in the benchmark specifications. The booth’s multiplier that was developed in the first lab module has been integrated into this AP datapath by doing some minor modifications to the AP datapath. All the operations and functionality of the datapath has been shown and verified in the report below.

# AP datapath Simulations

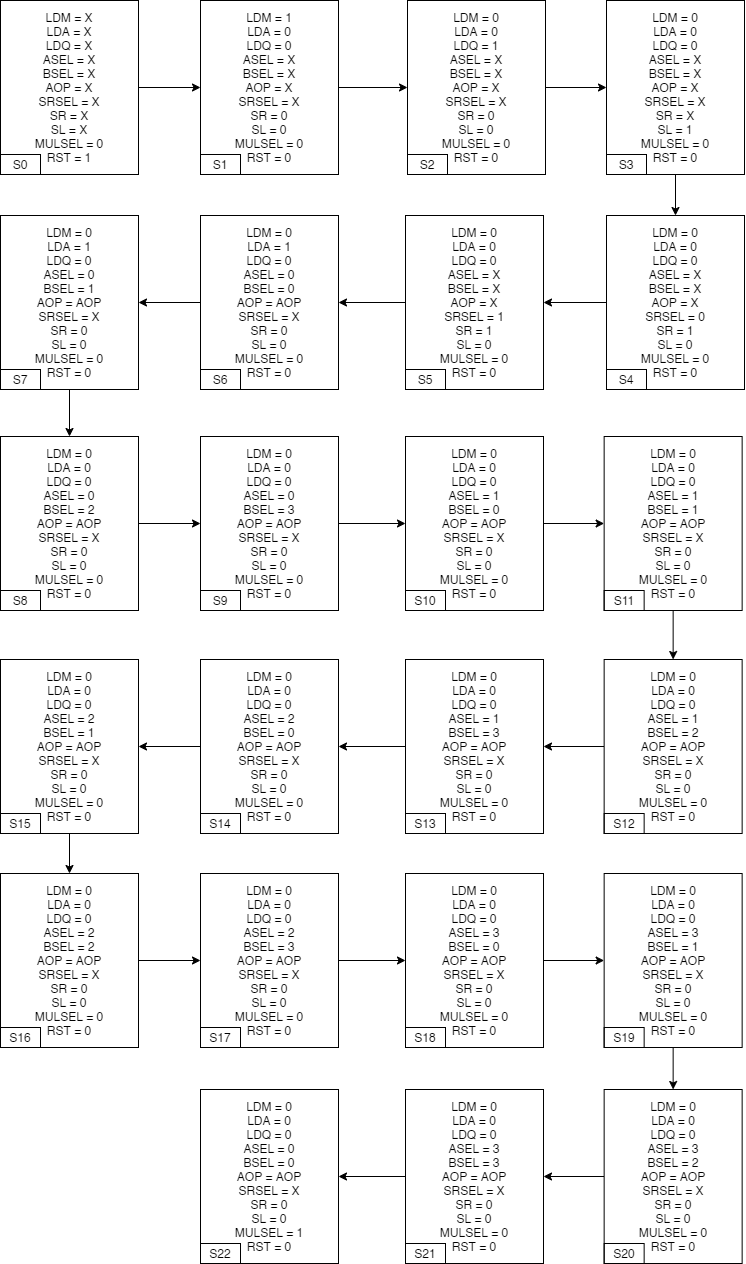




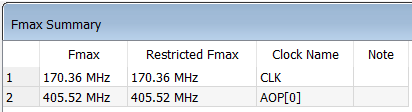
# Multiplication Simulation



# State Diagram

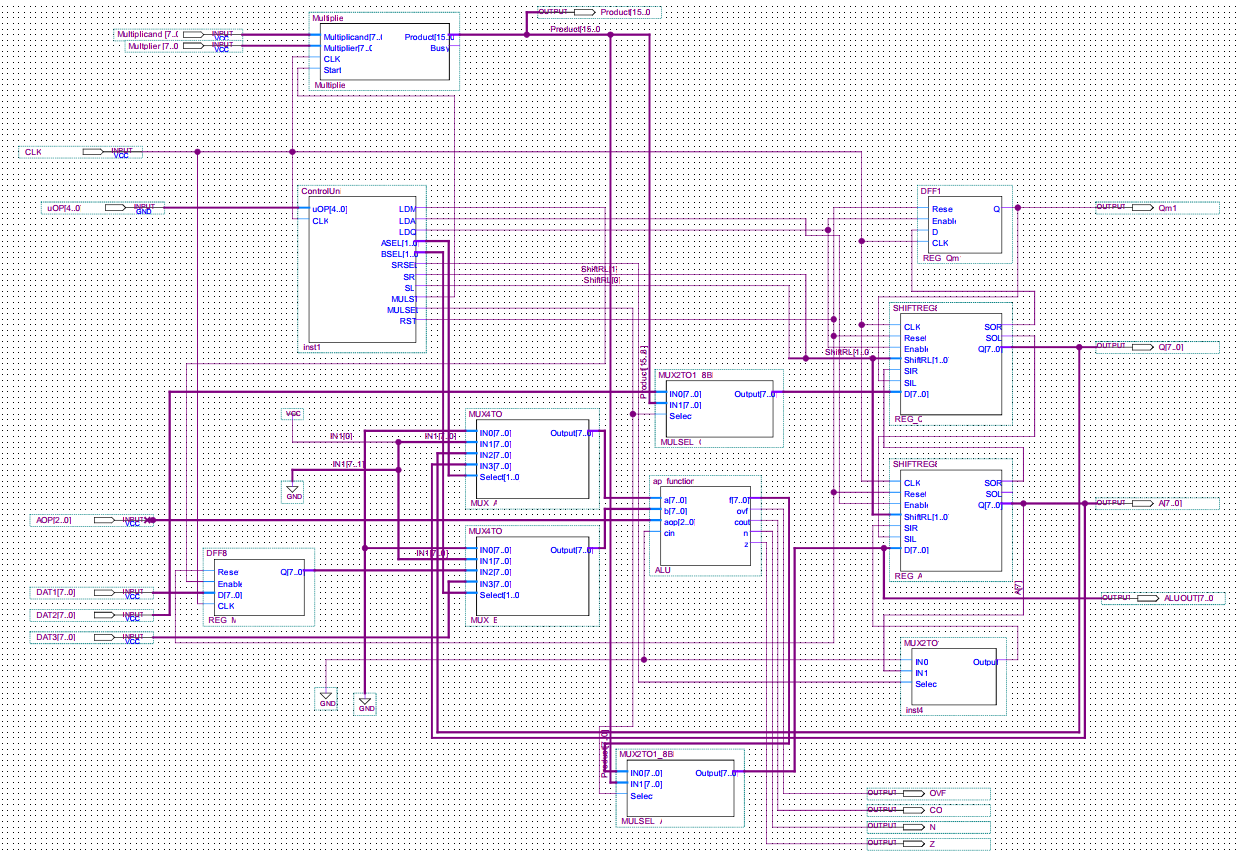


# Timing Analyzer Summary

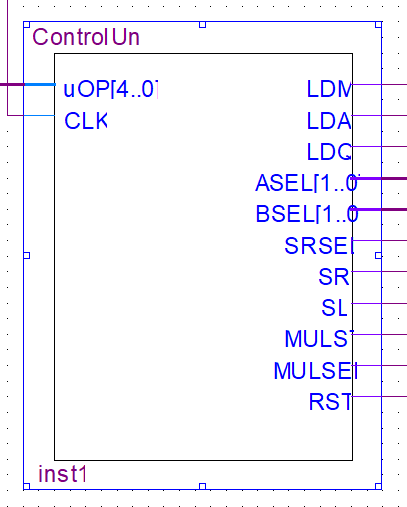


# Schematic Design Files

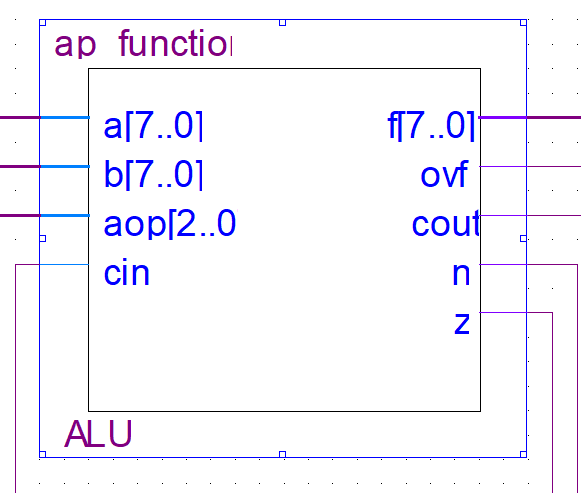
* Datapath



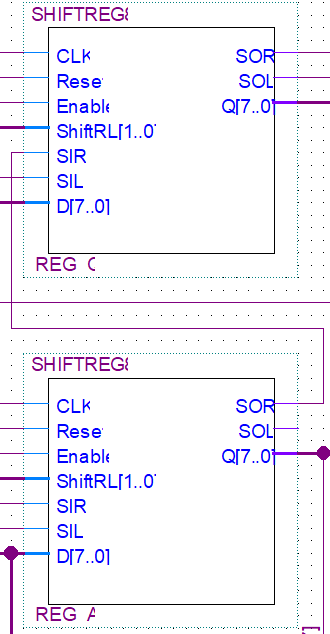
* Control unit



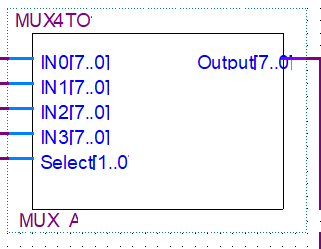
* Arithmetic Processor



* Register A and Q



* 4 to 1 MUX



* Booth Multiplier

