Project 1: UART TX

UART Basics

A Universal Asynchronous Receiver-Transmitter (UART) is a peripheral device for asynchronous serial communication in which the data format and transmission speeds are configurable. It sends data bits one by one, from the least significant to the most significant, framed by start and stop bits so that precise timing is handled by the communication channel.

The universal asynchronous receiver-transmitter (UART) takes bytes of data and transmits the individual bits in a sequential fashion. At the destination, a second UART re-assembles the bits into complete bytes. Each UART contains a shift register, which is the fundamental method of conversion between serial and parallel forms. Serial transmission of digital information (bits) through a single wire or other medium is less costly than parallel transmission through multiple wires.

For UART to work, the following settings need to be the same on both the transmitting and receiving side:

- Baud Rate.
- Parity bit.
- Data bits size.
- Stop bits size.

A UART frame consists of 5 elements:

1. Idle (logic high (1))
2. Start bit (logic low (0))
3. Data bits
4. Parity bit
5. Stop (logic high (1))

Idle: It refers to the state of the transmission line when no data is being sent. The idle state of a UART line is a logic high1. This means that if you were to look at the signal on an oscilloscope, you would see a constant high voltage level indicating that the line is ready but not currently transmitting data.

Start Bit: When data is ready to be sent, the line transitions from this idle state (logic high) to a start bit (logic low), signaling the beginning of a new data word.

Data Bits: These are the actual bits of information being transmitted from one UART to another. The number of data bits in a UART frame can vary from 5 to 9 bits, but a common and widely used configuration is 8 bits. The data bits are sent one by one, from the least significant to the most significant.

Parity Bit (Optional): The parity bit is a method for error detection. It is placed after all of the data bits. The parity bit is calculated based on the data bits and is used by the receiving UART to determine if any data has changed during transmission. There are several types of parity including even, and odd. For ‘Even’ parity, the sum of all of the '1’s in the data plus the Parity bit should be an Even number. For ‘Odd’ parity, the sum of all of the '1’s in the data plus the Parity bit should be an Odd number.

Stop Bit: The stop bit signals the end of a data packet. It follows the last data bit or the parity bit in the transmission. The stop bit is a logic high, which means it returns the line to the idle state. The use of stop bits allows the receiving UART to detect the end of the incoming data packet. UARTs often let you choose between 1, 1.5 and 2 stop bits. The choice of the number of stop bits depends on the system requirements.

No clock information is conveyed through the serial line. Before the transmission starts, the transmitter and receiver must agree on a set of parameters in advance, which include the baud rate (i.e., number of bits per second), the number of data bits and stop bits, and use of the parity bit. The commonly used baud rates are 2400, 4800, 9600, and 19,200 bauds.

UART Transmitter

Function: Takes parallel data and converts it into a serial stream of bits ready for transmission over a single communication line.

Key Components:

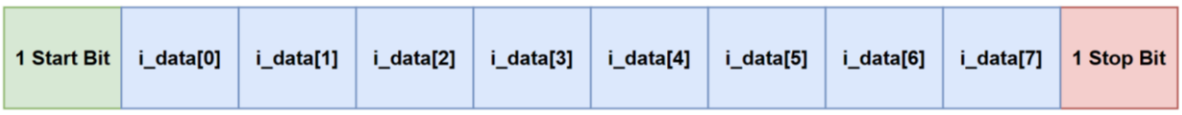
- Parallel Data Input: The port where the transmitter accepts the data to be transmitted.
- Shift Register: Temporarily stores the data and shifts the bits out one by one for serial transmission.
- Parity Generator (Optional): If parity is enabled, calculates, and adds the appropriate parity bit (even or odd) to the data frame.
- Start/Stop Bit Generator: Adds the start and stop bits, which are essential for framing and synchronizing the data.

Process:

1. The transmitter receives parallel data.
2. It loads this data into the shift register.
3. (If enabled) The parity generator computes and adds the parity bit.
4. The transmitter adds a start bit to signal the beginning of a data frame.
5. The shift register shifts the data bits out one by one onto the transmission line.
6. The transmitter appends a parity bit, then a stop bit to indicate the end of the data frame.

Our design is customized for a UART with a 9600 baud rate, 8 data bits, 1 stop bit, and no parity bit.

Signal	Direction	Width	Description
i_clk	Input	1	Positive-edge-triggered system clock (50 MHz).
i_rst_n	Input	1	Negative-edge-triggered synchronous system reset. The system enters the reset state when i_rst_n is low (0).
i_data	Input	8	The parallel data to be transmitted.
i_en	Input	1	A flag indicating that the input data is valid.
o_data	Output	1	Serial data output.
o_done	Output	1	A flat that goes high after transmission is done.
o_busy	Output	1	A flag indicating that the UART TX is busy.



Submission:

- RTL Design of the UART TX.
- FSM Block Diagram.
- UART TX Testbench.

Deadline:
Thursday, 2024/03/14, at 10 P.M.

Submit to:
shirefy49@gmail.com