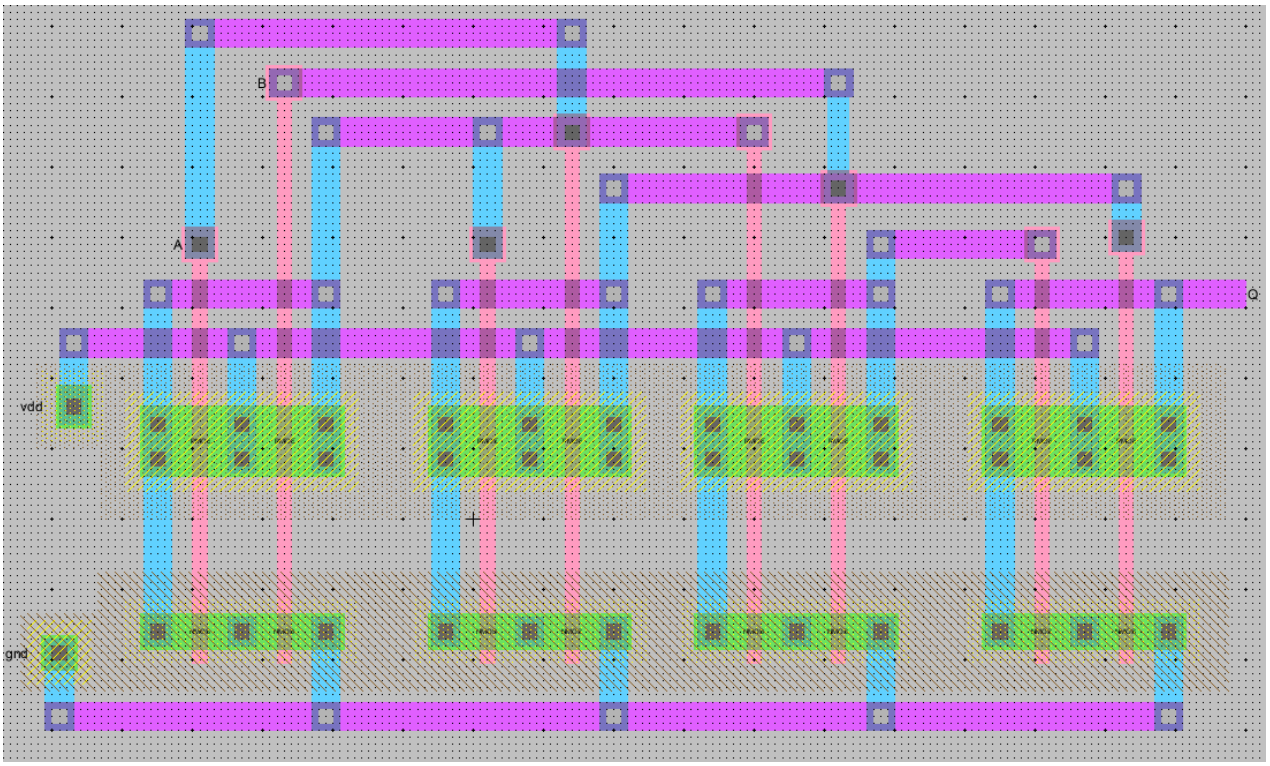
Table of Contents

1 Layout of XOR gate 2
2 Schematic 3
3 Simulation 4
4 Tests 5
4.1 DRC 5
4.2 ERC 5
4.3 NCC (LVS) (Bonus) 5
5 Export GDSII file 6
6 Faced problems 7

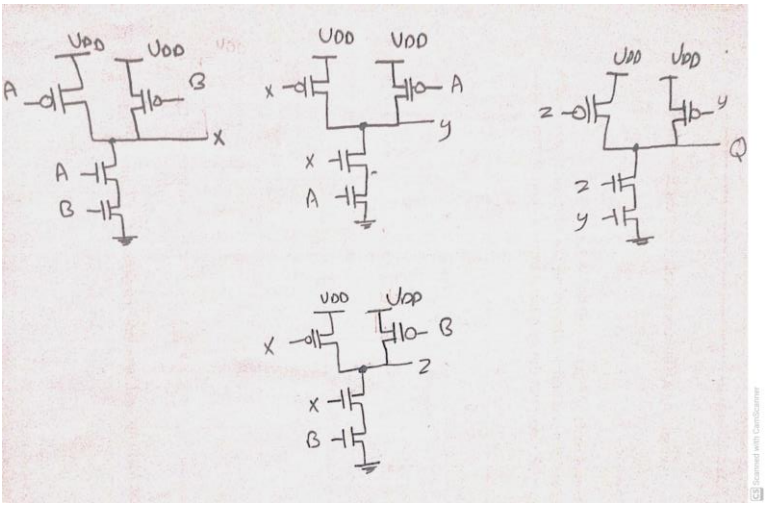
1 Layout of XOR gate



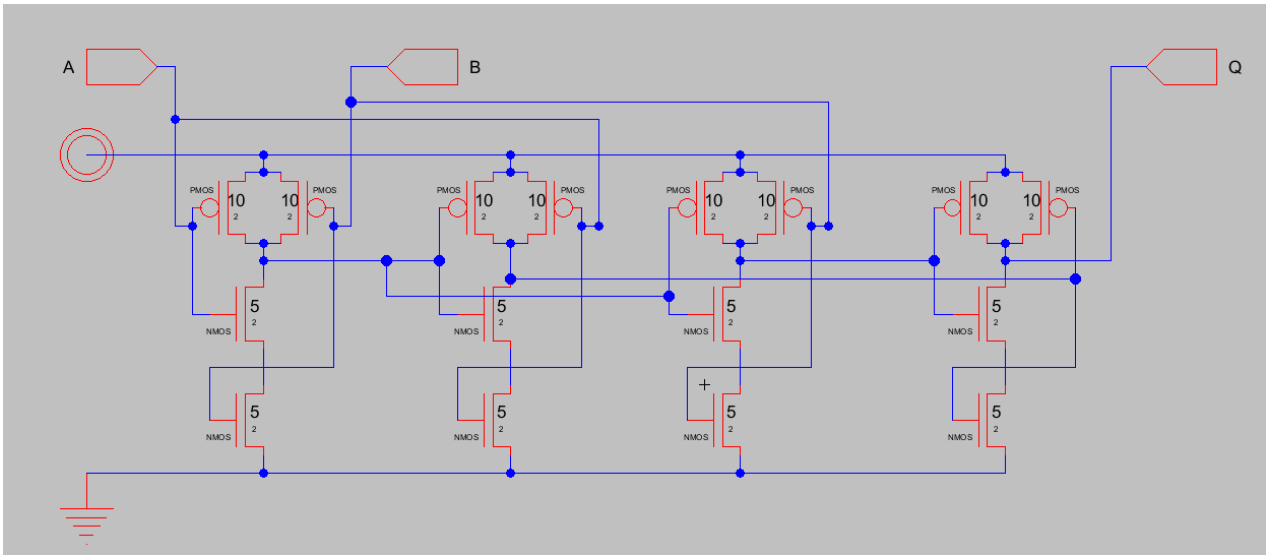
First, I used electric software to draw layout of the design and I added spice parameter to each PMOS and NMOS. I used two metal layers first in in blue and second is purple. Polysilicon is in the red color. nwell and pwell as shown in the layout figure with lines and dots background.

- Inputs: A, B
- Power supply: vdd
- Ground: gnd
- Output: Q

2 Schematic



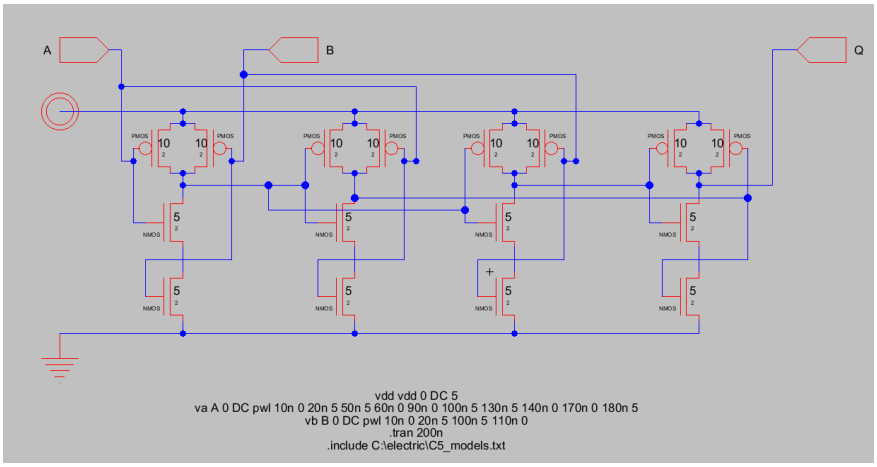
Seconed, I drew the schematic on paper before implementing it on electric software



Third, I drew the schematic of the XOR gate from the layout sizing the PMOS with $\frac{W}{L} = 2 * \frac{W}{L}$ NMOS. Then set the spice parameter of the transistors for either PMOS or NMOS.

- Inputs: A, B
- Power supply: vdd
- Ground: gnd
- Output: Q

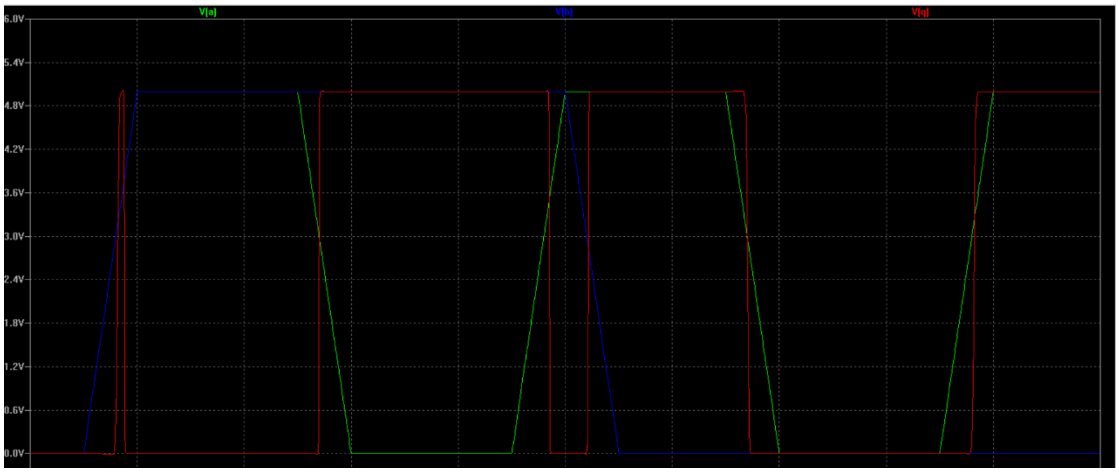
3 Simulation



Fourth, I wrote a spice code to be able to simulate the design implemented in the schematic to make sure that the schematic design of 2-INPUT XOR is correct and gate correctly function so when I do LVS test and no errors occur I am going to be sure that layout also function correctly. I used LTspice simulator.

Code explains by lines:

1. Apply DC pulse of amplitude 0v ⟹ 5v
2. Apply DC pulse as input for both A,B that change according to the written time
3. Transit analysis of the transistor to draw versus time
4. Included model file (like PDK file)



Output of the simulation

- Va , Vb input
- Vq output

4 Tests

The results of the simulation that assure the correct functionality of designs

4.1 DRC

```
================================14================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 29 networks
Checking cell 'XOR_schem{lay}'
        No errors/warnings found
0 errors and 0 warnings found (took 0.032 secs)
```

First DRC to check the correct design of the layout

```
================================1================================
Library /D:/Layout/ICT2/XOR.jelib read, took 0.018 secs
Checking library 'XOR' for repair... library checked
No errors found
================================2================================
Checking schematic cell 'XOR_schem{sch}'
   No errors found
0 errors and 0 warnings found (took 0.017 secs)
```

Second DRC to check the correct design of the schematic

4.2 ERC

```
================================15================================
Checking Wells and Substrates in 'XOR:XOR_schem{lay}' ...
   Geometry collection found 74 well pieces, took 0.003 secs
   Geometry analysis used 12 threads and took 0.003 secs
NetValues propagation took 0.0 secs
Checking short circuits in 2 well contacts
   Additional analysis took 0.002 secs
No Well errors found (took 0.008 secs)
```

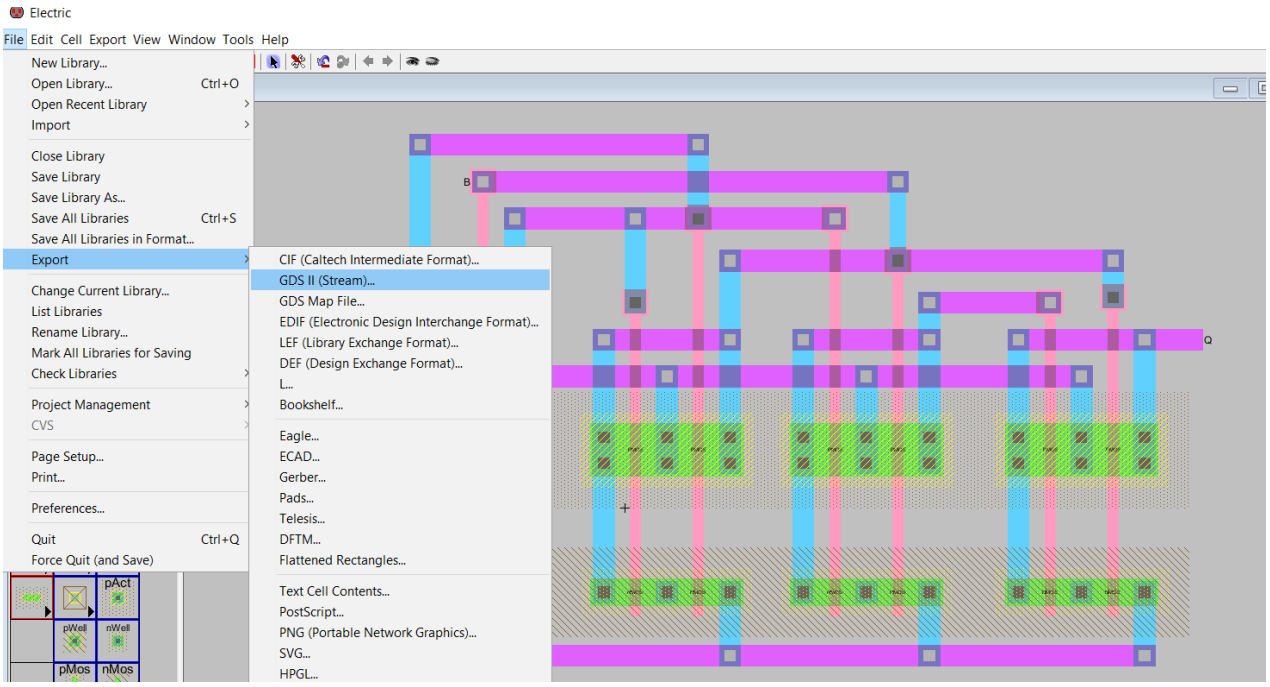
First ERC to check the correct design of the layout

4.3 NCC (LVS) (Bonus)

```
================================16================================
Hierarchical NCC every cell in the design: cell 'XOR_schem{sch}'  cell 'XOR_schem{lay}'
Comparing: XOR:XOR_schem{sch} with: XOR:XOR_schem{lay}
  exports match, topologies match, sizes not checked in 0.033 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.039 seconds.
```

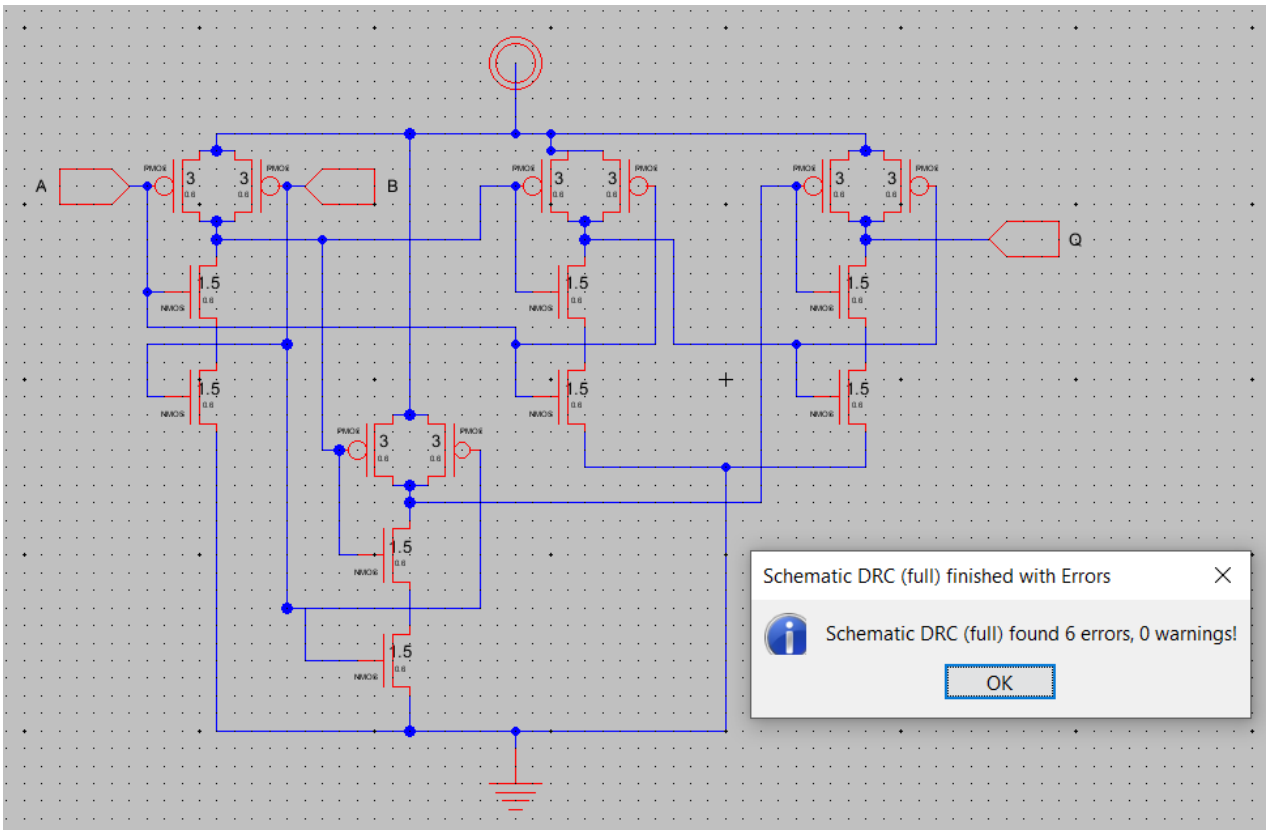
Last test was the layout versus schematic test **(LVS)**

5 Export GDSII file



Last step in layout design flow is to export GDSII file (graphic database system) and sent it to the foundry

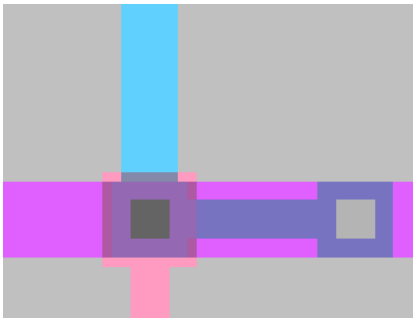
6 Faced problems

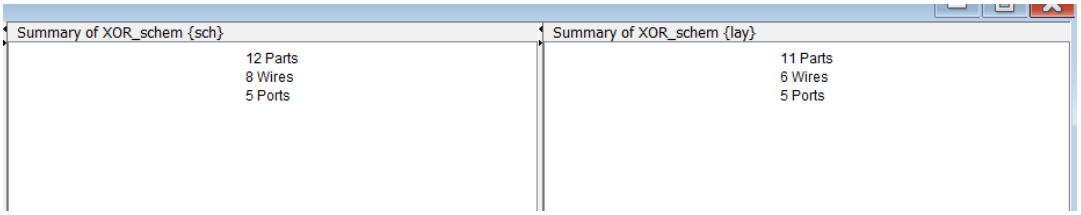



```
================================112================================
Schematic DRC (full) error 1 of 6: Unnecessary pin (between 2 arcs)
================================113================================
Schematic DRC (full) error 2 of 6: Unnecessary pin (between 2 arcs)
================================114================================
Schematic DRC (full) error 3 of 6: Nodes 'node Wire_Pin['pin@55']' 'node Off-Page['conn@2']' have touching ports that are not connected
================================115================================
Schematic DRC (full) error 4 of 6: Unnecessary pin (between 2 arcs)
================================116================================
Schematic DRC (full) error 5 of 6: Unnecessary pin (between 2 arcs)
================================117================================
Schematic DRC (full) error 6 of 6: Arc dangles
```

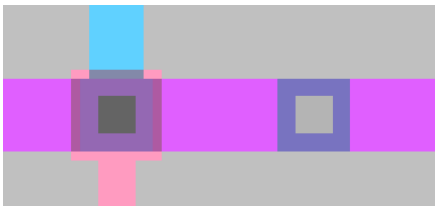
Here are some problems I faced in early schematic design like some unnecessary pins, arc dangles, improper connections.

Also, the wires were too much so I redesigned the schematic for more cleaner look.

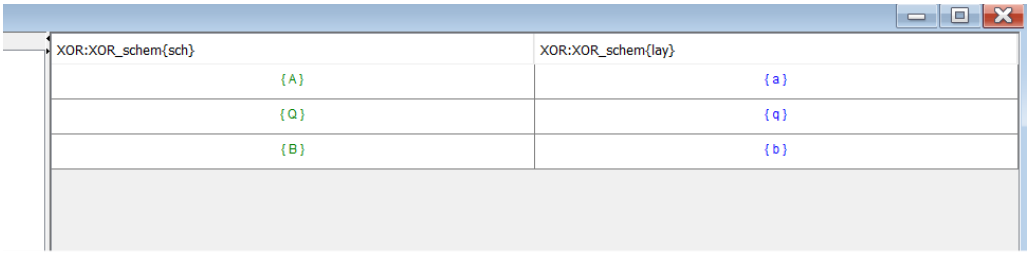




In the layout I connected metal1 to metal2 to polysilicon which was wrong when I started getting schematic I noticed it also from NCC test (LVS) number of wires and parts did not match.



So, I deleted the metal 1 and crossed over polysilicon by metal 2



Another error happened during LVS test was the ports wasn't matched in schematic and layout because they had different names one was all caps letters and other small