Table of Contents

1. Hand analysis gm , ro , Vov	3
2. Transistor analysis	4
3. Final Design	11
4. Gain and power	12
5. Comparison	
6. Frequency response	14
6.1 Hand analysis	14
6.2 Simulation results	19
7. Phase margin	
8. Corner analysis	21
9. Stability analysis	21
10. Mistakes made then resolved	24

1. Hand analysis gm, ro, Vov

First, we assumed maximum current used is ISS = 40~uA since the power budget is 4mw so the current in half of differential amplifier circuit Id = 20uA we used small value of current with the given budget to achieve low power consumption by the telescopic cascode amplifer.

Second, we assumed ranges of the input voltage and output voltage so we can get equations of over drive voltages of each transistor

$$Vout \, range = 0.65 - 0.75 = 0.7V$$

 $Vin \, range = 0.75 - 0.8 = 0.775V$

EQ1:

Vin > Vth1 + Vov1 + Vovss

Vin(min) = Vth1 + Vov1 + Vovss

EQ2:

VIN - Vn < Vth Vn = Vb1 - Vgs3 = Vb1 - Vth3 - Vov3 Vin - Vb1 + Vth3 + Vov3 < Vth1Vb1 > Vin(max) - Vth1 + Vth3 + Vov3

EQ3:

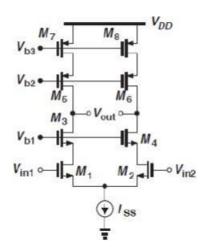
Vb1 - VOUTmin < Vth3Vb1 < Vth3 + VOUT(min)

EQ4:

Voutmax - Vb2 < -Vth5Vb2 > Vout(max) - Vth5

EQ5:

1.2 - Vb2 > Vth5 + Vov5 + Vov7Vb2 < 1.2 - Vth5 - Vov5 - Vov7 (all values is positive)



Third, we assumed transconductances are equal to each other and output resistances are ratios from each other and calculated these values from gain equation of circuit.

$$G_m = -gm_1$$
 $R_{out} = (ro1 * gm3 * ro3 // ro5 * gm5 * ro7)$
 $abs(Gain) = G_m * R_{out} = gm1 * (ro1 * gm3 * ro3 // ro5 * gm5 * ro7) = 600$

$$\frac{gm1}{Id} = 15 \qquad assumption$$

$$Vov1 = 133 \, mV$$

$$gm1 = 300uS$$

$$gm3 = gm5 = gm1 = gm7$$

$$ro1 = ro7 = ro3 / 2 = ro5 / 2$$

$$Gain = gm1^2 * (\frac{ro3^2}{4}) = 600$$

$$ro5 = ro3 = 163K$$

$$ro1 = ro7 = 81.5K$$

2. Transistor analysis

After we assumed values of transconductance, and we got the value of output resistance we ratio between transconductance and current gm/id and we also got the ratio between transconductance and output conductance gm/gds.

To get the length of the channel we used gm/id methodology by dc sweep on the gate voltage and parametric sweep over several values of channel length, using standard width, to achieve the required values for the ratios $\frac{gm}{ads}$ & $\frac{gm}{id}$, as width don't affect these ratios.

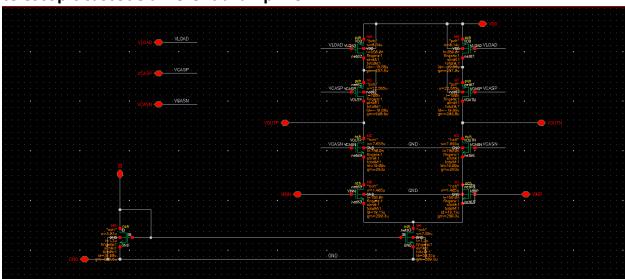
$$gm * ro = \frac{2 * b}{V_{vo}} * \frac{1}{\lambda * b} = \frac{2}{V_{ov} * \lambda}$$

$$\frac{gm}{I_D} = \frac{2 * I_D}{V_{vo}} * \frac{1}{I_D} = \frac{2}{V_{ov}}$$

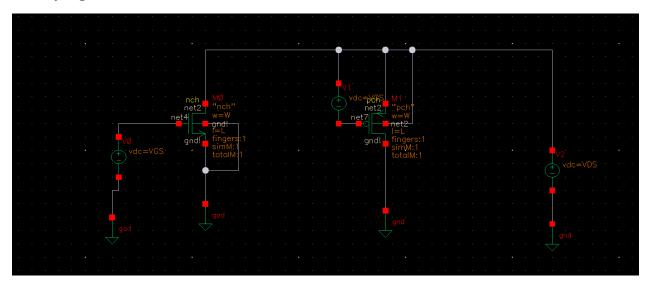
To get value of transistor width we said that width is direct proportional to the current (initial values of current and width are 20uA, 10um) and from graph we got the value of the current.

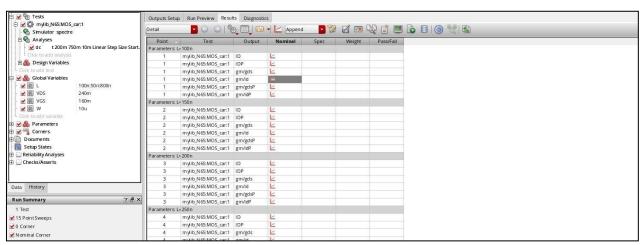
$$I_D \alpha w$$
 $w_{stan} = 10 um$

telescopic cascode differential amplifier:



Sweeping circuit:





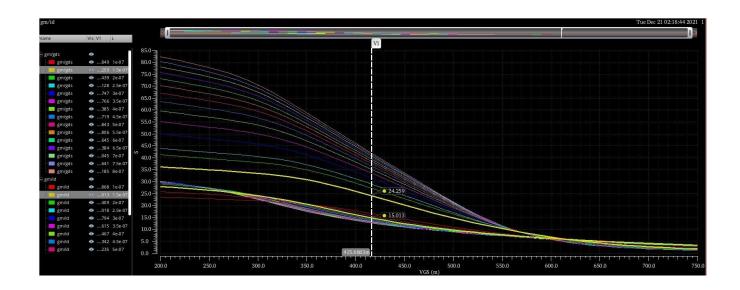
$$\frac{gm}{id} = 15$$

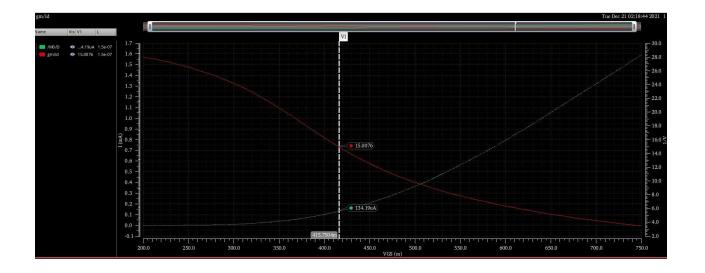
$$\frac{gm}{gds} = 24.45$$

$$l = 150 nm$$

$$w = \frac{20}{134.6} * 10 um = 1.486 um$$

 $Vgs1 = 416 \, mV$





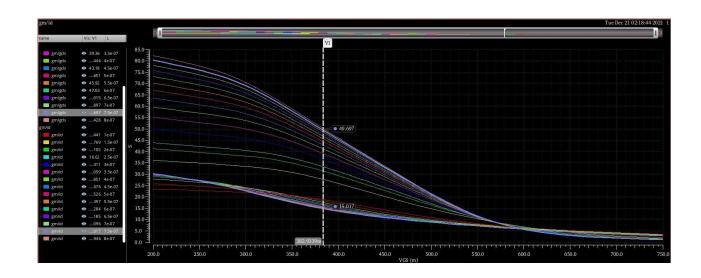
$$\frac{gm}{id} = 15$$

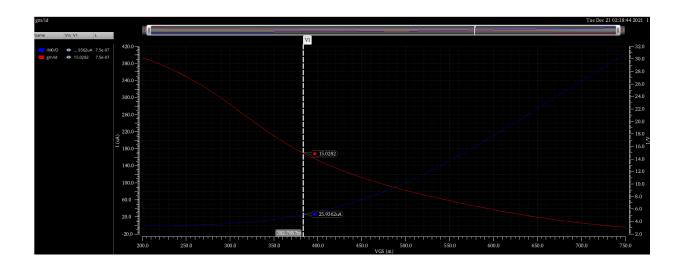
$$\frac{gm}{gds} = 48.9$$

 $l=750\,nm$

 $w=7.656\,um$

 $Vgs3 = 382.9 \, mV$





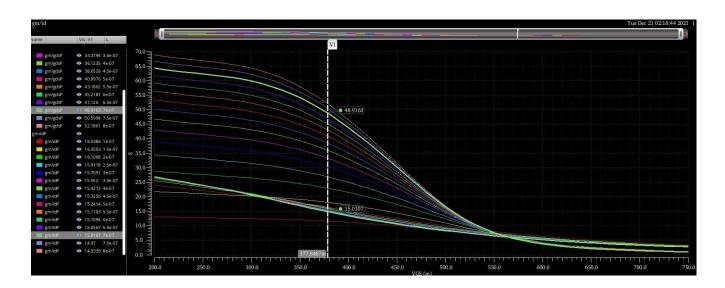
$$\frac{gm}{id} = 15$$

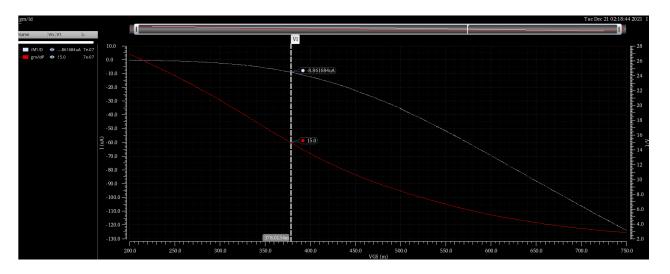
$$\frac{gm}{gds} = 48.9$$

 $l=700\,nm$

 $w=22.584\,um$

 $Vgs5 = -378 \, mV$





$$\frac{gm}{id} = 15$$

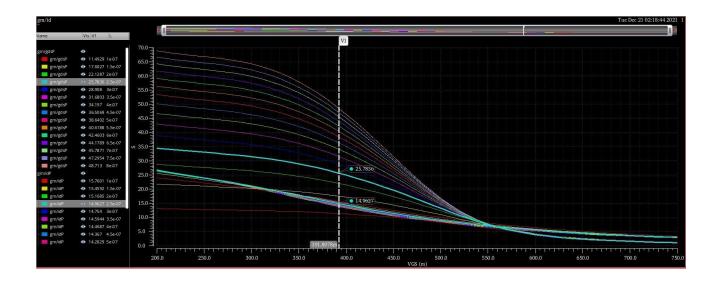
$$\frac{gm}{gds} = 24.45$$

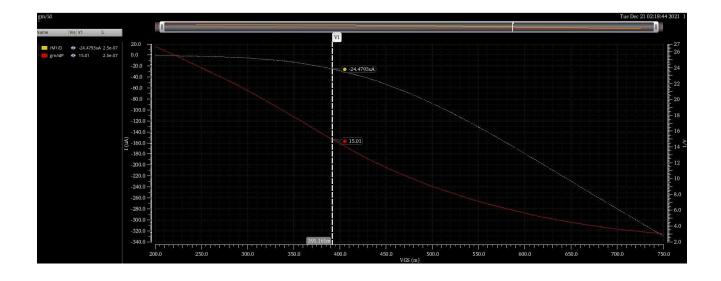
 $l=250\,nm$

 $w = 8.139 \, um$

 $Vgs7 = -391.5 \, mV$

 $Vload = 1.2 - 391.5m = 0.808 \, mV$





Mss

from V input common mode min and VGS1

 $Vov5 < 334 \, mV$

 $Vovss = 200 \, mV$ assumption

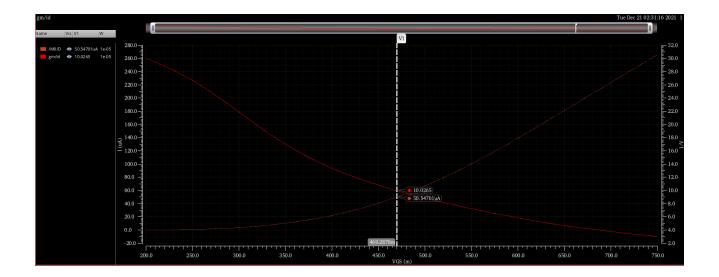
gmss

 $\frac{d}{id} = 10$

L = 1.2 um assumption

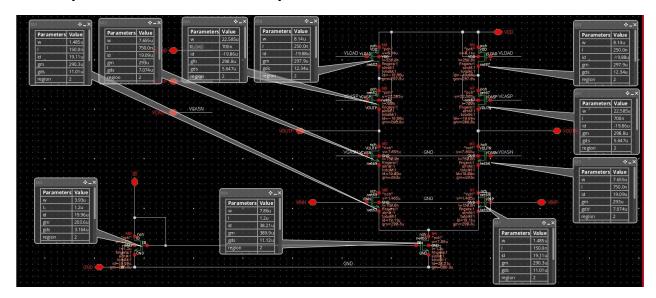
 $w = 7.86 \, um$

 $Vgsss = 474 \, mV$

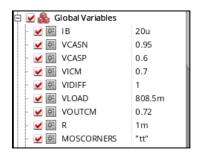


3. Final Design

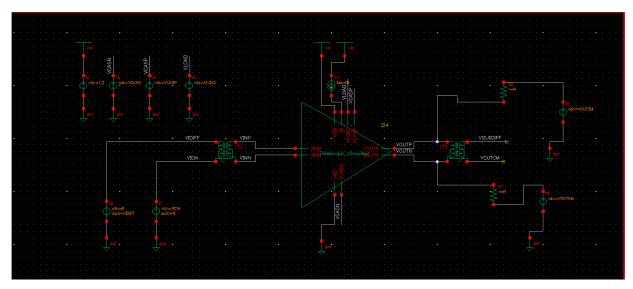
telescopic cascode differential amplifier:



Bias voltages:

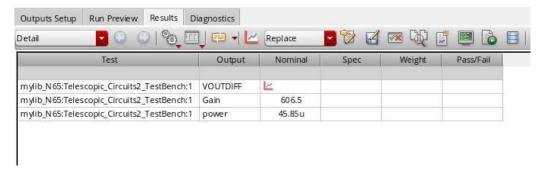


telescopic cascode differential amplifier testbench:

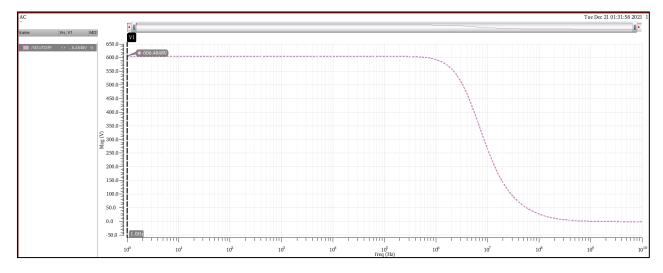


4. Gain and power

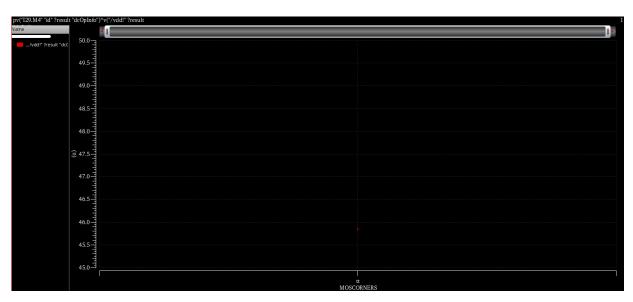
Power and gain:



gain:



Power:



5. Comparison

	gm hand	gm sim	error	ro hand	ro sim	error
M1	300 uS	290.3 uS	3.3 %	81.5 Kohm	90.8 Kohm	10 %
M3	300 uS	293 uS	2.3 %	163 Kohm	141.4 Kohm	15 %
M5	300 uS	298.8 uS	0.4 %	163 Kohm	177.1 Kohm	7.9 %
M7	300 uS	297.9 uS	0.7 %	81.5 Kohm	81.03 Kohm	0.6 %
MSS	400 uS	389.9 uS	2.5 %	-	-	-

$$gain\ error = \frac{gain\ sim - gain\ hand}{gain\ sim} = 0.99\%$$

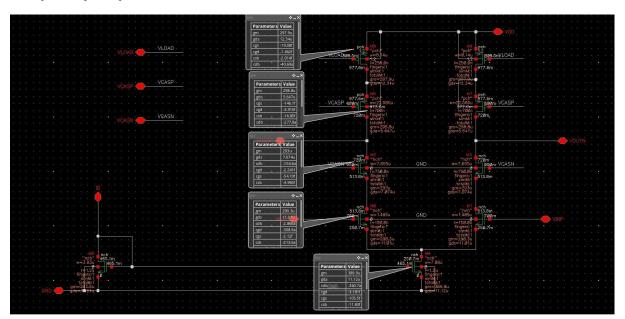
$$I_{SS}$$
 $error = \frac{I_{SS} sim - I_{SS} hand}{I_{SS} sim} = 4.7 \%$

6. Frequency response

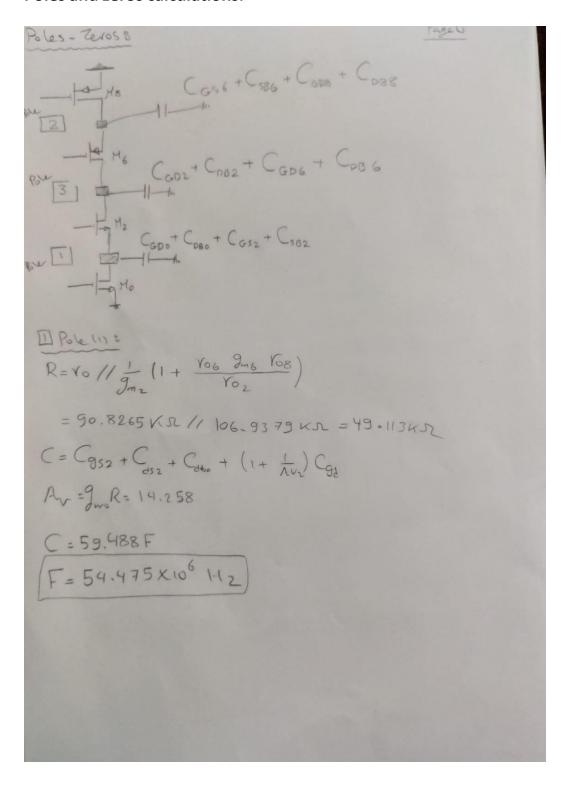
6.1 Hand analysis

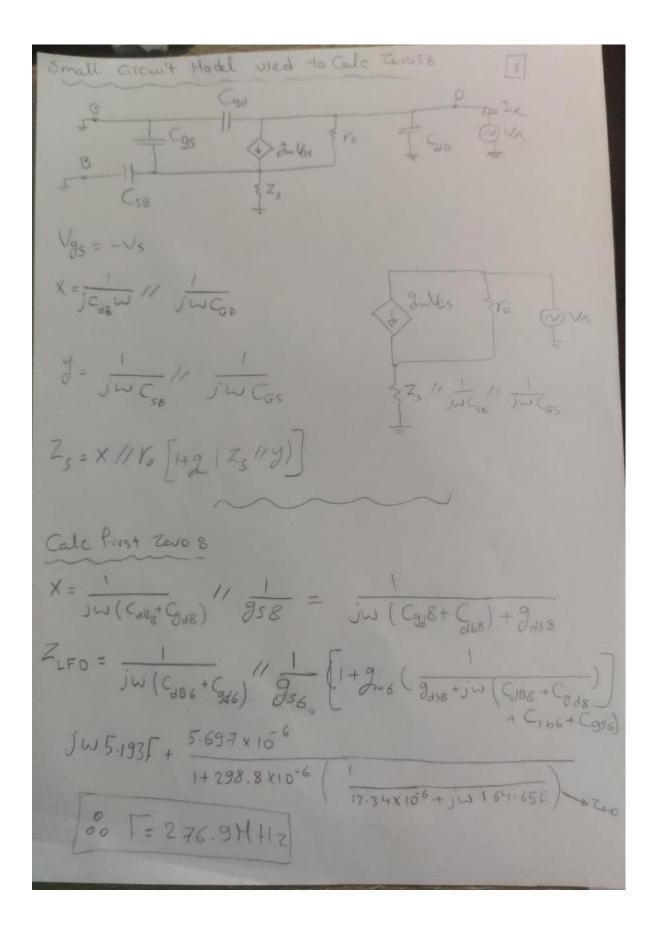
Since the poles are close to each other so they affected each other so they are different from simulations poles results.

Frequency response of transistors:



Poles and zeros calculations:



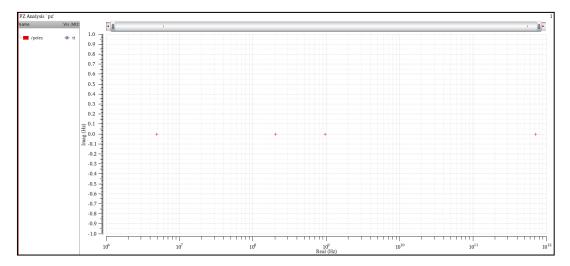


750= Jul (Cyg2+Cg/2) 9ds2 (1+ (8m2+2ubr) (9ds1+Jule) C1 = S80 + C900 + C562 + C952 = 59.47 F 9ds2 1+ (3m2+9m62) (9ds2+Jux) >00 (gmz+gmbz) (gds) + iwc) = 1 F= 841.36 HHz Third tero - oct so X

6.2 Simulation results

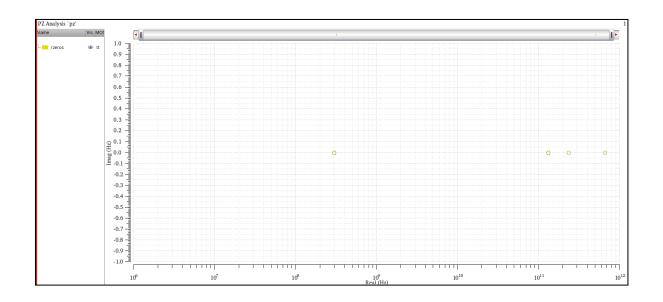
Poles:

_ qfactor	/poles Mtt (Hz)
1 500.0E-3	4.852E6
2 500.0E-3	204.1E6
3 500.0E-3	965.6E6
4 500.0E-3	716.7E9

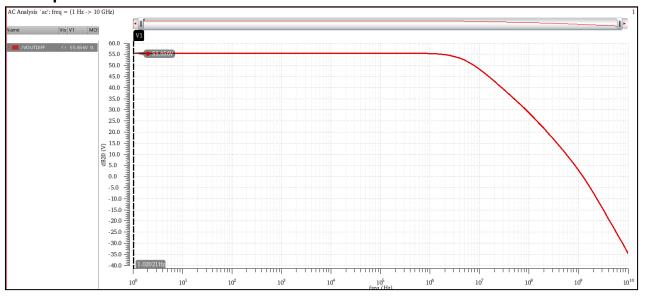


Zeros:

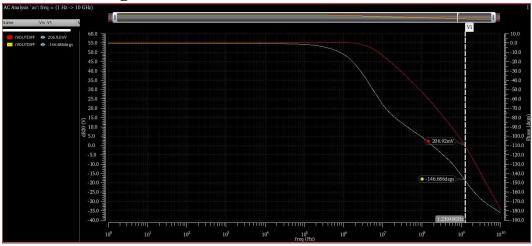
_ qfactor	/poles Mtt (Hz)	qfactor	/zeros Mtt (Hz)
1 500.0E-3	4.852E6	500.0E-3	299.6E6
2 500.0E-3	204.1E6	-500.0E-3	132.6E9
3 500.0E-3	965.6E6	-500.0E-3	236.4E9
4 500.0E-3	716.7E9	500.0E-3	665.0E9



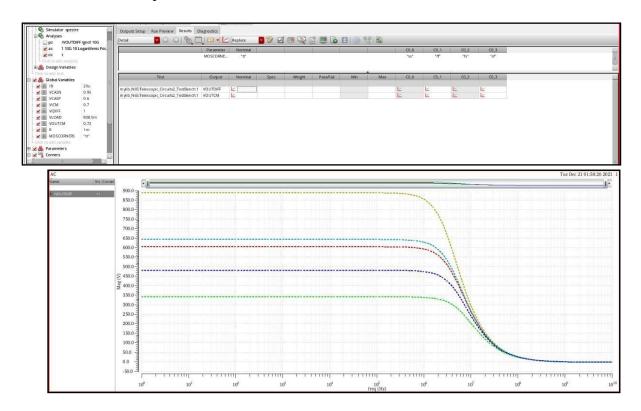
Bodie plot:



7. Phase margin

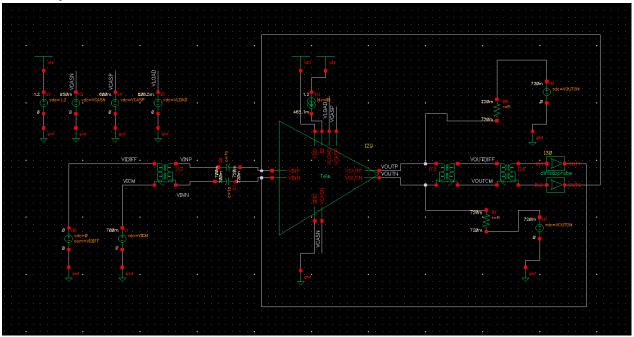


8. Corner analysis

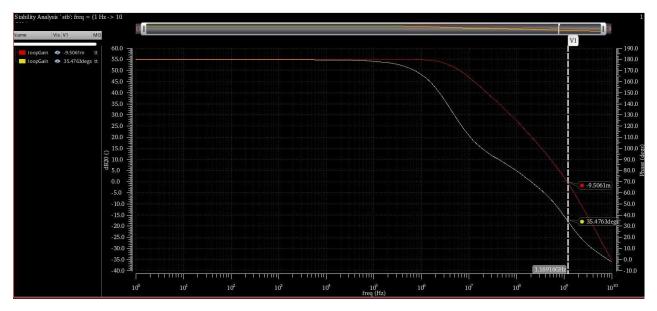


9. Stability analysis

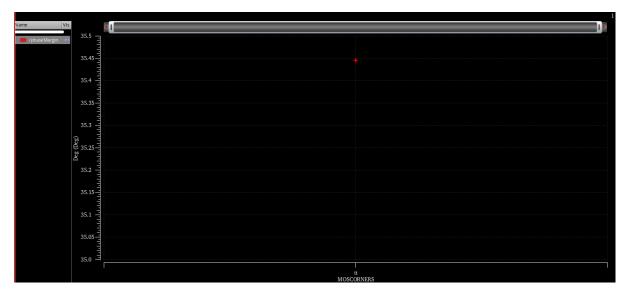
Stability test bench:



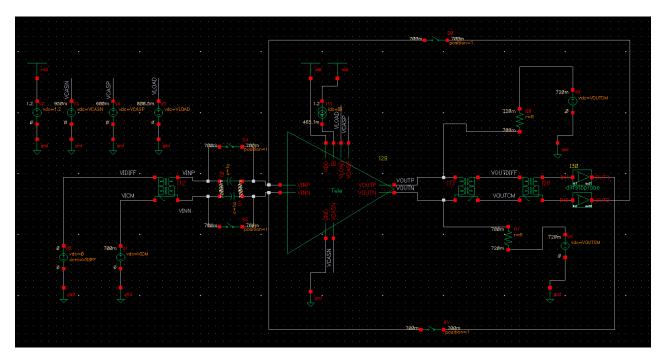
Stability loop gain:



Stability phase margin:



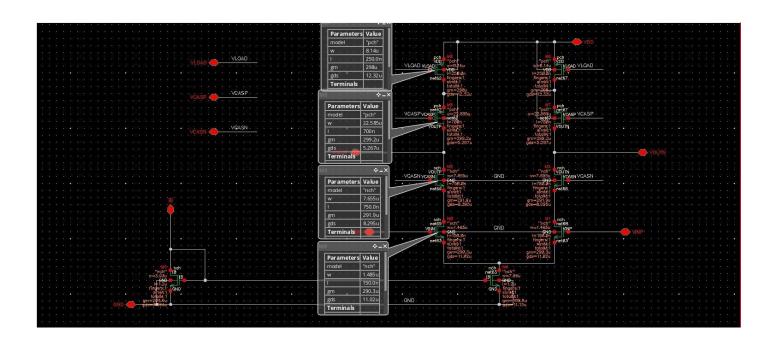
Final testbench



By changing switches conditions we can get open loop simulation and closed loop simulation as well.

10. Mistakes made then resolved

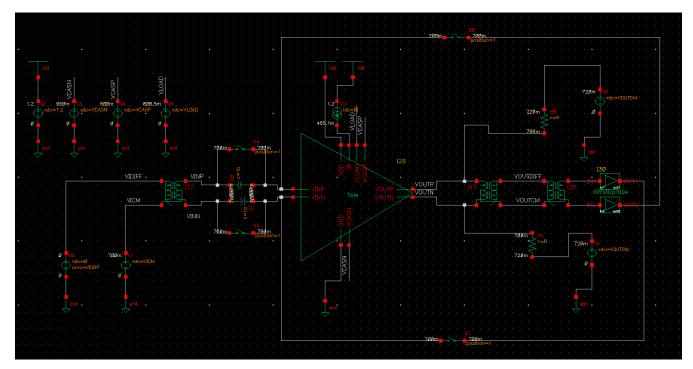
Old design:



Old gain:

Test	Output	Nominal	Spec	Weight	Pass/Fail
mylib_N65:Telescopic_Circuits2_TestBench:1	VOUTDIFF	<u>~</u>			
mylib_N65:Telescopic_Circuits2_TestBench:1	Gain	575.5			
mylib_N65:Telescopic_Circuits2_TestBench:1	power	45.85 u			

Stability test with wrong switch conditions:



Stability loop gain:

