EiceDRIVER™

High voltage gate driver IC

6ED family - 2nd generation

3 phase 600 V gate drive IC
6ED003L06-F2
6ED003L02-F2

EiceDRIVER™

datasheet

<Revision 2.8>, 05.08.2016

Industrial Power Control

Revision History	
Page or Item	**Subjects (major changes since previous revision)**
<Revision 2.8>, 05.08.2016	
p.15	Increased the maximum operating ambient temperature to 105 °C
p.2	Updated disclaimer
p.11	Updated parameter V_{HO}
all	revised wording for test temperature
pp. 8	Delete link to application note

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Last Trademarks Update 2010-10-26

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EiceDRIVER™
3 phase 600 V gate drive IC

1 Overview

Main features

- Thin-film-SOI-technology
- Maximum blocking voltage +600V
- Separate control circuits for all six drivers
- CMOS and LSTTL compatible input (negative logic)
- Signal interlocking of every phase to prevent cross-conduction
- Detection of over current and under voltage supply
- externally programmable delay for fault clear after over current detection

PG-DSO28

PG-TSSOP28
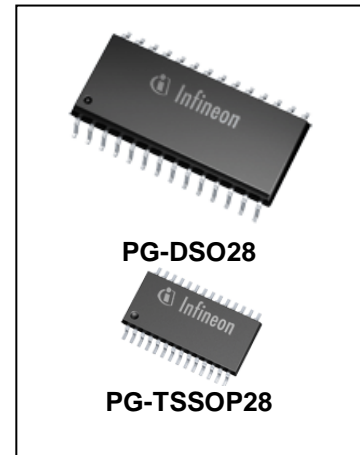
Product highlights

- Insensitivity of the bridge output to negative transient voltages up to -50V given by SOI-technology
- 'shut down' of all switches during error conditions

Typical applications

- Home appliances
- Fans, pumps
- General purpose drives

Product family

Table 1   Members of 6ED family – 2nd generation

Sales Name	high side control input HIN1,2,3 and LIN1,2,3	typ. UVLO-Thresholds	Bootstrap diode	Package
6ED003L06-F2 / 6ED003L02-F2	negative logic	11.7 V / 9.8 V	No	DSO28 / TSSOP28

Description

The devices are full bridge drivers to control power devices like MOS-transistors or IGBTs in 3-phase systems with a maximum blocking voltage of +600 V. Based on the used SOI-technology there is an excellent ruggedness on transient voltages. No parasitic thyristor structures are present in the device. Hence, no parasitic latch-up may occur at all temperatures and voltage conditions.

The six independent drivers are controlled at the low-side using CMOS resp. LSTTL compatible signals, down to 3.3 V logic. The device includes an under-voltage detection unit with hysteresis characteristic and an over-current detection. The over-current level is adjusted by choosing the resistor value and the threshold level at pin ITRIP. Both error conditions (under-voltage and over-current) lead to a definite shut down of all six switches. An error signal is provided at the FAULT open drain output pin. The blocking time after over-current can be adjusted with an RC-network at pin RCIN. The input RCIN owns an internal current source of 2.8 µA. Therefore, the resistor R_{RCIN} is optional. The typical output current can be given with 165 mA for pull-up and 375 mA for pull down. Because of system safety reasons a 310 ns interlocking time has been realised. The function of input EN can optionally be extended with an over-temperature detection, using an external NTC-resistor (see Fig.1).
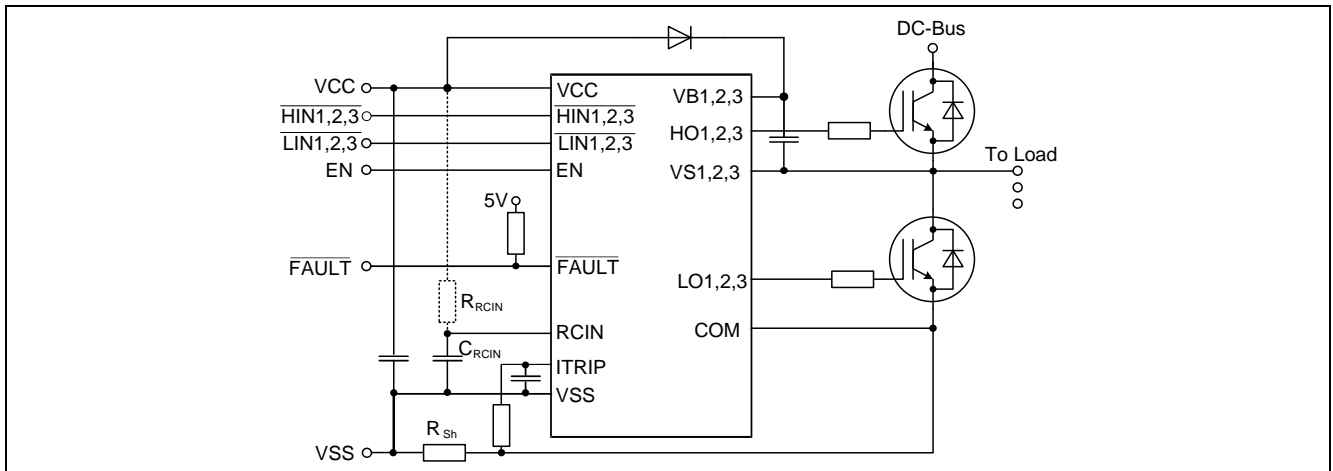
Figure 1   Typical Application

2   Blockdiagram
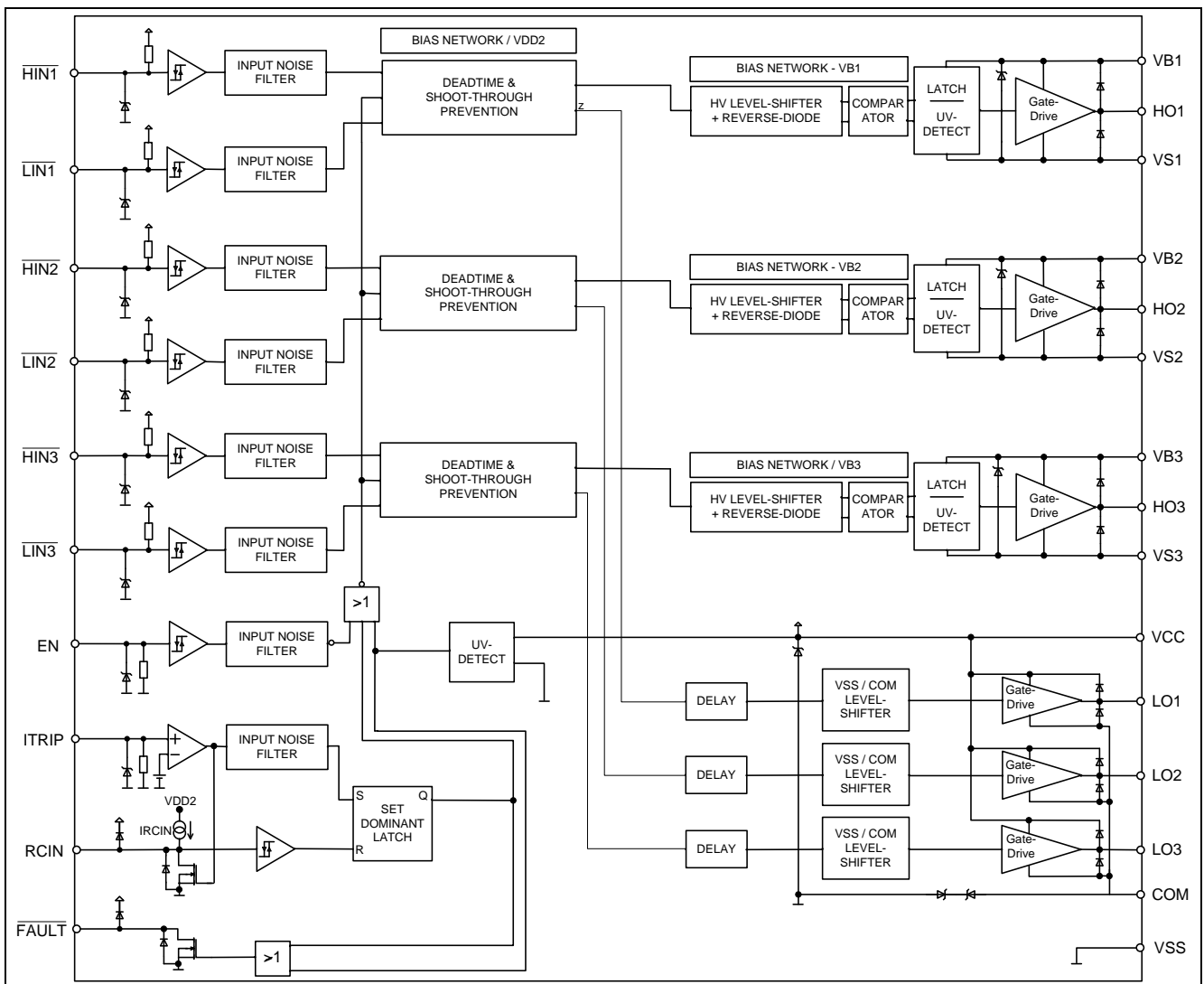
Figure 2   Block diagram for 6ED003L06-F2 / 6ED003L02-F2

3 Pin configuration, description, and functionality

1	VCC	VB1	28
2	$\overline{HIN1}$	HO1	27
3	$\overline{HIN2}$	VS1	26
4	$\overline{HIN3}$	nc	25
5	$\overline{LIN1}$	VB2	24
6	$\overline{LIN2}$	HO2	23
7	$\overline{LIN3}$	VS2	22
8	$\overline{FAULT}$	nc	21
9	ITRIP	VB3	20
10	EN	HO3	19
11	RCIN	VS3	18
12	VSS	nc	17
13	COM	LO1	16
14	LO3	LO2	15
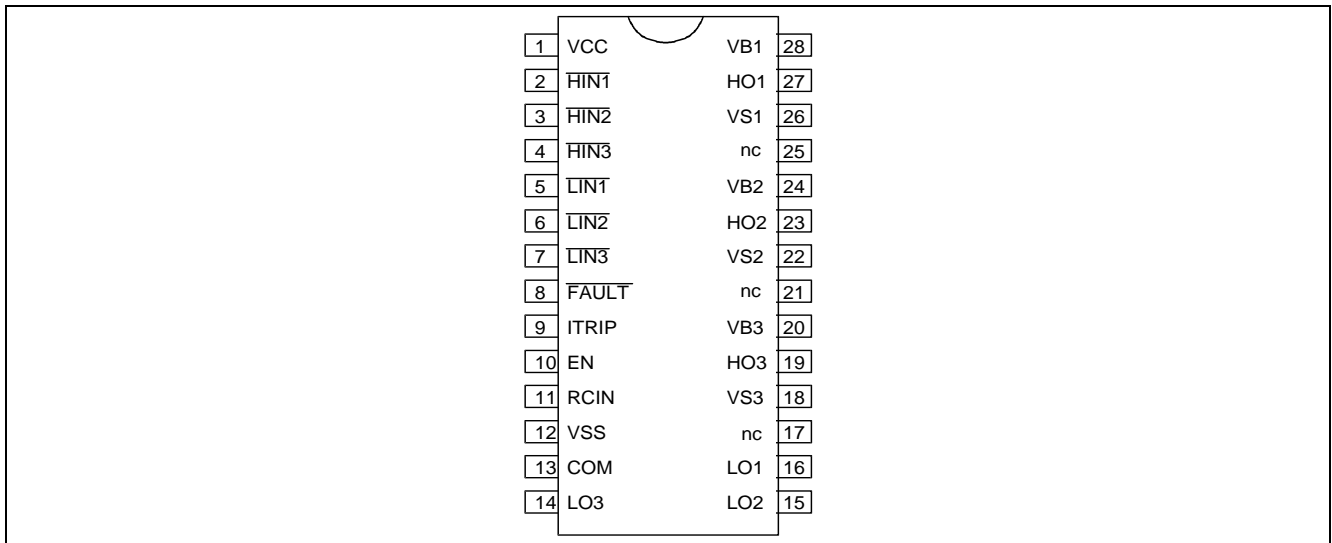
Figure 3   Pin Configuration of 6ED003L06-F2 and 6ED003L02-F2

Table 2   Pin Description

Symbol	Description
VCC	Low side power supply
VSS	Logic ground
/HIN1,2,3	High side logic input
/LIN1,2,3	Low side logic input
/FAULT	Indicates over-current and under-voltage (negative logic, open-drain output)
EN	Enable I/O functionality (positive logic)
ITRIP	Analog input for over-current shut down, activates FAULT and RCIN to VSS
RCIN	External RC-network to define FAULT clear delay after FAULT-Signal (T_{FLTCLR})
COM	Low side gate driver reference
VB1,2,3	High side positive power supply
HO1,2,3	High side gate driver output
VS1,2,3	High side negative power supply
LO1,2,3	Low side gate driver output
nc	Not connected

3.1   Low Side and High Side Control Pins (Pin 2, 3, 4, 5, 6, 7)

The Schmitt trigger input threshold of them are such to guarantee LSTTL and CMOS compatibility down to 3.3 V controller outputs. Input Schmitt trigger and noise filter provide beneficial noise rejection to short input pulses according to Figure 4 and Figure 5.
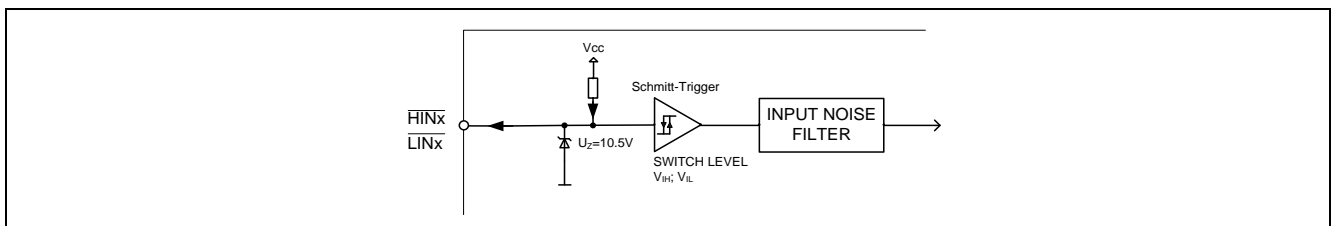
Figure 4   Input pin structure

An internal pull-up of about 75 kΩ (negative logic) pre-biases the input during supply start-up and a ESD zener clamp is provided for pin protection purposes. The zener diodes are therefore designed for single pulse stress only and not for continuous voltage stress over 10V.
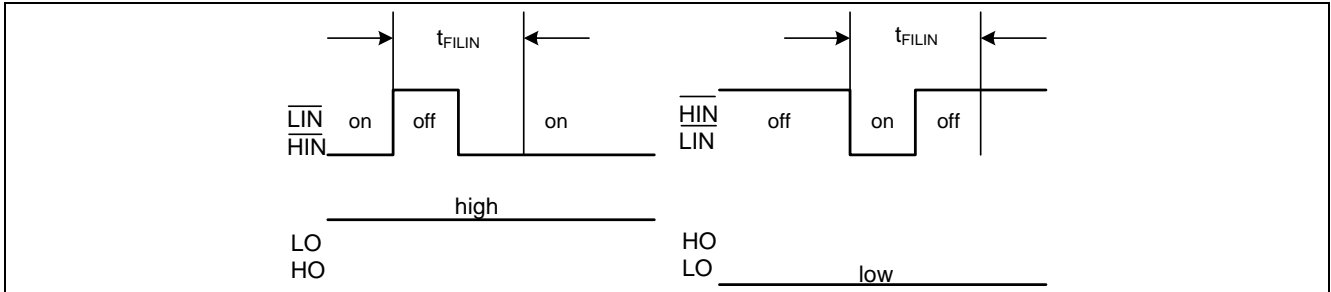
Figure 5   Input filter timing diagram

It is anyway recommended for proper work of the driver not to provide input pulse-width lower than 1 µs.

The 6ED-F2 driver IC provide additionally a shoot through prevention capability which avoids the simultaneous on-state of two channels of the same leg (i.e. HO1 and LO1, HO2 and LO2, HO3 and LO3). When two inputs of a same leg are activated, only one leg output is activated, so that the leg is kept steadily in a safe state.

A minimum dead time insertion of typ. 310 ns is also provided, in order to reduce cross-conduction of the external power switches.

3.2   EN (Gate Driver Enable, Pin 10)

The signal applied to pin EN controls directly the output stages. All outputs are set to LOW, if EN is at LOW logic level. The internal structure of the pin is given in Figure 6. The switching levels of the Schmitt-Trigger are here $V_{EN,TH+}$ = 2.1 V and $V_{EN,TH-}$ = 1.3 V. The typical propagation delay time is t_{EN} = 780 ns. There is an internal pull down resistor (75 kΩ), which keeps the gate outputs off in case of broken PCB connection.
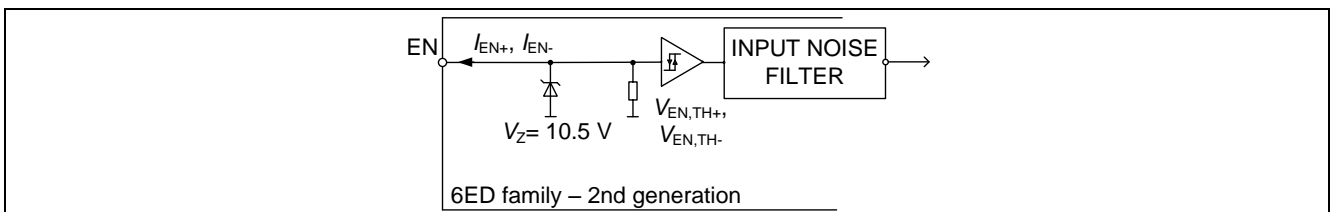
Figure 6   EN pin structures

3.3   /FAULT (Fault Feedback, Pin 8)

/Fault pin is an active low open-drain output indicating the status of the gate driver (see Figure 7). The pin is active (i.e. forces LOW voltage level) when one of the following conditions occur:

- Under-voltage condition of VCC supply: In this case the fault condition is released as soon as the supply voltage condition returns in the normal operation range (please refer to VCC pin description for more details).

- Over-current detection (ITRIP): The fault condition is latched until current trip condition is finished and RCIN input is released (please refer to ITRIP pin).
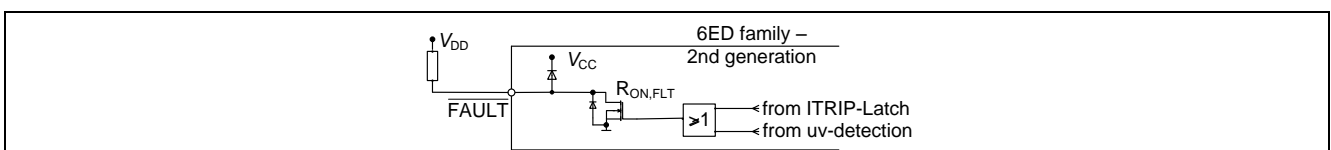
Figure 7   /FAULT pin structures

3.4   ITRIP and RCIN (Over-Current Detection Function, Pin 9, 11)

The 6ED family – 2nd generation provides an over-current detection function by connecting the ITRIP input with the motor current feedback. The ITRIP comparator threshold (typ 0.44 V) is referenced to VSS ground. A input noise filter (typ. t_{ITRIPMIN} = 230 ns) prevents the driver to detect false over-current events.

Over-current detection generates a hard shut down of all outputs of the gate driver and provides a latched fault feedback at /FAULT pin. RCIN input/output pin is used to determine the reset time of the fault condition. As soon as ITRIP threshold is exceeded the external capacitor connected to RCIN is fully discharged. The capacitor is then recharged by the RCIN current generator when the over-current condition is finished. As soon as RCIN voltage exceeds the rising threshold of typ $V_{\text{RCIN,TH}}$ = 5.2 V, the fault condition releases and the driver returns operational following the ontrol input pins according to section 3.1.

3.5   VCC, VSS and COM (Low Side Supply, Pin 1, 12,13)

VCC is the low side supply and it provides power both to input logic and to low side output power stage. Input logic is referenced to VSS ground as well as the under-voltage detection circuit. Output power stage is referenced to COM ground. COM ground is floating respect to VSS ground with a maximum range of operation of +/-5.7 V. A back-to-back zener structure protects grounds from noise spikes.

The under-voltage circuit enables the device to operate at power on when a typical supply voltage higher than $V_{\text{CCUV+}}$ is present.

The IC shuts down all the gate drivers power outputs, when the VCC supply voltage is below $V_{\text{CCUV-}}$ = 9.8 V. This prevents the external power switches from critically low gate voltage levels during on-state and therefore from excessive power dissipation. Please consult the individual output characteristic of the driven transistor.

3.6   VB1,2,3 and VS1,2,3 (High Side Supplies, Pin 18, 20, 22, 24, 26, 28)

VB to VS is the high side supply voltage. The high side circuit can float with respect to VSS following the external high side power device emitter/source voltage. Due to the low power consumption, the floating driver stage can be supplied by bootstrap topology connected to VCC. The device operating area as a function of the supply voltage is given in Figure 12.

3.7   LO1,2,3 and HO1,2,3 (Low and High Side Outputs, Pin 14, 15, 16, 19, 23, 27)

Low side and high side power outputs are specifically designed for pulse operation such as gate drive of IGBT and MOSFET devices. Low side outputs (i.e. LO1,2,3) are state triggered by the respective inputs, while high side outputs (i.e. HO1,2,3) are edge triggered by the respective inputs. In particular, after an under voltage condition of the VBS supply, a new turn-on signal (edge) is necessary to activate the respective high side output, while after a under voltage condition of the VCC supply, the low side outputs switch to the state of their respective inputs.

4 Electrical Parameters

4.1 Absolute Maximum Ratings

All voltages are absolute voltages referenced to V_{SS} -potential unless otherwise specified. All parameters are valid for T_a=25 °C.

Table 3   Abs. maximum ratings

Parameter		Symbol	Min.	Max.	Unit
High side offset voltage(Note 1)	DSO28 TSSOP28	V_S	V_{CC}-V_{BS}-6	600 180	V
High side offset voltage (t_p<500ns, Note 1)			V_{CC} -V_{BS} − 50	–	
High side offset voltage(Note 1)	DSO28 TSSOP28	V_B	V_{CC} − 6	620 200	
High side offset voltage (t_p<500ns, Note 1)			V_{CC} − 50	–	
High side floating supply voltage (V_B vs. V_S) (internally clamped)		V_{BS}	-1	20	
High side output voltage (V_{HO} vs. V_S)		V_{HO}	-0.5	V_B + 0.5	
Low side supply voltage (internally clamped)		V_{CC}	-1	20	
Low side supply voltage (V_{CC} vs. V_{COM})		V_{CCOM}	-0.5	25	
Gate driver ground		V_{COM}	-5.7	5.7	
Low side output voltage (V_{LO} vs. V_{COM})		V_{LO}	-0.5	V_{CCOM} + 0.5	
Input voltage /LIN, /HIN, EN, ITRIP		V_{IN}	-1	10	
FAULT output voltage		V_{FLT}	-0.5	V_{CC} + 0.5	
RCIN output voltage		V_{RCIN}	-0.5	V_{CC} + 0.5	
Power dissipation (to package) Note 2	DSO28 TSSOP28	P_D	– –	1.3 0.6	W
Thermal resistance (junction to ambient, see section 6)	DSO28 TSSOP28	$R_{th(j-a)}$	– –	75 165	K/W
Junction temperature		T_J	–	125	°C
Storage temperature		T_S	- 40	150	
offset voltage slew rate (Note 3)		dV_S/dt		50	V/ns

Note :The value for ESD immunity is 1.0kV (Human Body Model). ESD immunity for pins inside the low side (i.e. VCC, /HINx, /LINx, FAULT, EN, RCIN, ITRIP, VSS, COM, LOx) and ESD immunity for pins inside each high side itself (i.e. VBx, HOx, VSx) is guaranteed up to 1.5kV (Human Body Model).

Note 1 : Insensitivity of bridge output to negative transient voltage up to −50V is not subject to production test − verified by design / characterization. External bootstrap diode is mandatory. Refer to application note.

Note 2: Consistent power dissipation of all outputs. All parameters inside operating range.

Note 3: Not subject of production test, verified by characterisation

4.2 Required operation conditions

All voltages are absolute voltages referenced to V_{SS} -potential unless otherwise specified. All parameters are valid for T_a=25 °C.

Table 4   Required Operation Conditions

Parameter		Symbol	Min.	Max.	Unit
High side offset voltage (Note 1)	DSO28 TSSOP28	V_B	7	620 200	V
Low side supply voltage (V_{CC} vs. V_{COM})	DSO28 TSSOP28	V_{CCOM}	10	25	

4.3 Operating Range

All voltages are absolute voltages referenced to V_{SS} -potential unless otherwise specified. (T_a = 25°C)

Table 5   Operating range

Parameter	Symbol	Min.	Max.	Unit
High side floating supply offset voltage	V_S	V_{CC} - V_{BS} -1	500	V
High side floating supply offset voltage (V_B vs. V_{CC}, statically)	V_{BCC}	-1.0	500	
High side floating supply voltage (V_B vs. V_S, Note 1)	V_{BS}	13	17.5	
High side output voltage (V_{HO} vs. V_S)	V_{HO}	0	V_{BS}	
Low side output voltage (V_{LO} vs. V_{COM})	V_{LO}	0	V_{CC}	
Low side supply voltage	V_{CC}	13	17.5	
Low side ground voltage	V_{COM}	-2.5	2.5	
Logic input voltages /LIN, /HIN, EN, ITRIP (Note 2)	V_{IN}	0	5	
FAULT output voltage	V_{FLT}	0	V_{CC}	
RCIN input voltage	V_{RCIN}	0	V_{CC}	
Pulse width for ON or OFF (Note 3)	t_{IN}	1	–	µs
Ambient temperature	T_a	-40	105	°C

Note 1 : Logic operational for V_B (V_B vs. V_{SS}) > 7,0V

Note 2 : All input pins (/HINx, /LINx) and EN, ITRIP pin are internally clamped (see abs. maximum ratings)

Note 3 : In case of input pulse width at /LINx and /HINx below 1µs the input pulse may not be transmitted properly

4.4 Static logic function table

VCC	VBS	RCIN	ITRIP	ENABLE	FAULT	LO1,2,3	HO1,2,3
$<V_{CCUV-}$	X	X	X	X	0	0	0
15V	$<V_{BSUV-}$	X	0	3.3 V	High imp	/LIN1,2,3	0
15V	15V	<3.2 V ↓	0	3.3 V	0	0	0
15V	15V	X	$> V_{IT,TH+}$	3.3 V	0	0	0
15V	15V	$> V_{RCIN,TH}$	0	3.3 V	High imp	/LIN1,2,3	/HIN1,2,3
15V	15V	$> V_{RCIN,TH}$	0	0	High imp	0	0

4.5 Static parameters

$V_{CC} = V_{BS} = 15V$ unless otherwise specified. All parameters are valid for T_a=25 °C.

Table 6   Static parameters

Parameter		Symbol	Values			Unit	Test condition
			Min.	Typ.	Max.		
High level input voltage		V_{IH}	1.7	2.1	2.4	V	
Low level input voltage		V_{IL}	0.7	0.9	1.1		
EN positive going threshold		$V_{EN,TH+}$	1.9	2.1	2.3		
EN negative going threshold		$V_{EN,TH-}$	1.1	1.3	1.5		
ITRIP positive going threshold		$V_{IT,TH+}$	380	445	510	mV	
ITRIP input hysteresis		$V_{IT,HYS}$	45	70			
RCIN positive going threshold		$V_{RCIN,TH}$	-	5.2	6.4	V	
RCIN input hysteresis		$V_{RCIN,HYS}$	-	2.0	-		
Input clamp voltage (/HIN, /LIN, EN, ITRIP)		$V_{IN,CLMAP}$	9	10.3	12		I_{IN} = 4mA
Input clamp voltage at high impedance (/HIN, /LIN)		$V_{IN,FLOAT}$	-	5.3	5.8		controller output pin floating
High level output voltage	LO1,2,3	V_{OH}	-	V_{CC} -0.7	V_{CC} -1.4		I_O = 20mA
	HO1,2,3		-	V_B -0.7	V_B -1.4		
Low level output voltage	LO1,2,3	V_{OL}	-	V_{COM}+ 0.2	V_{COM}+ 0.6		I_O = -20mA
	HO1,2,3		-	V_S+ 0.2	V_S + 0.6		
V_{CC} and V_{BS} supply undervoltage positive going threshold		V_{CCUV+} V_{BSUV+}	11	11.7	12.5		
V_{CC} and V_{BS} supply undervoltage negative going threshold		V_{CCUV-} V_{BSUV-}	9.5	9.8	10.8	V	
V_{CC} and V_{BS} supply undervoltage lockout hysteresis		V_{CCUVH} V_{BSUVH}	1.2	1.9	-		

Table 6   Static parameters

Parameter	Symbol	Values			Unit	Test condition
		Min.	Typ.	Max.		
High side leakage current betw. VS and VSS	I_{LVS+}	-	1	12.5	µA	V_S = 600V
High side leakage current betw. VS and VSS	I_{LVS+}[1]	-	10	-		T_J = 125°C, V_S = 600V
High side leakage current between VSx and VSy (x=1,2,3 and y=1,2,3)	I_{LVS-}[1]	-	10	-		T_J = 125°C V_{Sx} - V_{Sy} = 600V
Quiescent current V_{BS} supply (VB only)	I_{QBS1}	-	210	400	µA	HO=low
Quiescent current V_{BS} supply (VB only)	I_{QBS2}	-	210	400		HO=high
Quiescent current V_{CC} supply (VCC only)	I_{QCC1}	-	1.1	1.8	mA	V_{LIN}=float.
Quiescent current V_{CC} supply (VCC only)	I_{QCC2}	-	1.3	2		V_{LIN}=0, V_{HIN}=3.3 V
Input bias current	I_{LIN+}	-	70	100	µA	V_{LIN}=3.3 V
Input bias current	I_{LIN-}	-	110	200	µA	V_{LIN}=0
Input bias current	I_{HIN+}	-	70	100		V_{HIN}=3.3 V
Input bias current	I_{HIN-}	-	110	200		V_{HIN}=0
Input bias current (ITRIP=high)	I_{ITRIP+}		45	120		V_{ITRIP}=3.3 V
Input bias current (EN=high)	I_{EN+}	-	45	120		V_{ENABLE}=3.3 V
Input bias current RCIN (internal current source)	I_{RCIN}		2.8			V_{RCIN} = 2 V
Mean output current for load capacity charging in range from 3 V (20%) to 6 V (40%)	I_{O+}	120	165	-	mA	C_L=10 nF
Peak output current turn on (single pulse)	I_{Opk+}[1]		240			R_L = 0 Ω, t_p <10 µs
Mean output current for load capacity discharging in range from 12 V (80%) to 9 V (60%)	I_{O-}	250	375	-		C_L=10 nF
Peak output current turn off (single pulse)	I_{Opk-}[1]		420			R_L = 0 Ω, t_p <10 µs
RCIN low on resistance of the pull down transistor	$R_{on,RCIN}$	-	40	100		V_{RCIN}=0.5 V
FAULT low on resistance of the pull down transistor	$R_{on,FLT}$	-	45	100		V_{FAULT}=0.5 V

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[1] Not subject of production test, verified by characterisation

4.6 Dynamic parameters

$V_{CC} = V_{BS} = 15$ V, $V_S = V_{SS} = V_{COM}$ unless otherwise specified. All parameters are valid for T_a=25 °C.

Table 7   Dynamic parameters

| Parameter	Symbol	Values			Unit	Test condition
		Min.	Typ.	Max.		
Turn-on propagation delay	t_{on}	400	530	800	ns	$V_{LIN/HIN}$ = 0 or 3.3 V
Turn-off propagation delay	t_{off}	360	490	760		
Turn-on rise time	t_r	-	60	100		$V_{LIN/HIN}$ = 0 or 3.3 V
Turn-off fall time	t_f	-	26	45		C_L = 1 nF
Shutdown propagation delay ENABLE	t_{EN}	-	780	1100		V_{EN}=0
Shutdown propagation delay ITRIP	t_{ITRIP}	400	670	1000		V_{ITRIP}=1 V
Input filter time ITRIP	$t_{ITRIPMIN}$	155	230	380		
Propagation delay ITRIP to FAULT	t_{FLT}	-	420	700		
Input filter time at LIN/HIN for turn on and off	t_{FILIN}	120	300	-		$V_{LIN/HIN}$ = 0 & 3.3 V
Input filter time EN	t_{FILEN}	300	600	-		
Fault clear time at RCIN after ITRIP-fault, (C_{RCin}=1nF)	t_{FLTCLR}	1.0	1.9	3.0	ms	$V_{LIN/HIN}$ = 0 & 3.3 V V_{ITRIP} = 0
Dead time	DT	150	310	-	ns	$V_{LIN/HIN}$ = 0 & 3.3 V
Matching delay ON, max(ton)-min(ton), ton are applicable to all 6 driver outputs	MT$_{ON}$	-	20	100		external dead time > 500 ns
Matching delay OFF, max(toff)-min(toff), toff are applicable to all 6 driver outputs	MT$_{OFF}$	-	40	100		external dead time >500 ns
Output pulse width matching. Pw$_{in}$-PW$_{out}$	PM		40	100		PW$_{in}$ > 1 µs

5 Timing diagrams
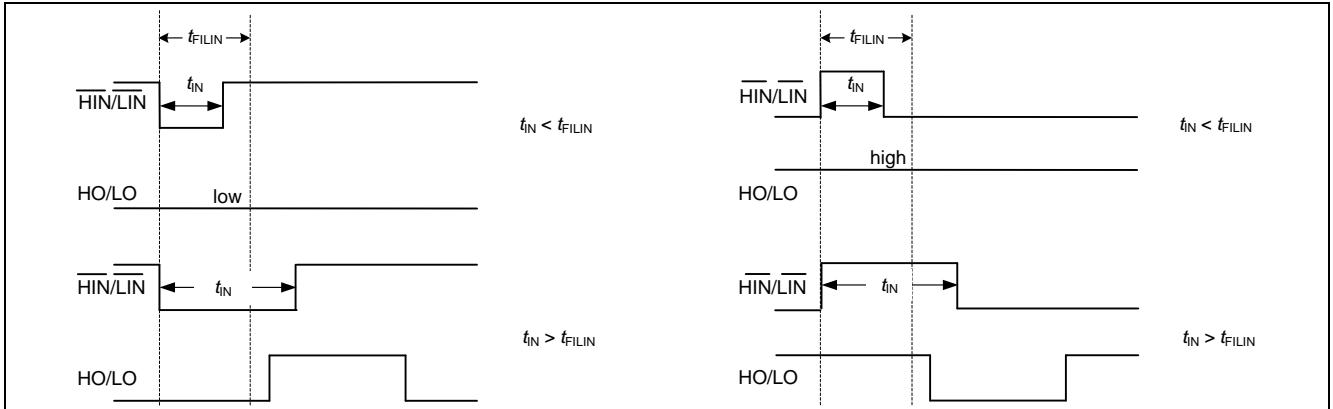
Figure 8 **Timing of short pulse suppression**
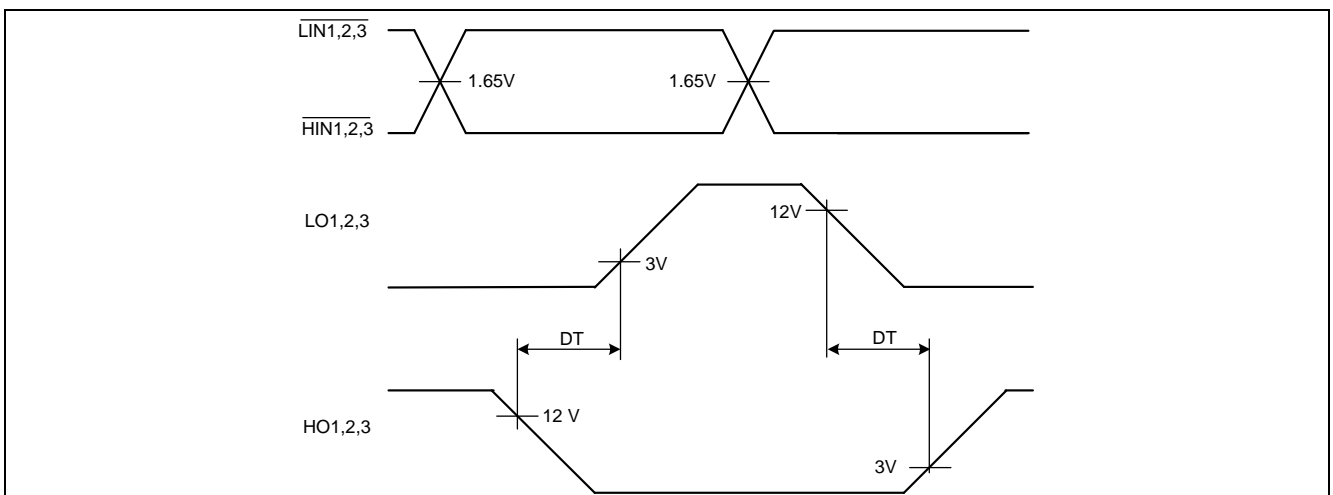

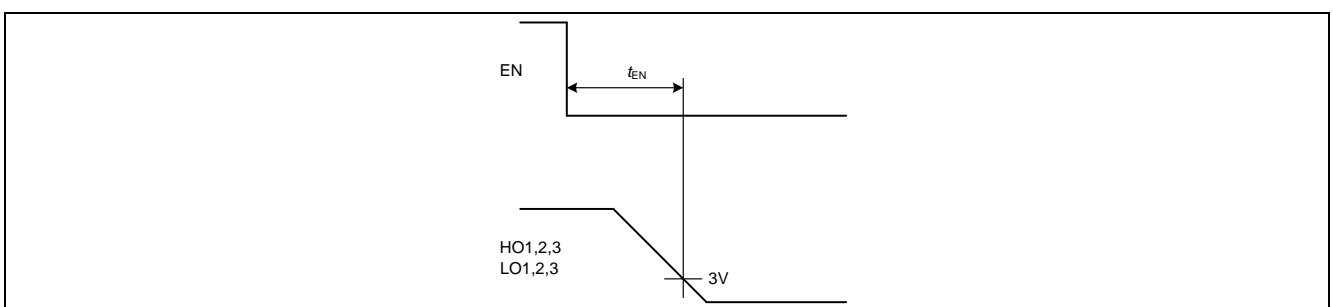**Figure 9** **Timing of internal deadtime**

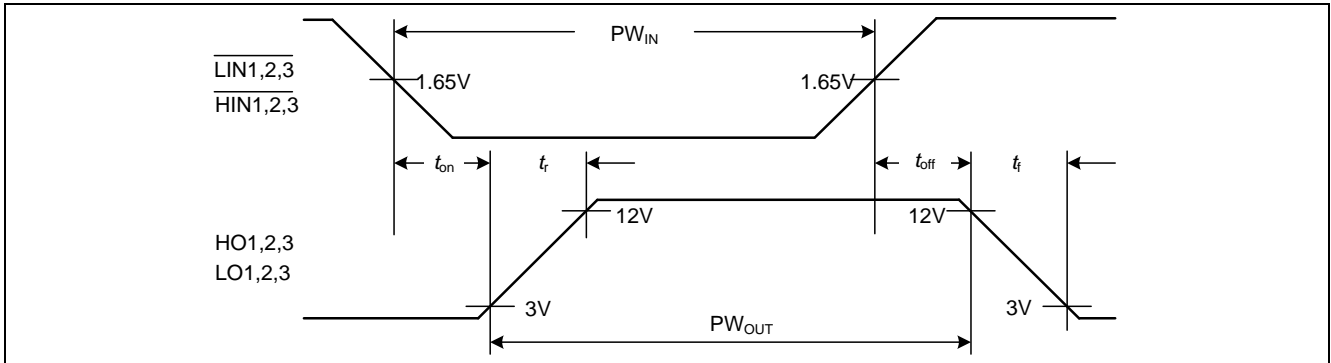**Figure 10** **Enable delay time definition**

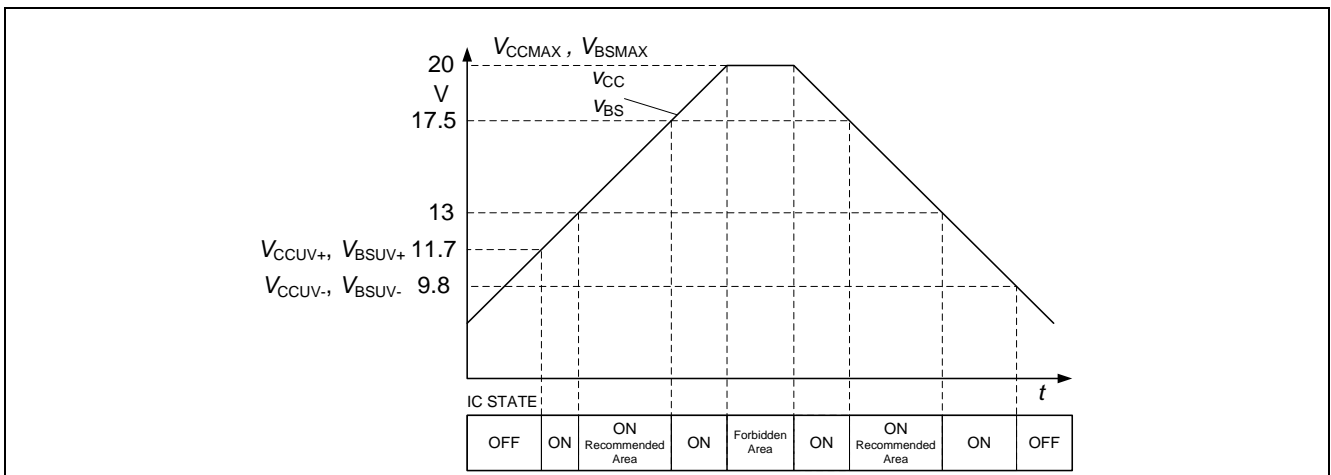**Figure 11   Input to output propagation delay times and switching times definition**
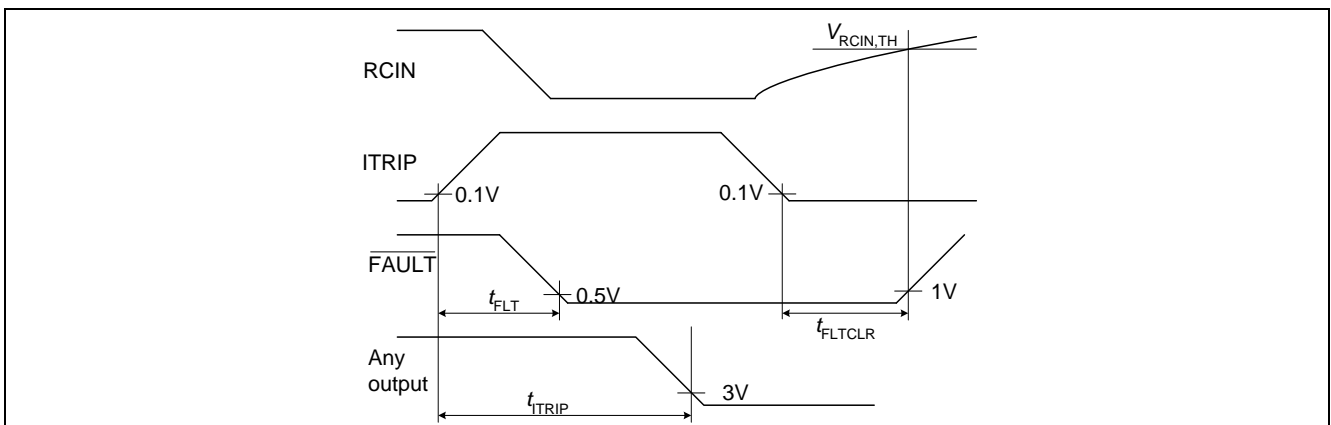

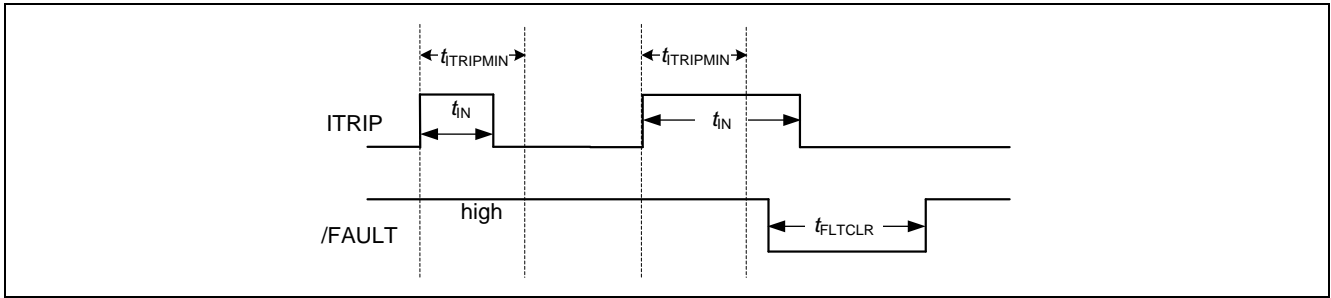**Figure 12   Operating areas**

Figure 13   ITRIP-Timing

Figure 14   ITRIP input filter time

6 Package

6.1 PG-DSO-28

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	2,65	-	0,104
A1	0,10	0,30	0,004	0,012
b	0,33	0,51	0,013	0,020
c	0,23	0,32	0,009	0,013
D	17,70	18,10	0,697	0,713
E	10,00	10,63	0,394	0,419
E1	7,40	7,60	0,291	0,299
e	1,27 BSC		0,050 BSC	
N	28		28	
L	0,40	1,27	0,016	0,050
h	0,25	0,75	0,010	0,030
Θ	0°	8°	0°	8°
F1	9,73		0,383	
F2	0,65		0,026	
F3	1,67		0,066	

1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
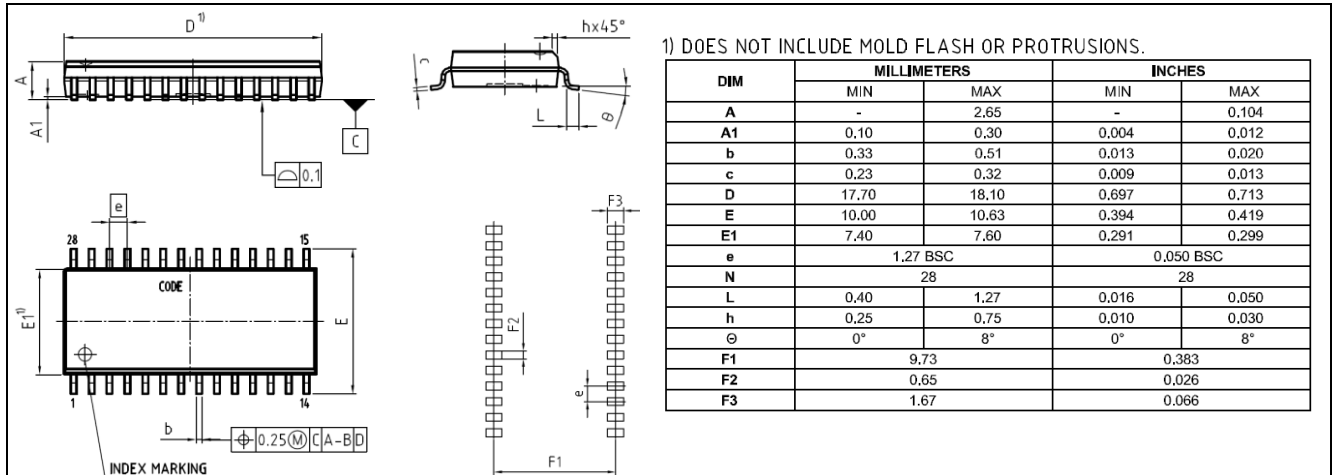
Figure 15   Package drawing

Dimensions	$80.0 \times 80.0 \times 1.5$ mm³	λ_{therm} [W/m·K]
Material	FR4	0.3
Metal (Copper)	70µm	388
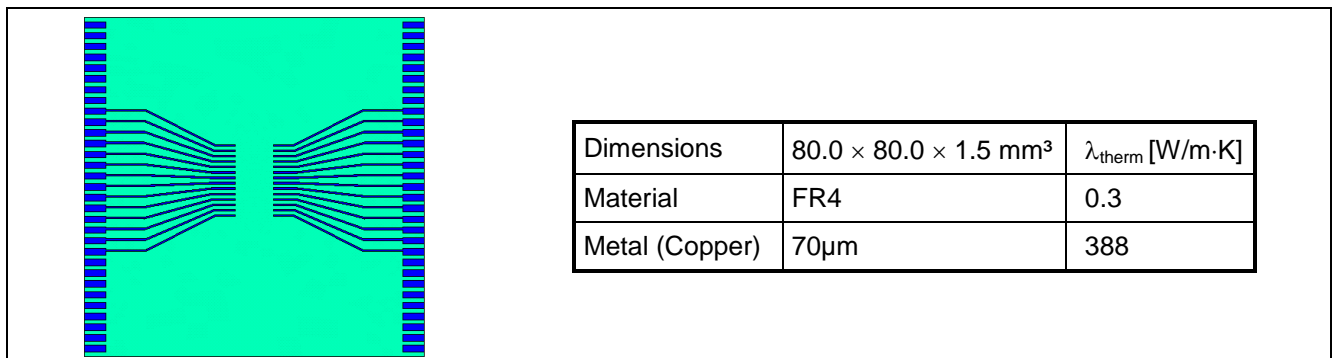
Figure 16   PCB reference layout

6.2 PG-TSSOP-28

Footprint for Reflow soldering
e = 0.65
A = 6.10
L = 1.30
B = 0.40

HLG05506

Index Marking

[1] Does not include plastic or metal protrusion of 0.15 max. per side
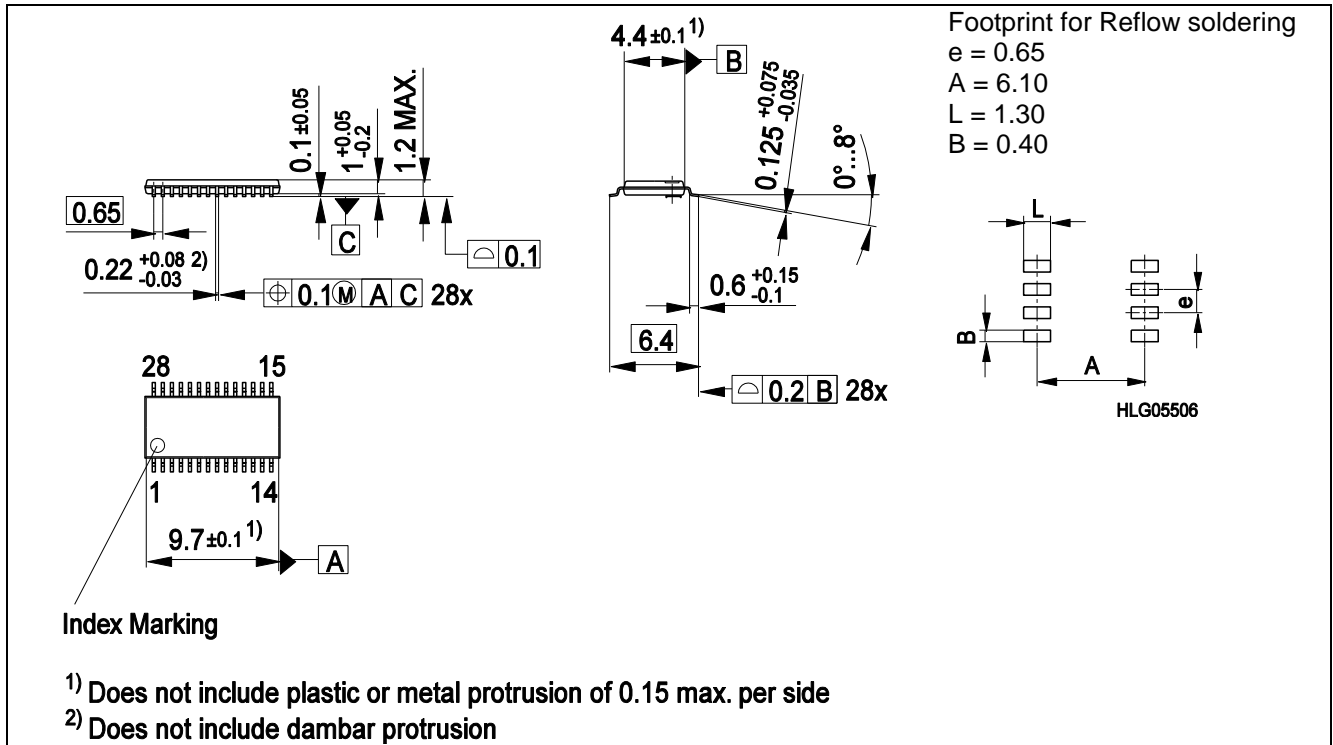[2] Does not include dambar protrusion
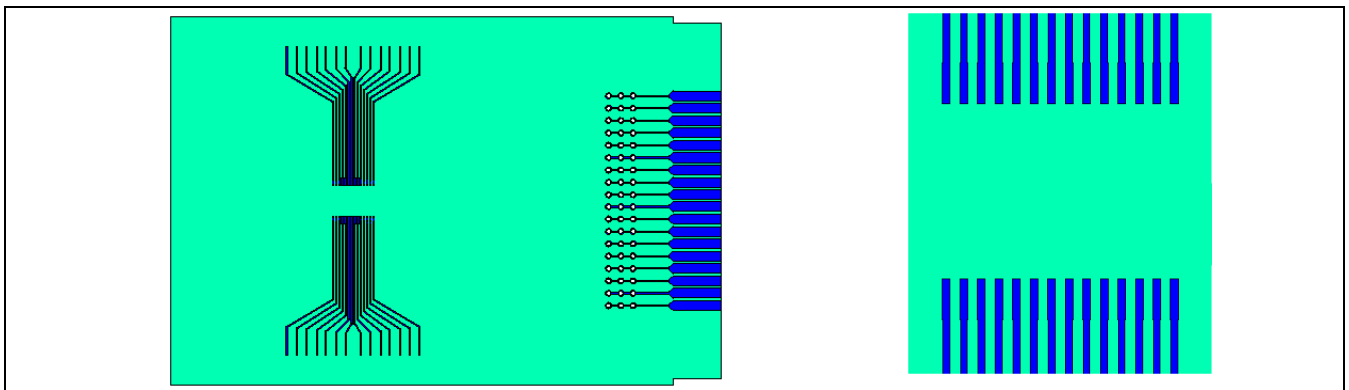
Figure 17   Package drawing

**Figure 18   PCB reference layout (according to JEDEC 1s0P)
left: Reference layout
right: detail of footprint**

Table 8   Data of reference layout

Dimensions	Material	Metal (Copper)
$76.2 \times 114.3 \times 1.5$ mm³	FR4 ($\lambda_{therm} = 0.3$ W/mK)	70µm ($\lambda_{therm} = 388$ W/mK)