

Training Course  
on

# FPGA based Digital Design using Verilog HDL



By

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# Design Implementation

## ☐ Running Implement Design

The Implement Design process converts the logical design represented in that source (and all sources in the hierarchy from that source down) into a physical file format that can be implemented in the selected target device.

First, run all processes (Synthesis through Place & Route) associated with the your design files. To do so, run Implement Design on the HDL files:

1. Select top (top.v) in the Sources in Project window.

# Design Implementation

## ❑ Running Implement Design

2. Double-click Implement Design in the Processes for Source “top” window.

This runs all processes.

**NOTE:** A check mark in the Processes for Source window denotes a process that was run successfully. An exclamation mark indicates that the process was run and that there is a warning for the process. More information about warnings can be obtained in the Transcript window.

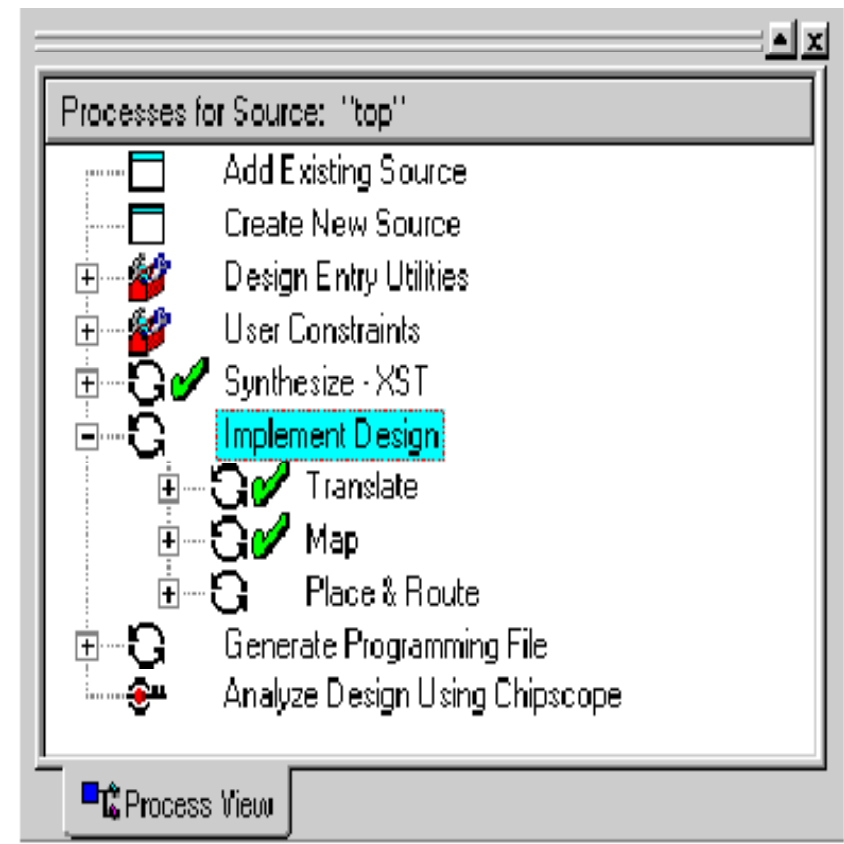


Figure 1 : Implement Design processes



## Design Implementation

### □ Implementation sub-processes

- The **Translate process** merges all of the input netlists and design constraint information and outputs a Xilinx NGD (Native Generic Database) file. The output NGD file can then be mapped to the targeted device family.
- The **Map process** first performs a logical DRC (Design Rule Check) on the design in the NGD file produced by the Translate process. Map then maps the logic to the components (logic cells, I/O cells, and other components) in the target Xilinx FPGA. The output design is an NCD (Native Circuit Description) file physically representing the design



## Design Implementation

### □ **Implementation sub-processes – contd'**

mapped to the components in the Xilinx FPGA. The NCD file can then be placed and routed.

- The **Place and Route process** (PAR) takes a mapped NCD file, places and routes the design, and produces an NCD file to be used by the programming file generator (BitGen).



## Design Implementation

### **□ Viewing the Design in Floorplanner**

Now, you can view the implemented design in Floorplanner. The Floorplanner is a graphical tool in which you can view and change the design hierarchy, floorplan, and perform design rule checks.

- 1. In Project Navigator, select top (top.v) in the Sources in Project window.**
- 2. In the Processes for Source window, click the + sign beside Implement Design and the + sign beside Place & Route.**
- 3. Double-click View/Edit Placed Design (Floorplanner)**

The Floorplanner tool is launched and displays the placement of the design for the project.



## Design Implementation

### □ Viewing the Design in Floorplanner

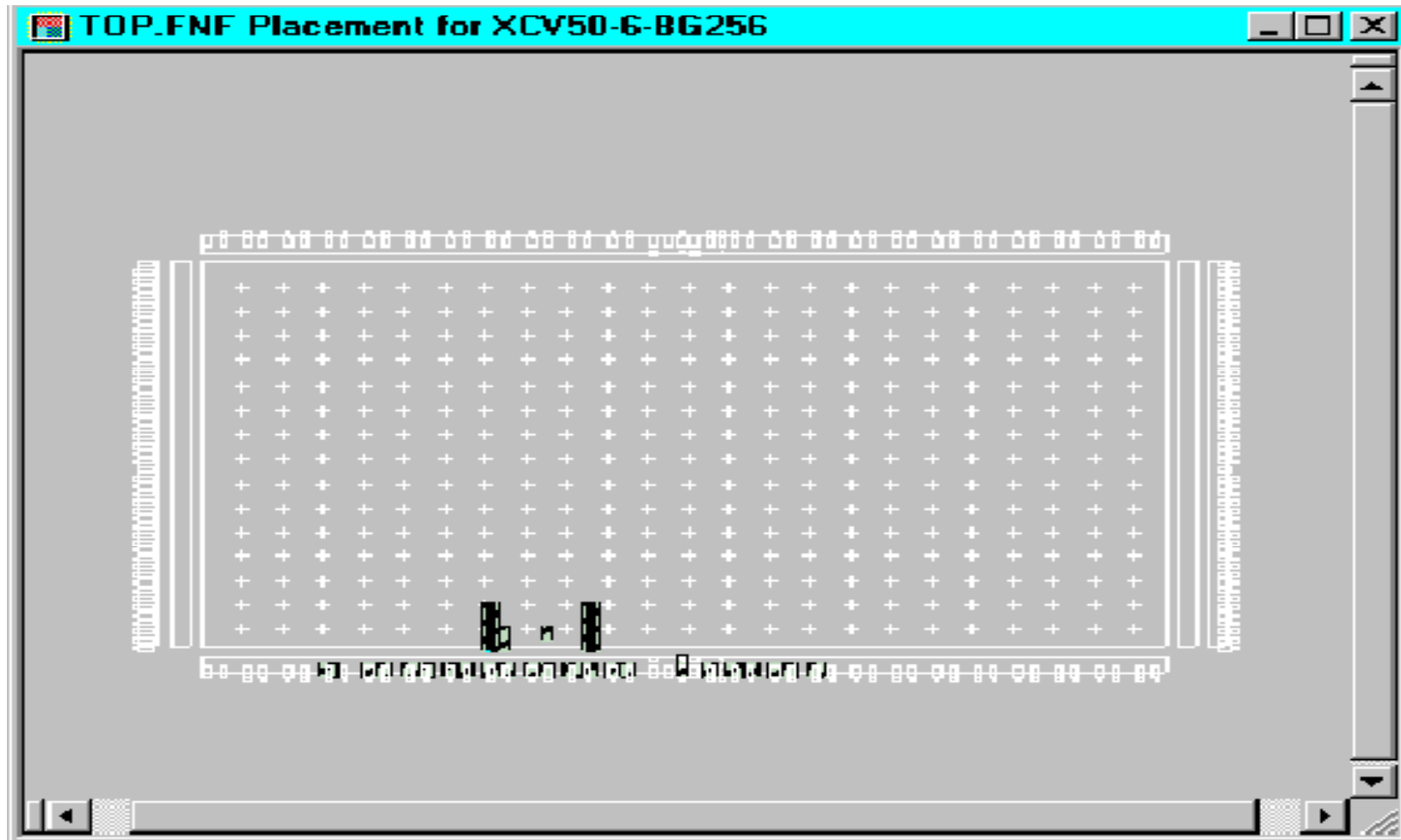
To view the implemented design results in a more meaningful way, you can display and zoom in on the input/output signals.

1. In the top.fnf Design Hierarchy window (View .Hierarchy), select (highlight) the top-level hierarchy, 'top (22 IOBs, 13 FGs, 8 CYS, 8 DFFs, 1 BUFG)', to show the signals in the Placement window.
2. Select View .Zoom .In or click the Zoom In icon.
3. Verify that all the I/Os are accounted for by holding the cursor over each of the pads and reading the pad name in the lower left corner of the Floorplanner window.

# Design Implementation

## □ Viewing the Design in Floorplanner

The placement in Floorplanner should look like the following.





# Generate PROM file

## ➤ Step1: Prepare Configuration File... (Generate PROM File)

- In “Generate Programming File” sub-menu, Run “PROM, ACE or JTAG File” option.

The screenshot displays the Xilinx ISE software interface for a project named 'ram\_block'. The 'Processes' window on the left shows the 'Generate Programming File' process as completed. A context menu is open over this process, with the 'Run' option selected. The 'FPGA Design Summary' window on the right provides a detailed overview of the project status, including project file, module name, target device, and product version. The 'Device Utilization Summary' table at the bottom right shows zero utilization for the logic.

**RAM\_BLOCK Project Status**

|                         |                |                       |                            |
|-------------------------|----------------|-----------------------|----------------------------|
| <b>Project File:</b>    | ram_block.isc  | <b>Current State:</b> | Programming File Generated |
| <b>Module Name:</b>     | ram_32x8       | <b>• Errors:</b>      | No Errors                  |
| <b>Target Device:</b>   | xc2s150-5pq208 | <b>• Warnings:</b>    | No Warnings                |
| <b>Product Version:</b> | ISE 8.2i       | <b>• Updated:</b>     | Fri Jul 13 13:24:43 2007   |

**RAM\_BLOCK Partition Summary**

No partition information was found.

**Device Utilization Summary**

| Logic Utilization                              | Used | Available | Utilization | Note(s) |
|--|------|-----------|-------------|---------|
| <b>Logic Distribution</b>                      |      |           |             |         |
| Number of Slices containing only related logic | 0    | 0         | 0%          |         |
| Number of Slices containing unrelated logic    | 0    | 0         | 0%          |         |

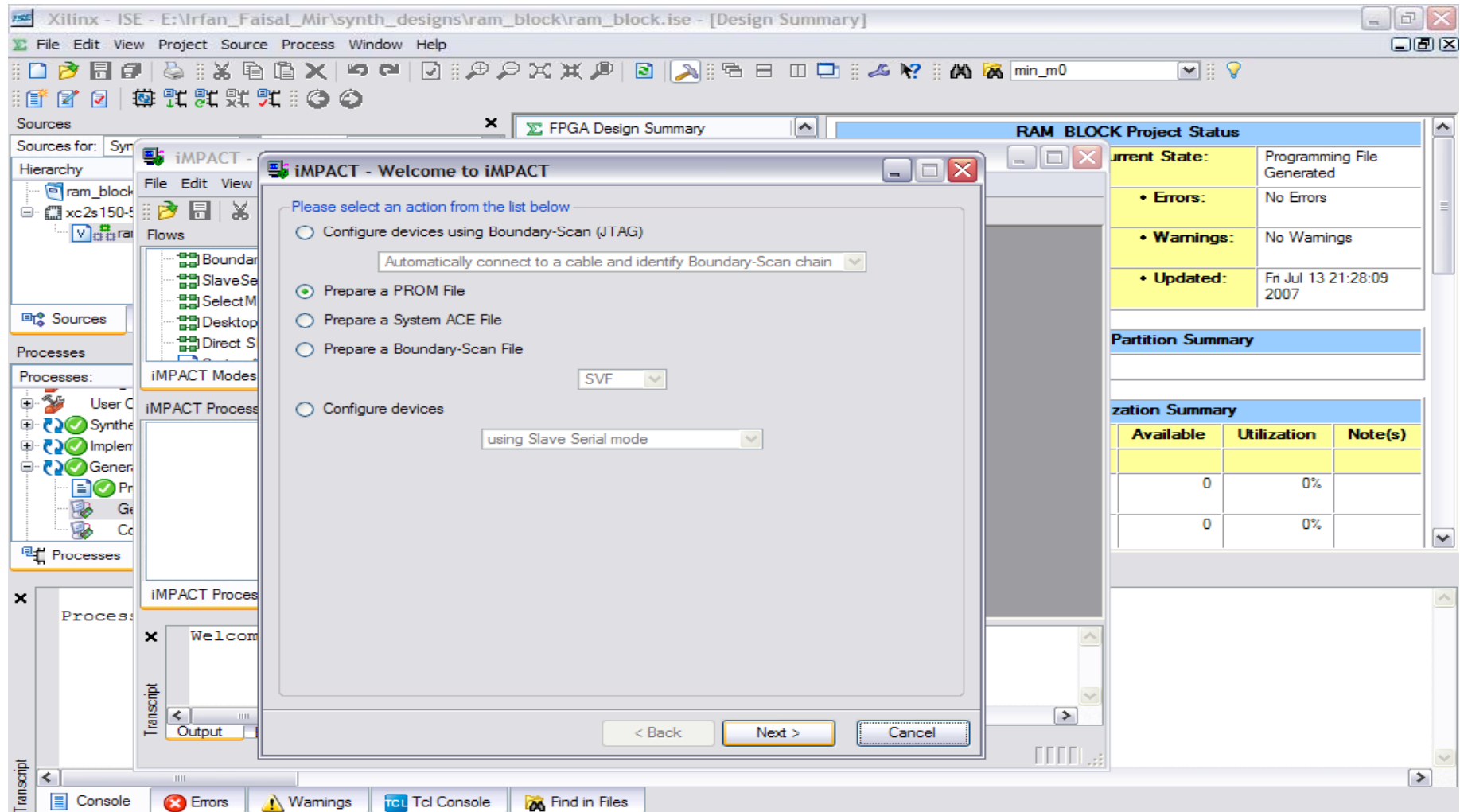
**Transcript**

```
Started : "Generate Programming File"
Process "Generate Programming File" completed successfully
```

# Generate PROM file

## ➤ Step1: Prepare Configuration File... (Generate PROM File)

- Select “Prepare a PROM File” option here and click on Next..





## Generate PROM file

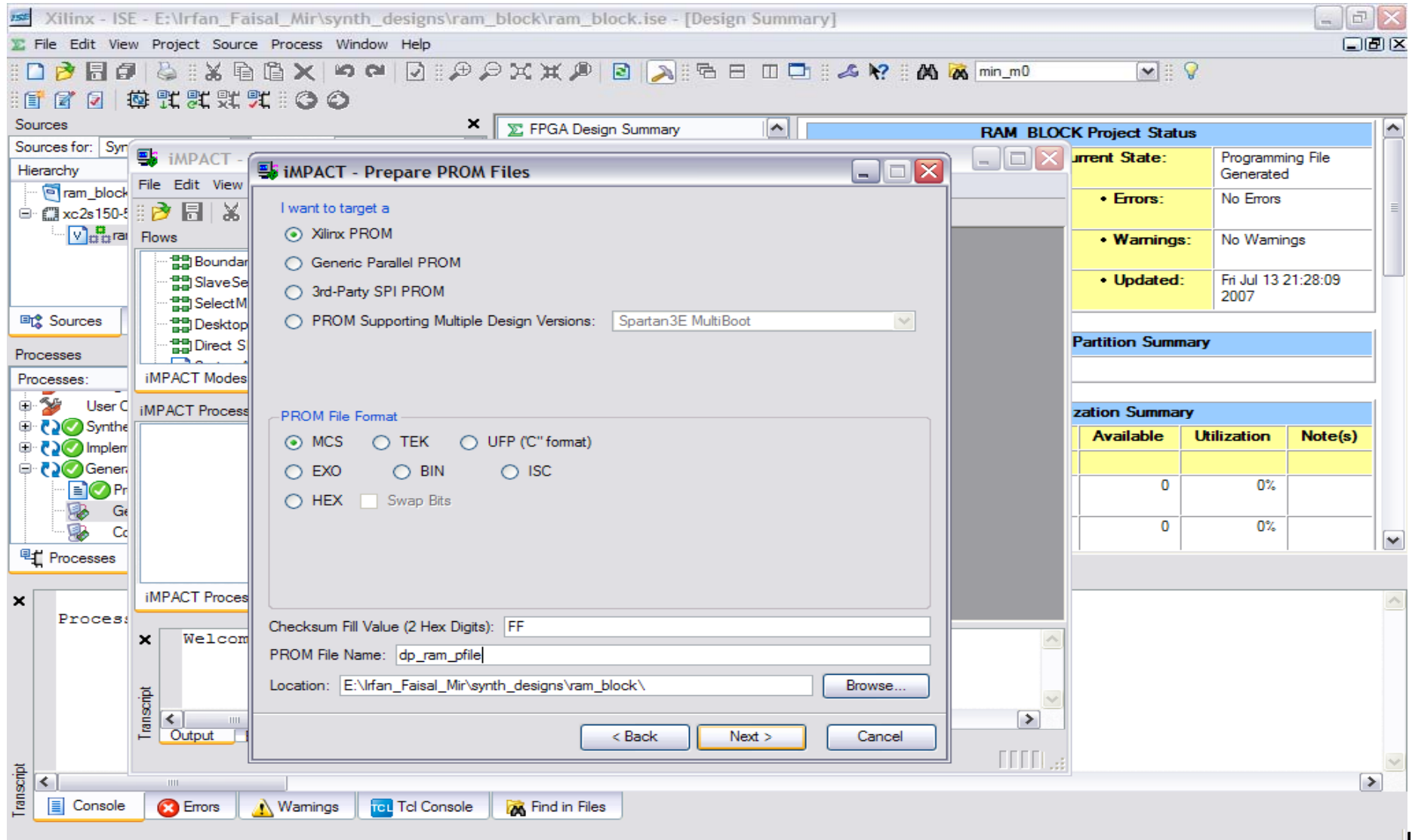
### ➤ **Step2: Prepare PROM File... (Generate PROM File)**

- PROM file is generated with *\*.mcs* extension.
- In PROM File Name give the name of the PROM file.
- In Location give the path where the PROM file should be created.
- Important point in generating a PROM file is to know the part number and
  - family of PROM used with FPGA.
  - The PROM used with FROM is xcf01s.
  - Select xcf as a PROM (FLASH).
  - Select the part number xcf01s as shown in the following dialog box and click Add.

See snapshot on next slide

# Generate PROM file

## ➤ Step2: Prepare PROM File... (Generate PROM File)



# Generate PROM file

## ➤ Step2: Prepare PROM File... (Generate PROM File)

The screenshot displays the Xilinx ISE environment. The main window is titled "Xilinx - ISE - E:\Irfan\_Faisal\_Mir\synth\_designs\ram\_block\ram\_block.ise - [Design Summary]". The "iMPACT - Specify Xilinx PROM Device" dialog is open, showing options for "Auto Select PROM", "Enable Revisioning", and "Enable Compression". The "Number of Revisions" is set to 1. The "Select a PROM" section shows "xcf" selected, with a list of "xcf01s" at position 0. The "Add" button is visible. The background shows the "RAM BLOCK Project Status" window with the following details:

| RAM BLOCK Project Status |                            |
|--------------------------|----------------------------|
| Current State:           | Programming File Generated |
| Errors:                  | No Errors                  |
| Warnings:                | No Warnings                |
| Updated:                 | Fri Jul 13 21:28:09 2007   |

Below the status window, there is a "Partition Summary" and a "Utilization Summary" table.

| Partition Summary |             |         |
|-------------------|-------------|---------|
| Available         | Utilization | Note(s) |
| 0                 | 0%          |         |
| 0                 | 0%          |         |

| Utilization Summary |             |         |
|---------------------|-------------|---------|
| Available           | Utilization | Note(s) |
| 0                   | 0%          |         |
| 0                   | 0%          |         |

# Generate PROM file

## ➤ Step2: Prepare PROM File... (Generate PROM File)

**iIMPACT - File Generation Summary**

You have entered following information:

|                 |              |
|-----------------|--------------|
| PROM Type:      | Serial       |
| File Format     | mcs          |
| Fill Value      | FF           |
| PROM filename   | dp_ram_pfile |
| Number of PROMs | 1            |

| Position | Part Name |
|----------|-----------|
| 0        | xcf01s    |

Click "Finish" to start adding device files.

< Back Finish Cancel

**RAM BLOCK Project Status**

**Current State:** Programming File Generated

- Errors:** No Errors
- Warnings:** No Warnings
- Updated:** Fri Jul 13 21:28:09 2007

**Partition Summary**

**Utilization Summary**

| Available | Utilization | Note(s) |
|-----------|-------------|---------|
| 0         | 0%          |         |
| 0         | 0%          |         |

# Generate PROM file

## ➤ Step2: Prepare PROM File... (Generate PROM File)

The screenshot displays the Xilinx ISE environment. The main window is titled "Xilinx - ISE - E:\Irfan\_Faisal\_Mir\synth\_designs\ram\_block\ram\_block.ise - [Design Summary]". The "FPGA Design Summary" window is open, showing the "RAM BLOCK Project Status" table:

| RAM BLOCK Project Status |                            |
|--------------------------|----------------------------|
| Current State:           | Programming File Generated |
| • Errors:                | No Errors                  |
| • Warnings:              | No Warnings                |
| • Updated:               | Fri Jul 13 21:28:09 2007   |

The "Add Device" dialog is open, showing the "Look in:" field set to "ram\_block". The file list includes:

- \_ngo
- \_xmsgs
- netgen
- output\_files
- tasks
- work
- xst
- ram\_32x8.bit

The "File name:" field is set to "ram\_32x8" and the "Files of type:" field is set to "FPGA Bit Files (\*.bit)".

The "PROM File Formatter" window is also visible, showing the "XILINX PROM" icon and the "xcf01s 0 % Full" status.

The "Transcript" window at the bottom shows the following commands:

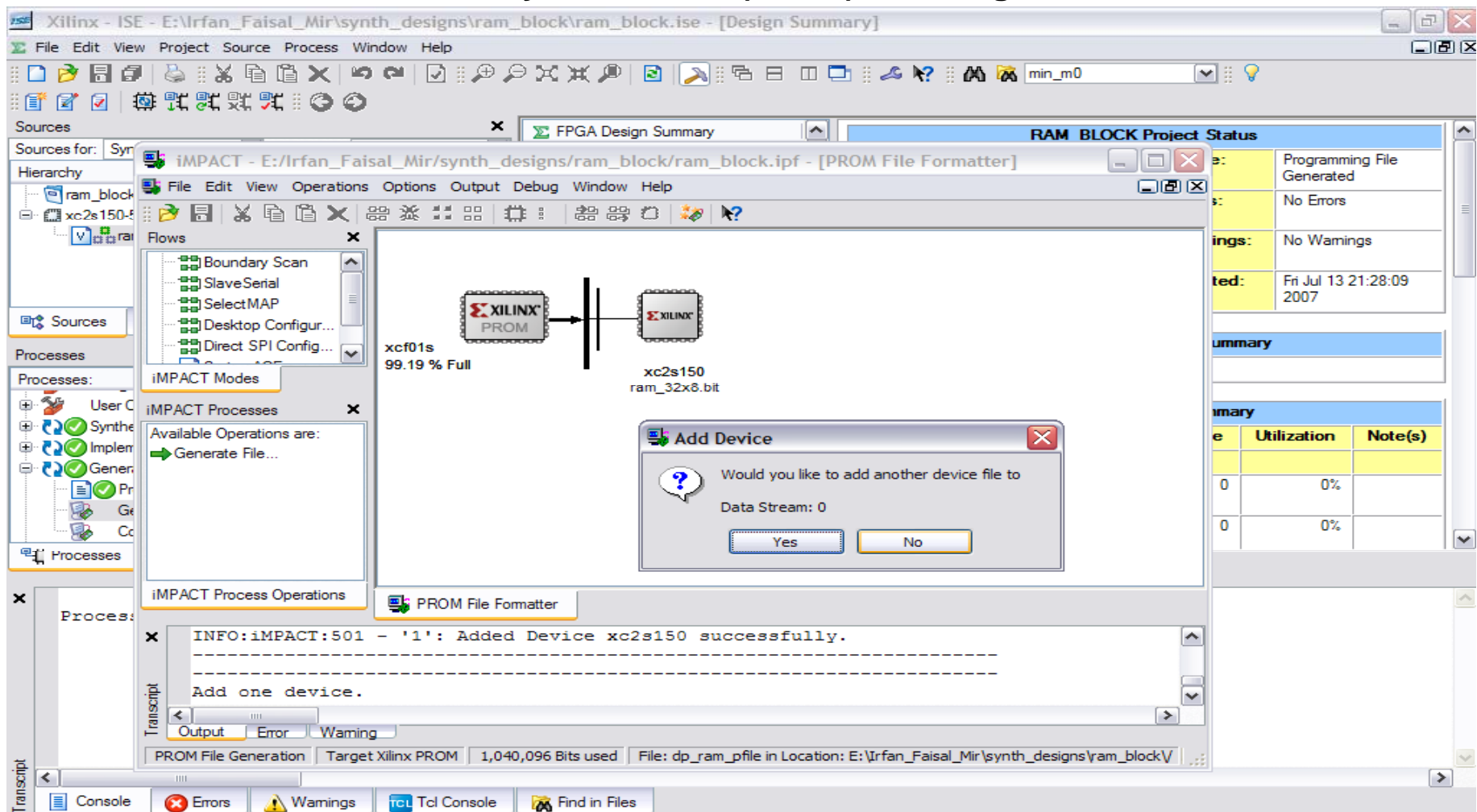
```
// *** BATCH CMD : setCurrentDesign  
// *** BATCH CMD : setCurrentDevice  
// *** BATCH CMD : setAttribute -c
```



# Generate PROM file

## ➤ Step3: PROM File Formatter... (Generate PROM File)

- FPGA is detected and is displayed along with its part number. Select No as we have only one device (FPGA) to configure.



The screenshot displays the Xilinx ISE environment. The main window is titled 'Xilinx - ISE - E:\Irfan\_Faisal\_Mir\synth\_designs\ram\_block\ram\_block.isc - [Design Summary]'. It shows a 'FPGA Design Summary' window with a diagram of the device configuration. The diagram shows a 'xc2s150' device connected to a 'xc2s150 ram\_32x8.bit' device. The 'xc2s150' device is labeled '99.19 % Full'. The 'FPGA Design Summary' window also shows a table of device utilization:

| Device  | Utilization | Note(s) |
|---------|-------------|---------|
| xc2s150 | 0%          |         |
| xc2s150 | 0%          |         |

The console window at the bottom shows the following message:

```
INFO:iMPACT:501 - '1': Added Device xc2s150 successfully.
```

The 'PROM File Formatter' dialog box is open, asking 'Would you like to add another device file to Data Stream: 0'. The 'No' button is highlighted.



# Generate PROM file

## ➤ Step4: PROM File Formatter... (Generate PROM File)

- Click on “Generate File” in iMPACT Processes to generate PROM file....
- The dialog box shows the successful generation of PROM file.

The screenshot shows the Xilinx ISE environment with the iMPACT window open. The iMPACT window displays a diagram of the PROM and the target device (xc2s150). A blue banner in the center reads "PROM File Generation Succeeded". The bottom status bar shows "PROM File Generation" and "Target Xilinx PROM".

The iMPACT window also shows the "Available Operations are:" list with "Generate File..." selected. The "IMPACT Process Operations" window shows the following text:

```
Writing file "E:\Irfan_Faisal_Mir\synth_designs\ram_block\//dp_ram_pfile.sig".
Total configuration bit size = 1040096 bits.Total configuration byte size = 130012 byt
// *** BATCH CMD : setCurrentDesign -version 0
```

The "RAM BLOCK Project Status" window shows the following information:

| Category                   | Value                    |
|----------------------------|--------------------------|
| Programming File Generated | Yes                      |
| No Errors                  | Yes                      |
| No Warnings                | Yes                      |
| Generated                  | Fri Jul 13 21:28:09 2007 |

The "Summary" table shows the following utilization:

| Category | Utilization | Note(s) |
|----------|-------------|---------|
| 0        | 0%          |         |
| 0        | 0%          |         |

# Configure Device

## ➤ Step1: Select Mode (Configure Device through iMPACT)

- Now Run the last step of “Generate Programming File” i.e. “configure device (iMPACT)” in project navigator window.

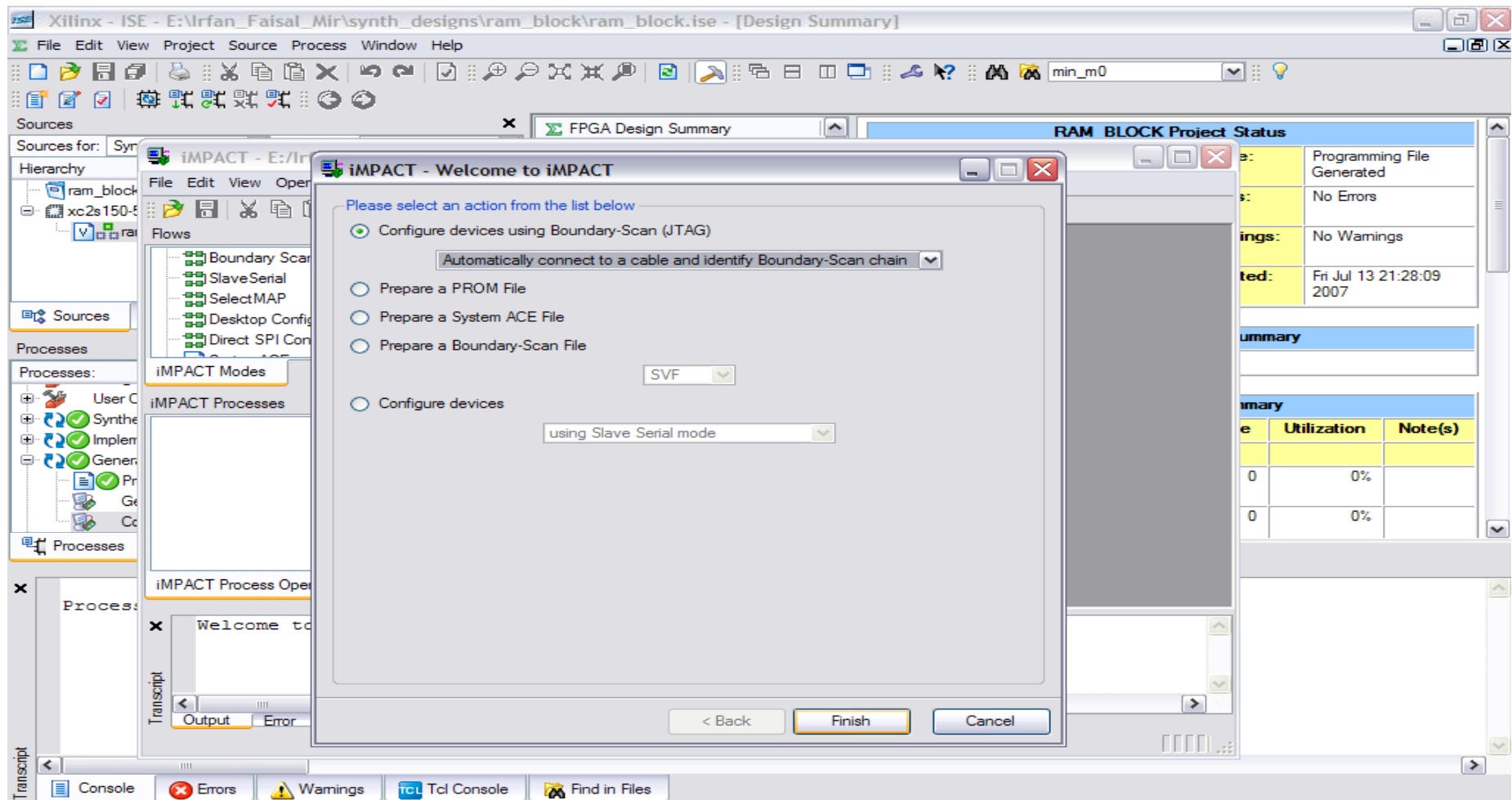
The screenshot shows the Xilinx ISE IDE interface. The title bar indicates the project is 'ram\_block.isc' in the 'E:\Irfan\_Faisal\_Mir\synth\_designs\ram\_block' directory. The 'Processes' window on the left shows a list of steps: User Constraints, Synthesize - XST, Implement Design, Generate Programming File, Programming File Generation Report, Generate PROM, ACE, or JTAG File, and Configure Device (iMPACT). The 'Configure Device (iMPACT)' step is highlighted, and a context menu is open over it with options: Run, Rerun, Rerun All, Stop, Open Without Updating, and Properties... The 'FPGA Design Summary' window in the center shows a tree view of reports including Summary, IOB Properties, Timing Constraints, Pinout Report, Clock Report, Errors and Warnings, Synthesis Messages, Translation Messages, Map Messages, and Place and Route Messages. The 'RAM\_BLOCK Project Status' window on the right displays project details: Project File (ram\_block.isc), Current State (Programming File Generated), Module Name (ram\_32x8), Errors (No Errors), Target Device (xc2s150-5pq208), Warnings (No Warnings), Product Version (ISE 8.2i), and Updated date (Fri Jul 13 21:28:09 2007). Below this is the 'RAM\_BLOCK Partition Summary' showing no partition information was found. At the bottom is the 'Device Utilization Summary' table.

| Device Utilization Summary                     |      |           |             |         |
|--|------|-----------|-------------|---------|
| Logic Utilization                              | Used | Available | Utilization | Note(s) |
| <b>Logic Distribution</b>                      |      |           |             |         |
| Number of Slices containing only related logic | 0    | 0         | 0%          |         |
| Number of Slices containing unrelated logic    | 0    | 0         | 0%          |         |

# Configure Device

## ➤ Step1: Select Mode (Configure Device through iMPACT)

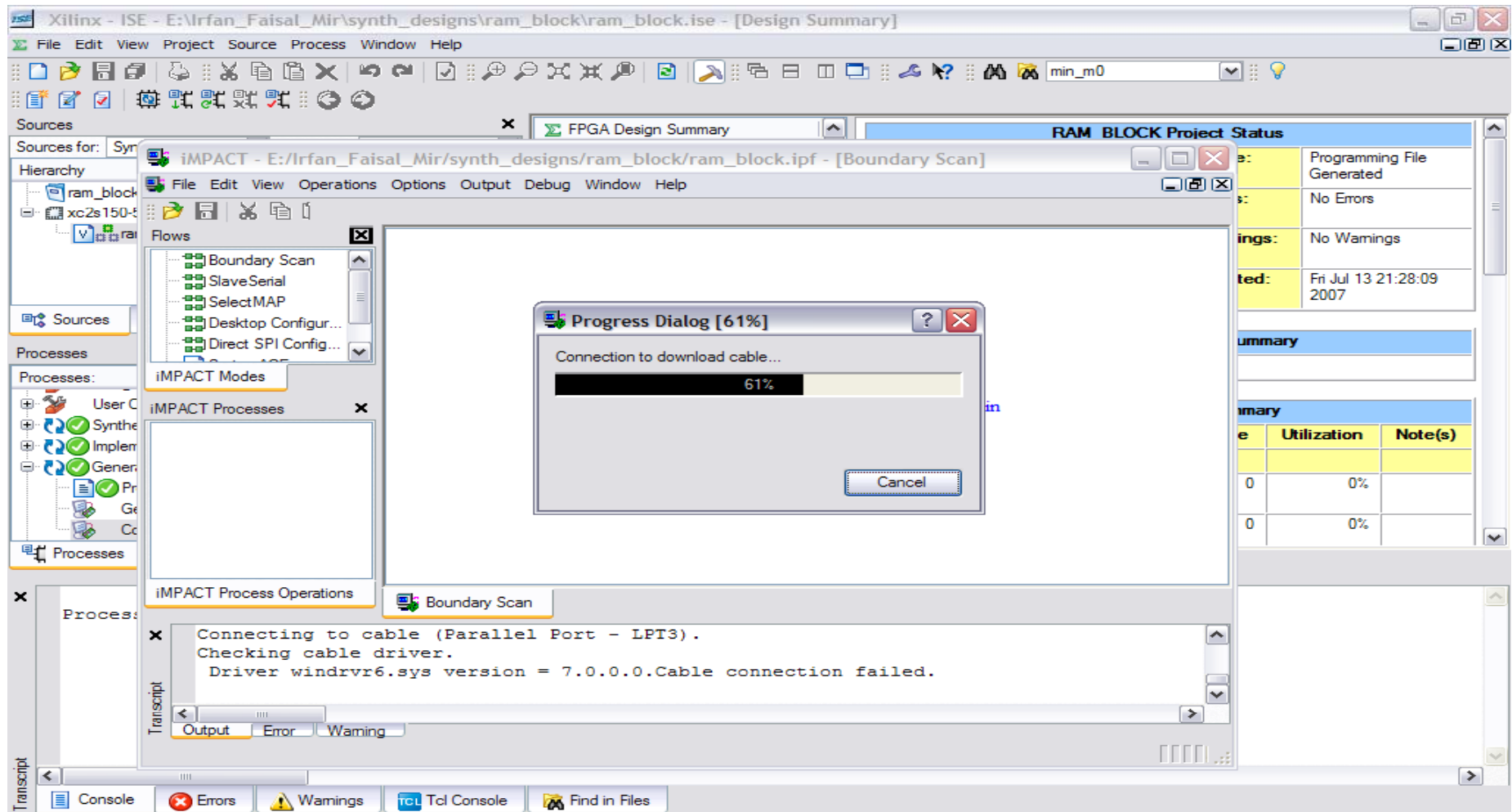
- Select the “Configure device using Boundary-Scan (JTAG)” option and click on finish..



# Configure Device

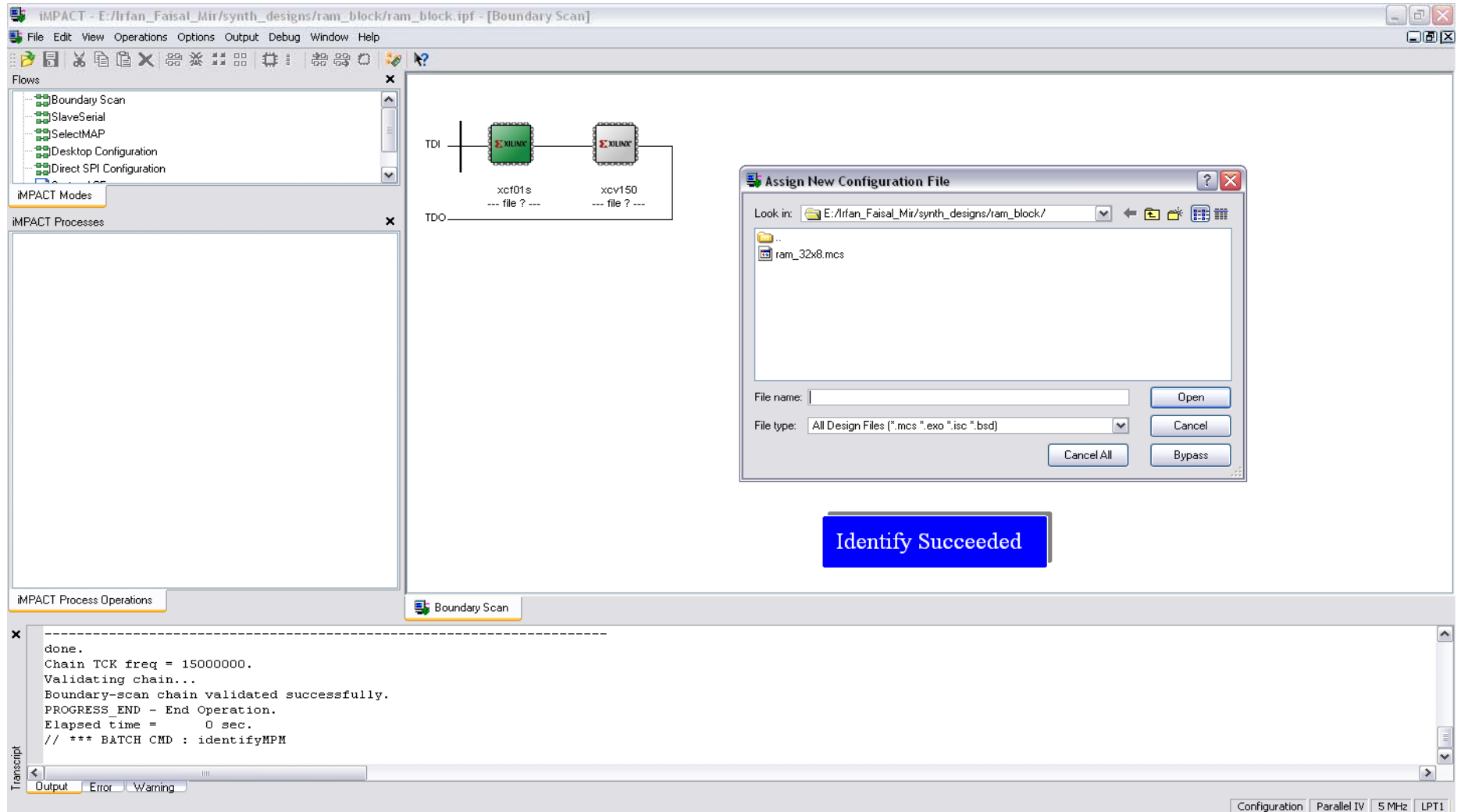
## ➤ Step2: Detect Cable (Configure Device through iMPACT)

- Click Next... It will automatically detect cable and identify Boundary-Scan chain



# Configure Device

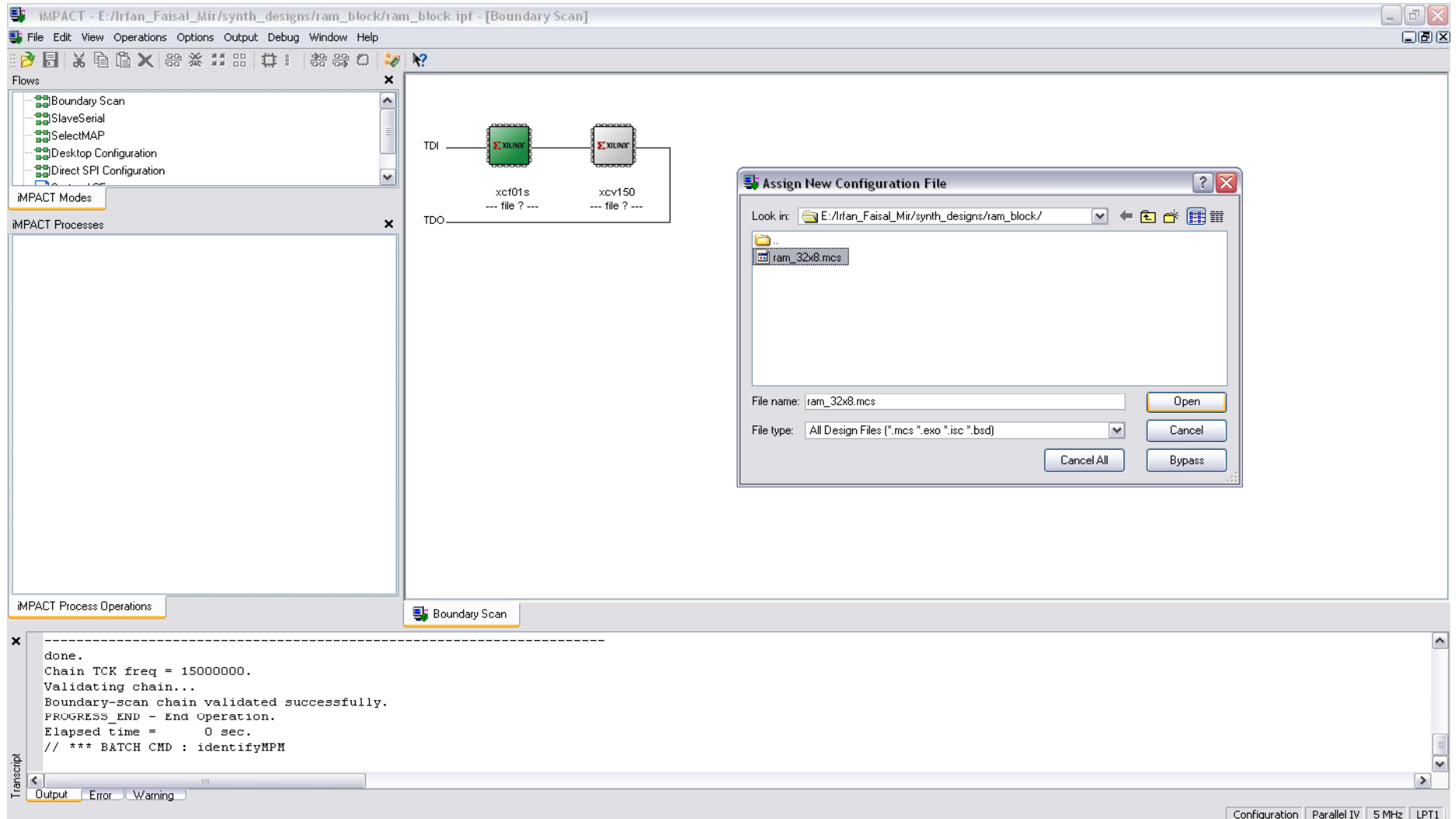
- **Step3: Devices detect in Boundary Scan Chain (Configure Device through iMPACT).. Two devices (PROM and FPGA) are appeared in window.**



# Configure Device

## ➤ Step4: Assign File to PROM only (Configure Device through iMPACT)

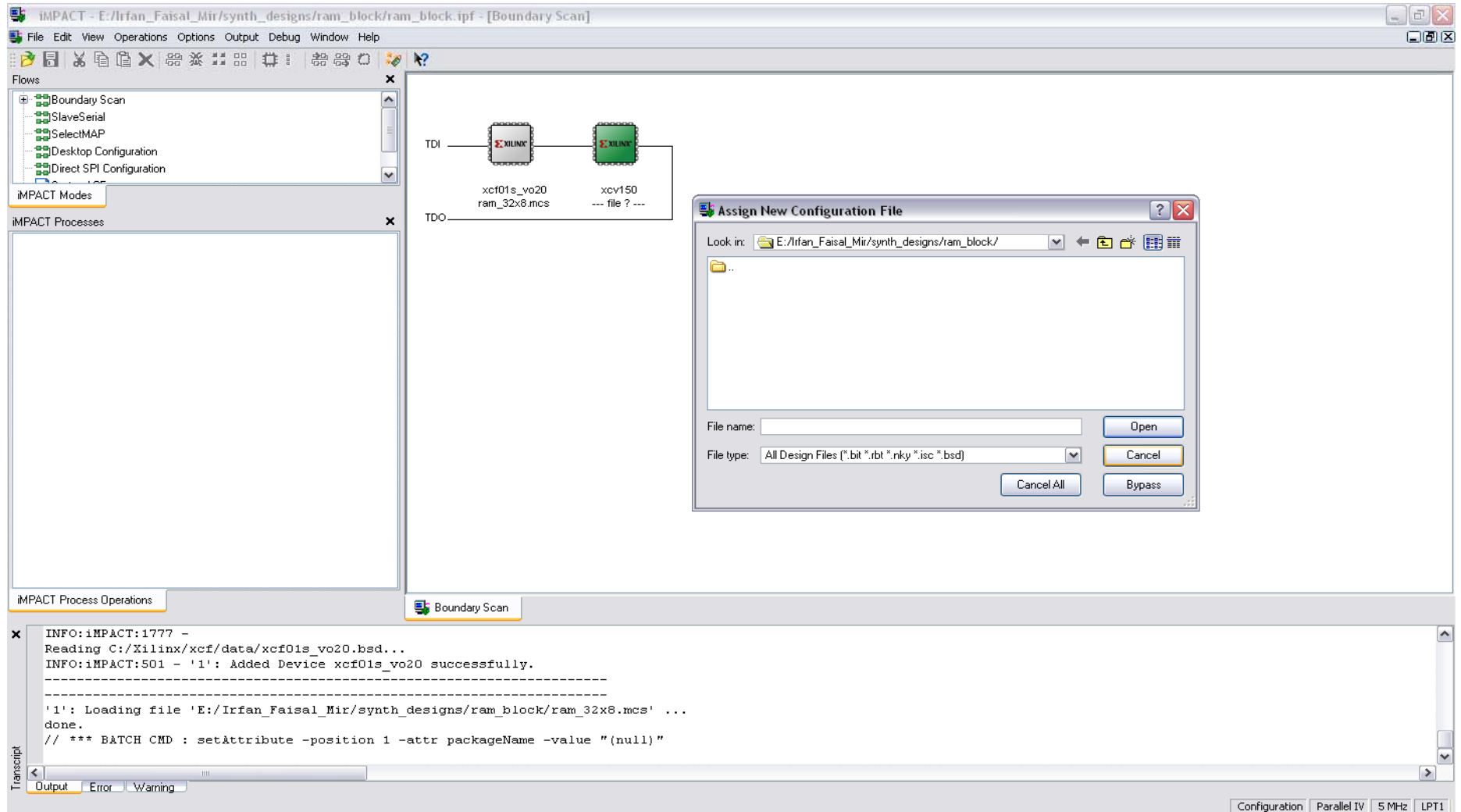
- Add \*.mcs file to PROM and DON'T need to assign \*.bit file to FPGA.



# Configure Device

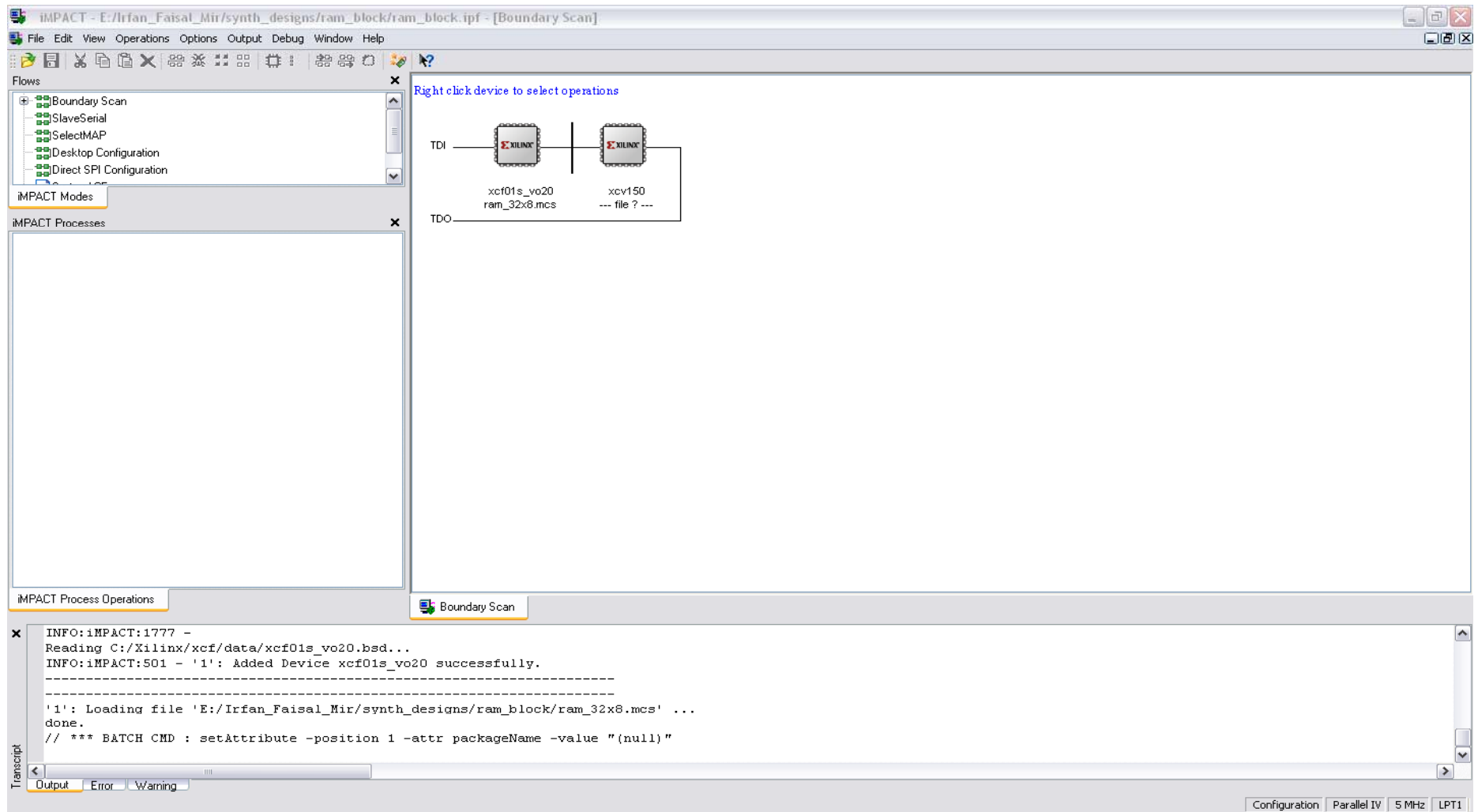
## ➤ Step4: Assign File to PROM only (Configure Device through iMPACT)

- Add \*.mcs file to PROM and DON'T need to assign \*.bit file to FPGA.



# Configure Device

- **Step4: Assign File to PROM only (Configure Device through iMPACT)**
  - Add \*.mcs file to PROM and DON'T need to assign \*.bit file to FPGA.

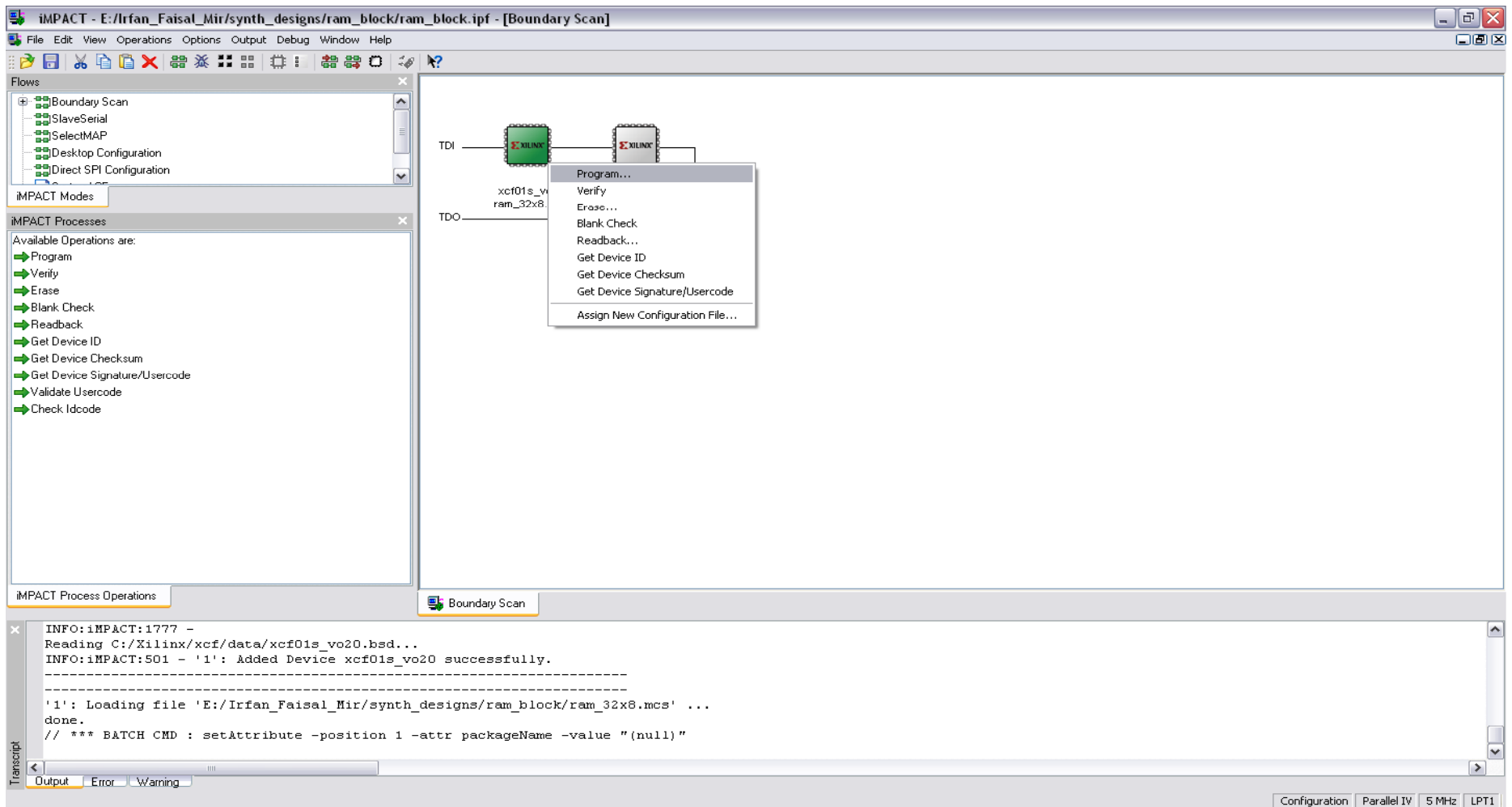




# Configure Device

## ➤ Step6: Program PROM (Configure Device through iMPACT)

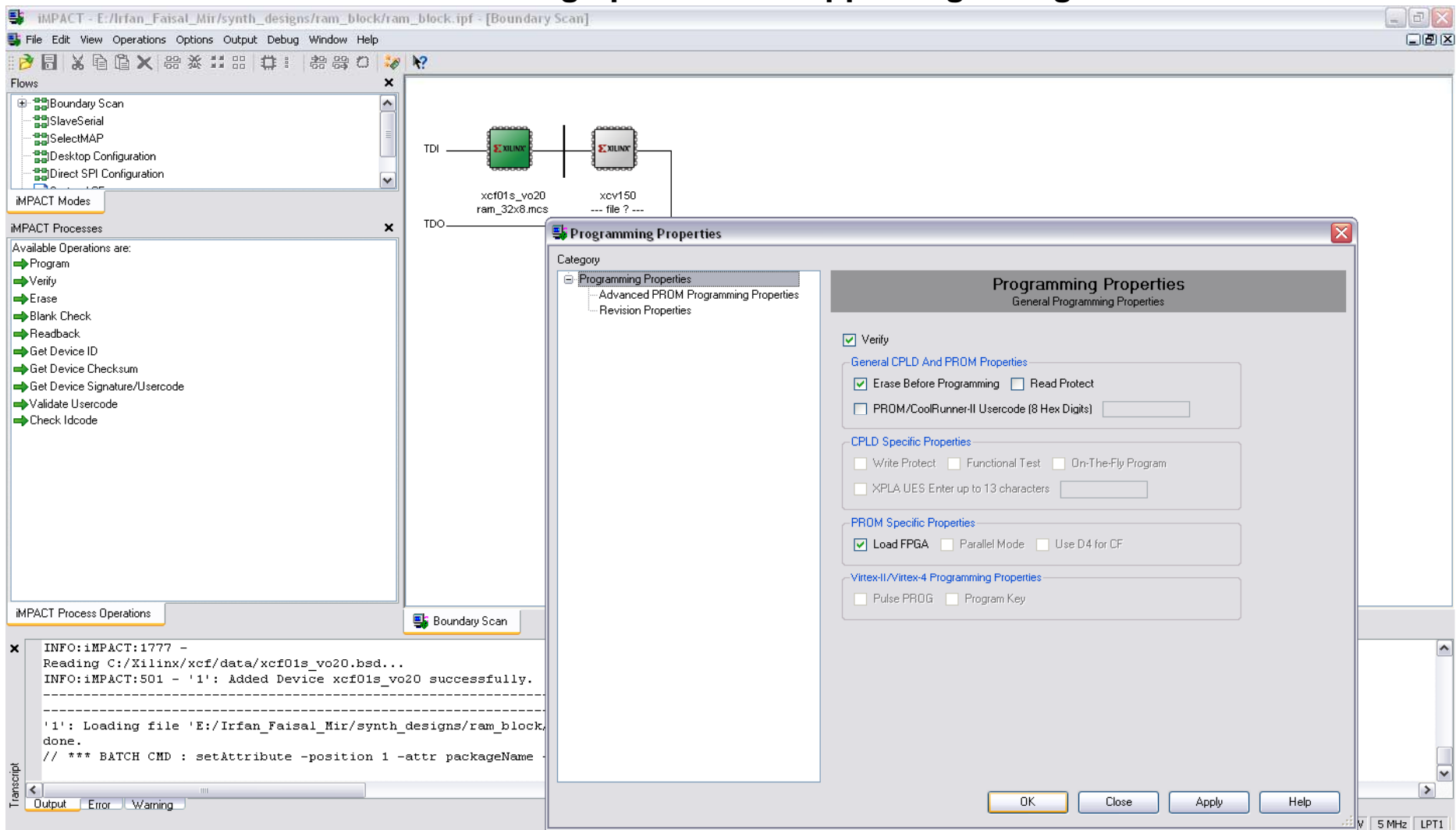
- Right click the PROM and click program.
- Click the following options in an appearing dialog box.



# Configure Device

## ➤ Step6: Program PROM (Configure Device through iMPACT)

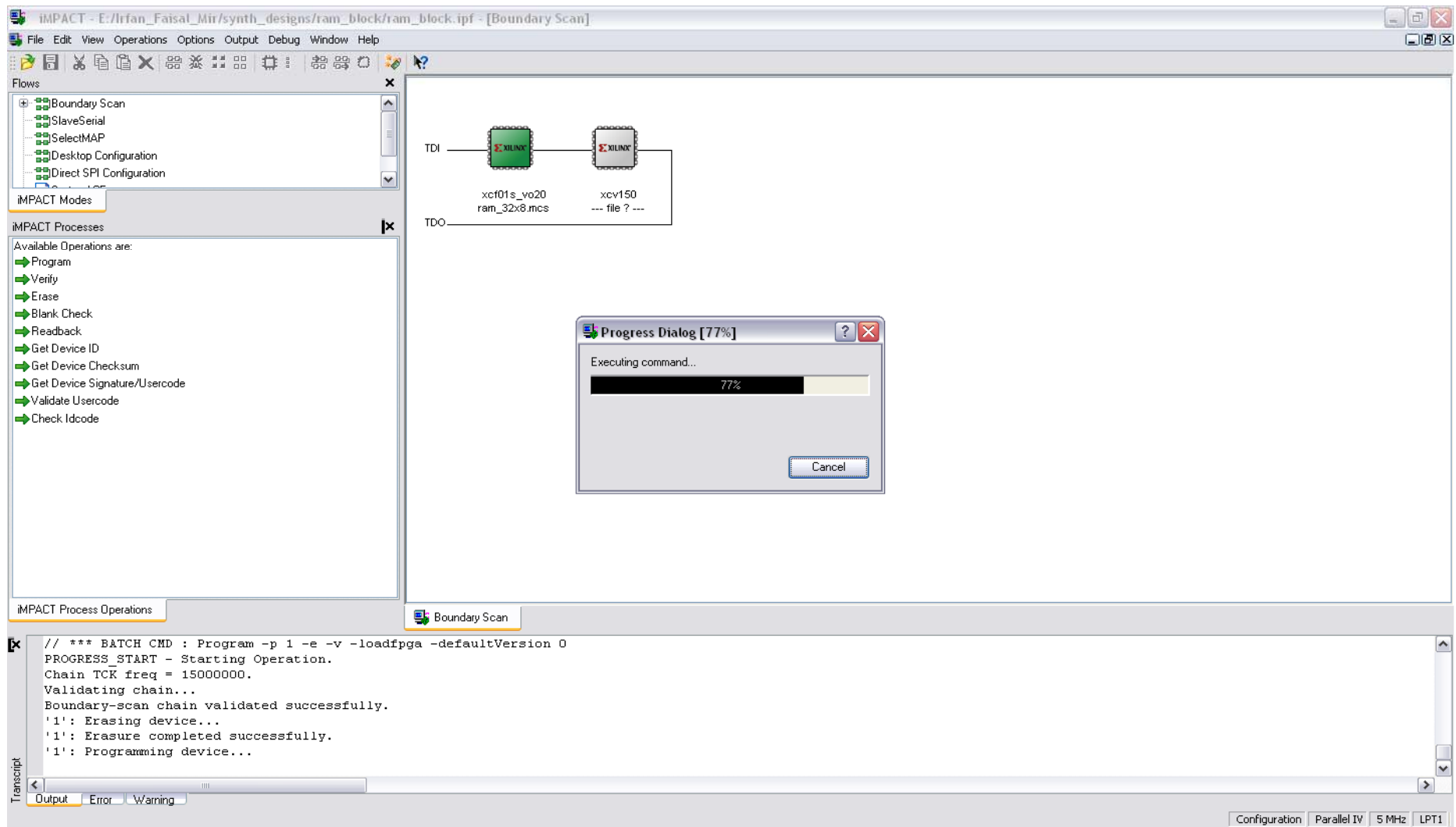
- Click the following options in an appearing dialog box.



# Configure Device

## ➤ Step6: Program PROM (Configure Device through iMPACT)

- Program Flash PROM process is going on...



# Configure Device

## ➤ Step6: Program PROM (Configure Device through iMPACT)

- The PROM is programmed successfully. The PROM will configure the FPGA automatically.

