Training Course
on

# FPGA based Digital Design using Verilog HDL


By

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**** Organized by*** **Skill Development Council,**
***( Ministry of Labour, Manpower and overseas Pakistani )***
**Govt. of Pakistan.**

# Design Implementation

## ❑ Running Implement Design

**The Implement Design process converts the logical design represented in that source (and all sources in the hierarchy from that source down) into a physical file format that can be implemented in the selected target device.**

**First, run all processes (Synthesis through Place & Route) associated with the your design files. To do so, run Implement Design on the HDL files:**

1. **Select top (top.v) in the Sources in Project window.**

# Design Implementation

## ❑ Running Implement Design

**2. Double-click Implement Design in the Processes for Source “top” window.**

**This runs all processes.**

**NOTE: A check mark in the Processes for Source window denotes a process that was run successfully. An exclamation mark indicates that the process was run and that there is a warning for the process. More information about warnings can be obtained in the Transcript window.**

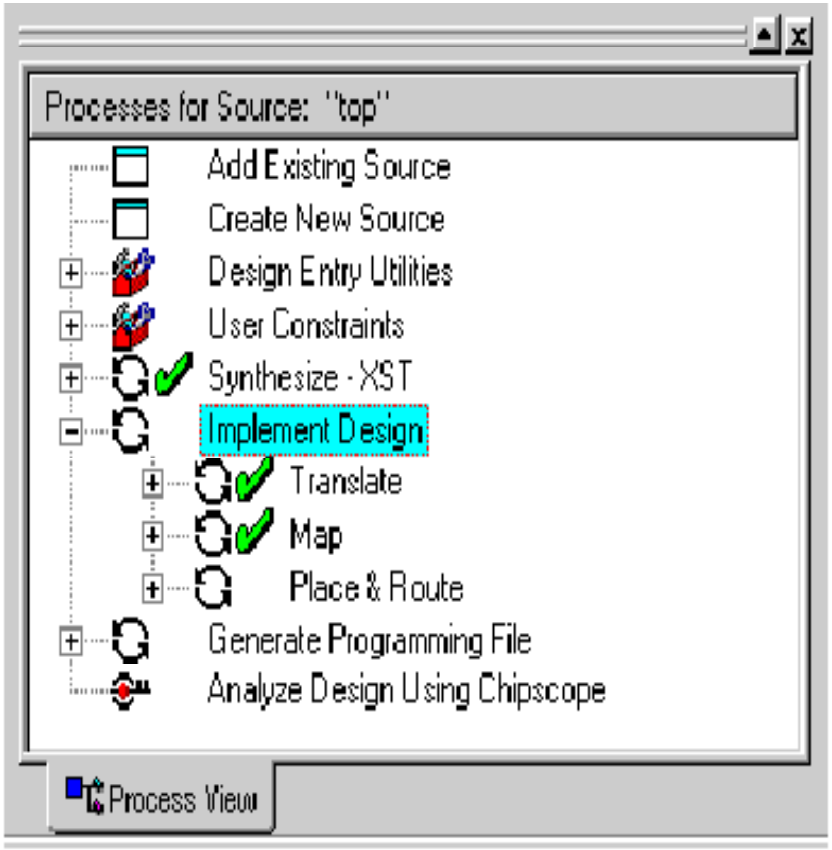



*Figure : Implement Design processes*

# Design Implementation

## ❑ Implementation sub-processes

- The **Translate process** merges all of the input netlists and design constraint information and outputs a Xilinx NGD (Native Generic Database) file. The output NGD file can then be mapped to the targeted device family.

- The **Map process** first performs a logical DRC (Design Rule Check) on the design in the NGD file produced by the Translate process. Map then maps the logic to the components (logic cells, I/O cells, and other components) in the target Xilinx FPGA. The output design is an NCD (Native Circuit Description) file physically representing the design

# Design Implementation

## ❑ Implementation sub-processes – contd'

mapped to the components in the Xilinx FPGA. The NCD file can then be placed and routed.

- The **Place and Route process** (PAR) takes a mapped NCD file, places and routes the design, and produces an NCD file to be used by the programming file generator (BitGen).

# Design Implementation

## ❑ Viewing the Design in Floorplanner

**Now, you can view the implemented design in Floorplanner. The Floorplanner is a graphical tool in which you can view and change the design hierarchy, floorplan, and perform design rule checks.**

1. **In Project Navigator, select top (top.v) in the Sources in Project window.**
2. **In the Processes for Source window, click the + sign beside Implement Design and the + sign beside Place & Route.**
3. **Double-click View/Edit Placed Design (Floorplanner)**

**The Floorplanner tool is launched and displays the placement of the design for the project.**

# Design Implementation

## ❑ Viewing the Design in Floorplanner

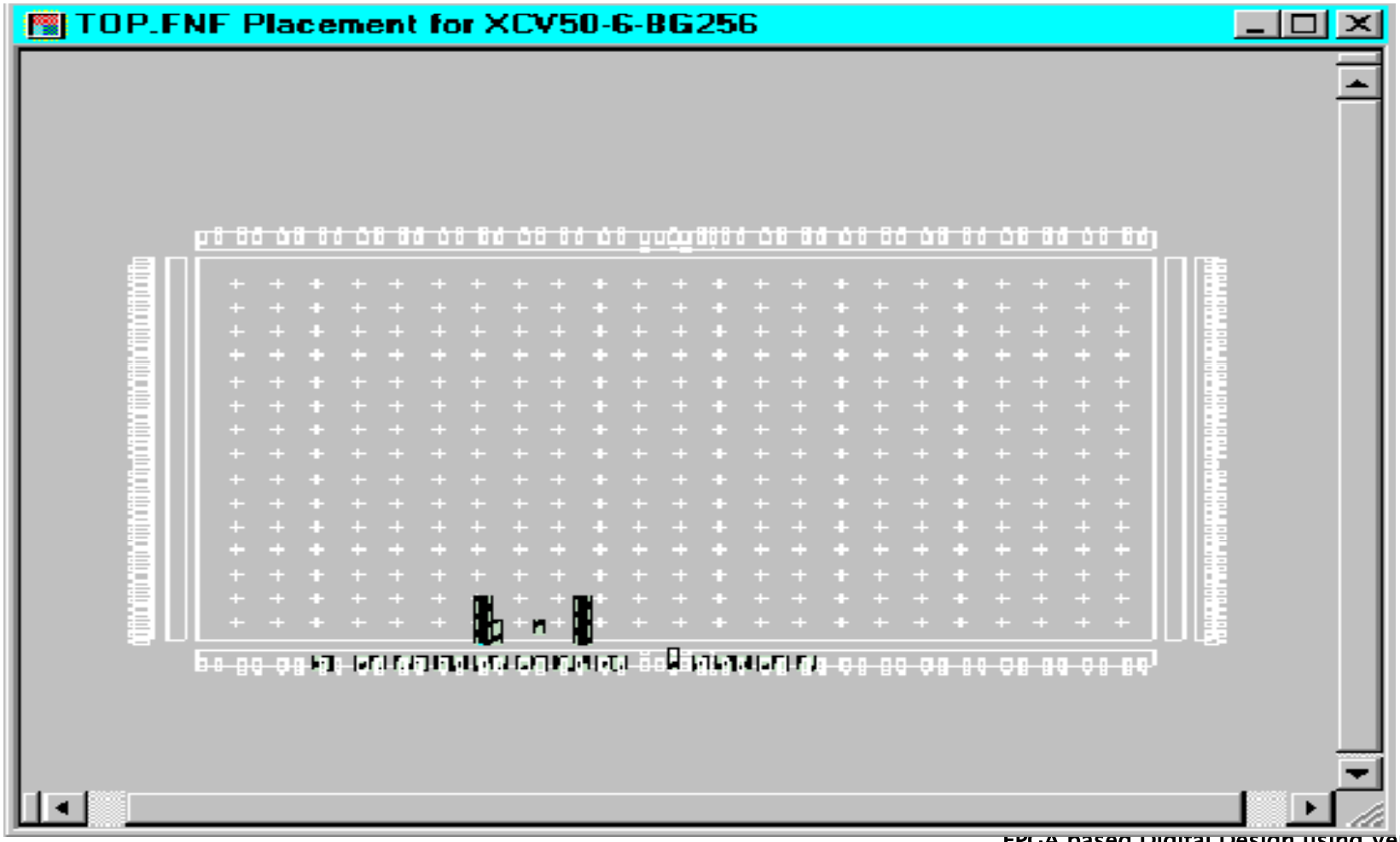
**To view the implemented design results in a more meaningful way, you can display and zoom in on the input/output signals.**

1. **In the top.fnf Design Hierarchy window (View .Hierarchy), select (highlight) the top-level hierarchy, 'top (22 IOBs, 13 FGs, 8 CYS, 8 DFFs, 1 BUFG)', to show the signals in the Placement window.**
2. **Select View .Zoom .In or click the Zoom In icon.**
3. **Verify that all the I/Os are accounted for by holding the cursor over each of the pads and reading the pad name in the lower left corner of the Floorplanner window.**

# Design Implementation

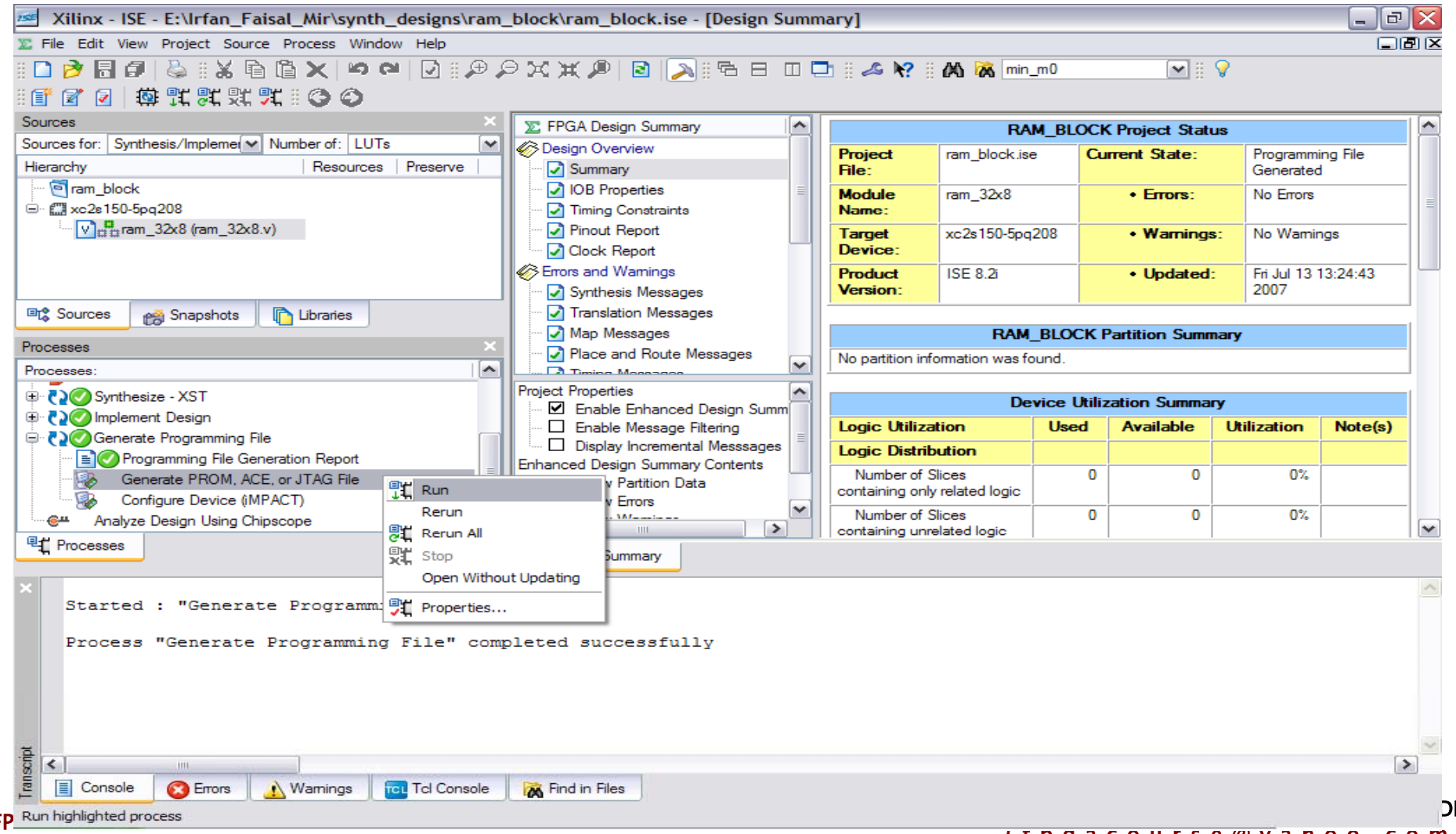
## ❑ Viewing the Design in Floorplanner

**The placement in Floorplanner should look like the following.**



# Generate PROM file

- **Step1: Prepare Configuration File… (Generate PROM File)**
  - **In “Generate Programming File” sub-menu, Run “PROM, ACE or JTAG File” option.**





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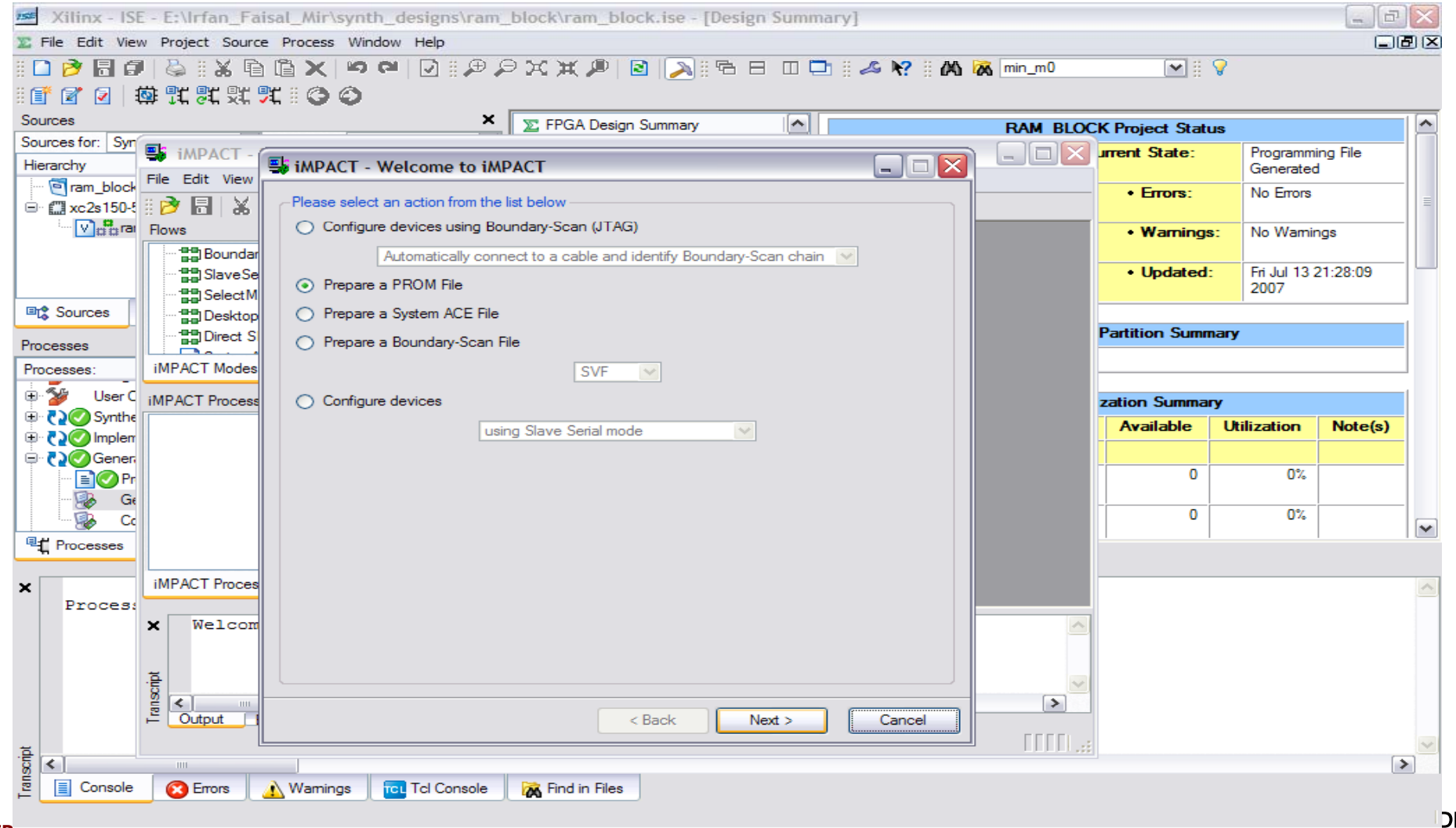
# Generate PROM file

- **Step1: Prepare Configuration File… (Generate PROM File)**
  - **Select “Prepare a PROM File” option here and click on Next..**



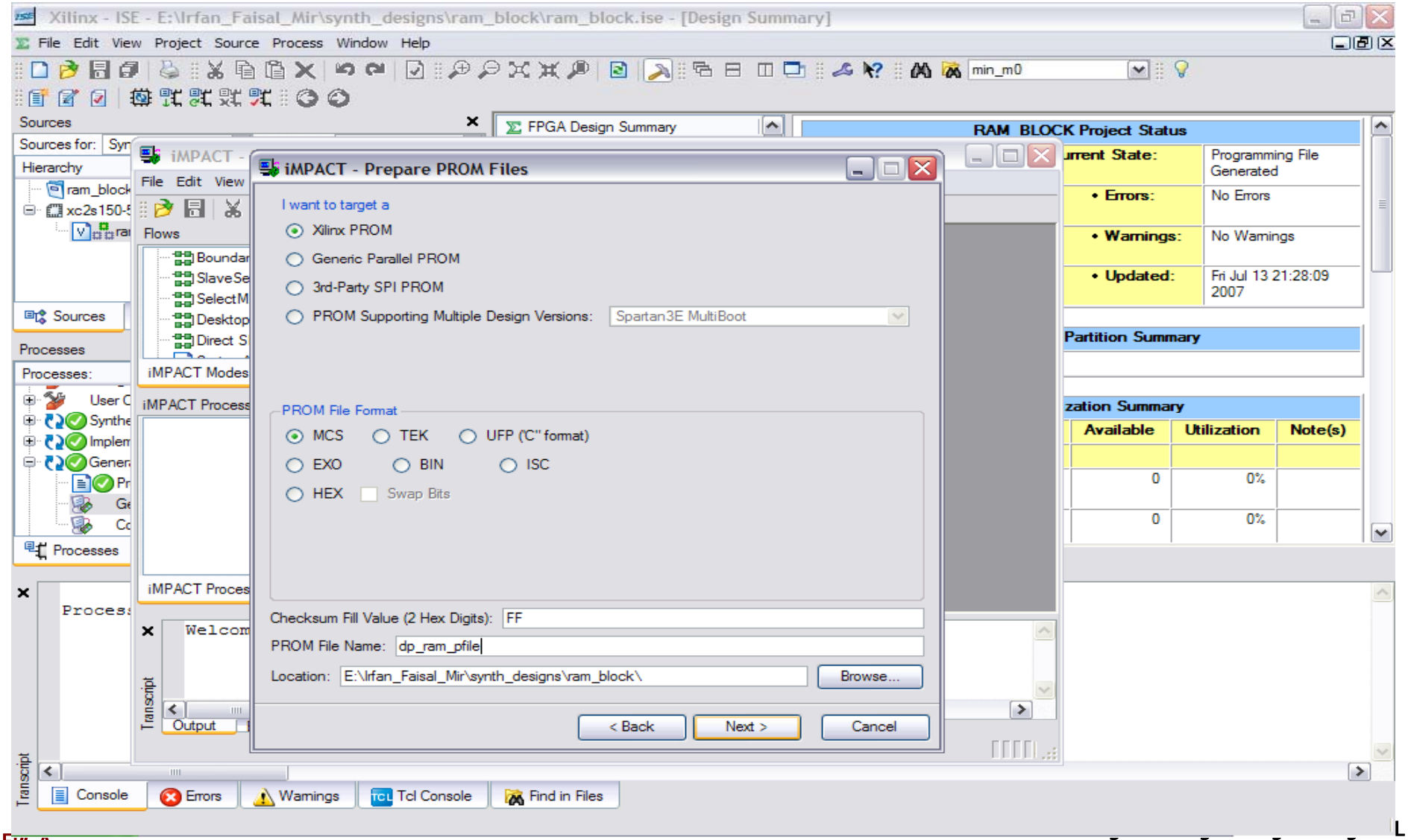
# Generate PROM file

- **Step2: Prepare PROM File… (Generate PROM File)**
  - **PROM file is generated with *.*mcs* extension.**
  - **In PROM File Name give the name of the PROM file.**
  - **In Location give the path where the PROM file should be created.**
  - **Important point in generating a PROM file is to know the part number and**
  - **family of PROM used with FPGA.**
  - **The PROM used with FROM is xcf01s.**
  - **Select xcf as a PROM (FLASH).**
  - **Select the part number xcf01s as shown in the following dialog box and click Add.**

**See snapshot on next slide**

# Generate PROM file

- **Step2: Prepare PROM File… (Generate PROM File)**





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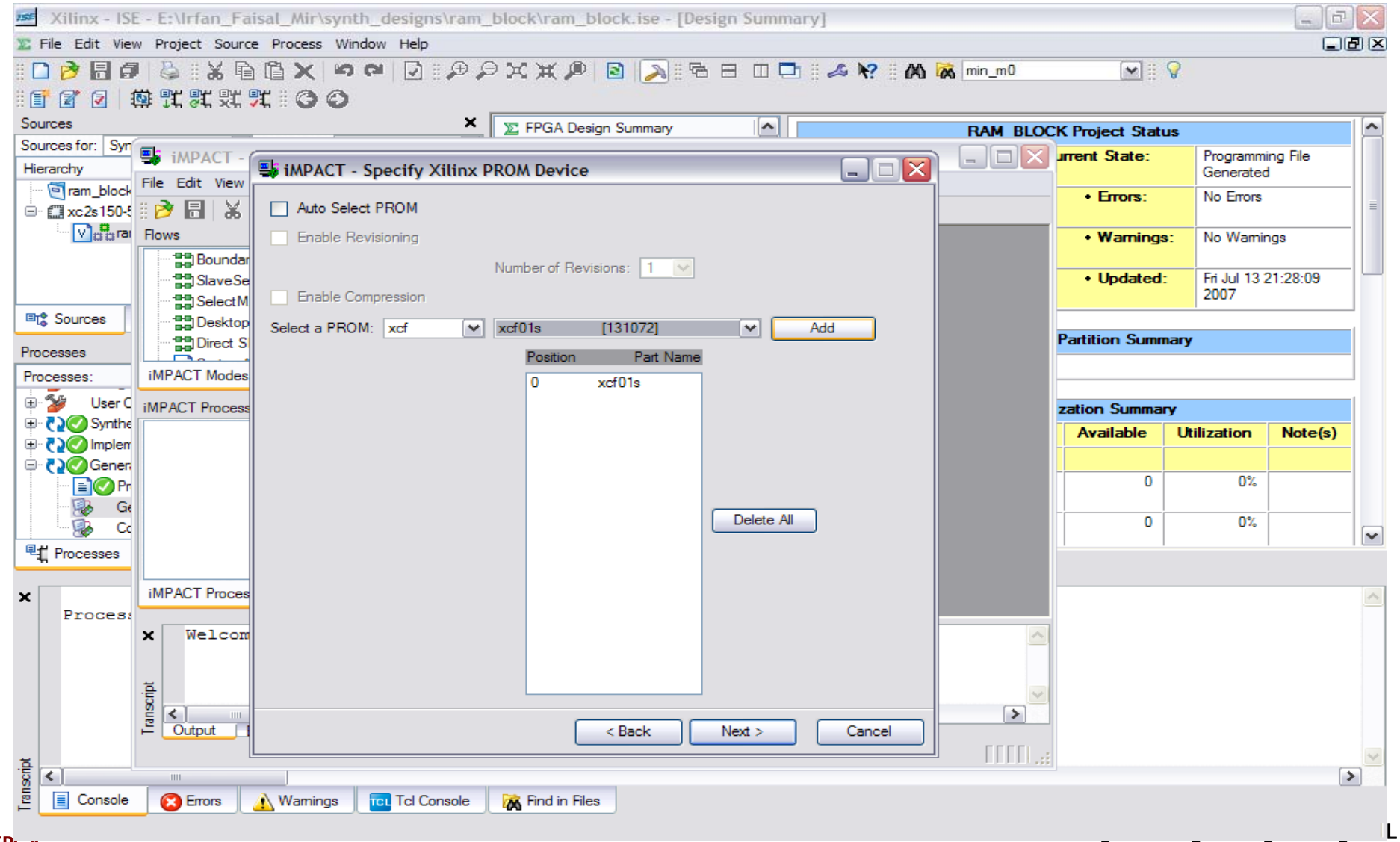
# Generate PROM file

- **Step2: Prepare PROM File… (Generate PROM File)**





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# Generate PROM file

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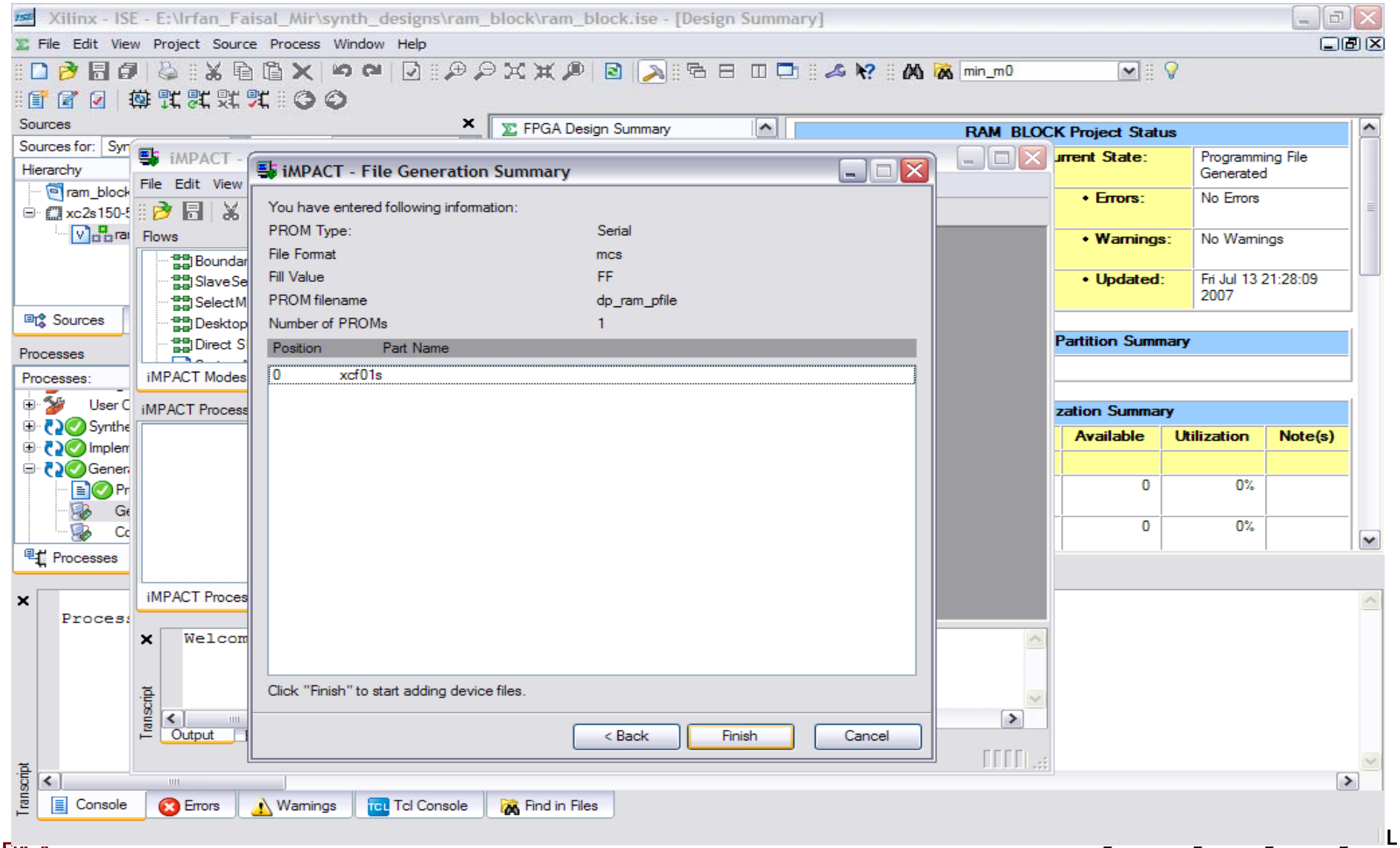



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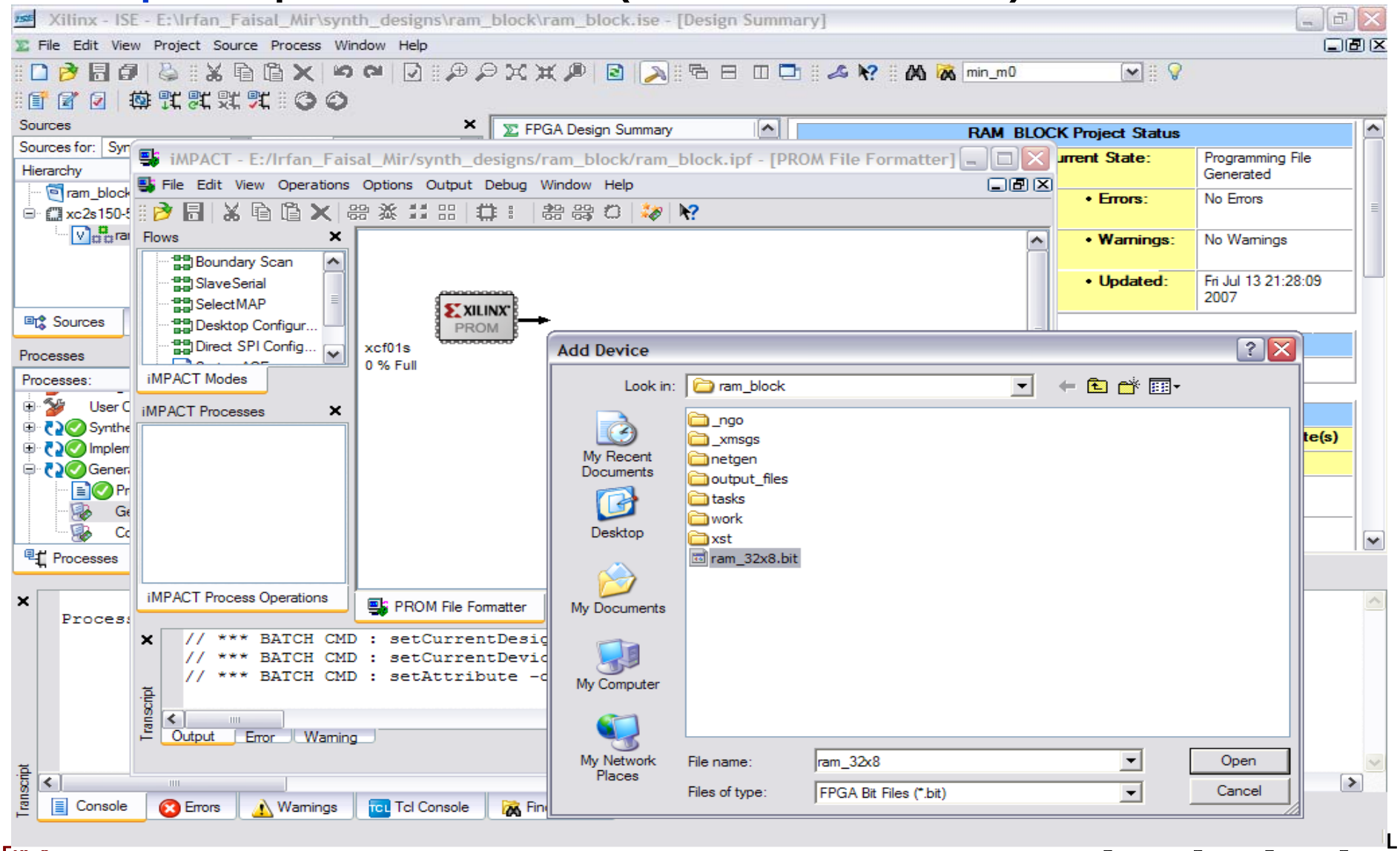
# Generate PROM file

- **Step2: Prepare PROM File… (Generate PROM File)**





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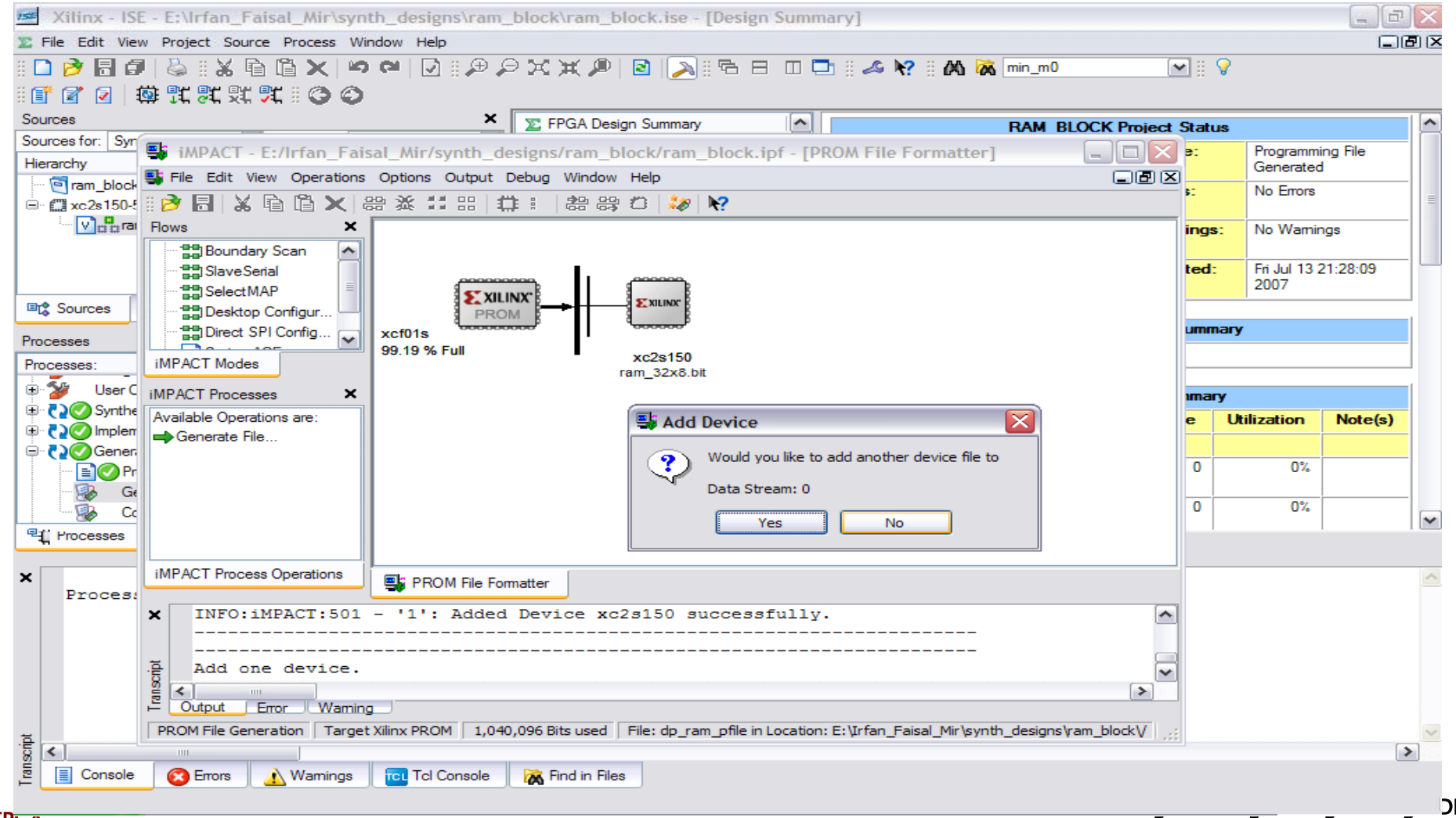
# Generate PROM file

- **Step3: PROM File Formatter… (Generate PROM File)**
  - **FPGA is detected and is displayed along with its part number. Select No as we have only one device (FPGA) to configure.**





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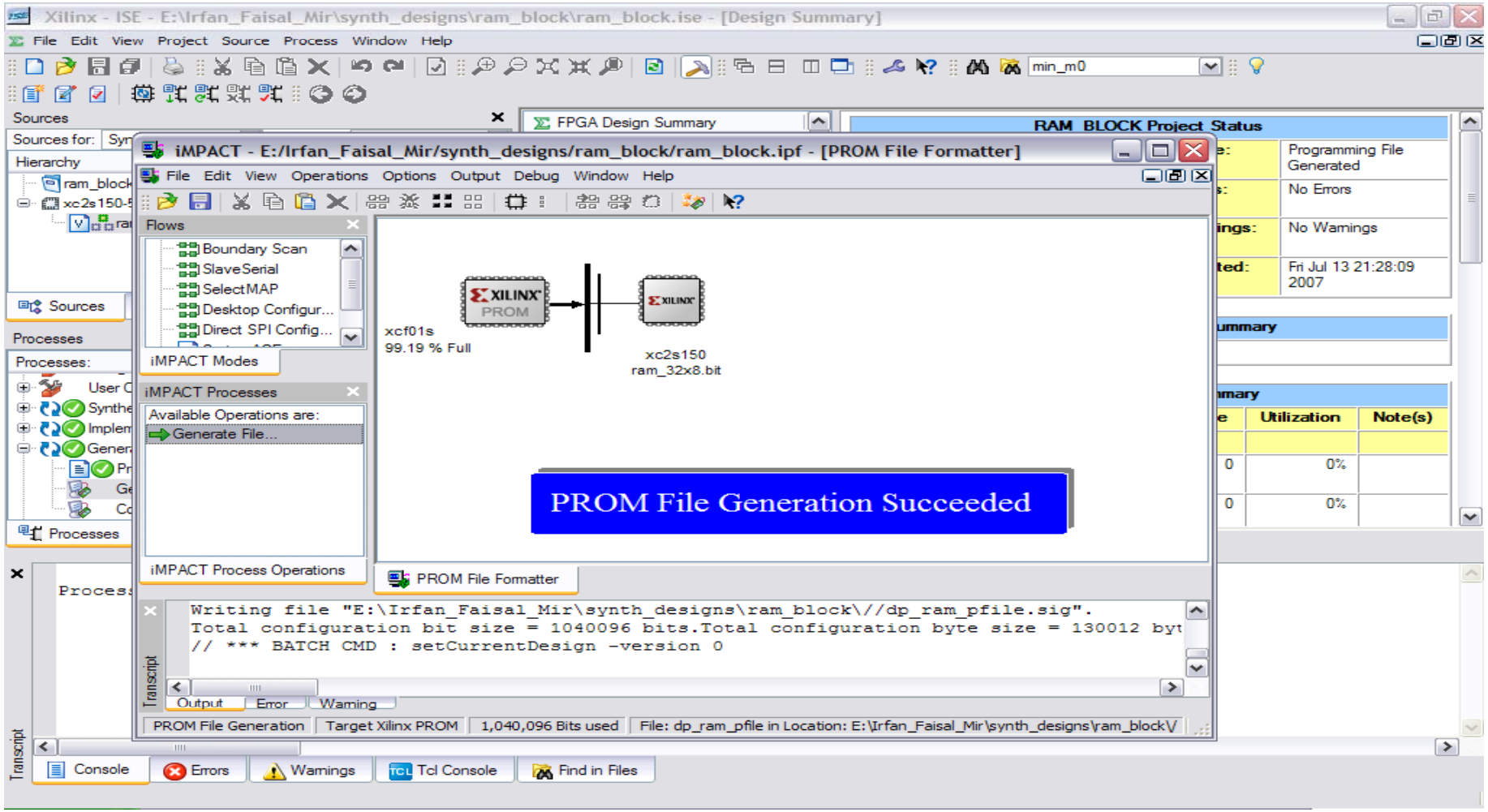
# Generate PROM file

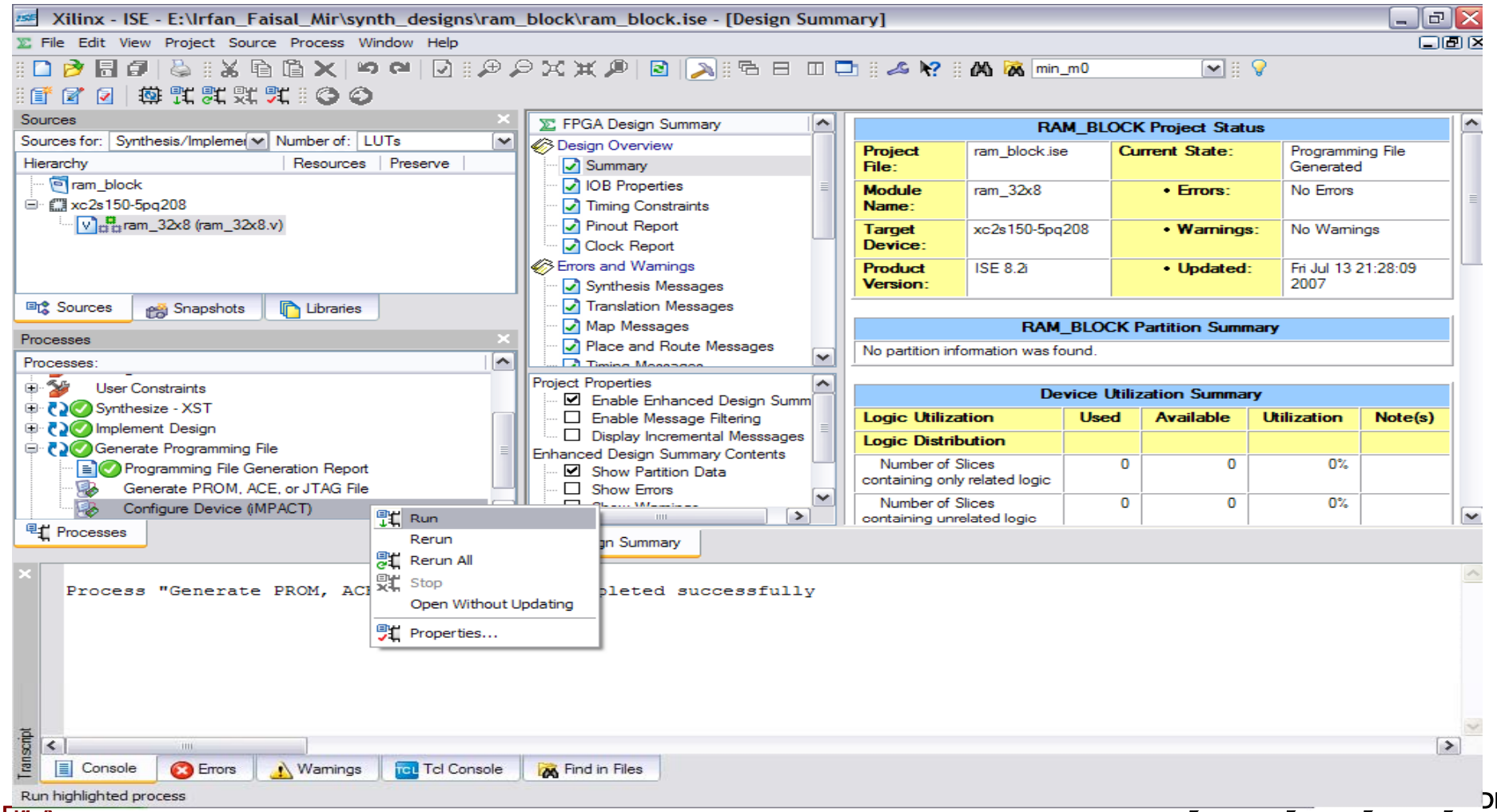
## ➢ Step4: PROM File Formatter… (Generate PROM File)

- Click on “Generate File” in iMPACT Processes to generate PROM file….
- The dialog box shows the successful generation of PROM file.



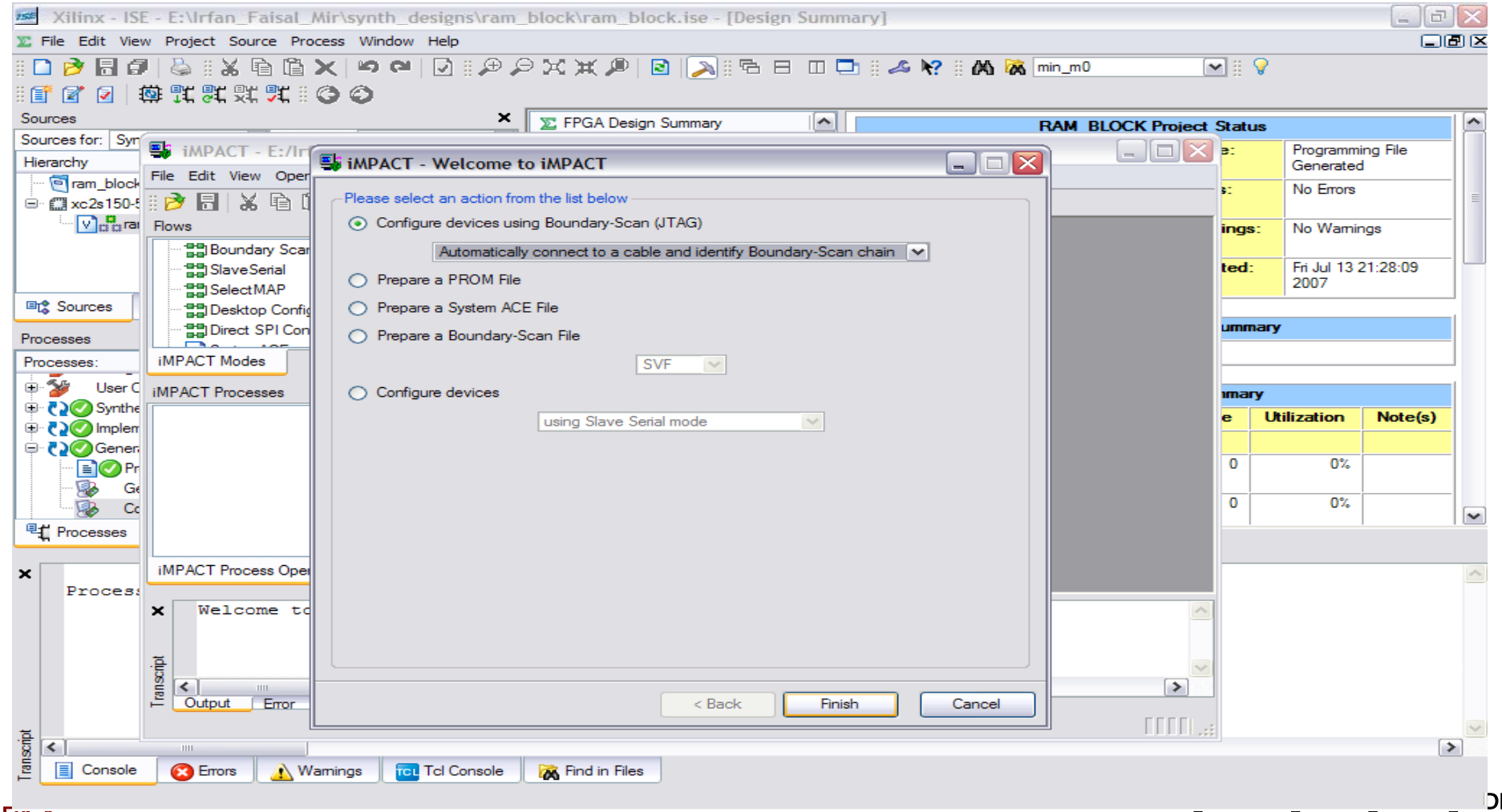
# Configure Device

- **Step1: Select Mode (Configure Device through iMPACT)**
  - **Now Run the last step of "Generate Programming File" i.e. "configure device (iMPACT)" in project navigator window.**



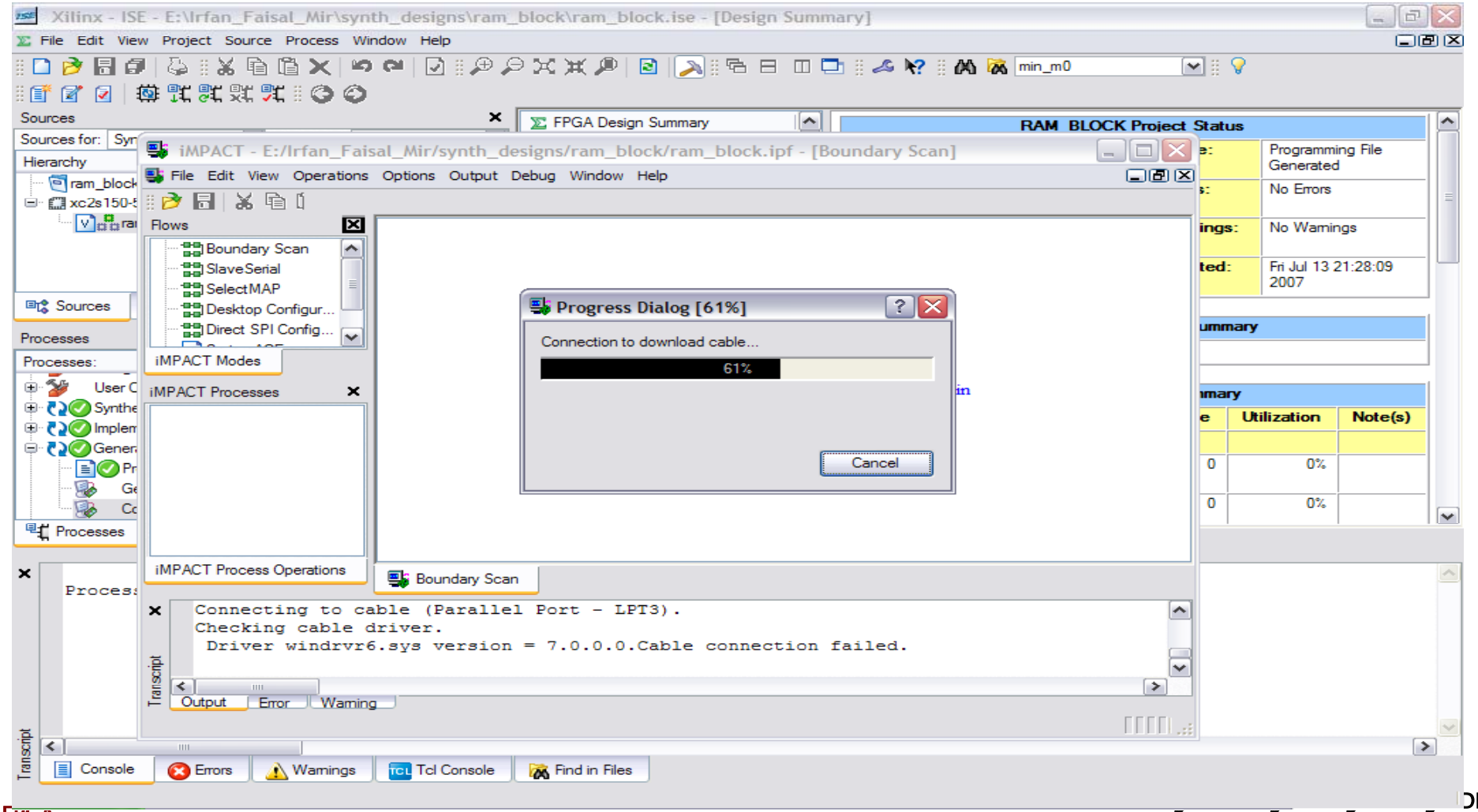
# Configure Device

- **Step1: Select Mode (Configure Device through iMPACT)**
  - **Select the “Configure device using Boundary-Scan (JTAG)” option and click on finish..**



# Configure Device

- **Step2: Detect Cable (Configure Device through iMPACT)**
  - **Click Next… It will automatically detect cable and identify Boundary-Scan chain**





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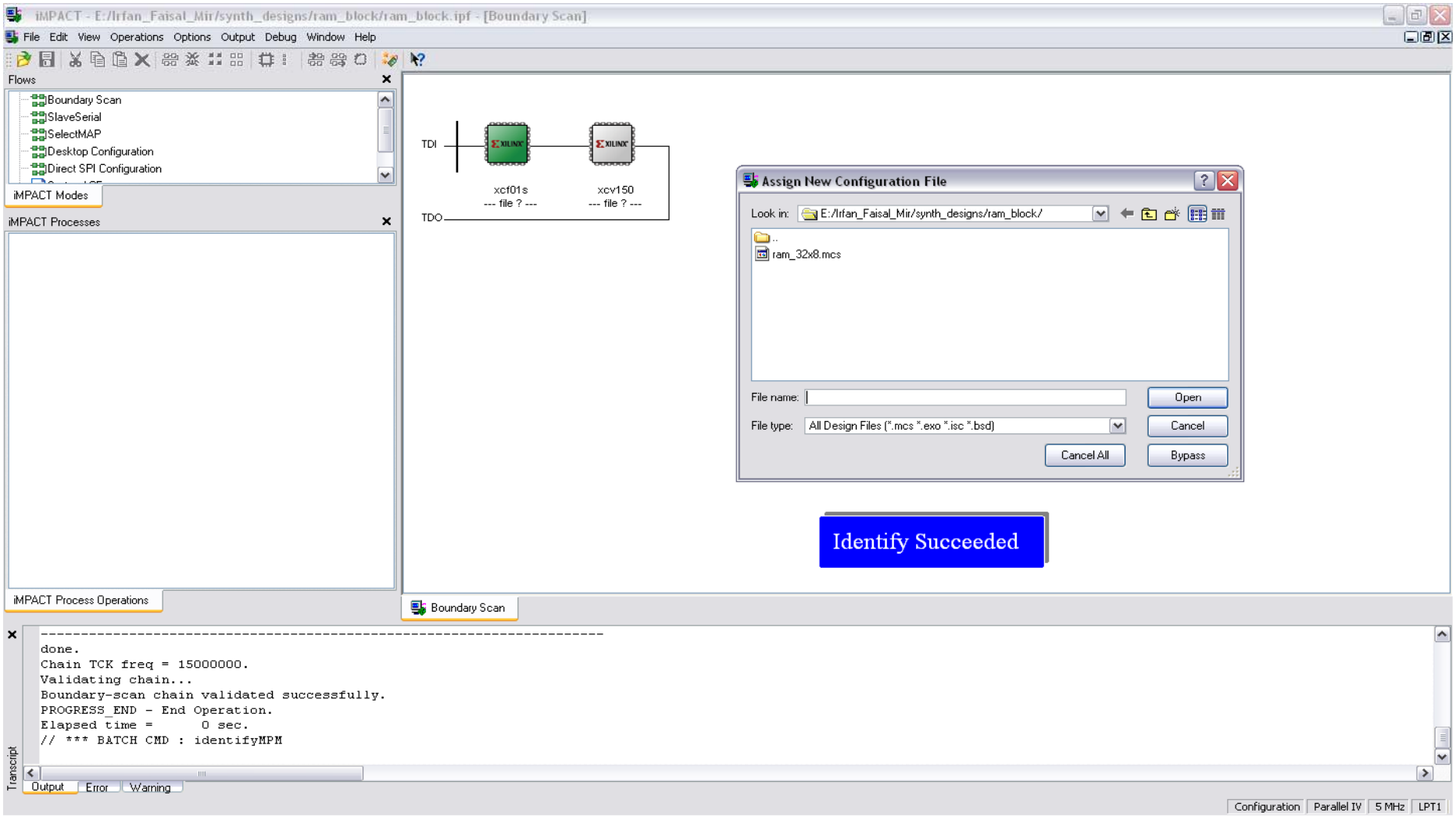
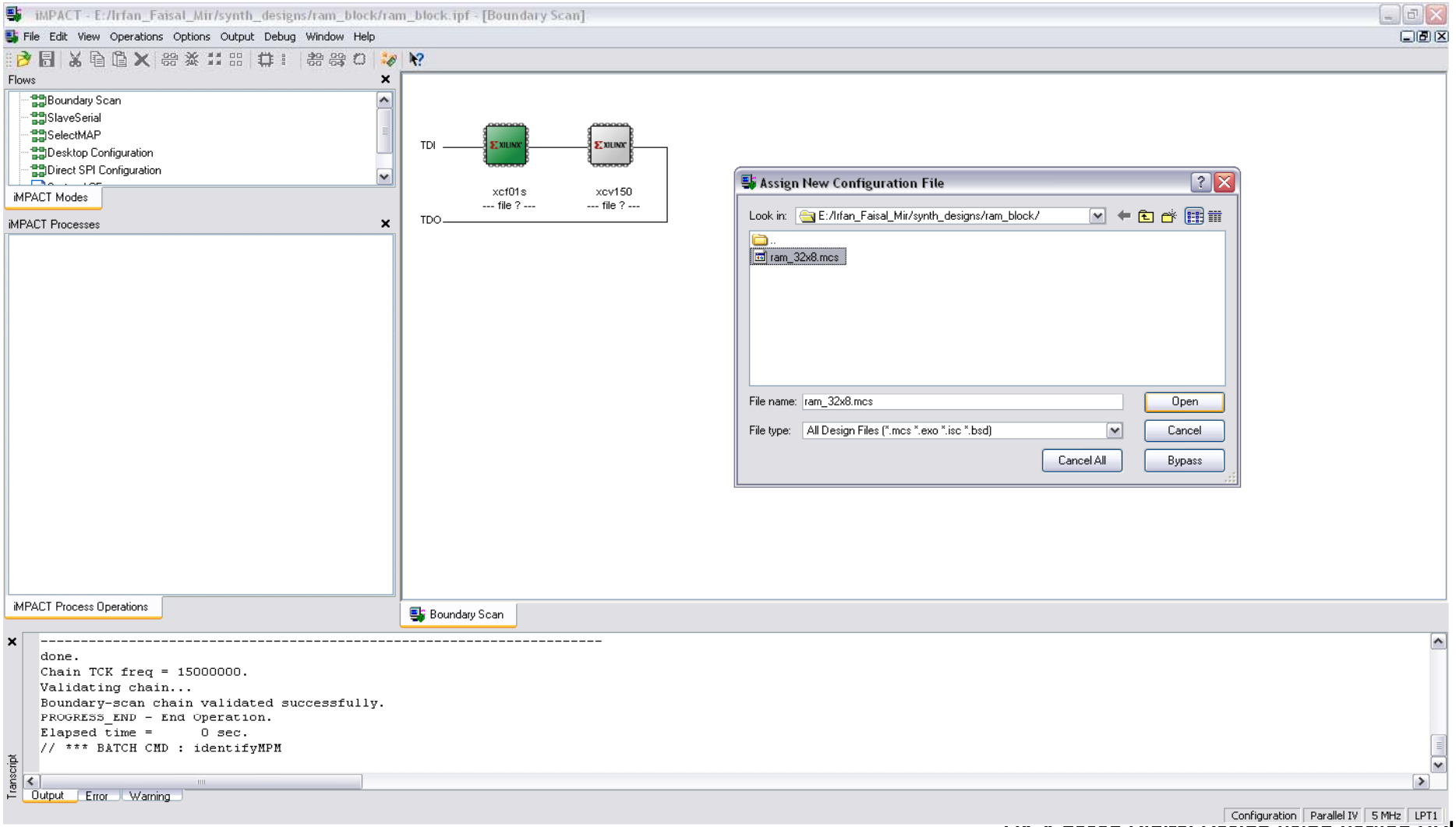
# Configure Device

- **Step3: Devices detect in Boundary Scan Chain (Configure Device through iMPACT).. Two devices (PROM and FPGA) are appeared in window.**



# Configure Device

- **Step4: Assign File to PROM only (Configure Device through iMPACT)**
  - **Add *.*mcs* file to PROM and DON'T need to assign *.bit file to FPGA.**



# Configure Device

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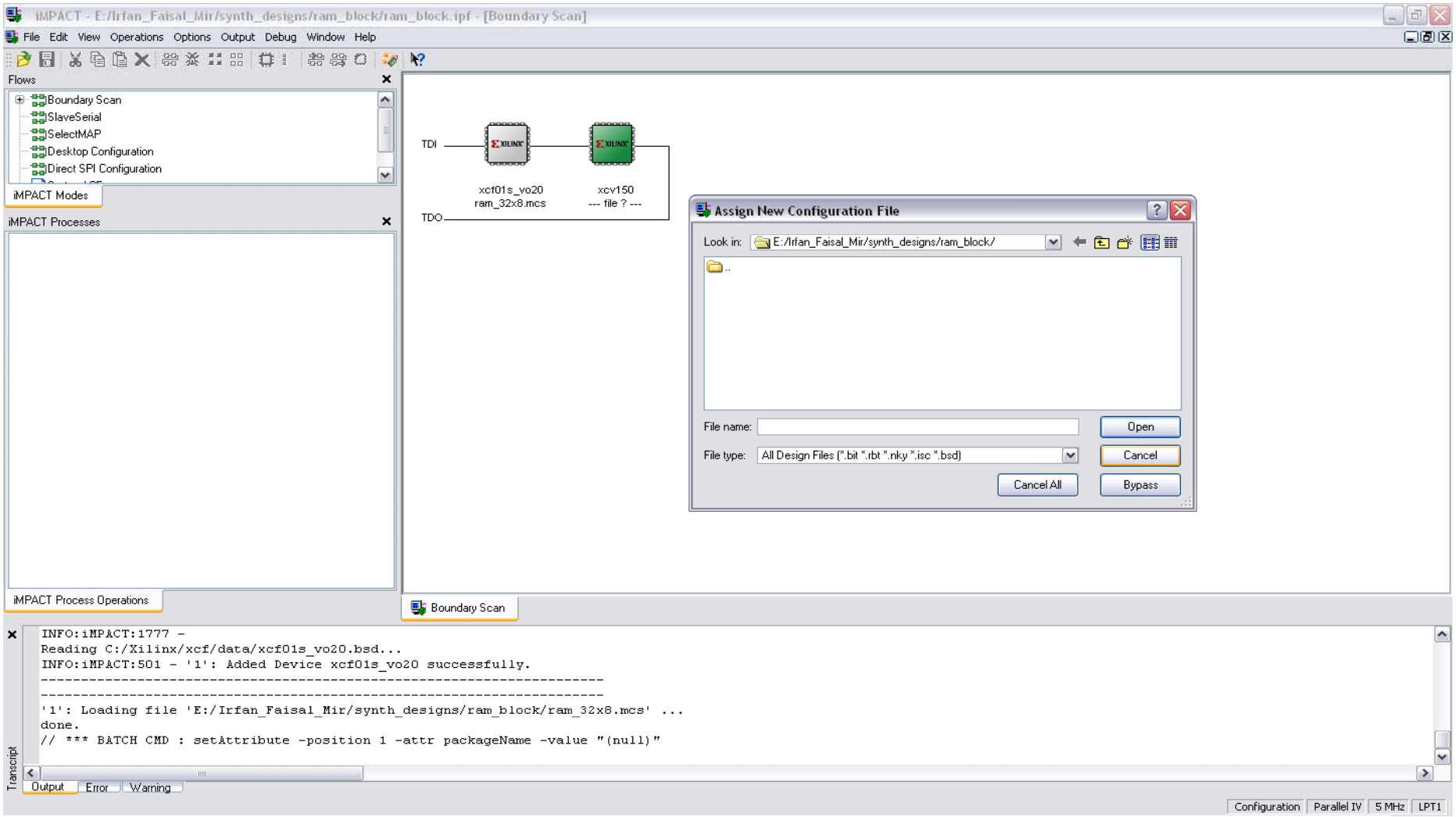
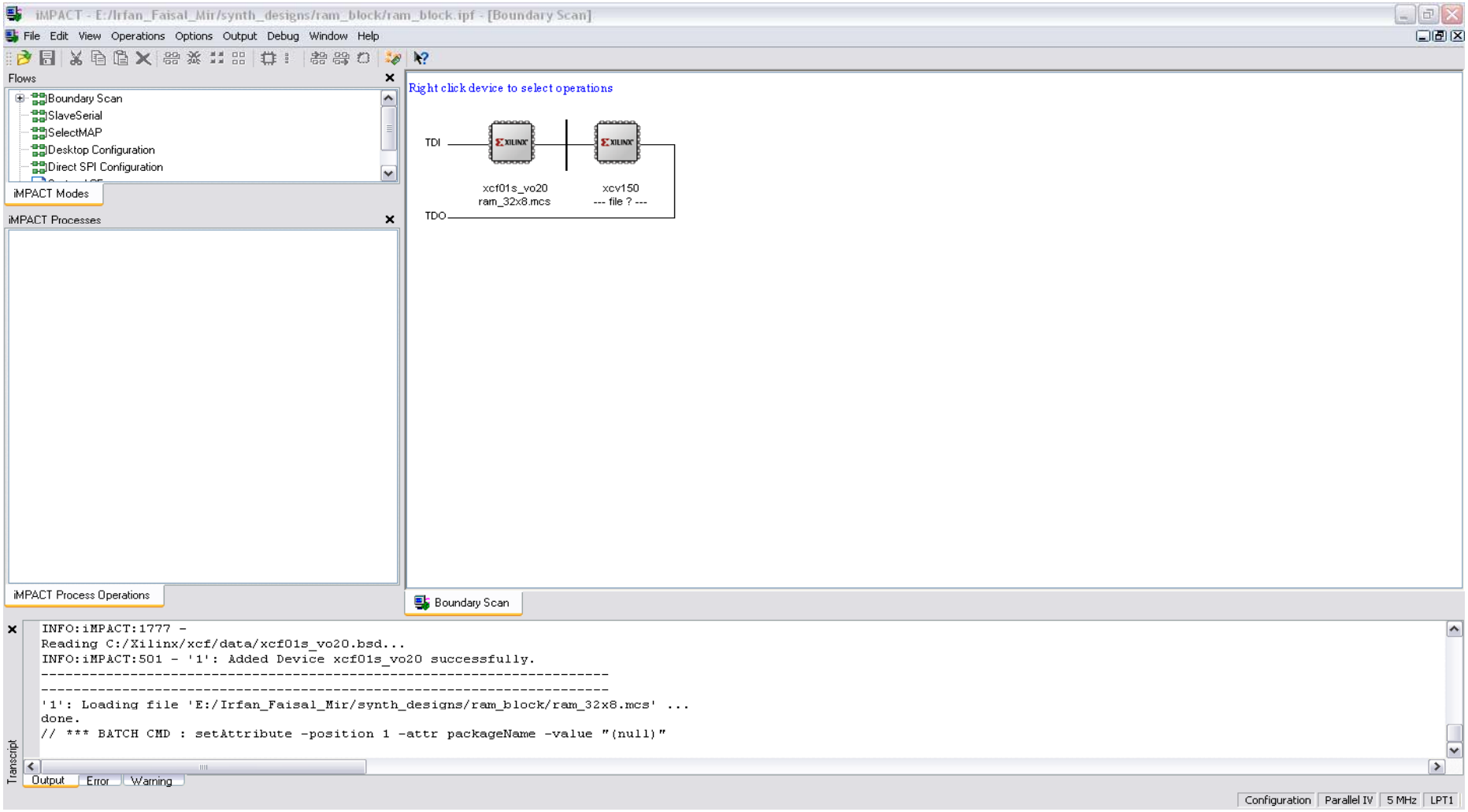


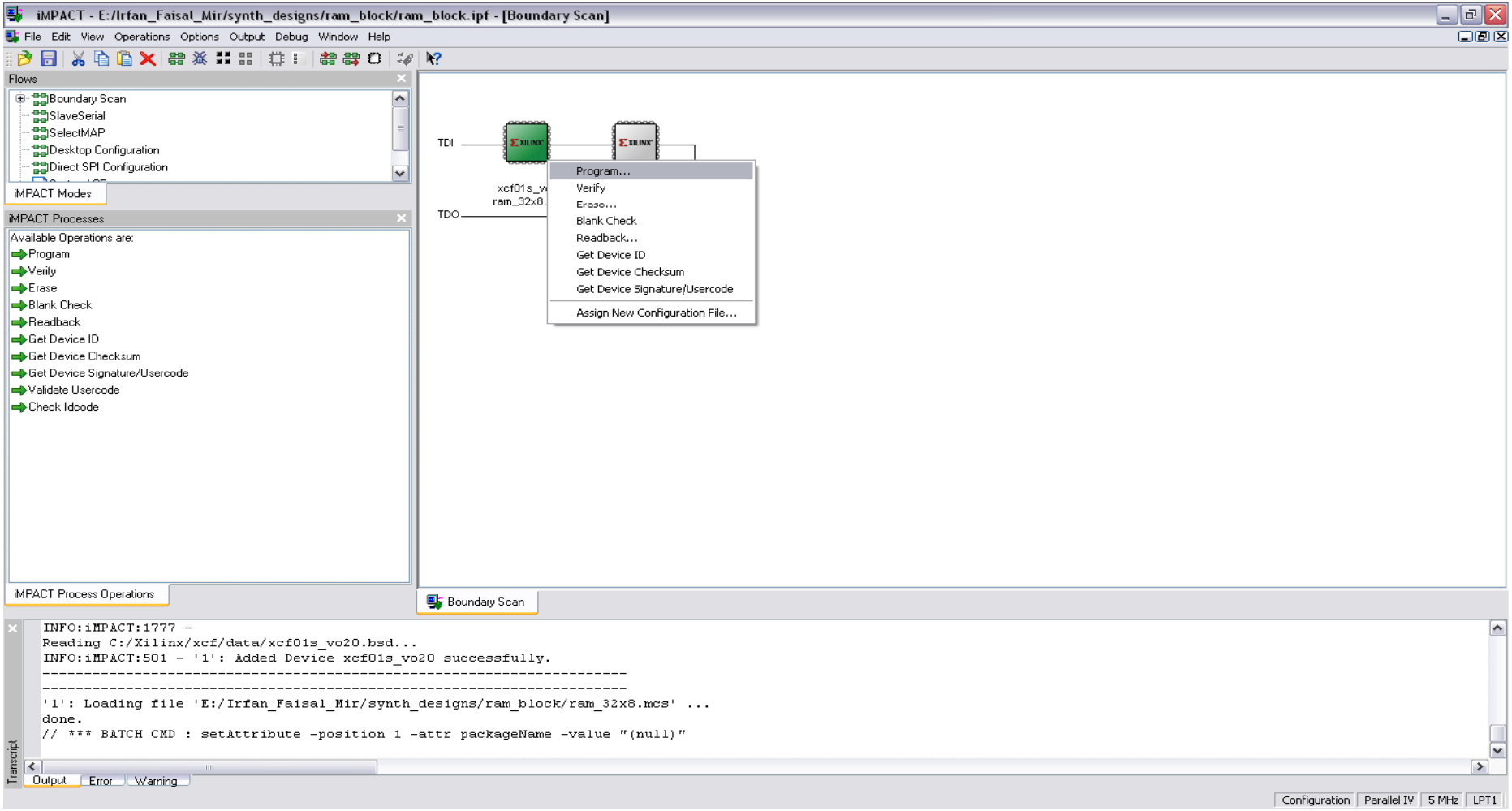
# Configure Device

- **Step4: Assign File to PROM only (Configure Device through iMPACT)**
  - **Add *.*mcs* file to PROM and DON'T need to assign *.bit file to FPGA.**



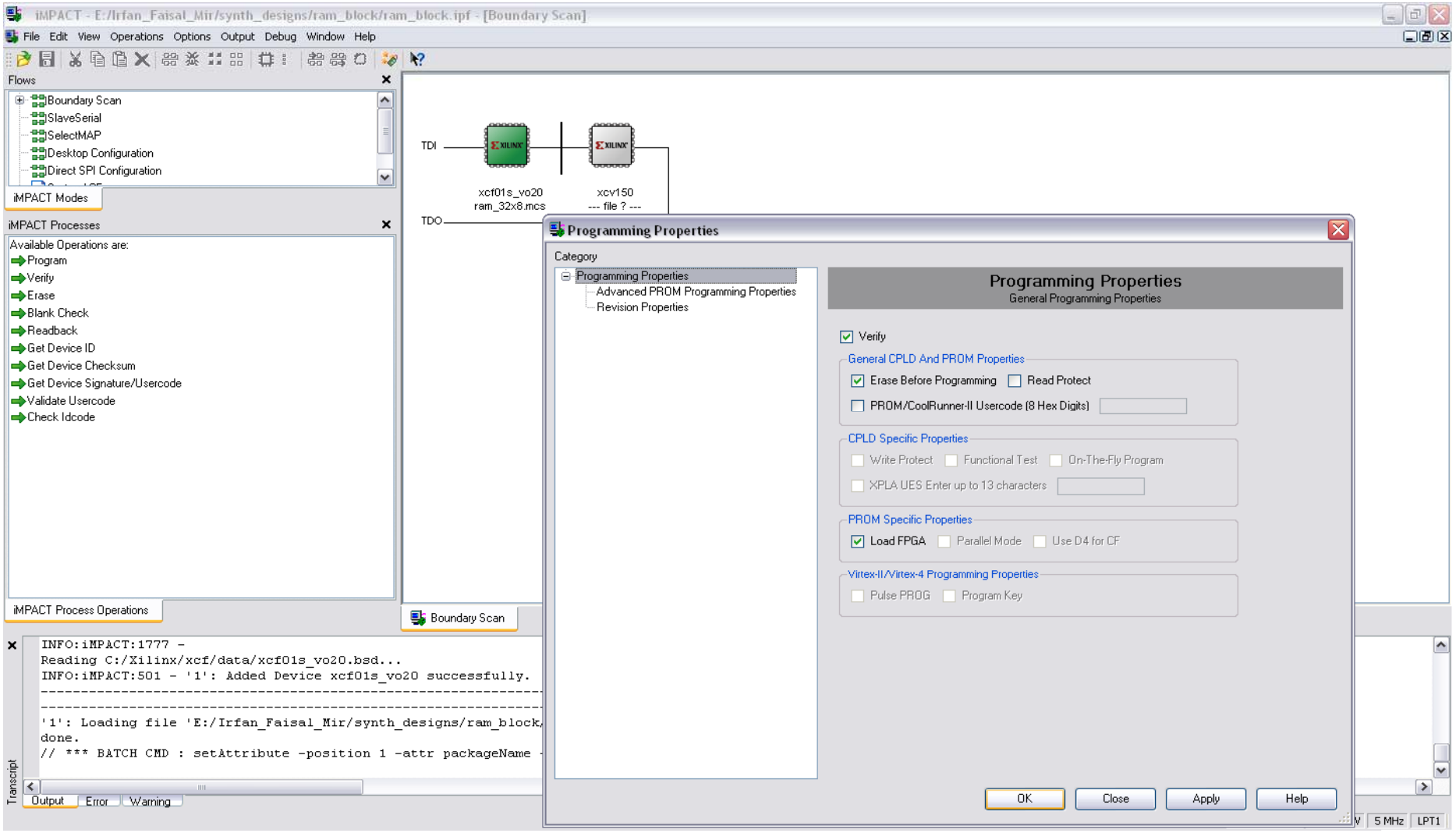
# Configure Device

- **Step6: Program PROM (Configure Device through iMPACT)**
  - **Right click the PROM and click program.**
  - **Click the following options in an appearing dialog box.**



# Configure Device

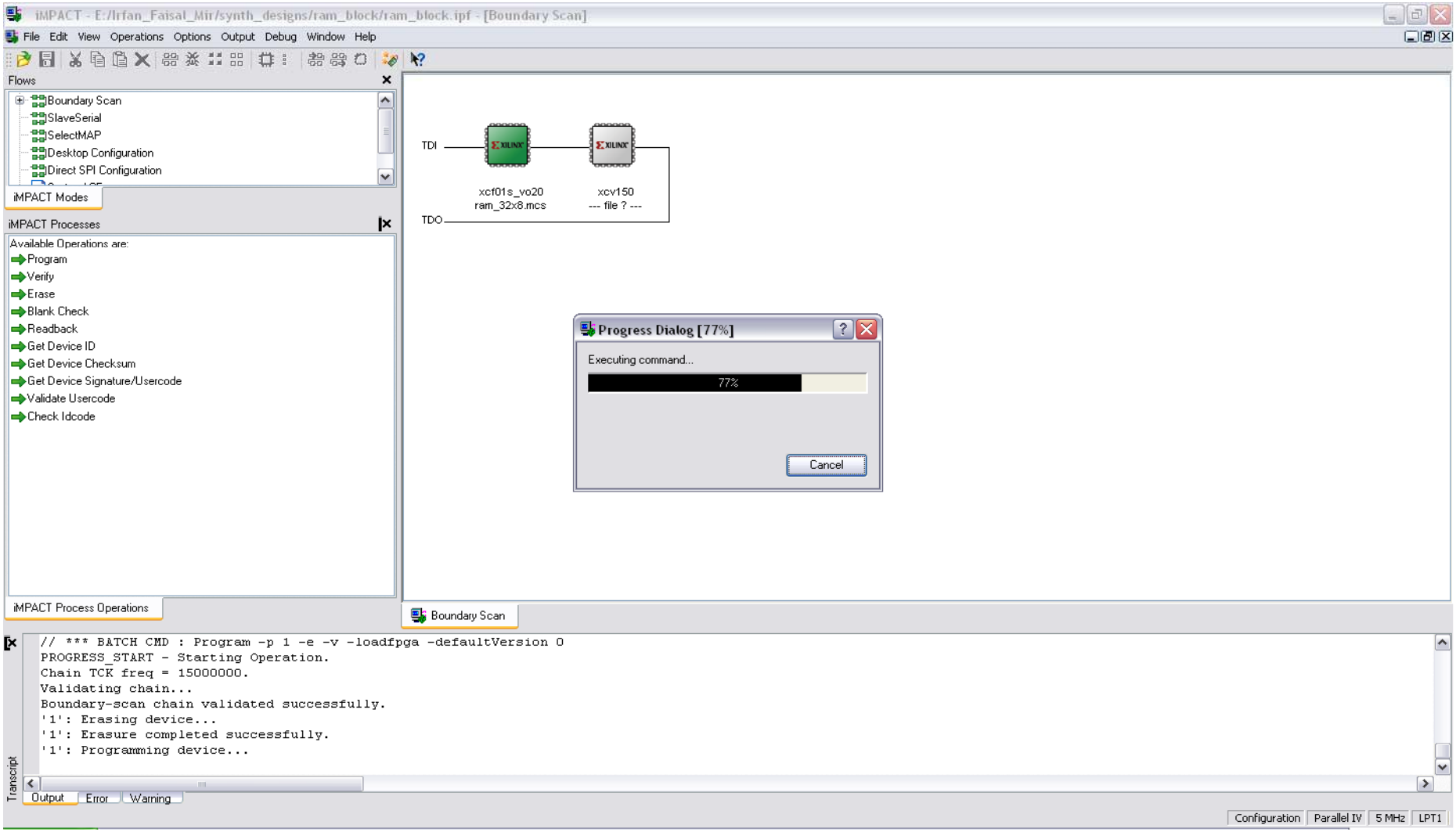
- **Step6: Program PROM (Configure Device through iMPACT)**
  - **Click the following options in an appearing dialog box.**



# Configure Device

## ➢ Step6: Program PROM (Configure Device through iMPACT)

- **Program Flash PROM process is going on...**



# Configure Device

- **Step6: Program PROM (Configure Device through iMPACT)**
  - **The PROM is programmed successfully. The PROM will configure the FPGA automatically.**