Training Course
on

FPGA based Digital Design using Verilog HDL

By

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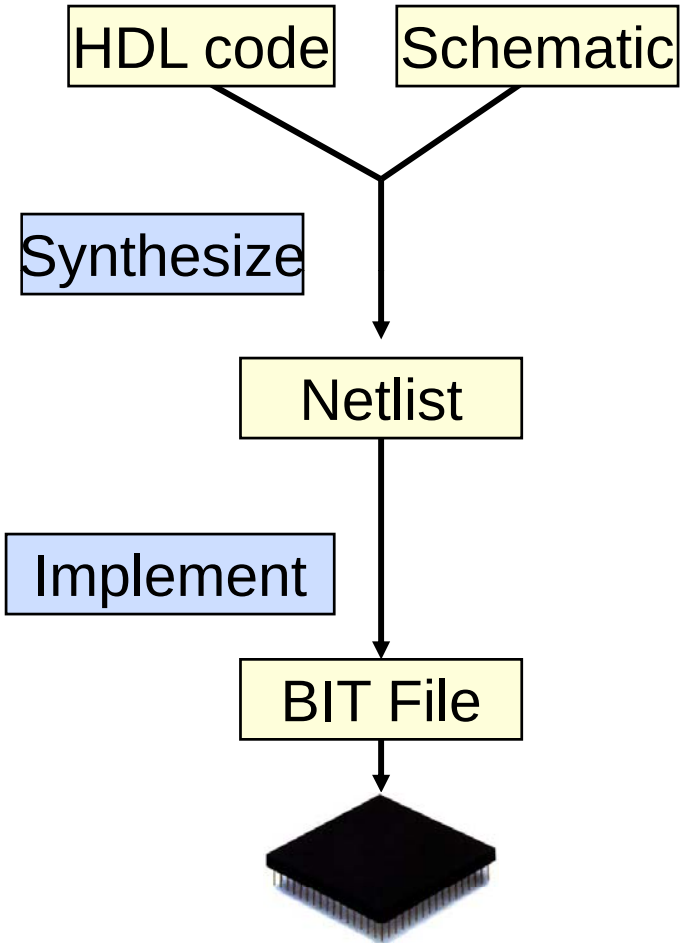
(HDL Designer)

**** Organized by*** **Skill Development Council,**
(Ministry of Labour, Manpower and overseas Pakistani)
Govt. of Pakistan.

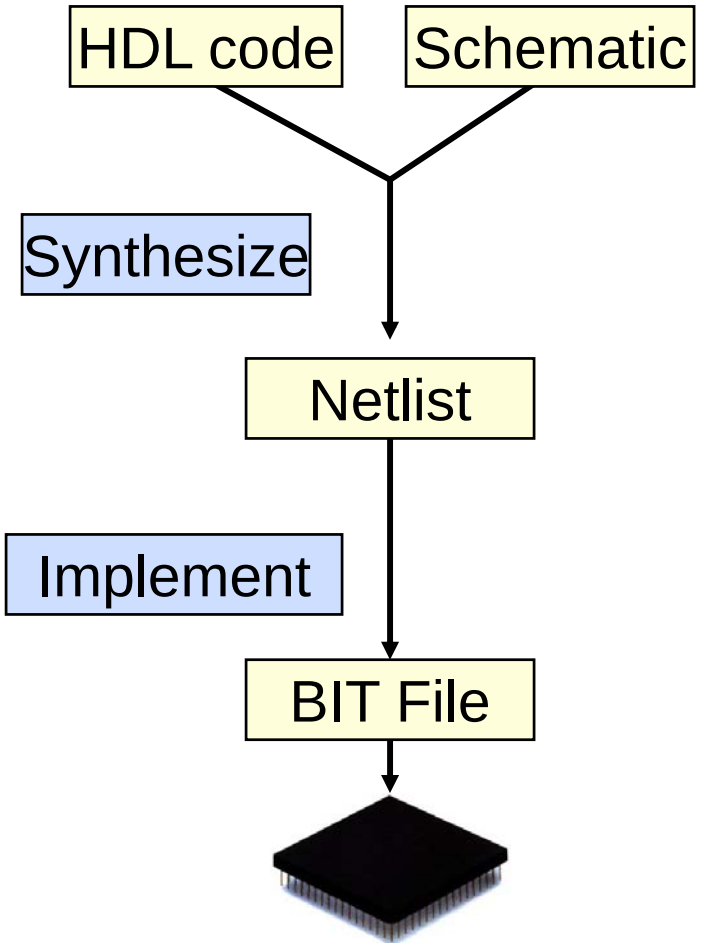
Xilinx FPGA Design Process (i)

- **Step1: Design**
  - **Two design entry methods: HDL(Verilog or VHDL) or schematic drawings**
- **Step 2: Synthesize to create Netlist**
  - **Translates V, VHD, SCH files into an industry standard format EDIF file**



Xilinx FPGA Design Process (ii)

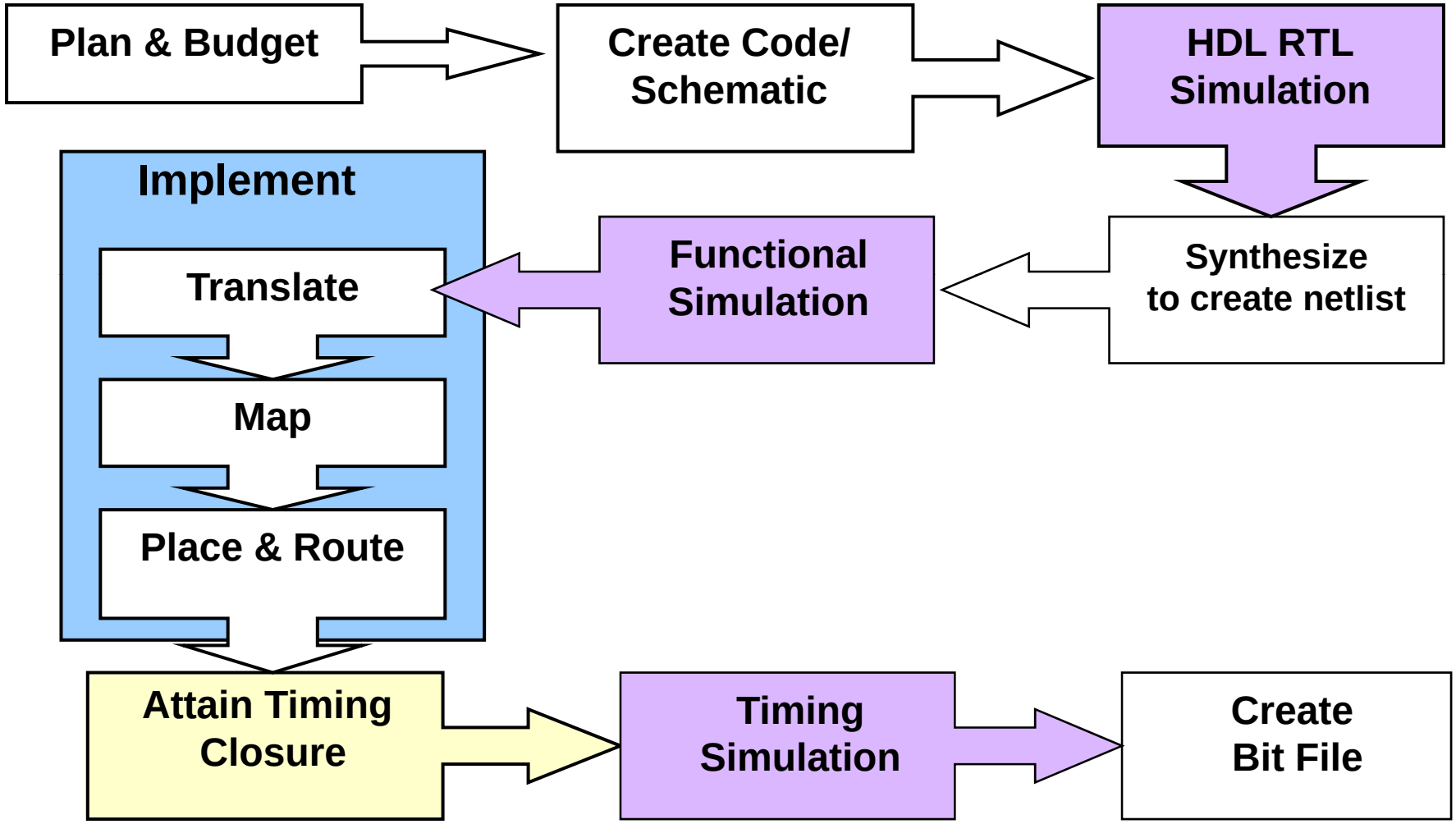
- **Step 3: Implement design (netlist)**
  - **Translate, Map, Place & Route**
- **Step 4: Configure FPGA**
  - **Download BIT file into FPGA**



Software use for Synthesis, Implementation and Configuration

- *Foundation Series ISE*
  (Integrated Software Environment)
- *For PC platforms:*
  Win98, Win2000/Xp, and NT4.0
- *For UNIX platforms:*
  HP and Solaris

Xilinx Design Flow

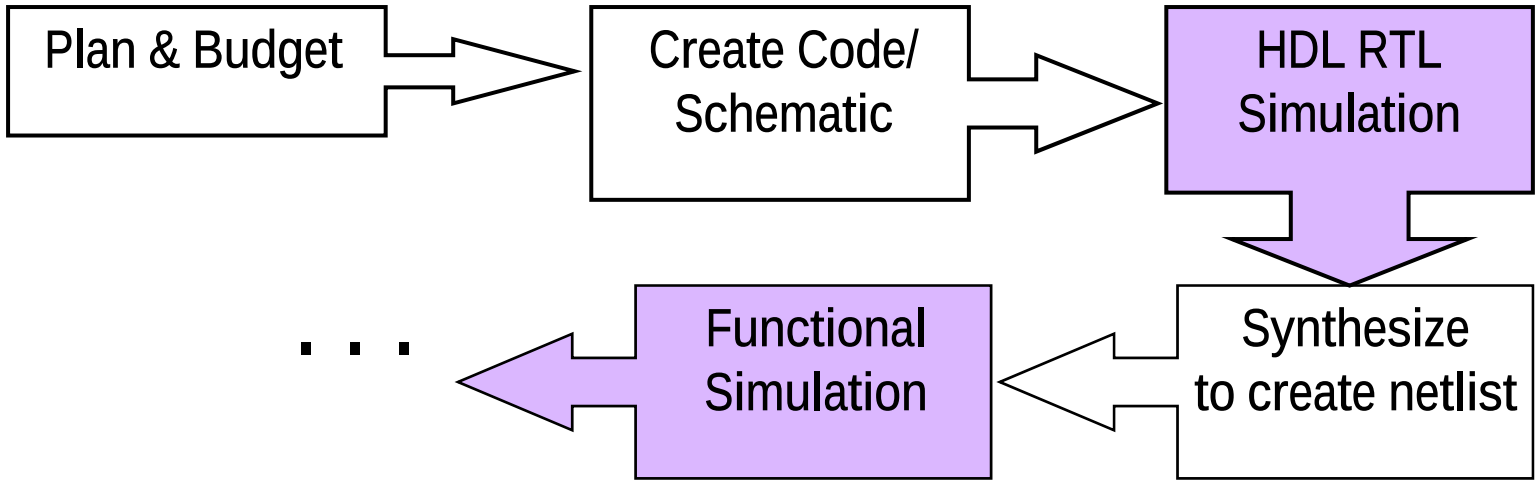


Design Entry in Xilinx ISE

- **Plan & Budget:** First you should plan and define budget
- **Two design entry methods:** HDL or schematic
  - Core Generator available to assist design entry
- Whichever method you use, you will need a tool to generate an EDIF netlist to program a Xilinx FPGA

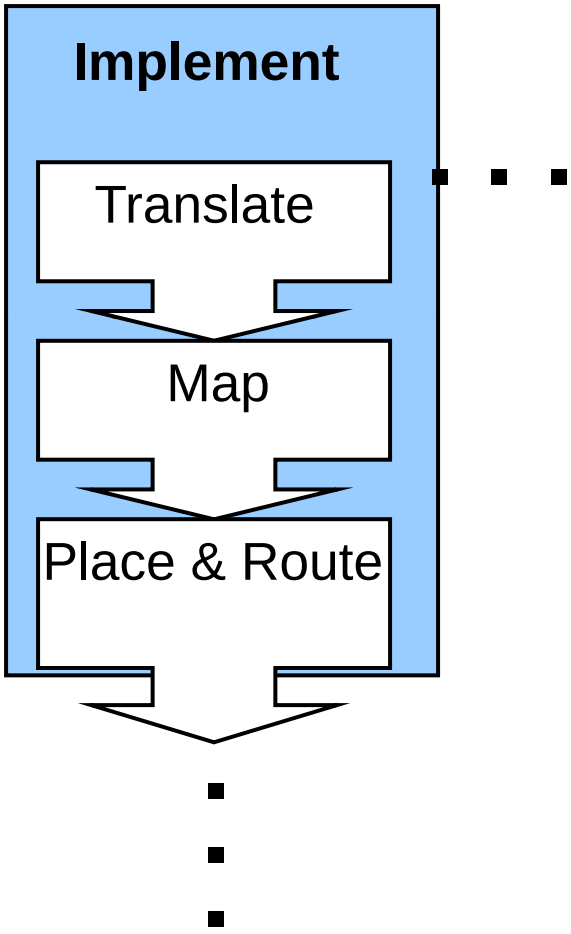
Design Entry in Xilinx ISE -- contd

- **Popular synthesis tools: Synplify, Leonardo Spectrum, FPGA Compiler II, and XST**
- **Simulate design so that it works as expected!**



Xilinx Implementation

- Once you generate a netlist, you can implement the design
- There are several outputs of implementation
  - Reports
  - Timing simulation netlists
  - Floorplan files
  - FPGA Editor files
  - and more!

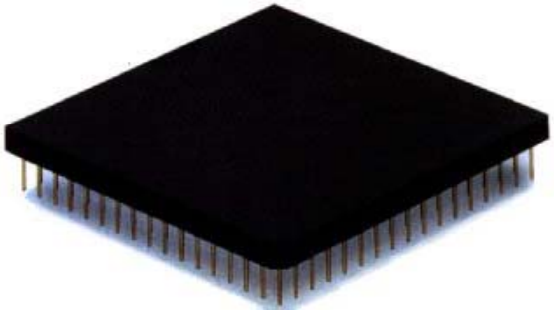


What is Implementation?

- More than just “Place & Route”
- Implementation includes many phases
  - Translate: Merge multiple design files into a single netlist
  - Map: Group logical symbols from the netlist (gates) into physical components (CLBs,IOBs)
  - Place & Route: Place components onto the chip, connect them, and extract timing data into reports
- Each phase generates files that allow you to use other Xilinx tools (such as Floorplanner, FPGA Editor, XPower, Multi-Pass Place & Route)

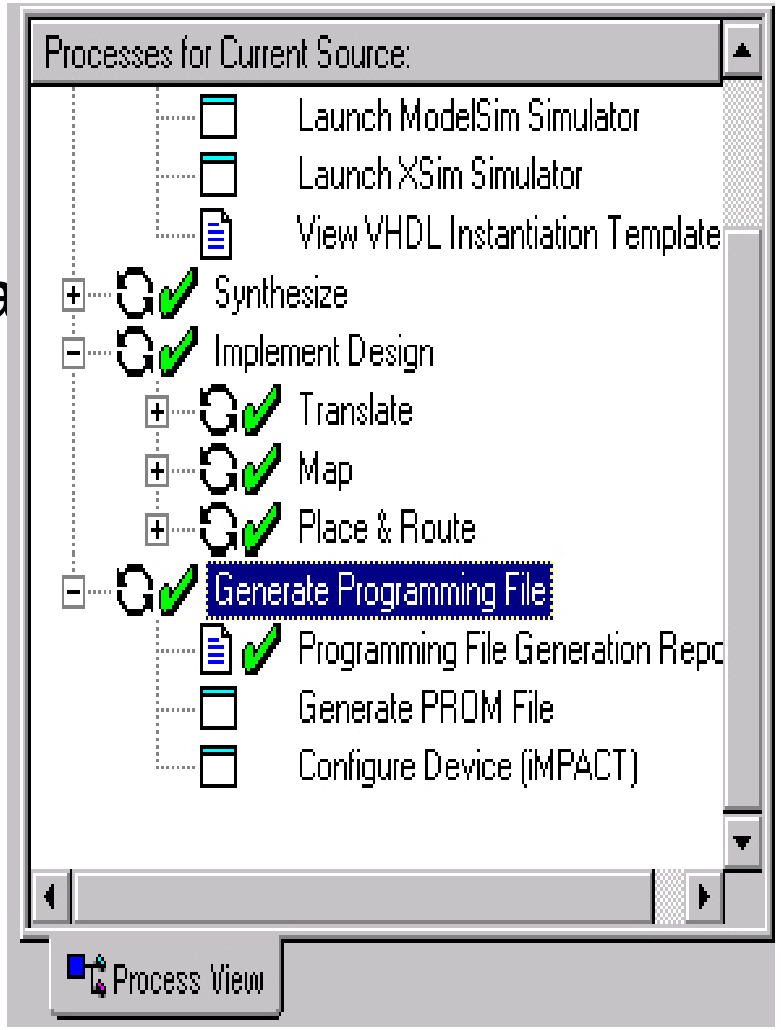
Download in Xilinx FPGAs

- Once a design is implemented, you must create a file that the FPGA can understand
  - This file is called a bit stream: a BIT file (.bit extension)
- The BIT file can be downloaded directly to the FPGA, or can be converted into a PROM file which stores the programming information



Program the FPGA

- There are two ways to program an FPGA
  - Through a PROM device
    - You will need to generate a file that the PROM programmer will understand
  - Directly from the computer
    - Use the iMPACT configuration tool



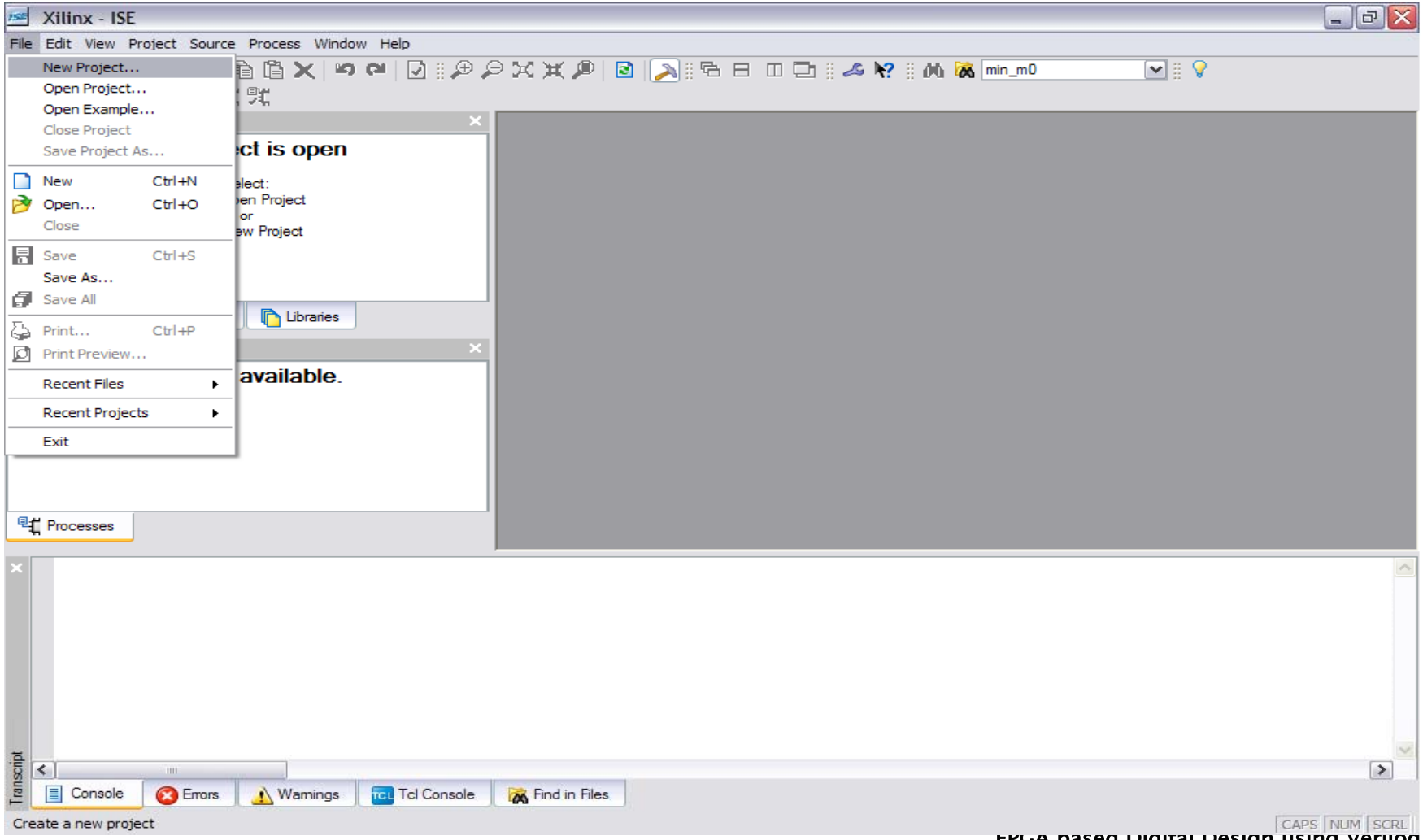
Xilinx ISE has a complete Solution

- The Xilinx design process contains only four steps: design, synthesize, implement, configure

- The Xilinx design process can all be done through the ISE Project Navigator

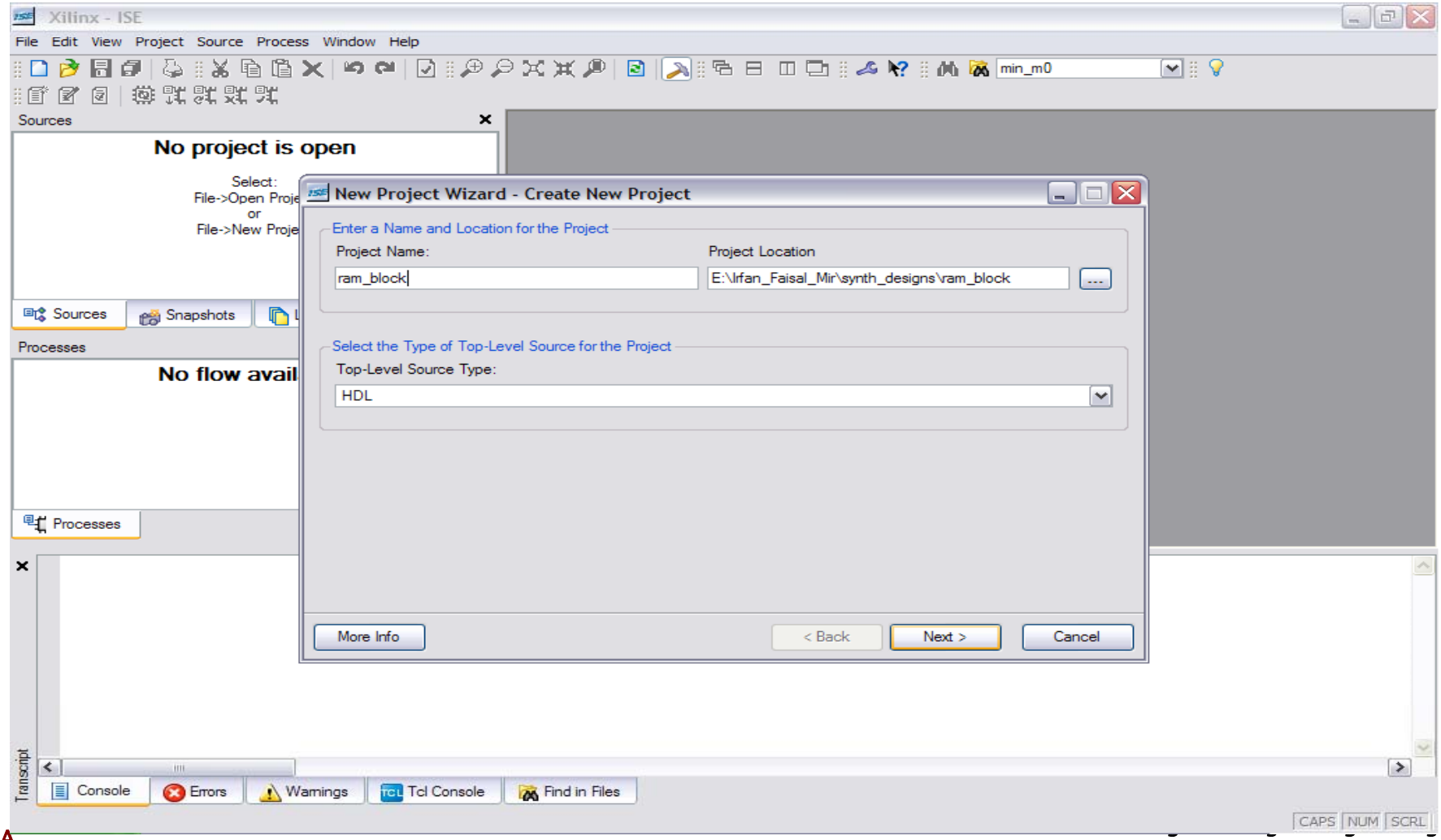
Design Example

- **Step1: Create Project in ISE 8.2i (Project Navigator)**
  - **In file menu, start from “New Project” option…**



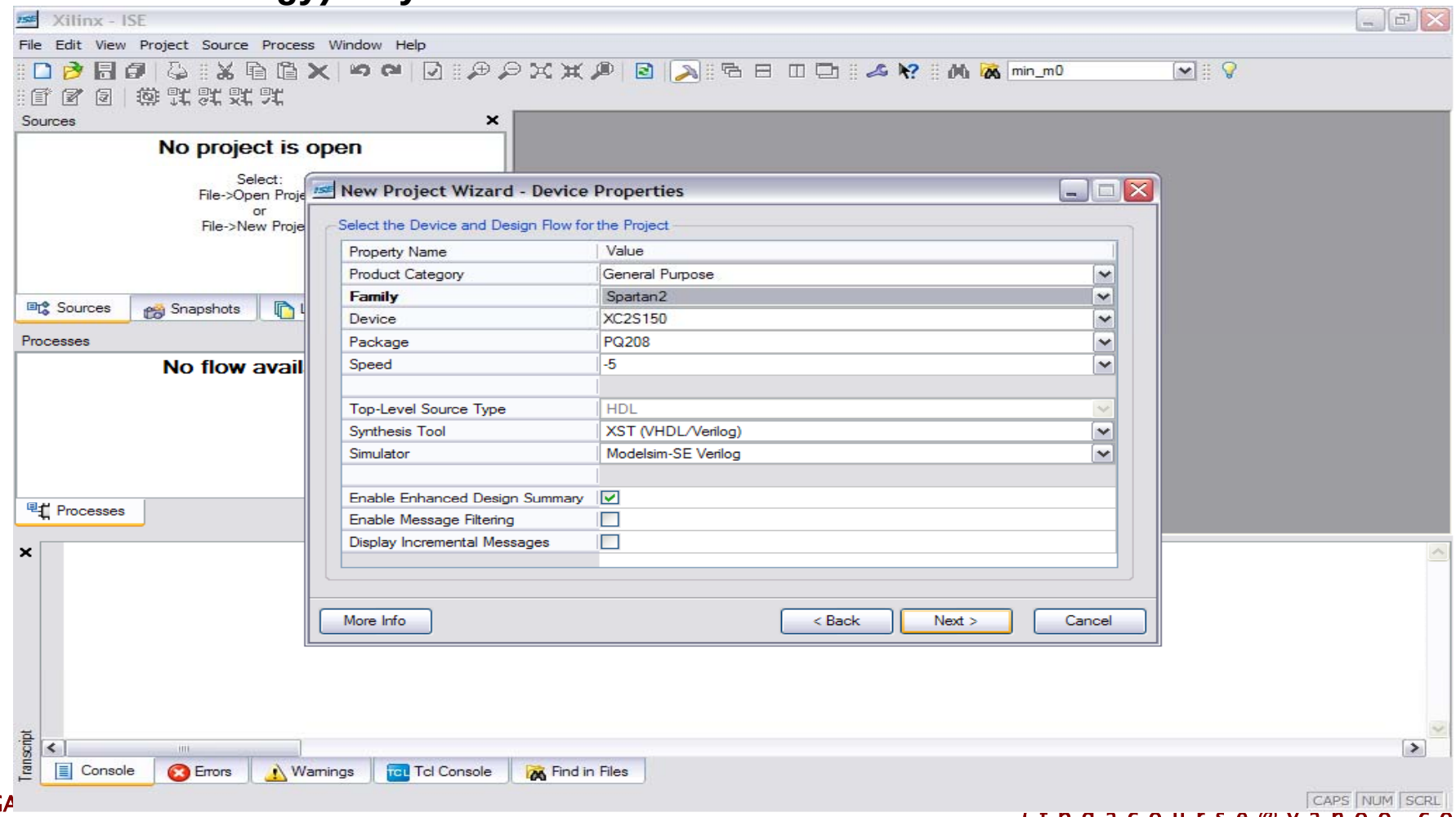
Design Example

- **Step1: Create Project in ISE 8.2i (Project Navigator)**
  - **Write Project name, mention project path and select Top Level Module Type "HDL"**



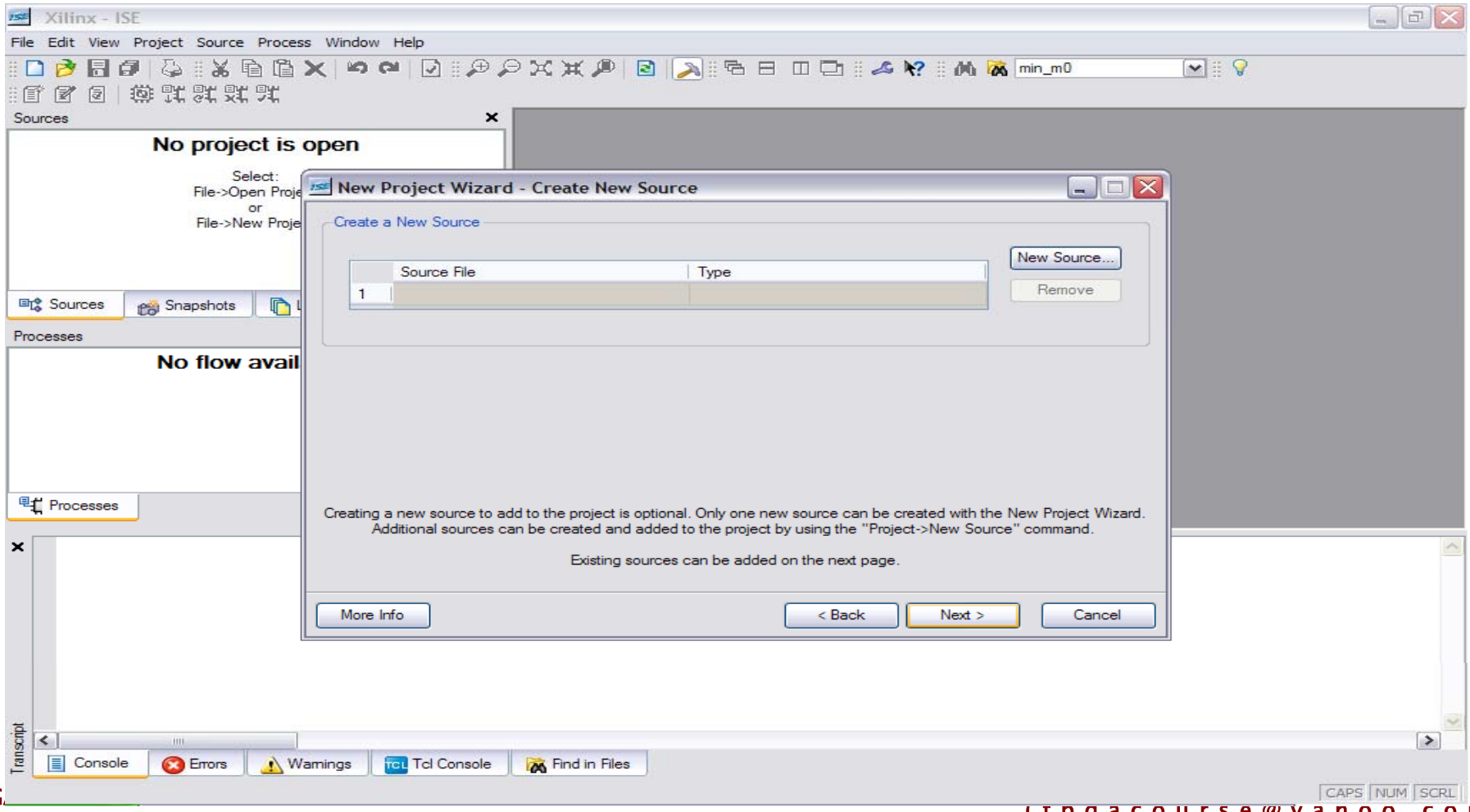
Design Example

- **Step1: Create Project in ISE 8.2i (Project Navigator)**
  - **Select Device Family, Device, package, speed grade for FPGA. Here you also select Synthesis Flow for FPGA. ISE 8.2i has support XST (Xilinx Synthesis Technology) only.**



Design Example

- **Step2: Create New Files in ISE 8.2i (Project Navigator)**
  - **Here you can create new Verilog HDL files in current project…We simply ignore this step because we have already existing files that are verified in ModelSim simulator.**



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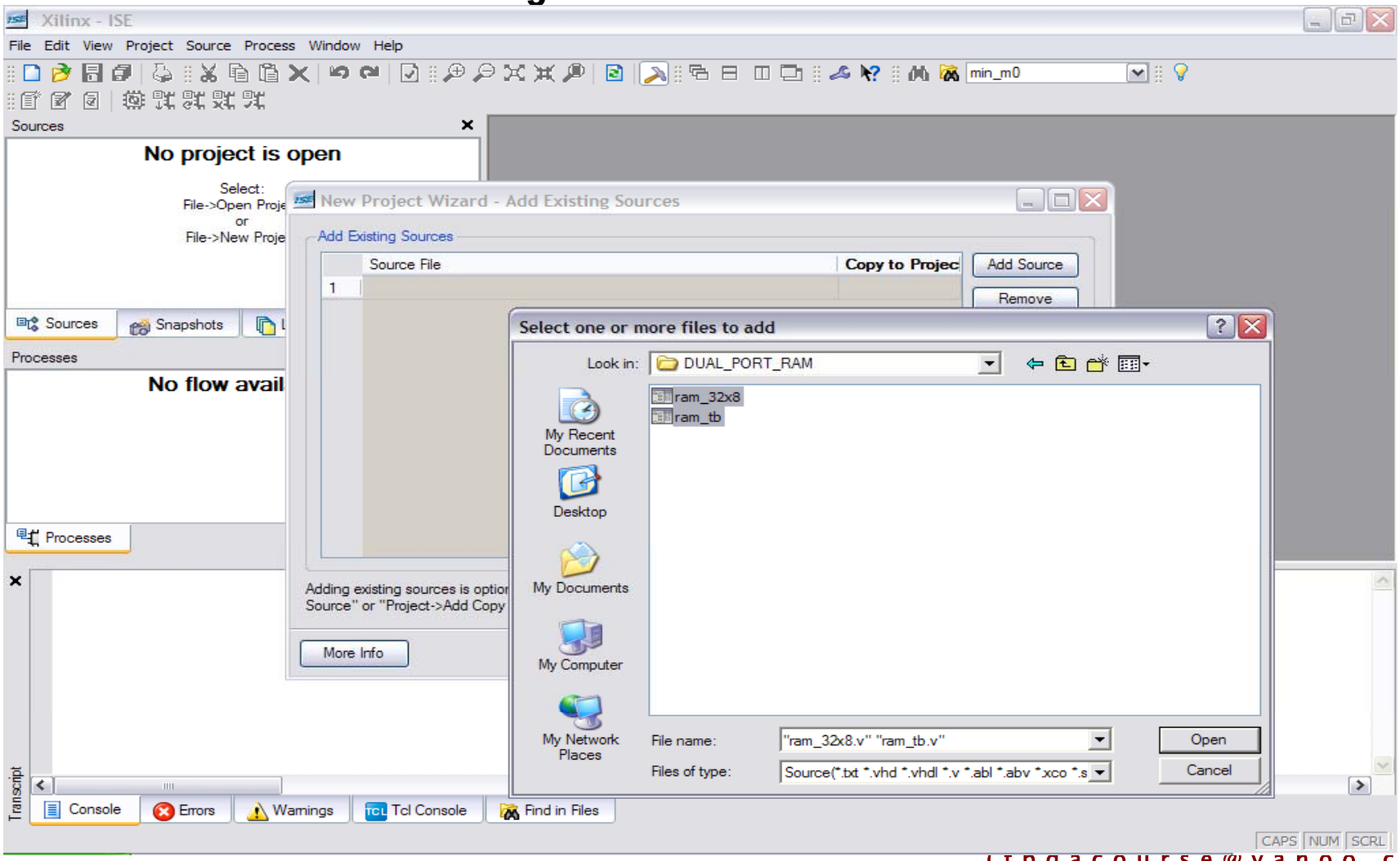
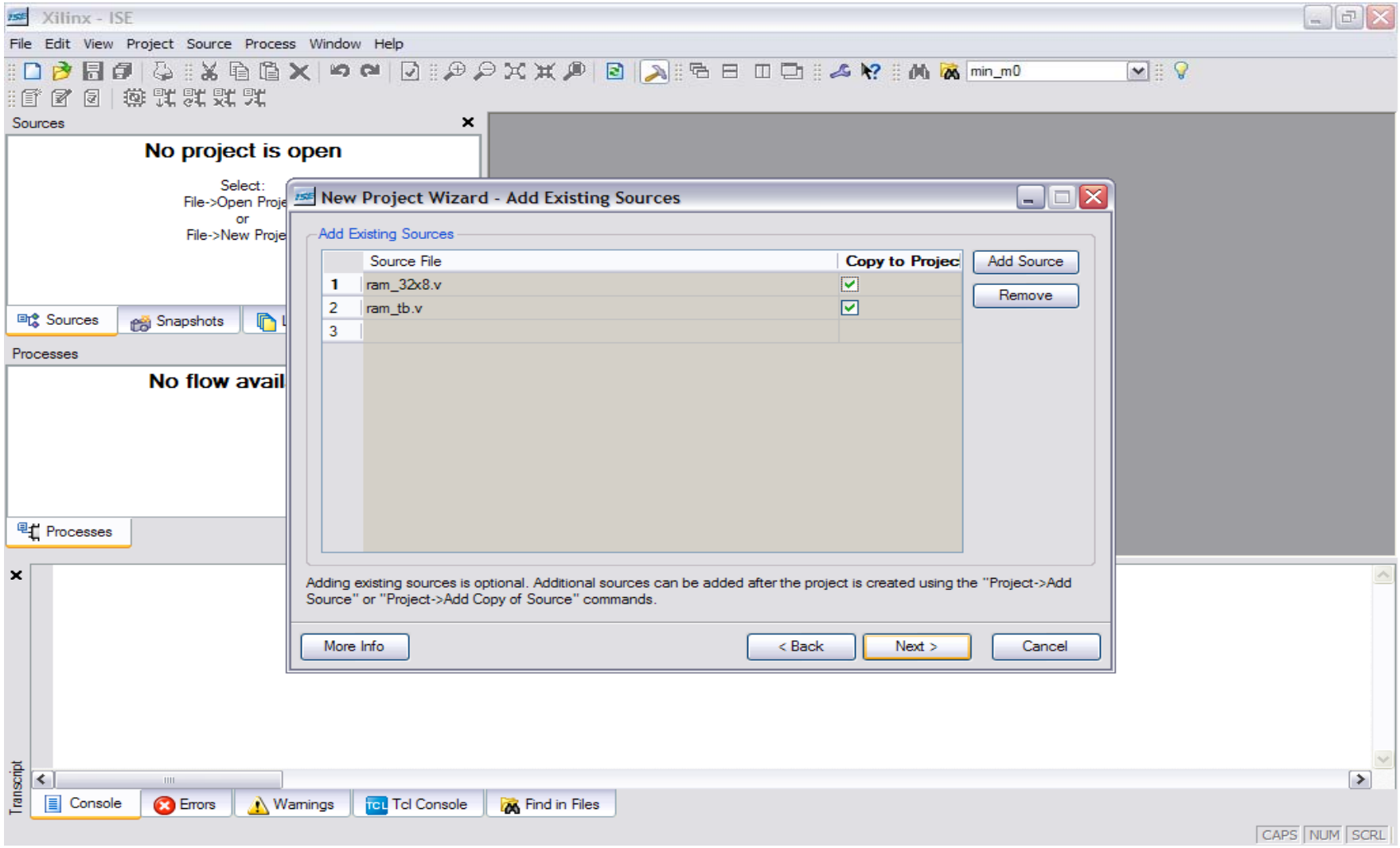
Design Example

- **Step2: Add existing Files in Project by using ISE 8.2i (Project Navigator)**
  - **Here we add existing verilog source files (RTL + Testbench) in ISE 8.2i. ISE detects which one is Design file or Test Fixture file itself.**



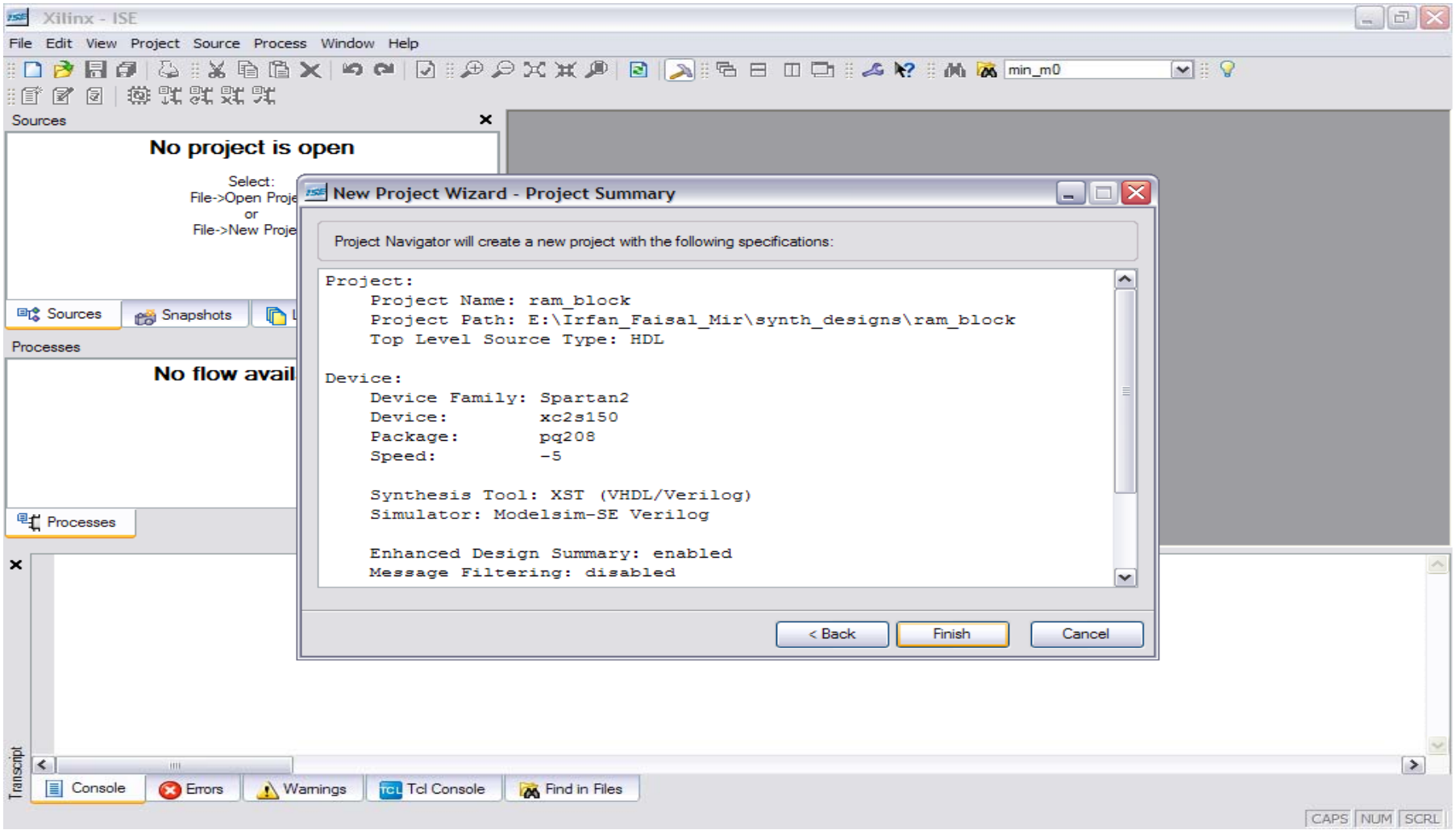
Design Example

- **Step3: Mention file type by using ISE 8.2i (Project Navigator)**
  - **Here we may copy these files or not in ISE working directory….**



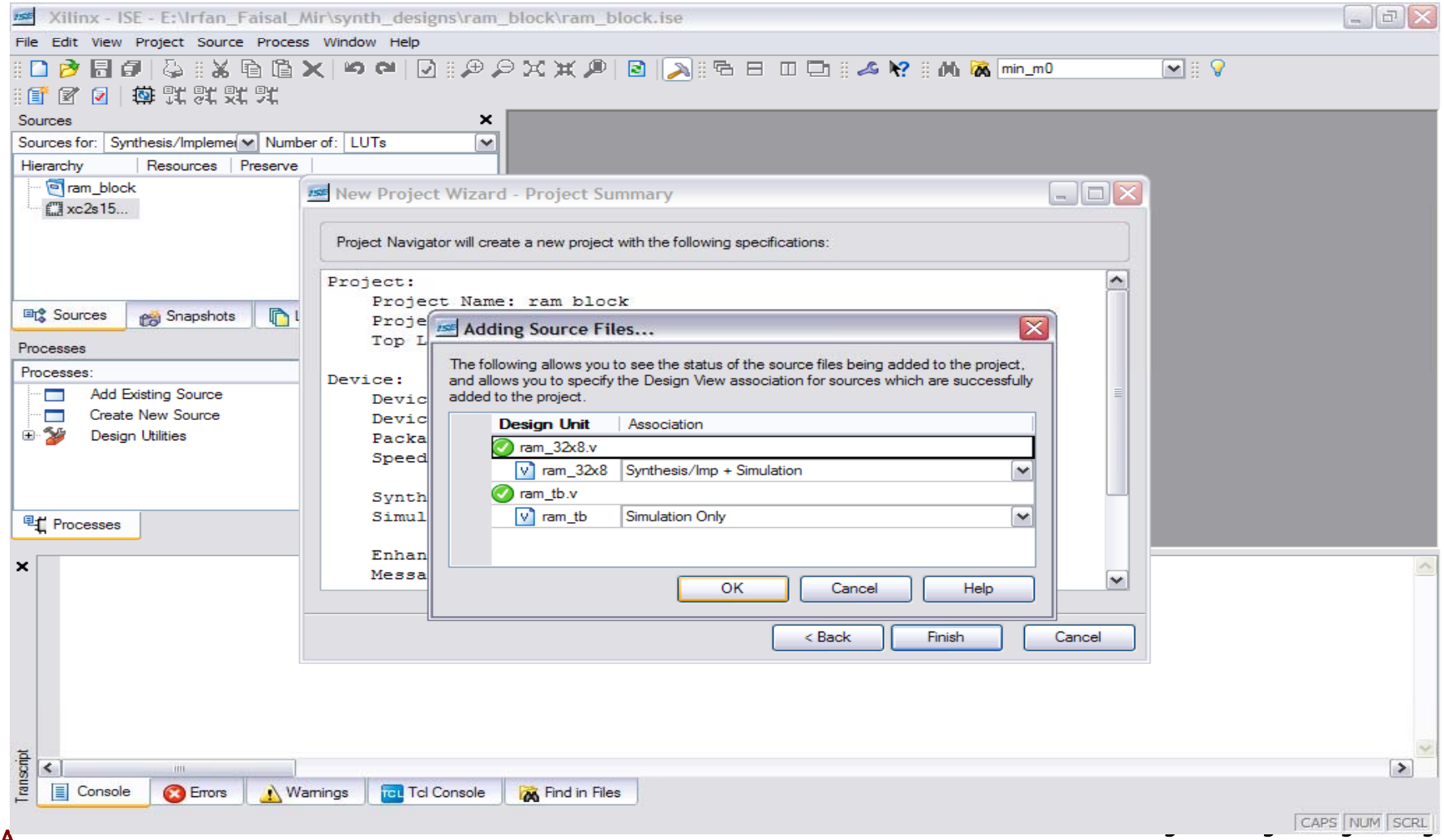
Design Example

- **Step3: Mention file type by using ISE 8.2i (Project Navigator)**
  - **Now design entry step has completed now. Select finish to close it…**



Design Example

- **Step3: Mention file type by using ISE 8.2i (Project Navigator)**
  - **Here we select the file type whether it is Verilog Design File or Verilog Test Fixture file…**



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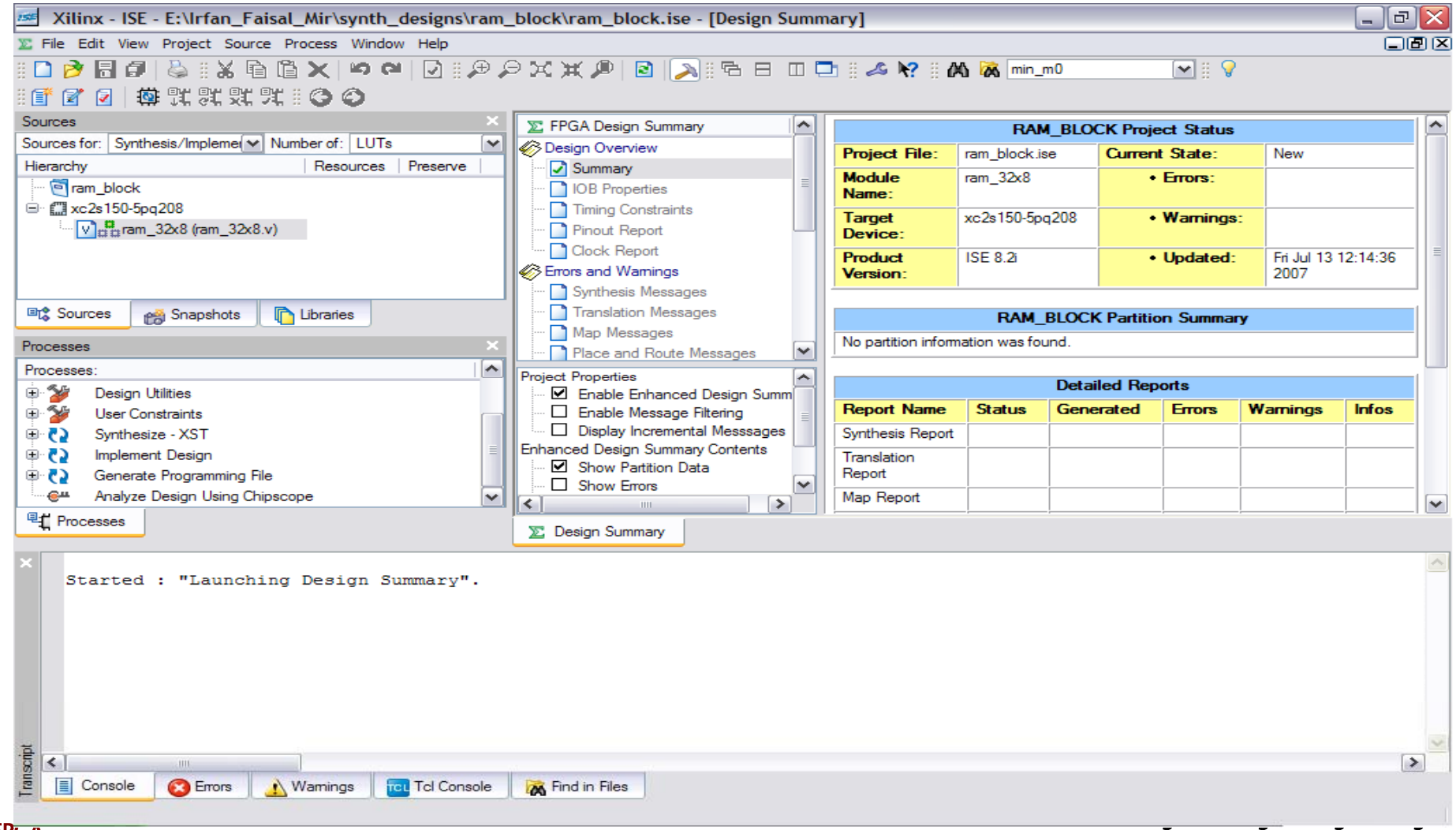
Design Example

- **Step4: Synthesis your design by using ISE 8.2i (Project Navigator)**
  - **First select the top module file of your project in “sources in project” small window.**



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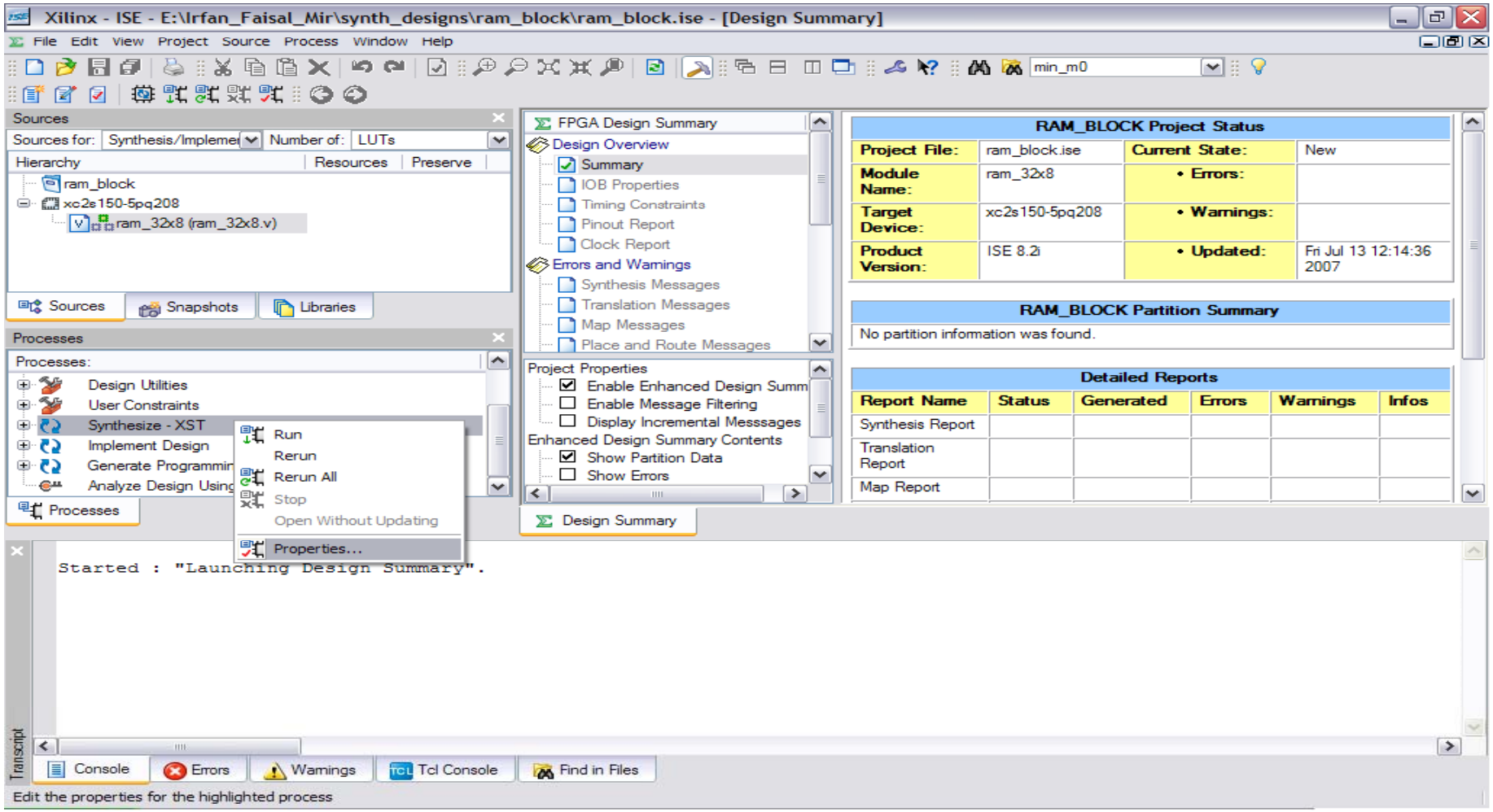
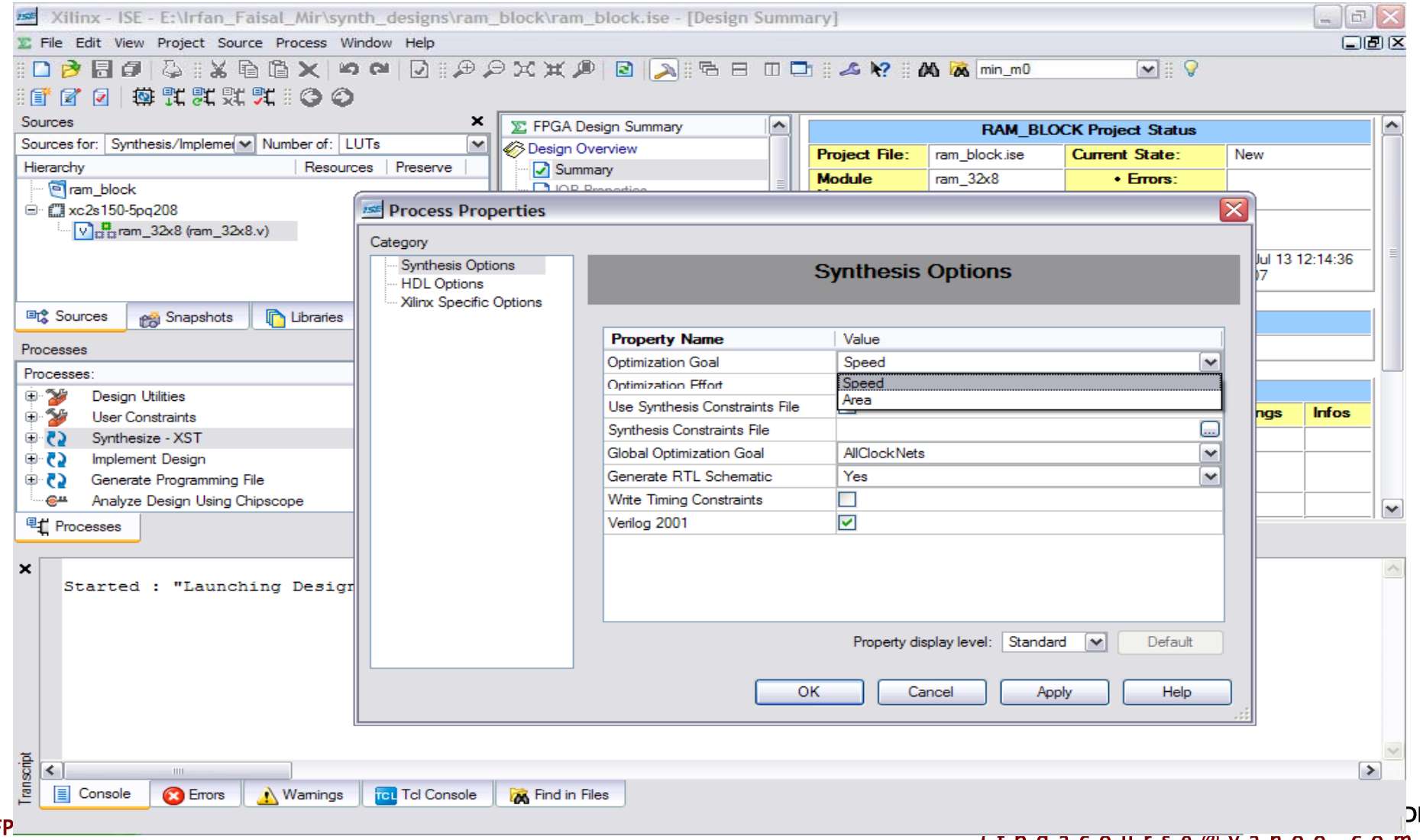
Design Example

- **Step4: Synthesis your design by using ISE 8.2i (Project Navigator)**
  - **Just right click on "Synthesize XST" in "Processes for Source" small window. View the properties...**



Design Example

- **Step4: Synthesis your design by using ISE 8.2i (Project Navigator)**
  - **You can control the synthesis flow of your design.**



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Design Example

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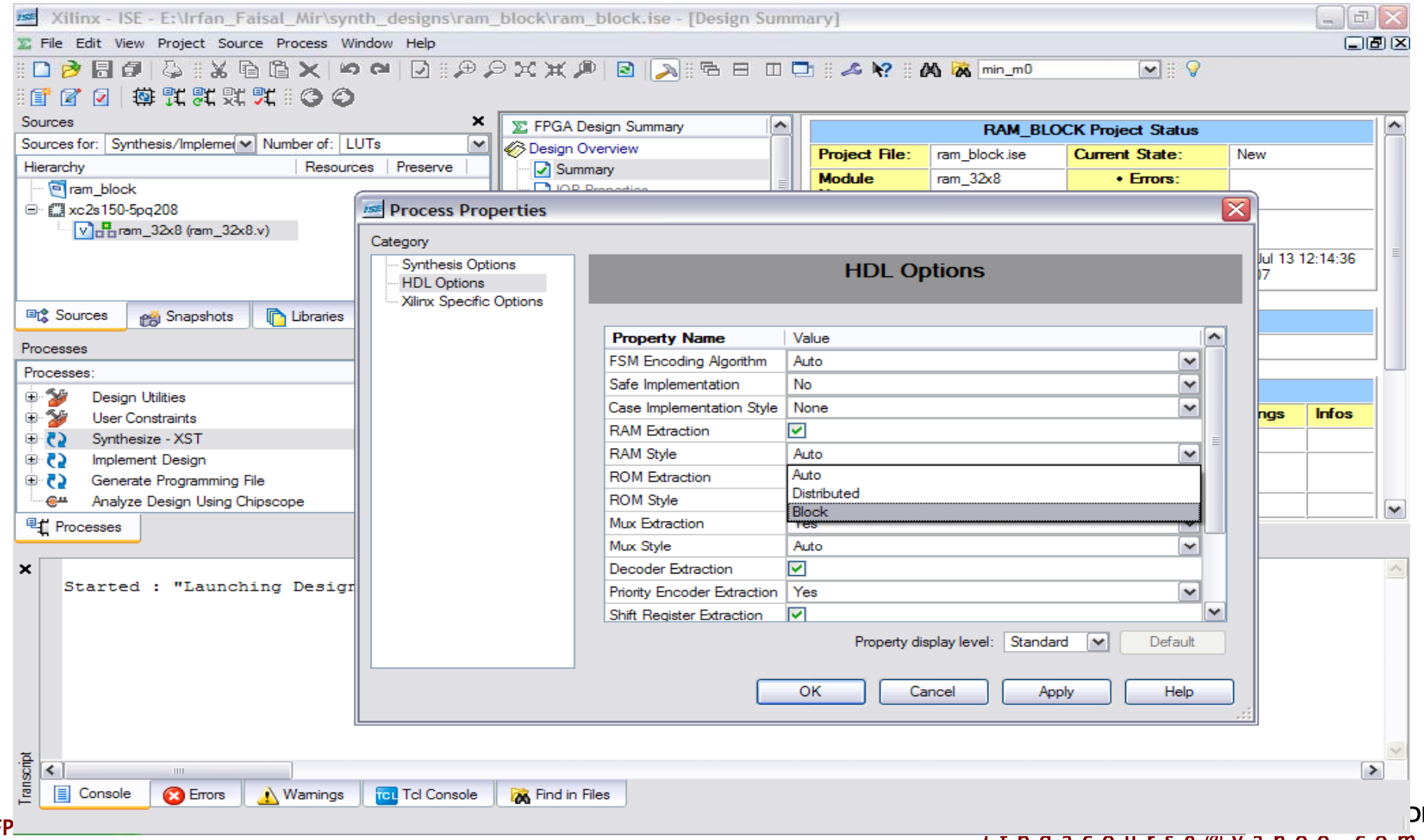

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Design Example

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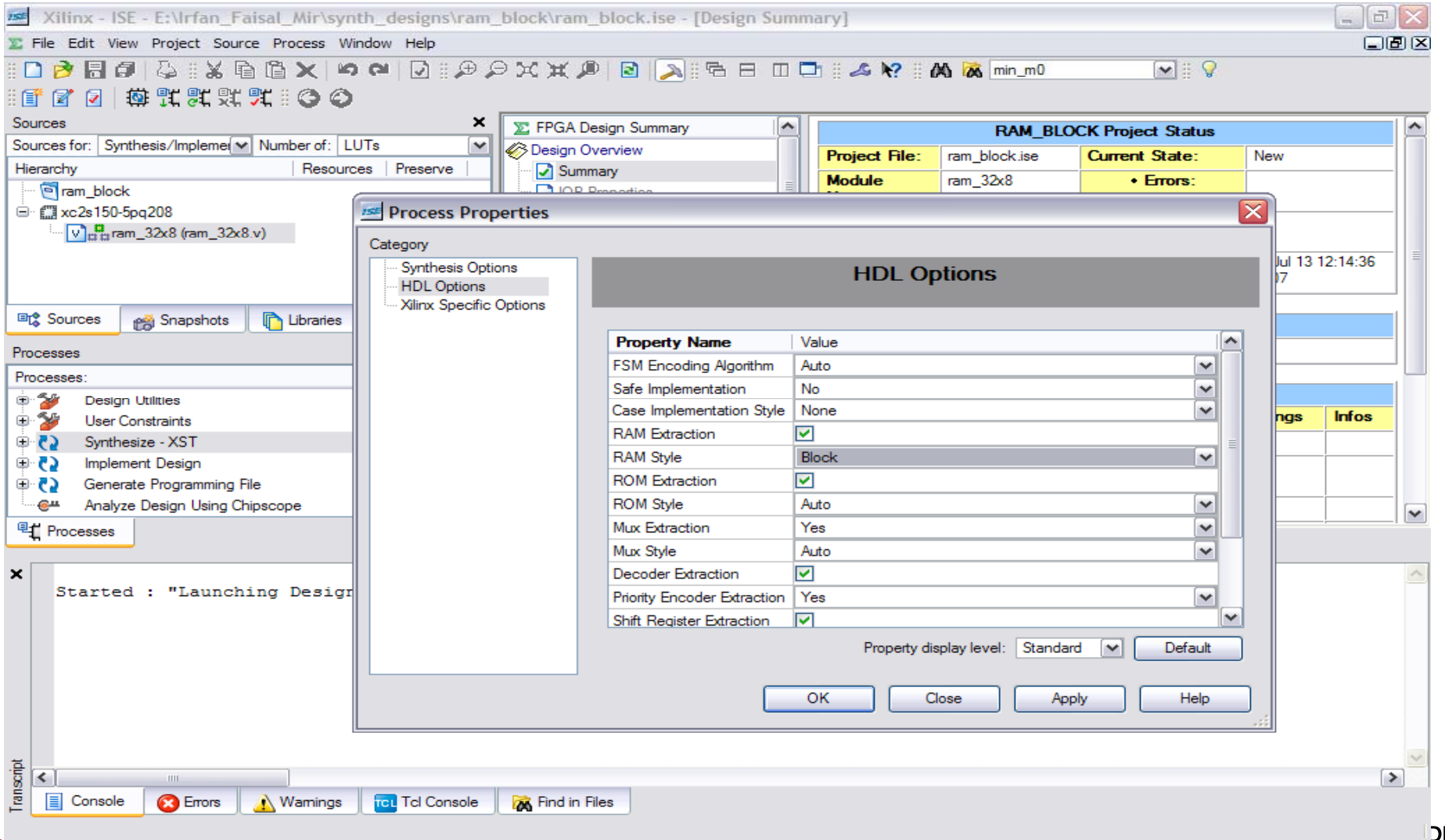

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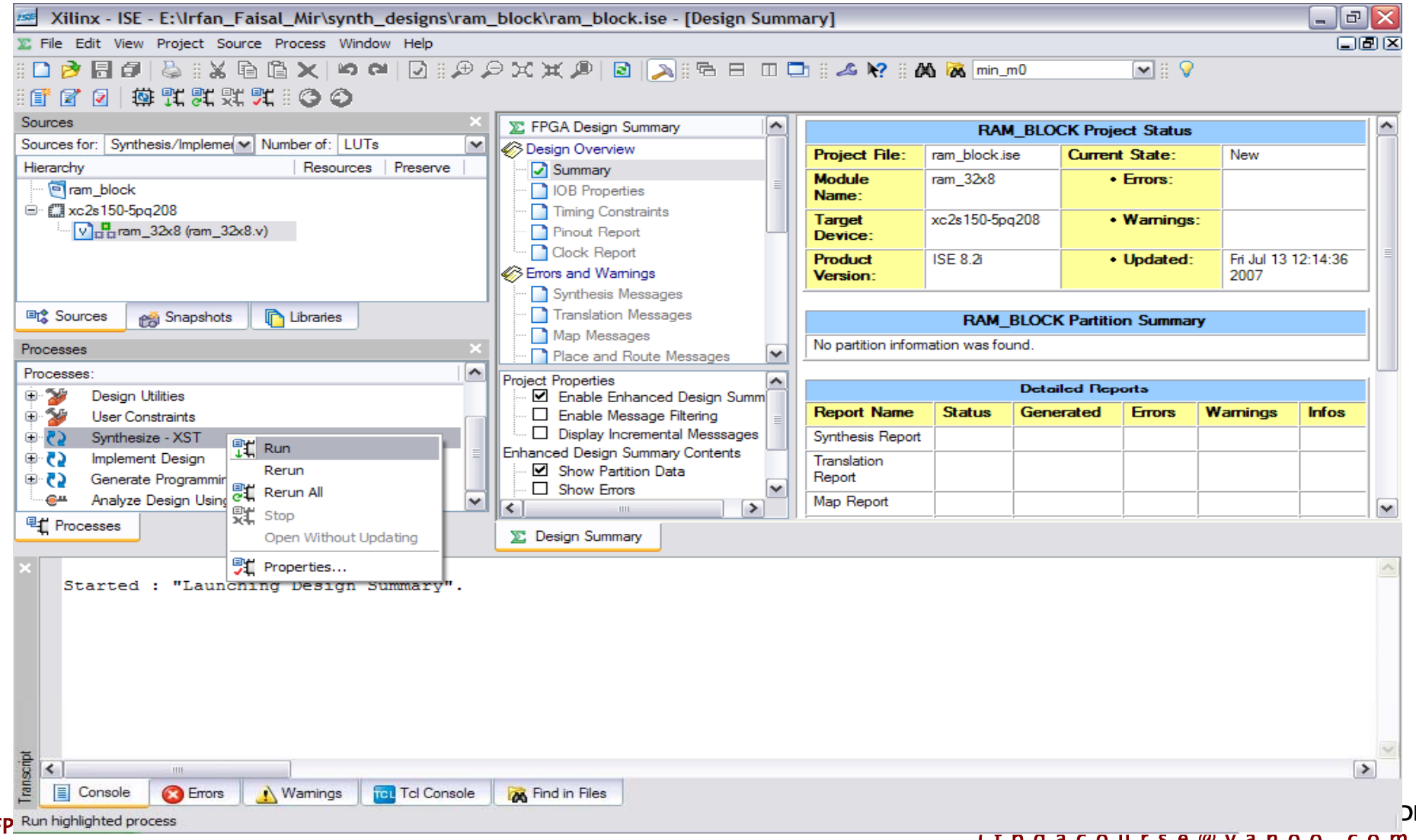
Design Example

- **Step4: Synthesis your design by using ISE 8.2i (Project Navigator)**
  - **Finally click on Run and synthesis flow will go on…**



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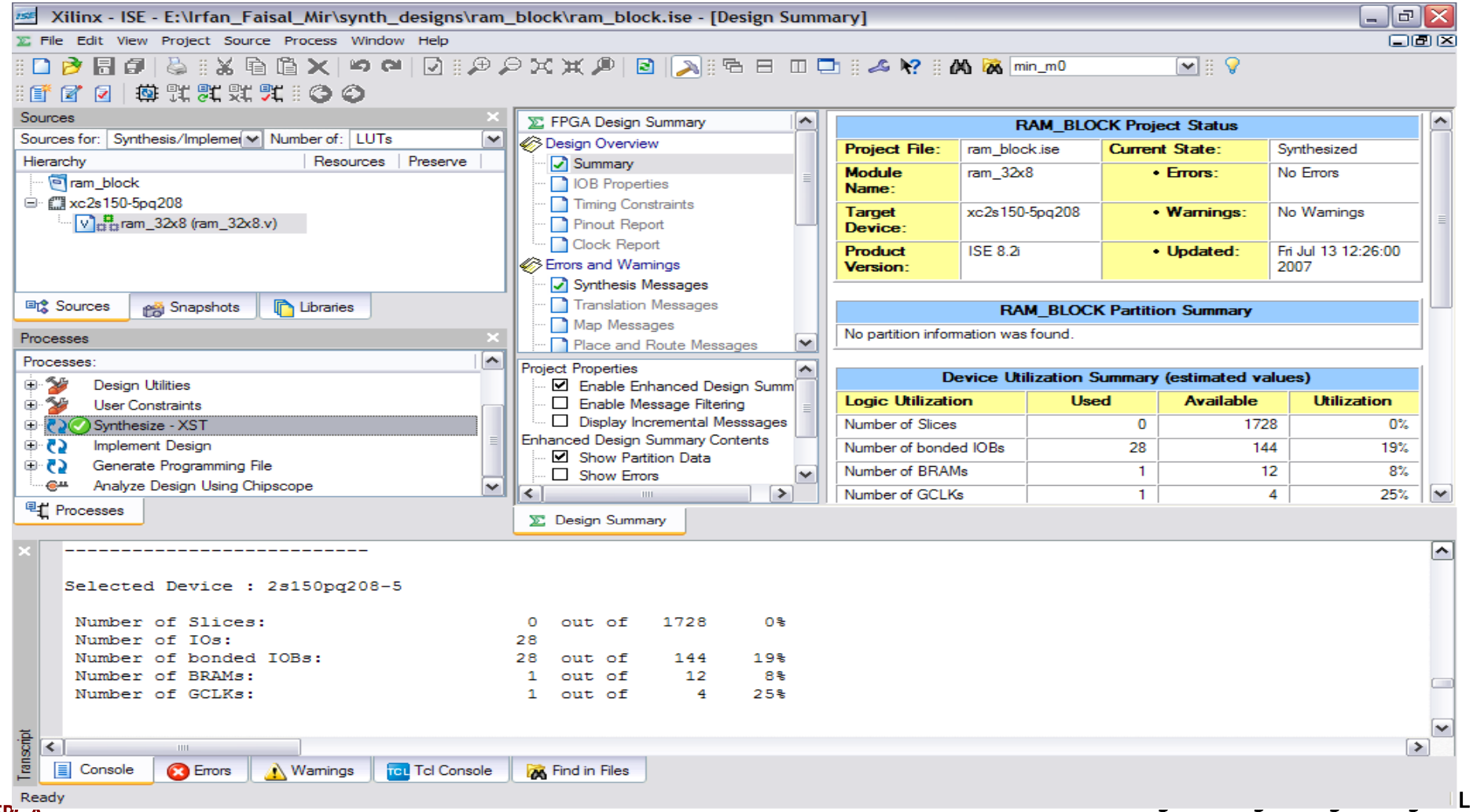
Design Example

- **Step4: Synthesis your design by using ISE 8.2i (Project Navigator)**
  - **At the end of synthesis process, it will show the PASS (✓) or FAIL (✗) indication…**



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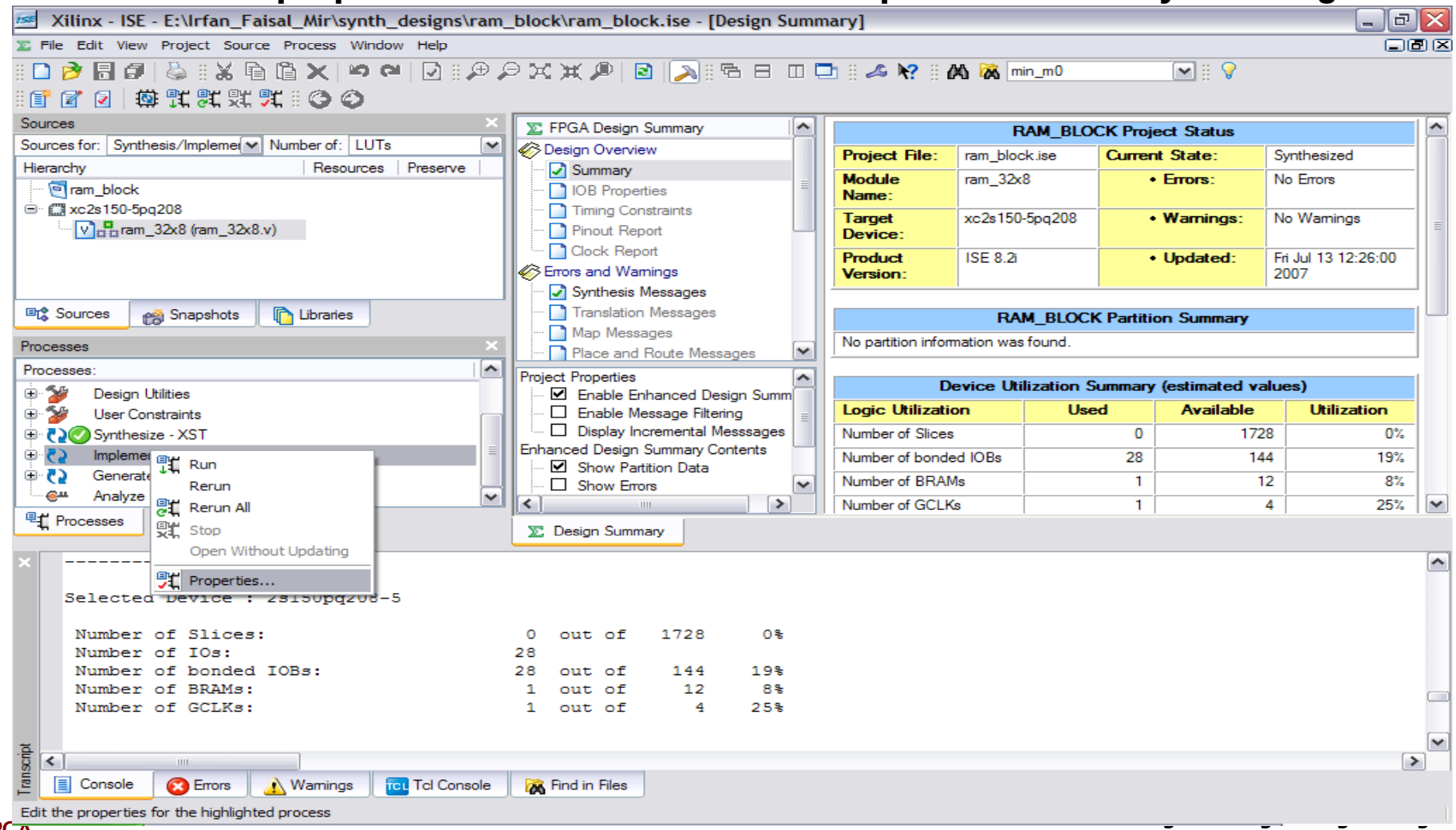
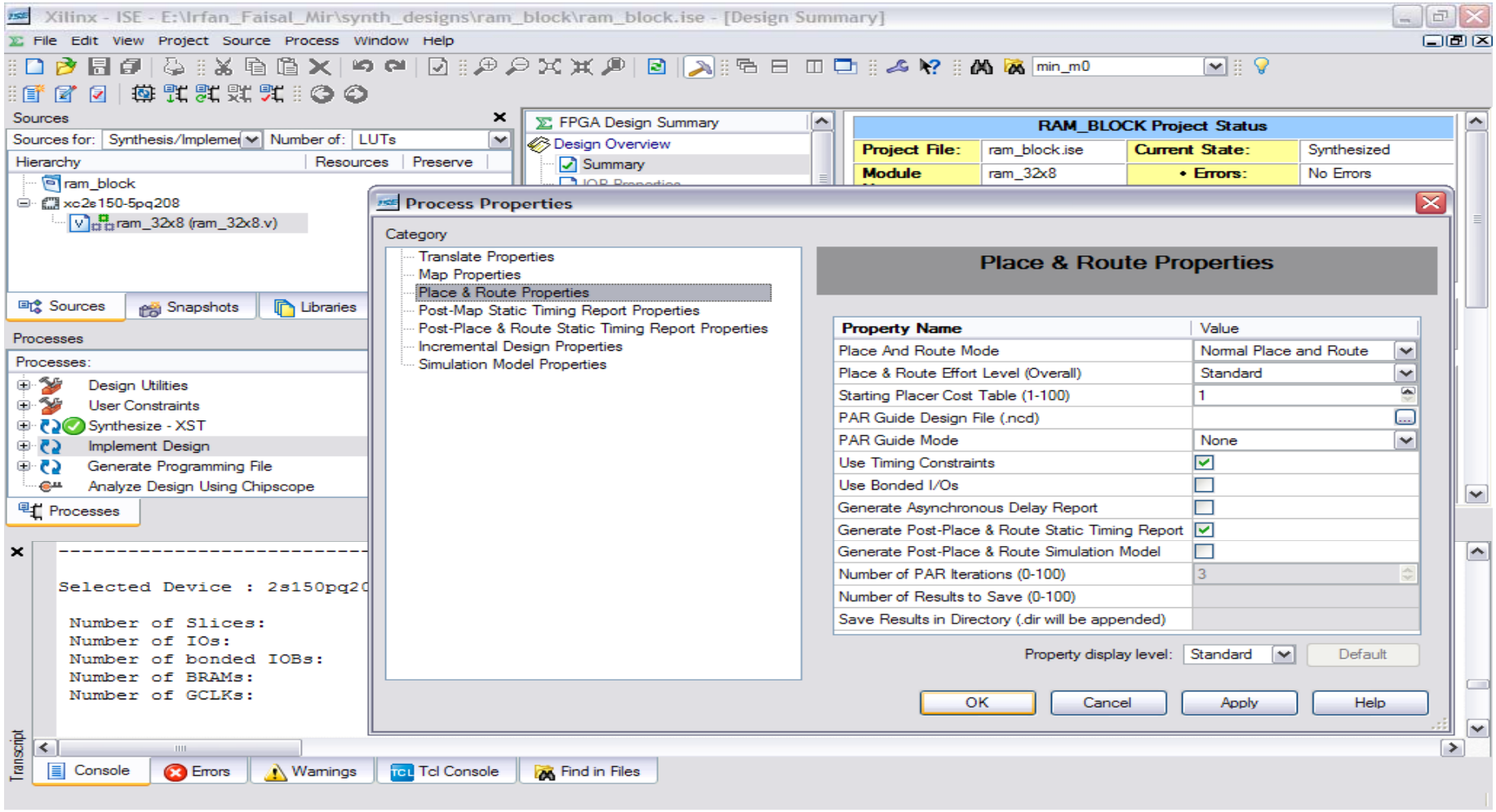
Design Example

- **Step5: Implement Design by using ISE 8.2i (Project Navigator)**
  - **Just right click on "Implement Design" in "Processes for Source" small window. View the properties…You can control the Implement flow of your design.**



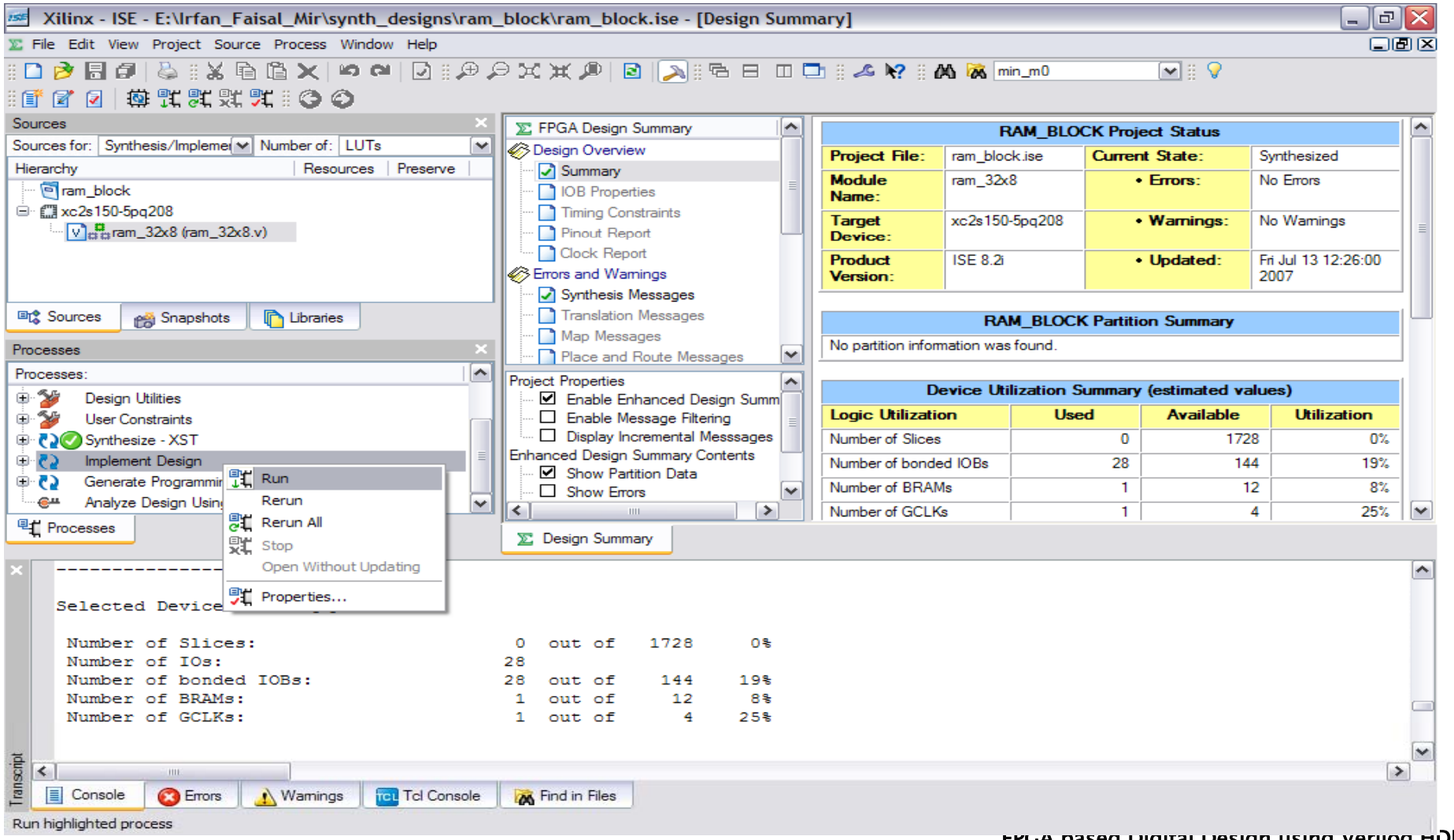
Design Example

- **Step5: Implement Design by using ISE 8.2i (Project Navigator)**
  - **Just right click on "Implement Design" in "Processes for Source" small window. View the properties…You can control the Implement flow of your design.**



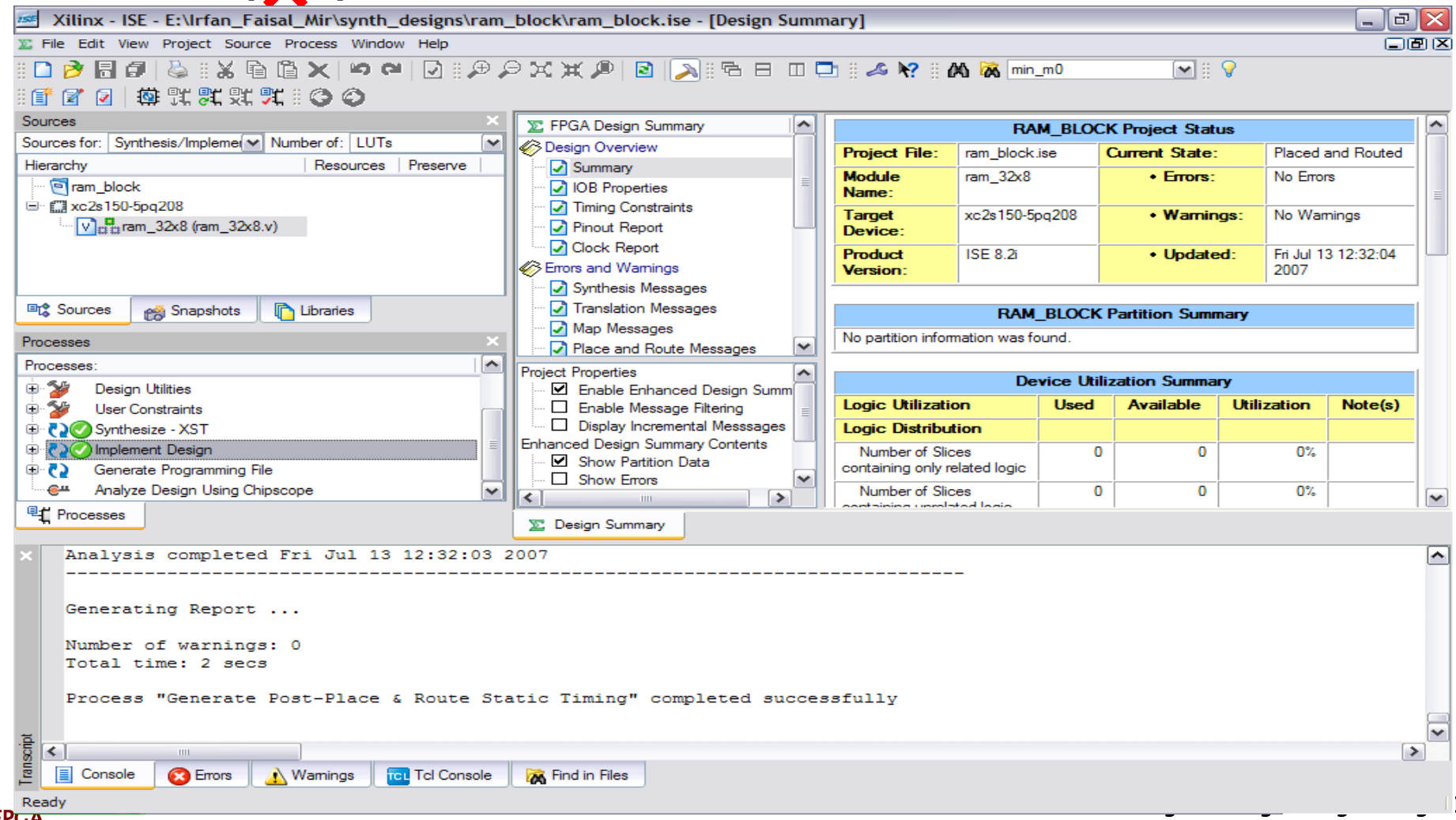
Design Example

- **Step5: Implement Design by using ISE 8.2i (Project Navigator)**
  - **Finally click on Run and Implementation flow will go on…**



Design Example

- **Step5: Implement Design by using ISE 8.2i (Project Navigator)**
  - **At the end of Implementation process, it will show the PASS (✓) or FAIL (✗) indication…**



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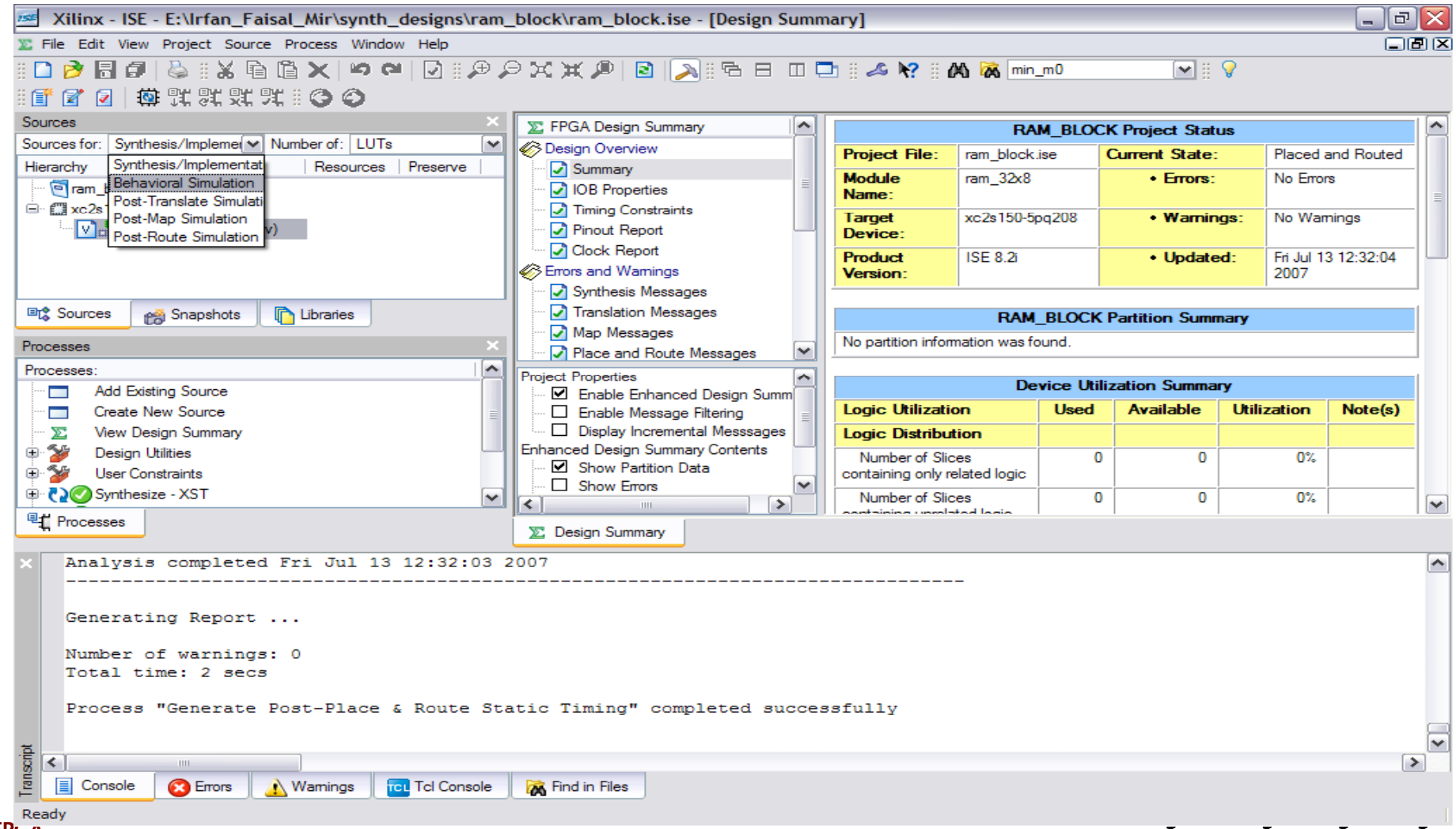
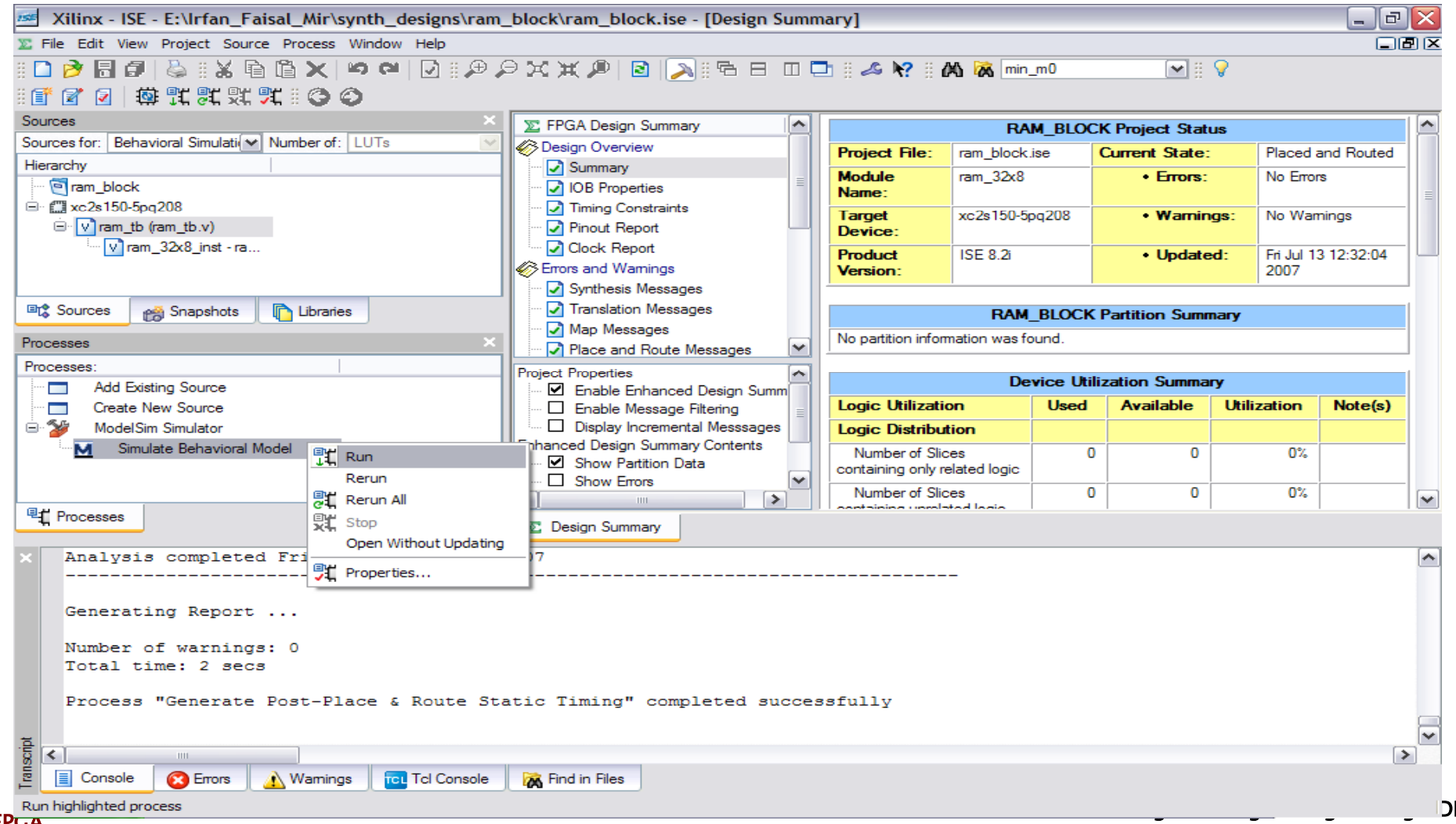
Design Example

- **Step6: Simulate Behavioral Model of your Design in ISE 8.2i (Project Navigator)**
  - **First highlight Behavioral Simulation option in "Sources in Project"…you will see ModelSim Simulator options in "Processes for Source" small window.**



Design Example

- **Step6: Simulate Behavioral Model of your Design in ISE 8.2i (Project Navigator)**
  - **First highlight Test Bench Top File in "Sources in Project"…you will see ModelSim Simulator options in "Processes for Source" small window.**



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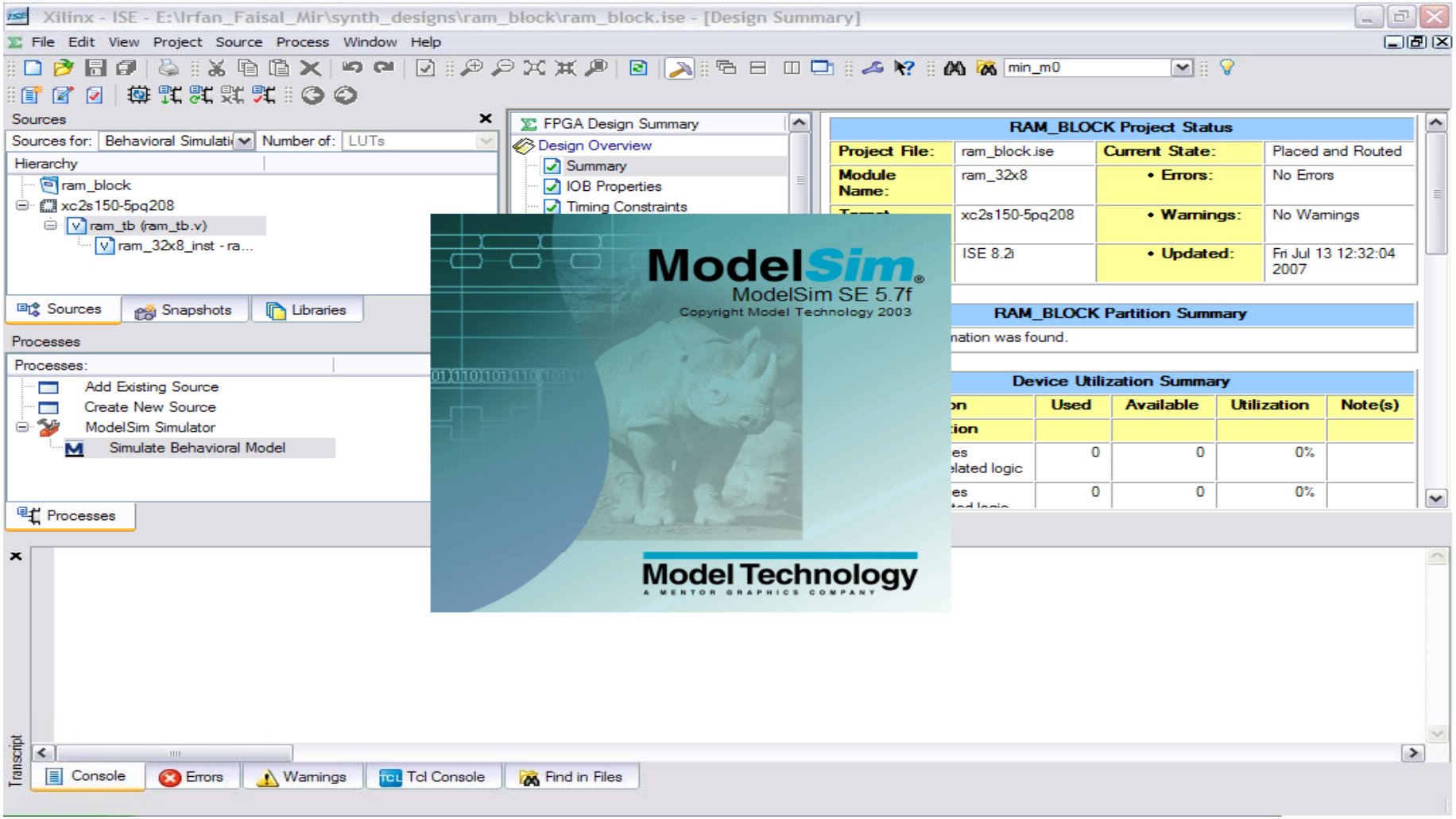
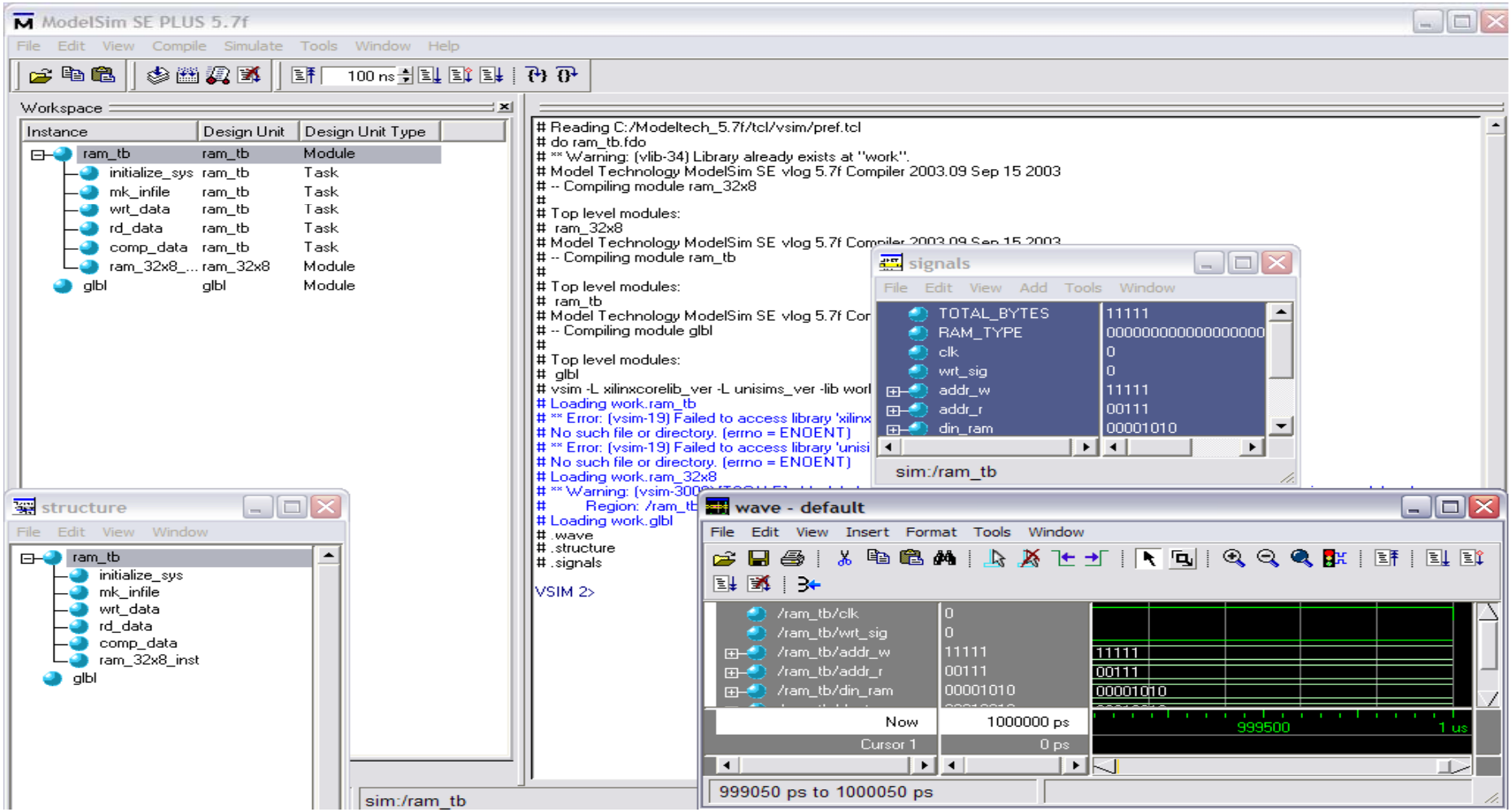
Design Example

- **Step6: Simulate Behavioral Model of your Design in ISE 8.2i (Project Navigator)**
  - **Now click on “Simulate Behavioral Model” in “Processes for Source” window.**



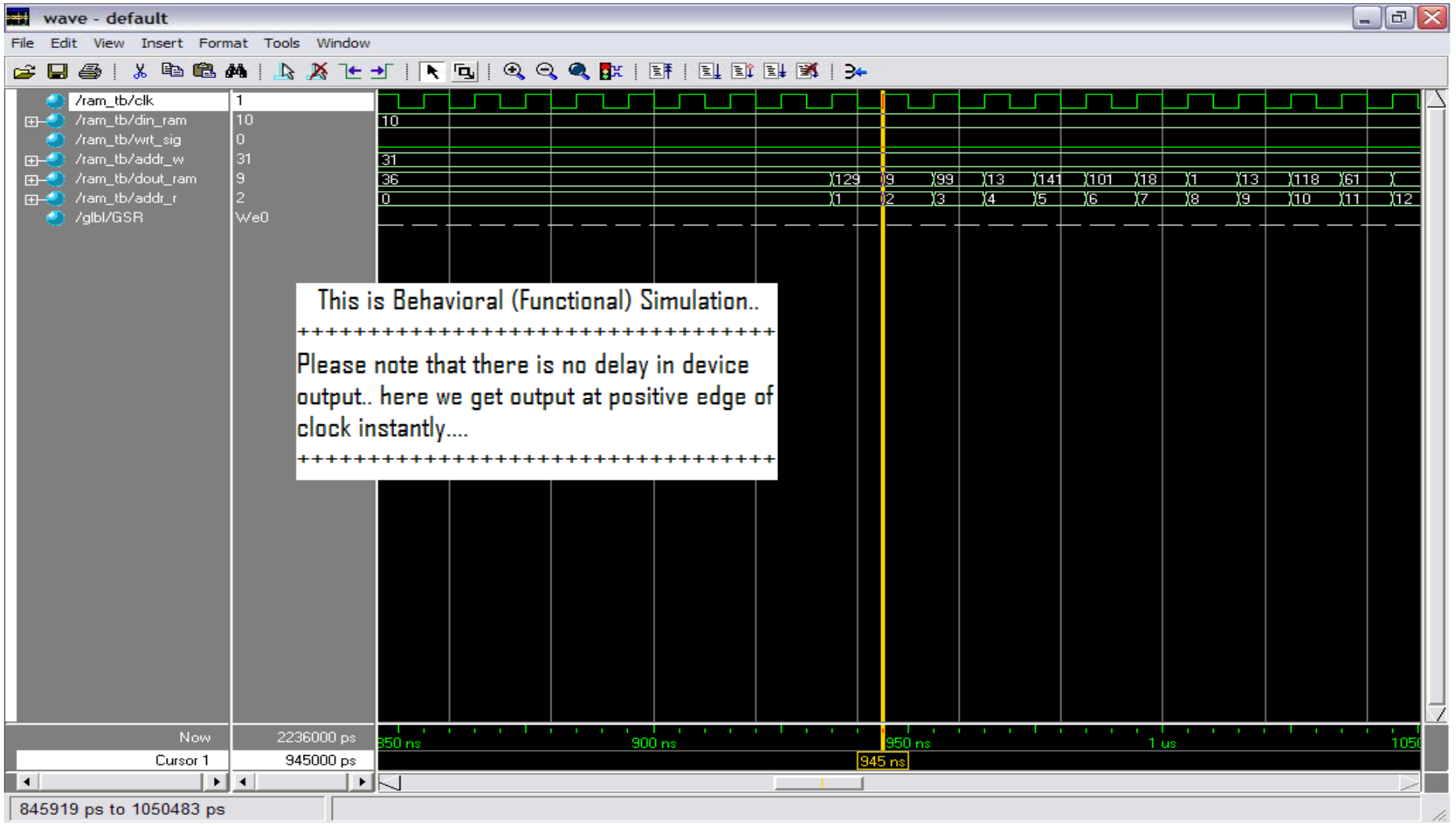
Design Example

- **Step6: Simulate Behavioral Model of your Design in ISE 8.2i (Project Navigator)**
  - **You see the ModelSim Simulator main window…Now you can verify your functional / RTL simulation.**



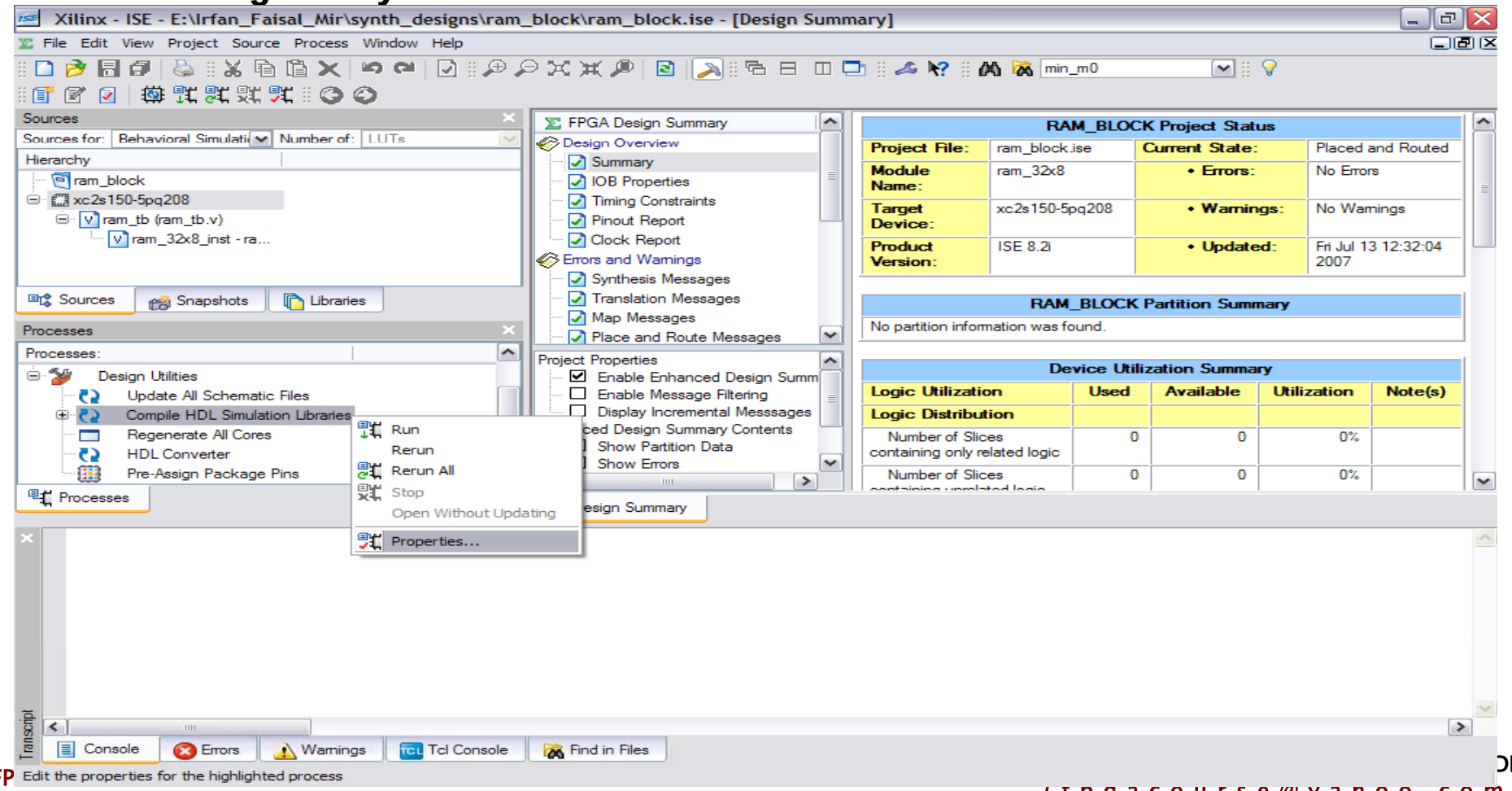
Design Example

- **Step6: Simulate Behavioral Model for Functional/RTL Simulation**
  - **You can verify your design by using Waveform Viewer in ModelSim…**



Design Example

- **Step7: Load Simulation Libraries before Timing Simulation in ISE 8.2i**
  - **First highlight project option (e.g xc150e-6pq208) in "Sources in Project" sub-window. You see "Design Entry Utilities" in "Processes for Source" sub-window. Now see the properties of "Compile HDL simulation Libraries" in "Design Entry Utilities" sub-menu.**



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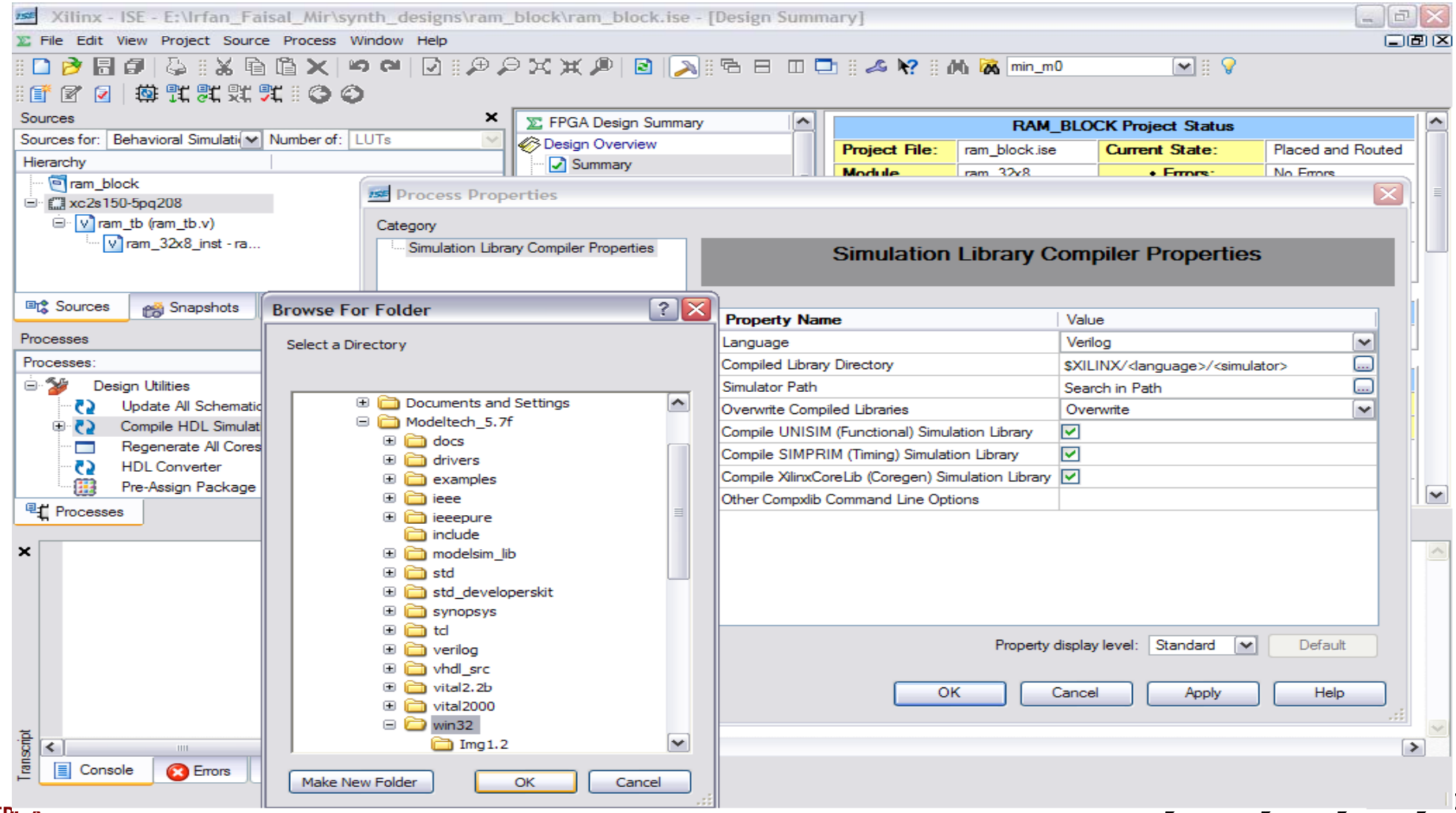
Design Example

- **Step7: Load Simulation Libraries before Timing Simulation in ISE 8.2i**
  - **In "Compile HDL Simulation Libraries" properties menu…select verilog option and give the path of "win32 folder" of ModelSim SE Simulator.**



Design Example

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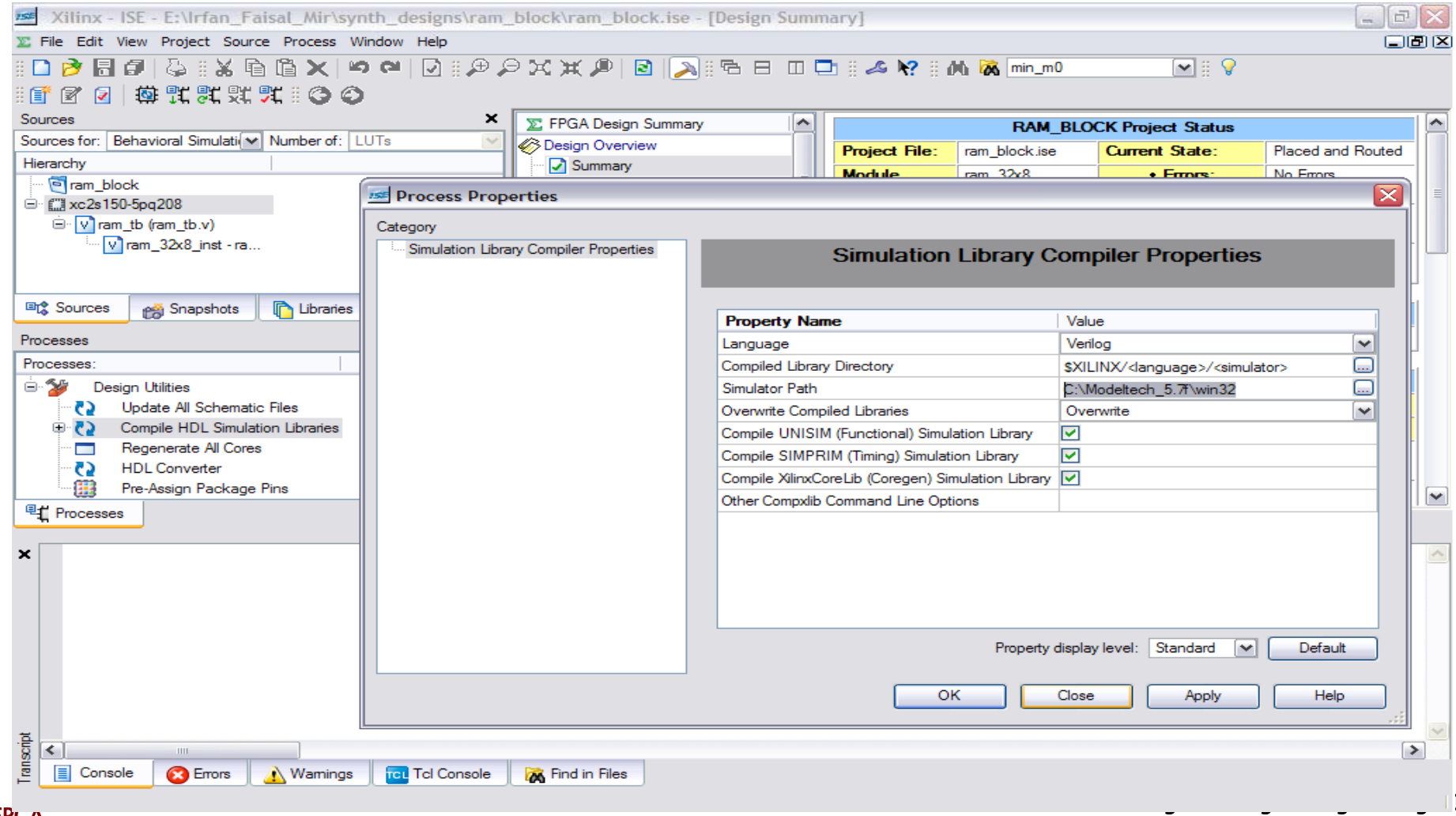

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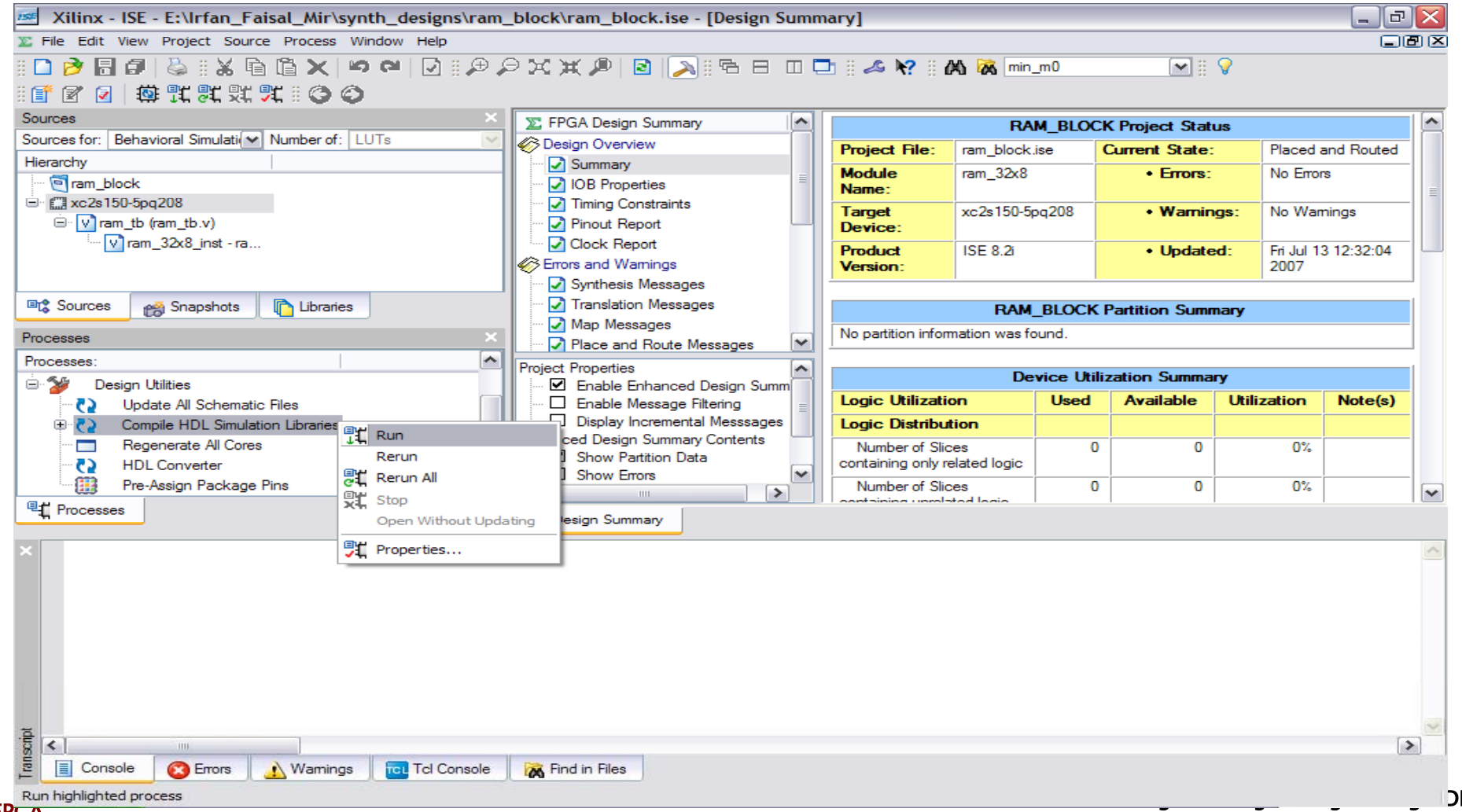
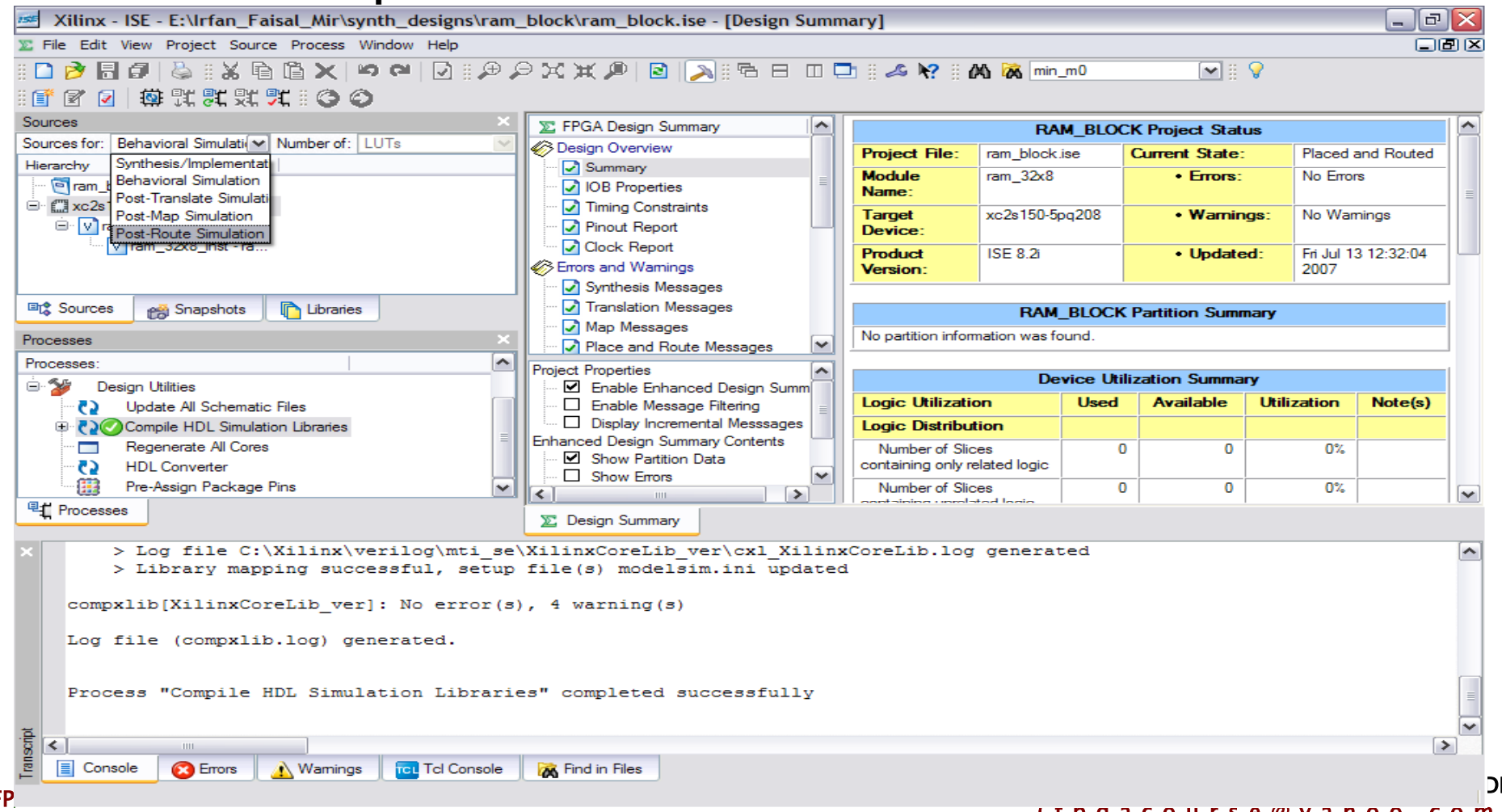
Design Example

- **Step7: Load Simulation Libraries before Timing Simulation in ISE 8.2i**
  - **Run the "Compile HDL Simulation Libraries"… It will compile "simprim, unisim, XilinxCoreLib libraries" in your current project.**



Design Example

- **Step7: Load Simulation Libraries before Timing Simulation in ISE 8.2i**
  - **At the end of "Compile HDL Simulation Libraries" process, it will show the PASS (✓) or FAIL (✗) indication… Then highlight Post-Route Simulation option in Sources window..**



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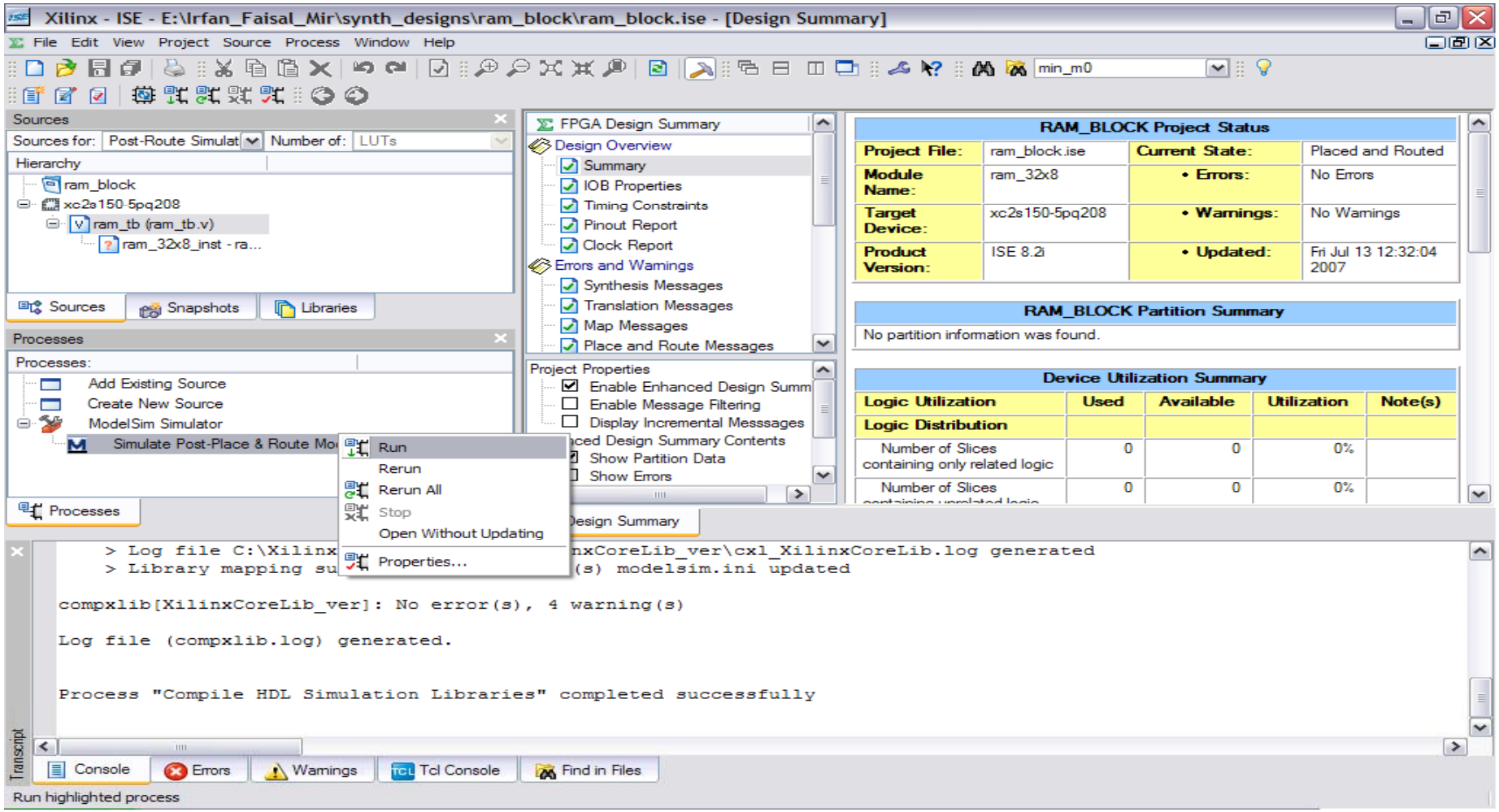
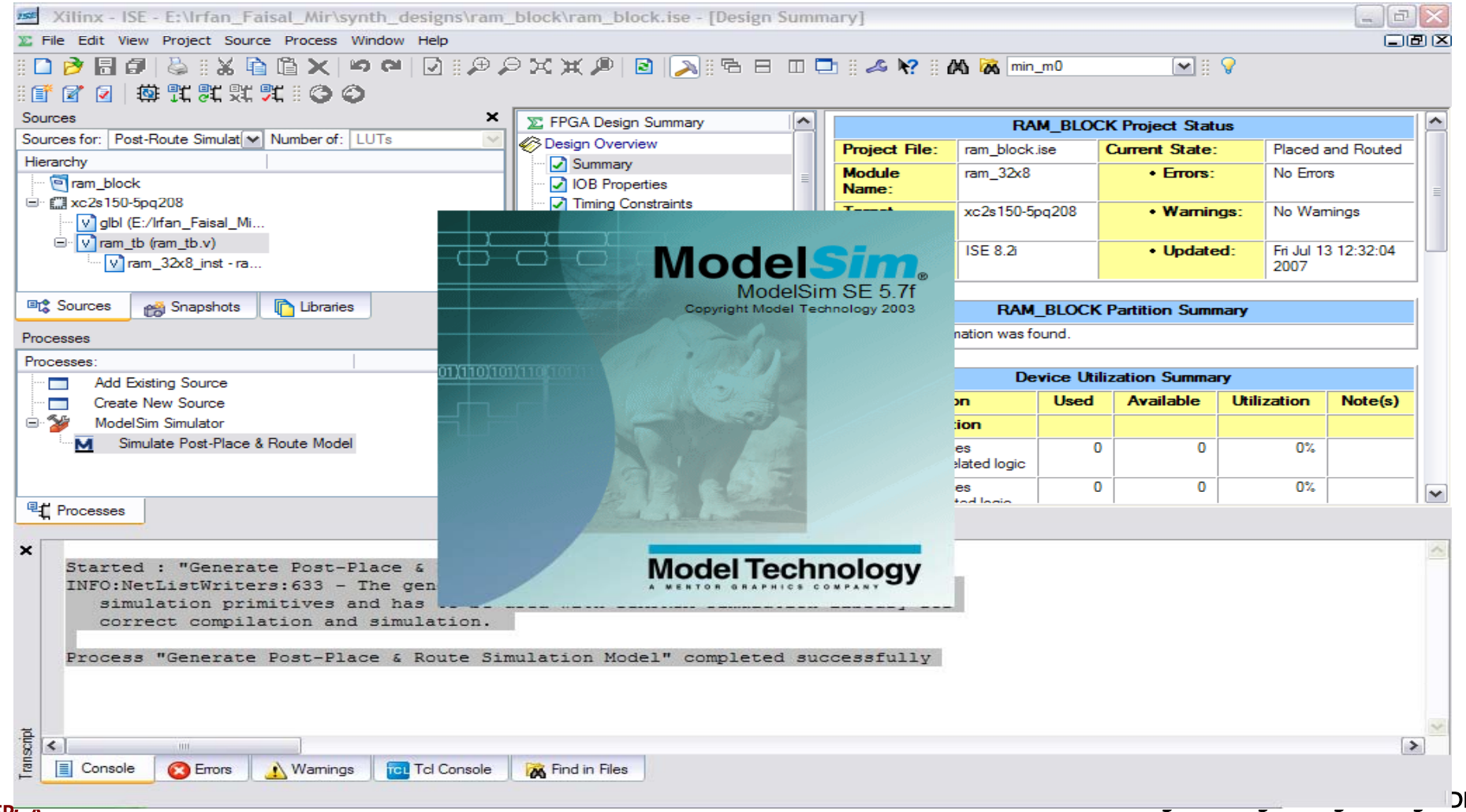
Design Example

- **Step8: Simulate Post-Place & Route Verilog Model of your Design in ISE 8.2i**
  - **First highlight Test Bench Top File in "Sources in Project"… you will see ModelSim Simulator options in "Processes for Source" small window.**



Design Example

- **Step8: Simulate Post-Place & Route Verilog Model of your Design in ISE 8.2i**
  - **Now Run the "Simulate Post-Place & Route Verilog Model" in "Processes for Source" small window.**



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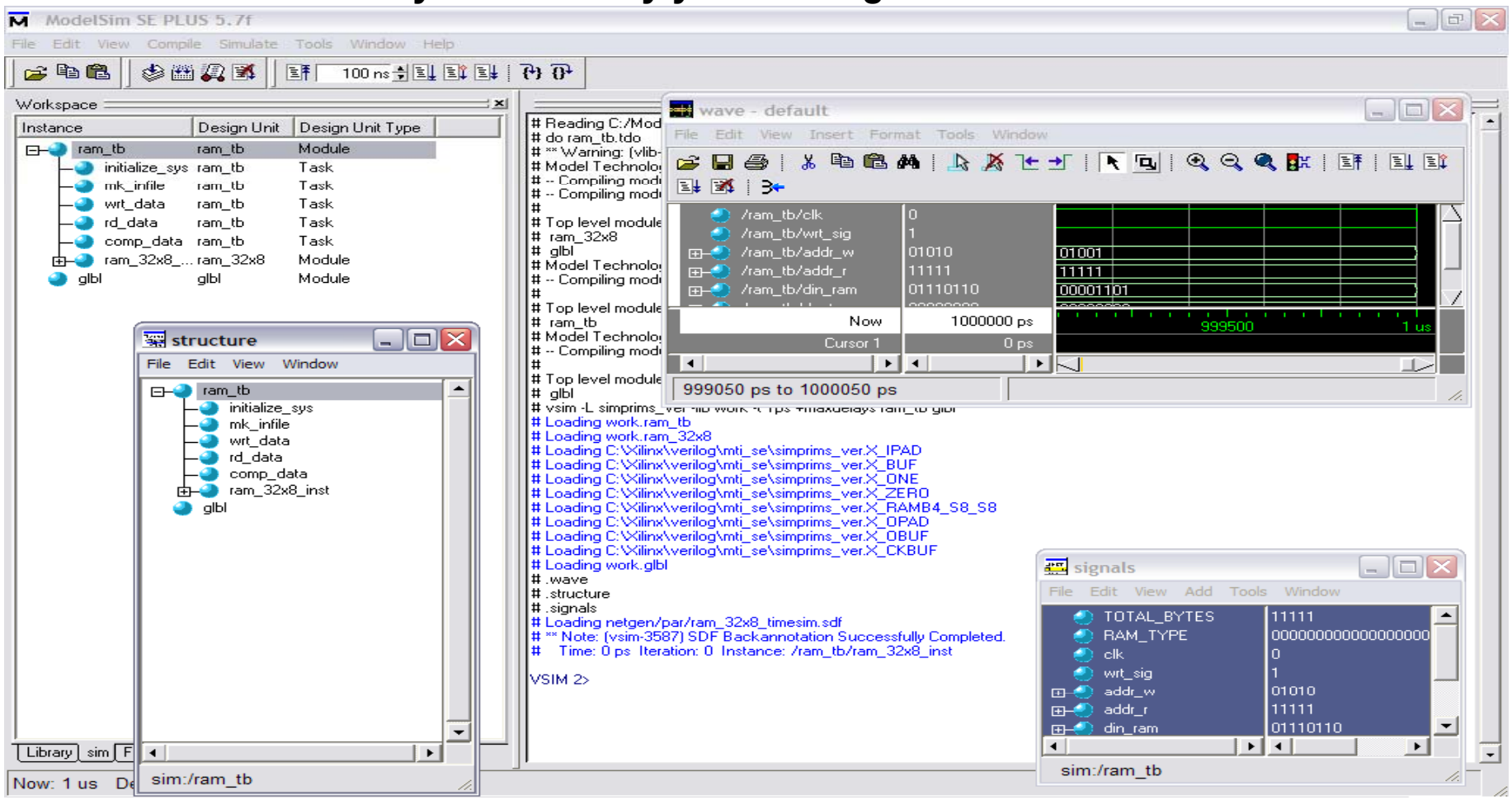
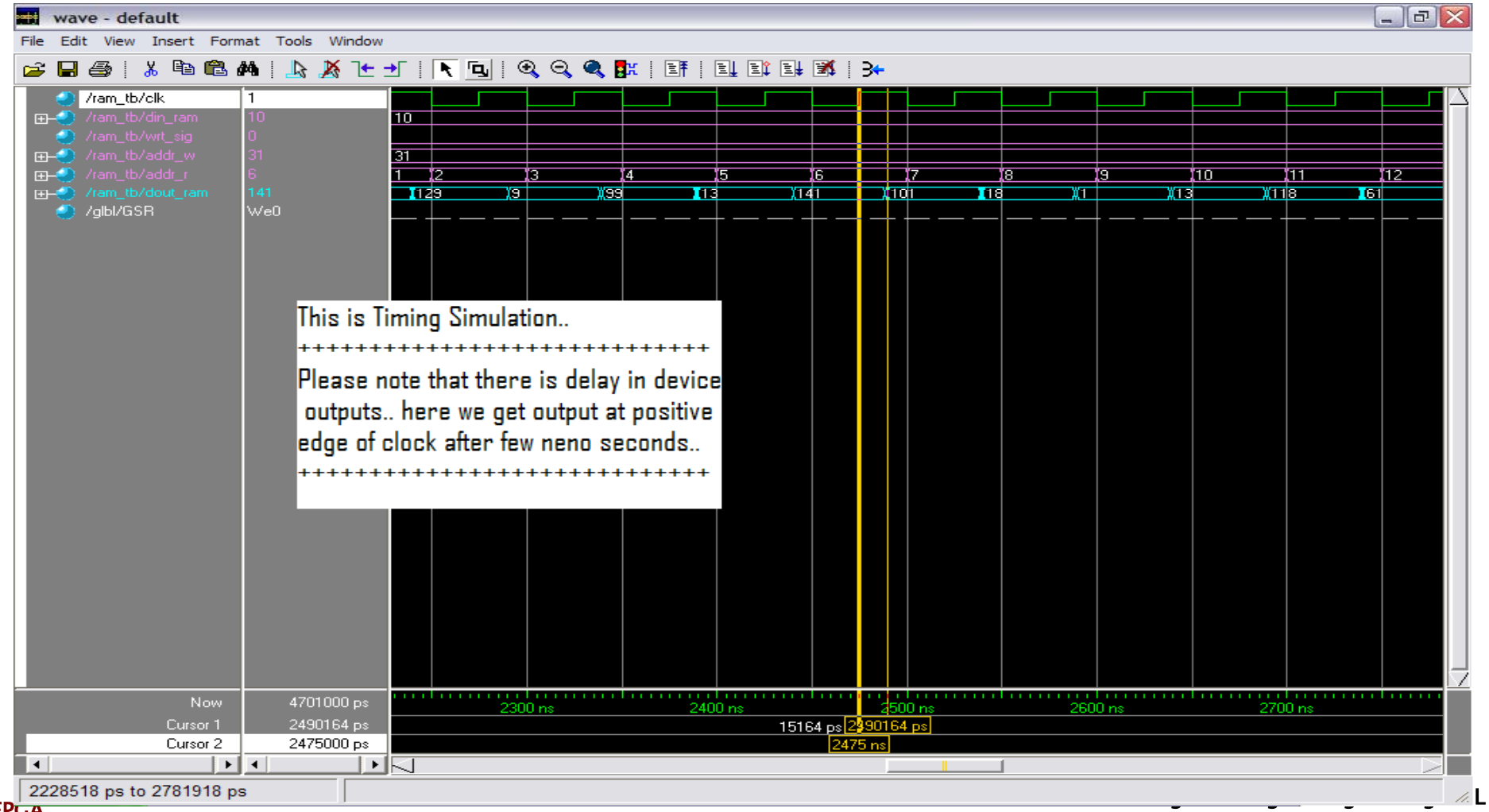
Design Example

- **Step8: Simulate Post-Place & Route Verilog Model of your Design in ISE 8.2i**
  - **You see the ModelSim Simulator main window…Be sure that "SIMPRIMS_VER" & "UNISIMS_VER" & "XILINXCORELIB_VER" Libraries are installed. Now you can verify your Timing simulation.**



Design Example

- **Step8: Simulate Post-Place & Route Verilog Model for Timing Simulation of your Design in ISE 8.2i**
  - **You can verify your design timing by using Waveform Viewer in ModelSim..**



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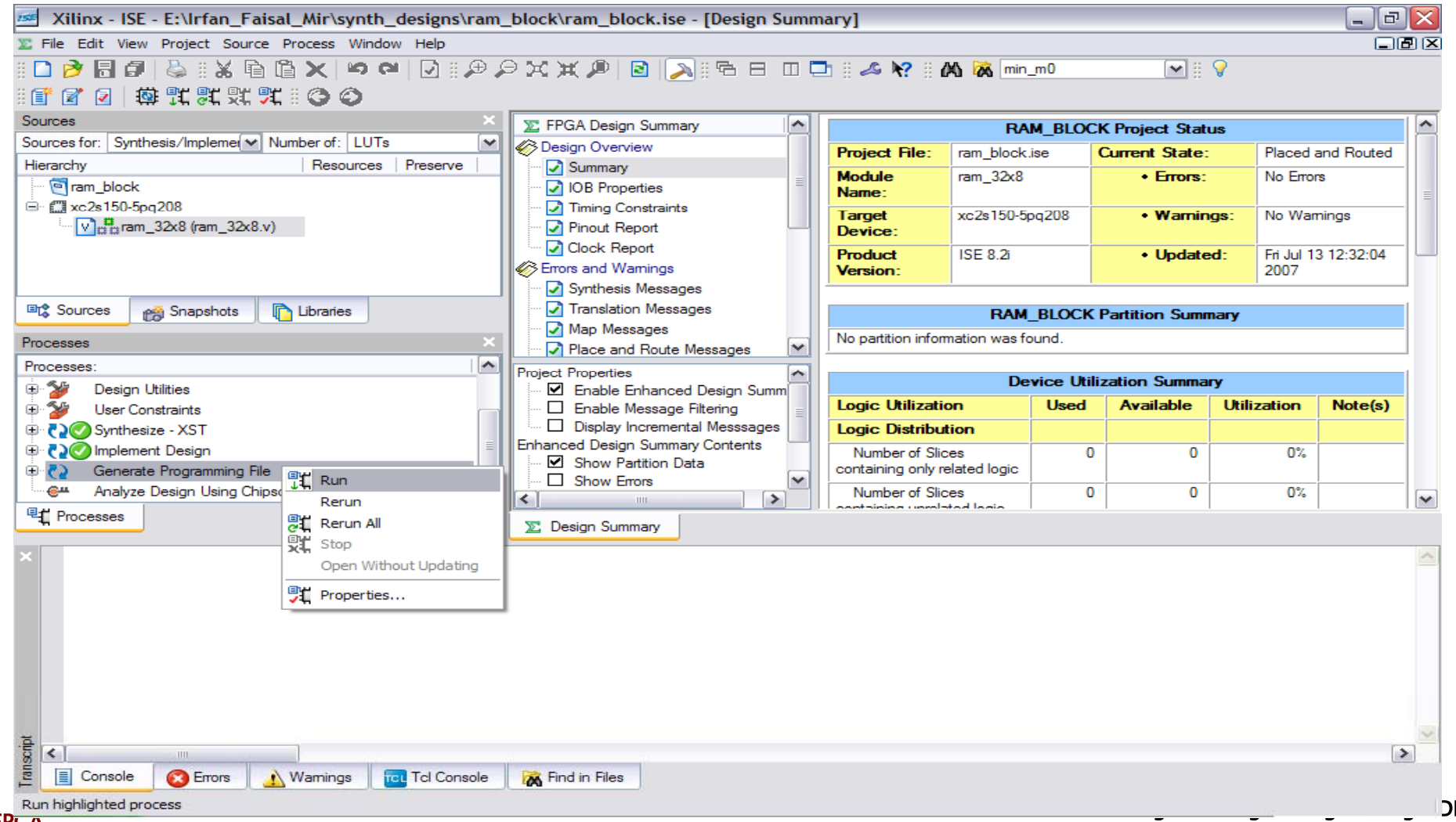
Design Example

- **Step9: Generate Programming File of your Design in ISE 8.2i**
  - **Click on “Run” option of “Generate Programming File” in “Processes for Source” small window. In “properties...” option, you can change its options.**



Design Example

- **Step9: Generate Programming File of your Design in ISE 8.2i**
  - **At the end of "Generate Programming File" process, it will show the PASS (✓) or FAIL (✗) indication…**