CHIP DESIGNING

(FPGA based Digital Design using Verilog HDL)

This course covers design simulation, verification/testing and synthesis/implementation of FPGA based digital systems using the standard Verilog hardware description language and Synthesis Tool. It also covers Digital Signal Processing (DSP) implementation in FPGAs and real-time debugging with Xilinx ChipScope Pro Tools.

This course is heavily ***Laboratory*** oriented in which the participants will be designed and evaluated digital circuits. Computer Aided Design (CAD) tools will be used for the experiments.

Course Outlines:

- Digital Design Methodology
- Verilog HDL with designing issues
- Introduction to VHDL and comparison with Verilog HDL
- Behavioral and RTL Design
- Optimized state machine based design
- Testing and Verification Methodology
- Xilinx FPGA/CPLD architecture
- Xilinx FPGA Design Flow
- Constraint Definitions and its analysis
- Digital Circuits Designed for specific FPGA
- Timing Analysis, Core Generator, Floor Planner, FPGA Editor
- Synthesis and implementation using ISE 8.2i
- DSP Implementation (Difference equations, Fix-point arithmetic, Q-format, FIR/IIR Filters, Multi-rate, Pipelining, transforms etc) in FPGAs
- System On Chip (SoC)
- FPGA configuration modes and in-depth study of FPGA based PCB
- Real time debugging for Xilinx FPGA by using ChipScope Pro Tools
- Hardware Testing of FPGA based Design on Xilinx training boards

Attention:

Already 350 Engineers/Scientists, mostly from Defense Organizations, have successfully completed this course under Skill Development Council (SDC), Govt. of Pakistan.

**** Opportunity for Fresh Engineers to improve their skills in High Tech field of Electronics..***

Note: *The above figures are stated at 26-05-2009*

Prerequisites

- → B.E Electronics / Electrical, Computer / IT Engineering, M.Sc Electronics / Computer Science (Students are warmly welcome…)
- → Basics of Digital Electronics and Microprocessor Fundamentals
- → Programming Basics (prefer C language)

- ✓ ***For More Information, feel free to contact at:***
  Ph. # 051-2224501-2

❖ Course Schedule

This training course is heavily ***Laboratory*** oriented in which the participants design and evaluate digital circuits. Computer Aided Design (CAD) tools are used for the experiments.

Duration	**72 Credits Hours (Six Weeks)**	
Lectures	Sixteen (16)	1.5 hrs per lecture
LABs	Twenty (20)	2.5 hrs per lab

Table: Course duration

Note: The Lecture/LAB contents may slightly change during the course.

1st. Week

DAY	TIME	TOPIC	TIME	LAB WORK
1	**1.5 hrs**	1. Course Introduction. 2. Design Methodology, Digital Design Objective, Combinational & Sequential Design Basics, Clock Methodology, Critical & Cycle Time	**2.5 hrs**	→ ModelSim Tool Training
2	**1.5 hrs**	1. Verilog HDL Basics, Verilog Value Set, Numbers in Verilog, Net, Register & Vectors, Arrays, Memories, Parameters, Strings, System tasks, Compiler Directives In Verilog 2. Abstraction Levels (Switch, Gate, Dataflow & Behavioral), Modules & Ports, Module instances, Hierarchal Design Concept, Gate Level Modeling using Examples	**2.5 hrs**	→ Simulation of 1-bit ADDER/SUB using Gate Level & Data Flow Level in ModelSim → Simulation of 1-bit MUX/DEMUX using Gate Level & Data Flow Level in ModelSim → Simulation of 4-bit MUX/DEMUX using 1-bit in ModelSim
3	**1.5 hrs**	1. Continuous Assignment, Port Assignments, Operators (Logical, Bitwise, Reduction, Shift, Concatenation, Relational, Equality, Conditional, Arithmetic) 2. Behavioral Modeling, Procedural Blocks (initial, always)	**2.5 hrs**	→ Simulation of 4-bit ADDER/SUB using bit in ModelSim → Simulation of implementation of Timing Diagrams, D-FF/Register and 4-bit Ripple Carry Counter in ModelSim

2nd. Week

DAY	TIME	TOPIC	TIME	LAB WORK
1	**1.5 hrs**	1. Blocking & Non-Blocking Assignments, Clock & Async / Sync Reset in Digital System Events, Combinatorial Statements, Timing Analysis, Delays 2. Procedural Statements (if, case/casex/casez, for, while, repeat, forever), Mixed abstraction modeling	**2.5 hrs**	→ Design a Single/Dual Clock RAM and simulate in ModelSim → Design a FIFO and simulate in ModelSim
2	**1.5 hrs**	1. Test Bench Concept, Formation of Test Bench, File Handling, Tasks, Functions, Test Drivers / Vectors, Built-in-Self-Test (BIST), Boundary Scan Testing 2. System Tasks, Compiler Directives, Parameters/Define Statements	**2.5 hrs**	→ Generate random data & use File Handling using Tasks to improve testability by using ModelSim
3	**1.5 hrs**	1. Digital Systems, State Machine Concept, Moore & Mealy State Machines based Design, One Hot State Machine 2. State machine based memory Controller	**2.5 hrs**	→ Design a Traffic Controller by using state machine and Simulate in ModelSim → Design a UART Transmitter by using state machine and Simulate in ModelSim

3rd. Week

DAY	TIME	TOPIC	TIME	LAB WORK
1	**1.5 hrs**	1. Behavioral/RTL Coding Techniques (Synchronous / Asynchronous Design, Race Condition, Delay Dependent Logic, Glitches, Hold Time Violations, Gated Clocking, Metastability), Simulation / Synthesis Issues	**2.5 hrs**	→ Design an ADC Interface with FPGA and Simulate in ModelSim
2	**1.5 hrs**	1. Behavioral/RTL Coding Techniques 2. RTL Coding Guidelines	**2.5 hrs**	→ Design a DAC Interface with FPGA and Simulate in ModelSim
3	**1.5 hrs**	1. Introduction of FPGA & CPLD, FPGA & CPLD basics, Xilinx FPGA series, FPGA Technology, FPGA advantages, FPGA variations, FPGA Configurable Logic Blocks (CLBs), LUT Implementation in CLBs, FPGA IO Blocks 2. Xilinx XC4000 & Spartan Series FPGA internal architecture	**2.5 hrs**	→ Design a DSP Processor (Ti TMSC64x) Interface with FPGA and Simulate in ModelSim → Design a UART Receiver by using state machine and Simulate in ModelSim

4th. Week

DAY	TIME	TOPIC	TIME	LAB WORK
1	**1.5 hrs**	1. Xilinx FPGA Design Process, Synthesis Flow (Xilinx Synthesis Technology), 2. Core Generator	**2.5 hrs**	→ Xilinx ISE Tool Training (Overview with Synthesis, Implementation and Configuration) → Generate a Block RAM for FIFO by using ISE 8.2i Core Generator
2	**1.5 hrs**	1. Timing Simulation 2. Implementation Flow (Translate, MAP and Place & Route), Constraint Editor, Functional / Timing Verification, Floor Planner, FPGA Editor, Configuration Flow (configuration modes), EPROM File Formatter, iMPACT tool basics	**2.5 hrs**	→ Timing Simulation of Dual Clock RAM (with Block & Distributed) → Use Constraints Editor , iMPACT tool, mcs, bit file generation
3	**1.5 hrs**	1. Concepts of Digital Signal Processing (DSP) in Field Programmable Gate Array (FPGA)	**2.5 hrs**	→ Design a 4-Tap FIR Filter and Simulate in ModelSim → Use pipelining for increasing design frequency

5th. Week

DAY	TIME	TOPIC	TIME	LAB WORK
1	**1.5 hrs**	1. Concepts of Digital Signal Processing (DSP) in Field Programmable Gate Array (FPGA) 2. DLL blocks in FPGAs	**2.5 hrs**	→ Training Board Description and Flasher on FPGA Training Kit → UP & DOWN Counter and 7-Segment Display Panel Interface on FPGA Training Kit
2	**1.5 hrs**	1. Introduction to configuration, Xilinx PROM, OTP & In System Programmable, Configuration Modes, Master Serial Mode, Slave Serial Mode, SelectMap Mode, JTAG or Boundary Scan Mode 2. Configuration Modes, Master Serial Mode, Slave Serial Mode, SelectMap Mode, JTAG or Boundary Scan Mode	**2.5 hrs**	→ LCD Interface with FPGA Training Kit → Traffic Controller on FPGA Training Kit → ADC and DAC Interface with FPGA Training Kit
3	**1.5 hrs**	1. UART-transmitter on FPGA Development Board	**2.5 hrs**	→ UART-Receiver on FPGA Development Board

6th. Week

DAY	TIME	TOPIC	TIME	LAB WORK
1	**1.5 hrs**	1. Real-time debugging for Xilinx FPGA by using Xilinx ChipScope Pro Tools	**2.5 hrs**	→ Monitor internal signals of UART core by using ChipScope
2	**1.5 hrs**	1. System-on-Chip Concept 2. New Trends in VLSI Industry	**2.5 hrs**	→ Monitor internal signals of UART Core by using ChipScope
3	**1.5 hrs**	Case Study	**2.5 hrs**	→ Case Study