

Training Course
on

FPGA based Digital Design using Verilog HDL



By

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*** *Organized by* Skill Development Council,**
(*Ministry of Labour, Manpower and overseas Pakistani*)
Govt. of Pakistan.

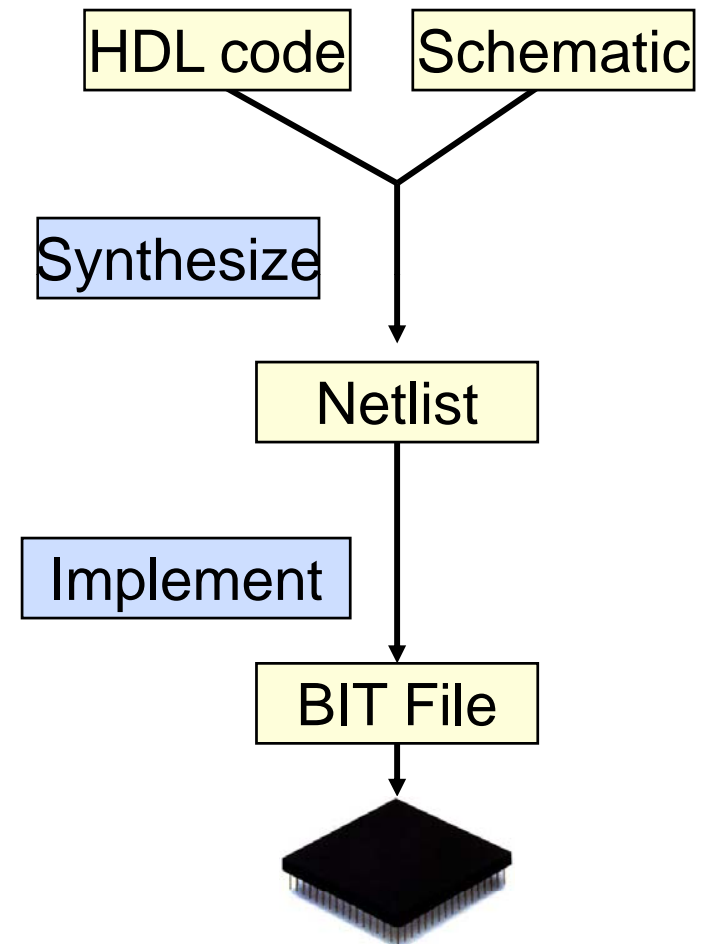
Xilinx FPGA Design Process (i)

➤ Step1: Design

- Two design entry methods:
HDL(Verilog or VHDL) or
schematic drawings

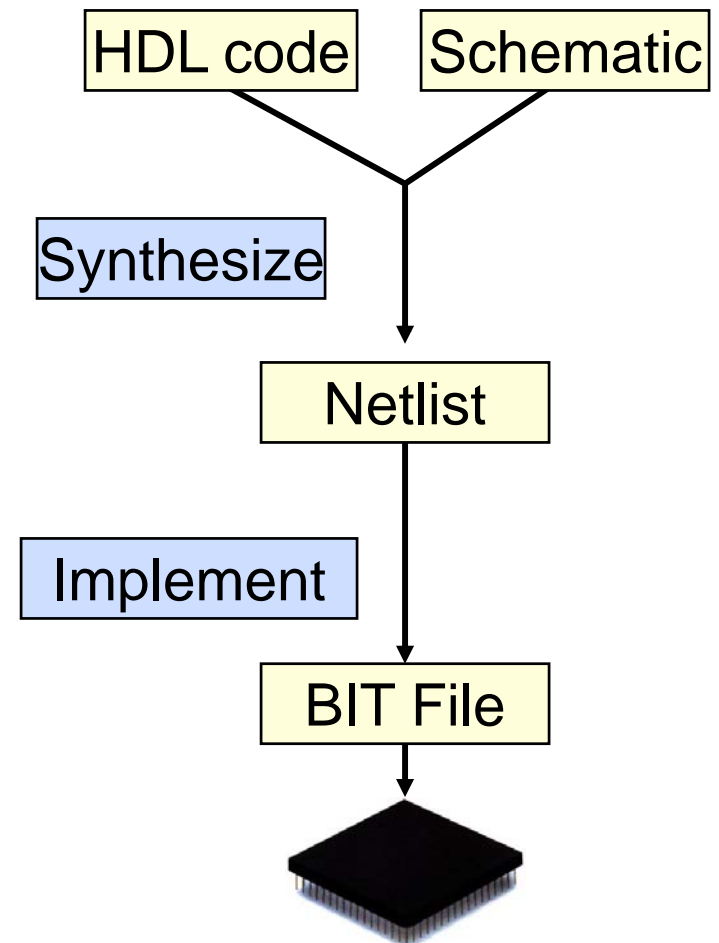
➤ Step 2: Synthesize to create Netlist

- Translates V, VHD, SCH files
into an industry standard
format EDIF file



Xilinx FPGA Design Process (ii)

- **Step 3: Implement design (netlist)**
 - Translate, Map, Place & Route
- **Step 4: Configure FPGA**
 - Download BIT file into FPGA

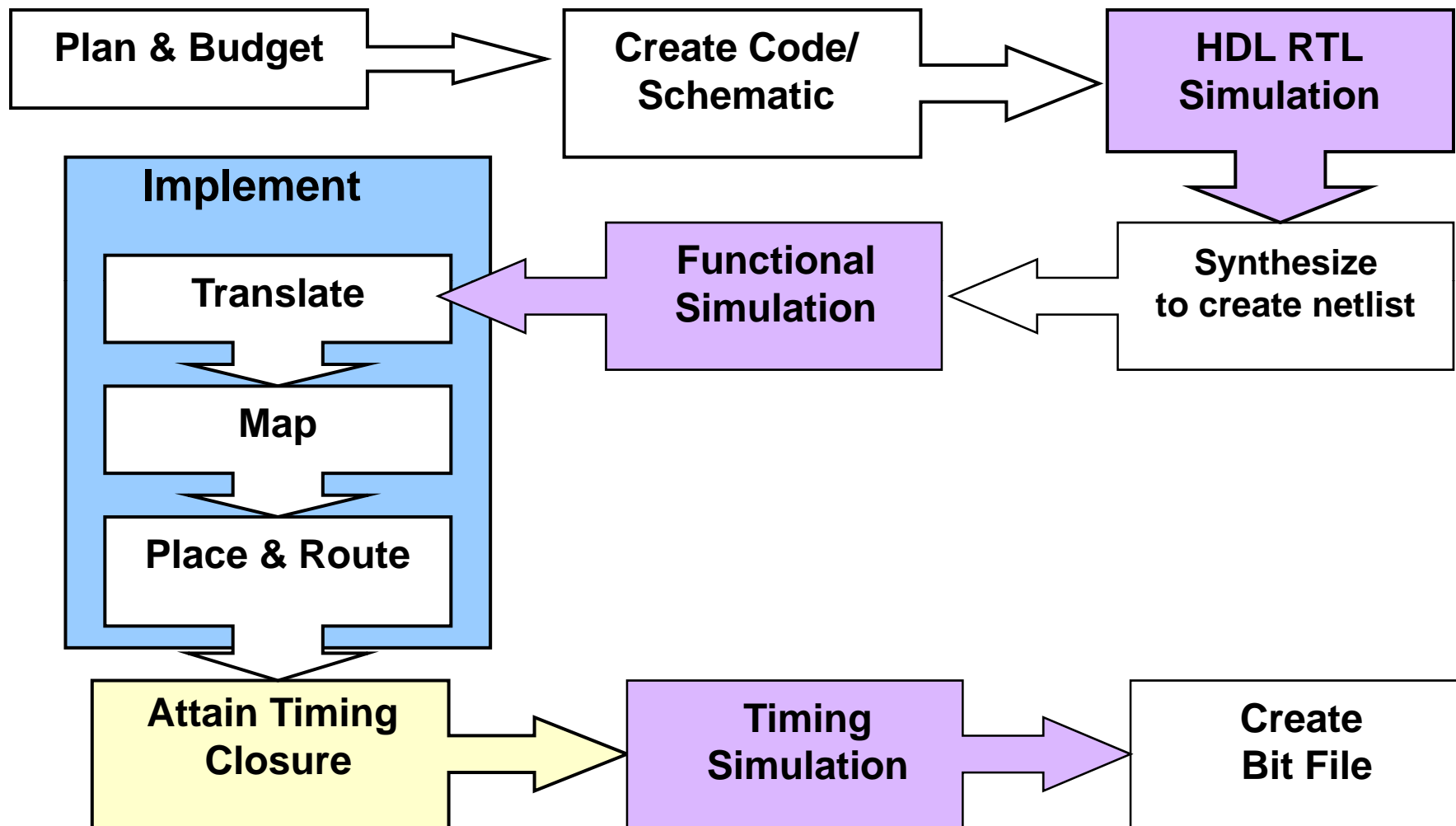


Software use for Synthesis, Implementation and Configuration

- *Foundation Series ISE*
(Integrated Software Environment)
- *For PC platforms:*
Win98, Win2000/Xp,
and NT4.0
- *For UNIX platforms:*
HP and Solaris



Xilinx Design Flow



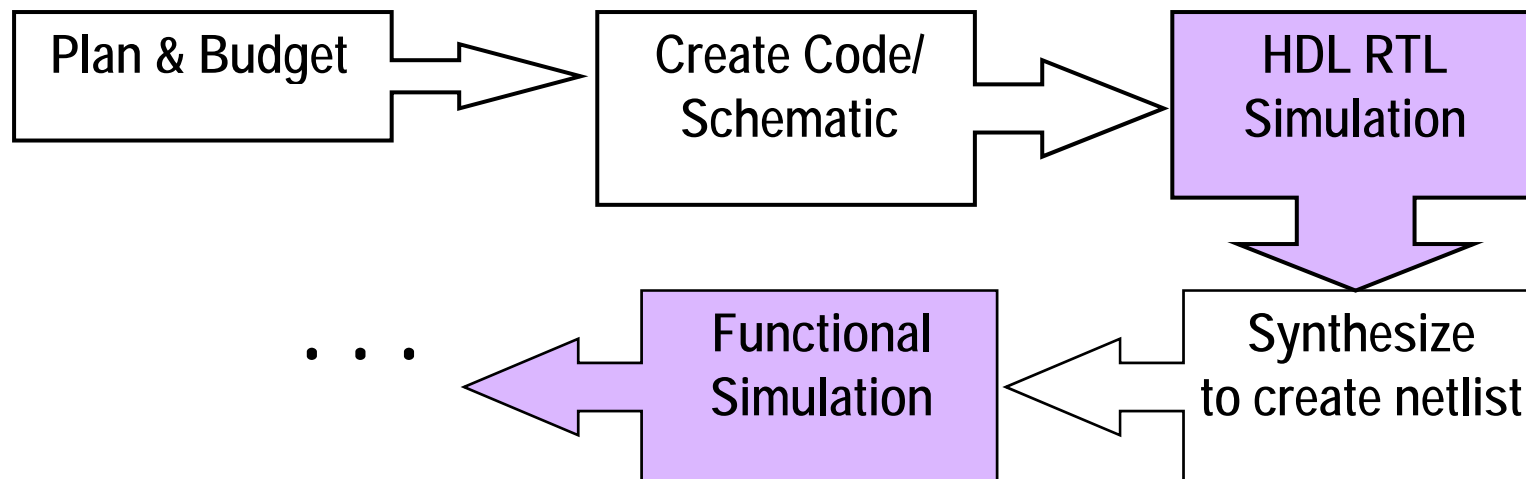


Design Entry in Xilinx ISE

- **Plan & Budget:** First you should plan and define budget
- **Two design entry methods:** HDL or schematic
 - Core Generator available to assist design entry
- Whichever method you use, you will need a tool to generate an EDIF netlist to program a Xilinx FPGA

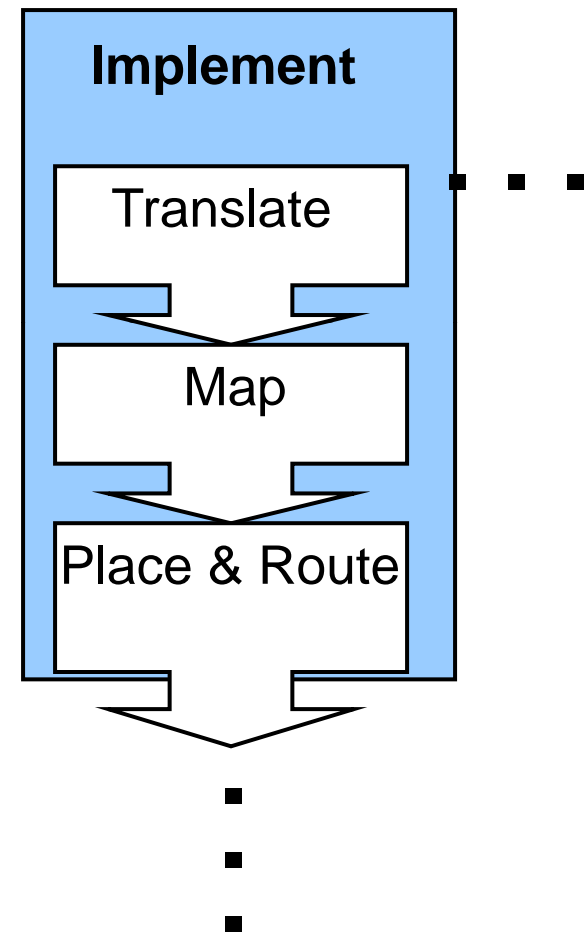
Design Entry in Xilinx ISE -- contd

- **Popular synthesis tools:** Synplify, Leonardo Spectrum, FPGA Compiler II, and XST
- **Simulate design so that it works as expected!**



Xilinx Implementation

- Once you generate a netlist, you can implement the design
- There are several outputs of implementation
 - Reports
 - Timing simulation netlists
 - Floorplan files
 - FPGA Editor files
 - and more!



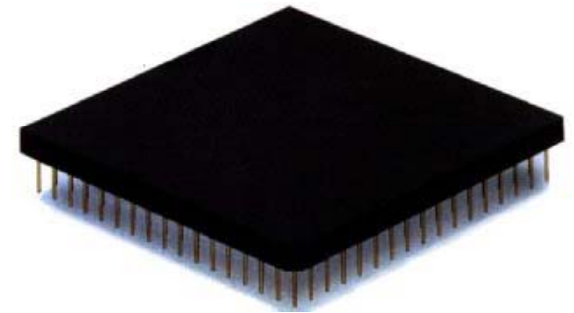


What is Implementation?

- More than just “Place & Route”
- Implementation includes many phases
 - **Translate:** Merge multiple design files into a single netlist
 - **Map:** Group logical symbols from the netlist (gates) into physical components (CLBs, IOBs)
 - **Place & Route:** Place components onto the chip, connect them, and extract timing data into reports
- Each phase generates files that allow you to use other Xilinx tools (such as Floorplanner, FPGA Editor, XPower, Multi-Pass Place & Route)

Download in Xilinx FPGAs

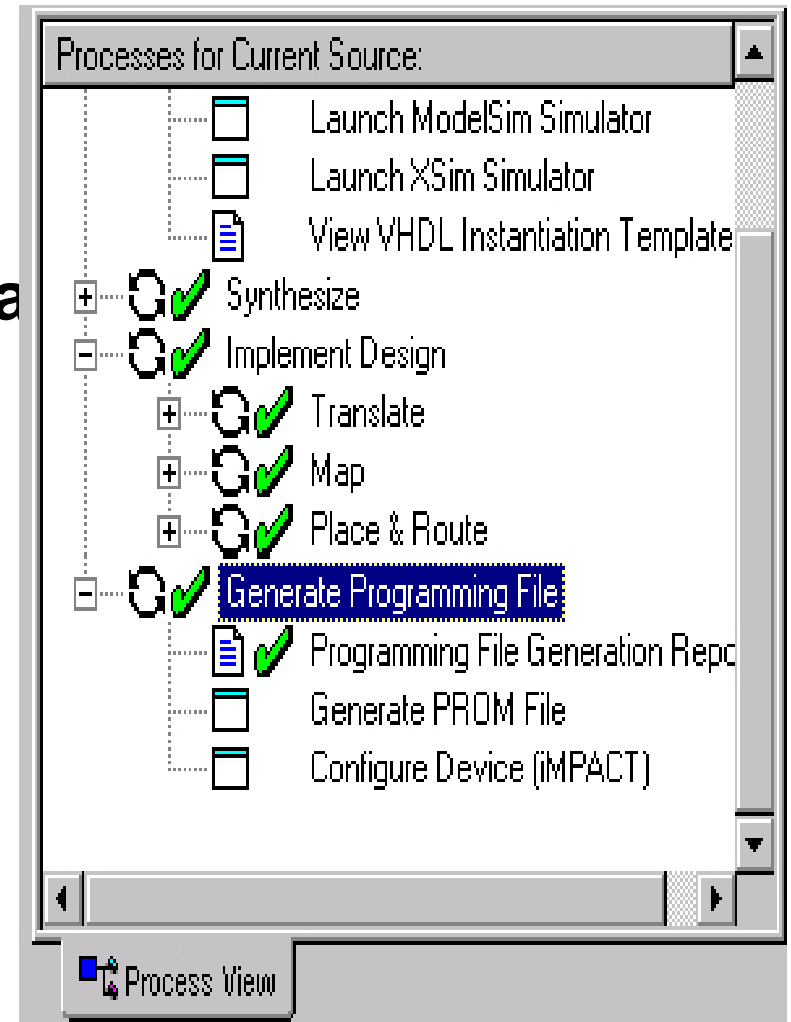
- Once a design is implemented, you must create a file that the FPGA can understand
 - This file is called a bit stream: a BIT file (.bit extension)
- The BIT file can be downloaded directly to the FPGA, or can be converted into a PROM file which stores the programming information



Program the FPGA

➤ There are two ways to program an FPGA

- **Through a PROM device**
 - You will need to generate a file that the PROM programmer will understand
- **Directly from the computer**
 - Use the iMPACT configuration tool



Xilinx ISE has a complete Solution

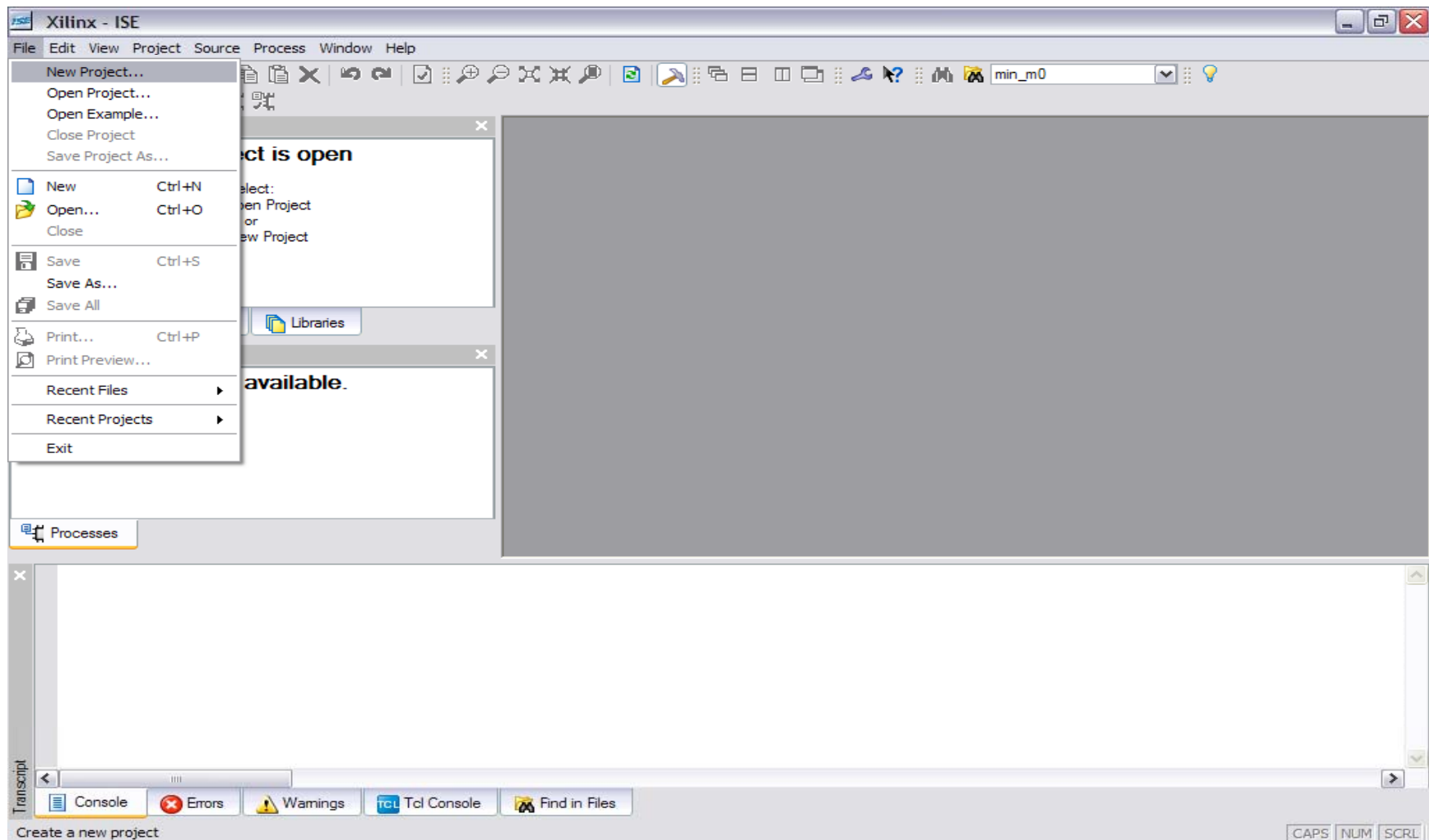
❖ The Xilinx design process contains only four steps: design, synthesize, implement, configure

❖ The Xilinx design process can all be done through the ISE Project Navigator



Design Example

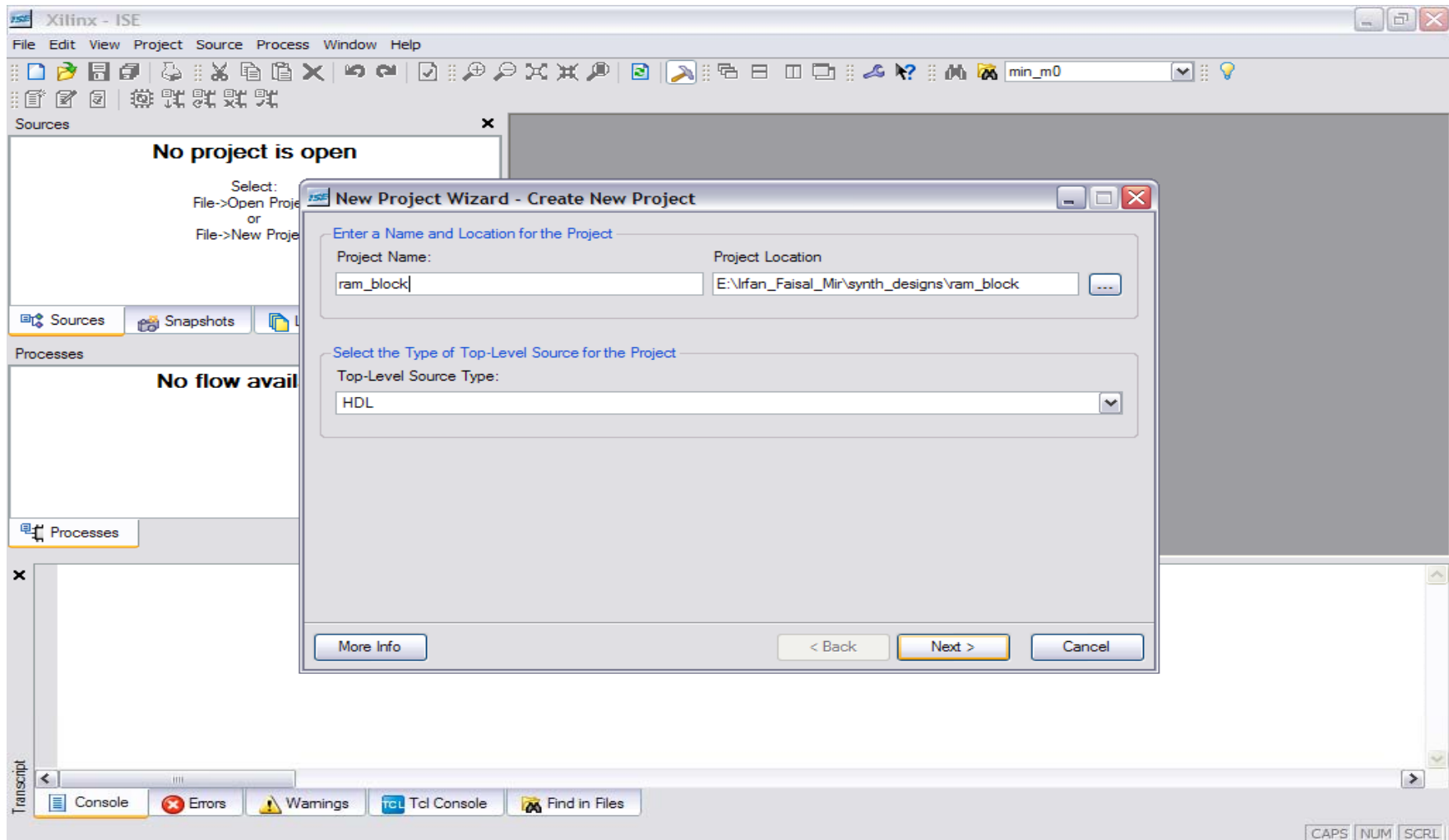
- **Step1:** Create Project in ISE 8.2i (Project Navigator)
 - In file menu, start from “New Project” option...



Design Example

➤ Step1: Create Project in ISE 8.2i (Project Navigator)

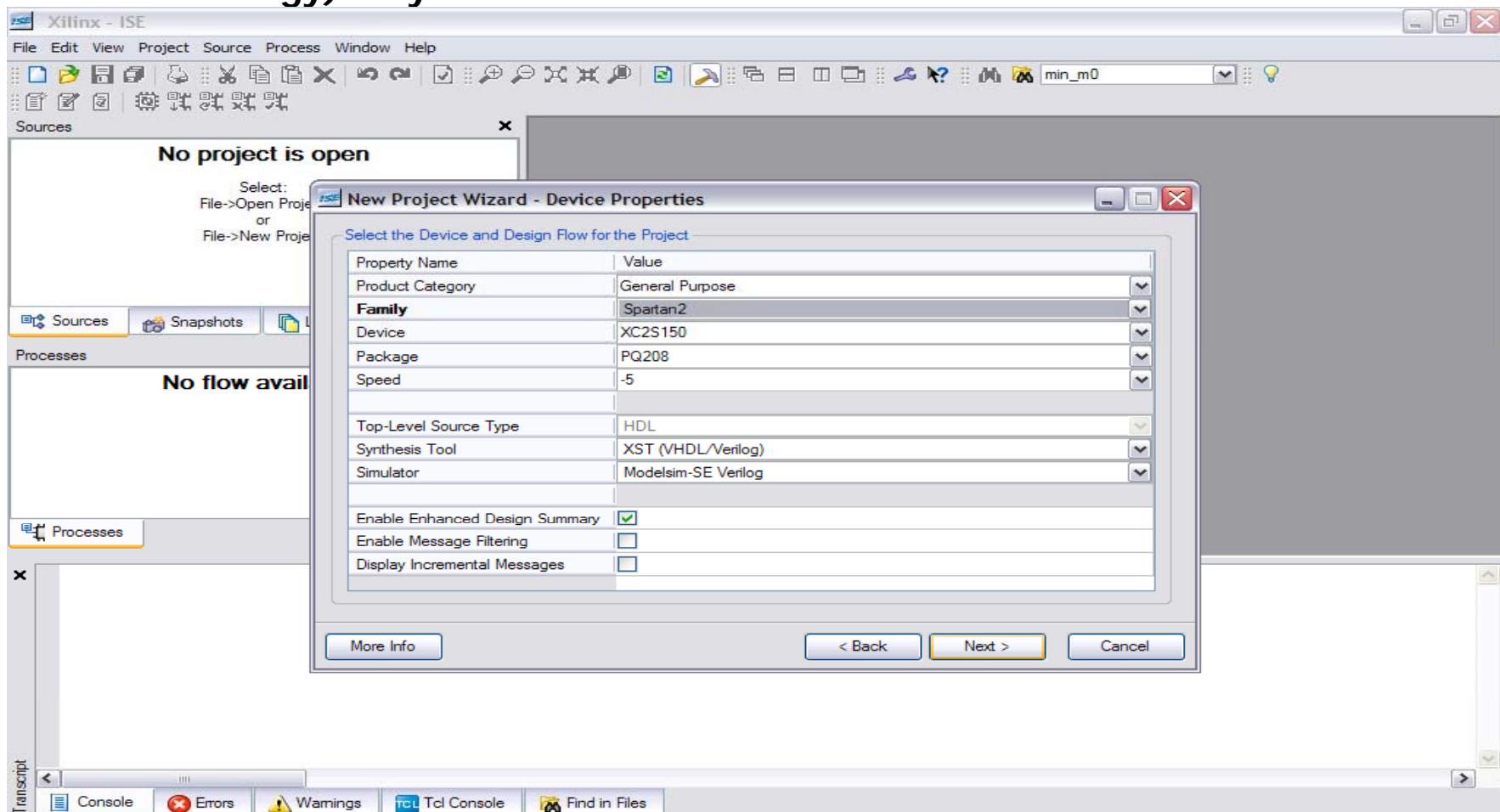
- Write Project name, mention project path and select Top Level Module Type "HDL"



Design Example

➤ Step1: Create Project in ISE 8.2i (Project Navigator)

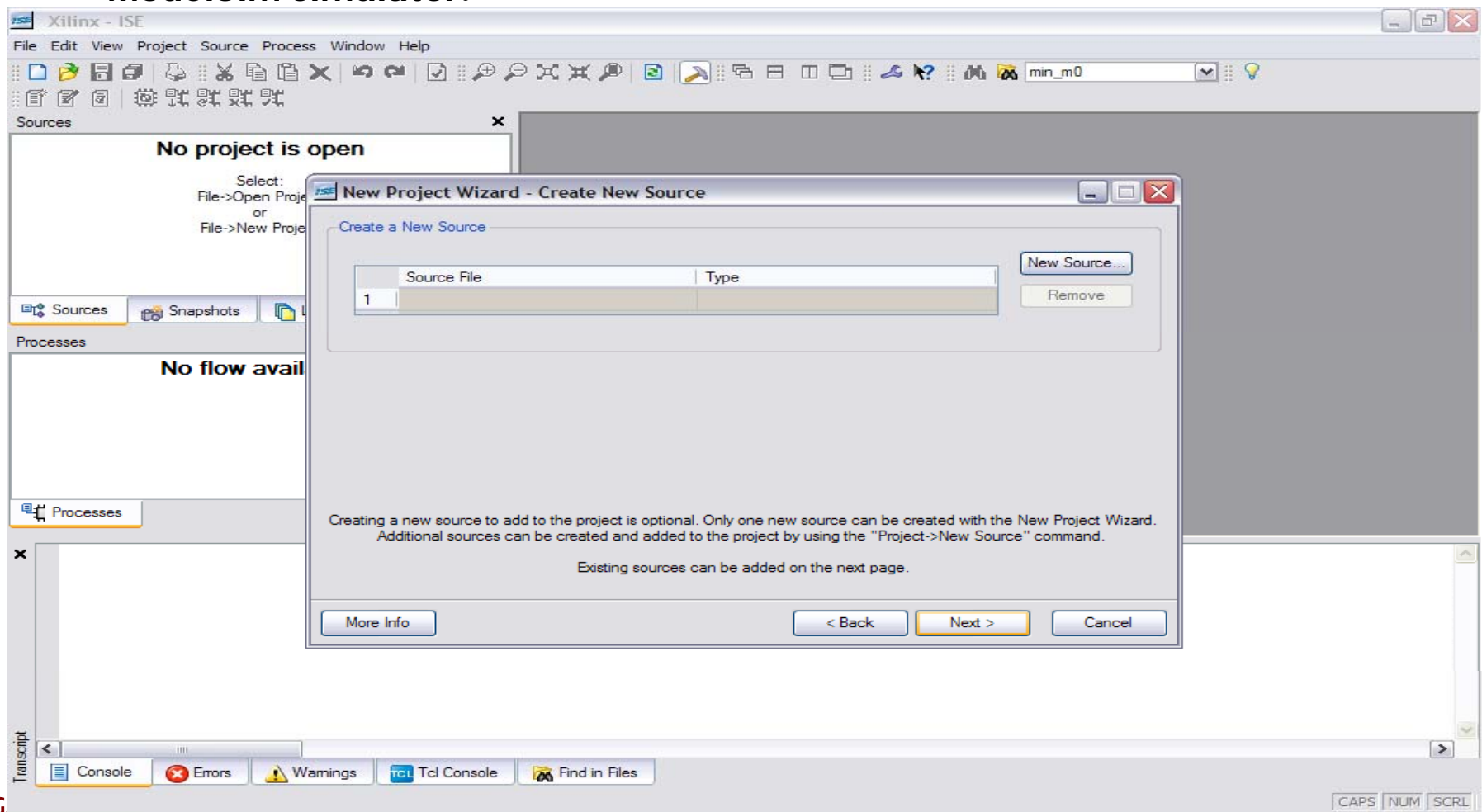
- Select Device Family, Device, package, speed grade for FPGA. Here you also select Synthesis Flow for FPGA. ISE 8.2i has support XST (Xilinx Synthesis Technology) only.



Design Example

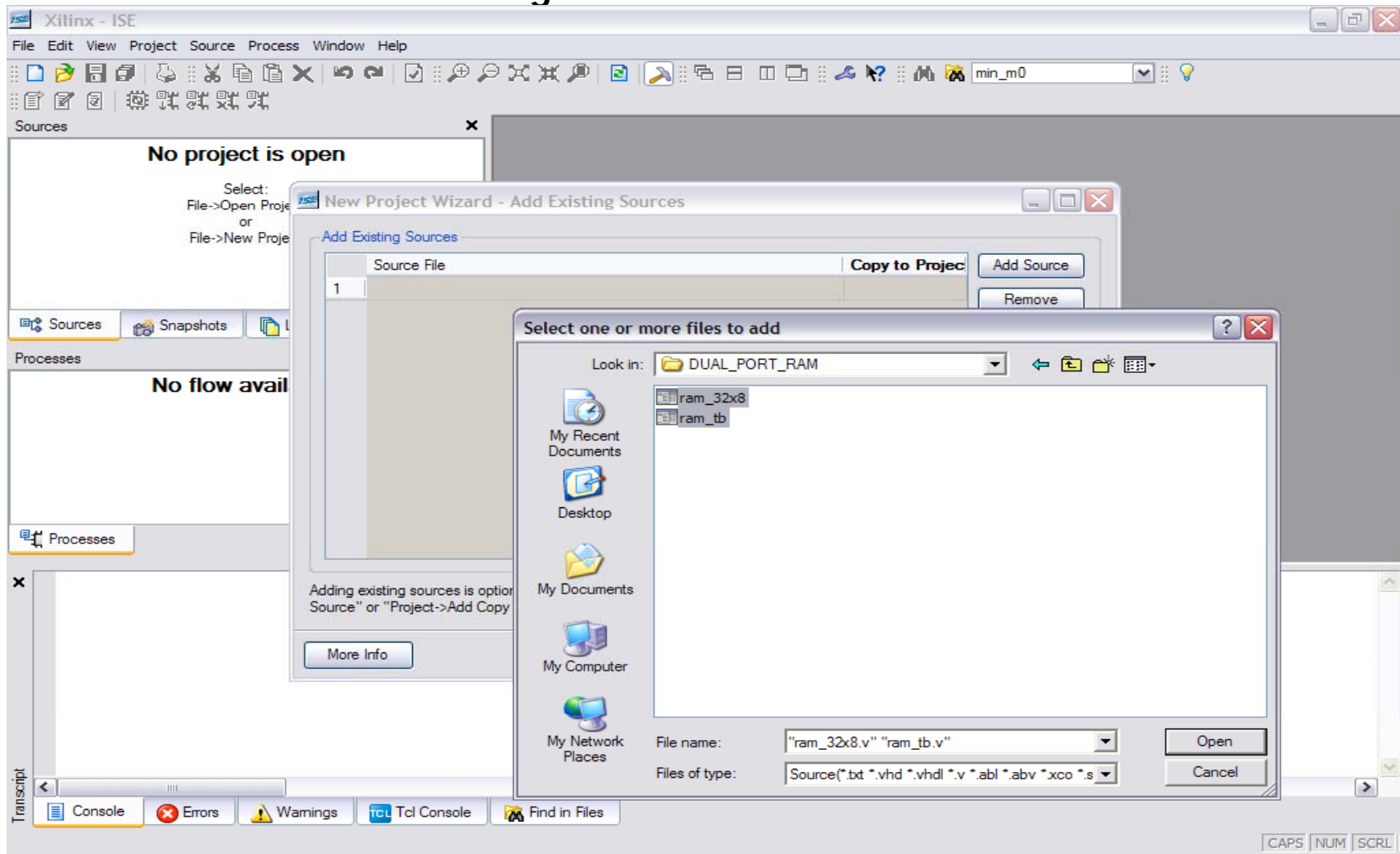
➤ Step2: Create New Files in ISE 8.2i (Project Navigator)

- Here you can create new Verilog HDL files in current project...We simply ignore this step because we have already existing files that are verified in ModelSim simulator.



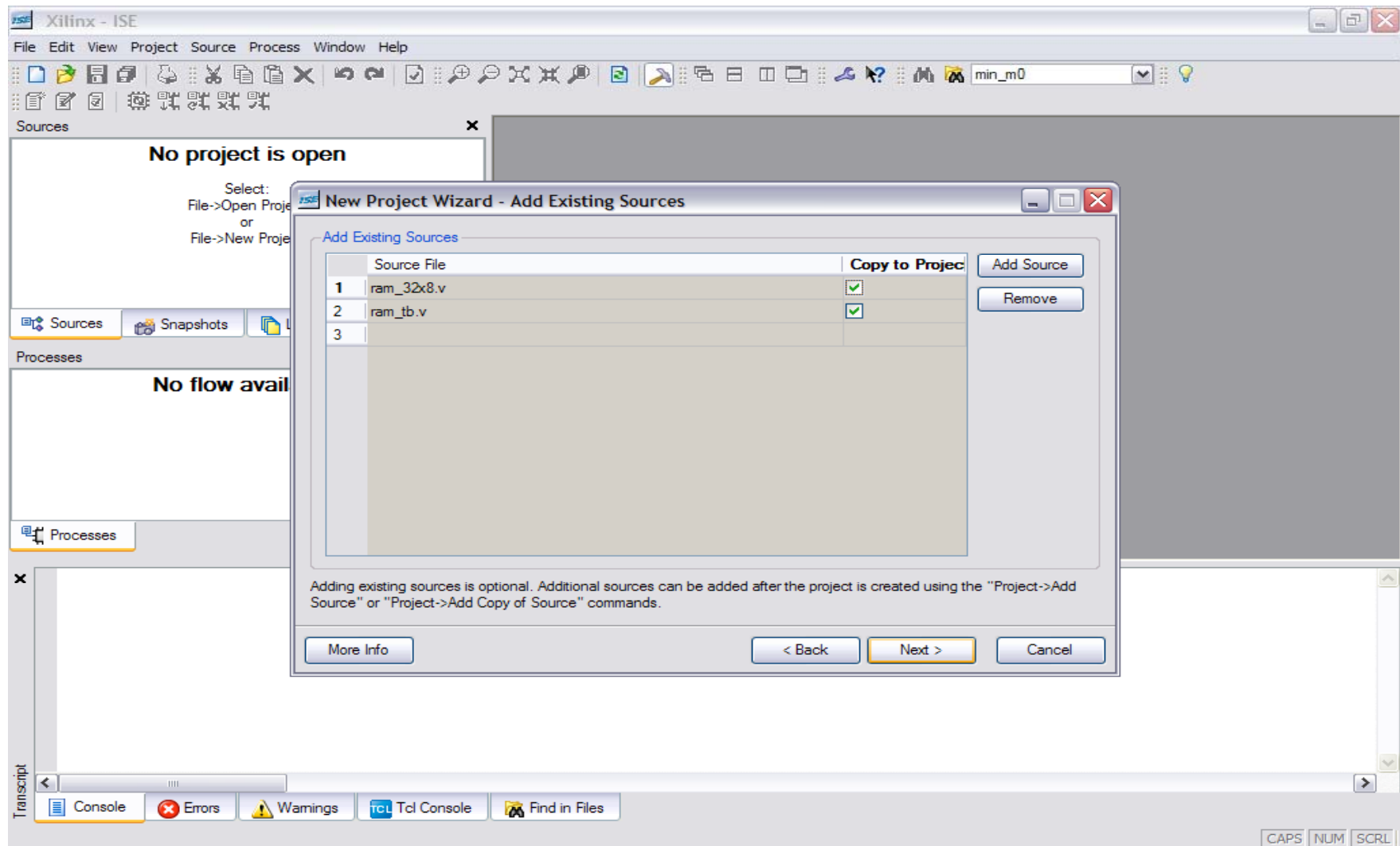
Design Example

- **Step2:** Add existing Files in Project by using ISE 8.2i (Project Navigator)
 - Here we add existing verilog source files (RTL + Testbench) in ISE 8.2i. ISE detects which one is Design file or Test Fixture file itself.



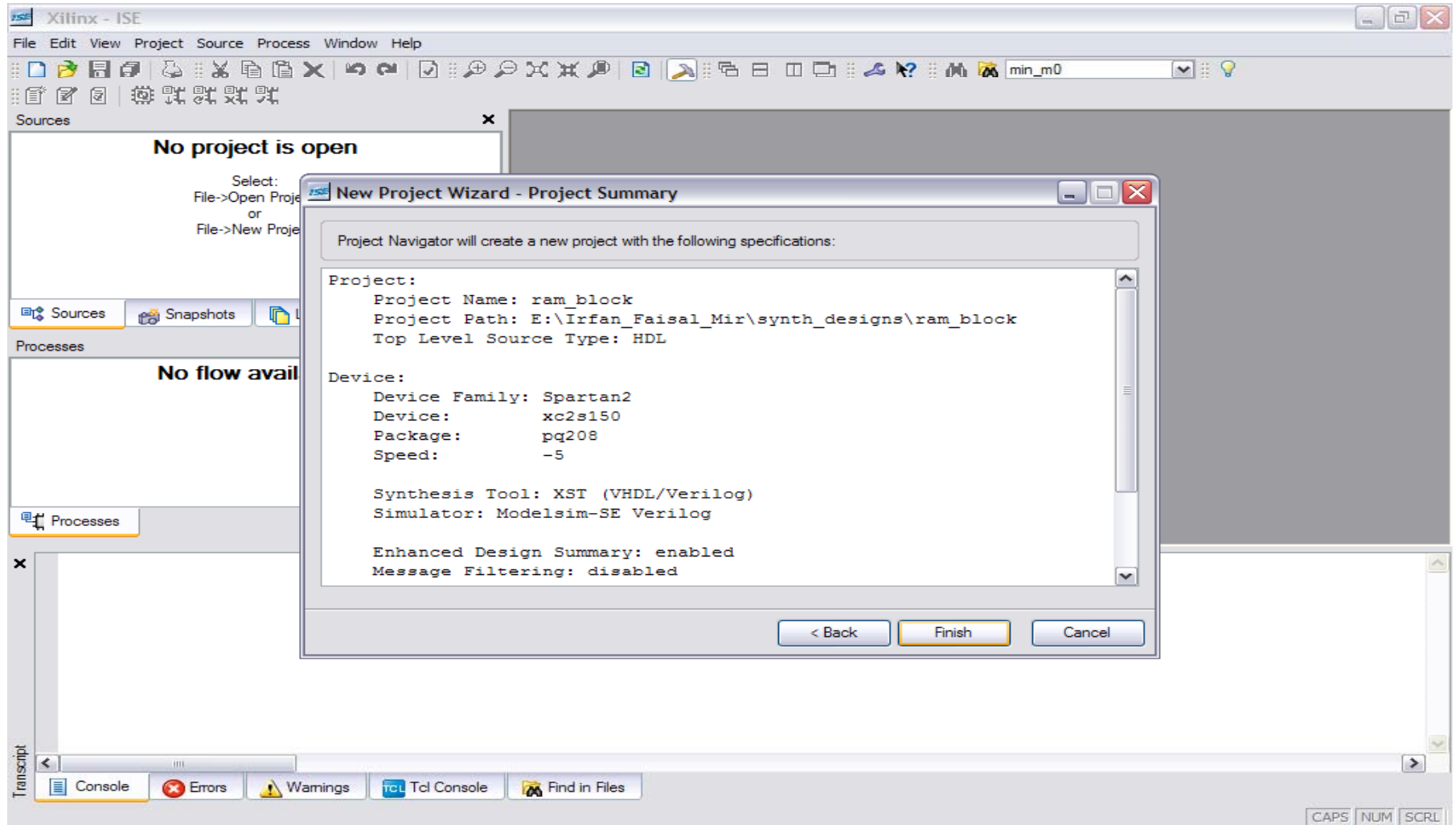
Design Example

- **Step3:** Mention file type by using ISE 8.2i (Project Navigator)
 - Here we may copy these files or not in ISE working directory....



Design Example

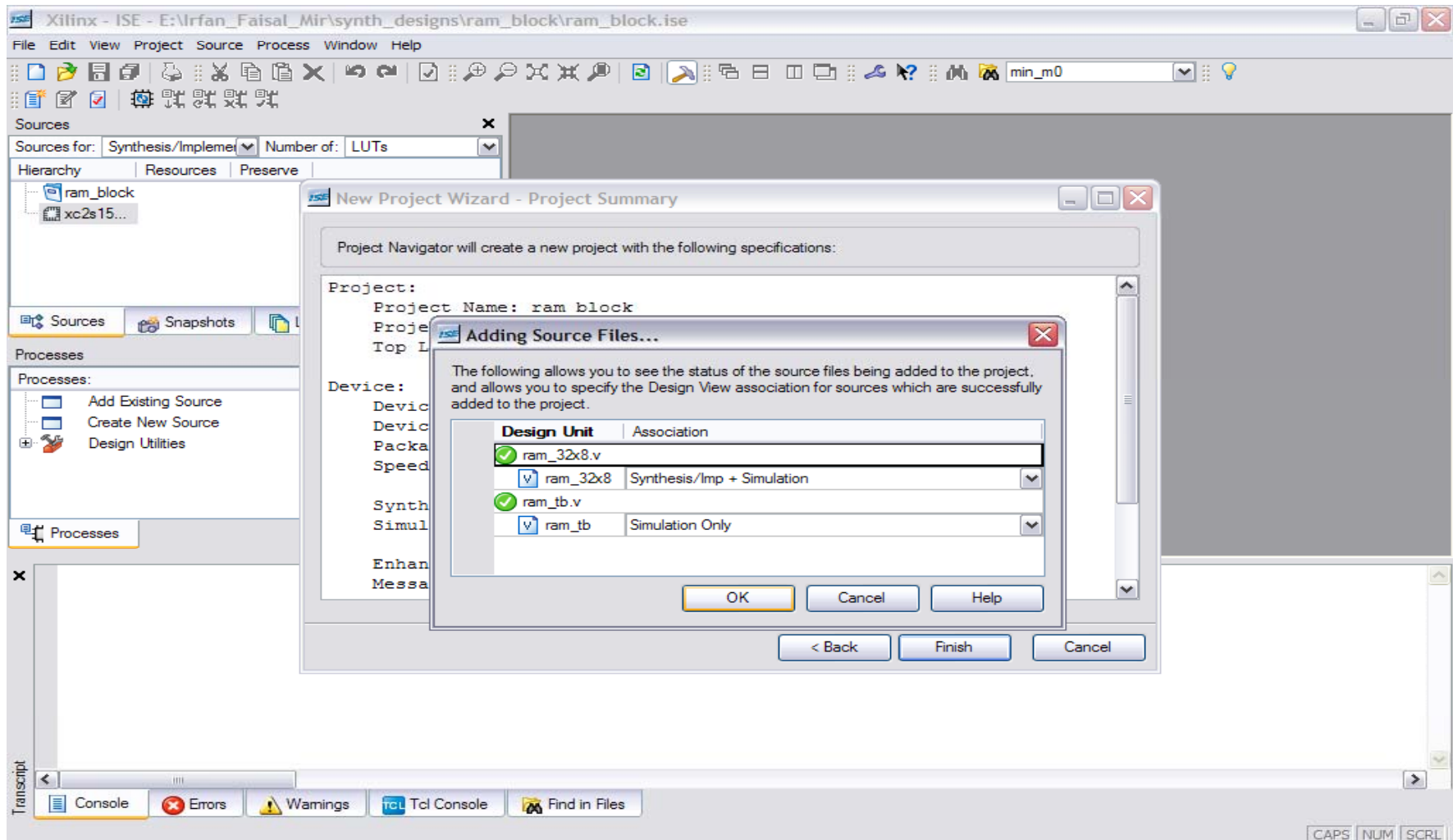
- **Step3:** Mention file type by using ISE 8.2i (Project Navigator)
- Now design entry step has completed now. Select finish to close it...



Design Example

➤ Step3: Mention file type by using ISE 8.2i (Project Navigator)

- Here we select the file type whether it is Verilog Design File or Verilog Test Fixture file...



Design Example

- **Step4:** Synthesis your design by using ISE 8.2i (Project Navigator)
 - First select the top module file of your project in “sources in project” small window.

The screenshot displays the Xilinx ISE 8.2i Project Navigator interface. The main window is titled "Xilinx - ISE - E:\Irfan_Faisal_Mir\synth_designs\ram_block\ram_block.isc - [Design Summary]". The "Sources" pane on the left shows the project hierarchy with "ram_block" selected. The "Processes" pane on the left lists various design steps, with "Design Utilities" selected. The "FPGA Design Summary" pane on the right shows the "Design Overview" section, which includes a tree view of the design summary contents. The "Project Properties" section is also visible, showing options like "Enable Enhanced Design Summary" and "Show Partition Data". The "Design Summary" pane on the right displays the "RAM_BLOCK Project Status" table, which includes project file, module name, target device, and product version. Below this is the "RAM_BLOCK Partition Summary" section, which states "No partition information was found." The "Detailed Reports" section at the bottom right shows a table with columns for Report Name, Status, Generated, Errors, Warnings, and Infos. The "Console" pane at the bottom shows the message "Started : 'Launching Design Summary'."

Project File:	ram_block.isc	Current State:	New
Module Name:	ram_32x8	• Errors:	
Target Device:	xc2s150-5pq208	• Warnings:	
Product Version:	ISE 8.2i	• Updated:	Fri Jul 13 12:14:36 2007

No partition information was found.	
-------------------------------------	--

Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report					
Translation Report					
Map Report					

Design Example

- **Step4:** Synthesis your design by using ISE 8.2i (Project Navigator)
 - Just right click on "Synthesize XST" in "Processes for Source" small window. View the properties...

The screenshot shows the Xilinx ISE 8.2i Project Navigator interface. The 'Processes' window is open, showing a list of processes for the source file 'ram_block.isc'. The 'Synthesize - XST' process is selected, and a context menu is open with the 'Properties...' option highlighted. The 'FPGA Design Summary' window is also open, displaying the 'RAM_BLOCK Project Status' and 'Detailed Reports'.

RAM_BLOCK Project Status

Project File:	ram_block.isc	Current State:	New
Module Name:	ram_32x8	• Errors:	
Target Device:	xc2s150-5pq208	• Warnings:	
Product Version:	ISE 8.2i	• Updated:	Fri Jul 13 12:14:36 2007

RAM_BLOCK Partition Summary

No partition information was found.

Detailed Reports

Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report					
Translation Report					
Map Report					

Project Properties

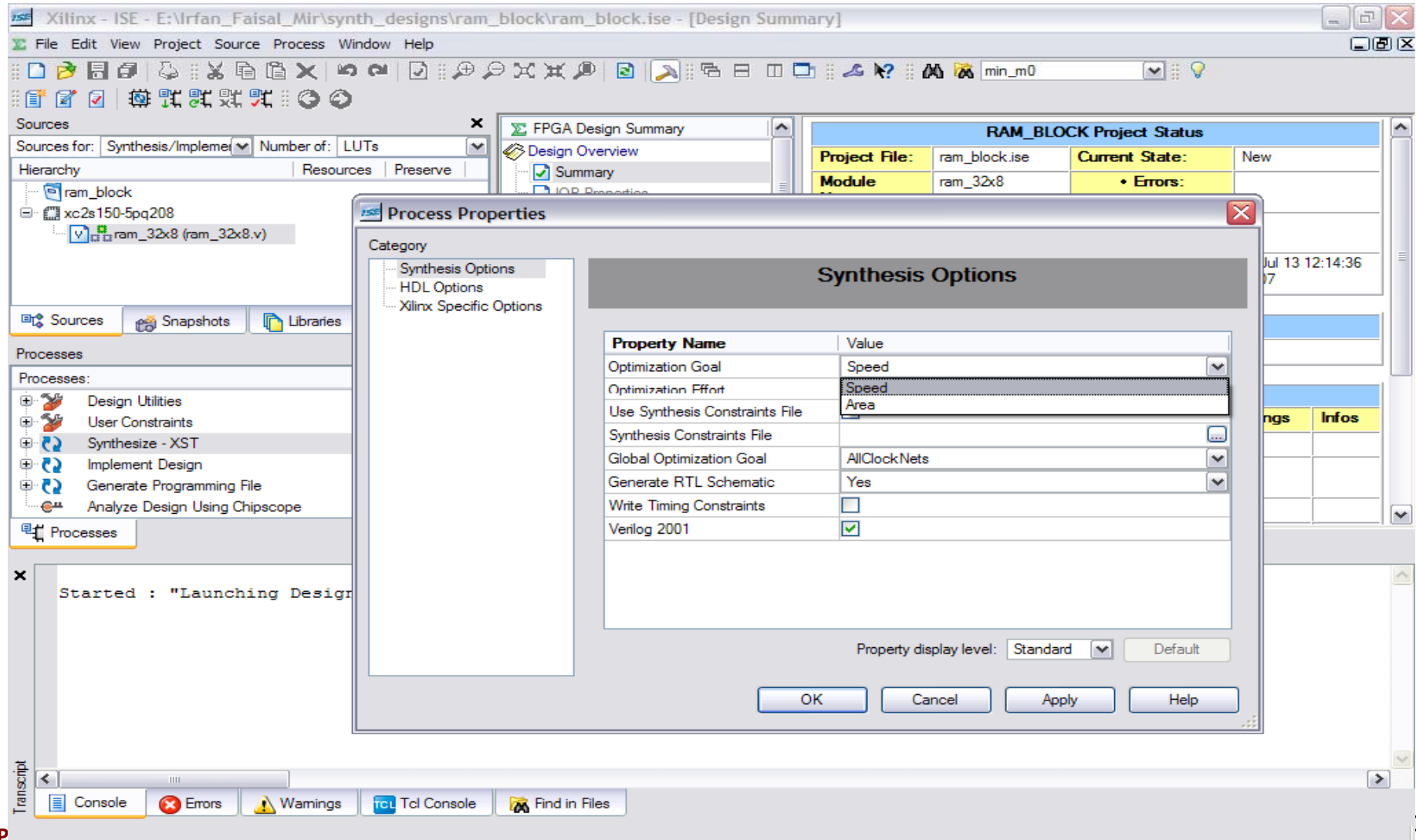
- ☒ Enable Enhanced Design Summary
- ☐ Enable Message Filtering
- ☐ Display Incremental Messages
- ☒ Show Partition Data
- ☐ Show Errors

Transcript

Started : "Launching Design Summary".

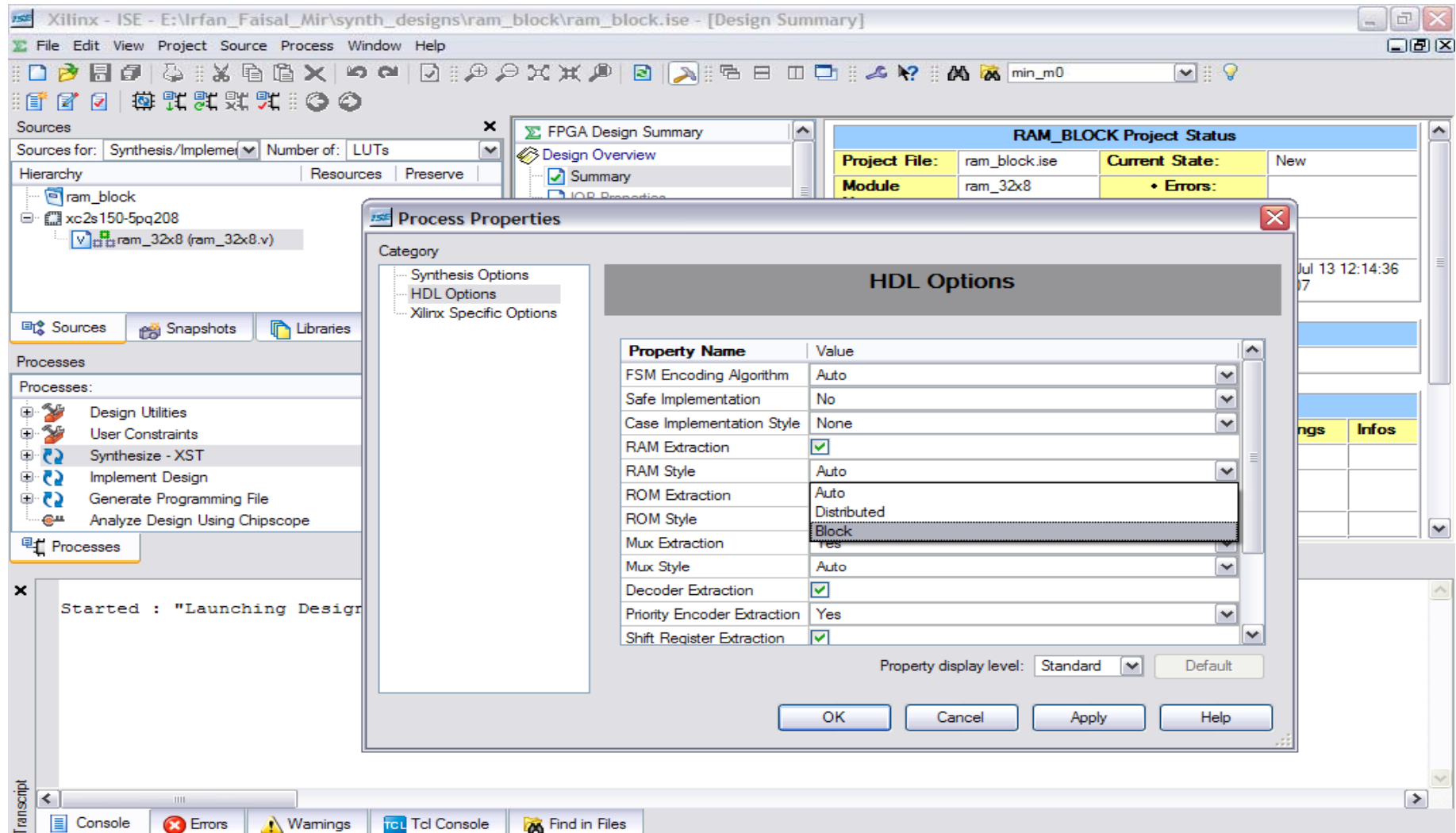
Design Example

- **Step4:** Synthesis your design by using ISE 8.2i (Project Navigator)
 - You can control the synthesis flow of your design.



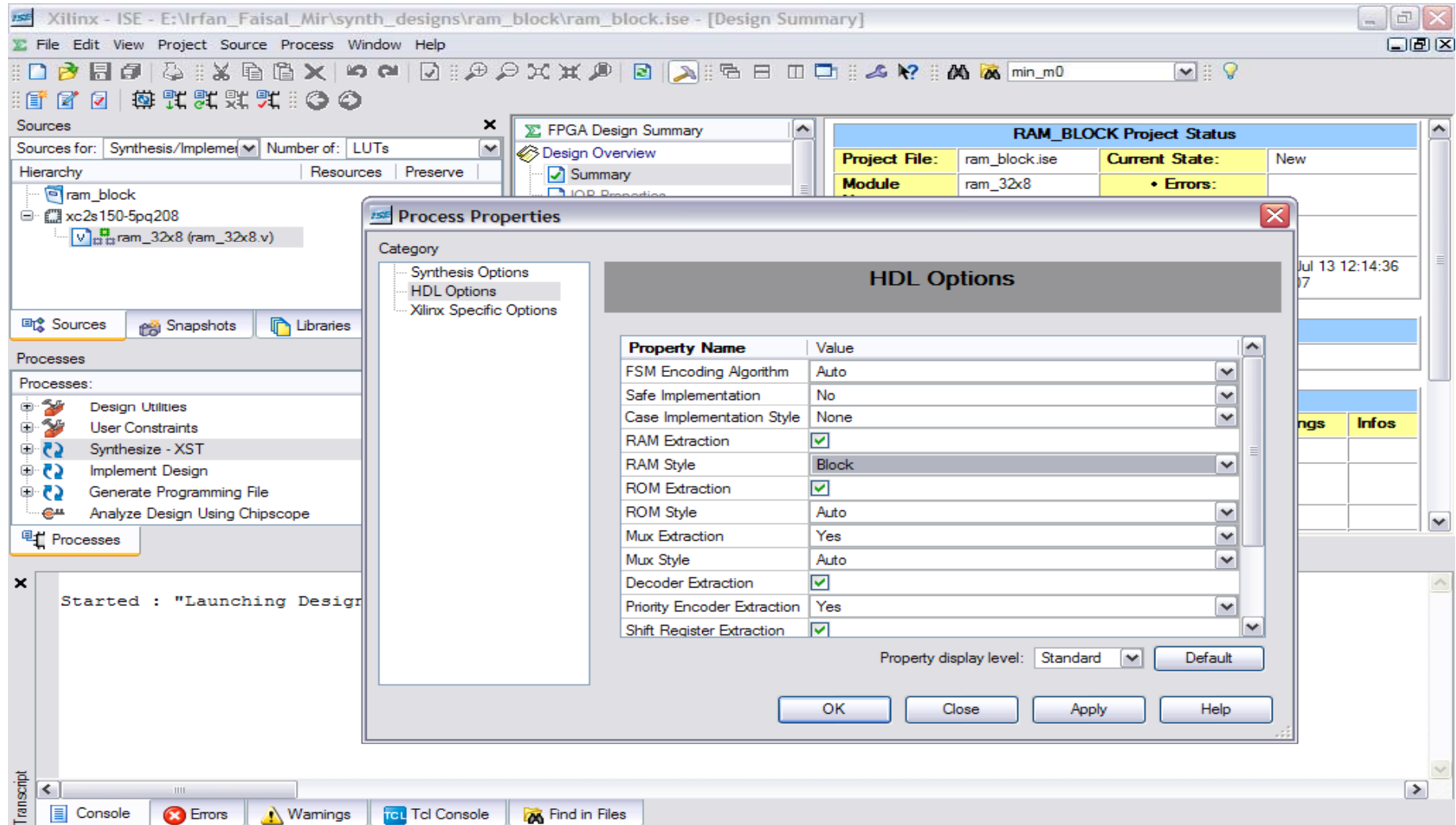
Design Example

- **Step4:** Synthesis your design by using ISE 8.2i (Project Navigator)
 - You can control the synthesis flow of your design.



Design Example

- **Step4:** Synthesis your design by using ISE 8.2i (Project Navigator)
 - You can control the synthesis flow of your design.



Design Example

- **Step4:** Synthesis your design by using ISE 8.2i (Project Navigator)
 - Finally click on Run and synthesis flow will go on...

The screenshot displays the Xilinx ISE 8.2i Project Navigator interface. The title bar indicates the project is 'ram_block.isc' located at 'E:\Irfan_Faisal_Mir\synth_designs\ram_block\ram_block.isc'. The 'Sources' pane on the left shows the project hierarchy: 'ram_block' containing 'xc2s150-5pq208' and 'ram_32x8 (ram_32x8.v)'. The 'Processes' pane shows the 'Synthesize - XST' process selected, with a context menu open showing options like 'Run', 'Rerun', 'Rerun All', 'Stop', 'Open Without Updating', and 'Properties...'. The 'FPGA Design Summary' pane on the right provides a detailed overview of the project status and partitioning.

RAM_BLOCK Project Status

Project File:	ram_block.isc	Current State:	New
Module Name:	ram_32x8	• Errors:	
Target Device:	xc2s150-5pq208	• Warnings:	
Product Version:	ISE 8.2i	• Updated:	Fri Jul 13 12:14:36 2007

RAM_BLOCK Partition Summary

No partition information was found.

Detailed Reports

Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report					
Translation Report					
Map Report					

The 'Design Summary' pane at the bottom shows the 'Run' process highlighted, with a status bar indicating 'Run highlighted process'.

Design Example

- **Step4:** Synthesis your design by using ISE 8.2i (Project Navigator)
- At the end of synthesis process, it will show the PASS (✓) or FAIL (✗) indication...

The screenshot shows the Xilinx ISE 8.2i Project Navigator interface. The title bar indicates the project is 'Xilinx - ISE - E:\Irfan_Faisal_Mir\synth_designs\ram_block\ram_block.isc - [Design Summary]'. The menu bar includes File, Edit, View, Project, Source, Process, Window, and Help. The toolbar contains various icons for file operations and project management.

The **Sources** pane on the left shows the project hierarchy: 'ram_block' containing 'xc2s150-5pq208' and 'ram_32x8 (ram_32x8.v)'. The **Processes** pane shows the 'Synthesize - XST' process as the current step, marked with a green checkmark. The **Design Summary** pane on the right provides a detailed overview of the project status and utilization.

RAM_BLOCK Project Status

Project File:	Current State:
ram_block.isc	Synthesized

Module Name:	Errors:
ram_32x8	No Errors

Target Device:	Warnings:
xc2s150-5pq208	No Warnings

Product Version:	Updated:
ISE 8.2i	Fri Jul 13 12:26:00 2007

RAM_BLOCK Partition Summary

No partition information was found.

Device Utilization Summary (estimated values)

Logic Utilization	Used	Available	Utilization
Number of Slices	0	1728	0%
Number of bonded IOBs	28	144	19%
Number of BRAMs	1	12	8%
Number of GCLKs	1	4	25%

The **Console** pane at the bottom shows the output of the synthesis process, including the selected device and utilization statistics.

```
-----
Selected Device : 2s150pq208-5

Number of Slices:          0 out of 1728    0%
Number of IOs:             28 out of 144    19%
Number of bonded IOBs:     28 out of 144    19%
Number of BRAMs:           1 out of 12     8%
Number of GCLKs:           1 out of 4      25%
```

Design Example

➤ Step5: Implement Design by using ISE 8.2i (Project Navigator)

- Just right click on "Implement Design" in "Processes for Source" small window. View the properties...You can control the Implement flow of your design.

The screenshot shows the Xilinx ISE 8.2i Project Navigator interface. The 'Processes' window is open, showing a list of processes. The 'Implement Design' process is selected, and a context menu is displayed with the 'Properties...' option highlighted. The 'Properties' dialog for the 'Implement Design' process is open, showing the 'Selected Device' as 'xc2s150-5pq208-5'. The dialog also displays the 'Device Utilization Summary (estimated values)' table.

RAM_BLOCK Project Status			
Project File:	ram_block.isc	Current State:	Synthesized
Module Name:	ram_32x8	• Errors:	No Errors
Target Device:	xc2s150-5pq208	• Warnings:	No Warnings
Product Version:	ISE 8.2i	• Updated:	Fri Jul 13 12:26:00 2007

RAM_BLOCK Partition Summary			
No partition information was found.			

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	0	1728	0%
Number of bonded IOBs	28	144	19%
Number of BRAMs	1	12	8%
Number of GCLKs	1	4	25%

Selected Device : xc2s150-5pq208-5			
Number of Slices:	0	out of	1728 0%
Number of IOs:	28		
Number of bonded IOBs:	28	out of	144 19%
Number of BRAMs:	1	out of	12 8%
Number of GCLKs:	1	out of	4 25%

Design Example

➤ Step5: Implement Design by using ISE 8.2i (Project Navigator)

- Just right click on "Implement Design" in "Processes for Source" small window. View the properties...You can control the Implement flow of your design.

The screenshot displays the Xilinx ISE 8.2i Project Navigator interface. The main window shows the project hierarchy with 'ram_block' selected. The 'Processes' pane on the left lists various design steps, with 'Implement Design' highlighted. A 'Process Properties' dialog box is open, showing the 'Place & Route Properties' tab. The 'Property Name' and 'Value' table is as follows:

Property Name	Value
Place And Route Mode	Normal Place and Route
Place & Route Effort Level (Overall)	Standard
Starting Placer Cost Table (1-100)	1
PAR Guide Design File (.ncd)	
PAR Guide Mode	None
Use Timing Constraints	<input checked="" type="checkbox"/>
Use Bonded I/Os	<input type="checkbox"/>
Generate Asynchronous Delay Report	<input type="checkbox"/>
Generate Post-Place & Route Static Timing Report	<input checked="" type="checkbox"/>
Generate Post-Place & Route Simulation Model	<input type="checkbox"/>
Number of PAR Iterations (0-100)	3
Number of Results to Save (0-100)	
Save Results in Directory (.dir will be appended)	

The 'Property display level' is set to 'Standard'. The 'OK', 'Cancel', 'Apply', and 'Help' buttons are visible at the bottom of the dialog.

Design Example

➤ Step5: Implement Design by using ISE 8.2i (Project Navigator)

- Finally click on Run and Implementation flow will go on...

The screenshot shows the Xilinx ISE 8.2i Project Navigator interface. The 'Processes' pane on the left shows the 'Implement Design' process selected, with a context menu open showing options: Run, Rerun, Rerun All, Stop, Open Without Updating, and Properties... The 'FPGA Design Summary' pane in the center shows the 'Design Overview' section with a list of reports: Summary, IOB Properties, Timing Constraints, Pinout Report, Clock Report, Errors and Warnings, Synthesis Messages, Translation Messages, Map Messages, and Place and Route Messages. The 'Project Properties' section shows options for 'Enable Enhanced Design Summary', 'Enable Message Filtering', 'Display Incremental Messages', 'Enhanced Design Summary Contents', 'Show Partition Data', and 'Show Errors'. The 'RAM_BLOCK Project Status' pane on the right shows the project file 'ram_block.isc', current state 'Synthesized', module name 'ram_32x8', target device 'xc2s150-5pq208', product version 'ISE 8.2i', and updated date 'Fri Jul 13 12:26:00 2007'. The 'RAM_BLOCK Partition Summary' pane shows 'No partition information was found.' The 'Device Utilization Summary (estimated values)' pane shows a table with logic utilization data.

Logic Utilization	Used	Available	Utilization
Number of Slices	0	1728	0%
Number of bonded IOBs	28	144	19%
Number of BRAMs	1	12	8%
Number of GCLKs	1	4	25%

Selected Device:

Number of Slices:	0	out of	1728	0%
Number of IOs:	28			
Number of bonded IOBs:	28	out of	144	19%
Number of BRAMs:	1	out of	12	8%
Number of GCLKs:	1	out of	4	25%

Run highlighted process

Design Example

➤ Step5: Implement Design by using ISE 8.2i (Project Navigator)

- At the end of Implementation process, it will show the PASS (✓) or FAIL (✗) indication...

Xilinx - ISE - E:\Irfan_Faisal_Mir\synth_designs\ram_block\ram_block.ise - [Design Summary]

File Edit View Project Source Process Window Help

Sources for: Synthesis/Implement Number of: LUTs

Hierarchy

- ram_block
 - xc2s150-5pq208
 - ram_32x8 (ram_32x8.v)

Processes

- Design Utilities
- User Constraints
- Synthesize - XST
- Implement Design**
- Generate Programming File
- Analyze Design Using Chipscope

FPGA Design Summary

- Design Overview
 - Summary
 - IOB Properties
 - Timing Constraints
 - Pinout Report
 - Clock Report
- Errors and Warnings
 - Synthesis Messages
 - Translation Messages
 - Map Messages
 - Place and Route Messages
- Project Properties
 - Enable Enhanced Design Summary
 - Enable Message Filtering
 - Display Incremental Messages
 - Enhanced Design Summary Contents
 - Show Partition Data
 - Show Errors

RAM_BLOCK Project Status

Project File:	ram_block.ise	Current State:	Placed and Routed
Module Name:	ram_32x8	Errors:	No Errors
Target Device:	xc2s150-5pq208	Warnings:	No Warnings
Product Version:	ISE 8.2i	Updated:	Fri Jul 13 12:32:04 2007

RAM_BLOCK Partition Summary

No partition information was found.

Device Utilization Summary

Logic Utilization	Used	Available	Utilization	Note(s)
Logic Distribution				
Number of Slices containing only related logic	0	0	0%	
Number of Slices containing unrelated logic	0	0	0%	

Analysis completed Fri Jul 13 12:32:03 2007

Generating Report ...

Number of warnings: 0
Total time: 2 secs

Process "Generate Post-Place & Route Static Timing" completed successfully

Console Errors Warnings Tcl Console Find in Files

Ready

Design Example

- **Step6:** Simulate Behavioral Model of your Design in ISE 8.2i (Project Navigator)
 - First highlight Behavioral Simulation option in "Sources in Project"...you will see ModelSim Simulator options in "Processes for Source" small window.

The screenshot displays the Xilinx ISE 8.2i Project Navigator interface. The 'Sources' window on the left shows the project hierarchy with 'ram_block.isc' selected, and the 'Behavioral Simulation' option highlighted in the context menu. The 'Processes' window below it shows the 'Synthesize - XST' process selected. The 'FPGA Design Summary' window on the right provides a comprehensive overview of the project, including the design overview, errors and warnings, project properties, and device utilization summary.

RAM_BLOCK Project Status

Project File:	Current State:
ram_block.isc	Placed and Routed
Module Name:	• Errors: No Errors
Target Device:	• Warnings: No Warnings
Product Version:	• Updated: Fri Jul 13 12:32:04 2007

RAM_BLOCK Partition Summary

No partition information was found.

Device Utilization Summary

Logic Utilization	Used	Available	Utilization	Note(s)
Logic Distribution				
Number of Slices containing only related logic	0	0	0%	
Number of Slices containing unrelated logic	0	0	0%	

Analysis completed Fri Jul 13 12:32:03 2007

Generating Report ...

Number of warnings: 0
Total time: 2 secs

Process "Generate Post-Place & Route Static Timing" completed successfully

Design Example

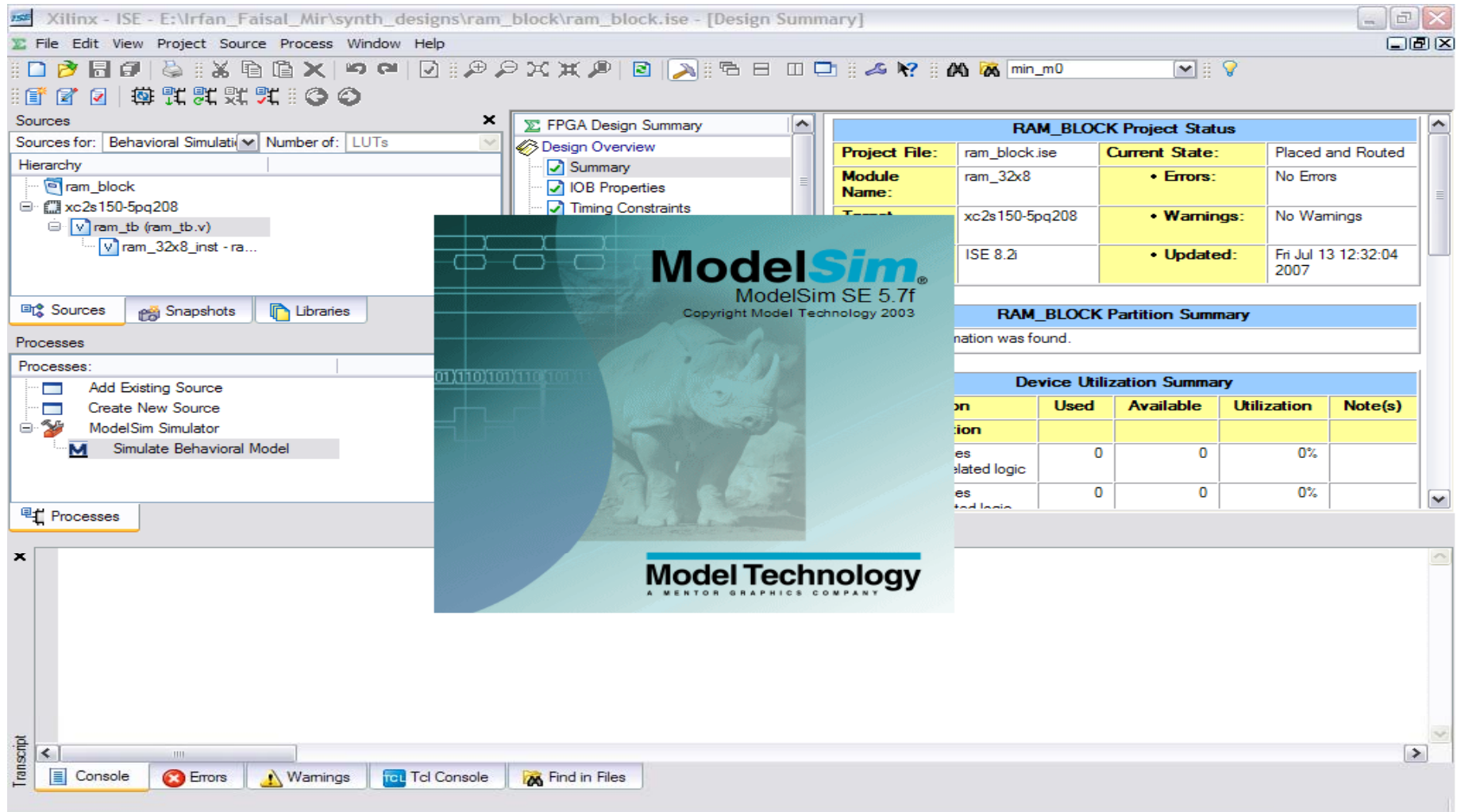
- **Step6:** Simulate Behavioral Model of your Design in ISE 8.2i (Project Navigator)
 - First highlight Test Bench Top File in "Sources in Project"...you will see ModelSim Simulator options in "Processes for Source" small window.

The screenshot shows the Xilinx ISE 8.2i Project Navigator interface. The 'Sources' window on the left displays a project hierarchy with 'ram_block' as the top level, containing 'xc2s150-5pq208' and 'ram_tb (ram_tb.v)'. The 'Processes' window is open for 'ram_tb (ram_tb.v)', showing a context menu with options: Run, Rerun, Rerun All, Stop, Open Without Updating, and Properties... The 'FPGA Design Summary' window is also visible, showing project status and device utilization. The 'Console' window at the bottom displays the following text:

```
Analysis completed Fri Jul 13 12:32:04 2007
Generating Report ...
Number of warnings: 0
Total time: 2 secs
Process "Generate Post-Place & Route Static Timing" completed successfully
```

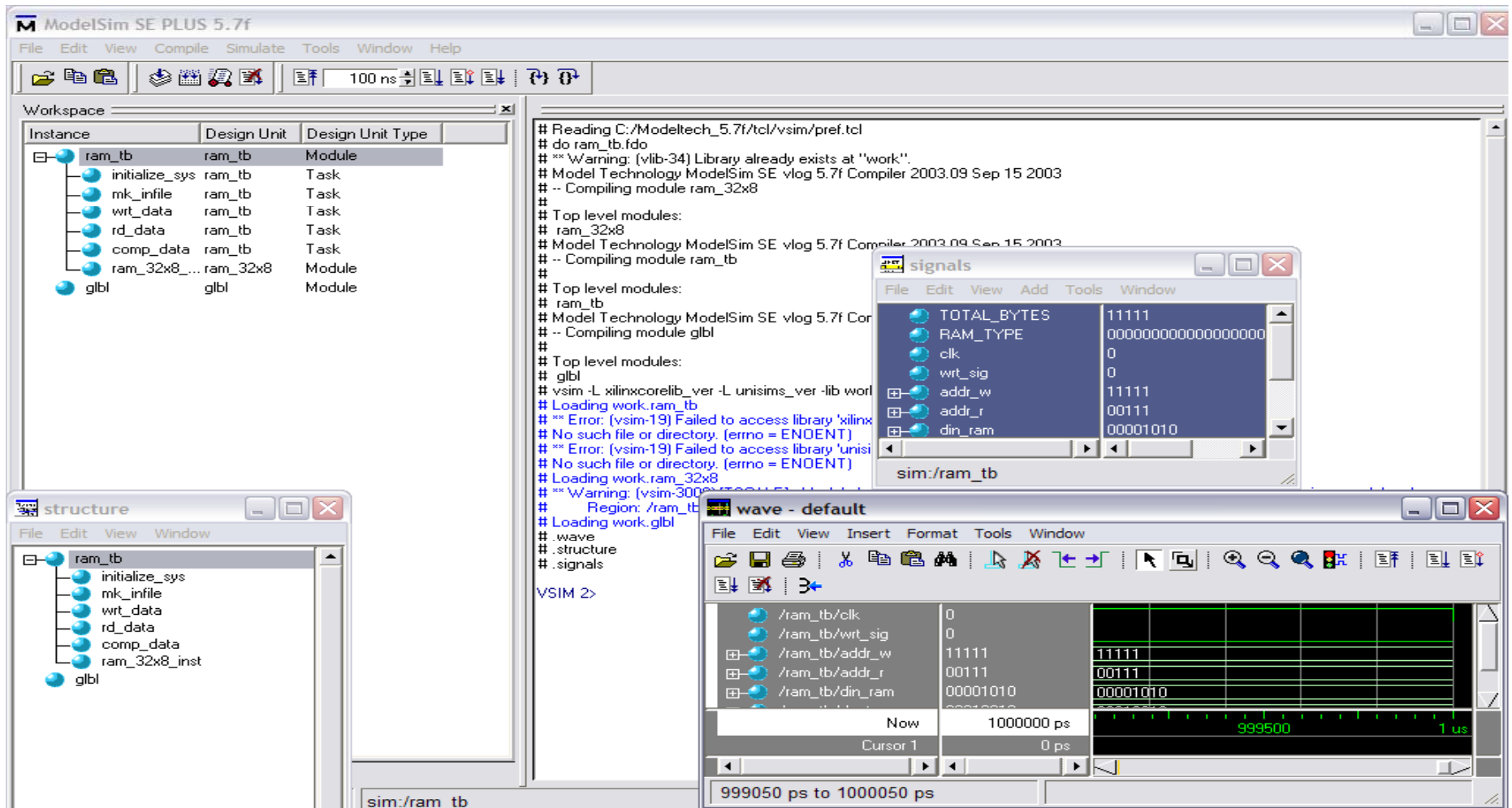
Design Example

- **Step6:** Simulate Behavioral Model of your Design in ISE 8.2i (Project Navigator)
 - Now click on “Simulate Behavioral Model” in “Processes for Source” window.



Design Example

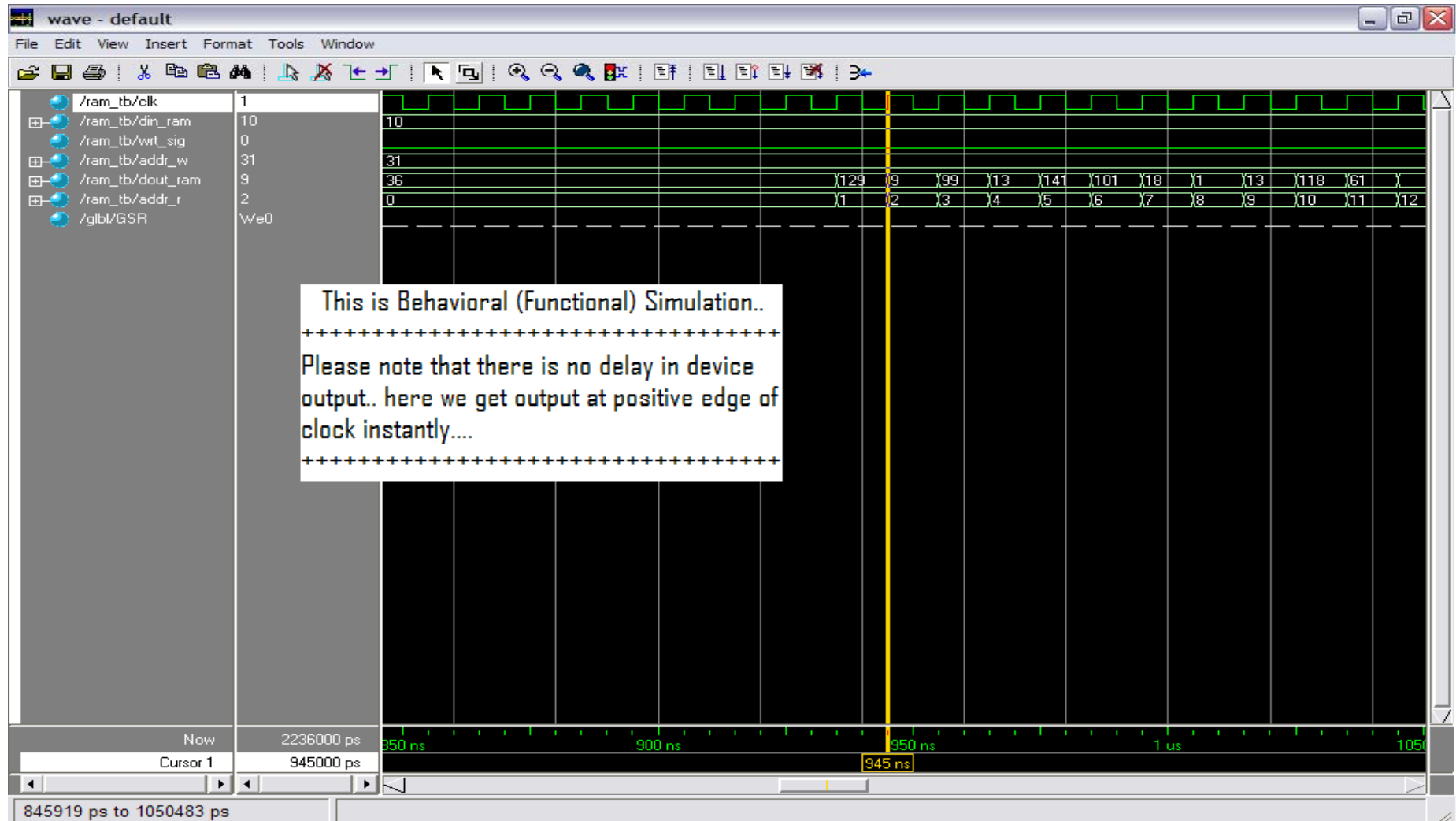
- **Step6:** Simulate Behavioral Model of your Design in ISE 8.2i (Project Navigator)
 - You see the ModelSim Simulator main window...Now you can verify your functional/RTL simulation.



Design Example

➤ Step6: Simulate Behavioral Model for Functional/RTL Simulation

- You can verify your design by using Waveform Viewer in ModelSim...



Design Example

- **Step7:** Load Simulation Libraries before Timing Simulation in ISE 8.2i
 - First highlight project option (e.g xc150e-6pq208) in “Sources in Project” sub-window. You see “Design Entry Utilities” in “Processes for Source” sub-window. Now see the properties of “Compile HDL simulation Libraries” in “Design Entry Utilities” sub-menu.

The screenshot shows the Xilinx ISE 8.2i Design Summary window for a project named 'ram_block'. The 'Sources' pane on the left shows a hierarchy with 'ram_block' containing 'xc2s150-5pq208', which in turn contains 'ram_tb (ram_tb.v)' and 'ram_32x8_inst - ra...'. The 'Processes' pane shows 'Design Utilities' with 'Compile HDL Simulation Libraries' highlighted. A context menu is open over this option, showing 'Run', 'Rerun', 'Rerun All', 'Stop', 'Open Without Updating', and 'Properties...'. The 'FPGA Design Summary' pane on the right shows the 'Design Overview' section with 'Summary', 'IOB Properties', 'Timing Constraints', 'Pinout Report', and 'Clock Report' all checked. Below this, the 'Errors and Warnings' section shows 'Synthesis Messages', 'Translation Messages', 'Map Messages', and 'Place and Route Messages' all checked. The 'Project Properties' section shows 'Enable Enhanced Design Summary', 'Enable Message Filtering', 'Display Incremental Messages', 'Show Design Summary Contents', 'Show Partition Data', and 'Show Errors' all checked. The 'RAM_BLOCK Project Status' table shows the project file as 'ram_block.isc', current state as 'Placed and Routed', module name as 'ram_32x8', target device as 'xc2s150-5pq208', product version as 'ISE 8.2i', and updated on 'Fri Jul 13 12:32:04 2007'. The 'RAM_BLOCK Partition Summary' table shows 'No partition information was found.' The 'Device Utilization Summary' table shows logic utilization with 0 slices containing only related logic and 0 slices containing unrelated logic, both at 0% utilization.

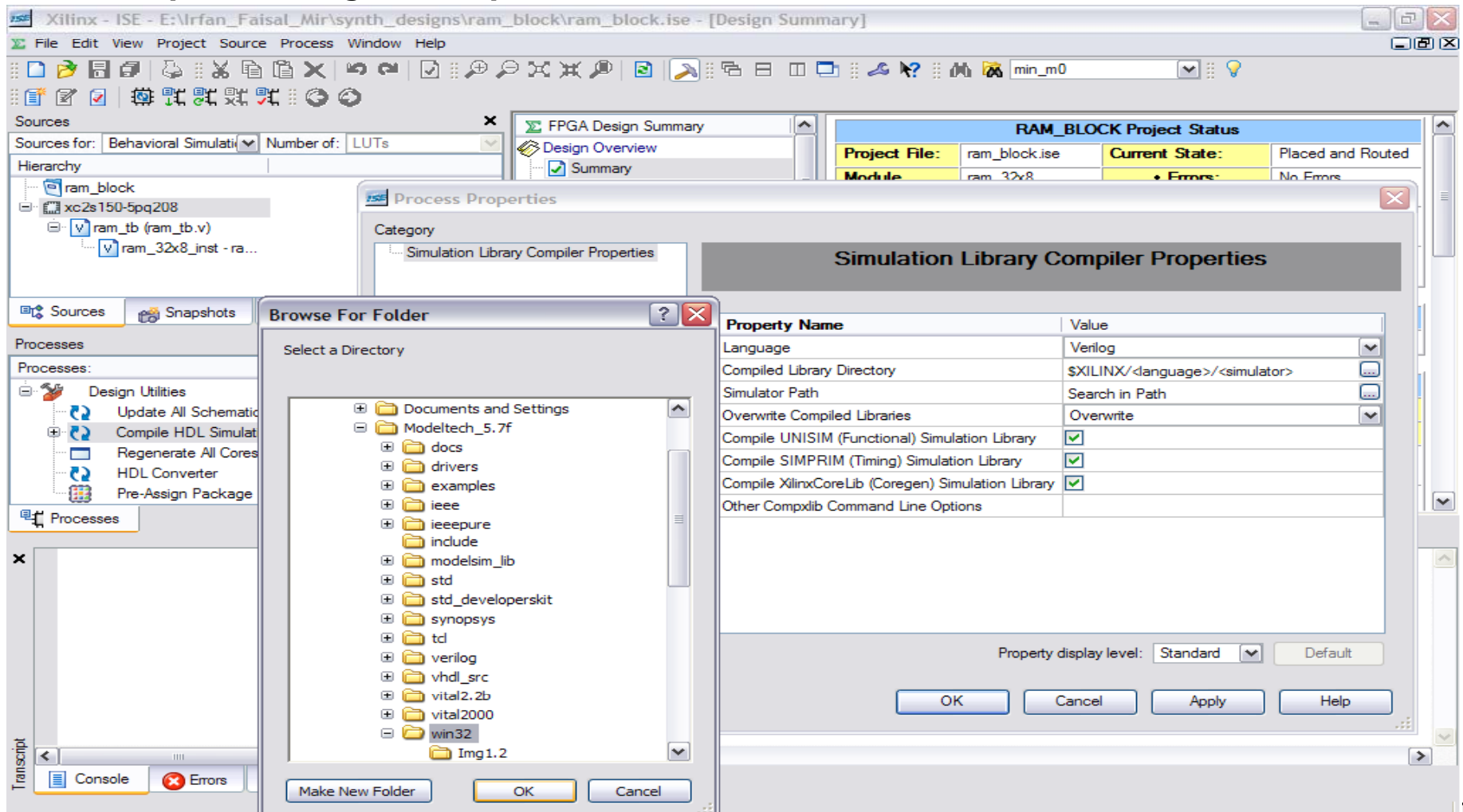
Project File:	ram_block.isc	Current State:	Placed and Routed
Module Name:	ram_32x8	• Errors:	No Errors
Target Device:	xc2s150-5pq208	• Warnings:	No Warnings
Product Version:	ISE 8.2i	• Updated:	Fri Jul 13 12:32:04 2007

No partition information was found.	
-------------------------------------	--

Logic Utilization	Used	Available	Utilization	Note(s)
Logic Distribution				
Number of Slices containing only related logic	0	0	0%	
Number of Slices containing unrelated logic	0	0	0%	

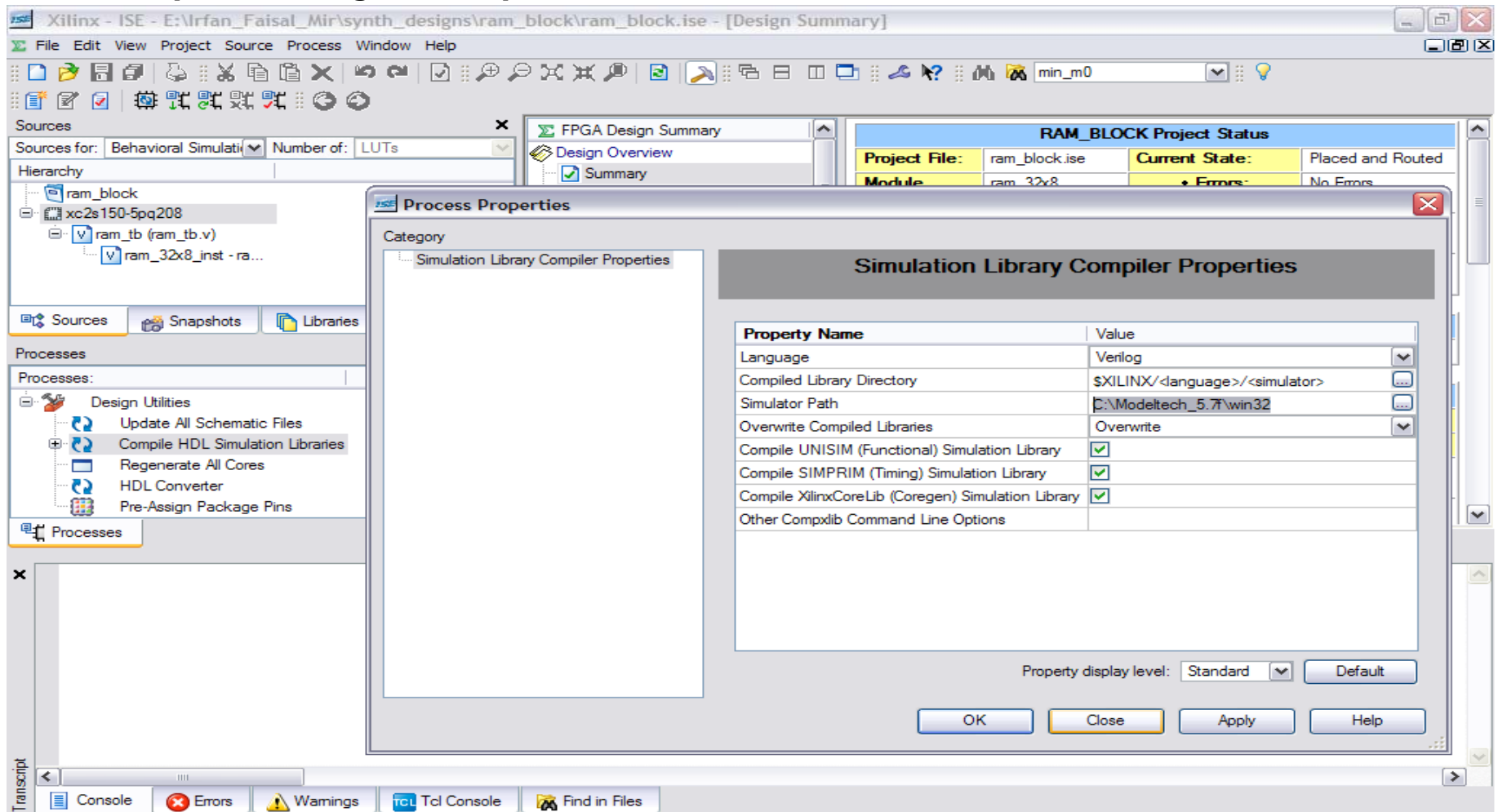
Design Example

- **Step7:** Load Simulation Libraries before Timing Simulation in ISE 8.2i
 - In “Compile HDL Simulation Libraries” properties menu...select verilog option and give the path of “win32 folder” of ModelSim SE Simulator.



Design Example

- **Step7:** Load Simulation Libraries before Timing Simulation in ISE 8.2i
 - In “Compile HDL Simulation Libraries” properties menu...select verilog option and give the path of “win32 folder” of ModelSim SE Simulator.



Design Example

- **Step7:** Load Simulation Libraries before Timing Simulation in ISE 8.2i
- Run the “Compile HDL Simulation Libraries”... It will compile “simprim, unisim, XilinxCoreLib libraries” in your current project.

The screenshot shows the Xilinx ISE 8.2i Design Summary window for a project named 'ram_block'. The 'Processes' pane on the left shows the 'Compile HDL Simulation Libraries' process highlighted. A context menu is open over this process, showing options: Run, Rerun, Rerun All, Stop, Open Without Updating, and Properties... The 'FPGA Design Summary' pane in the center shows the 'Design Overview' section with various reports checked. The 'Project Properties' section shows 'Enable Enhanced Design Summary' checked. The right pane displays the 'RAM_BLOCK Project Status' and 'Device Utilization Summary'.

RAM_BLOCK Project Status

Project File:	ram_block.isc	Current State:	Placed and Routed
Module Name:	ram_32x8	Errors:	No Errors
Target Device:	xc2s150-5pq208	Warnings:	No Warnings
Product Version:	ISE 8.2i	Updated:	Fri Jul 13 12:32:04 2007

RAM_BLOCK Partition Summary

No partition information was found.

Device Utilization Summary

Logic Utilization	Used	Available	Utilization	Note(s)
Logic Distribution				
Number of Slices containing only related logic	0	0	0%	
Number of Slices containing unrelated logic	0	0	0%	

Design Example

➤ Step7: Load Simulation Libraries before Timing Simulation in ISE 8.2i

- At the end of "Compile HDL Simulation Libraries" process, it will show the PASS (✓) or FAIL (✗) indication... Then highlight Post-Route Simulation option in Sources window..

The screenshot shows the Xilinx ISE 8.2i Design Summary window for a project named 'ram_block'. The 'Processes' pane on the left shows the 'Compile HDL Simulation Libraries' process completed successfully. The 'FPGA Design Summary' pane in the center shows the 'Design Overview' section with all items checked, including 'Summary', 'IOB Properties', 'Timing Constraints', 'Pinout Report', 'Clock Report', 'Errors and Warnings', 'Synthesis Messages', 'Translation Messages', 'Map Messages', and 'Place and Route Messages'. The 'Project Properties' section shows 'Enable Enhanced Design Summary' and 'Show Partition Data' checked. The 'RAM_BLOCK Project Status' pane on the right shows the project file 'ram_block.isc', module name 'ram_32x8', target device 'xc2s150-5pq208', and product version 'ISE 8.2i'. The 'RAM_BLOCK Partition Summary' pane shows 'No partition information was found.' The 'Device Utilization Summary' pane shows a table with logic utilization data.

Logic Utilization	Used	Available	Utilization	Note(s)
Logic Distribution				
Number of Slices containing only related logic	0	0	0%	
Number of Slices containing unrelated logic	0	0	0%	

The 'Transcript' pane at the bottom shows the following output:

```
> Log file C:\Xilinx\verilog\mti_se\XilinxCoreLib_ver\cxl_XilinxCoreLib.log generated
> Library mapping successful, setup file(s) modelsim.ini updated

compplib[XilinxCoreLib_ver]: No error(s), 4 warning(s)

Log file (compplib.log) generated.

Process "Compile HDL Simulation Libraries" completed successfully
```

Design Example

- **Step8:** Simulate Post-Place & Route Verilog Model of your Design in ISE 8.2i
 - First highlight Test Bench Top File in "Sources in Project"... you will see ModelSim Simulator options in "Processes for Source" small window.

RAM_BLOCK Project Status

Project File:	ram_block.isc	Current State:	Placed and Routed
Module Name:	ram_32x8	Errors:	No Errors
Target Device:	xc2s150-5pq208	Warnings:	No Warnings
Product Version:	ISE 8.2i	Updated:	Fri Jul 13 12:32:04 2007

RAM_BLOCK Partition Summary

No partition information was found.

Device Utilization Summary

Logic Utilization	Used	Available	Utilization	Note(s)
Logic Distribution				
Number of Slices containing only related logic	0	0	0%	
Number of Slices containing unrelated logic	0	0	0%	

Processes

Processes:

- Add Existing Source
- Create New Source
- ModelSim Simulator
- Simulate Post-Place & Route Model

Context Menu for 'Simulate Post-Place & Route Model':

- Run
- Rerun
- Rerun All
- Stop
- Open Without Updating
- Properties...

Transcript

```
> Log file C:\Xilinx\bin\isegui\XilinxCoreLib_ver\cxl_XilinxCoreLib.log generated
> Library mapping successful

compplib[XilinxCoreLib_ver]: No error(s), 4 warning(s)

Log file (compplib.log) generated.

Process "Compile HDL Simulation Libraries" completed successfully
```

Design Example

- **Step8:** Simulate Post-Place & Route Verilog Model of your Design in ISE 8.2i
 - Now Run the “Simulate Post-Place & Route Verilog Model” in “Processes for Source” small window.

The screenshot displays the Xilinx ISE 8.2i interface. The 'Processes' window on the left shows the process list with 'Simulate Post-Place & Route Model' selected. The 'FPGA Design Summary' window on the right shows the project status. The 'ModelSim SE 5.7f' watermark is overlaid on the center.

RAM_BLOCK Project Status

Project File:	Current State:	
ram_block.isc	Placed and Routed	
Module Name:	• Errors:	No Errors
Target:	• Warnings:	No Warnings
ISE 8.2i	• Updated:	Fri Jul 13 12:32:04 2007

RAM_BLOCK Partition Summary

Information was found.

Device Utilization Summary

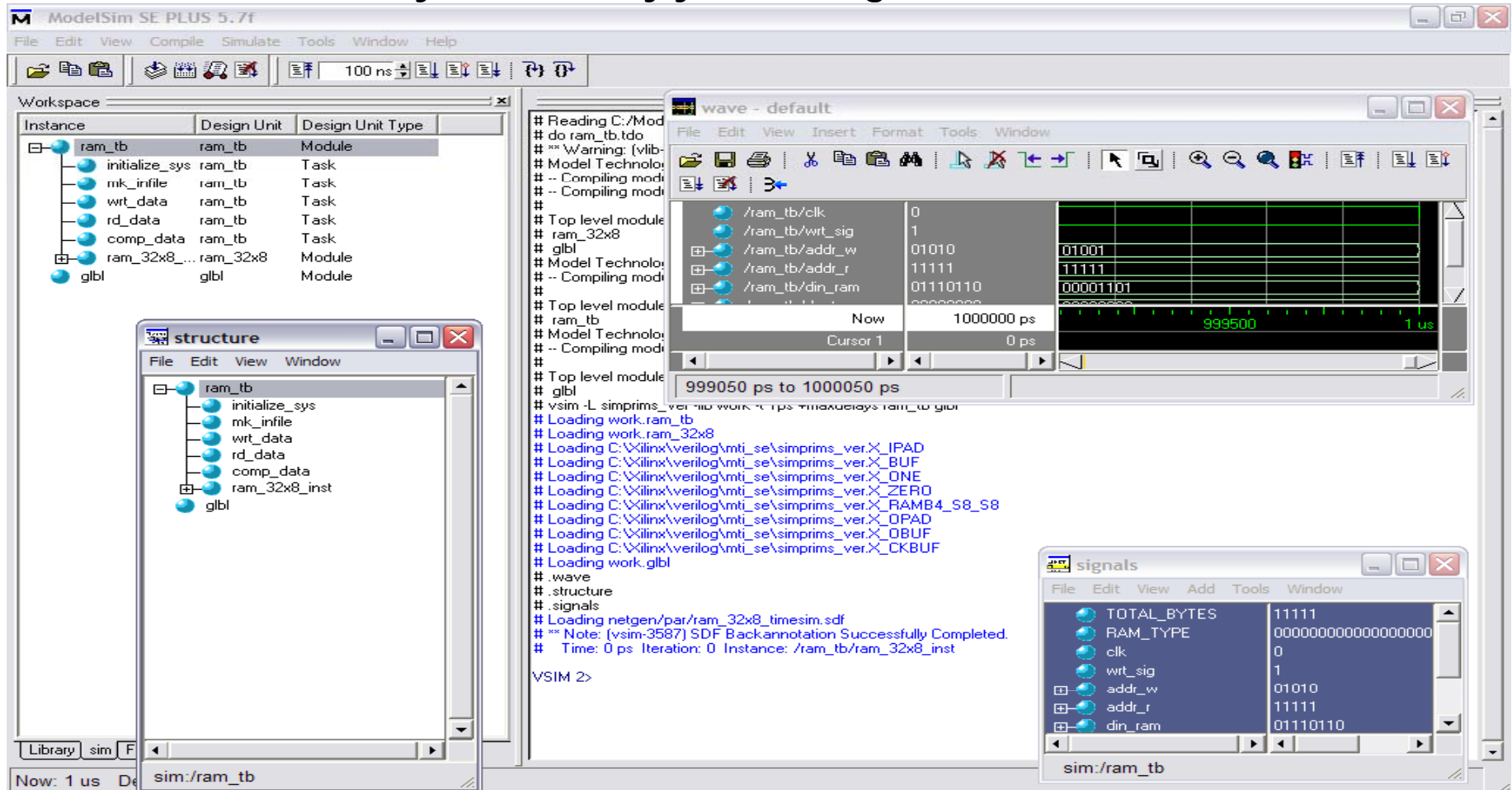
Category	Used	Available	Utilization	Note(s)
Logic	0	0	0%	
IOB	0	0	0%	

Transcript

```
Started : "Generate Post-Place & Route Simulation Model"
INFO:NetListWriters:633 - The generated simulation primitives and has correct compilation and simulation.
Process "Generate Post-Place & Route Simulation Model" completed successfully
```

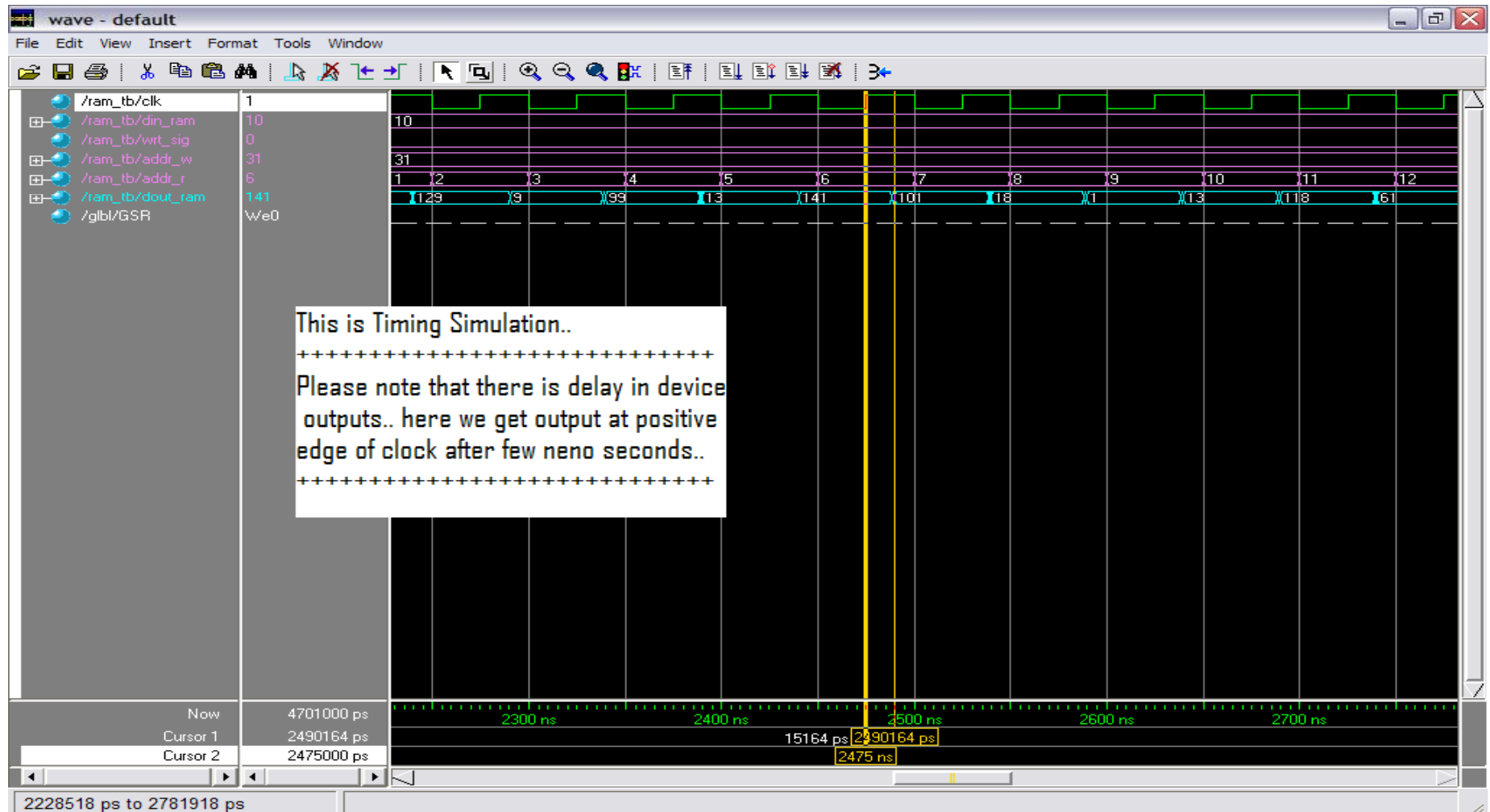
Design Example

- **Step8:** Simulate Post-Place & Route Verilog Model of your Design in ISE 8.2i
 - You see the ModelSim Simulator main window...Be sure that "SIMPRIMS_VER" & "UNISIMS_VER" & "XILINXCORELIB_VER" Libraries are installed. Now you can verify your Timing simulation.



Design Example

- **Step8:** Simulate Post-Place & Route Verilog Model for Timing Simulation of your Design in ISE 8.2i
 - You can verify your design timing by using Waveform Viewer in ModelSim..



Design Example

➤ Step9: Generate Programming File of your Design in ISE 8.2i

- Click on “Run” option of “Generate Programming File” in “Processes for Source” small window. In “properties...” option, you can change its options.

The screenshot displays the Xilinx ISE 8.2i interface. The 'Processes' window is open, showing the 'Generate Programming File' process. A right-click context menu is visible over this process, with the 'Run' option selected. The 'FPGA Design Summary' window is also open, showing the 'Design Overview' tab. The 'RAM_BLOCK Project Status' section indicates the project is 'Placed and Routed' with no errors or warnings. The 'Device Utilization Summary' table shows 0% utilization for the number of slices.

Project File:	Current State:
ram_block.isc	Placed and Routed
Module Name:	• Errors: No Errors
Target Device:	• Warnings: No Warnings
Product Version:	• Updated: Fri Jul 13 12:32:04 2007

No partition information was found.	
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Logic Utilization	Used	Available	Utilization	Note(s)
Logic Distribution				
Number of Slices containing only related logic	0	0	0%	
Number of Slices containing unrelated logic	0	0	0%	

Design Example

➤ Step9: Generate Programming File of your Design in ISE 8.2i

- At the end of "Generate Programming File" process, it will show the PASS (✓) or FAIL (✗) indication...

The screenshot displays the Xilinx ISE 8.2i Design Summary window for a project named 'ram_block'. The window is divided into several panes:

- Sources:** Shows the project hierarchy with 'ram_block' and 'xc2s150-5pq208' as the target device.
- Processes:** Lists the design processes, with 'Generate Programming File' highlighted and marked with a green checkmark, indicating successful completion.
- FPGA Design Summary:** A tree view showing the design overview (Summary, IOB Properties, Timing Constraints, Pinout Report, Clock Report) and errors/warnings (Synthesis Messages, Translation Messages, Map Messages, Place and Route Messages, Timing Messages, Bitgen Messages, All Current Messages).
- Project Properties:** A list of checkboxes for enabling various design summary features, such as 'Enable Enhanced Design Summary', 'Show Partition Data', and 'Show Errors'.
- RAM_BLOCK Project Status:** A table summarizing the project details.
- RAM_BLOCK Partition Summary:** A section indicating that no partition information was found.
- Device Utilization Summary:** A table showing the utilization of logic resources.
- Transcript:** A text area at the bottom showing the command 'Started : "Generate Programming File".' and the message 'Process "Generate Programming File" completed successfully'.

Project File:	ram_block.isc	Current State:	Programming File Generated
Module Name:	ram_32x8	• Errors:	No Errors
Target Device:	xc2s150-5pq208	• Warnings:	No Warnings
Product Version:	ISE 8.2i	• Updated:	Fri Jul 13 13:24:43 2007

Logic Utilization	Used	Available	Utilization	Note(s)
Logic Distribution				
Number of Slices containing only related logic	0	0	0%	
Number of Slices containing unrelated logic	0	0	0%	
Number of bonded IOBs	27	140	19%	
Number of Block RAMs	1	12	8%	
Number of GCLKs	1	4	25%	

Started : "Generate Programming File".
Process "Generate Programming File" completed successfully