PIC24H Engineering Samples Rev. A0 Silicon Errata

PIC24HJXXXGPXXX, (Rev. A0) Silicon Errata

The PIC24H Engineering Samples (Rev. A0) you received were found to conform to the specifications and functionality described in the following documents:

- DS70175 – "*PIC24H Family Data Sheet*"
- DS70157 – "*dsPIC30F/dsPIC33F Programmer's Reference Manual*"
- DS70046 – *"dsPIC30F Family Reference Manual"*

The exceptions to the specifications in the documents listed above are described in this section. The specific devices for which these exceptions are described are listed below:

- PIC24HJ64GP206
- PIC24HJ64GP210
- PIC24HJ128GP206
- PIC24HJ128GP506
- PIC24HJ256GP206
- PIC24HJ256GP610

PIC24H Rev. A0 silicon is identified by performing a "Reset and Connect" operation to the device using MPLAB® ICD 2 with MPLAB IDE v7.31 or later. The following text is then visible under the MPLAB ICD 2 section in the output window in MPLAB IDE:

```
Setting Vdd source to target
Target Device PIC24HJ256GP610 found,
revision = Rev 0x3000
...Reading ICD Product ID
Running ICD Self Test
...Passed
MPLAB ICD 2 Ready
```

The errata described in this section will be addressed in future revisions of silicon.

Silicon Errata Summary

The following list summarizes the errata described in further detail through the remainder of this document:

1. SPI with 1:1 Prescaler

   The SPI modules do not function correctly when the SPI clock prescale ratio is set to 1:1.

2. SPI Master Reception for Bit Rates above 8 Mbps

   SPI Master reception does not function correctly at bit rates higher than 8 Mbps, if the data is sampled at the middle of the serial clock period.

3. ADC with Sample/Hold CH3

   Sample/Hold amplifier CH3 does not function correctly for the Analog-to-Digital Converter modules.

4. LATC and LATD Reads

   The LATC and LATD register reads do not function.

5. DMA Single-Shot Mode

   The Direct Memory Access Single-Shot mode does not function correctly.

The following sections will describe the errata and work around to these errata, where they may apply.

1. Module: SPI with 1:1 Prescaler

The SPI1 and SPI2 modules do not generate any serial clock signals and, therefore, do not function correctly for the following values of the PPRE<1:0> (SPIxCON1<1:0>) and the SPRE<2:0> (SPIxCON1<4:2>) bits:

- PPRE = 11, SPRE = 111

Work around

Users may set up the SPI module with any prescale ratio other than 1:1.

2. Module: SPI Master Reception for Bit Rates above 8 Mbps

Master mode receptions using the SPI1 and SPI2 module do not function correctly for bit rates above 8 Mbps if the Master has the SMP bit (SPIxCON1<9>) cleared (Master samples data at the middle of the serial clock period).

In this case, the data transmitted by the Slave is received shifted right by one bit by the Master. For example, if the data transmitted by the Slave was 0xAAAA, the data received by the Master would be 0x5555 (0xAAAA shifted right by one bit).

Work around

Users may set up the SPI module so that the bit rate is 8 Mbps or lower.

Alternatively, the bit rate can be configured higher than 8 Mbps, but the SMP bit (SPIxCON1<9>) of the SPI Master must be set (Master samples data at the end of the serial clock period).

3. Module: ADC with Sample/Hold CH3

The Sample/Hold amplifier CH3 does not function correctly when used with the Analog-to-Digital Converter (ADC) modules. The corresponding conversion result is always read as 0x0000.

Work around

Do not use the Sample/Hold amplifier CH3 with the ADC1 or ADC2 module. You may use CH0, CH1 and CH2.

4. Module: LATC and LATD Reads

The LATC and LATD register reads do not function. Performing a read or read-modify-write operation on the LATC register or the LATD register will not function.

Do not perform read or read-modify-write operations on the LATC and LATD registers. Inspect the disassembly listing of any user application software that may be accessing the LATC or LATD register, to ensure that read or read-modify-write operations are not being performed on these registers.

To verify the contents of the LATC register, perform the following steps:

- Write to LATC
- Make a PORTC pin an output
- Read the PORTC register

The same steps can be performed to verify the contents of the LATD register.

Note: The Port pin state, and therefore the read value, depends on the load attached to the Port pin.

5. Module: DMA Single-Shot Mode

The DMA Single-Shot mode does not function correctly for more than one block transfer. After one block transfer, the DMA channel becomes unusable until a device reset occurs.

Work around

If more than one DMA data block transfers are required during the entire program execution, the user application may set up the required DMA channel to operate in Continuous mode, and disable the DMA channel every time the corresponding DMA interrupt has occurred.

However, if only one DMA data block transfer is required for a particular DMA channel during the entire program execution, the Single-Shot mode may be used.

APPENDIX A: REVISION HISTORY

Revision A (2/2006)

First release of the document.

NOTES:

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