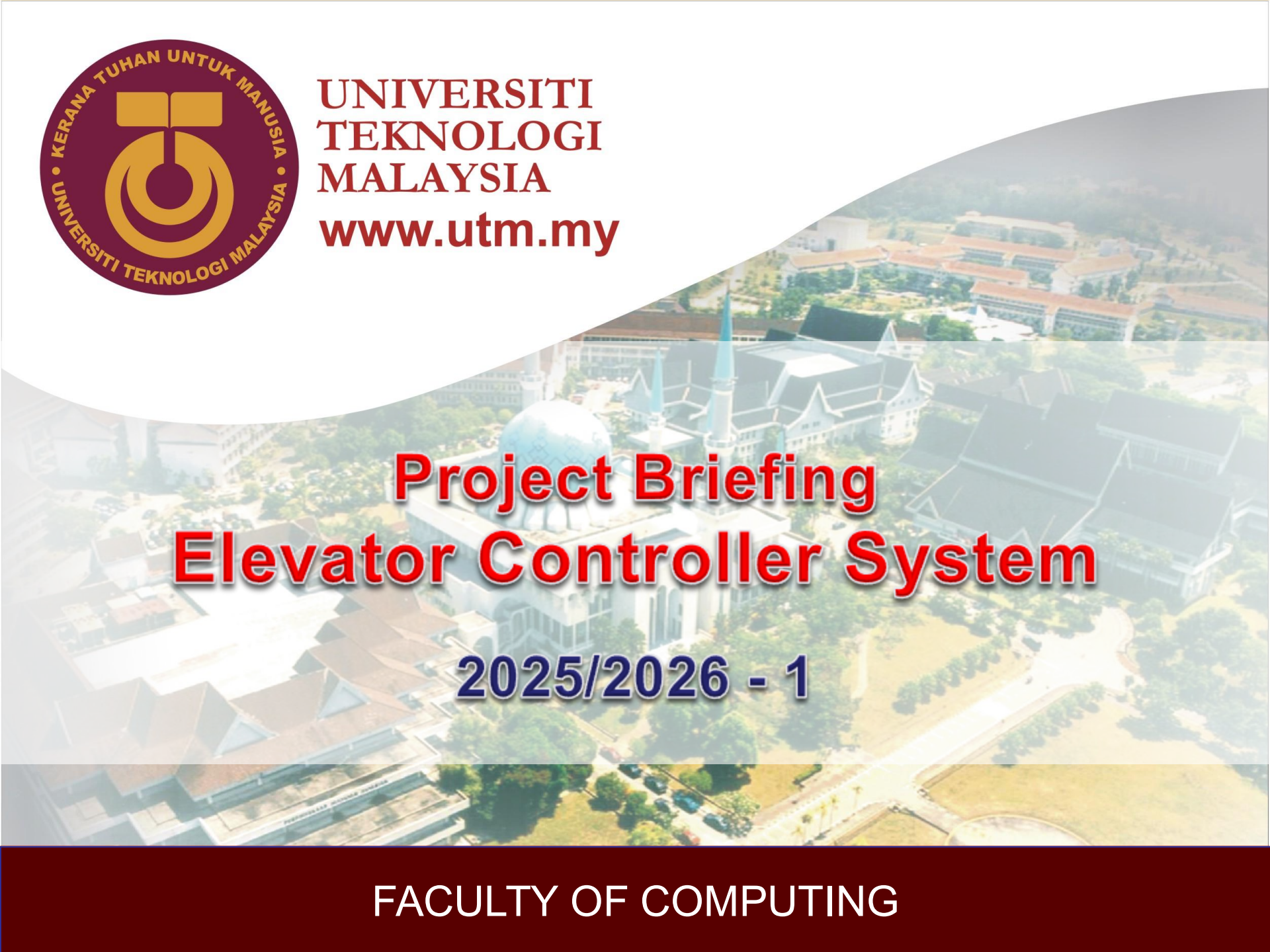

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Project Briefing
Elevator Controller System

2025/2026 - 1

FACULTY OF COMPUTING

Overview

- The project is to implement knowledge from this course by simulating an imaginary case study.
- The project is done in a group of 3 or 4 students
- Strategies used:
  - Group self explore
  - Creative problem solution and design
  - Good reporting and presentation

Case Study

To design an electronic controller for elevator / lift in a hotel building

Case Study

- Scenario:
  - A hotel visitor will use the elevator to go up / down from one level to another
  - The visitor will key in the desired level to go, tag the visitor room card, close the elevator door and push UP / DOWN button
  - Then the elevator will go UP / DOWN by counting UP / DOWN one level to another until it reaches to desired level

Scenario

Lift UP

- Key in level up
- Tag in card hotel
- Door Close
- Lift goes up to destination
- Lift stop at destination
- Door Open

Lift DOWN

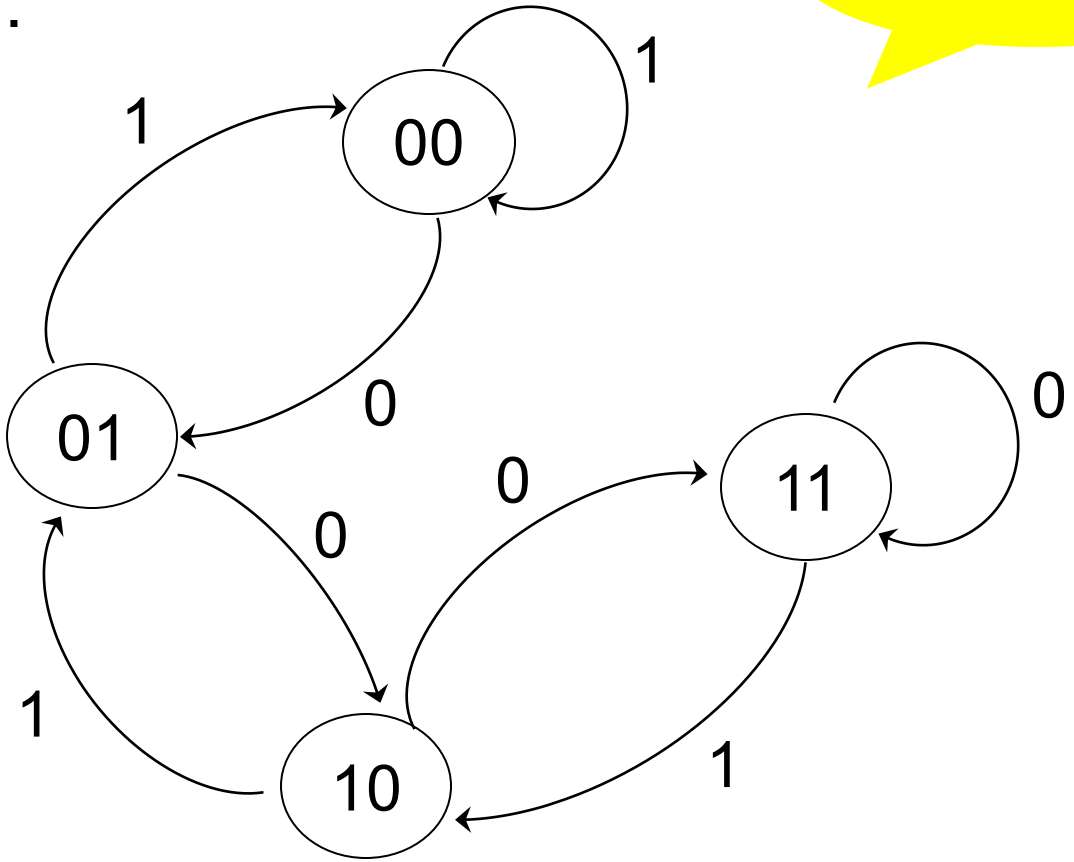
- Key in level down
- Tag in card hotel
- Door Close
- Lift goes down to destination
- Lift stop at destination
- Door Open

Basic Design

- 4 floor elevator system
  - For level 0, 1, 2, and 3
  - Use 2-bit up/down counter
    - 0 = count UP
    - 1 = count DOWN
  - Function in synchronous mode
  - Uses D flip flop

Basic Design

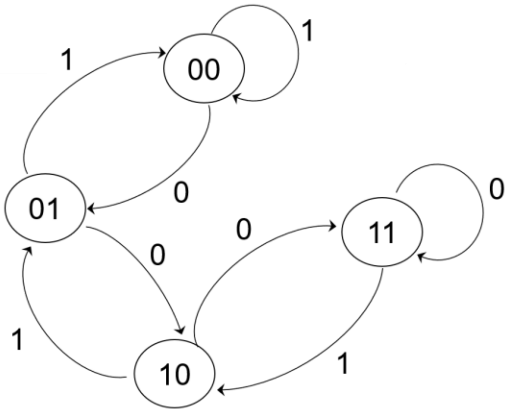
- State diagram:



Basic Design

- Next State and flip flop transition table:

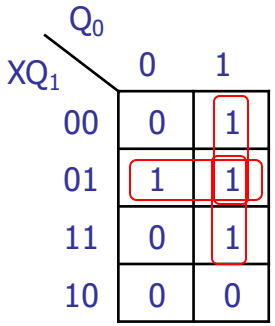
Input, X	Present State		Next State		D FF	
	$Q1_n$	$Q0_n$	$Q1_{n+1}$	$Q0_{n+1}$	D1	D0
0	0	0	0	1	0	1
0	0	1	1	0	1	0
0	1	0	1	1	1	1
0	1	1	1	1	1	1
1	0	0	0	0	0	0
1	0	1	0	0	0	0
1	1	0	0	1	0	1
1	1	1	1	0	1	0



Basic Design

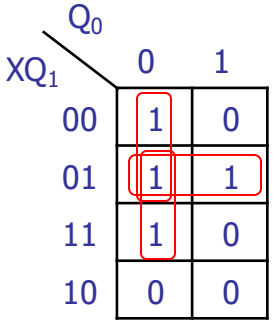
- K-map:

Input, X	Present State		Next State		D FF	
	$Q1_n$	$Q0_n$			D1	D0
0	0	0			0	1
0	0	1			1	0
0	1	0			1	1
0	1	1			1	1
1	0	0			0	0
1	0	1			0	0
1	1	0			0	1
1	1	1			1	0



D_1

$$D_1 = \bar{X}Q_0 + \bar{X}Q_1 + Q_1Q_0$$



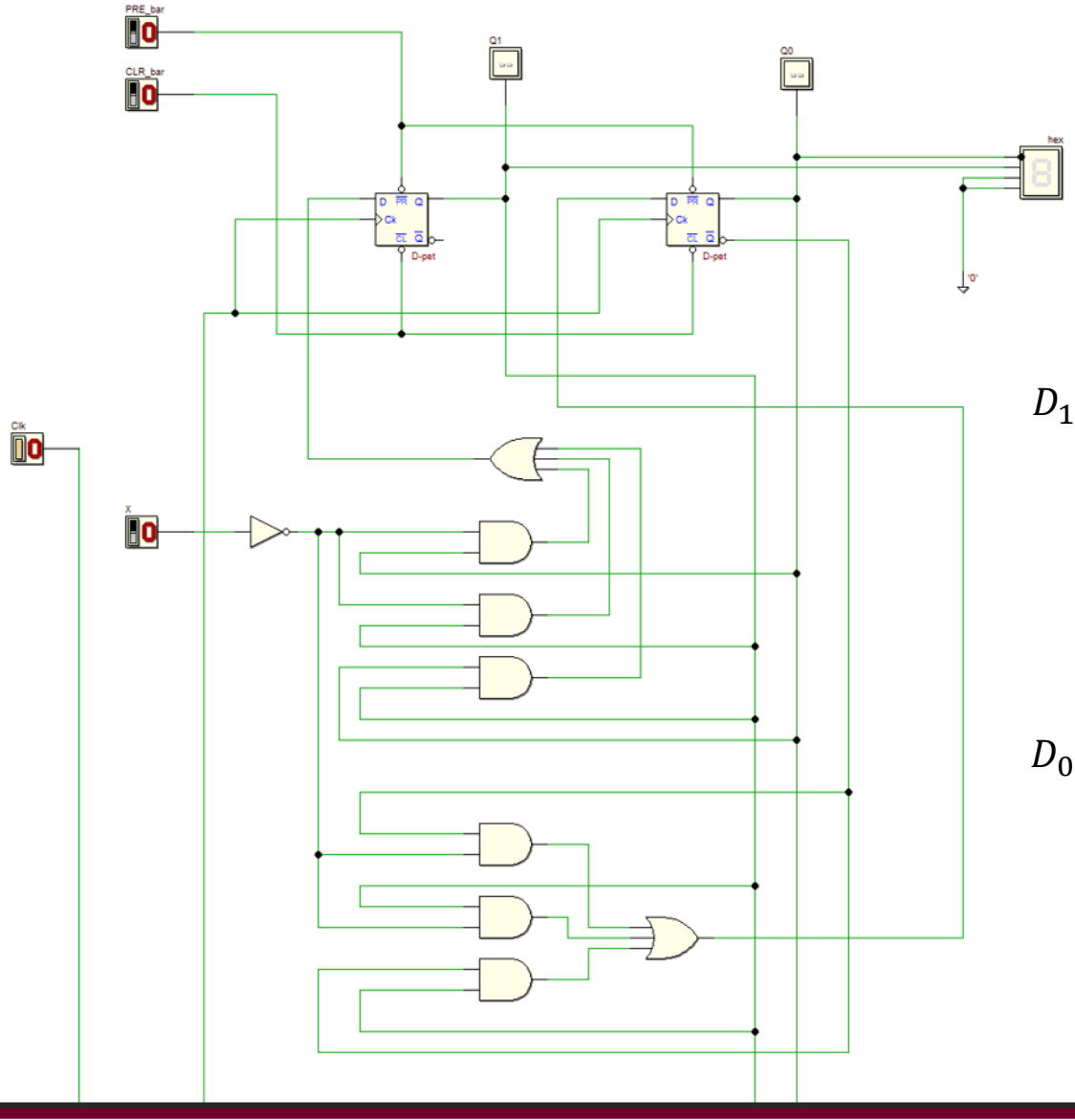
D_0

$$D_0 = \bar{X}\overline{Q_0} + \bar{X}Q_1 + Q_1\overline{Q_0}$$

Basic Design in DEEDS

- Flip-flop using D Flip-flop
- Comparator for current state and targeted level floor using XNOR and NAND
- Pattern detector for clock enabler using AND gate.
  - If output AND gate is HIGH, clock is enabled, and counter can run.
- Use push button instead of clock generator.
  - This is to eliminate undesirable state during states transition

Design in DEEDS



2-bit UP / DOWN counter using D flip flops

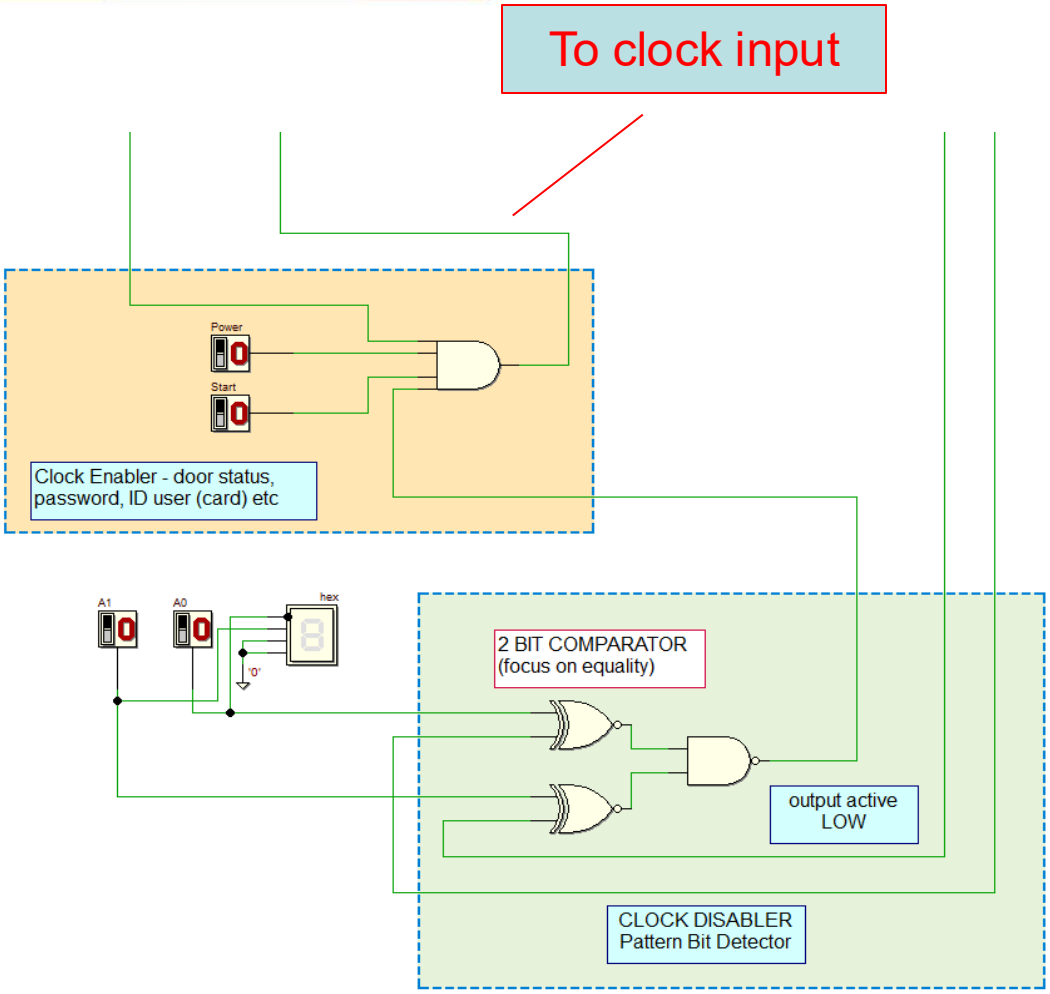
$$D_1 = \bar{X}Q_0 + \bar{X}Q_1 + Q_1Q_0$$

XQ_1 \ Q_0	0	1
00	0	1
01	1	1
11	0	1
10	0	0

$$D_0 = \bar{X}\overline{Q_0} + \bar{X}Q_1 + Q_1\overline{Q_0}$$

XQ_1 \ Q_0	0	1
00	1	0
01	1	1
11	1	0
10	0	0

Design in DEEDS



Clock Enabler and Comparator

Rule

1. Clock to the counter will be enabled when **HIGH** output goes to **clk** input at D flip-flop.
2. Gate **AND** will goes **HIGH** when CLK (push button) is HIGH **and** Power is HIGH **and** Start is HIGH **and** output comparator **IS NOT EQUAL**.
3. If comparator is **equal**, then NAND gate will generate output **LOW**, thus will **disable** the **clock** to D flip-flop.

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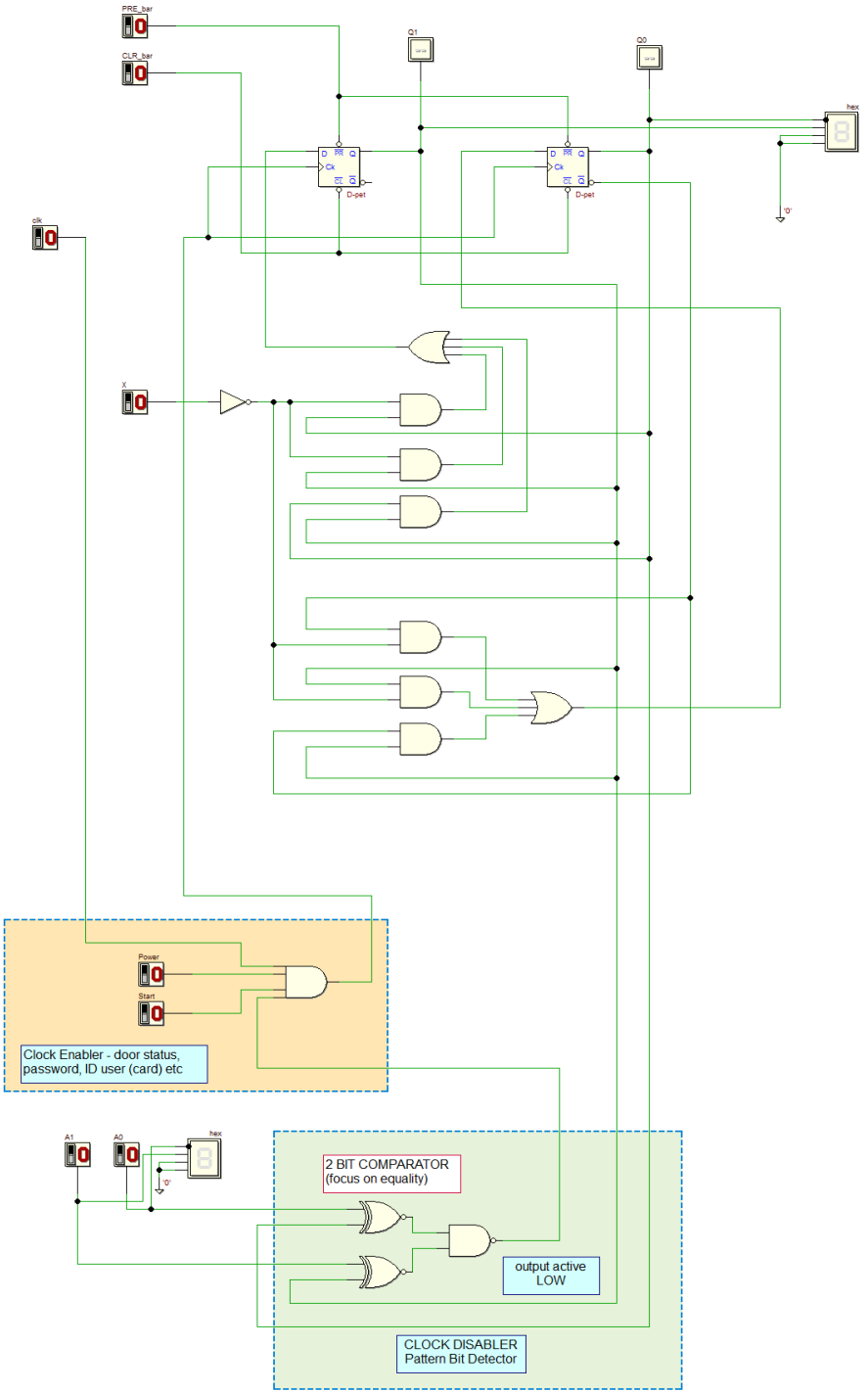
Operation:

Set value (UP)

- PRE_bar=CLR_bar= 1
- X=0 (count up)
- Power=1
- Give desired floor, e.g = 3 (from current floor = 0)
- Start=1
- Push clock button (Clk), counter will do count up from initial (current 0) to desired floor 3.

Set value (Down)

- PRE_bar=CLR_bar= 1
- X=1 (count down)
- Power=1
- Give desired floor, e.g = 0 (from current floor =3)
- Start=1
- Push clock button (Clk), counter will do count down from initial (current 3) to desired floor 0.



Your job …

- You must enhance the previous design to 3-bit synchronous counter (count UP/DOWN) to support 8 floors hotel elevator.
- Thus, must show 4 inputs K-map, i.e., X, Q_2, Q_1, Q_0 to design the counter circuit and related states / flip flop transition tables.
- Use JK flip flop in your circuit design.

Your job …

- Introduce these features to the input controller:
  - to detect visitor card hotel
  - to indicate door open / close
  - to use passcode

PROJECT REPORT CONTENT

- Background / overview
- Problem Statement
- Suggested Solution
  - must include all the diagrams / tables and explain
  - … state diagram, state table, transition table
- System Implementation (must include DEEDS drawing and explain)
- Conclusion and Reflection
  - Summarizes the whole project. Write your reflections.
  - Describe your achievements, strength and weaknesses.
  - Propose future work to improve your design

Report Format

Format

- Times New Roman 12 font size
- 1.5 spacing

What should be in the report?

- TITLE PAGE
- DEDICATION & ACKNOWLEDGEMENT
- TABLE OF CONTENTS
- REPORT CONTENT
- REFERENCES
- APPENDICES

Under Appendices:

- List of tasks distribution among members of group
- Photo(s) of your group working together
- And others supporting materials that will strengthen the explanation of your project.

DEMO VIDEO

- Prepare 15 minutes video to demo / demonstrate your project outcome
- Explain how you run the circuit simulation
- Produce the demo video in mp4 format
- Upload the demo video to elearning

Submission

- Project report
- Deeds source file (*.pbs)
- Demo video

- DUE: 25 January 2025 (end of study leave week)

- Submit via *https://elearning.utm.my/*