Tutorials

TUTORIAL 1: Digital Logic Overview

1. Fill in the terms for the definition.

Term	Definition
i)	Being continuous or having continuous values.
ii)	A basic logic operation in which a true (HIGH) output occurs only when all the input conditions are true (HIGH).
iii)	The basic timing signal in digital system.
iv)	Related to digits or discrete quantities.
v)	A sudden change from one level to another, followed after a time, called the pulse width, by a sudden change back to the original level.
vi)	The time interval on the leading edge of a pulse between 10% and 90% of the amplitude

2. Find the duty cycle of a digital waveform if the period is twice the pulse width.

3. Name the device that is use for

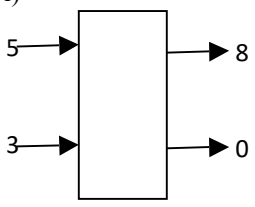
   i. converting a binary number to 7-segment display format.

   ii. data storage.

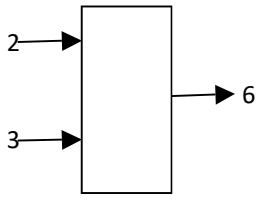
4. A basic 2-input logic circuit has a HIGH on one input and a LOW on the other input, and the output is LOW. Identify the circuit.

5. Name the logic function of each of the block below based on your observation of the inputs and outputs.

i)



ii)



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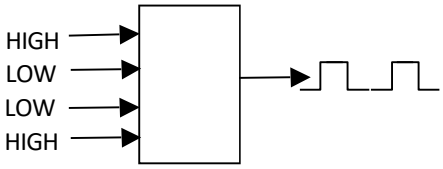


6. A pulse waveform with a frequency of 10 kHz is applied to the input of a counter. During 100ms, how many pulses are counted?

7. A periodic digital waveform has a pulse width of 25 μs and a period of 150 μs. Determine the frequency and the duty cycle.

8. i) List 3 main advantages of a digital system compared to an analog system.

ii) An _____ is required to convert an analog signal to a digital signal, and a system that consist of both analog and digital circuits is called a _____ system

iii) The smallest unit in a digital systems is called _____

iv) Determine wheter the following is an analog or a digital quantities, circle the right answer

1) A person weight ***Analog / Digital***
2) Number of cars at the parking lot ***Analog / Digital***
3) Storage capacity of a memory ***Analog / Digital***
4) Tyre pressure ***Analog / Digital***

9 i) Determine the frequency of a waveform in Fig 1 if T is 10ms.

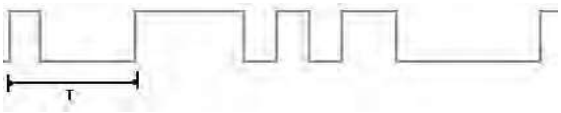


Fig 1

ii) Draw a digital waveform to represent the following digital value 1000101110 (left value first),if the pulse width is 1µs, determine the duration of each bit before it change to a new bit.

10. How many times the digital logic level changed in 1 second if the signal is a square wave with a frequency of 1MHz.

11. Draw a square wave with 25% duty cycle and clearly label the positive edge and the trailing edge.

12. List the suitable logical function for the following problems

i) sending multiple input to a destination using a single cable : _____

ii) converting a key press on a keypad to a BCD code : _____

iii) determine the number of visitors to an expo : _____

iv) determine whether a car exceed the speed limit : _____

v) routing a different packet for a designated destination : _____

vi) memorize characters type on a keyboard : _____

13. What is the difference between a fixed function IC compared to programmable IC

14. Determine which gate has the following property, assume FALSE = 0 and TRUE = 1

a. Output is opposite of the input
b. If both input FALSE then the output will be FALSE
c. If one of the input FALSE the output will be FALSE

TUTORIAL 2: Number Systems and Codes

1. Convert the binary numbers to its decimal equivalent.
   a. 10110_2
   b. 10010101_2
   c. 1101011_2
   d. 100100001001_2
   e. 100101100_2
2. Convert the decimal numbers to its binary equivalent using **repetitive division method**.
   a. 77_{10}
   b. 96_{10}
   c. 205_{10}
   d. 1040_{10}
   e. 3216_{10}
3. Convert the decimal numbers in Question (2) to its binary equivalent using **weighted summation** method.
4. Convert the decimal numbers to its binary equivalent (to four radix point)
   a. 1305.375_{10}
   b. 111.33_{10}
   c. 301.12_{10}
   d. 164.875_{10}
   e. 1000.01_{10}
5. Convert the hexadecimal numbers to its decimal equivalent.
   a. 743_{16}
   b. 2000_{16}
   c. $7FF_{16}$
   d. $ABCD_{16}$
   e. 165_{16}
6. Convert the decimal numbers to its hexadecimal equivalent.
   a. 59_{10}
   b. 1024_{10}
   c. 2313_{10}
   d. $65{,}536_{10}$
   e. 919_{10}

7. Convert the octal numbers to its decimal equivalent.
   a. 56_8
   b. 467_8
   c. 1000_8
   d. 2341_8
   e. 31456_8
8. Convert the decimal numbers to its octal equivalent.
   a. 59_{10}
   b. 1024_{10}
   c. 2313_{10}
   d. 65536_{10}
   e. 919_{10}
9. When a large decimal number is to be converted to binary, it is **sometimes** easier to convert it to hex and then from hex to binary. Try this procedure for 3216_{10} and compare it with the procedure used in Question (2).
10. Convert the binary numbers in Question (1) to
    a. hexadecimal
    b. octal
11. Convert the binary numbers to its equivalent hexadecimal and octal values.
    a. 10111010100.101
    b. 1000001101111.01
12. Encode the decimal numbers in BCD.
    a. 77_{10}
    b. 96_{10}
    c. 205_{10}
    d. 1040_{10}
    e. 3216_{10}
13. The following numbers are in BCD. Convert them to decimal.
    a. 100101110101010010
    b. 010101010101
    c. 0111011101110101
14. Which of the following numbers are valid BCD values?
    a. 0110101100110001
    b. 1001110000001000
    c. 00000000000

15. What is the largest BCD-encoded decimal value that can be represented in three bytes?

16. For the question below please refer to the ASCII table.

    a. What is the most significant nibble of the ASCII code for letter E?

    b. Represent the statement "X = 3 × Y" in ASCII code. Attach each character values with even parity bit.

    c. The following bytes (shown in hex) represent a person's name as it would be stored in the computer's memory. Determine the name of each person.

        i. 42 72 61 64 20 50 69 74 74

        ii. 41 6E 67 65 6C 69 6E 61

17. Calculate the lower and upper bound of signed number for 7-bit number system using the representation of

    a. sign and magnitude

    b. 1's complement

    c. 2's complement

18. Calculate the binary signed values in the representation format of (i) sign and magnitude, (ii) 1's complement and 2's complement using 8-bit number system.

    a. $+ 55_{10}$

    b. $+ 127_{10}$

    b. $- 87_{10}$

    c. $- 128_{10}$

19. Given a number system specification: **size of a number is 6 bit, including the sign bit AND signed numbers using 2's complement**

    Calculate and show your working for the arithmetic operations below.

    a. 18 + 3

    b. -18 + 3

    c. 18 – 3

    d. -18 - 3

TUTORIAL 3: Logic Gates Overview

1. For a 2-input NOR gate functioning as a negative-AND gate, output X is HIGH if both inputs A and B are HIGH.

   TRUE / FALSE

2. A two-input XNOR gate will produce a HIGH output when both inputs are equal.

   TRUE / FALSE

3. A NOR gate with inverters at the inputs has the same logic function as an AND gate.

   TRUE / FALSE

4. A 2-input NAND gate and a 2-input NOR gate produces the same output when both inputs are HIGH.

   TRUE / FALSE

5. The _____ gate produces a HIGH output when all inputs are LOW.

   a. NOR

   b. NAND

   c. XOR

   d. AND

6. A 2-input logic gate **X** produces a HIGH output when input A is LOW and input B is HIGH. Which of the following is **NOT** logic gate **X**?

   a. OR

   b. NOR

   c. NAND

   d. XOR

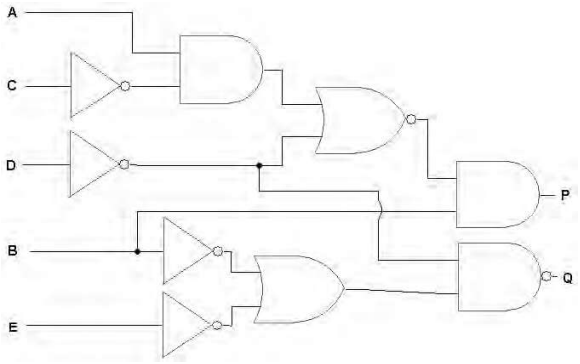
7. Complete the following questions:

   i) Draw the logic symbol of an XOR gate.

   ii) Give appropriate labels to the inputs and output.

   iii) Write its truth table.

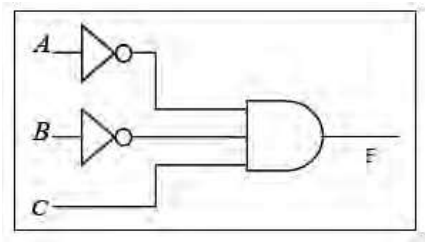
8. Write the Boolean expressions of output P and Q.

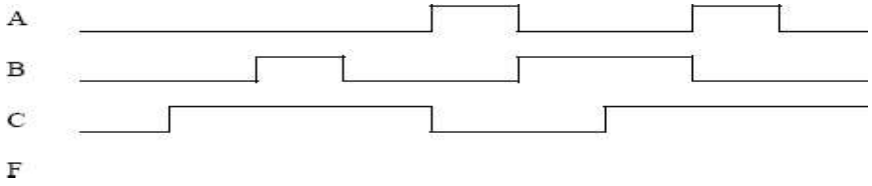


P = ?

Q = ?

9. Complete the timing diagram based on the given input for the following logic diagram.





10. Draw symbol for the following gates:

i) 2-input AND gate

ii) 2-input OR gate

iii) Inverter

iv) 2-input NAND gate

v) 2-input NOR gate

11. Given an AND gate with 3 inputs, what should the input values be to get an output of 1 (HIGH)?

12. Given an OR gate with 3 inputs, what should the input values be to get an output of 1 (HIGH)?

13. Fill in the table below, follow the example given.

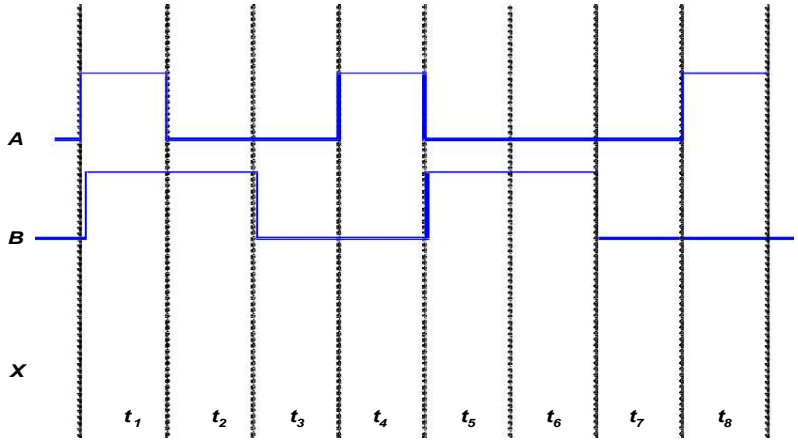
Gate	Input			Output
	A	B	C	
AND	1	0	1	
OR	0	1	0	
AND	1	1	1	
OR	0	0	0	X = A + B + C = 0 + 0 + 0 = 0
NOR	1	1	1	
AND	1	0	0	

14. Given the input waveform(s) below, show the appropriate output waveform, ***X***, with a timing diagram.

    i) XNOR

    ii) XOR

    iii) NAND



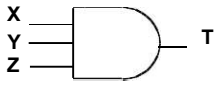
15. Identify the following devices according to logic function:

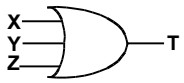
    i) 74LS04

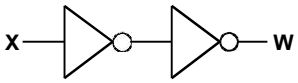
    ii) 74ALS10

    iii) 74HC00

16. Given the logic gates below, write the logic expression for it.

    i) 

    ii) 

    iii) 

TUTORIAL 4: Boolean Algebra and Logic Simplification

1. Using any logic gates, draw the logic diagram of the given function. Do NOT simplify the function

$$X = \overline{A} + B(D + \overline{E}\,\overline{F})(\overline{A + C})$$

2. Directly apply DeMorgan's law to the following expressions. You do NOT have to simplify the expressions.

i) $Y = \overline{(A + \overline{B} + C)} + \overline{\overline{C}\,D\,\overline{E}}$

ii) $Y = \overline{P + \overline{Q}\,(\overline{R + S\,P})}$

3. Simplify the function using Boolean Algebra

$$Y = A\,B\,\overline{C} + A\,\overline{B} + A\,B\,C + \overline{A}\,\overline{B}$$

4. Develop a truth table for the following expression. From the truth table derive a standard product-of-sums (POS) expression.

$$f = (A + \overline{B})(A + C)(A + B + \overline{C})$$

5. Use a Karnaugh map to reduce the expression to a minimum sum-of-products (SOP) form

$$f = \overline{A}\,B(C\,\overline{D} + C\,D) + A\,C\,D$$

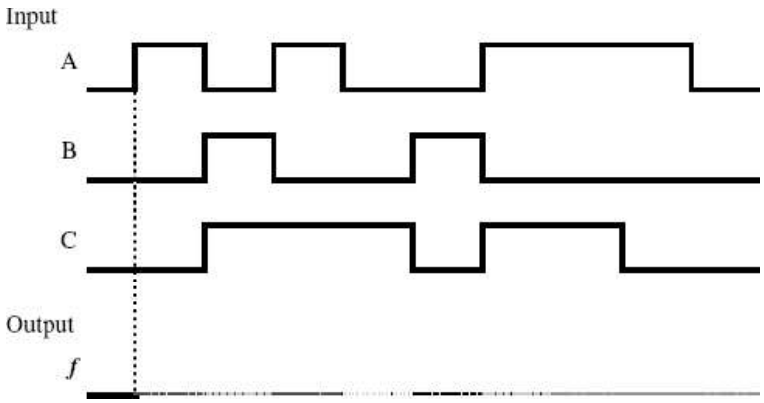
6. For the truth table given below,

A	B	C	f
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

i) Express the output function, f in Standard Sum-of-Products (SOP) form.

ii) Express the output function, f in Standard Product-of-Sums (POS) form.

iii) If the following waveforms are applied to the inputs, A, B, and C of the logic circuit, draw the output waveform for the function, f.



7. Below is the truth table of a three-input XOR gate.

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

i) Express Y in standard sum-of-product (SOP) variable form.
ii) Express Y in standard product-of-sum (POS) variable form

8. Construct the truth table for

$$Y = A\overline{BC} + \overline{AB}\,C + \overline{AC}\,B$$

9. Using any logic gates, draw the logic diagram of

$$P = \overline{\overline{(X + Z)} + \overline{Y}(W + \overline{XZ})}$$

10. Using Karnaugh Map,find the minimum SOP expression for the following function

i)

$$Y = \overline{P}\,\overline{Q}\,\overline{R}\,\overline{S} + \overline{P}\,\overline{Q}\,\overline{R}\,S + \overline{P}\,\overline{Q}\,R\,\overline{S} + P\,\overline{Q}\,\overline{R}\,\overline{S} + P\,\overline{Q}\,\overline{R}\,S + \overline{P}\,Q\,\overline{R}\,\overline{S} + P\,Q\,\overline{R}\,\overline{S}$$

ii)

$$G(w, x, y, z) = \sum m(1, 3, 14, 15) + d(0, 2, 6, 8, 13)$$

11. Implement $Y = \overline{a}(b + \overline{d}(\overline{\overline{ac} + e}))$ using any type of logic devices

12. Using Karnaugh Map, find the minimum SOP of the given m-notation

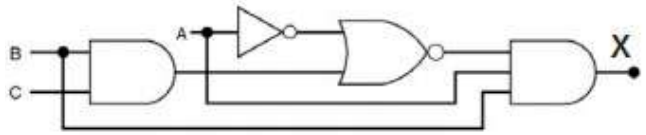
$$F(p, q, r) = \sum m(0,1,3,4,6)$$

13. Prove that

$$x\,y + x\,\overline{y} + \overline{x}\,\overline{y} = x + \overline{y}$$

TUTORIAL 5: Combinational Logic Circuit

1. Draw the logic circuit for the following using only **2-input AND gates**, **2-input OR gates** and **inverters.**
   a. $(A\overline{B}C + D\overline{E})$
   b. $(D\overline{E}F + A\overline{B})C$
   c. $(\overline{A} + \overline{B} + \overline{C})(\overline{D} + \overline{E} + \overline{F})$
   d. $A\overline{B}(\overline{C} + \overline{D})$
   e. $(\overline{A}\overline{B} + C + D)\overline{E}F$
2. Convert the circuits in Question 1a, 1b,and 1d, using only **NAND** gates.
3. Convert the circuits in Question 1c and 1e, using only **NOR** gates.
4. Convert the following circuit to NAND only then prove that the converted circuit is the same as the original circuit.



5. Referring to truth table below, draw the circuit to implement the function using
   i) AND-OR
   ii) AND-OR-Invert

Inputs			Output
A	**B**	**C**	**X**
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

DESIGN EXERCISE

For each of the given problems, do the following:

a. Determine the input, output and the relationship between output and the input
b. Create the truth table or Boolean expression
c. From the truth table or Boolean expression, gets the simplified expression using a Karnaugh map(s) or Boolean Algebra.
d. Draw a logic circuit for the simplified expression using only 2-input AND gates, 2-input OR gates and inverters.
e. Re-draw the simplified logic circuit using only NAND gates for POS and NOR only for SOP.
f. Re-draw the simplified logic circuit using dual symbol

1. Car Safety Alarm

- Design a car safety alarm considering four inputs
  - Door closed (D)
  - Key in (K)
  - Seat pressure (S)
  - Seat belt closed (B)
- The alarm (A) should sound if
  - The key is in and the door is not closed, or
  - The door is closed and the key is in and the driver is in the seat and the seat belt is not closed

2. A Majority High

- Design a circuit that will give a HIGH output (F), when the majority of the 3 inputs are HIGH

3. Elevator Door Control

- Design a logic circuit that controls an elevator door in a three-story building, considering the following inputs
  - Elevator moving (M)
    - M = 1 : elevator is moving
    - M = 0 : elevator has stopped
  - F1, F2, F3 :- floor indicator
    - HIGH when elevator is positioned at the level of the particular floor
    - F2 = 1 : elevator at level with floor 2. F1 = F3 = 0.
- The circuit output is the OPEN signal.
  - OPEN = 1 : elevator door will open.

4. **Sound the Horn**
   - A manufacturing plant needs to have a horn sound to signal quitting time. The horn should be activated when either of the following conditions is met:
     - It is after 5 p.m. and all machines are shut down.
     - It is Friday, the production run for the day is complete, and all the machines are shut down.
   - Design a logic circuit that will control the horn. (Hint: use four logic input variables to represent various conditions; for example, input A will be HIGH only when the time of day is 5 p.m. or later.)

5. **BCD Counter**
   - A BCD counter that produces 4 bits output, representing the BCD code for the number of pulses that have been applied to the counter input. For example, after 4 pulses have occurred, the counter outputs are *DCBA* = $0100_2 = 4_{10}$. The counter resets to zero on the tenth pulse and starts counting over again. In other words, the DBCA outputs will be never represents a number greater than $1001_2 = 9_{10}$.
   - Design the logic circuit that produces a HIGH output whenever the count output is 2, 3 or 9

6. **Conditional Output**

   The circuit has 4 inputs, labelled as ABCD, where A is the MSB and D is the LSB. The inputs represent a number in a 2's complement form. You are required to design a circuit that has the following characteristic

   a) When B = C = 0, the output will be LOW
   b) Other than condition a), when the input value is **positive odd** or **negative even**, the output will be HIGH.
      Positive odd is positive numbers that are odd and negative even is negative numbers that are even.
   c) The condition where all input 1's does not exist in the system

7. **Count numbers of 1's at the input**
   Input to the system is a binary number that can have a value of 0 to 7. Count the number of 1 at the input and display it at as a two bit binary number. For example if the input is 5 it will be input as 101, and the number 1's at the input are 2 therefore the output is 10 (two in binary).

TUTORIAL 6: Functions of Combinational Logic

1. What are the **equations** to retrieve the sum (**Σ**) and the carry output ($\mathbf{C_{out}}$) of a full adder?
2. How **many full adders** are needed to complete these additions?
    a. 101 and 010
    b. 1100 and 0101
    c. 111 and 001
    d. 1010 and 1101
    e. 010 and 011
    f. 11001 and 10101

3. For Question 3 (Show your workings):
    a. Draw the block diagram of parallel adders for Question 3
    b. Get *every instance* of sum (**Σ**) and carry output ($\mathbf{C_{out}}$) for each full adder.
    c. Get the results.

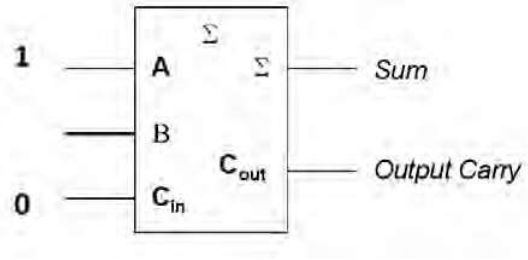
4. Use the parallel adder truth table (Table 1) to find the sum and output carry for the addition of the following two 4 bit number if the input carry (C_{n-1}) is 0. Show the diagram.

$X_4 X_3 X_2 X_1 = 1101$ $\quad\quad$ $Y_4 Y_3 Y_2 Y_1 = 0101$

Table 1

X_n	Y_n	C_{n-1}	C_n	$\sum_n$
0	0	0	0	0
0	1	0	0	1
1	0	0	0	1
1	1	0	1	0
0	0	1	0	1
0	1	1	1	0
1	0	1	1	0
1	1	1	1	1

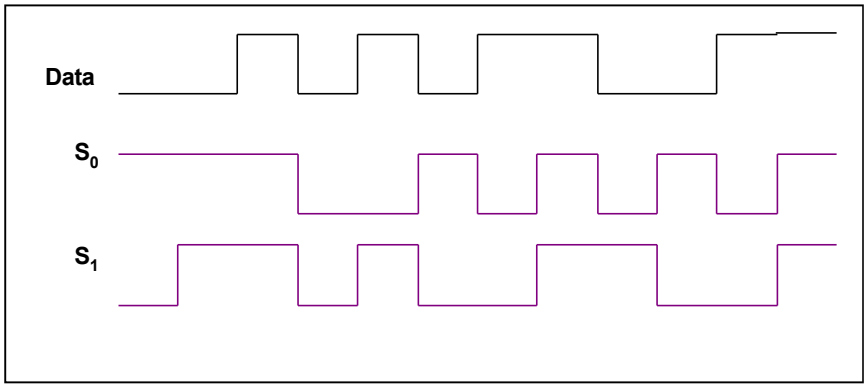
5. Determine the outputs of **Sum** and **Output Carry** for the inputs given for Full Adder as shown below.



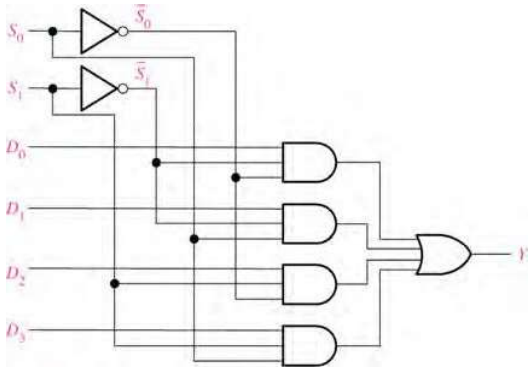
6. Implement the function f(A,B,C) = Σ(0, 2, 4, 7) using a 4 x 1 multiplexer.

7. Convert the following:
   a. 98 in BCD to binary
   b. 01110101 in BCD to binary

8. A DEMUX has 4 outputs D0, D1, D2 and D3. Given the information below, draw the appropriate waveforms for the outputs.



9. a) What type of multiplexer shown in a figure below.
   b) Develop the truth table for multiplexer in figure below.



10. What is the difference between **decoder** and **multiplexer**.

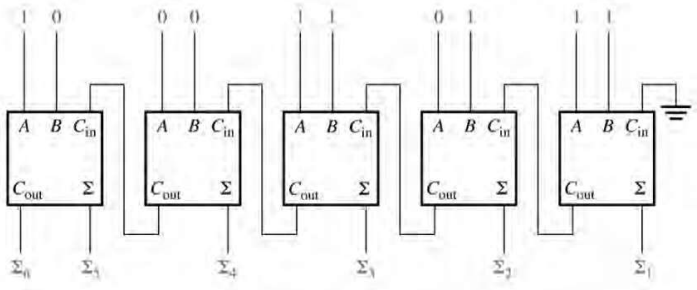
11. Design :
    a. BCD-to-decimal decoder using the minimal number of 2-input AND gates
    b. Repeat, using two 2-to-4-line decoders and a few interconnecting AND gates

12. Using a full-adder, determine the logic state (1 or 0) at each gate output for the following inputs:
    (a) $A = 1, B = 1, C_{in} = 1$
    (b) $A = 0, B = 1, C_{in} = 1$
    (c) $A = 0, B = 1, C_{in} = 0$

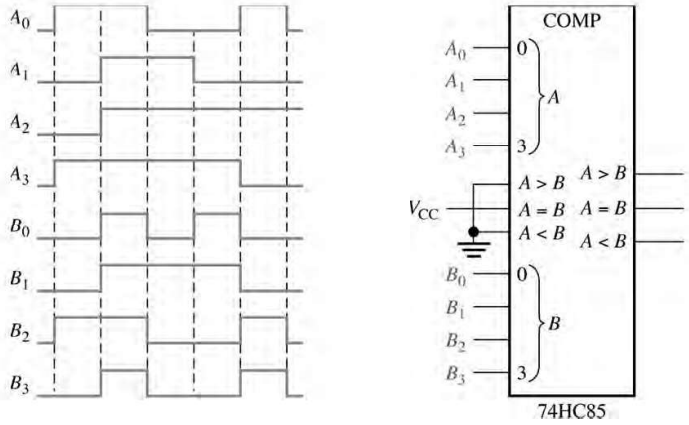
13. What the full-adder inputs that will produce each of the following outputs:
    (a) $\Sigma = 0, C_{out} = 0$
    (b) $\Sigma = 1, C_{out} = 0$
    (c) $\Sigma = 1, C_{out} = 1$
    (d) $\Sigma = 0, C_{out} = 1$

14. Determine the outputs of a full-adder for each of the following inputs:
    (a) $A = 1, B = 0, C_{in} = 0$
    (b) $A = 0, B = 0, C_{in} = 0$
    (c) $A = 0, B = 1, C_{in} = 1$
    (d) $A = 1, B = 1, C_{in} = 1$

15. For the parallel-adder, determine the complete sum by analysis of the logical operation of the circuit. Verify your result by longhand addition of the two input numbers.



16. For the 4-bit comparator, plot each output waveform for the inputs shown. The outputs are active-HIGH.



17. Show the decoding logic for each of the following codes if an active-HIGH (1) output is required:

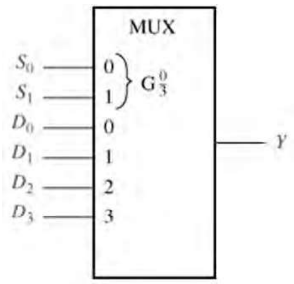
    (a) 1101
    (b) 1000
    (c) 11011
    (d) 11100
    (e) 101010
    (f) 111110
    (g) 000101
    (h) 1110110

18. For the decimal-to-BCD encoder logic, assume that the 9 input and the 3 input are both HIGH. What is the output code? Is it a valid BCD code?

19. Convert the following decimal numbers to BCD and then to binary.

    (a) 2
    (b) 8
    (c) 13
    (d) 26
    (e) 33

20. For the multiplexer given, determine the output for the following input states: $D_0 = 0$, $D_1 = 1$, $D_2 = 1$, $D_3 = 0$, $S_0 = 1$, $S_1 = 0$.



21. Draw a logic circuit for 2-to-1 multiplexer (MUX) using gates.

22. (a) Show how two 2-to-1 MUX (with no added gates) could be connected to form a 3-to-1 MUX. Input selection should be as follows:
    If $AB = 00$, select I_0
    If $AB = 00$, select I_1
    If $AB = 1$ – (B is a don't care), select I_2

    (b) Show how two 4-to-1 and one 2-to-1 MUX could be connected to form an 8-to-1 MUX with three control inputs.

    (c) Show how four 2-to-1 and one 4-to-1 MUX could be connected to form an 8-to-1 MUX with three control inputs.

23. Design a circuit which will either subtract X form Y or Y from X, depending on the value of A. If $A = 1$, the output should be X - Y, and if $A = 0$, the output should be Y – X. Use a 4 bit subtracter and two 4-bit 2-to-1 MUX.

24. Realize a full adder using 3-to-8 line decoder and

    (a) two OR gates
    (b) two NOR gates

TUTORIAL 7 : Latches and Flip-Flops

A) Objective Question

i. What ***advantage*** does a J-K flip-flop have over an S-R FF?

   a. It has fewer gates.
   b. It has only one output.
   c. It has no invalid states.
   d. It does not require a clock input.

ii. If both inputs of an S-R flip-flop are ***low***, what will happen when the clock goes high?

   a. An invalid state will exist.
   b. No change will occur in the output.
   c. The output will toggle.
   d. The output will reset.

iii. The ***asynchronous inputs*** are normally labelled _____ and _____, and are normally active _____ inputs.

   a. PRE, CLR, low
   b. ON, OFF, high
   c. START, STOP, low
   d. SET, RESET, high

iv. When ***both inputs*** of a J-K pulse-triggered FF are high, and the clock cycles, the output will

   a. be invalid.
   b. not change.
   c. remain unchanged.
   d. toggle.

v. Flip-flops are normally used for all of the following applications, ***except***

   a. counting.
   b. logic gates.
   c. frequency division.
   d. data storage.

vi. When a flip-flop is used to ***divide*** the clock frequency,

a. the J and K inputs are connected to ground.

b. the J and K inputs are connected to Vcc.

c. the reset is tied to the clock.

d. all the inputs are connected to the preset.

vii. The ***invalid state*** of an S-R latch occurs when

a. S = 1, R = 0

b. S = 0, R = 1

c. S = 1, R = 1

d. S = 0, R = 0

viii. Which of the following best describes the action of ***pulse-triggered FF's***?

a. The clock and R-S inputs must be pulse shaped.

b. The data is entered on the leading edge of the clock, and transferred out on the trailing edge of the clock.

c. A pulse on the clock transfers data from input to output.

d. The synchronous inputs must be pulsed.

ix. Like the latch, the ***flip-flop*** belongs to a category of logic circuits known as

a. Monostable multivibrators

b. Bistable multivibrators

c. Astable multivibrators

d. One-shots

B) Subjective Question

1) Answer the following questions:

a. List three types of **latches**.

b. What is the Q output of a D latch when **EN = 1 and D = 1**?

c. How does a J-K flip-flop **differ** from an S-R flip-flop in its basic operation?

2) For a **gated S-R active high latch**,

a. Determine the **Q output** for the input shown in ***Figure 1***. Show them in proper relation to enable (EN) input. Assume that Q starts LOW.

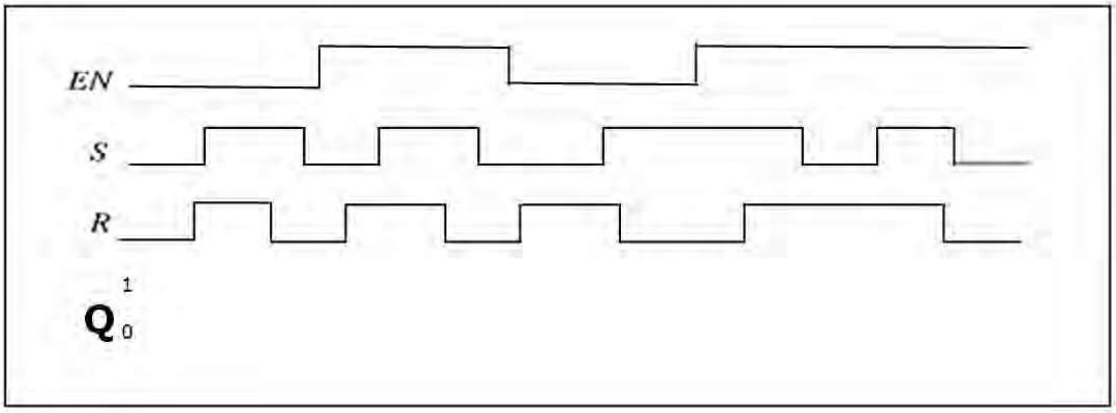


Figure 1

b) Determine the **Q waveform** relative to the clock if the signals shown in ***Figure 2*** are applied to the inputs of the J-K flip-flop. Assume that Q is initially LOW.

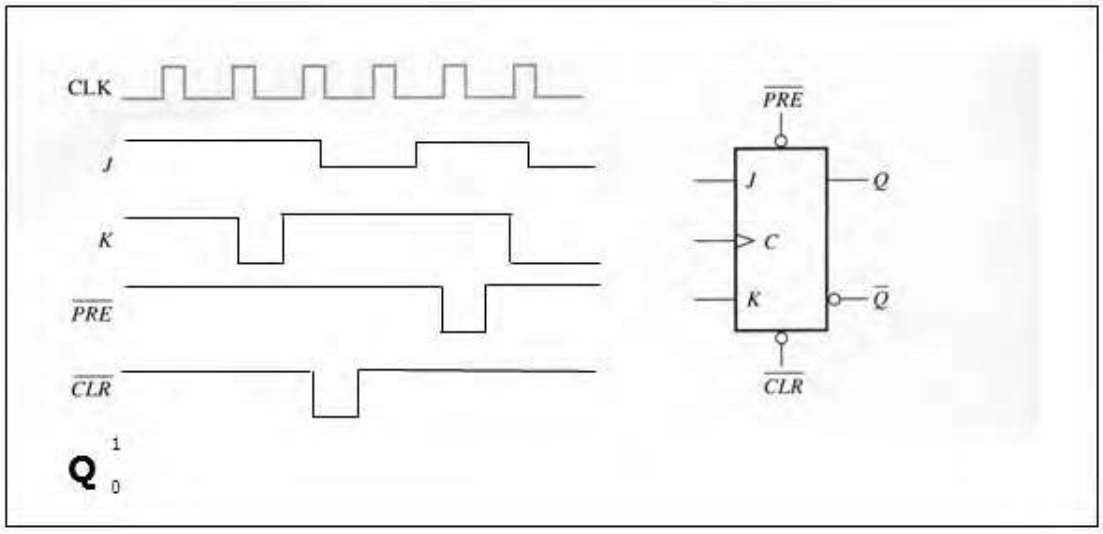


Figure 2

TUTORIAL 8: Counters

I. Answer True or False for the following statement.

1. Sequential circuits can be synchronous and asynchronous. True/ False
2. A synchronous sequential circuit changes its states at discrete instants of time. True/ False
3. Asynchronous sequential circuits can have state transitions at discrete instants of time. True/ False
4. Synchronous sequential circuits are also known as clocked sequential circuits. True/ False
5. A transition of a clock from 0 to 1 is called the falling edge. True/ False
6. The clock period is the time when the clock signal is equal to 1. True/ False
7. The memory used in synchronous sequential circuits are flip-flops. True/ False

II. Design and Analysis Problems

1. Design a 4-bit synchronous binary counter using T flip-flops by following the procedure:
   a. Create the state table.
   b. Identify the input of T flip-flops.
   c. Draw K-maps to identify the Boolean expression for the T flip-flops.
   d. Draw the circuit diagram.

2. Design the 3-bit Gray code counter based on the state diagram of Figure 1 using JK flip-flops.

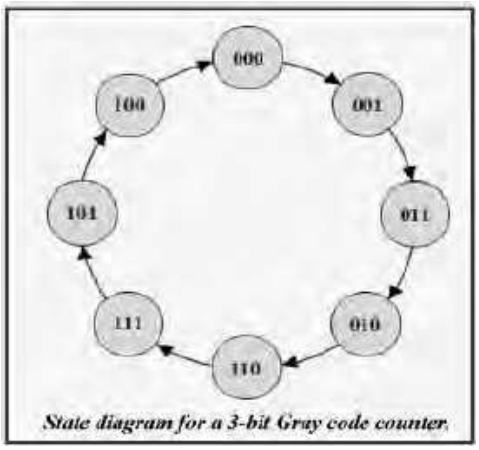


Figure 1

3. Design a 3-bit up/down counter of Gray code sequence as shown in Figure 2 using D flip-flops.

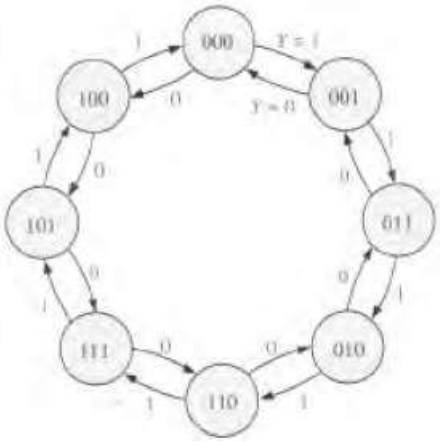


Figure 2

4. Design a synchronous counter of the sequence in Figure 3 using T flip-flop.

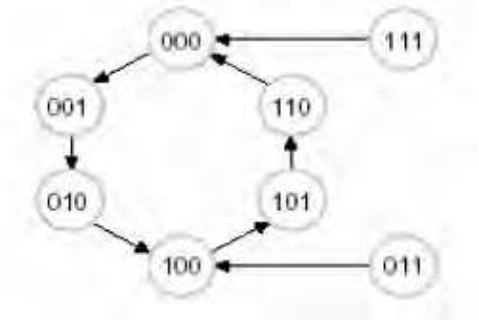


Figure 3

5. Design a 3-bit counter which counts in the sequence:

000, 011, 010, 110, 111, 101, 100, (repeat) 000, …..

a. Use D flip-flops
b. Use T flip-flops
c. Use JK flip-flops

6. An M-N flip-flop works as follows:

If MN = 00, the next state of the flip-flop is 0.

If MN = 01, the next state of the flip-flop is the same as the present state.

If MN = 10, the next state of the flip-flop is the complement of the present state.

If MN = 11, the next state of the flip-flop is 1.

a. Complete Table 1 (use don't care when possible).

Table 1: Excitation Table for MN Flip-Flop

Present State	Next State	M	N
0	0		
0	1		
1	0		
1	1		

b. Using MN flip-flops, design a counter which counts in the following sequence:

000, 001, 011, 111, 101, 100, (repeat) 000, …

7. Use JK flip-flops to design a 3-bit synchronous up/down counter that starts at 001 and cycles through Prime numbers only (i.e. numbers divisible by only themselves or 1). Assume that M=0 counts down, M=1 counts up.

8. Design a synchronous counter to count backwards from 9 down to 0 using JK flip-flops. (Procedure: determine the number of flip-flops required, sketch the state transition table, use K-maps to simplify each J,K signal, sketch the circuit).
Note: Ensure that if an unused state is encountered the counter will return to state 9 on receipt of the next clock pulse.

9. Answer True or False based on the state diagram in Figure 5.

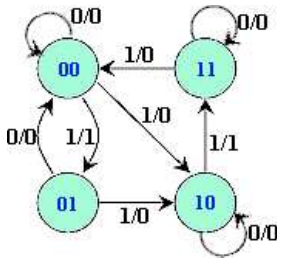


Figure 5

a. When the circuit is in state 00, the label 1/0 means that the circuit will go to the next state 10.

b. If the present state is 01, and the input is 0, the next state would be 10.

c. If the circuit is presently in state 11, it will remain in its present state 11 if the input is 0 and the output is 0.

10. Consider a sequential circuit shown in Figure 4. It has one input *X*, one output *Z* and two state variables Q1Q2 (thus having four possible present states 00, 01, 10, 11). Based on the circuit, derive:

    a. the Boolean expression for D1, D2 and *Z*.

    b. the state table and FF transition table.

    c. the state diagram.

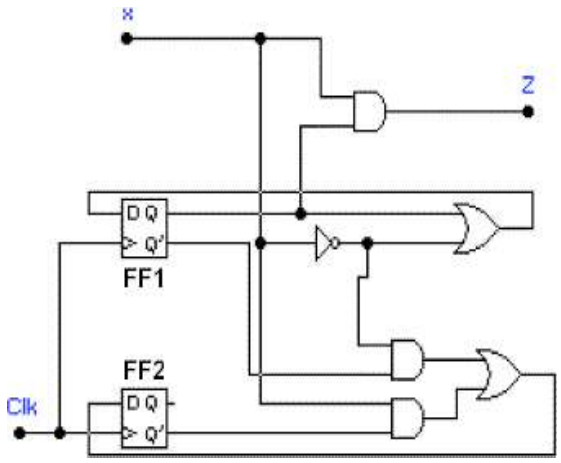


Figure 4

11. Derive the next state, the output table and the state diagram for the sequential circuit shown in

    a. Figure 5 b. Figure 6

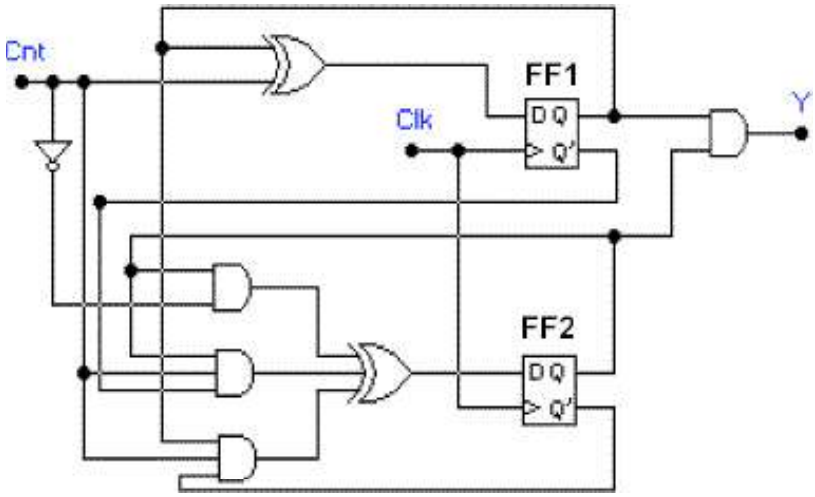


Figure 5

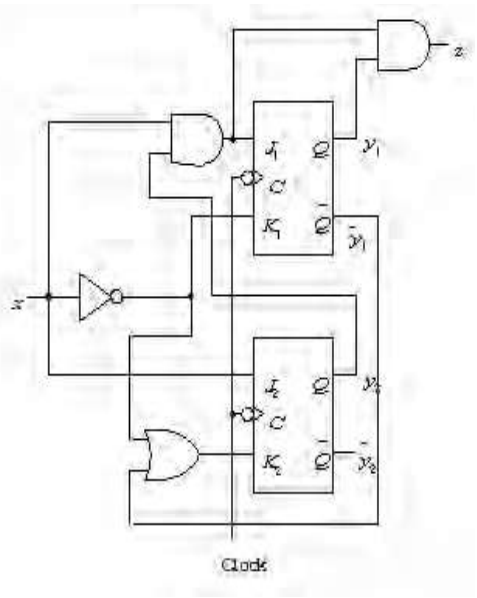


Figure 6

TUTORIAL 9: Shift Registers

1. a) What are the two properties of a shift register?
   b) For a 5-bit SISO with a clock of 1MHz, how long does it takes to transfer a data entered at the input to the output?

2. Referring to IC 74HC164, answer the following questions
   a) Input A and B of the IC held HIGH and its Q_7 output is connected to the pin $\overline{CLK}$ via an inverter. Determine the output sequence of the IC for every clock cycle.
   b) An 8-bit digital word is applied to a 74HC164 8-bit SIPO shift register. The word is to be applied to three different circuits after a time delays of 3μs, 6μs and 8μs. Show the connection to the IC to satisfy the requirement.

3. Initially an 8-bit SISO shift register is loaded with the data word 11101001. The data word 156_{10} is then entered serially from right to left. After 7 clock pulses the circuit is disabled. Write down a table that shows the bits stored after 7 clock pulses.

4. An 8-bit binary counter, a 6-bit ring counter and a 10-bit Johnson counter are connected in cascade. A clock frequency of 10MHz is applied to the input of the first counter. Calculate the frequency of the output waveform.

5. a) Describe the operation of a shift register in Figure 1.

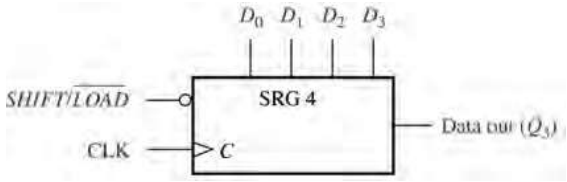


Figure 1

   b) If a nibble data 1101 is to be loaded and shifted by the circuit,
      i) Determine the logic value at the inputs.
      ii) Draw a timing diagram to show the operation of the shift register.

6. a) Which shift-register counter requires the most flip-flops for a given MOD number?
   b) Which shift-register counter requires the most decoding circuitry?

7. a) Design a 3-bit ring counter using D flip-flop.
   b) How to set the most significant output of the 3-bit ring counter that you design?
   c) By using table, show the output of the ring counter for 6 clock cycles.
   d) Draw the state diagram of the designed ring counter and determine its MOD.

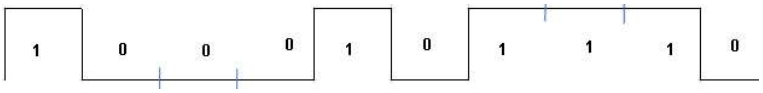
8. Redo all Questions 7 but change the circuit to 5-bits Johnson counter.

ANSWERS TO SELECTED QUESTIONS

Tutorial 1

1. i) Analog ii) AND gate iii) clock iv) digital v) pulse vi) risetime
2. 50%
3. i) 7 segment driver ii) memory
4. AND or NOR or XNOR gate
5. i) Adder ii) Multiplier iii) Multiplexer
6. 1000
7. Frequency = 6.67 KHz, duty cycle = 16.7 %
8. i) a) programmable
   b) ease of storage
   c) ease of fabrication on IC
   ii) Analog to Digital Converter (ADC), hybrid
   iii) bit
   iv) 1) Analog 2) Digital 3) Digital 4) Analog

9. i) Cannot be determine because it is a non periodic (aperiodic) signal



ii)

iii) 1µs

10. A squarewave has a high and low for each cycle and it is a periodic signal. Therefore the

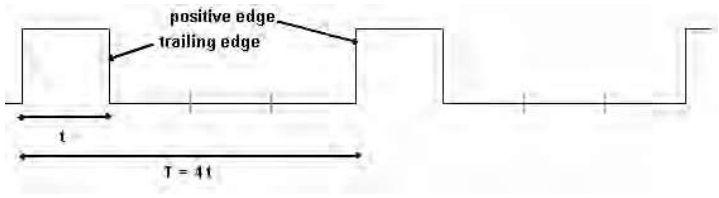
$Period, T = \frac{1}{f} = \frac{1}{1Mhz} = \frac{1}{10^6} = 1\mu s$

Within a cycle there are 2 signal change low to high and high to low.

For 1 second, $no\ of\ cycles = \frac{1}{1\mu s} = 1 \times 10^6$

Therefore no of signal change = 2 x (1×10^6) = 2 million times.

11.



12. i) Multiplexer
    ii) Encoder
    iii) Counter
    iv) comparator
    v) DeMultiplexer
    vi) Memory
13. For fix function IC the function of the IC cannot be changed while for Programmable IC ,its function can be change by reprogramming the IC
14. a. NOT
    b. OR , AND
    c. AND

Tutorial 2

1b. 149 1d. 2313

2a. 1001101 2c. 11001101 2e. 110010010000

4a. 10100011001.0110 4c. 100101101.0001 4e. 1111101000.0000

5b. 8192 5c. 43981

6a. 3B 6c. 909 6e. 397

7b. 311 7d. 1249

8b. 2000 8d. 200000

10a. 16, 95, 6B, 909, 12C

11a. 5D4.A, 2724.2

12c. 0010 000 0101 12e. 0011 0010 0001 0110

13b. 555

14b. Invalid 14c. Valid

17c. -64 to + 63

18b. **0**111 1111, **0**111 1111, **0**111 1111

18d. Out of range for sign & magnitude representation, out of range for 1's complement, -128 for 2's complement

Tutorial 3

1. FALSE
2. TRUE
3. TRUE
4. TRUE
5. AND
6. NOR
7. (a) XOR Symbol and its labels

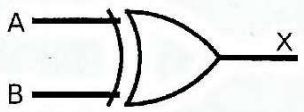
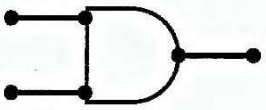


Figure 1: XOR Symbol and its labels

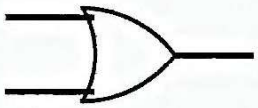
(b) Figure 1 truth table.

A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

8. $P = \overline{A\overline{C} + \overline{D}} \times B, \quad Q = \overline{\overline{B} + \overline{E} \times \overline{D}}$
9. F = 010100001
10. (a) AND Gate

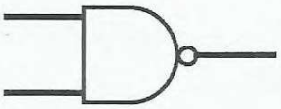


(b) OR Gate

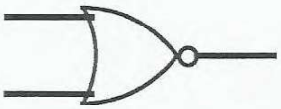


(c) NOT Gate

(d) NAND Gate



(e) NOR Gate



11. All inputs are 1 (HIGH).

12. At least one input is 1 (HIGH)

13.

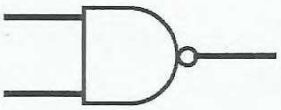
GATE	INPUT A	INPUT B	INPUT C	OUTPUT
AND	1	0	1	0
OR	0	1	0	1
AND	1	1	1	1
OR	0	0	0	0
NOR	1	1	1	0
AND	1	0	0	0

14. (a) XNOR, X = 10100010
    (b) XOR, X = 01011101
    (c) NAND, X = 01111111

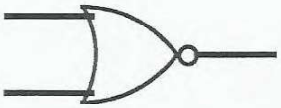
15. (a) Hex Inverter
    (b) Triple 3-input NAND
    (c) Quad 2-input NAND

16. (a) $T = X.Y.Z$
    (b) $T = X + Y + Z$
    (c) $W = \overline{\overline{X}} = X$

(d) NAND Gate



(e) NOR Gate



11. All inputs are 1 (HIGH).

12. At least one input is 1 (HIGH)

13.

GATE	INPUT A	INPUT B	INPUT C	OUTPUT
AND	1	0	1	0
OR	0	1	0	1
AND	1	1	1	1
OR	0	0	0	0
NOR	1	1	1	0
AND	1	0	0	0

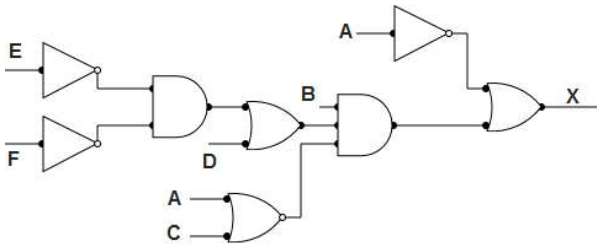
14. (a) XNOR, X = 10100010
    (b) XOR, X = 01011101
    (c) NAND, X = 01111111

15. (a) Hex Inverter
    (b) Triple 3-input NAND
    (c) Quad 2-input NAND

16. (a) $T = X.Y.Z$
    (b) $T = X + Y + Z$
    (c) $W = \overline{\overline{X}} = X$

Tutorial 4

1 .



2. i)$Y = \bar{A}B\bar{C} + C + \bar{D} + E$

ii) $Y = \bar{P}Q + R + SP$

3. $Y = A + B$

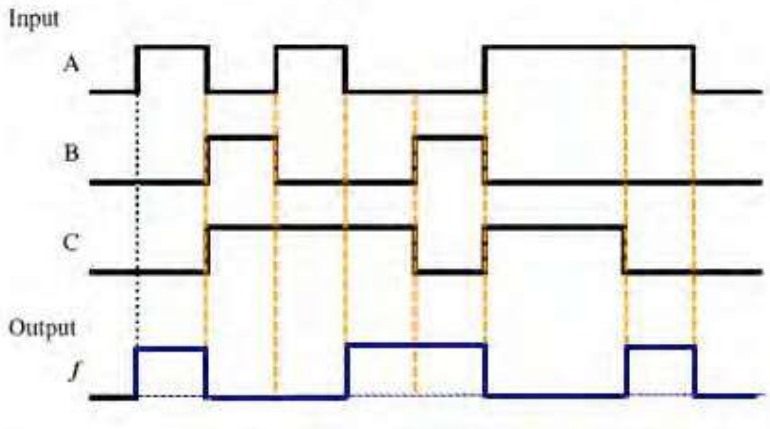
4. $f = (A + B + C)(A + B + \bar{C})(A + \bar{B} + C)(A + \bar{B} + \bar{C})$

5. $f = \bar{A}BC + ACD$

6. i) $f = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$

ii) $f = (A + B + C)(A + \bar{B} + \bar{C})(\bar{A} + B + \bar{C})(\bar{A} + \bar{B} + C)$

iii)



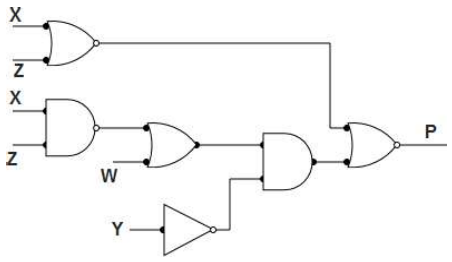
7. i) $Y = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$

ii) $Y = (A + B + C)(A + \bar{B} + \bar{C})(\bar{A} + B + \bar{C})(\bar{A} + \bar{B} + C)$

8.

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

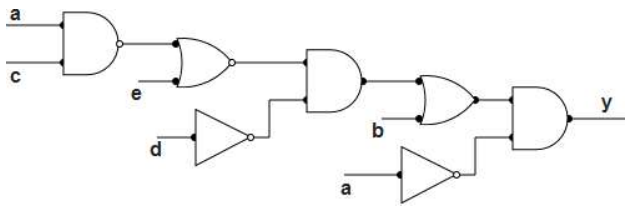
9.



10.i) $Y = \bar{R}\bar{S} + \bar{P}\bar{Q}\bar{R} + \bar{Q}\bar{S}$

ii) $G = \bar{W}\bar{X} + WXY$

11.



12 $F_{(p,q,r)} = pq + p\bar{r} + \bar{p}r$

Tutorial 8

2.

Present State			Next State			JK Transition Table					
Q2	Q1	Q0	$Q2_+$	$Q1_+$	$Q0_+$	J2	K2	J1	K1	J0	K0
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	1	0	X	1	X	X	1
0	1	0	1	1	0	1	X	X	0	1	X
0	1	1	0	1	0	0	X	X	1	X	1
1	0	0	0	0	0	X	1	0	X	0	X
1	0	1	1	0	0	X	0	0	X	X	1
1	1	0	1	1	1	X	0	X	0	1	X
1	1	1	1	0	1	X	0	X	1	X	0

Q2 \ Q1Q0	00	01	11	10
0	0	0	0	1
1	X	X	X	X

$J2=Q1\overline{Q0}$

Q2 \ Q1Q0	00	01	11	10
0	X	X	X	X
1	1	0	0	0

$K2=\overline{Q1}\ \overline{Q0}$

Q2 \ Q1Q0	00	01	11	10
0	0	1	X	X
1	0	0	X	X

$J1=\overline{Q2}Q0$

Q1Q0 / Q2	00	01	11	10
0	X	X	1	0
1	X	X	1	0

K1= Q0

Q1Q0 / Q2	00	01	11	10
0	1	X	X	1
1	0	X	X	1

J0=Q1

Q1Q0 / Q2	00	01	11	10
0	X	1	1	X
1	X	X	0	X

3.

Present State				Next State			D FF Transition		
I	**Q2**	**Q1**	**Q0**	**$Q2_+$**	**$Q1_+$**	**$Q0_+$**	**D2**	**D1**	**D0**
0	0	0	0	1	0	0	1	0	0
0	0	0	1	0	0	0	0	0	0
0	0	1	0	0	1	1	0	1	1
0	0	1	1	0	0	1	0	0	1
0	1	0	0	1	0	1	1	0	1
0	1	0	1	1	1	1	1	1	1
0	1	1	0	0	1	0	0	1	0
0	1	1	1	1	1	0	1	1	0
1	0	0	0	0	0	1	0	0	1
1	0	0	1	0	1	1	0	1	1
1	0	1	0	1	1	0	1	1	0
1	0	1	1	0	1	0	0	1	0
1	1	0	0	0	0	0	0	0	0
1	1	0	1	1	0	0	1	0	0
1	1	1	0	1	1	1	1	1	1
1	1	1	1	1	0	1	1	0	1