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Design of high performance multimedia control system for UAV/UGV based on SoC/FPGA Core.

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Abstract

The article deals about design of low cost/small size, high performance multimedia (audio, video) control system intended for usability in mobile AGV or flying UAV. There are presented two multimedia control systems, first one based on SoC device with open source operating system (OpenWrt) for not response critical operation (OS start after reset within 30 seconds, it is suitable for ground mobile or underwater devices). The second design is FPGA based without OS only with firmware for camera critical operation (start after reset within 1 second, it is suitable for aerial devices).

Keywords: Control System, FPGA, SoC, Unnamed Vehicles

Nomenclature

FPGA	Field-programmable gate array
SoC	System on a chip
UAV	Unmanned aerial vehicle
UGV	Unmanned ground vehicle

1. Introduction to control system

The article introduces design two control systems for mobile and aerial vehicles aimed for video/audio processing especially. This research introduces only basic framework solution for universal implementation to real devices. Practical implementation of similar project solutions can be found in these articles [1] and [2]. The standard control system based on 8bit MCU doesn't have enough resources to process audio/video stream together with motor control. We can handle this data bandwidth by separate DSP, SoC or CPU unit. The FPGA solution can substitute SoC by Soft CPU and 8bit MCU by extended IP blocks (timers, GPIO). In our design we use System on a chip (SoC) for mobile device control system and FPGA for aerial device control system. DSP cores are aimed to fast signal and math operation processing, video/sound processing is primarily not supported. Standard CPU cores contains only math unit and price is comparable to SoC cores,

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which includes many other peripherals in one silicon wafer. Basic description the main features of FPGA and SoC are introduced in next two subchapters.

1.1. System on a Chip

System on a chip (SoC) technology is the packaging of all the necessary electronic circuits and parts for a "system" on a single integrated circuit (IC), generally known as a microchip. For example, a system-on-a-chip for a sound-detecting device might include an audio receiver, an analog-to-digital converter (ADC), a microprocessor, necessary memory, and the input/output logic control for a user - all on a single microchip. System-on-a-chip technology is used in small, increasingly complex consumer electronic devices. Some such devices have more processing power and memory than a typical 10-year-old desktop computer. SoC equipped robots might act as programmable monitoring and inspection devices with remote video/audio functions. SoC video devices might help blind people, allowing them to see; SoC audio devices might allow deaf people to hear. Handheld computers with small whip antennas might someday be capable of browsing the Internet at megabit-per-second speeds from any point on the surface of the earth. SoC is evolving along with other technologies such as silicon-on-insulator (SOI), which can provide increased clock speed s while reducing the power consumed by a microchip [3].

1.2. Field-programmable gate array

A field-programmable gate array (FPGA) is an integrated circuit (IC) that can be programmed in the field after manufacture. FPGAs are similar in principle to, but have vastly wider potential application than, programmable read-only memory (PROM) chips. FPGAs are used by engineers in the design of specialized ICs that can later be produced hard-wired in large quantities for distribution to computer manufacturers and end users. Ultimately, FPGAs might allow computer users to tailor microprocessors to meet their own individual needs [4], [5].

2. Operating system vs Firmware for control system

On the market there are many specialized operating systems for embedded systems. The most widely used commercial embedded operating systems are Windows CE, Symbian, IOS. The commercial systems are usually provided without open source code or partially closed. The main problem of closed source code is driver support in hardware equipment. That is main reason to selecting open source code OS (GPL or BSD license). In the area of open source code OS we have many possibilities, for example well known mobile phone OS Android. The next selection can be Open embedded, OpenWrt, DD-WRT, Web OS. We are analyzed or tested some OS with these results. The Android and Windows CE are memory hungry systems, that's main disadvantage of implementation to embedded small control system. The Open embedded and DD-WRT are hard configurable OS only by command line source changing. The most usable open source operating system for embedded application was OpenWrt, which is primarily used in Wi-Fi routers hardware.

2.1. OpenWrt

OpenWrt is described as a Linux distribution for embedded devices. Instead of trying to create a single, static firmware, OpenWrt provides a fully writable file system with package management. This frees you from the application selection and configuration provided by the vendor and allows you to customize the device through the use of packages to suit any application. For developer, OpenWrt is the framework to build an application without having to build a complete firmware around it; for users this means the ability for full customization, to use the device in ways never envisioned [6].

The main advantages are small footprint (min. 4MB), low memory requirements (min. 16MB) and very easy reconfigurable menuconfig comparable with Linux kernel config. The repository contains currently about 2000 packages.

2.2. FPGA firmware/Real-time OS

Special branch of operating system are real-time systems for time critical control algorithms. Real-time systems are computer (control) systems that monitor, respond to, or control an external environment. This environment is connected to the computer (control) system through sensors, actuators, and other input-output interfaces. The real-time system must meet various timing and other constraints that are imposed on it by the real-time behavior of the external word. Real-Time systems can be classified by different perspectives. The first two classifications are hard real-time, soft real-time and firm real-time or fail-safe versus fail-operational, depending on the characteristics of the application. Hard real time must finish

the task within the restrict time; missing a deadline is a total system failure. Soft real time can finish the task "on time" or exceed the deadline time for a few amount of time. Special emphasis is placed on hard and soft real-time systems. A missed deadline in hard real-time systems is catastrophic and in soft real-time systems it can lead to a significant loss. Firm real-time tolerable infrequent deadline misses. Real-time embedded systems processing core can be a microcontroller, digital signal processors, microprocessor or FPGA [7].

In the second control system for aerial devices is the main condition fast restart. The real-time response is not so important. The real-time OS doesn't provide real-time restart, which was main reason for selection of FPGA system without OS. The main program loop is executed in low level direct in soft CPU, low level commands handle all device drivers too (camera, Wi-Fi). This method ensure fast restart lower than 1 second, which will be secure for aerial vehicle control.

3. Realization

Figure 1 shows principle scheme of both control systems SoC and FPGA based system. Both systems contains Wi-Fi communication interface for remote software application. Remote control program can handle both boards without modification.

System on a chip solution is based on commercially available parts: Arduino compatible JY-MCU board and modified access point board TP Link WR703N. FPGA system is new design of board which includes function from SoC and MCU to one IC as Soft Core CPU.

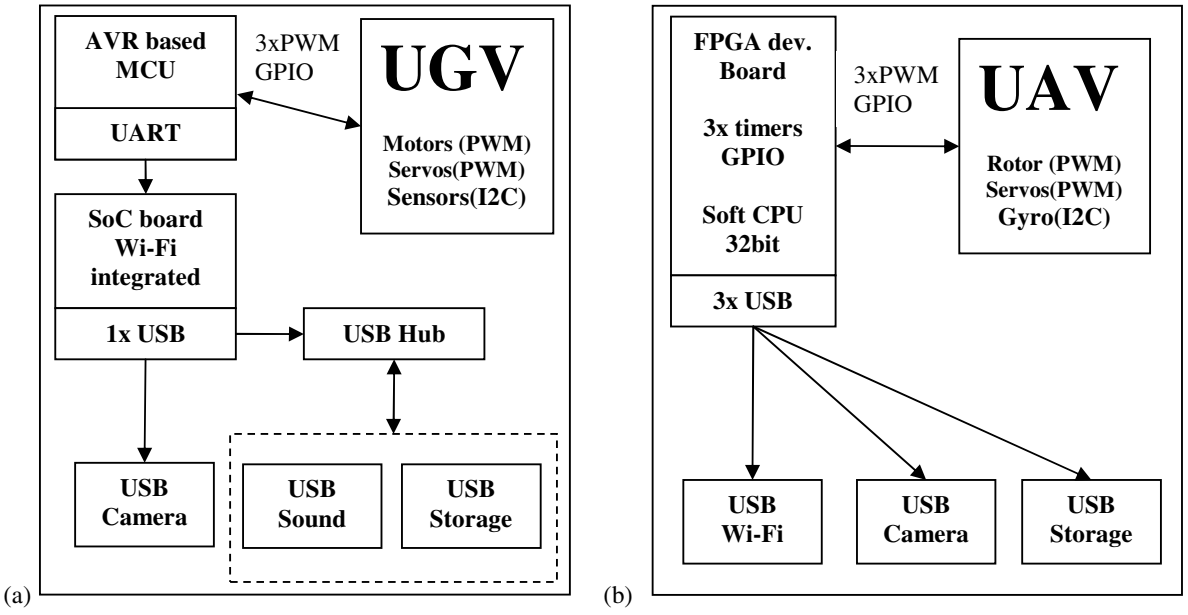

Fig. 1. Principle scheme of control systems (a) SoC for UGV (b) FPGA for UAV

3.1. Hardware

SoC control system contains 32 bit CPU board with external SDRAM and 8 bit MCU which communicates by UART interface. Older development of SoC control system was created by custom board with AT91SAM9260 (200Mhz) from Atmel and later upgraded to MX233 (454Mhz) from Freescale with same arm9 core ARM926EJ-S inspired by invariant control system [8]. Current replacement by TP Link router board was due to 2x lower cost, smaller dimension and integrated Wi-Fi communication. In comparison to Raspberry PI (credit card size), selected router board is 2x smaller and it has better support in OpenWrt. Basic parameters of selected hardware boards are:

SoC board description:

- Atheros AR9331 Chipset (400Mhz BogoMIPS : 265.42, MIPS architectute / Chip integrated wireless).
- Wifi 802.11 b/g/n 150Mbps.
- maximum current draw at 5V is 185mA, wireless power output 20dBm/100mW, average power consumption is 0.5W.

- 4 MB flash memory, 32 MB RAM (DDR SDRAM).
- 1xUSB 2.0 port, 1xUART, 1xEthernet Port

MCU board:

- Atmel 8bit AVR atmega32L (16Mhz)
- 1xUART
- GPIO
- 3xTimer used as PWM for motor control

FPGA control system contains 32 bit Soft CPU extended by timers, GPIO and soft terminal. The second MCU board for low level signal isn't necessary because there is any OS. The firmware can handle motor signal almost near to real-time.

Basic parameters of FPGA system are:

- Altera Cyclone 3
- Soft Core CPU (TSK 3000 50Mhz)
- SRAM 1Mbit
- Serial Flash (FPGA config + bootloader)
- 3x USB (Camera, Wi-Fi, Flash Storage)

Figure 2 (a) shows System on a chip solution unboxed, (b) shows FPGA development board Nanoboard 3000AL (altera cyclone 3 EP3C40F780C6 based) for debugging Soft CPU firmware application, (c) shows optimized design of FPGA board with minimal dimension. The custom board contains reduced FPGA (EP3C5E144C8) to 5K Gates instead of 40K which markedly reduce cost and dimension.

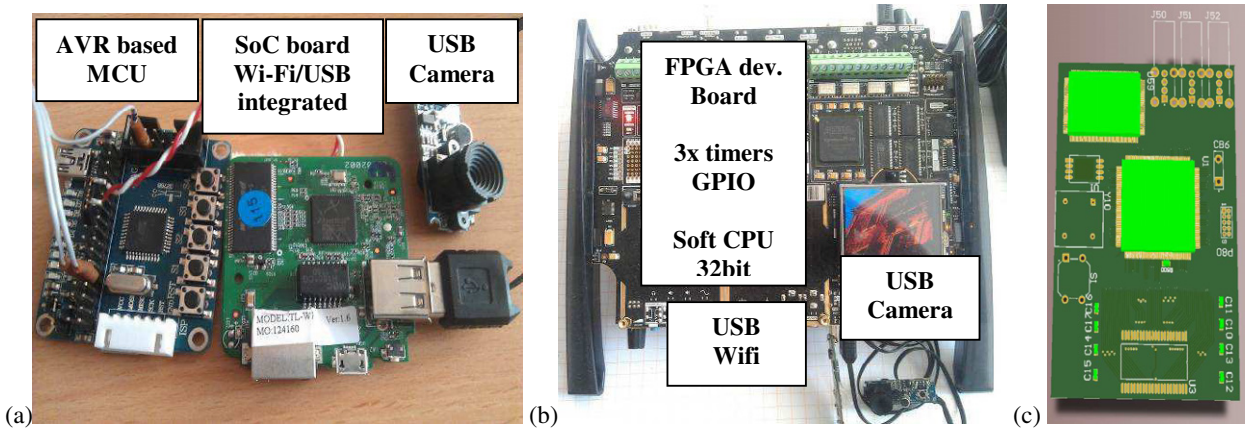

Fig. 2. Illustration of control system based on (a) System on a Chip with AVR MCU (b) FPGA development board (b) FPGA prototype

The main parameters of the design were dimension, weight and price. For Aerial control system was next important requirement very fast restart after some unpredictable fail state and real-time runtime.

Currently we can get weight lower to 40g for both SoC and FPGA system without battery (MCU, SoC/FPGA, USB camera).

3.2. Software of SoC and FPGA

The operating system for SoC board is modified OpenWrt OS, which is primarily aimed to wireless router. Kernel is Linux based version 3.3.8. OS footprint is reduced only to necessary drivers for USB video, audio, storage and wireless drivers. The size of the footprint is 4MB. Basic function of SoC board is video streaming and transfer control data from remote system to MCU board.

The video from USB camera uses video for Linux (v4l2) framework, universal video driver (uvc) and is coded to motion jpeg format. The remote control system can acquires video frames by mjpg-streamer software from installed web server. We are tested Gstreamer application which provides video/audio application too. Mjpg-streamer was selected because of it's provides lower CPU load. Gstreamer application is used only for audio streaming by ulaw G.711 codec.

If we use USB hub, the OS can be moved to external storage and this provide additional storage for web server (uhttpd), PHP web scripting language and Python programming language.

FPGA software using virtual 32bit Soft CPU (Tasking TSK_3000A). Main control loop handles low level drivers of all peripherals (USB video, USB Wi-Fi). USB web camera is limited to UVC driver. The Wi-Fi support is limited to BSD drivers run, run used for some Ralink models. Figure 3. (a) shows soft design of FPGA software by Open Bus library compatible with Wishbone components. Figure 3. (b) shows driver stack for selected components.

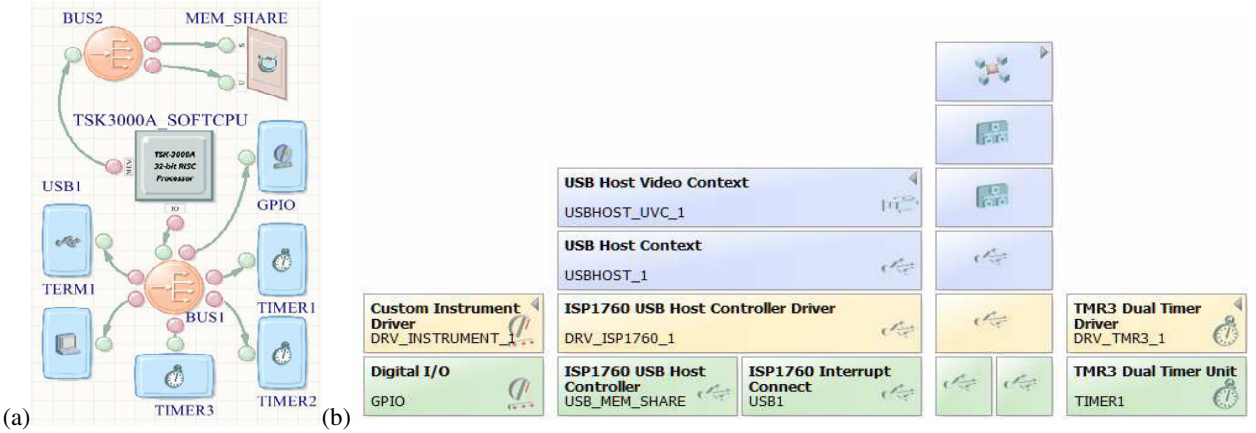

Fig. 3. Illustration of FPGA software design for (a) system by Open Bus library (b) used drivers stack.

Configuration and debugging of both systems are realized by terminal console in SoC (putty SSH access) and in FPGA solution by soft terminal.

The remote control system is universal for both systems (FPGA, SoC) and is written in C# language. All control libraries are ported to web control application ASPX and windows mobile framework. Figure 4. shows desktop remote application for simulation of UGV environment like used in [9], (b) video processing and (c) sound configuration interface.

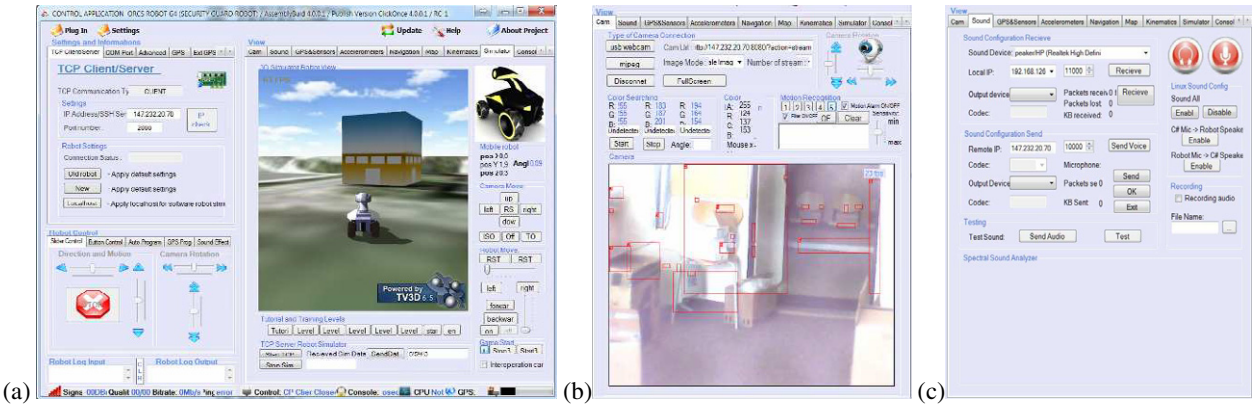

Fig. 4. (a) C# Remote software with AGV simulator (b) Video processing (c) Sound/Mic interface

3.3. *Implementation and Results*

Table 1. shows main differences between FPGA without OS and SoC solution with open source operating system (OpenWrt). The main disadvantage of FPGA solution is limited support of USB devices.

Figure 5. shows testing platforms for control system (a) UGV mobile platform without wheels for testing SoC system, (b) development system with FPGA for propeller thrust testing.

SoC control system will control main DC motor, one servo for turning left, right and one small servo for camera rotation. The FPGA system currently control only propeller for testing thrust. Next two servos are reserved for flight control according gyro data.

Table 1. Comparison of control system solution SoC/FPGA

Solution Description/dimension	Start after reset [s]	Weight [g]	CPU speed	Sound support	Wifi support	Video support	Price [EUR]
SoC solution [48x50mm]	30 s	14g + 13g	400 Mhz	any Linux driver	integrated	any Linux driver	20
MCU board [52x44mm]			16 Mhz				10
FPGA solution [50x70] Soft CPU 32bit SoC and low level timer, GPIO.	< 1 s	24g	50 Mhz	-	only Ralink BSD driver run, rum	only UVC driver	estimated 50

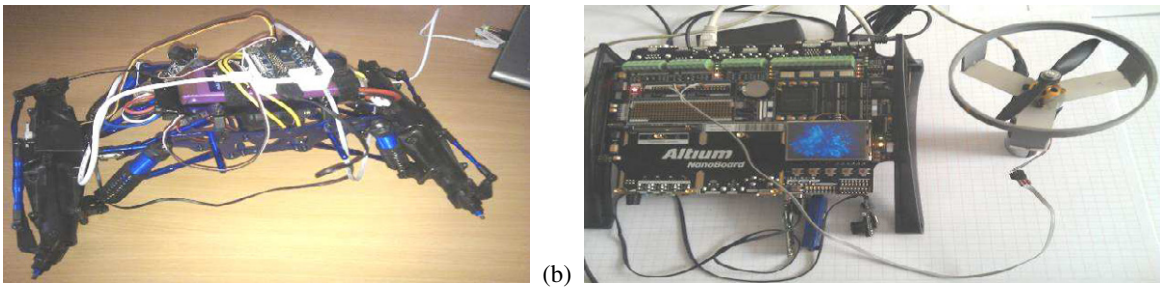

Fig. 5. Illustration of testing platform for (a) UGV SoC based control system (b) UAV FPGA based control system.

4. Conclusion

In the article were introduced two advanced multimedia control systems for UGV and UAV devices first based on SoC and second on FPGA core. The SoC solution provides higher performance and better compatibility with USB equipment. The main disadvantage is requirements of external MCU for signal processing (motor control /sensor data acquisition) and relatively long restart after fail state, which is caused by Linux core loaded to SDRAM memory after every restart. FPGA solution provides solution in one compact board. The system works without OS, all routines is executed in low level includes all device drivers. The main disadvantage is limited compatibility with USB devices (only UVC cameras, only BSD Wi-Fi Ralink devices). The next works in the project will be aimed to reliability testing of SoC based control system with mobile carriage and FPGA solution with aerial device according [11]. The next step of development is replacement of Wi-Fi technology by low size 3g USB modem to remove communication range problems.

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