

Analog IC Design – Cadence and Master Micro Tools

Lab 07

gm/ID Design Methodology

Intended Learning Objectives

In this lab you will:

- Design and simulate a 5T OTA.
- Learn how to plot and use the gm/ID design charts.
- Learn how to simulate the open-loop characteristics of the 5T OTA.
- Learn how to simulate the closed-loop characteristics of the 5T OTA.

NOTE: To get access to the Sizing Assistant (SA) please register at <https://adt.master-micro.com/> and create a support ticket from your dashboard. Verified instructors may also request access to an editable MS Word version of the labs and the model answers.

NOTE: The values and charts used in the lab document assume the provided 180 nm educational device models and 1.8 V supply. Other models/technologies can be used by applying reasonable adjustments to the lab values.

Part 1: gm/ID Design Charts

Download ADT:

- Go to <https://adt.master-micro.com>
- Register using your university or corporate email address. If you are a student or fresh grad, select academia as your organization type. If you don't have a university or corporate email address then register as unemployed and include your LinkedIn profile URL, but your account may take some time to get reviewed and approved.
- Read ADT readme file. Visit ADT website again and generate a free personal license.
- Use the spectre example LUTs included in ADT. Do NOT generate new LUTs.

Using ADT Device Xplore, plot the following design charts vs gm/ID for both PMOS and NMOS. Set $V_{DS} = V_{DD}/3$ and $L = 0.18\mu, 0.5\mu:0.5\mu:2\mu$

- 1) gm/gds
- 2) ID/W
- 3) gm/Cgg (use advanced Y expression)
- 4) VGS

Part 2: OTA Design

Use the gm/ID methodology to design a diff input single-ended (SE) output operational transconductance amplifier (OTA) that achieves the following specs. Use an ideal external 10uA DC current source in your test bench (not included in the OTA current consumption spec), but design your own current mirror.

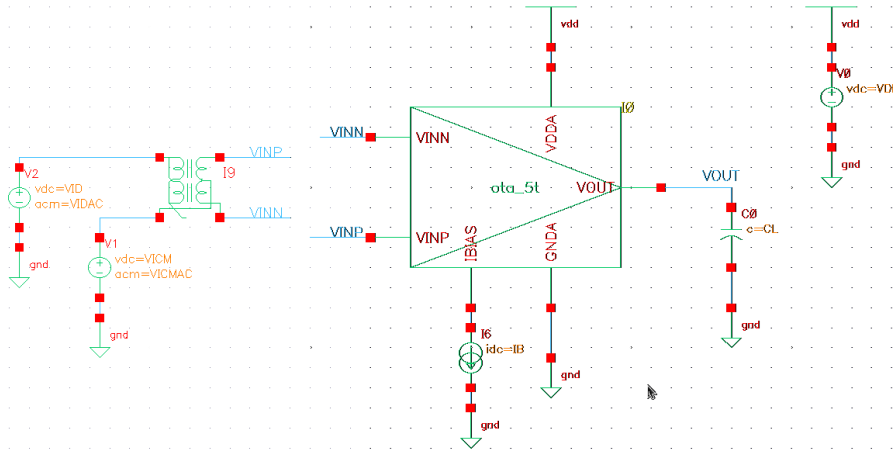
Technology	0.18um CMOS
Supply voltage	1.8V
Load	5pF
Open loop DC voltage gain	>= 34dB
CMRR @ DC	>= 74dB
Phase margin	>= 70°
OTA current consumption	<= 20uA
CM input range – low	<= 0.8V
CM input range – high	>= 1.5V
GBW	>= 5MHz

Commented [H01]: CMRR is gm/gds higher than Avdc. CMRR = Avdc + 40dB means gm/gds = 100 which is quite reasonable.

Report the following:

- 1) Detailed design procedure and hand analysis. You need to explain why you chose the architecture that you implemented.
- 2) Use the Sizing Assistant (SA) or the design charts in ADT to size the transistors.
- 3) A table showing W , L , g_m , I_D , g_m/I_D , V_{DSsat} , $V_{ov} = V_{GS} - V_{TH}$, and $V^* = 2I_D/g_m$ of all transistors (as calculated from gm/ID curves).

Part 3: Open-Loop OTA Simulation¹



Create a testbench for the OTA as shown above. Note that IDC connection (sinking or sourcing) in the test bench may be different from the one shown above depending on the type of your input pair

(PMOS/NMOS). Report the following:

1) Schematic of the OTA with DC node voltages clearly annotated.

- Use VICM at the middle of the CMIR.
- Is the current (and gm) in the input pair exactly equal?
- What is DC voltage at VOUT? Why?

2) Diff small signal ccs:

- Use AC analysis (1Hz:10GHz, logarithmic, 10 points/decade).
- Set VIDAC = 1 and VICMAC = 0.
- Use VICM at the middle of the CMIR.

→ Cadence Hint: Use Cadence calculator expressions to calculate circuit parameters (Ao, Ao in dB, BW, GBW, UGF). You may use Cadence calculator to create other useful expressions.

Name	Type	Expression/Signal/File
Ao	expr	y _{max} (mag(VF("/VOUT")))
Ao_dB	expr	dB20(y _{max} (mag(VF("/VOUT"))))
BW	expr	bandwidth(VF("/VOUT") 3 "low")
fu	expr	unityGainFreq(VF("/VOUT"))
GBW	expr	(Ao * BW)

- Plot diff gain (in dB) vs frequency.
- Compare simulation results with hand calculations in a table.

¹ An OTA can be simulated without closing the loop if it is perfectly matched (zero offset voltage). For this ST OTA in open loop, the output node DC level will follow the diode connected node. For two-stage OTA, the systematic offset voltage may drive the output to one of the rails. Also, when simulating mismatch (Monte Carlo simulation), open-loop simulation cannot be used. You must close the loop in the cases of random and systematic offset, so that the offset voltage is automatically adjusted by the feedback action and the dc bias is correctly set.

3) CM small signal ccs:

- Use AC analysis (1Hz:10GHz, logarithmic, 10 points/decade).
- Set VICMAC = 1 and VIDAC = 0.
- Use VICM at the middle of the CMIR.
- Plot CM gain in dB vs frequency.
- Compare simulation results with hand calculations in a table.
- (Optional) Avcm vs VICM:
 - Use **parametric sweep (not DC sweep)** for VICM = CMIR-low:10m:CMIR-high.
 - Plot CM gain at 1Hz in dB vs VICM.
 - ➔ Cadence Hint: Instead of using parametric sweep, a better alternative in Cadence is to use AC sweep but sweep a design variable (VICM) instead of sweeping the frequency. The frequency is set at 1 Hz (or any other small value) to get the low frequency gain (DC gain).
 - Justify the results.

4) CMRR:

- ➔ Cadence Hint: In some simulators, you have to get Avd and Avcm from two independent simulation runs (we cannot run both simultaneously because we have single ended output, thus we cannot differentiate between diff and CM signals at the output). But for Cadence spectre you should use XF analysis (1Hz:10GHz, logarithmic, 10 points/decade) because you need to calculate the transfer function between multiple inputs and a single output.
- ➔ Cadence Hint: Access XF analysis results from the results browser or from ADE results tab (Right Click -> Direct Plot -> Main Form). You may use this expression in the calculator to plot the CMRR: $\text{dB20}(\text{mag}(\text{getData}("/V2" ?result "xf"))) - \text{dB20}(\text{mag}(\text{getData}("/V1" ?result "xf"))) .$
- Use VICM at the middle of the CMIR.
- Plot CMRR in dB vs frequency at VICM at the middle of the CMIR.
- Compare simulation results with hand calculations in a table.
- (Optional) CMRR vs VICM:
 - Use **parametric sweep (not DC sweep)** for VICM = CMIR-low:10m:CMIR-high.
 - Plot CMRR at 1Hz in dB vs VICM.
 - ➔ Cadence Hint: Instead of using parametric sweep, a better alternative in Cadence is to use AC sweep but sweep a design variable (VICM) instead of sweeping the frequency. The frequency is set at 1 Hz (or any other small value) to get the low frequency gain (DC gain).
 - Justify the results.

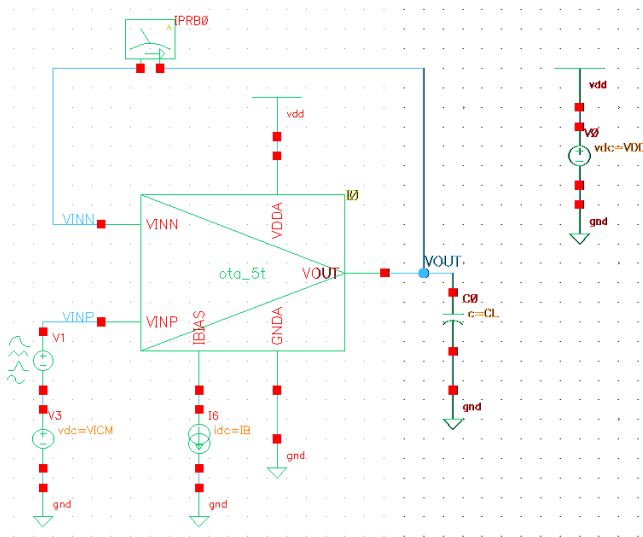
5) Diff large signal ccs:

- Use VICM at the middle of the CMIR.
- Use DC sweep (**not parametric sweep**) VID = -VDD:1m:VDD. You must use a small step (1mV) because the gain region is very small (steep slope).
- Plot VOUT vs VID.

- From the plot, what is the value of V_{out} at $V_{ID} = 0$? Why?
 - Plot the derivative of V_{OUT} vs V_{ID} . Compare the peak with A_{vd} .
- 6) CM large signal ccs (region vs V_{ICM}):
- Use **DC sweep** (not parametric sweep) $V_{ICM} = 0:10m:V_{DD}$.
 - Plot “region” OP parameter vs V_{ICM} for the input pair and the tail current source (0 cut-off, 1 triode, 2 sat, 3 subth, and 4 breakdown). Plot the results overlaid on the results of the previous method (10% reduction of GBW).
 - Plot “region” OP parameter vs V_{ICM} for the input pair and the tail current source.
 - Find the CM input range (CMIR). Compare with hand analysis in a table.
 - Note that the drawback of this method is that the “region” parameter cannot be experimentally measured in the lab.
- 7) (Optional) CM large signal ccs (GBW vs V_{ICM}):
- Use AC analysis (1Hz, 1 point only).
 - Set $V_{IDAC} = 1$ and $V_{ICMAC} = 0$.
 - Use **parametric sweep** (not DC sweep) $V_{ICM} = 0:10m:V_{DD}$.
 - Plot GBW vs V_{ICM} . Plot the results overlaid on the results of the previous method (region parameter).
- Cadence Hint: Instead of using parametric sweep, a better alternative in Cadence is to use AC sweep but sweep a design variable (V_{ICM}) instead of sweeping the frequency. The frequency is set at 1 Hz (or any other small value) to get the low frequency gain (DC gain).
- Annotate the CM input range. Calculate the input range as the range over which the GBW is within 90% of the max GBW, i.e., 10% reduction in GBW^2 .

² If you are using NMOS input pair, body effect may cause CMIR to extend till V_{DD} (why?).

PART 4: Closed-Loop OTA Simulation

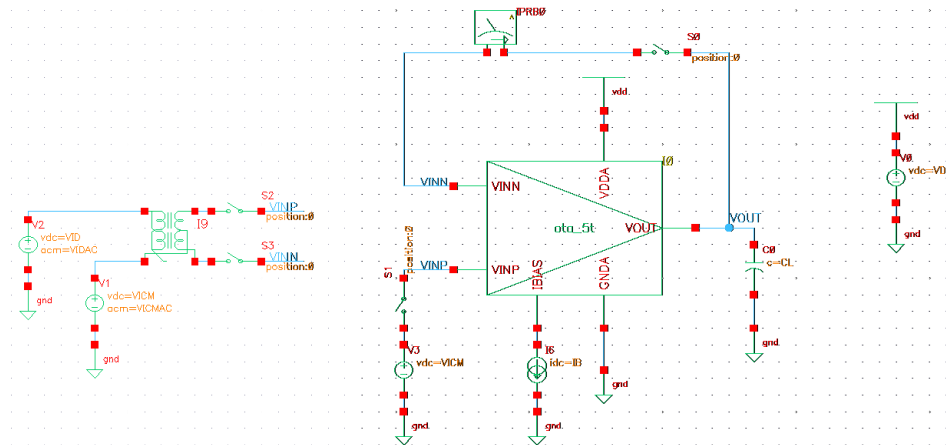


Create a testbench as shown above. Report the following:

- 1) Schematic of the OTA with DC OP point clearly annotated in unity gain buffer configuration. Use VIN = CMIR-low + 50mV.
 - Is the current (and gm) in the input pair exactly equal³? Why?
 - Calculate the mismatch in I_D and gm.
- 2) Loop gain:
 - Use STB analysis (1Hz:10GHz, logarithmic, 10 points/decade) in unity gain buffer configuration.
 - Use VICM at the middle of the CMIR.
 - Plot loop gain in dB and phase vs frequency.
 - ➔ Cadence Hint: Access STB analysis results from the results browser or from ADE results tab (Right Click in ADE Results tab-> Direct Plot -> Main Form).
 - Compare DC gain and GBW with those obtained from open-loop simulation. Comment
 - Compare simulation results with hand calculations in a table.

³ For the case of the OTA in closed-loop unity-gain buffer connection, the output will follow the input. The output voltage deviates from its CM level (the voltage at the mirror node for the 5T OTA) in order to match the input voltage. Since the gain is finite, there will be a non-zero differential input voltage that will cause an imbalance between the two sides of the differential pair. This imbalance behaves exactly like mismatch. To avoid this imbalance, we may close the loop using Vin equal to the voltage at the mirror node. Any other Vin will introduce mismatch between the gm's of the input pair, and you will have to use Avcm and CMRR equations that consider mismatch.

Part 5 (optional): Effect of Mismatch on CMRR



Copy your testbench in a new cell and modify the new schematic as shown above. Switches with different AC/DC setting are added in order to connect the feedback loop in DC and break it in AC. The DC OP point is set by the unity gain feedback buffer connection, while the AC stimulus is set by the balun. Note that the DC feedback loop will introduce mismatch in the input pair (why?). We will study the effect of mismatch on A_{vcm} and CMRR. Report the following:

- 1) CM small signal ccs:
 - Use AC analysis (at 1Hz, no frequency sweep). Keep OP simulation enabled because we will plot gm.
 - Set $VICMAC = 1$ and $VIDAC = 0$.
 - Use **parametric sweep (not DC sweep)** for $VIN = CMIR-low:10m:CMIR-high$.
 - Plot gm of the input pair overlaid vs VICM.
 - The two gm's intersect (are equal) at a specific VIN . Why? What is A_{vcm} at this value.
 - Plot CM gain at 1Hz in dB vs VIN . Extract it in Measures as shown below.
 - Add a cursor for A_{vcm} @ $VIN = CMIR-low + 50mV$. Compare simulation results with hand calculations in a table (Hint: use A_{vCM} formula that considers gm mismatch).
- 2) CMRR:
 - ➔ **Cadence Hint:** In some simulators, you have to get A_{vd} and A_{vcm} from two independent simulation runs (we cannot run both simultaneously because we have single ended output, thus we cannot differentiate between diff and CM signals at the output). But for Cadence spectre you should use XF analysis (1Hz:10GHz, logarithmic, 10 points/decade) because you need to calculate the transfer function between multiple inputs and a single output.

- Extract A_{vd} and A_{vcm} at 1Hz vs V_{IN} from two AC simulations as in the previous step (note that we cannot run both simultaneously because we have single ended output, thus we cannot differentiate between diff and CM signals at the output).
- Use **parametric sweep (not DC sweep)** for $V_{IN} = \text{CMIR-low}:10\text{m}:\text{CMIR-high}$.
- Plot CMRR in dB vs V_{IN} .
- Add a cursor for CMRR @ $V_{IN} = \text{CMIR-low} + 50\text{mV}$. Compare simulation results with hand calculations in a table (Hint: use CMRR formula that considers g_m mismatch).

Lab Summary

- In Part 1 you learned:
 - How to plot and use the g_m/I_D design curves.
- In Part 2 you learned:
 - How to design an OTA that meets desired specifications.
- In Part 3 you learned:
 - How to simulate the small-signal differential gain of a 5T OTA in open-loop configuration.
 - How to simulate the small-signal common-mode gain of a 5T OTA in open-loop configuration.
 - How to simulate the large-signal differential characteristics of a 5T OTA in open-loop configuration.
 - How to simulate the large-signal common-mode characteristics of a 5T OTA in open-loop configuration.
- In Part 4 you learned:
 - How to simulate the small-signal differential gain of a 5T OTA in closed-loop configuration.
 - How to simulate the small-signal common-mode gain of a 5T OTA in closed-loop configuration.
 - How to simulate the large-signal differential characteristics of a 5T OTA in closed-loop configuration.
 - How to simulate the large-signal common-mode characteristics of a 5T OTA in closed-loop configuration.
- In Part 5 you learned:
 - How to simulate the effect of mismatches on the characteristics of a 5T OTA.

Acknowledgements

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