Analog IC Design – Cadence and Master Micro Tools

Lab 07

gm/ID Design Methodology

Part 1: gm/ID Design Charts

NMOS

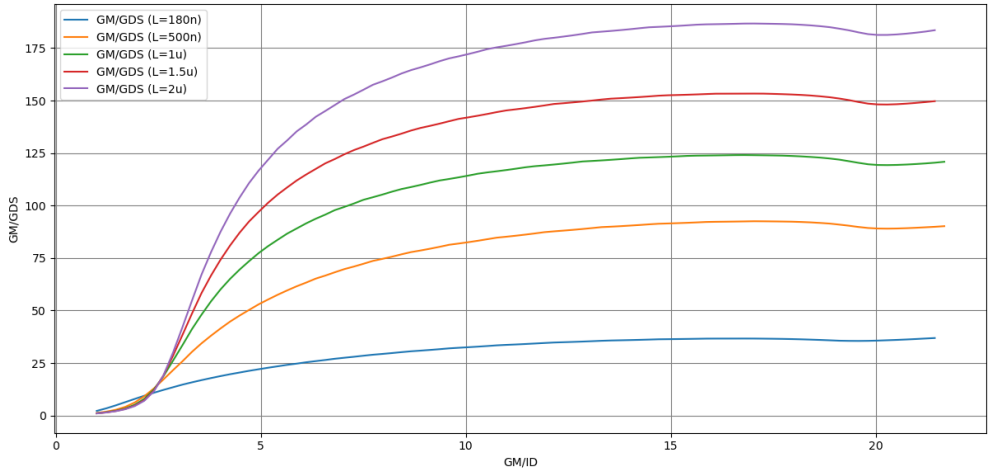


Figure 1 NMOS GM/GDS VS GM/ID

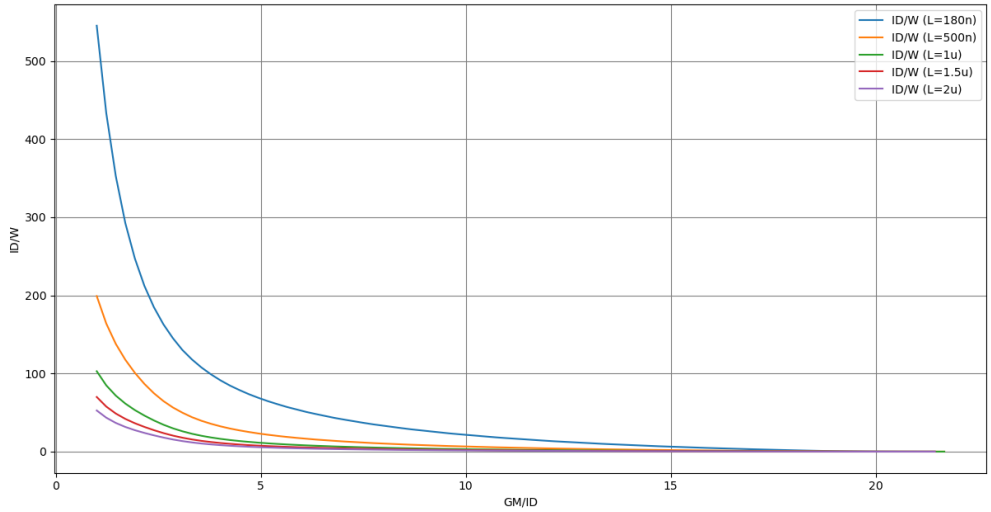


Figure 2 NMOS ID/W VS GM/ID

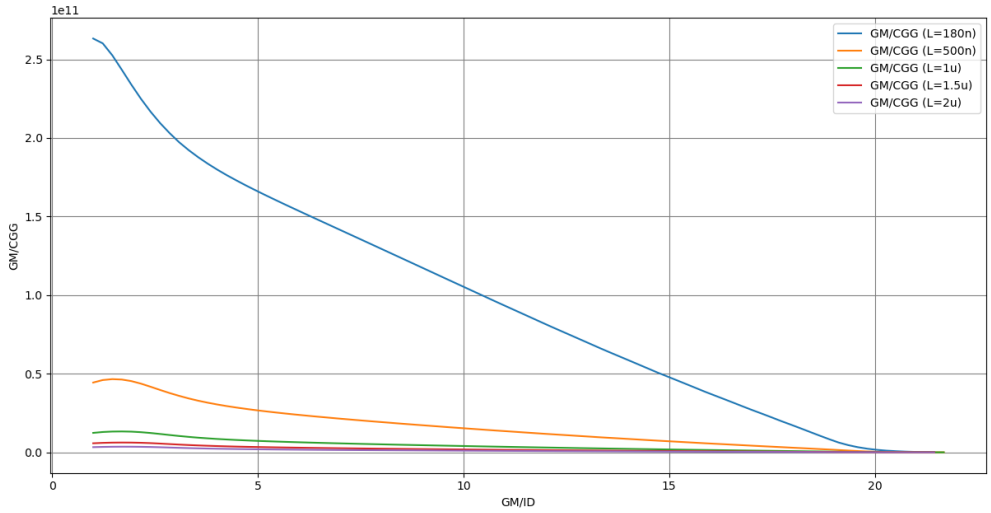


Figure 3 NMOS GM/CGG VS GM/ID

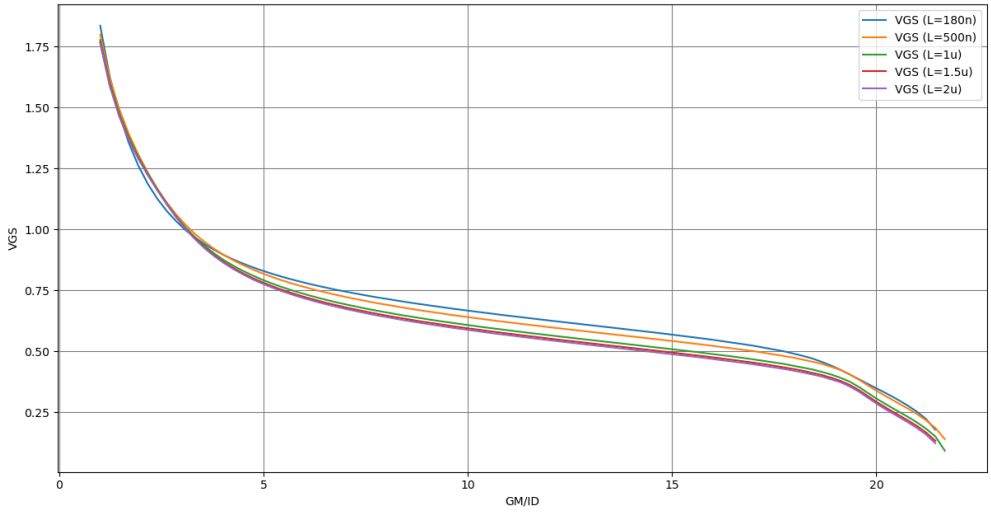


Figure 4 NMOS VGS VS GM/ID

PMOS

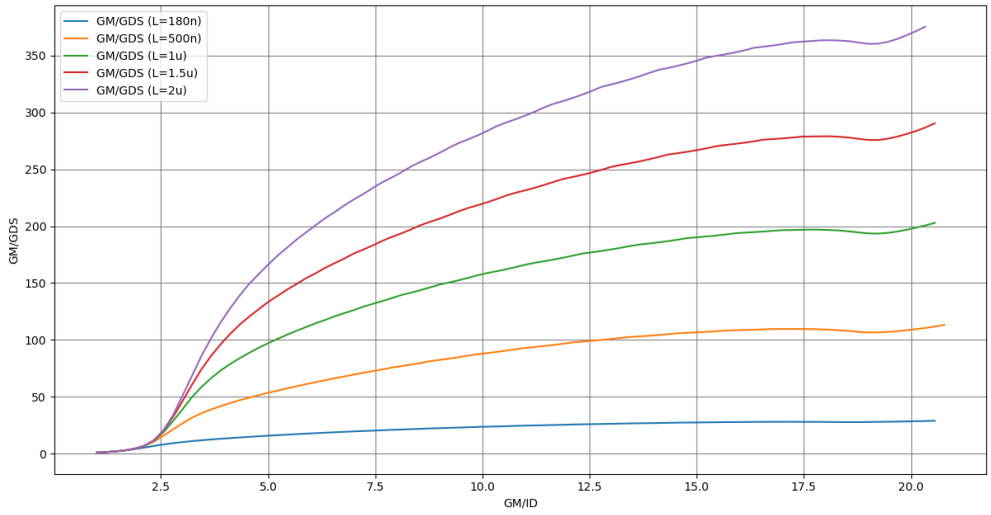


Figure 5 PMOS GM/GDS VS GM/ID

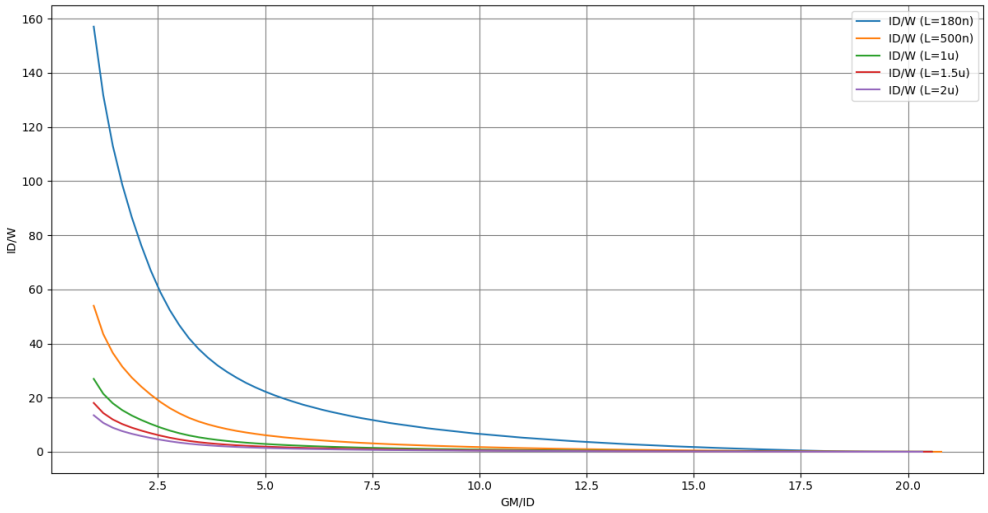


Figure 6 PMOS ID/W VS GM/ID

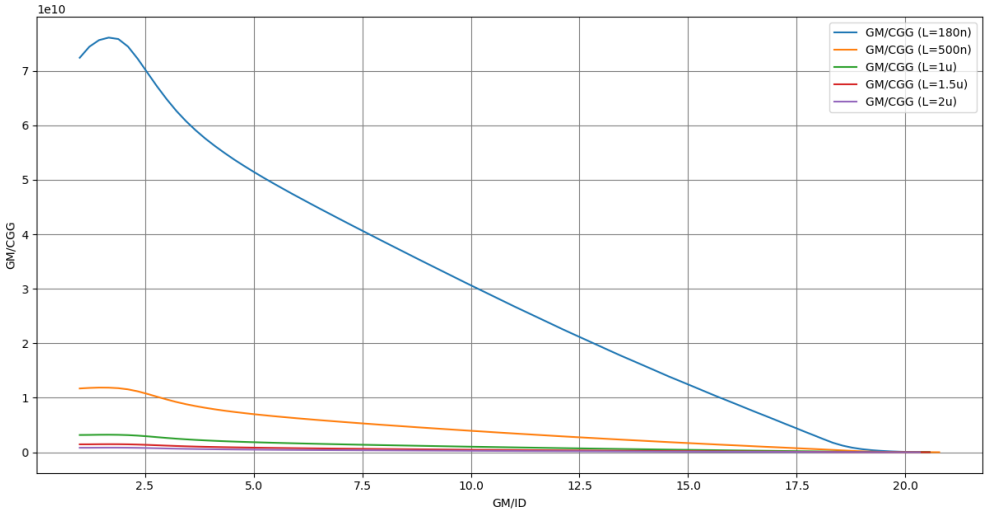


Figure 7 PMOS GM/CGG VS GM/ID

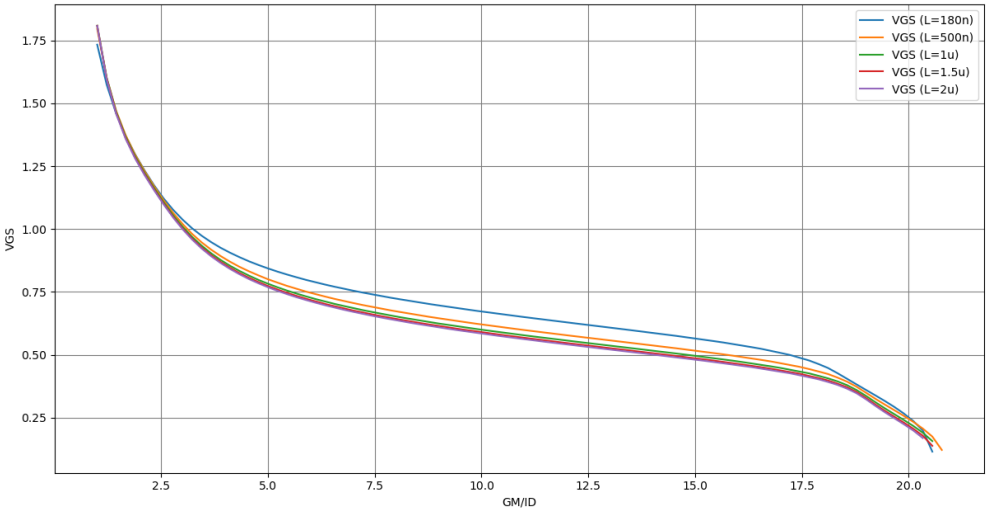


Figure 8 PMOS VGS VS GM/ID

Part 2: OTA Design

Report the following:

1) Detailed design procedure and hand analysis.

For 2 NMOS (Input pair)

GM/ID = 19 , Intrinsic Gain = 110 , L = 732.3n , W = 9.6u

For 2 PMOS (Active loads)

GM/ID = 10 , GDS = 1.732u , L = 381.5n , W = 2.86u

For Current Mirror

GM/ID = 8 , GDS = 2.489u , L = 1.64u , W =4.6328 u

We use GM/ID = 19 to make it in the WI to have high Open loop DC voltage gain.

And we use Intrinsic Gain = 110 that force the Length to be L = 771.4n and W = 9.6u for the NMOS Transistor, and so on for the other transistors.

You need to explain why you chose the architecture that you implemented.

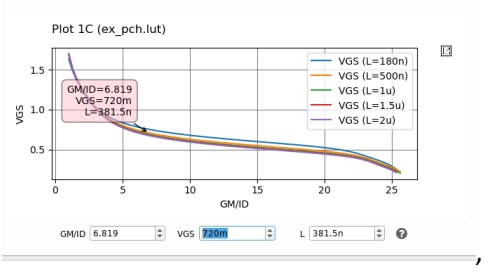
We used is NMOS for the input pair and PMOS current mirror load, as $Vicm(high)$ = 1.5V which is near to VDD

To make GBW ≥ 5MHz GBW =$\frac{\text{gm1}}{2*\pi*\text{CL}}$, CL = 5p, then we can use $gm1{,}2 = 190u$, so gm/ID $=19$

$Avd \geq 34dB$ (50.1), so we use $Avd = \text{gm/gds} = 110$

For the first transistors NMOS we designed it in the WI to guarantee high gain with small Vov & Vdsat to keep VICM_LOW , so we used gm/ID $=19$ & Gain $= 110$.

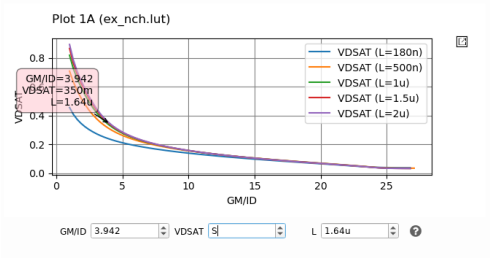
Then for the transistors PMOS (active loads) we designed it in the SI to minimize the effect of any variation on it and we designed it to have the same ro that NMOS has, and we checked the minimum gm/ID that will give us VICM_HIGH and it was equal 6.8



,

so we used gm/ID =10 & Gds = 1.732u.

Finally for the current mirror transistors we designed it in the SI to minimize the effect of any variation on it and we designed it to have the High ro that should be greater than the value of RSS that make the CMRR 74dB



, and we checked the minimum gm/ID that will give us VICM_HIGH, so we used gm/ID = 8 & Gds =2.489u.

2) Use the Sizing Assistant (SA) or the design charts in ADT to size the transistors.

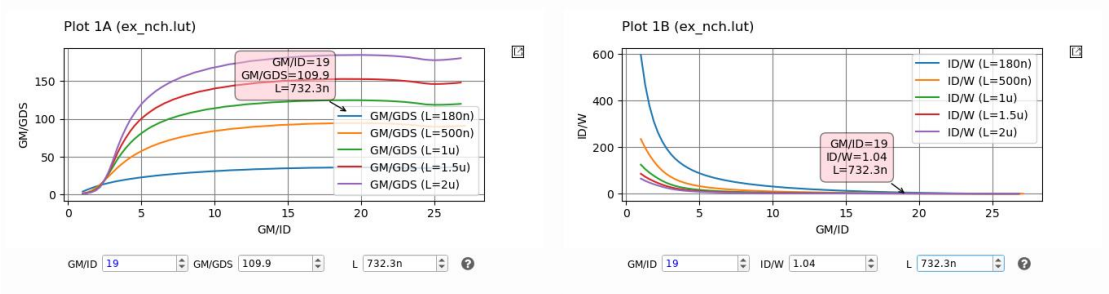


Figure 9 NMOS

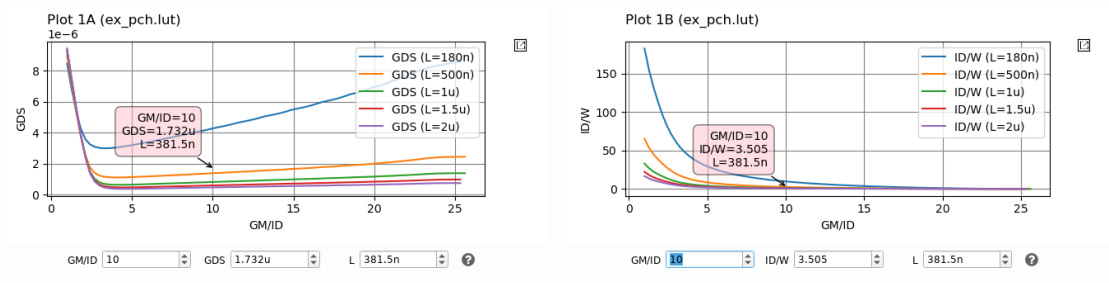


Figure 10 PMOS

$$\frac{1}{2 * gm3 * Rss} = -40dB$$

$$50 < gm3 * Rss$$

$$Rss > 500k$$

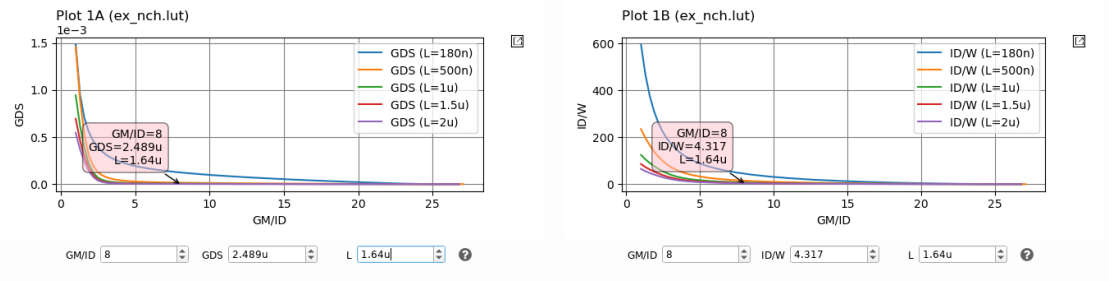


Figure 11 Current mirror

1) A table showing W, L, gm,ID, gm/ID, $VDSsat$, $Vov = VGS - VTH$, and $V* = 2ID/gm$ of all transistors (as calculated from gm/ID curves)

	NMOS	PMOS	Current Source
W	9.6u	1.533u	4.6328 u
L	732.3n	728.2n	1.64u
gm	190u	100u	80u
ID	10u	10u	20u
GM/ID	19	10	10
VDSsat	84.6m	162.7m	144.2m
Vov	74.3m	195.9m	191.6m
V*	107m	202.9m	201.3m

1) Schematic of the OTA with DC node voltages clearly annotated.

• With VICM at the middle of the CMIR.

• Is the current (and gm) in the input pair exactly equal?
YES, it is exactly equal.

• What is DC voltage at VOUT? Why?
VOUT = 1.163 V

Name	Type	Details	Value
VOUT	expr	VDC("/VOUT")	1.163

As it follows VF and it is equal VDD – VGS

2) Diff small signal ccs:

Name	Type	Details	Value	Plot	Save	Spec
VOUT	expr	VDC("/VOUT")		☐	☐	
Ao	expr	ymax(mag(VF("/VOUT")))	56.86	☑	☐	
A	expr	mag(VF("/VOUT"))		☑	☐	
Ao_dB	expr	dB20(ymax(mag(VF("/VOUT"))))	35.1	☑	☐	
BW	expr	bandwidth(VF("/VOUT") 3 "low")	107.1K	☑	☐	
UGF	expr	unityGainFreq(VF("/VOUT"))	6.125M	☑	☐	
GBW	expr	(Ao * BW)	6.091M	☑	☐	

Figure 12 circuit parameters

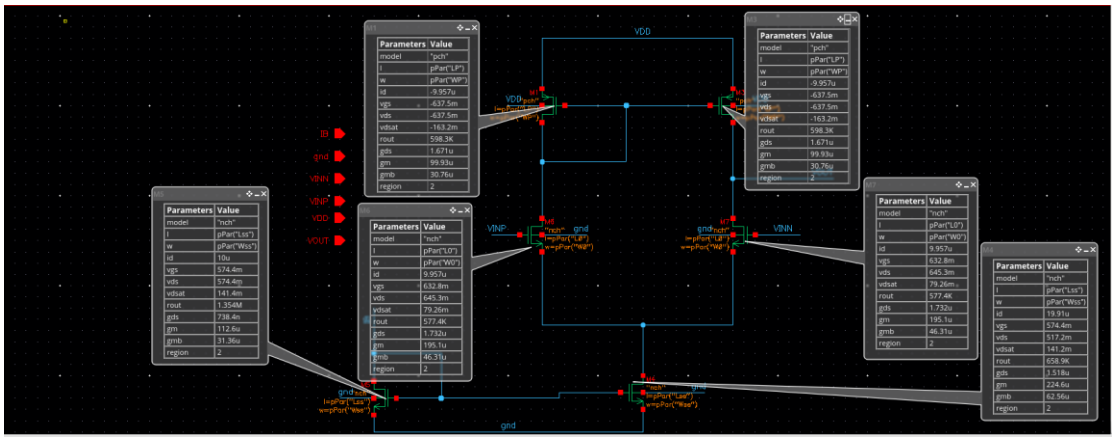


Figure 13 OP points

• Plot diff gain (in dB) vs frequency.

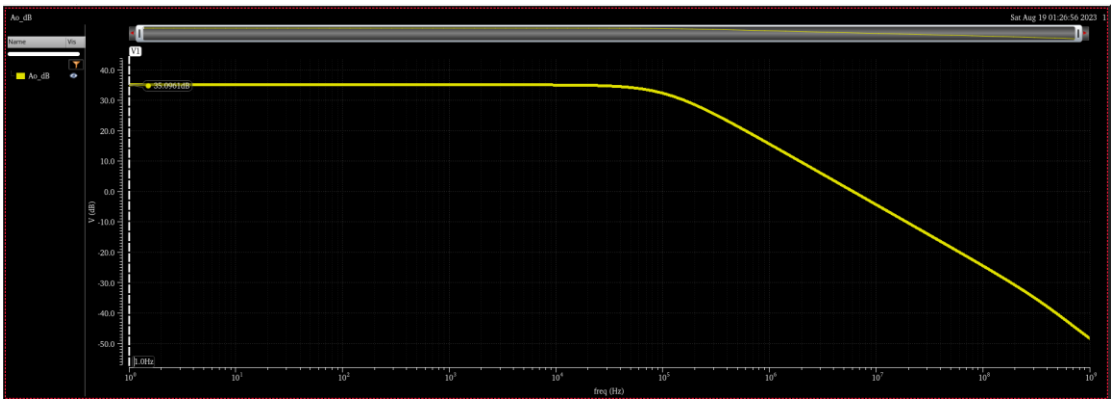


Figure 14 diff gain (dB) vs frequency

Hand Analysis

DC gain= $\frac{\text{gm}*\text{ro}}{2}$ = $\frac{195.1\text{u}}{2*1.732\text{u}}$ = 56.3 = 35 dB

Bandwidth= =$\frac{1}{\pi*\text{ro}*\text{Cl}} = \frac{1.732\text{u}}{\pi*5\text{p}} = 110.3\ k$

	Simulation	Analytic	Error
DC gain (dB)	35 dB	35 dB	0%
Bandwidth	107.1 k	$110.3\ k$	2.9%

GBW = 56 * 107 k = 6M

3) CM small signal ccs:

• Plot CM gain in dB vs frequency.

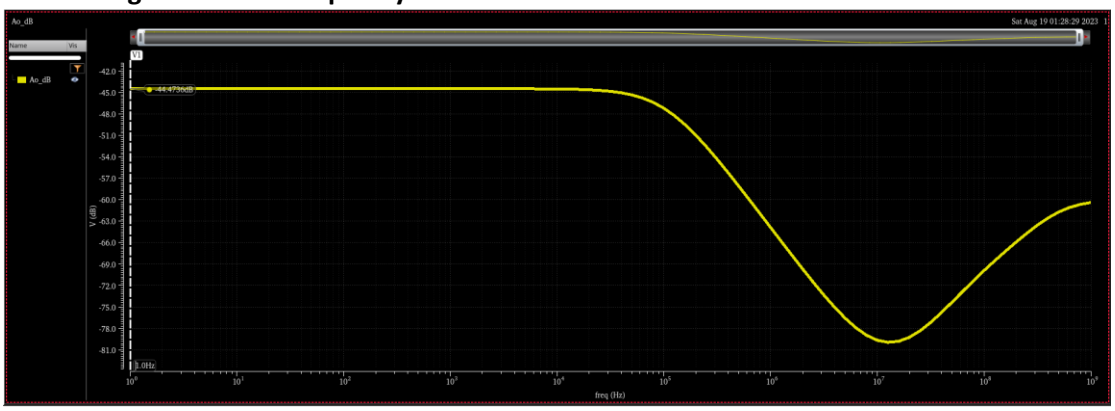


Figure 15 CM gain dB vs frequency.

Hand Analysis

DC gain= $\frac{1}{2*\text{gm3}*\text{Rss}}$ = $\frac{1.518\text{u}}{2*\ 100\text{u}}$ = 0.0076 = −42.4 dB

	Simulation	Analytic	Error
DC gain (dB)	-44.5 dB	−42.4 dB	4.7%

• (Optional) Avcm vs VICM:

➢ Plot CM gain at 1Hz in dB vs VICM.

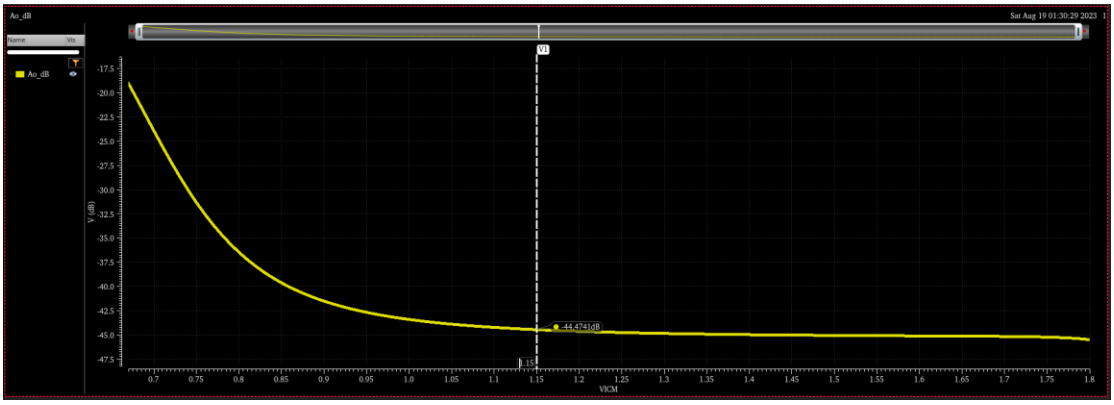


Figure 16 CM gain at 1Hz in dB vs VICM

➢ $AvCM$ is inversely proportional with $Vicm$, so increaseing VDS of the current mirror will increase its output resistance Rss, so $AvCM$ decreases, as $AvCM$ is inversely proportional with Rss.

4) CMRR:

• Plot CMRR in dB vs frequency at VICM at the middle of the CMIR.

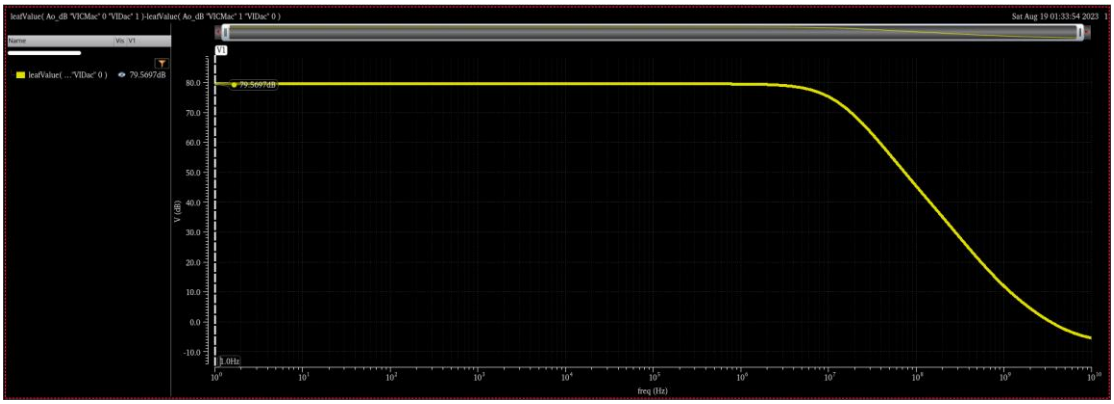


Figure 17 CMRR in dB vs frequency

$$CMRR = \frac{\text{Avd}}{\text{AvCM}} = \frac{56.3}{0.0076} = 35(dB) + 44.4\ (dB) = 79.4(dB)$$

	Simulation	Analytic	Error
$\boldsymbol{CMRR}$	**79.6**	**79.4**	**0.25%**

• (Optional) CMRR vs VICM:

➢ Plot CMRR at 1Hz in dB vs VICM.

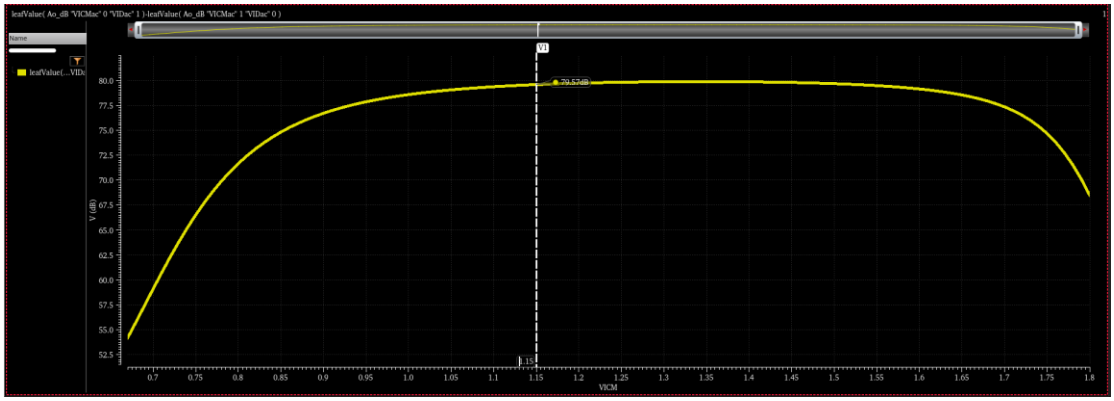


Figure 18 CMRR at 1Hz in dB vs VICM

➢ The first part of the curve of the CMRR increases with $Vicm$,as $AvCM$ is inversely proportional with $Vicm$, so increasing VDS of the current mirror will increase its output resistance Rss, $AvCM$ decreases, as $AvCM$ is inversely proportional with Rss, but at higher values it decreases again as $Vicm$ proportional with $VGD1$ so the input pair transistor is pushed towards the triode, so $ro1$ decreases so CMRR decreases again as Avd decreases.

5) Diff large signal ccs:

• Plot VOUT vs VID.

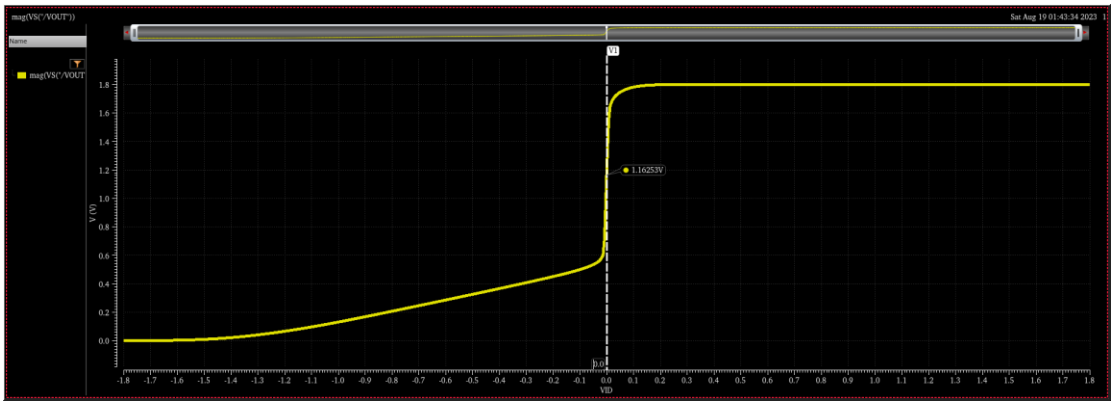


Figure 19 VOUT vs VID.

• From the plot, what is the value of Vout at VID = 0? Why?
1.16 V , as it is the same value for DC voltage at VOUT for input common mode as there is no differential input.

• Plot the derivative of VOUT vs VID. Compare the peak with Avd.

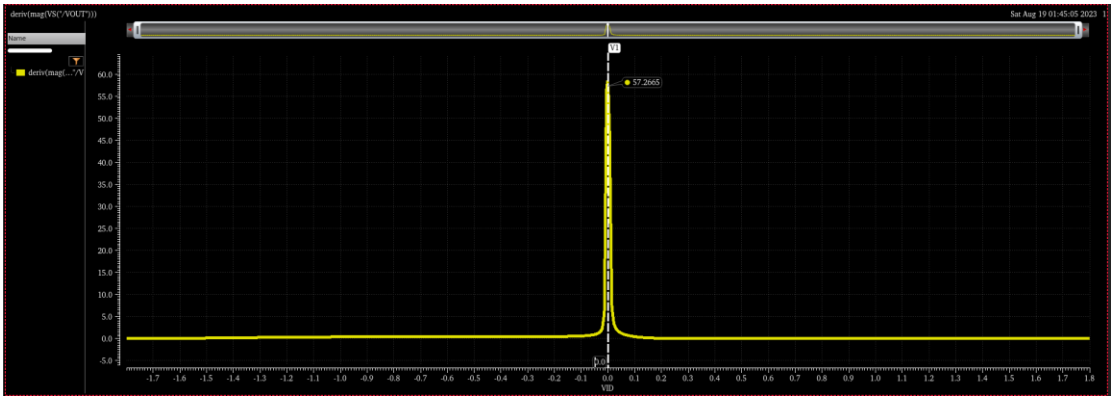


Figure 20 derivative of VOUT vs VID

Compare the peak with Avd.
the peak > Avd.

	Peak	Avd	ERROR
VALUE	57.3	56.2	1.9%

6) CM large signal ccs (region vs VICM):

• Plot "region" OP parameter vs VICM for the input pair and the tail current source

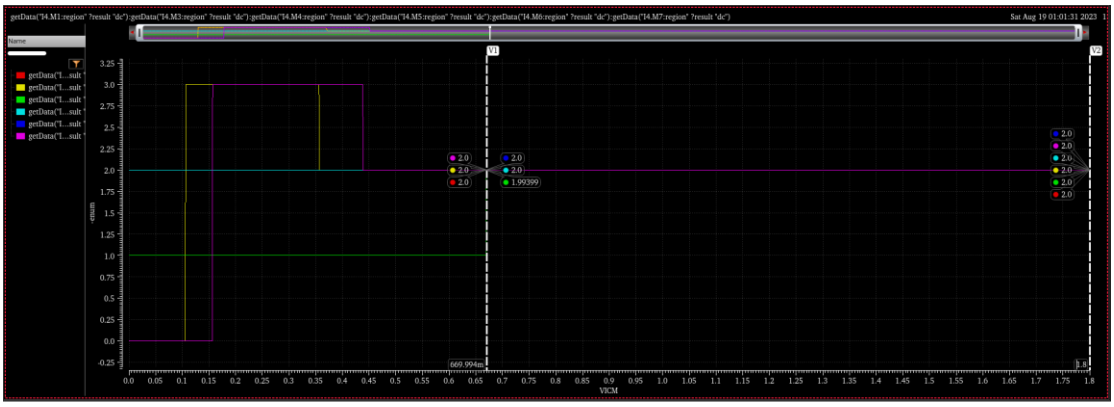


Figure 21 INPUT_CM Range

• Find the CM input range (CMIR). Compare with hand analysis in a table.

hand analysis
Tail CS in sat
$ViCM \geq VTHN + Vov1 + V$**dsat5**
$ViCM \geq$ **(632.8+ 141.2) m = 774 mV**
Input pair in sat
$ViCM \leq VDD -$ $\boldsymbol{VTHP}$ $- Vov3 + VTH$**N**
$ViCM \leq$ **1.8 – 637.5m + 567m = 1.73 V**

	Simulation	Hand Analysis
$ViCM$_MIN	669 mV	774 mV
$ViCM$_MAX	1.8 V	1.73 V

7) (Optional) CM large signal ccs (GBW vs VICM):

• Plot GBW vs VICM. Plot the results overlaid on the results of the previous method (region parameter).

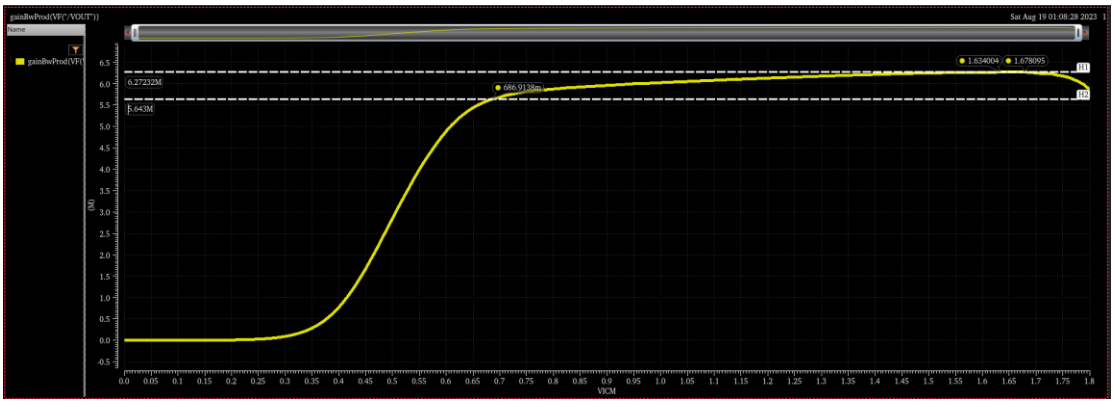
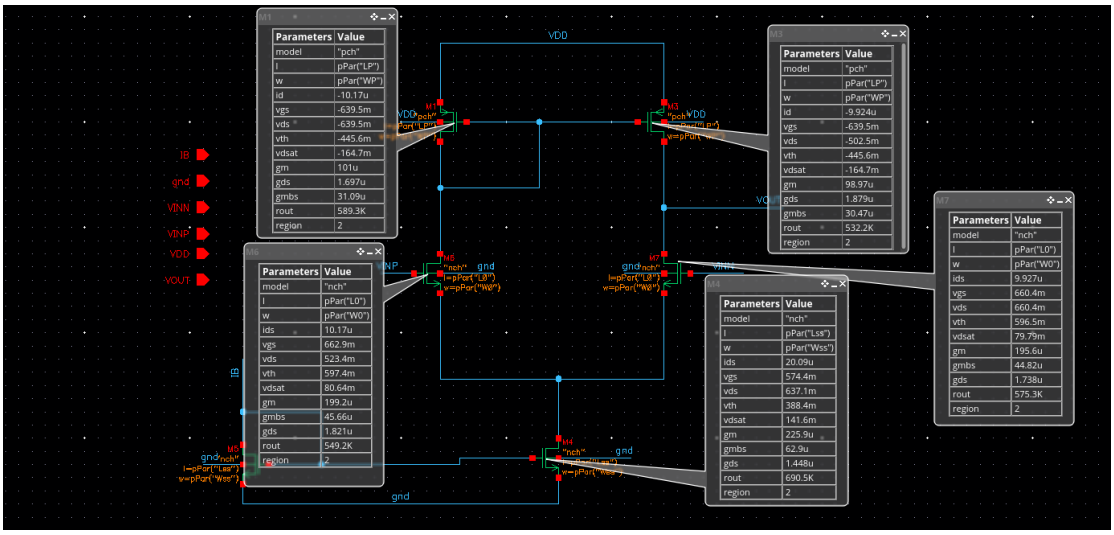


Figure 22 GBW vs VICM

• Annotate the CM input range. Calculate the input range as the range over which the GBW is within 90% of the max GBW, i.e., 10% reduction in GBW2.

the input range is [686.9 mV : 1.8 V]

PART 4: Closed-Loop OTA Simulation



• Is the current (and gm) in the input pair exactly equal? Why?

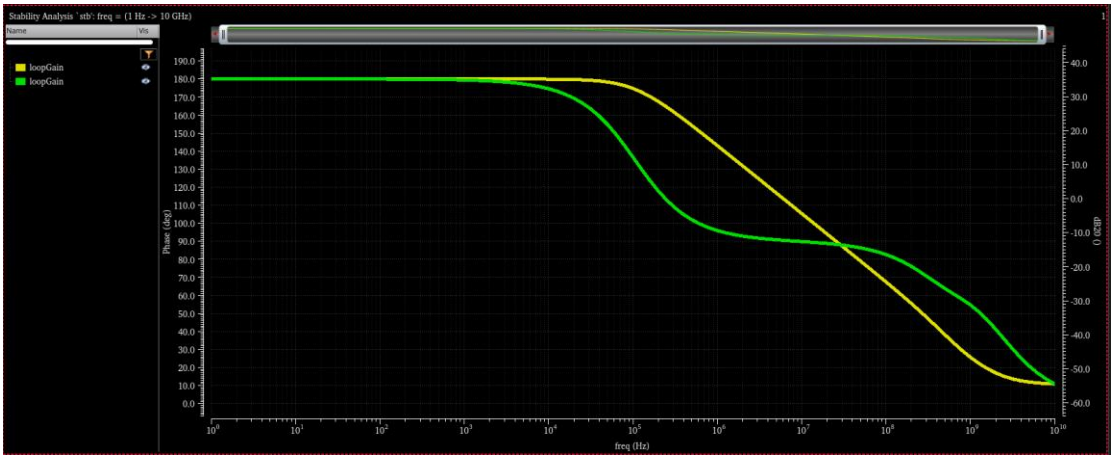
NO, as the feedback network will try to maintain a constant output voltage, which will cause the current in the input pair to vary depending on the input voltage. The gm of the input pair will also vary depending on the current.
We can analyze it from another aspect as the gain is finite, so there will be a non-zero differential input voltage which makes an imbalance between the two sides of the differential pair which makes the mismatch and when we close the loop Vin introduces mismatch between the gm's of the input pair.

• **Calculate the mismatch in ID and gm.**

$$\nabla I_D = 10.17 - 9.924 = 0.246\mu$$
$$\nabla g_m = 101 - 98.97 = 2.03\mu$$

2) Loop gain:

• **Plot loop gain in dB and phase vs frequency.**



Compare DC gain and GBW with those obtained from open-loop simulation.

GBW(**open-loop)** = 56 * 107 k = 6M

GBW(**closed-loop)** = 56 * 105 k =5.9M

Comment

DC gain and GBW with those obtained from open-loop and closed loop is the same, but the closed loop has small error due to the mismatch in gm and ID.

Hand Analysis

DC gain= $\frac{\text{gm}*\text{ro}}{2}$ = $\frac{195.1\text{u}}{2*1.732\text{u}}$ = 56.3 = 35 dB

Bandwidth= =$\frac{1}{\pi*\text{ro}*\text{Cl}} = \frac{1.732\text{u}}{\pi*5\text{p}} = 110.3\ k$

GBW = 56.3 * 110.3 k = 6.2M

	Simulation	Analytic	Error
DC gain (dB)	35 dB	35 dB	0%
GBW	5.9M	6.2M	5%

Part 5 (optional): Effect of Mismatch on CMRR

- **Plot gm of the input pair overlaid vs VICM.**

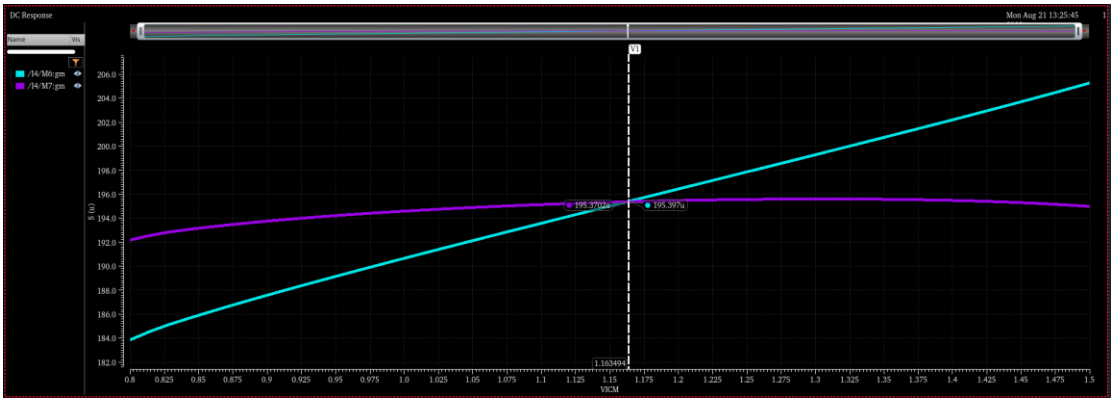
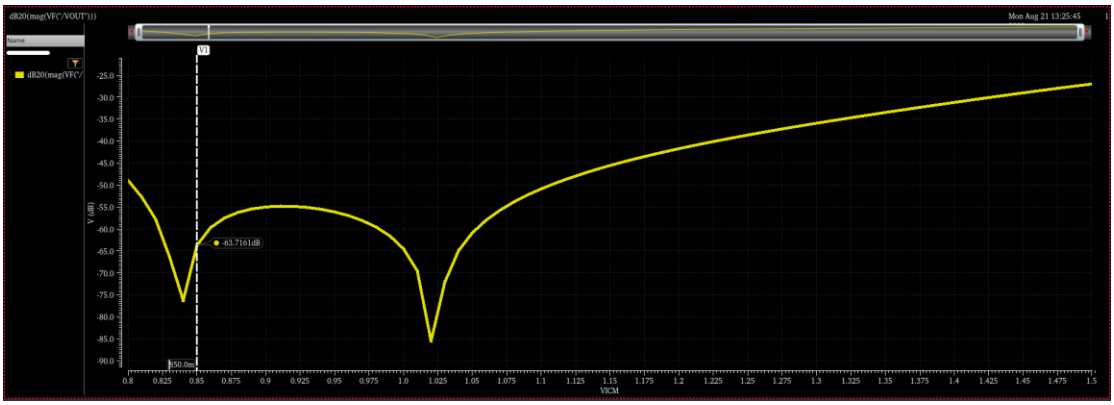


Figure 23 gm of the input pair overlaid vs VICM

The two gm's intersect (are equal) at VIN = 1.163 as it is the DC voltage at VOUT when VICM be at the middle of the CMIR and there is no VIDIFF. Avcm = -44.5 dB

- **Plot CM gain at 1Hz in dB vs VIN. Extract it in Measures as shown below.**



2) CMRR:

- **Plot CMRR in dB vs VIN.**

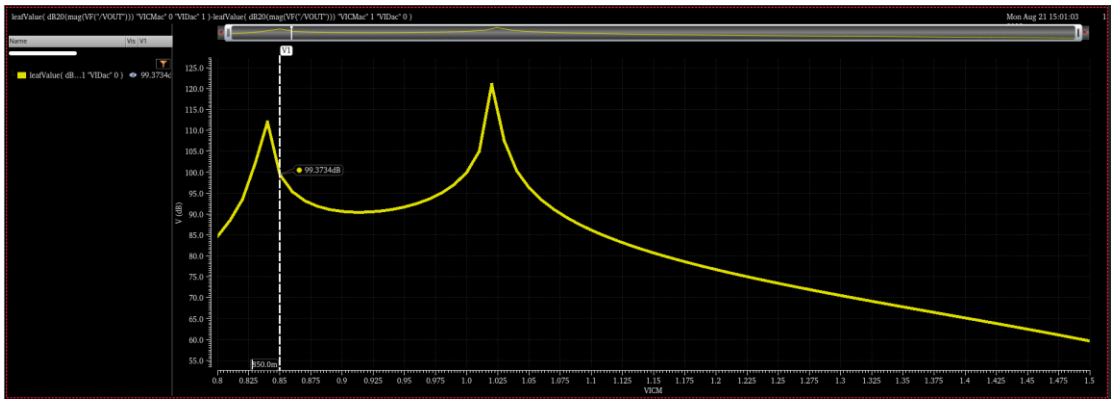


Figure 24 CMRR in dB vs VIN