وَمَا أُوتِيتُمْ مِنَ الْعِلْمِ إِلَّا قَلِيلًا

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Analog IC Design – Cadence Tools
Lab 01
LPF Simulation and MOSFET Characteristics

Intended Learning Objectives

This lab is divided into two parts:

- In Part 1 you will
  - Get familiar with Cadence custom IC design tools (Virtuoso Environment).
  - Learn the different types of simulations (transient, ac, pole-zero).
  - Learn how to run parametric sweeps.
- In Part 2 you will
  - Learn the difference between DC and parametric sweeps.
  - Compare the behavior of PMOS and NMOS transistors.
  - Compare the behavior of short-channel and long-channel MOSFETs.

PART 1: Low Pass Filter Simulation (LPF)

1. Transient Analysis

1) Design a first order low pass filter that has $R = 1k\Omega$ and 1ns time constant.
2) Apply a square wave input with $T_{high} = Pulse\ Width = 10ns$, $T_{clk} = Period = 20ns$, and $T_{rise} = T_{fall} = 100ps$.
3) Report transient analysis results for two periods (use max time step $= T_{clk}/100$).
4) Calculate rise and fall time (10% to 90%) using Cadence calculator expressions. Export the expressions to adexl.
5) Compare simulation with analytical results in a table.
6) Do parametric sweep for $R = 1{:}\ 1{:}\ 5k\Omega$. Report overlaid results. Comment on the results.

2. AC Analysis

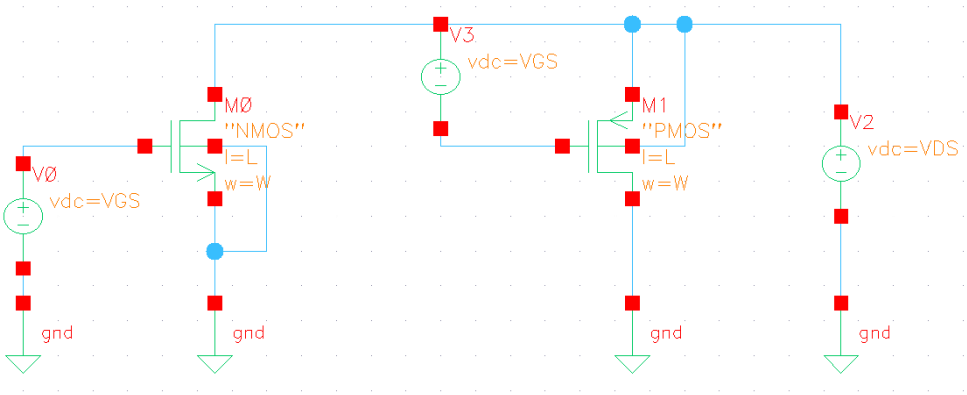
1) Report Bode Plot (magnitude and phase) for the previous LPF.
2) Calculate DC gain and 3dB bandwidth using Cadence calculator expressions. Export the expressions to adexl.
3) Compare simulation with analytical results in a table.
4) Do parametric sweep for $R = 1{,}10{,}100{,}1000k\Omega$. Report overlaid results. Comment on the results.

3. [Optional] Pole Zero Analysis

1) Report pole zero analysis results.
2) Find the pole frequency and compare it with the bandwidth calculated from AC analysis.

Part 2: MOSFET Characteristics

Create a testbench to characterize NMOS and PMOS devices as shown in the figure below.



1. ID vs VGS

1) Plot $I_D - V_{GS}$ characteristics for NMOS and PMOS devices. Set $V_{DS} = V_{DD}$, and $V_{GS} = 0{:}\,10m{:}\,V_{DD}$. Use $V_{DD} = 1.2V$ for 130nm technology and $V_{DD} = 1.8V$ for 180nm technology. Plot the results overlaid for the following:
   - Short channel device: $W = 1\mu m$ and $L = 200nm$
   - Long channel device: $W = 10\mu m$ and $L = 2\mu m$.
     Hint: Set L as a parameter and set $W = 5 \times L$

➔ Cadence Hint: Use DC sweep instead of parametric sweep whenever possible. DC sweep is extremely faster, and uses much less resources and disk space. In this question you should use DC sweep for VGS.

➔ Cadence Hint: To simulate both the short channel and the long channel devices in the same simulation run you can use parametric sweep. Define L as a parameter (L = 200n, 2u) and define W as a function of L (W = 5*L).

2) Comment on the differences between short channel and long channel results.
   - Which one has higher current? Why?
   - Is the relation linear or quadratic? Why?
3) Comment on the differences between NMOS and PMOS.
   - Which one has higher current? Why?
   - What is the ratio between NMOS and PMOS currents at VGS = VDD?
   - Which one is more affected by short channel effects?

2. g_m vs VGS

1) Plot g_m vs V_{GS} for NMOS device. Set $V_{DS} = V_{DD}$, and $V_{GS} = 0{:}\,10m{:}\,V_{DD}$. Plot the results overlaid for the following:
   - Short channel device: $W = 1\mu m$ and $L = 200nm$
   - Long channel device: $W = 10\mu m$ and $L = 2\mu m$.
2) Comment on the differences between short channel and long channel results.
   - Does g_m increase linearly? Why?
   - Does g_m saturate? Why?

➔ Cadence Hint: In order to save gm vs DC sweep variable, create an empty text file and write the following statement (without quotes): “save *:gm sigtype=dev”. To save all OP point parameters

for all transistors use (without quotes): "save *:oppoint sigtype=dev". Add this text file in adexl (Setup -> Model Libraries). You need to do this in every new testbench whenever you need to save small signal parameters.

3. ID vs VDS

1) Plot $I_D - V_{DS}$ characteristics for NMOS device. Set $V_{DS} = 0{:}\,10m{:}\,V_{DD}$, and $V_{GS} = 0{:}\,0.2{:}\,V_{DD}$ (nested sweep). Plot the results overlaid for the following:
    - Short channel device: $W = 1\mu m$ and $L = 200nm$
    - Long channel device: $W = 10\mu m$ and $L = 2\mu m$.

➔ Cadence Hint: In Mentor Eldo and Synopsys HSPICE you can do nested DC sweep (DC sweep with multiple variables) . But in Cadence Virtuoso you can use only one DC sweep variable. Thus, you should use DC sweep for the variable with fine step, i.e., the primary variable (VDS in this case), and parametric sweep for the variable with coarse step, i.e., secondary variable (VGS in this case). Actually, Cadence simulation engine (Spectre) can run nested DC sweeps if you invoke it from the command prompt rather than the GUI.

2) Comment on the differences between short channel and long channel results.
    - Which one has higher current? Why?
    - Which one has higher slope in the saturation region? Why?

4. [Optional] g_m and r_o in Triode and Saturation

1) Plot g_m and r_o vs V_{DS} for NMOS device. Use $W = 10\mu m$ and $L = 2\mu m$, $V_{DS} = 0{:}\,10m{:}\,V_{DD}$, and $V_{GS} \approx V_{TH} + 0.5V$.
   Hint: You can get an estimate of V_{TH} from the I_D vs V_{GS} characteristics, or you can print the operating point parameters of the transistor from DCOP/TRAN in Pyxis.
2) Comment on the variation of g_m vs V_{DS}.
    - In the first part of the curve, is the relation linear? Why?
    - Does g_m saturate? Why?
    - Where do you want to operate the transistor for analog amplifier applications? Why?
3) Comment on the variation of r_o vs V_{DS}.
    - Does r_o saturate just after the transistor enters saturation similar to gm? Why?
    - Does r_o increase if the transistor is biased more into saturation?
    - Should we operate the transistor at the edge of saturation?
    - Where do you want to operate the transistor for analog amplifier applications? Why?

Lab Summary

- In Part 1 you learned
    - How to run transient simulations.
    - How to run ac-analysis simulations.
    - How to run pole-zero simulations.
    - How to run parametric sweeps.
- In Part 2 you learned
    - How to plot the transistors I/V characteristics using DC analysis.
    - How to plot the transistors I/V characteristics using parametric sweeps.
    - The difference in transistor characteristics between an NMOS and a PMOS transistor.
    - The difference in transistor characteristics between a short-channel and a long-channel MOSFET.

- How the g_m of the transistor behaves vs VGS.
- How the g_m and r_o of the transistor behave in triode and in saturation.

Acknowledgements

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