Analog IC Design – Cadence Tools

Common Source Amplifier

Lab 02

PART 1: Sizing Chart

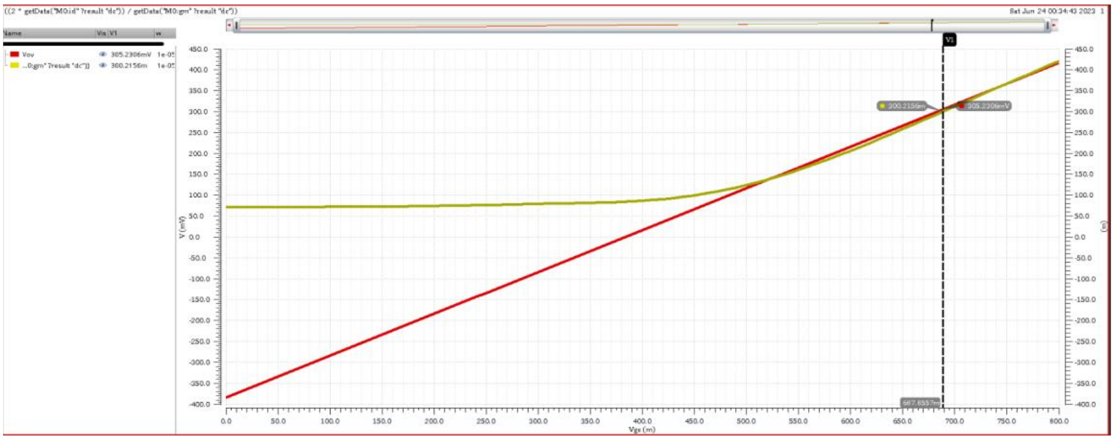


Figure 1 $V*$ *and* Vov *VS VGS*

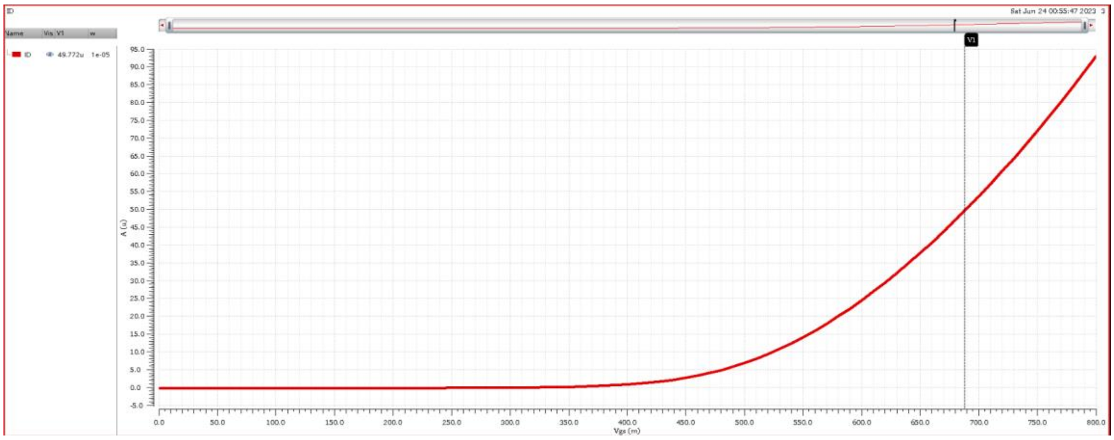


Figure 2 Id Vs VGS

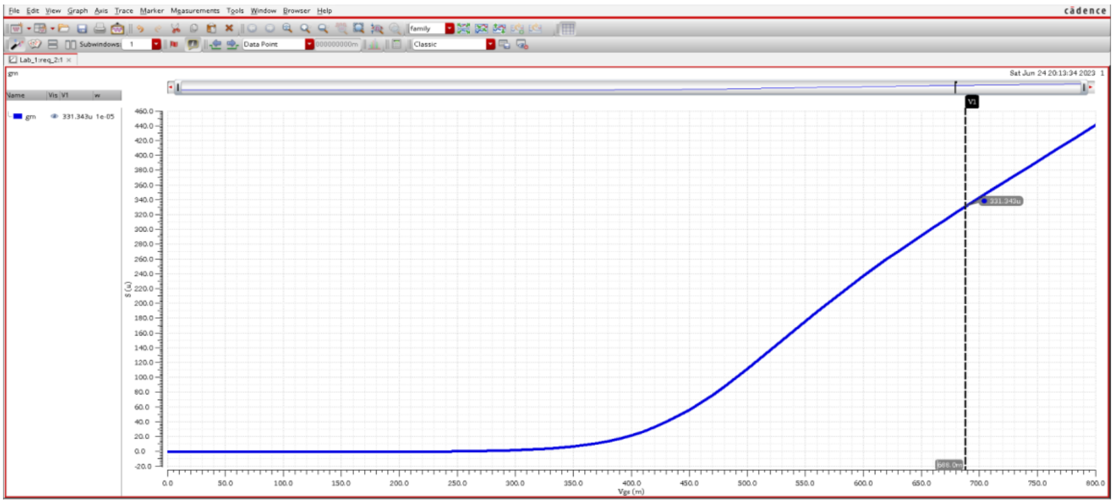


Figure 3 gm VS VGS

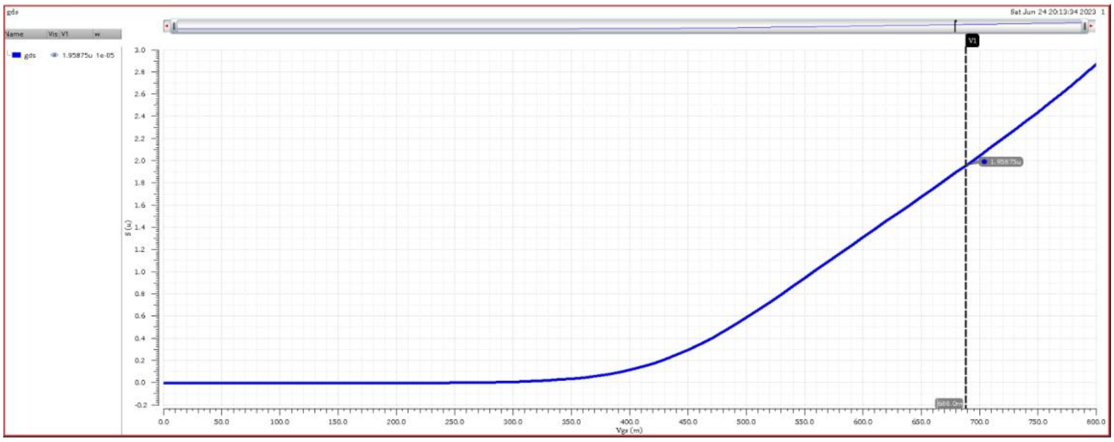


Figure 4 gds VS VGS

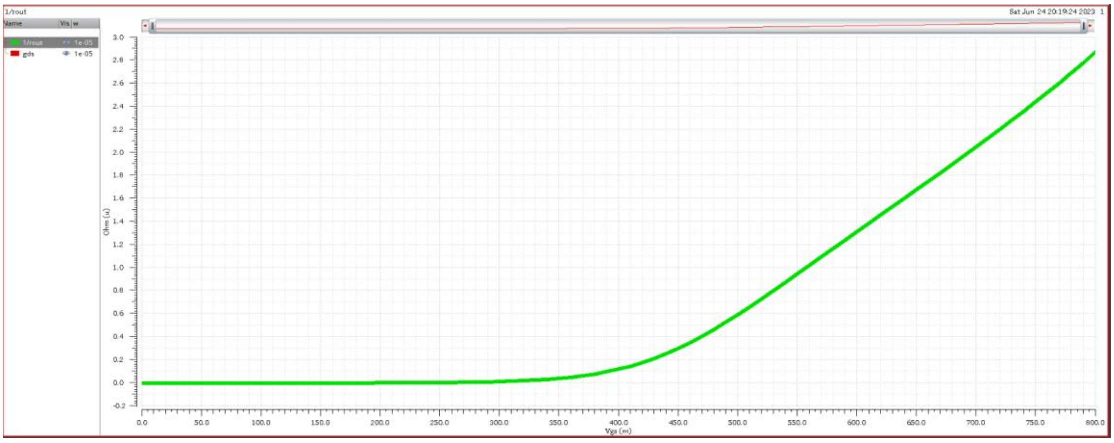


Figure 5 gds and (1/ro) are the same for certain VDS

At $V_Q^* = 0.3 , V_{GS} = 688m , I_D = 50\mu$

W	I_D
10μ	50μ
30μ	150μ

gm	I_D
332μ	50μ
996μ	150μ

gds	I_D
1.9588μ	50μ
5.8764μ	150μ

Checking:

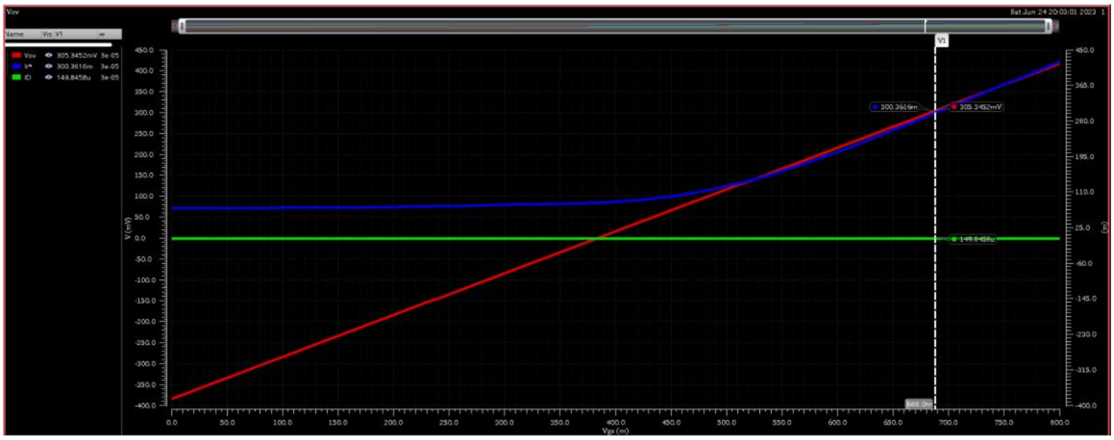
At: $V_{DD} = 1.8$

$R_D = 6k$

$V_{GS} = 688m$

$W = 30\mu$

$$\|A_v\| = g_m * R_D = \frac{2 * I_D * R_D}{V_{ov}} = \frac{2 * 150 * 6}{300} = 6$$



Equations

DC gain = -6 and ID = 150uA. VDD = 1.8V, L= $2\mu m$.

For MAX Swing

$$V_{RD} = V_{DS} = \frac{V_{DD}}{2} = 0.9\ v$$

$$R_D = \frac{0.9}{150\mu} = 6\ k\ \Omega$$

$$\|A_v\| = g_m * R_D = \frac{2 * I_D * R_D}{V_{ov}} = 6$$

(But V_{ov} isn't valid here)

Let's assume the width =10 μm.

$$V^* = \frac{2 * 0.9}{6} = 0.3$$

$$V_{GS} = 688m$$

PART 2: CS Amplifier

1. OP and AC Analysis

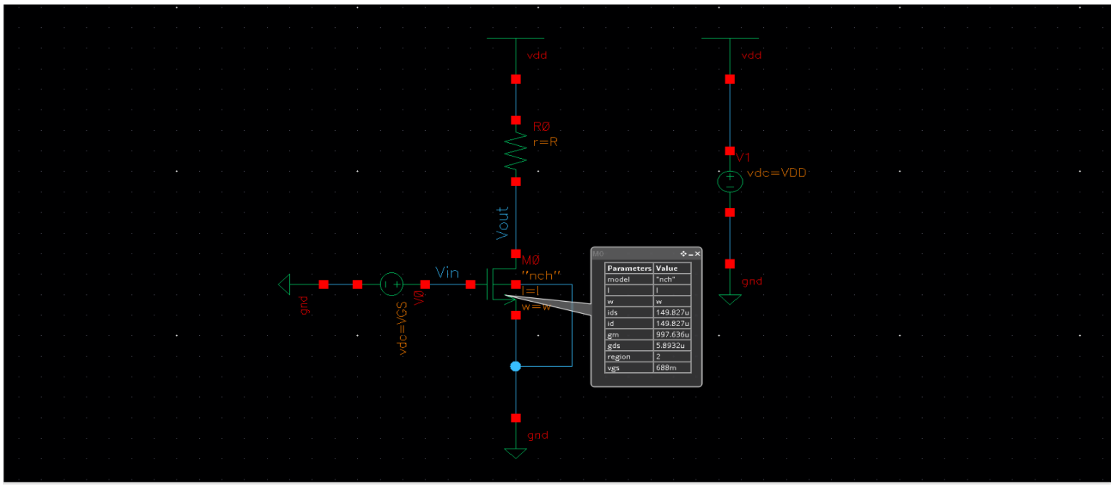


Figure 6 the DC OP

Test	Output	Nominal	Spec	Weight	Pass/Fail
Lab_2:req_2:1	id	149.8u			
Lab_2:req_2:1	gm	997.6u			
Lab_2:req_2:1	gds	5.893u			
Lab_2:req_2:1	rout	169.7k			
Lab_2:req_2:1	Gain	5.986			

Figure 7 the DC OP

It is almost the same results obtained in Part 1.

3) $R_D = 6\ k\ \Omega\ , r_o = 169.7\ k\ \Omega\ , \because\ R_D \ll r_o\ , \therefore\ (R_D//r_o) \approx R_D$

$$(R_D//r_o) = 5.795k$$

$$\text{Error} = \left|\frac{(R_D//r_o)-R_D}{(R_D//r_o)}\right| = \left|\frac{5.795-6}{5.8}\right| = 0.035$$

$$\|A_v\| = g_m * (R_D//r_o) = 5.781092$$

if we use min L, the error will not remain the same, and ro will be smaller and the error will be larger.
as L is directly proportional with ro.

4) The intrinsic gain of the transistor $= g_m * r_o = 997.6u * 169.7k = 169.293$
5) The amplifier gain $= g_m * R_D = 6$, The amplifier gain << The intrinsic gain.
6)

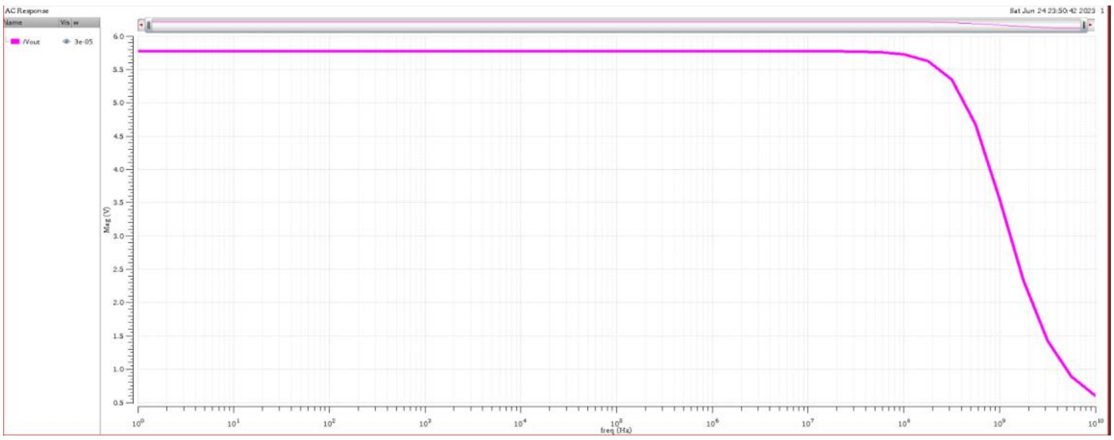


Figure 8 Vout VS Frequency (AC analysis)

AC Gain = 5.78v ,it meets the spec.

It act as LPF with Bandwidth = 791.6 M

2. Gain Non-Linearity

2)

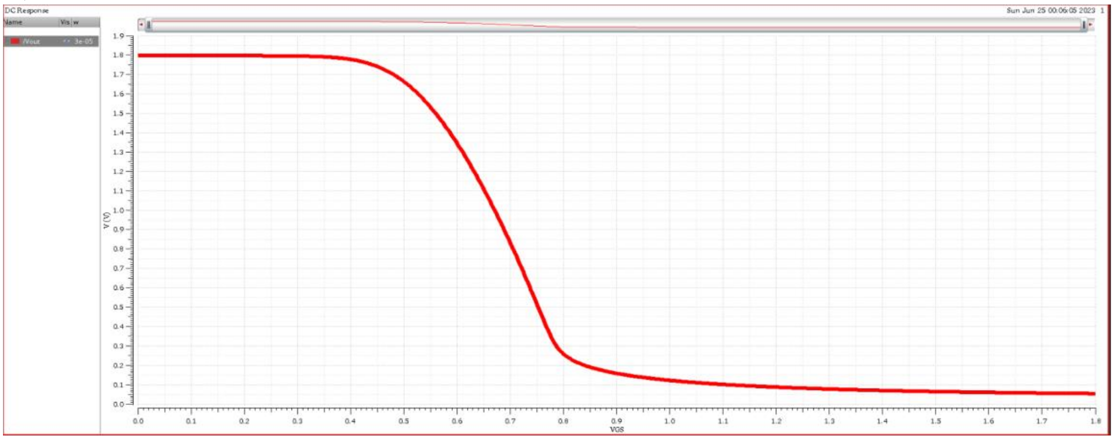


Figure 9 VOUT vs VIN (DC Sweep)

The relation between VOUT and VIN is non-linear

As it consists of 3 regions (cutoff, saturation, triode).

In the triode region of a MOSFET, When the gate-source voltage (VGS) is sufficiently low, VOUT and VIN have a linear relationship. The slope of this relationship depends on the MOSFET's transconductance (gm) and the load resistance (RD). However, as the drain-source voltage (VDS) increases, the MOSFET can transition to other regions, altering the linearity.

In the saturation region, where both VGS and VDS are high, VOUT remains relatively constant. Its value is determined by the supply voltage and other circuit parameters. The relationship between VOUT and VIN in this region is nonlinear.

Several factors influence the specific linearity characteristics, including the MOSFET's threshold voltage (Vth), the load impedance, and the circuit's biasing conditions. Additionally, higher-order effects like channel-length modulation and the Early effect can also impact the linearity between VOUT and VIN in large-signal MOSFET circuits.

3)

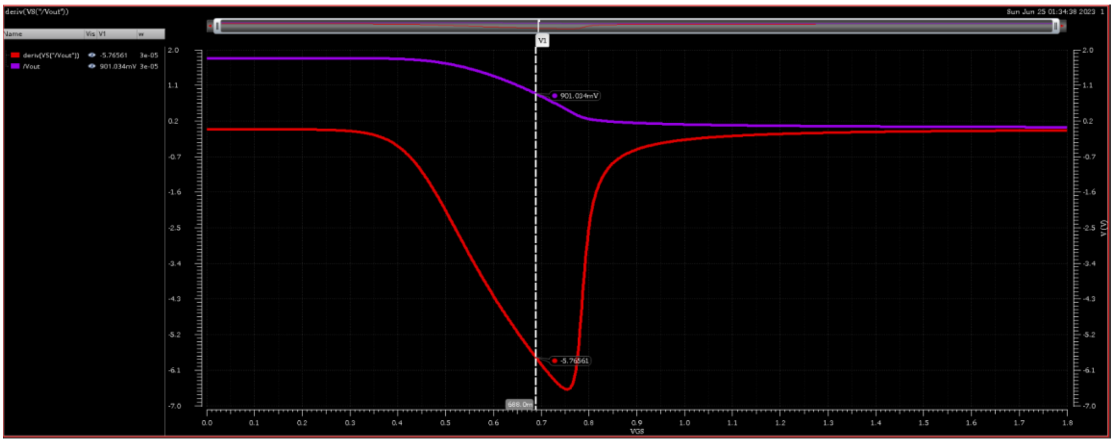


Figure 10 Scaled Gain (Derivative Vout) VS VGS

the gain is non-linear, Because the relation in saturation region follows the square law and the value of gm, and that is non-linear relation.

$$V_{out} = V_{DD} - I_D * R_D = V_{DD} - \frac{K_n}{2} * (V_{GS} - V_{th})^2 * R_D$$

4)

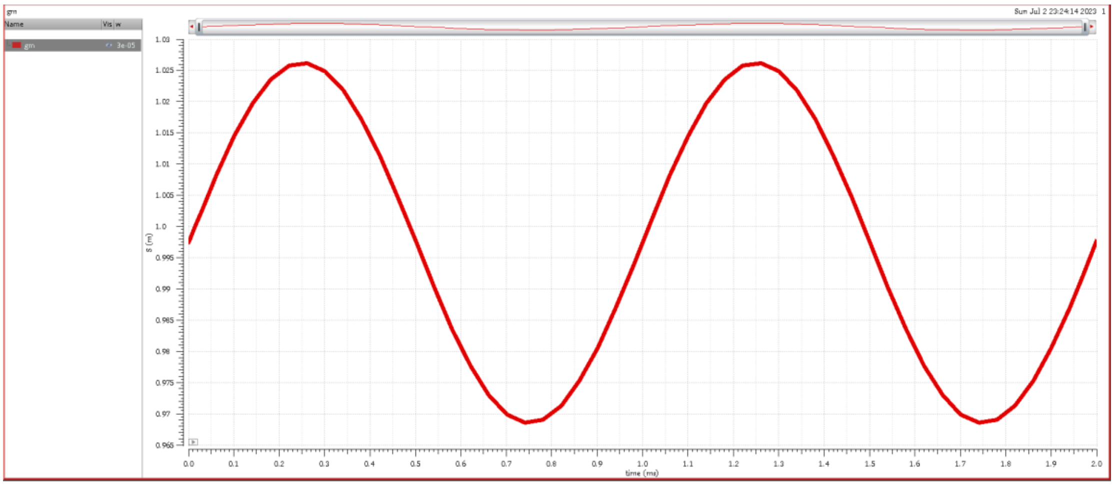


Figure 11 gm VS Time (Transient analysis)

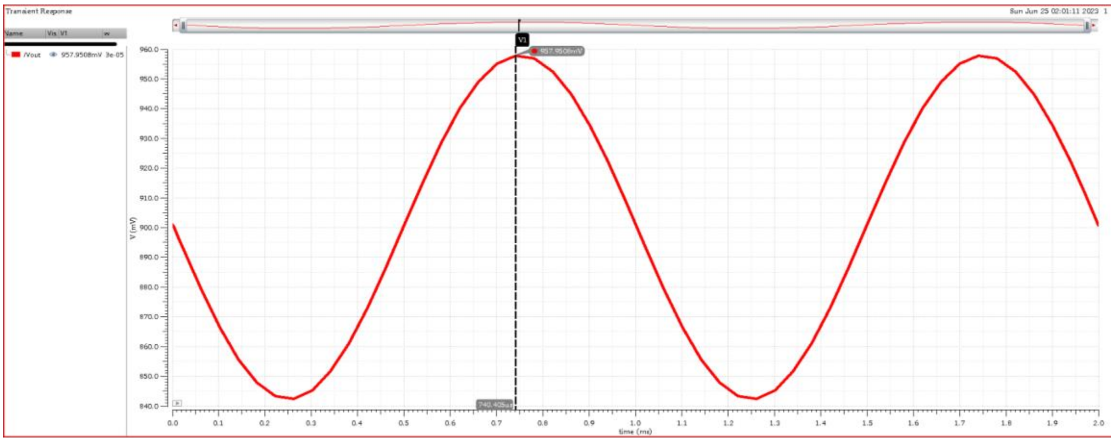


Figure 12 Vout VS Time (Transient analysis)

MAX=958m v, MIN=843m v

Gain =(MAX – MIN) / (2*Amplitude)=114/20 =5.7

gm varies with the input signal, that mean that

this amplifier isn't linear, as the linearity meaning that a change in inputs is followed by a scaled change in output without any distortion, but in the Transient analysis gm isn't linear with Vin and that mean that the gain in this case isn't linear but it could be approximately linear for the small signal at saturation region.