# Analog IC Design

# Lab 11 (Mini Project 02)

# Fully-Differential Folded Cascode OTA

## PART 1: gm/ID Design Charts

### NMOS

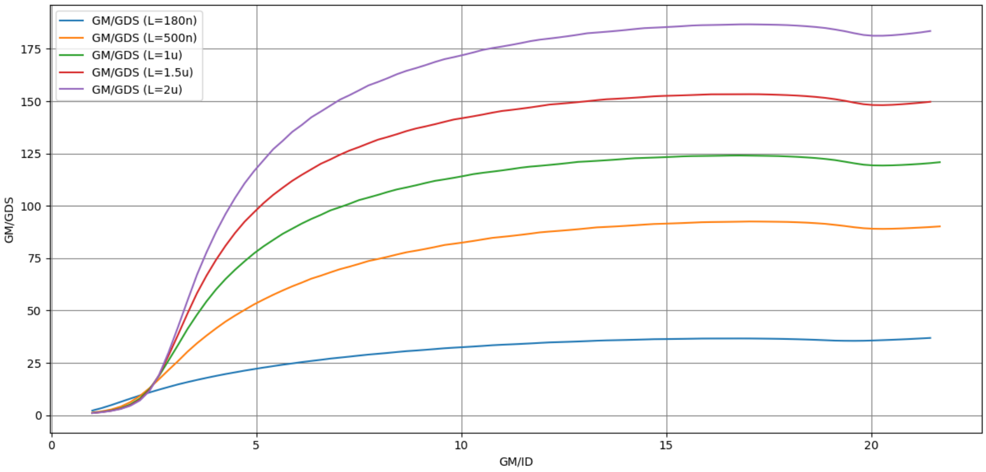



*Figure 1 NMOS GM/GDS VS GM/ID*

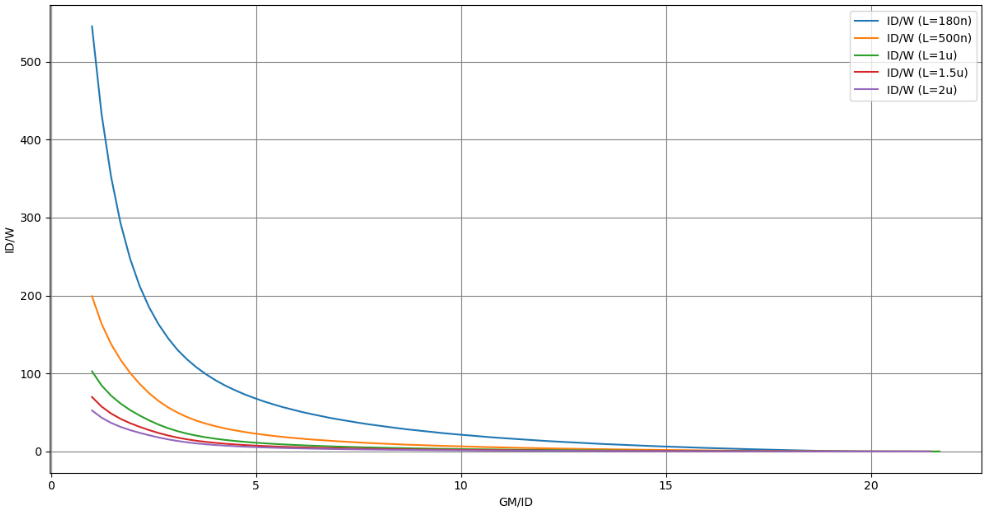



*Figure 2 NMOS ID/W VS GM/ID*

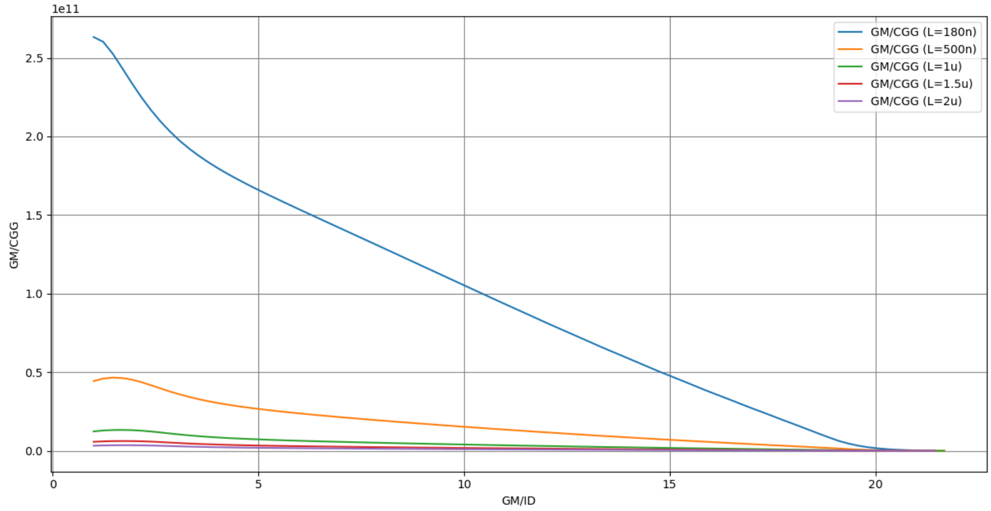



*Figure 3 NMOS GM/CGG VS GM/ID*

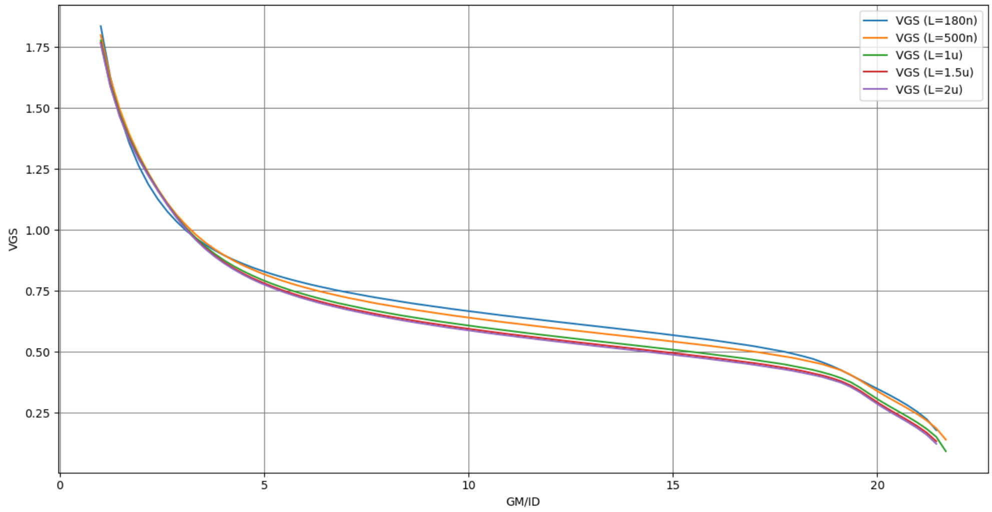



*Figure 4 NMOS VGS VS GM/ID*

## PMOS

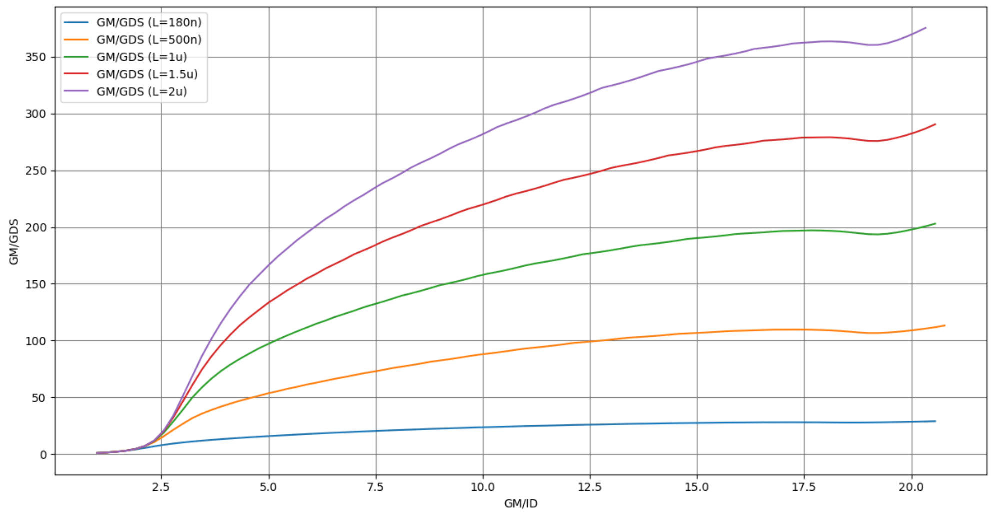



*Figure 5 PMOS GM/GDS VS GM/ID*

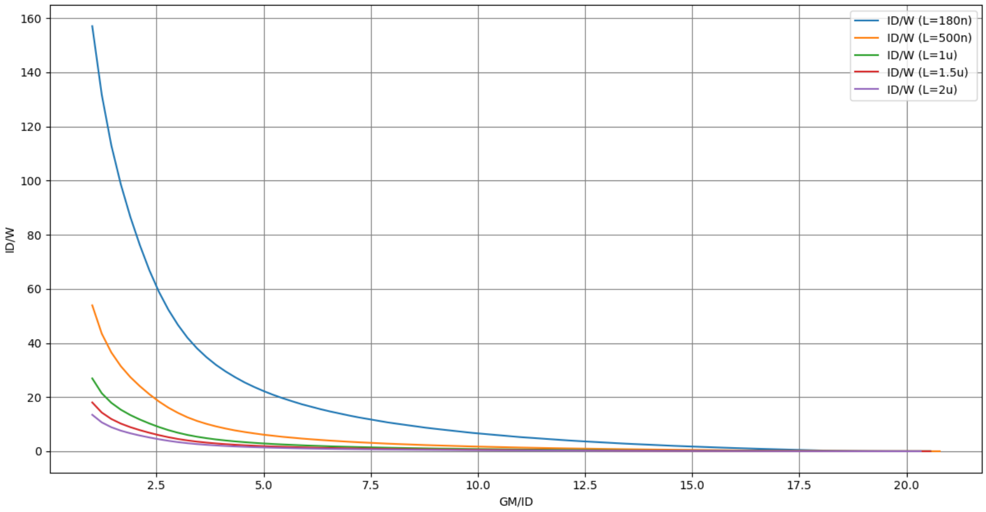



*Figure 6 PMOS ID/W VS GM/ID*

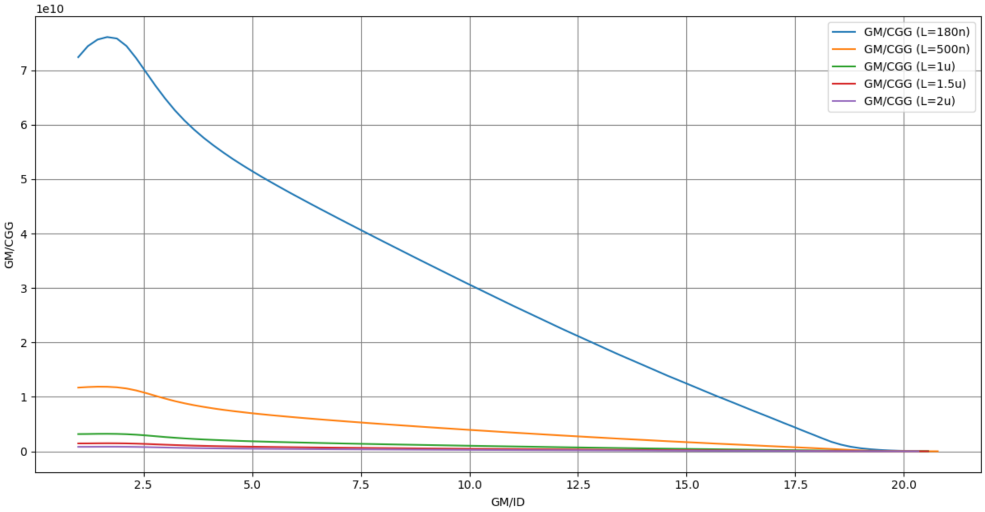



*Figure 7 PMOS GM/CGG VS GM/ID*

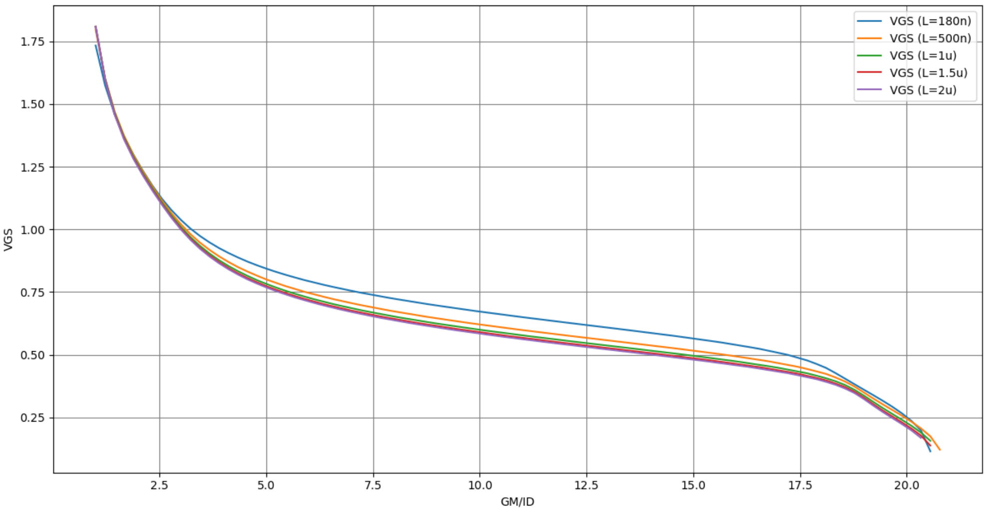
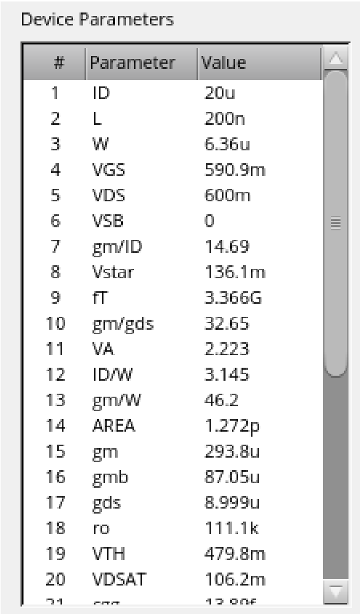



*Figure 8 PMOS VGS VS GM/ID*

**Part 2: OTA Design**

For the input pair

$VICM\_LOW = 0$ , so the input pair we will be used is PMOS.
$we\ will\ follow\ the$ Suggested Design Procedure


Device Parameters

| # | Parameter | Value |
|---|---|---|
| 1 | ID | 20u |
| 2 | L | 200n |
| 3 | W | 6.36u |
| 4 | VGS | 590.9m |
| 5 | VDS | 600m |
| 6 | VSB | 0 |
| 7 | gm/ID | 14.69 |
| 8 | Vstar | 136.1m |
| 9 | fT | 3.366G |
| 10 | gm/gds | 32.65 |
| 11 | VA | 2.223 |
| 12 | ID/W | 3.145 |
| 13 | gm/W | 46.2 |
| 14 | AREA | 1.272p |
| 15 | gm | 293.8u |
| 16 | gmb | 87.05u |
| 17 | gds | 8.999u |
| 18 | ro | 111.1k |
| 19 | VTH | 479.8m |
| 20 | VDSAT | 106.2m |

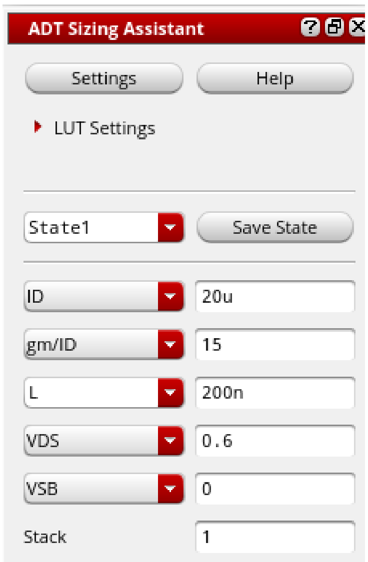
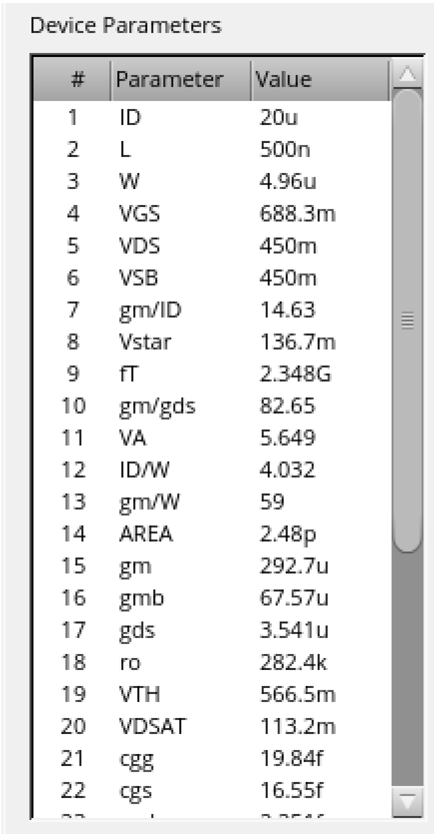



*Figure 9 input pair*


Device Parameters

| # | Parameter | Value |
|---|---|---|
| 1 | ID | 20u |
| 2 | L | 500n |
| 3 | W | 4.96u |
| 4 | VGS | 688.3m |
| 5 | VDS | 450m |
| 6 | VSB | 450m |
| 7 | gm/ID | 14.63 |
| 8 | Vstar | 136.7m |
| 9 | fT | 2.348G |
| 10 | gm/gds | 82.65 |
| 11 | VA | 5.649 |
| 12 | ID/W | 4.032 |
| 13 | gm/W | 59 |
| 14 | AREA | 2.48p |
| 15 | gm | 292.7u |
| 16 | gmb | 67.57u |
| 17 | gds | 3.541u |
| 18 | ro | 282.4k |
| 19 | VTH | 566.5m |
| 20 | VDSAT | 113.2m |
| 21 | cgg | 19.84f |
| 22 | cgs | 16.55f |

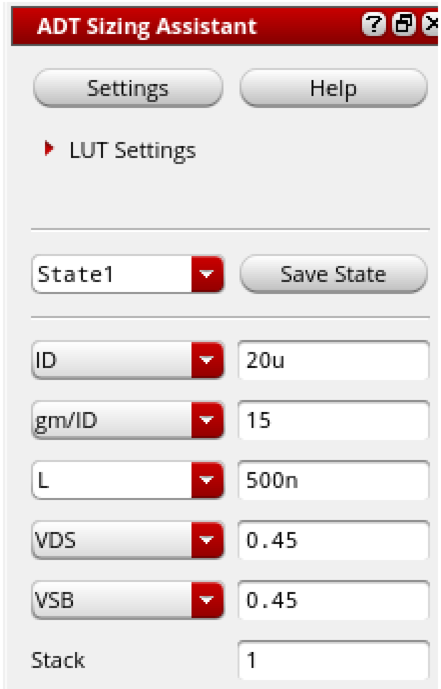
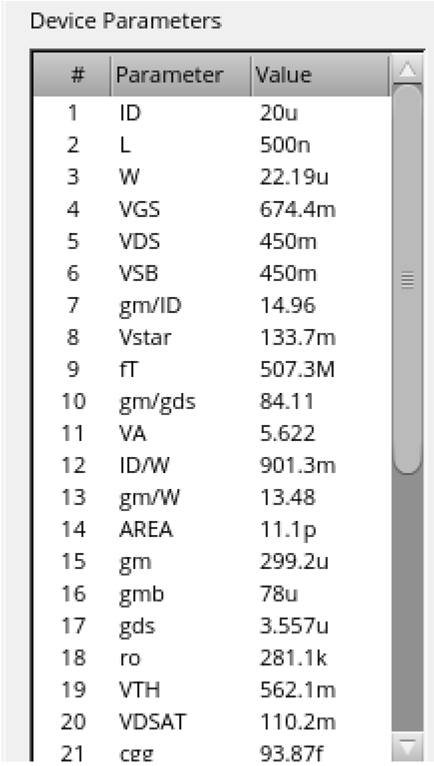



*Figure 10 Nmos Cascode*



Device Parameters

| # | Parameter | Value |
|---|---|---|
| 1 | ID | 20u |
| 2 | L | 500n |
| 3 | W | 22.19u |
| 4 | VGS | 674.4m |
| 5 | VDS | 450m |
| 6 | VSB | 450m |
| 7 | gm/ID | 14.96 |
| 8 | Vstar | 133.7m |
| 9 | fT | 507.3M |
| 10 | gm/gds | 84.11 |
| 11 | VA | 5.622 |
| 12 | ID/W | 901.3m |
| 13 | gm/W | 13.48 |
| 14 | AREA | 11.1p |
| 15 | gm | 299.2u |
| 16 | gmb | 78u |
| 17 | gds | 3.557u |
| 18 | ro | 281.1k |
| 19 | VTH | 562.1m |
| 20 | VDSAT | 110.2m |
| 21 | cgg | 93.87f |

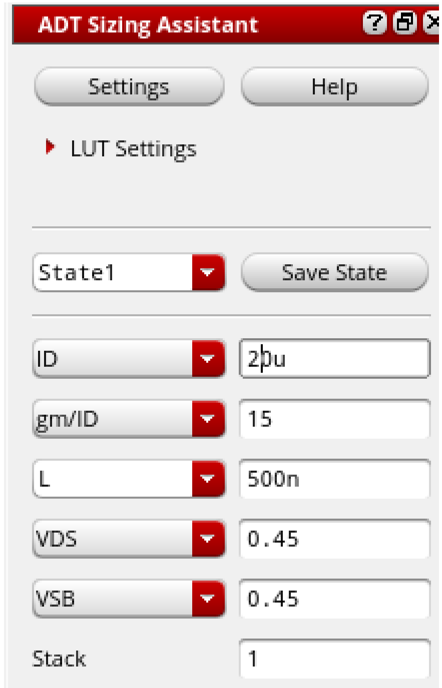
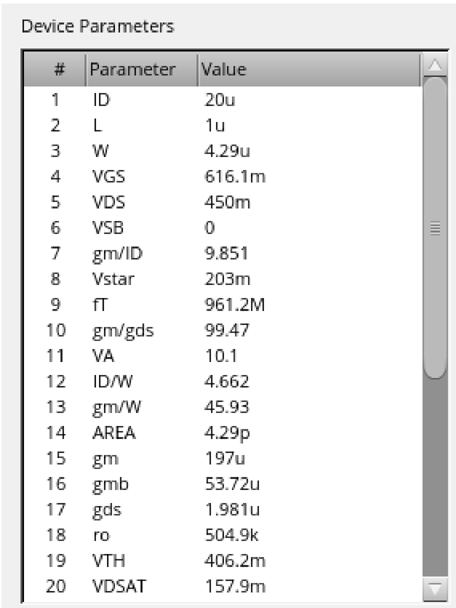



*Figure 11 Pmos Cascode*



Device Parameters

| # | Parameter | Value |
|---|---|---|
| 1 | ID | 20u |
| 2 | L | 1u |
| 3 | W | 4.29u |
| 4 | VGS | 616.1m |
| 5 | VDS | 450m |
| 6 | VSB | 0 |
| 7 | gm/ID | 9.851 |
| 8 | Vstar | 203m |
| 9 | fT | 961.2M |
| 10 | gm/gds | 99.47 |
| 11 | VA | 10.1 |
| 12 | ID/W | 4.662 |
| 13 | gm/W | 45.93 |
| 14 | AREA | 4.29p |
| 15 | gm | 197u |
| 16 | gmb | 53.72u |
| 17 | gds | 1.981u |
| 18 | ro | 504.9k |
| 19 | VTH | 406.2m |
| 20 | VDSAT | 157.9m |

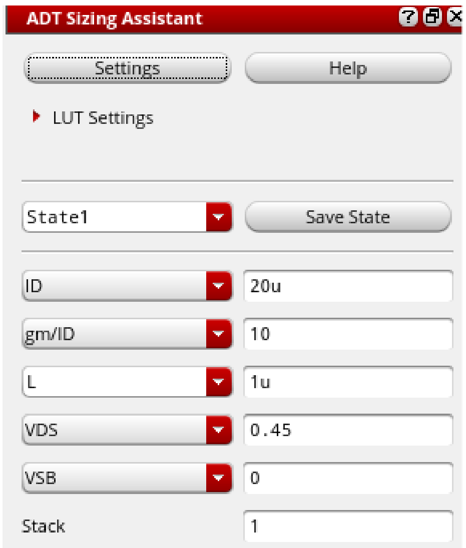
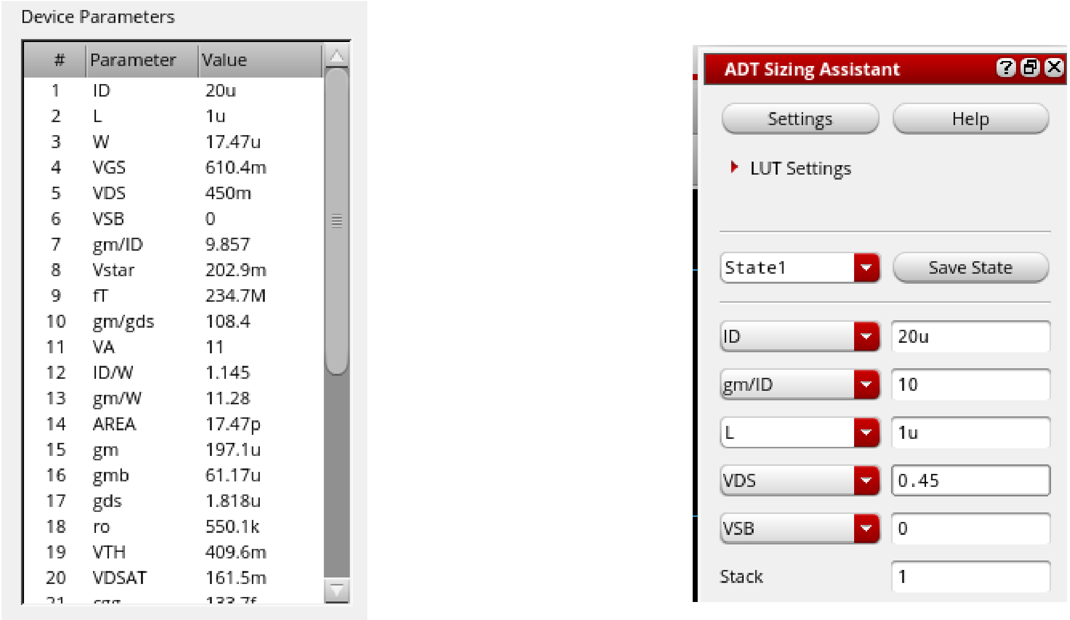



*Figure 12 Nmos current source*



Device Parameters

| # | Parameter | Value |
|---|---|---|
| 1 | ID | 20u |
| 2 | L | 1u |
| 3 | W | 17.47u |
| 4 | VGS | 610.4m |
| 5 | VDS | 450m |
| 6 | VSB | 0 |
| 7 | gm/ID | 9.857 |
| 8 | Vstar | 202.9m |
| 9 | fT | 234.7M |
| 10 | gm/gds | 108.4 |
| 11 | VA | 11 |
| 12 | ID/W | 1.145 |
| 13 | gm/W | 11.28 |
| 14 | AREA | 17.47p |
| 15 | gm | 197.1u |
| 16 | gmb | 61.17u |
| 17 | gds | 1.818u |
| 18 | ro | 550.1k |
| 19 | VTH | 409.6m |
| 20 | VDSAT | 161.5m |



*Figure 13 Pmos current source*

VCASCN ≈ VGSN + V* ≈ 688m + 203m = 791m

VCASCP ≈ VDD - |VGSP| - V* ≈ 1.8 – 674m – 203m = 923m

### PART 3: Open-Loop OTA Simulation (Behavioural CMFB)

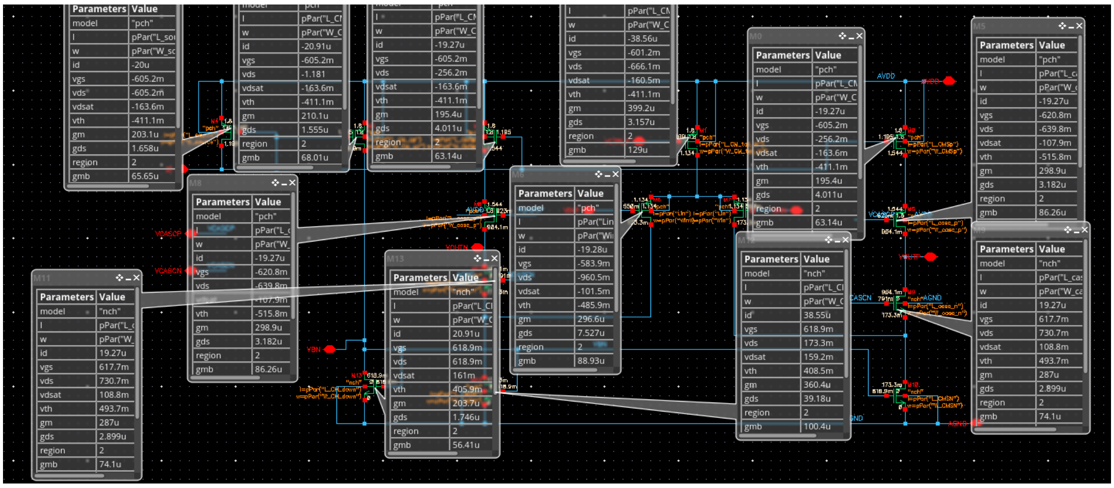


*Figure 14 OP parameters*

**What is the CM level at the OTA output?**

VOCM = 904.1 m

| | |
|---|---|
| VDC("/VOCM") | 904.1m |

**What are the differential input and output voltages of the error amplifier? What is the relation between them?**

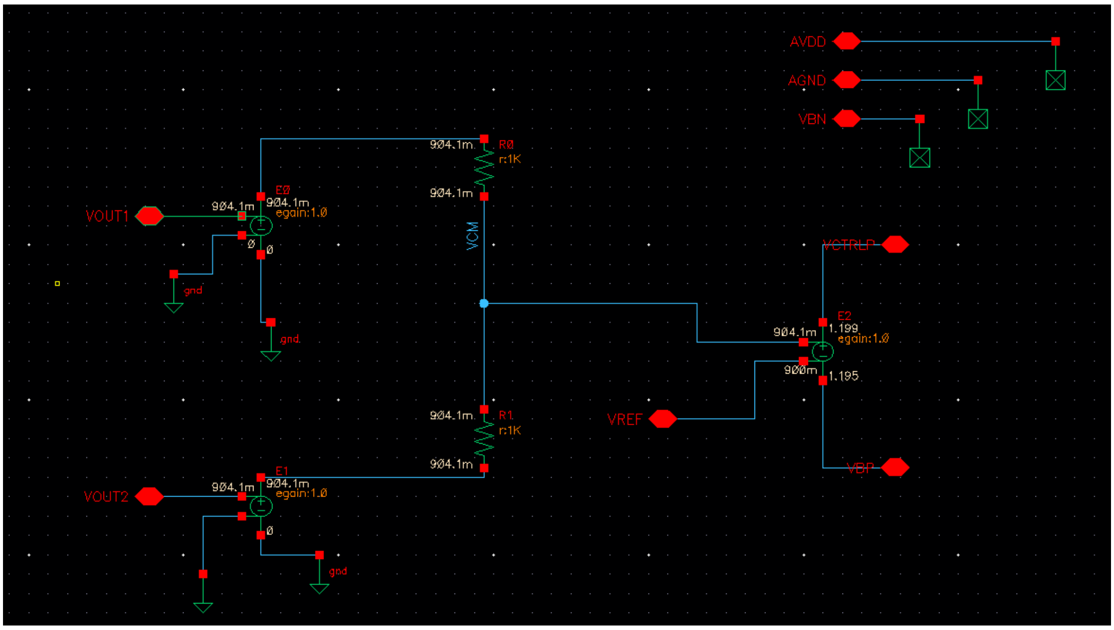



*Figure 15 error amplifier*

**VINdiff = 904.1m-900m = 0.4 mV**

**Voutdiff = 1.99-1.195 = 0.4 mV**

$$\frac{\textbf{Voutdiff}}{\textbf{VINdiff}} = 1\ , \boldsymbol{as\ it\ work\ as\ a\ buffer}$$

**2) Diff small signal ccs:**

- **Plot diff gain (magnitude in dB and phase) vs frequency.**

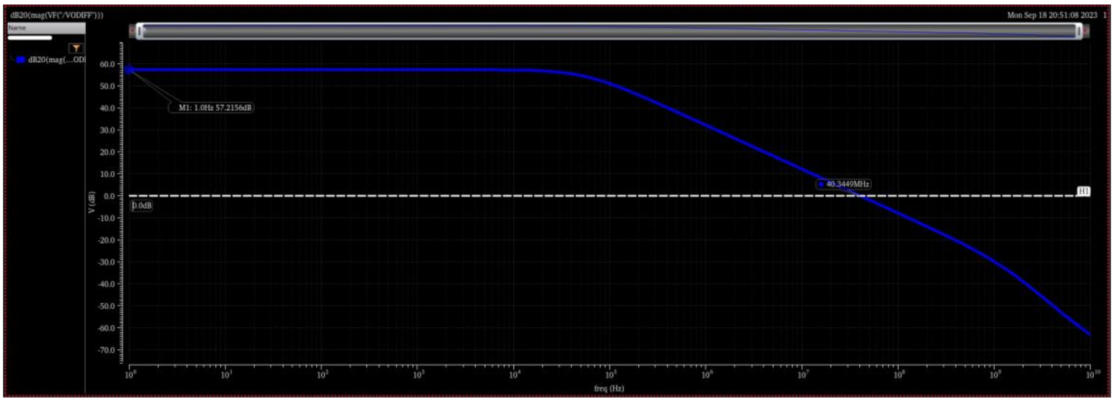



*Figure 16 diff gain (magnitude in dB) vs frequency*

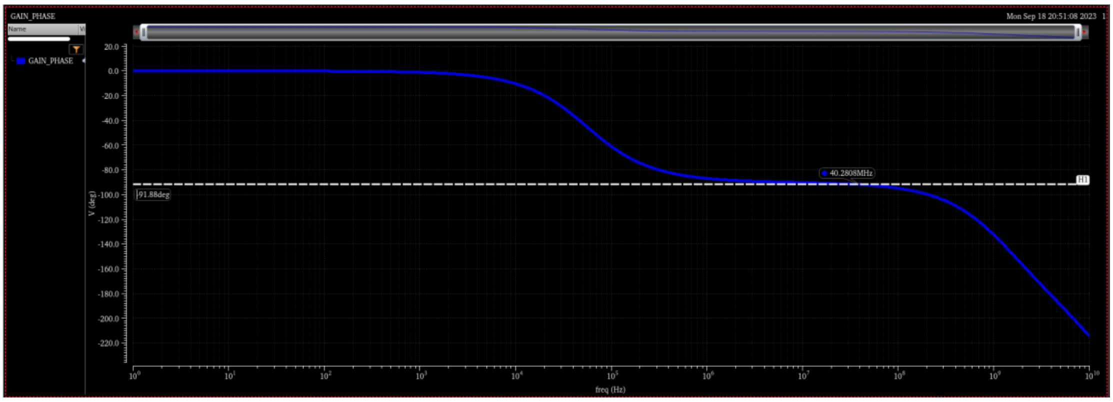



*Figure 17 diff gain (phase) vs frequency*

**• Calculate circuit parameters (DC gain, BW, GBW, UGF, and PM).**

| | | | |
|---|---|---|---|
| Ao | expr | ymax(mag(VF("/VODIFF"))) | 725.7 |
| Ao_dB | expr | dB20(ymax(mag(VF("/VODIFF")))) | 57.22 |
| BW | expr | bandwidth(VF("/VODIFF") 3 "low") | 55.59K |
| UGF | expr | unityGainFreq(VF("/VODIFF")) | 40.41M |
| GBW | expr | gainBwProd(VF("/VODIFF")) | 40.44M |
| | expr | phaseMargin(VF("/VODIFF")) | 88.12 |

*Figure 18 circuit parameters*

**• Compare simulation results with hand calculations in a table (use SS parameters from OP simulation in your hand analysis).**

$$Ao = Gm * Rout$$

$$Gm = gm_{in} = 296.6\,uS$$

$$R_{out} = RLFD_{cascN} \mid\mid RLFD_{cascP}$$

$$R_{out} = \frac{\left(1 + \frac{(gm_{cascN} + gmb_{cascN})}{gds_{folded} + gds_{input}}\right)}{gds_{cascN}} \;//\; \frac{\left(1 + \frac{(gm_{cascp} + gmb_{cascp})}{gds_{C-mirrorP}}\right)}{gds_{cascp}}$$

$$= \frac{1 + \frac{(300u + 86u)}{4u}}{3.2u} // \frac{1 + \frac{(287u + 74u)}{39u}}{2.9u} = \mathbf{30.5M // 3.54M \approx 3.17M\Omega}$$

$$A_{vd} = 296.6\,u \times 3.17M = 940V/V \approx \mathbf{59.46dB}$$

To calculate the bandwidth, we can notice that the load capacitance is much larger than the parasitic capacitances, hence we can calculate BW as follows:

$$BW \approx \frac{1}{2\pi Rout \times CL} = \frac{1}{2\pi \times 3.17M \times 1p} \approx \mathbf{50.2kHz}$$

$$GBW = A_{vd} \times BW = 940 \times \mathbf{50.2k} \approx \mathbf{47MHz}$$

$$f_u \approx GBW \approx \mathbf{497MHz}$$

$$PM = 90 - \tan^{-1}\left(\frac{GBW}{\omega_{p2}}\right)$$

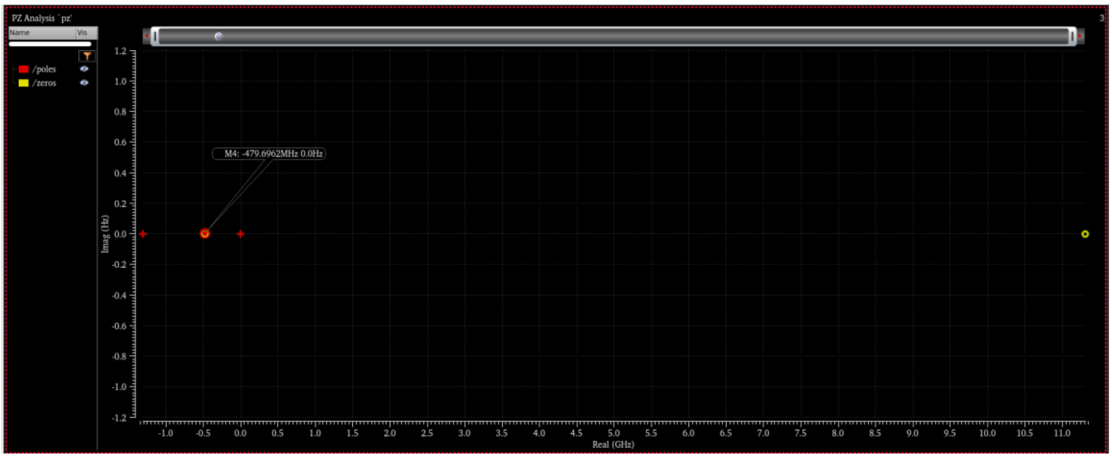



Figure 19 zeros & poles

$$PM = 90 - \tan^{-1}\left(\frac{\mathbf{47}M}{479.7M}\right) \approx \mathbf{84.39}\ \boldsymbol{deg}$$

| | Simulation | Hand analysis |
|---|---|---|
| DC _diff_gain | $\mathbf{57.22}\boldsymbol{dB}$ | $\mathbf{59.46}\boldsymbol{dB}$ |
| BW | $\mathbf{55.6}\boldsymbol{kHz}$ | $\mathbf{50.2}\boldsymbol{kHz}$ |
| GBW | $\mathbf{40.4}\boldsymbol{MHz}$ | $\mathbf{47}\boldsymbol{MHz}$ |
| UGF | $\mathbf{40.44}\boldsymbol{MHz}$ | $\mathbf{47}\boldsymbol{MHz}$ |
| PM | 88.12 | $\mathbf{84.39}\ \boldsymbol{deg}$ |

## PART 4: Open-Loop OTA Simulation (Actual CMFB)

$we\ will\ follow\ the$ Suggested Design Procedure

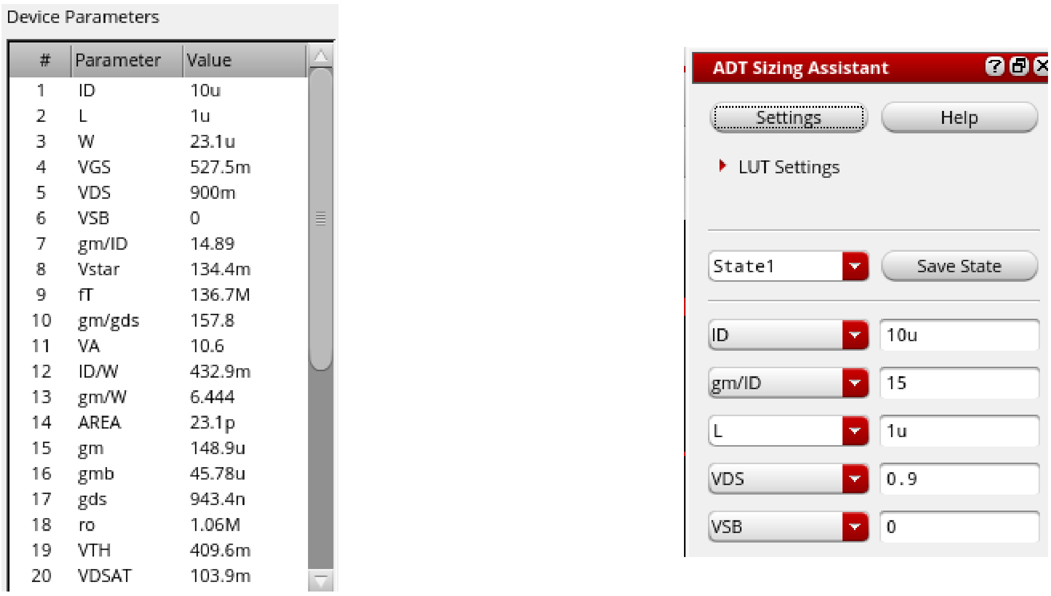



Figure 20 PMOS pair

Device Parameters

| # | Parameter | Value |
|---|---|---|
| 1 | ID | 10u |
| 2 | L | 1u |
| 3 | W | 5.61u |
| 4 | VGS | 536.8m |
| 5 | VDS | 600m |
| 6 | VSB | 0 |
| 7 | gm/ID | 14.65 |
| 8 | Vstar | 136.5m |
| 9 | fT | 565.9M |
| 10 | gm/gds | 122.8 |
| 11 | VA | 8.378 |
| 12 | ID/W | 1.783 |
| 13 | gm/W | 26.12 |
| 14 | AREA | 5.61p |
| 15 | gm | 146.5u |
| 16 | gmb | 40.7u |
| 17 | gds | 1.194u |
| 18 | ro | 837.8k |
| 19 | VTH | 405.3m |
| 20 | VDSAT | 105.6m |

| | |
|---|---|
| ID | 10u |
| gm/ID | 15 |
| L | 1u |
| VDS | 0.6 |
| VSB | 0 |
| Stack | 1 |

*Figure 21 NMOS pair*

$$\mathrm{Vout_{max}} = \mathrm{VDD} - \mathrm{VGSP} - \mathrm{V^*} = 1.8 - 620\,\mathrm{m} - 134\,\mathrm{m} = 1.046$$

$$\mathrm{Vout_{min}} = 2 * \mathrm{V^*} = 268\ \mathrm{m}$$

$$\mathrm{Vout_{cm_{avg}}} = \frac{(\mathrm{Vout_{max}} + \mathrm{Vout_{min}})}{2} = 0.657\mathrm{m}$$

VREF = $Vout\_cm\_avg + VGSP$ = 0.657m + 527.5m = 1.185

1) Schematic of the OTA and CMFB circuit with DC node voltages and transistors OP parameters (id, vgs, vds, vdsat, vth, gm, gds, region) clearly annotated.

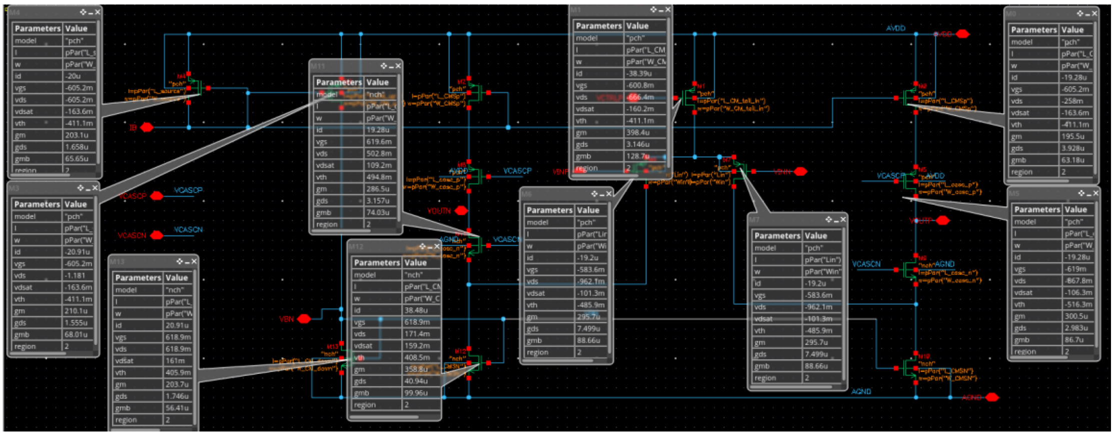


*Figure 22 transistors OP parameters*

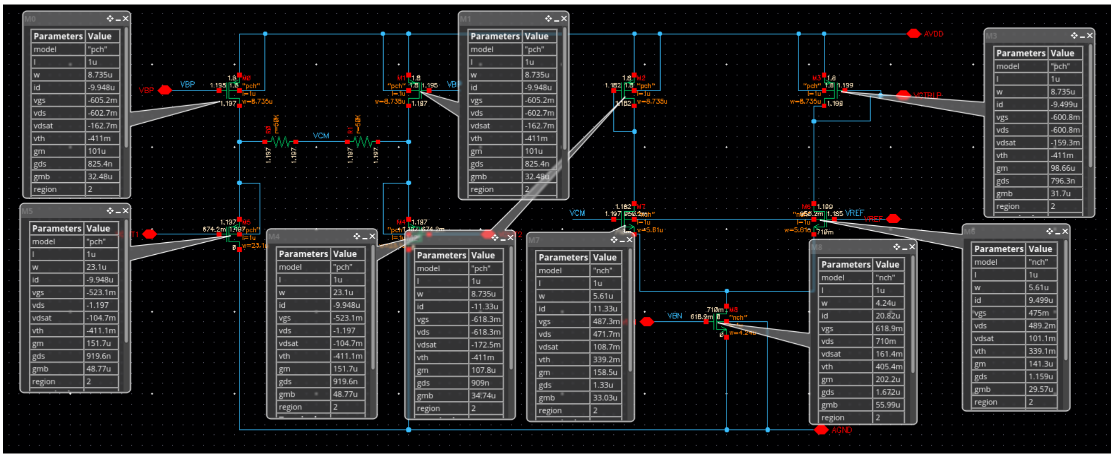


*Figure 23 transistors OP parameters*

**What is the CM level at the OTA output? Why?**

| | |
|---|---|
| VDC("/VOCM") | 674.2m |

As we designed the actual CMFB network to obtain a common mode of nearly 0.657 mV to maximize the output swing.

**What are the differential input and output voltages of the error amplifier? What is the relation between them?**

$$V_{indiff} = 1.197 - 1.185 = 12mV$$

$$V_{outdiff} = VGS_5 - VGS_2 = 1.199 - 1.182 = 17mV$$

$$\frac{V_{outdiff}}{V_{indiff}} = \frac{gm_{in} + gmb_{in}}{gm_{CM}} \approx \mathbf{1.417}$$

the gain of the error amplifier = $\frac{V_{outdiff}}{V_{indiff}}$

**2) Diff small signal ccs:**

- **Plot diff gain (magnitude in dB and phase) vs frequency.**

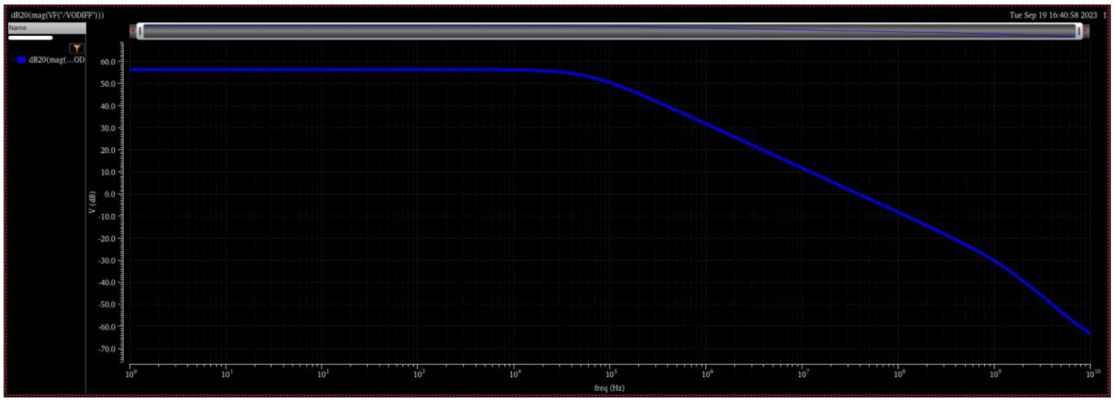


*Figure 24 diff gain (magnitude) vs frequency*

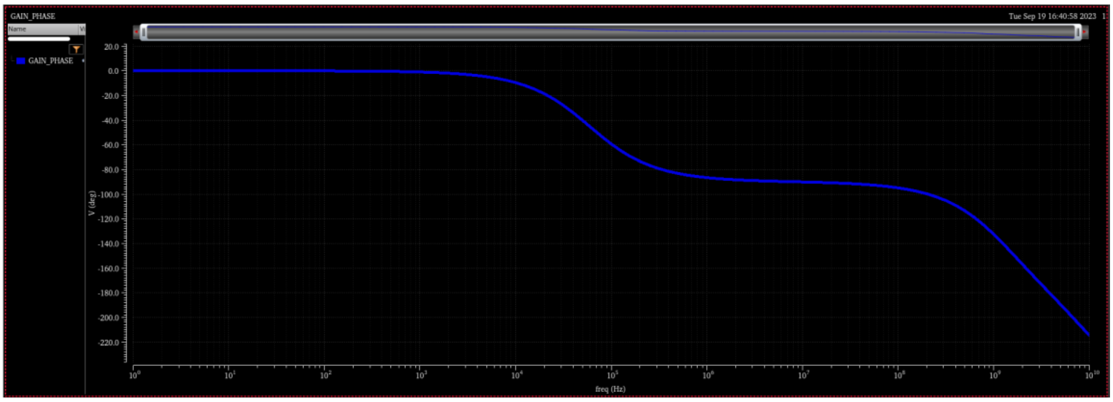


*Figure 25 diff gain (phase) vs frequency*

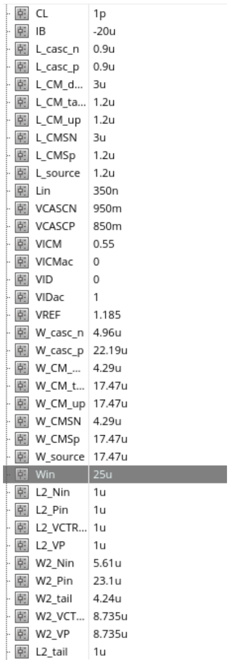
- **Calculate circuit parameters (DC gain, BW, GBW, UGF, and PM).**

| | | | |
|---|---|---|---|
| Ao | expr | ymax(mag(VF("/VODIFF"))) | 651 |
| Ao_dB | expr | dB20(ymax(mag(VF("/VODIFF")))) | 56.27 |
| BW | expr | bandwidth(VF("/VODIFF") 3 "low") | 59.47K |
| UGF | expr | unityGainFreq(VF("/VODIFF")) | 38.9M |
| GBW | expr | gainBwProd(VF("/VODIFF")) | 38.81M |
| | expr | phaseMargin(VF("/VODIFF")) | 88.15 |

*Figure 26 circuit parameters*

## PART 5: Closed Loop Simulation (AC and STB Analysis)

In part 2 we started with an initial point by assuming values for L and gm/ID for the folded cascode, in this part we change these values but keeping the same ratios for the currents and W and L based on designer's experience and trade-offs.



| | |
|---|---|
| CL | 1p |
| IB | -20u |
| L_casc_n | 0.9u |
| L_casc_p | 0.9u |
| L_CM_d... | 3u |
| L_CM_ta... | 1.2u |
| L_CM_up | 1.2u |
| L_CMSN | 3u |
| L_CMSp | 1.2u |
| L_source | 1.2u |
| Lin | 350n |
| VCASCN | 950m |
| VCASCP | 850m |
| VICM | 0.55 |
| VICMac | 0 |
| VID | 0 |
| VIDac | 1 |
| VREF | 1.185 |
| W_casc_n | 4.96u |
| W_casc_p | 22.19u |
| W_CM_... | 4.29u |
| W_CM_t... | 17.47u |
| W_CM_up | 17.47u |
| W_CMSN | 4.29u |
| W_CMSp | 17.47u |
| W_source | 17.47u |
| Win | 25u |
| L2_Nin | 1u |
| L2_Pin | 1u |
| L2_VCTR... | 1u |
| L2_VP | 1u |
| W2_Nin | 5.61u |
| W2_Pin | 23.1u |
| W2_tail | 4.24u |
| W2_VCT... | 8.735u |
| W2_VP | 8.735u |
| L2_tail | 1u |

*Figure 27 final Tunning Results*

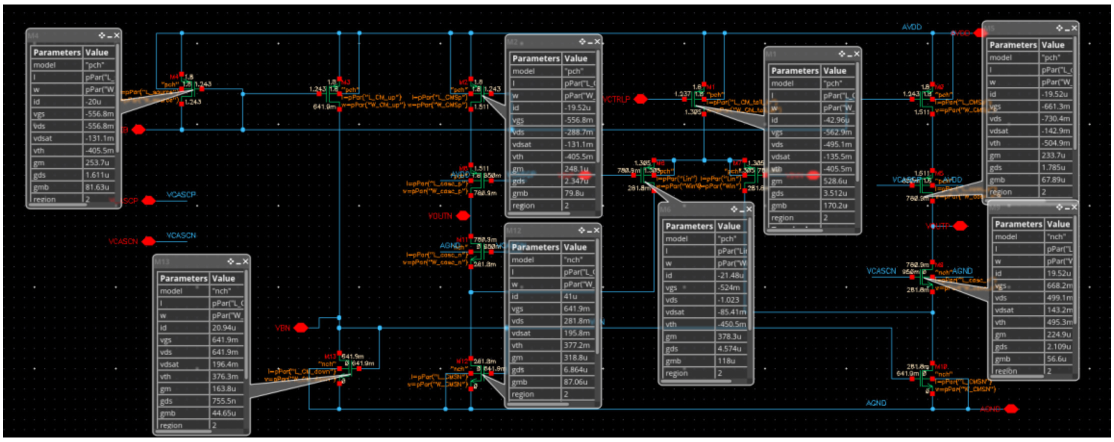


*Figure 28 OTA*

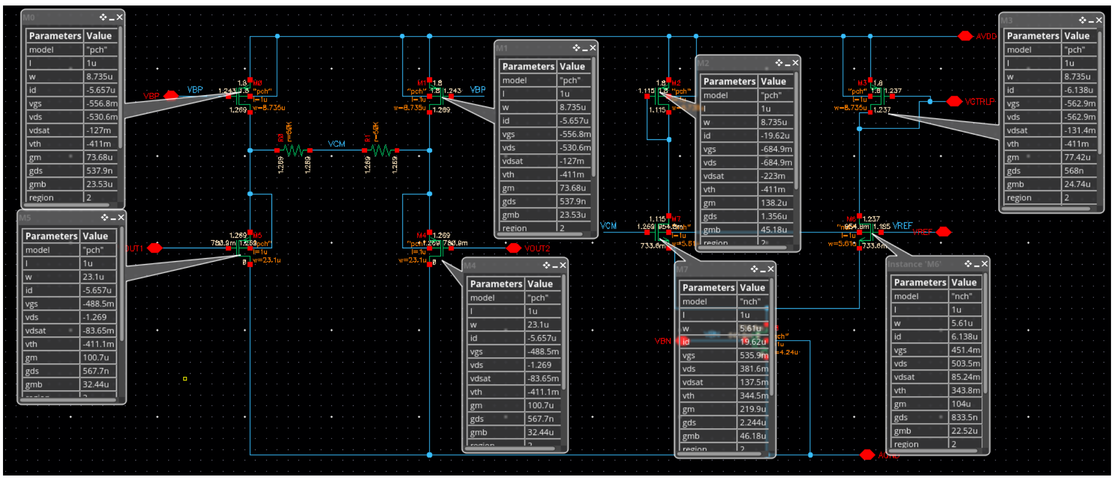


*Figure 29 CMFB circuit*

the CM level at the OTA output = 781m

| | | | |
|---|---|---|---|
| VOCM | expr | VDC("/VOCM") | 780.9m |

As we designed the actual CMFB network to obtain a common mode of nearly $0.657$ mV to maximize the output swing. But because of the limited gain the CMFB network will not be so accurate.

the CM level at the OTA input =781m

| | | | |
|---|---|---|---|
| VICM | expr | ((VDC("/VFBP") + VDC("/VFBN")) / 2) | 780.9m |

It is same as the CM level at the OTA output because the feedback connection is a large resistor which make the input and output voltage equal.

**2) Differential closed-loop response:**

**• Plot VODIFF vs frequency**

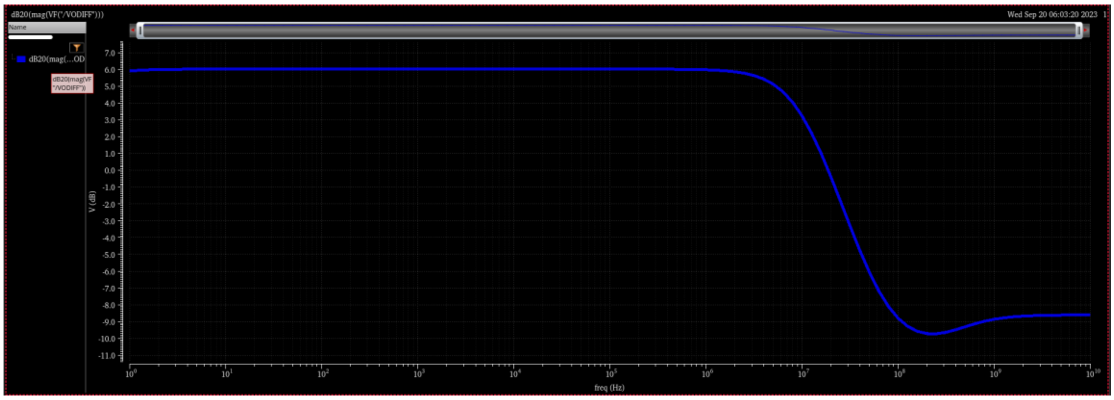



*Figure 30 VODIFF vs frequency*

**• Use Measures or cursors to calculate circuit parameters (DC gain, CL BW, CL GBW)**

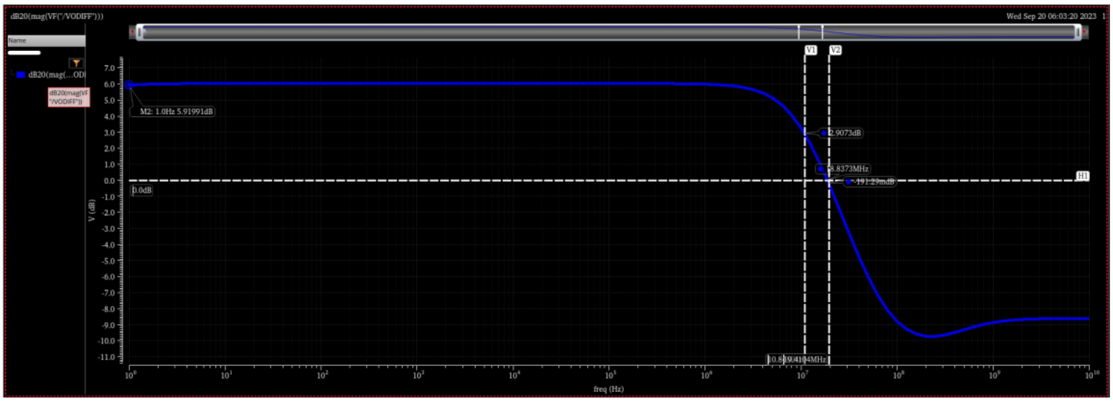



*Figure 31 circuit parameters*

| | | | |
|---|---|---|---|
| Ao | expr | ymax(mag(VF("/VODIFF"))) | 1.998 |
| Ao_dB | expr | dB20(ymax(mag(VF("/VODIFF")))) | 6.014 |
| BW | expr | bandwidth(VF("/VODIFF") 3 "low") | 12.17M |
| UGF | expr | unityGainFreq(VF("/VODIFF")) | 21.9M |
| GBW | expr | gainBwProd(VF("/VODIFF")) | 24.08M |
| | expr | phaseMargin(VF("/VODIFF")) | 94.63 |

*Figure 32 Measures*

**3) Differential and CMFB loops stability (STB analysis):**

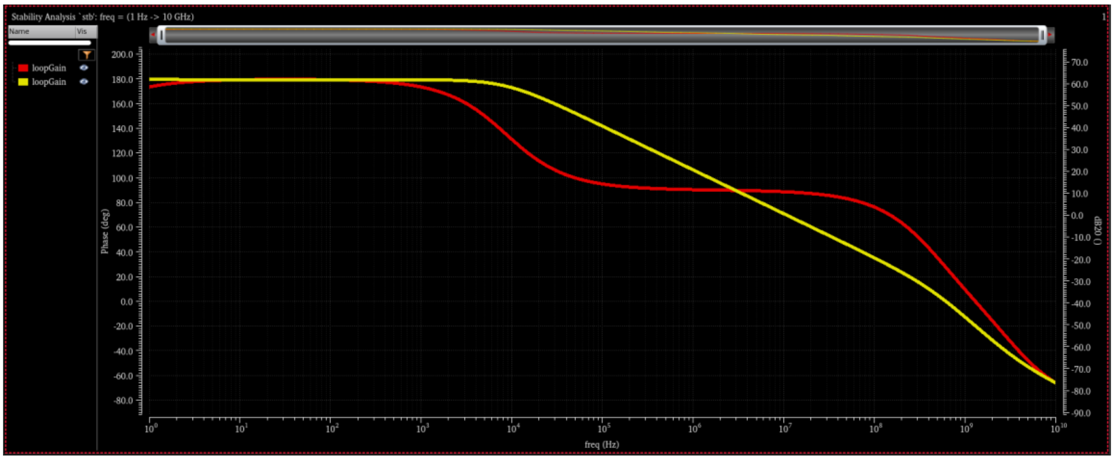



*Figure 33 DIFF LG in dB & phase vs frequency overlaid*

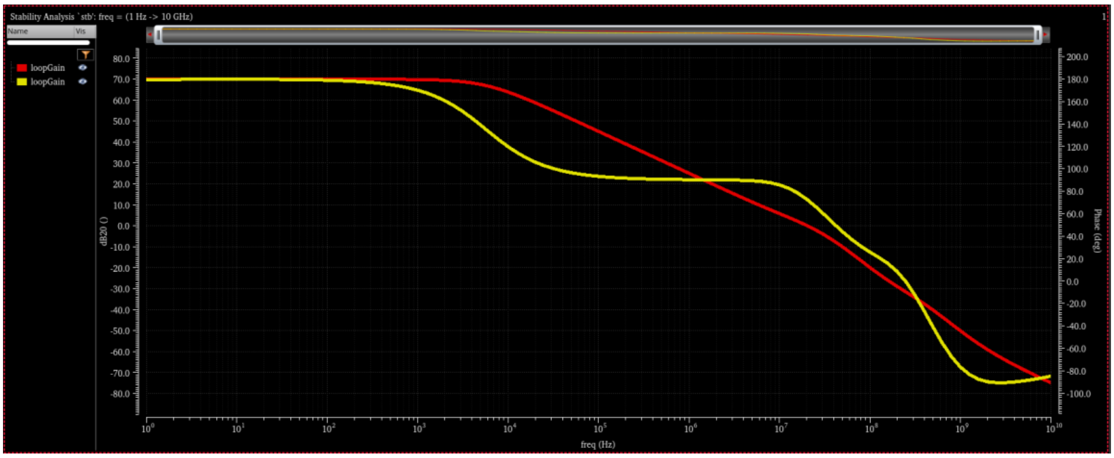



*Figure 34 CM LG in dB & phase vs frequency overlaid*

- **Compare GBW and PM of diff and CM loops. Comment.**

| | | | |
|---|---|---|---|
| LG_dB | expr | dB20(ymax(mag(getData("loopGain" ?result "stb")))) | 62.08 |
| GBW_LG | expr | gainBwProd(mag(getData("loopGain" ?result "stb"))) | 10.88M |
| BW_LG | expr | bandwidth(mag(getData("loopGain" ?result "stb")) 3 "low") | 8.536K |
| | expr | unityGainFreq(getData("loopGain" ?result "stb")) | 11.11M |

*Figure 35 DIFF Mode*

phaseMargin(deg)=88.529821

| | | | |
|---|---|---|---|
| LG_dB | expr | dB20(ymax(mag(getData("loopGain" ?result "stb")))) | 69.91 |
| GBW_LG | expr | gainBwProd(mag(getData("loopGain" ?result "stb"))) | 17.99M |
| BW_LG | expr | bandwidth(mag(getData("loopGain" ?result "stb")) 3 "low") | 5.734K |
| | expr | unityGainFreq(getData("loopGain" ?result "stb")) | 20.56M |

*Figure 36 CM*

phaseMargin(deg)=72.366094

| | DIFF | CM |
|---|---|---|
| **GBW** | **10.88M** | **20.56M** |
| **PM** | **91 deg** | **72 deg** |

We notice that CM GBW is higher than DIFF GBW which means faster effect.

- **Compare DC LG and GBW of the diff loop with those obtained from open-loop simulation.**

| | | | |
|---|---|---|---|
| LG_dB | expr | dB20(ymax(mag(getData("loopGain" ?result "stb")))) | 73.24 |
| GBW_LG | expr | gainBwProd(mag(getData("loopGain" ?result "stb"))) | 39.78M |
| BW_LG | expr | bandwidth(mag(getData("loopGain" ?result "stb")) 3 "low") | 8.643K |
| | expr | unityGainFreq(getData("loopGain" ?result "stb")) | 37.24M |

*Figure 37 open-loop simulation*

| | diff loop | open-loop |
|---|---|---|
| **GBW** | **10.88M** | **39.78M** |
| **DC_LG** | **62 dB** | **73.24 dB** |

**Comment**

$$\textbf{open} - \textbf{loop DC} + \textbf{20}\log\left(\frac{1}{3}\right) = \textbf{73} - \textbf{9.5} = \textbf{63.5 dB} \approx \textbf{diff loop}$$

$$\textbf{open} - \textbf{loop GBW} * \frac{1}{3} = \textbf{13} \approx \textbf{diff GBW}$$

The error Because the feedback factor $\beta \approx \frac{1}{3}$ but not exactly equal it as we didn't add the parasitic capacitance in our calculations or the the loading effect of the feedback**.**

## PART 6: Closed Loop Simulation (Transient Analysis)

### 1) Differential and CMFB loops stability (transient analysis):

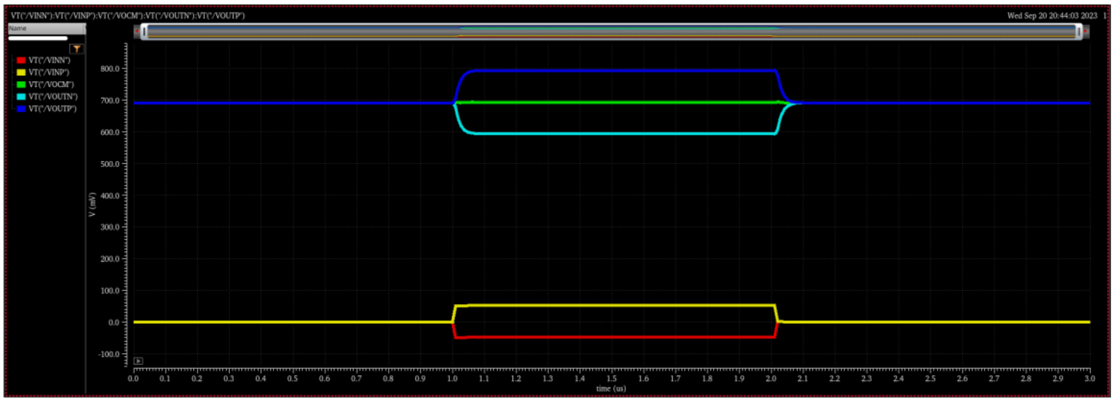



*Figure 38 transient signals DIFF*

The differential outputs have no ringing because its phase margin is 91 which means that the system is overdamped that is meaning that it is slow but also it is a stable system so it has an adequate PM and no ringing.

The CM output has a small ringing as its phase margin is 72 which means that the system is underdamped so it hasn't an adequate PM and it should be higher but it's a stable system.

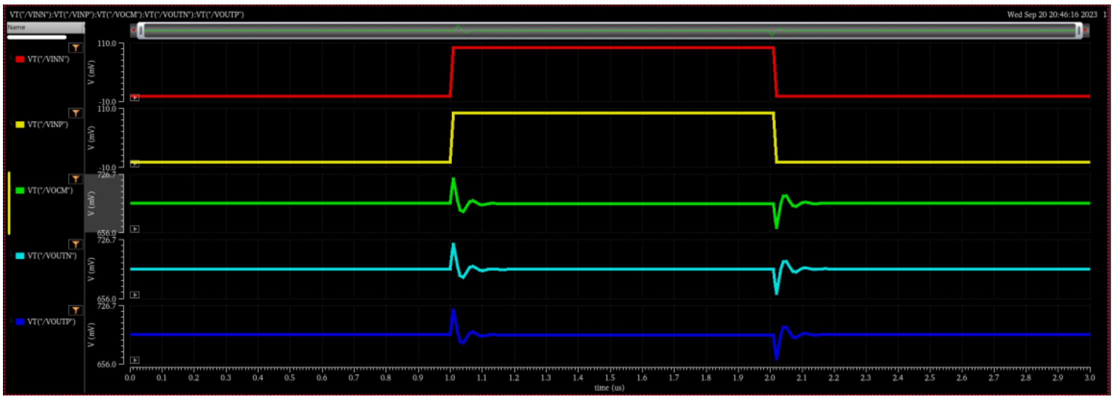


Figure 39 transient signals CM

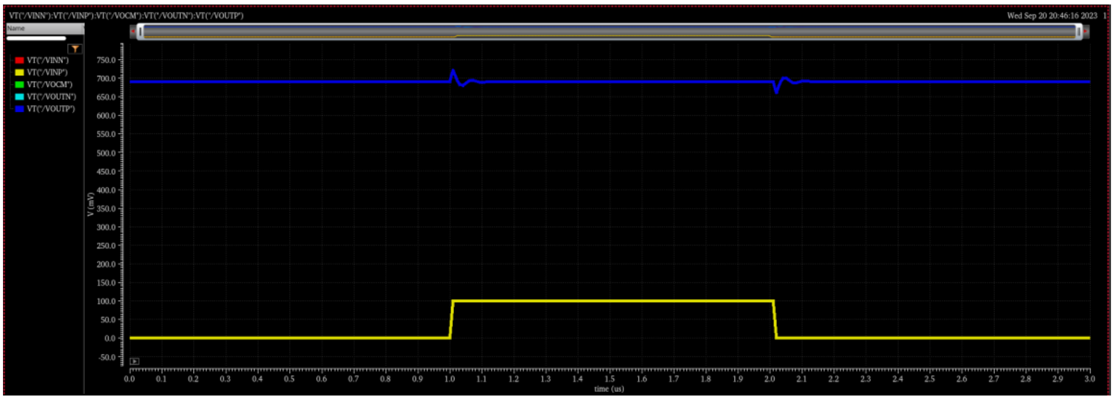


Figure 40 transient signals CM overloaded

The CM output has a small ringing as its phase margin is 72 which means that the system is underdamped so it hasn't an adequate PM and it should be higher but it's a stable system.

We mentioned above that the diff mode has adequate PM, but Common mode hasn't, so it is appeared that in the differential output there is no ringing as the signals have the same values and sign.

The system is stable, and the effect of the ringing isn't considered as it is in the Common mode, but there is no ringing in the Diff mode.

**2) Output swing:**

**• Plot the transient signals at VINP, VINN, VOUTP, VOUTN, and VOCM overlaid in the same figure.**

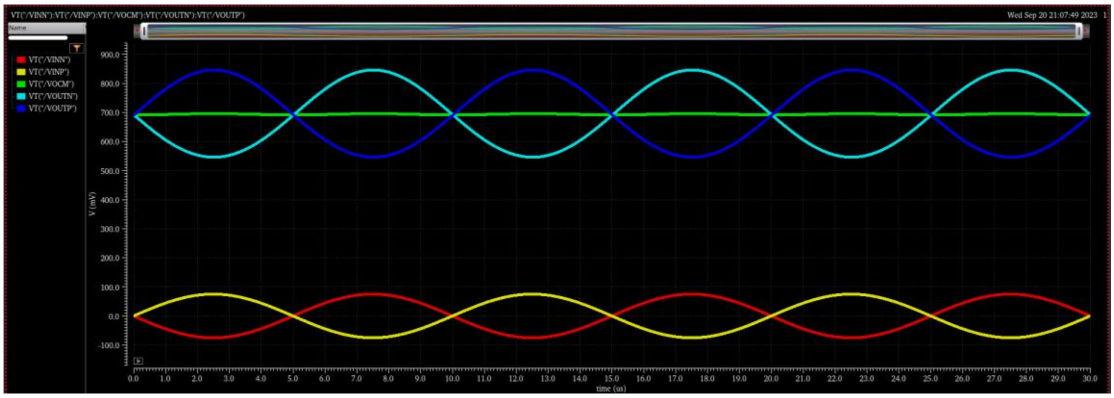


Figure 41 transient signals

**• Plot the transient signals at VIDIFF and VODIFF overlaid in the same figure.**

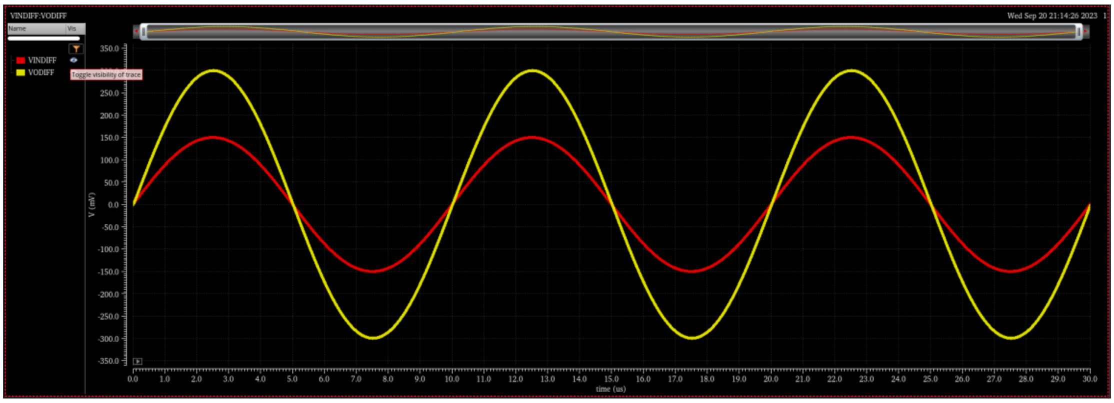



*Figure 42 VIDIFF and VODIFF overlaid.*

**• Calculate the diff input and output peak-to-peak swings and the closed loop gain.**

| | | | |
|---|---|---|---|
| PP_VIDIFF | expr | peakToPeak(VT("/net3")) | 300m |
| PP_VODIFF | expr | peakToPeak(VT("/VODIFF")) | 599.2m |
| Ao_CL | expr | (peakToPeak(VT("/VODIFF")) / peakToPeak(VT("/net3"))) | 1.997 |

**output peak-to-peak swings = 300m**

**input peak-to-peak swings =600m**

**closed loop gain = 2**