Analog IC Design – Cadence Tools & SA

Lab 05

Simple vs Wide Swing (Low Compliance) Cascode Current Mirror

Part 1: Exploring Sizing Trade-offs Using SA

Answer the following:

2) The % Change in current translates to a spec on the $\lambda = 1/VA$ of the device. How much is the required λ?

$$I_D = \beta V_{OV}^2(1 + \lambda V_{DS}) = \beta V_{OV}^2(1 + \lambda V_{OUT})$$

$$\Delta I_D = \beta V_{OV}^2 \, \lambda \, \Delta V_{OUT}$$

$$\frac{\Delta I_D}{I_D} = \frac{\lambda \Delta V_{OUT}}{1 + \lambda V_{OUT}} \approx \lambda \Delta V_{OUT} \;\; \rightarrow \;\; \lambda = 0.1$$

3) Sinking current means which device type? NMOS or PMOS?

The device type is NMOS.

4) The higher the gm/ID (the lower the $V*$) the higher the headroom (the available swing), but the larger the area. Examine this trade-off using SA as shown below. Report L and W vs Vstar.

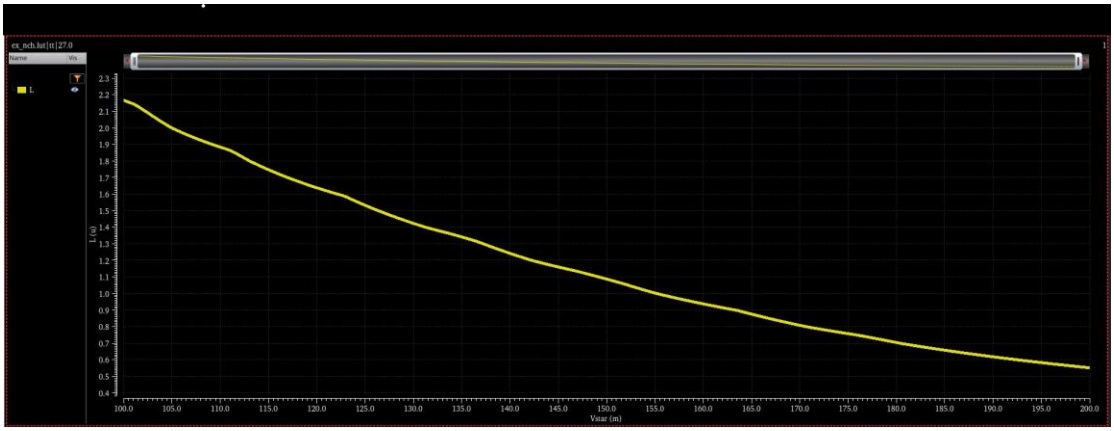


Figure 1 L VS Vstar

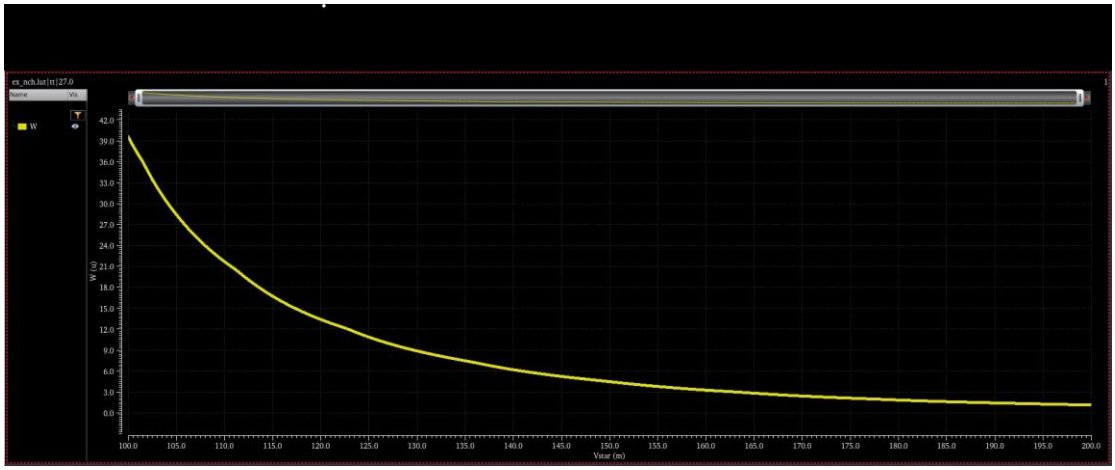


Figure 2 W VS Vstar

6)

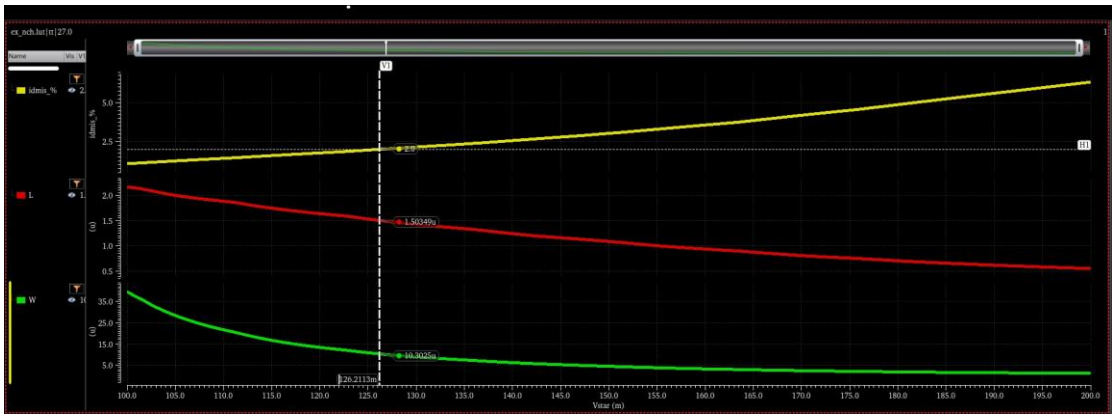


Figure 3 a bias point (Vstar) that gives idmis < 5%

idmis = 2%, $V^* = 126.2113mV$

W = 10.3u

L = 1.5u

7) Can we do the previous design trade-offs exploration sweeps using a standard SPICE simulator, i.e., sweep Vstar at a constant λ? Why?

NO, as We cannot guarantee the stability of all parameters in the emulator, and if we change one of the parameters to suit the design, another may change in a way that does not suit it. The goal is for all parameters to be in the allowed range with all changes $\boldsymbol{\lambda}$ is a parameter of the state on which the transistor is located, so this can be applied to it.

Part 2: Current Mirror Simulation

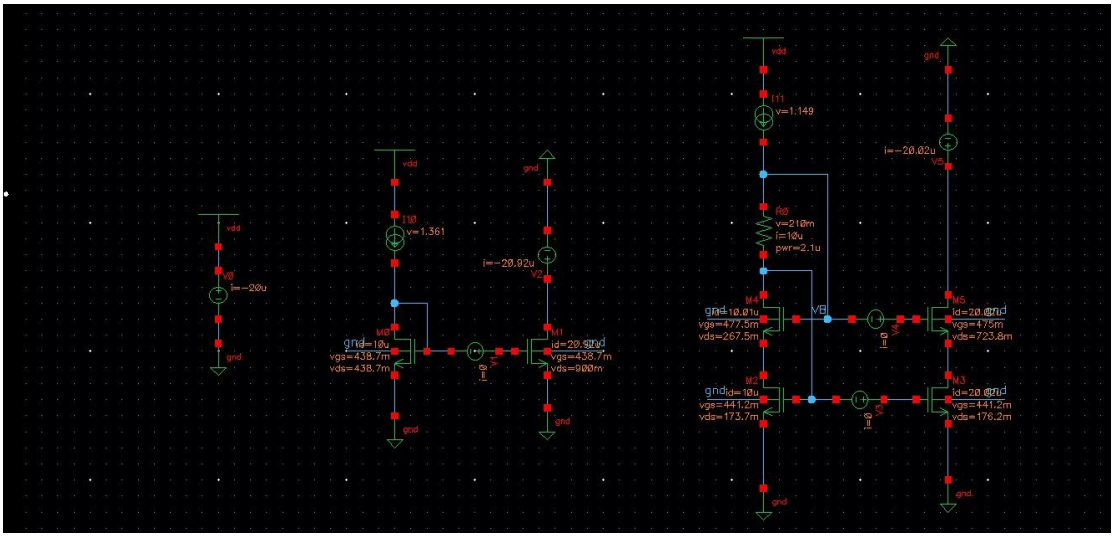


Figure 4 schematic

1. **Design and OP (Operating Point) Analysis**

   1) calculate a rough value for RB $= \frac{V_{ds3}}{I_B} = 17.6\ K\Omega$

   2)

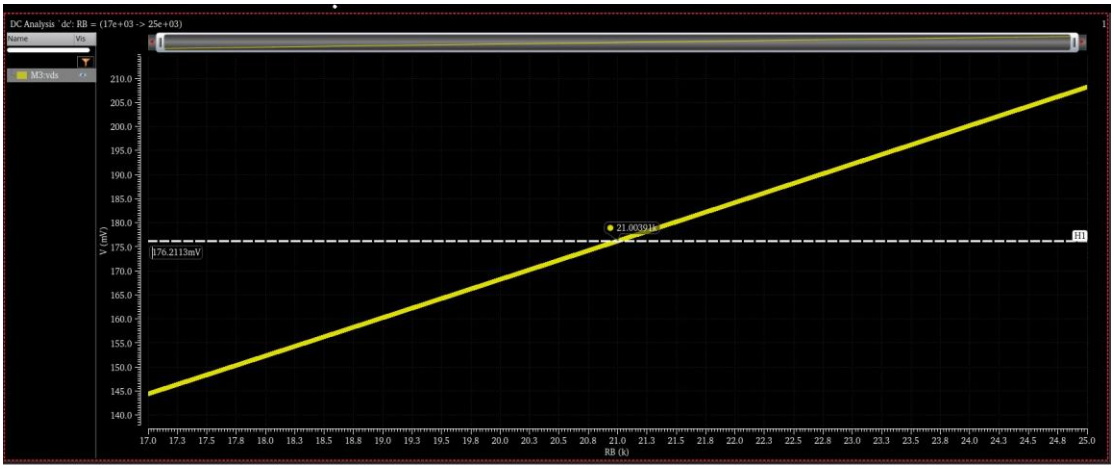


Figure 5 $VDS3$ vs Rb

Is the selected RB value larger or smaller than the rough analytical value? Why?

Larger, Because we ignored the body effect in the analytical calculation which causes Vth to be changed from the simulation value so Vgs will be effected by Vth and RB will be larger than the analytical value.

3)

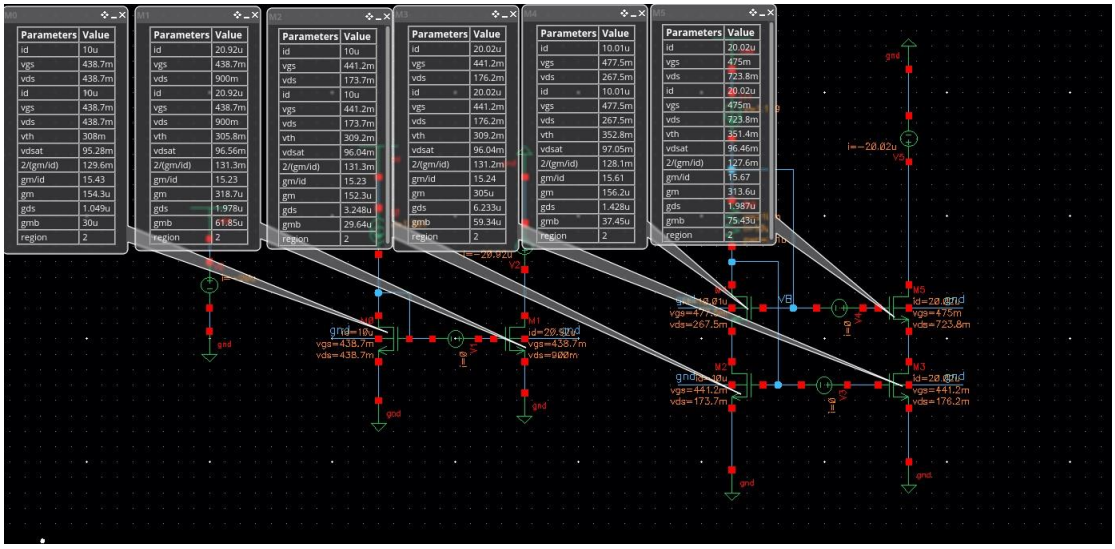


Figure 6 the OP point

4) Do all transistors operate in saturation?

YES.

2. DC Sweep ($Iout$ vs VOUT)

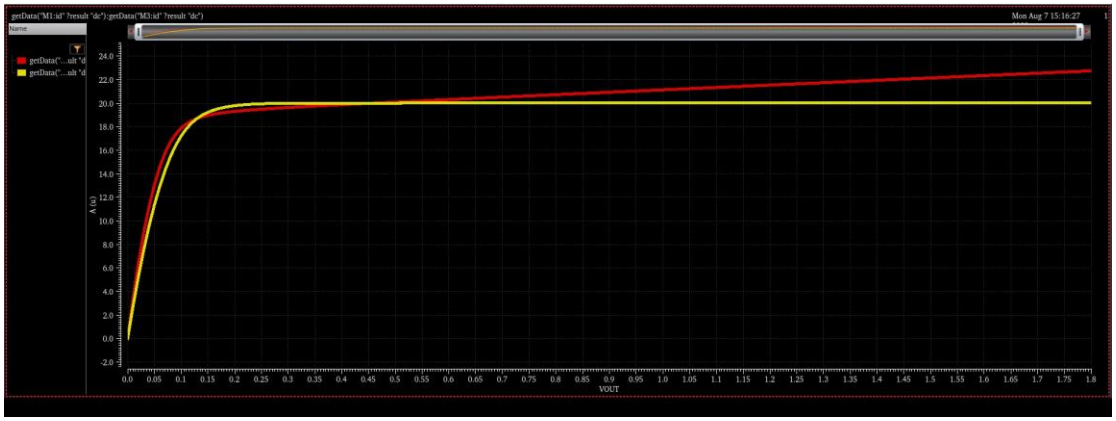


Figure 7 $Iout$ vs VOUT

o Comment on the difference between the two circuits.

the first circuit is the simple CS Which hasn't the same Vds for the two transistor M0 ,M1 that make little variation in the output current and the curve in the saturation region will be proportional to Vout, Unlike the wide swing one Which has the same Vds for the two transistor M2 ,M3 that make the slope of the curve constant in the saturation region.

o From the plot, find an estimate for the compliance voltage of each current mirror.

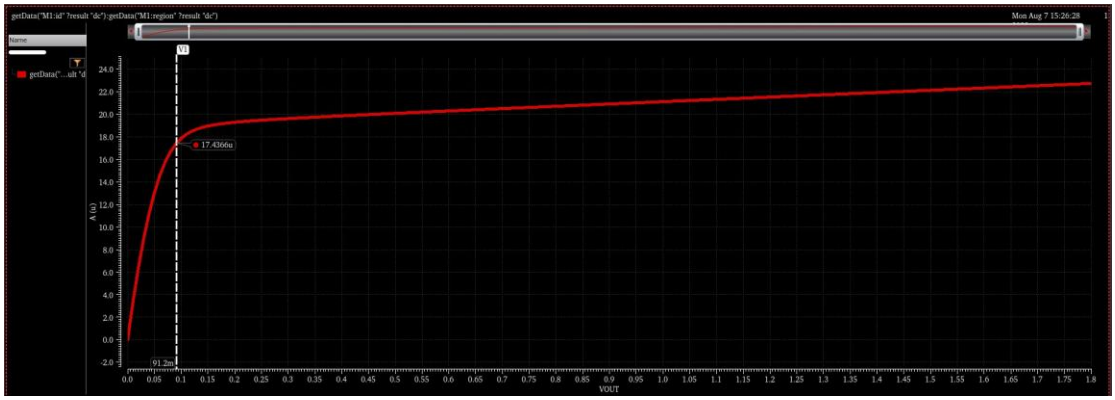


Figure 8 the compliance voltage of I1

the compliance voltage for simple CS = 91.2m

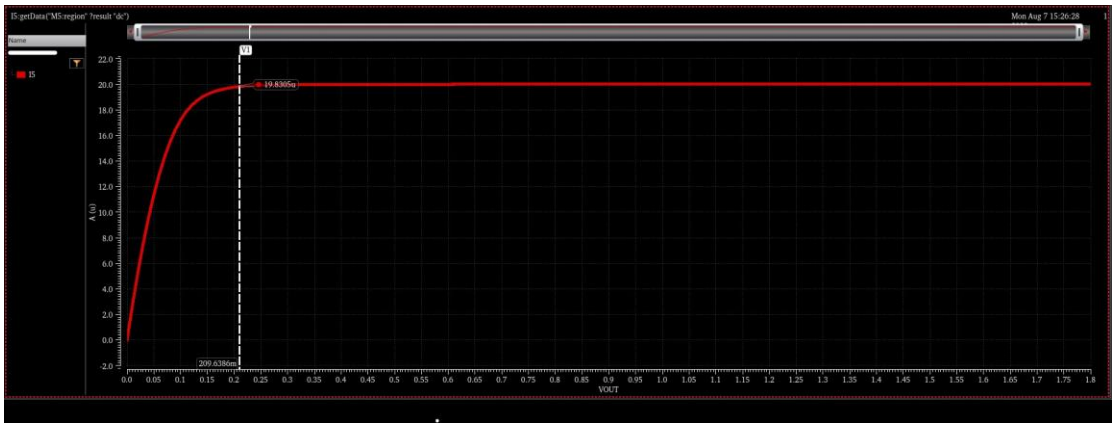
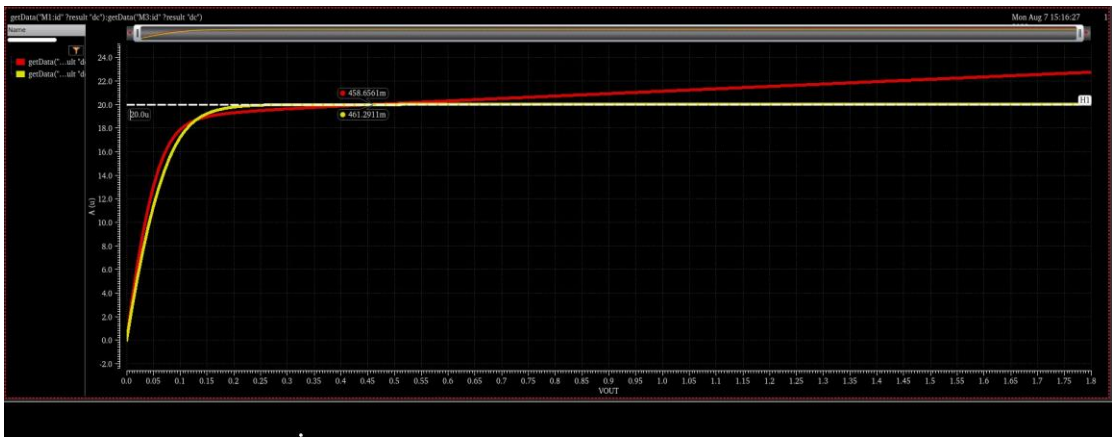


Figure 9 the compliance voltage of I2

the compliance voltage for wide swing (cascode) CS =209.6m

o $Iout$ of the simple CM is exactly equal to IB*2 at a specific value of VOUT. Why?



for simple CS = 458.7m

for wide swing (cascode) CS = 461.3m

Because the current mirror act as a perfect current mirror when Vds of the two transistors of the mirror become the same.

2) **For the simple current mirror, calculate the percent change in $Iout$ when VOUT changes from 0.5V to 1.5V (i.e., 1V change). Compare the result to the value expected from Part 1.**

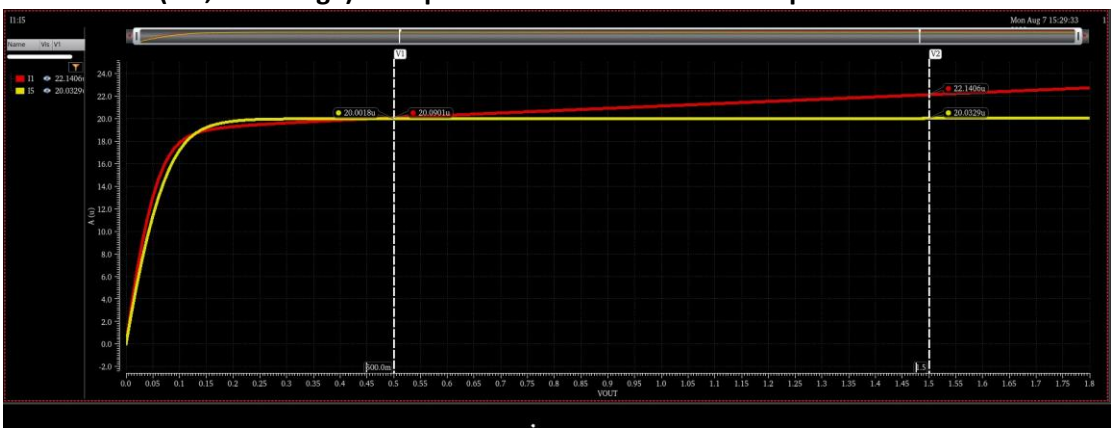


Figure 10 VOUT changes from 0.5V to 1.5V

the percent change = 10%

The Change in Current (**Δ**ID) for Change in the output Voltage $\boldsymbol{\Delta Vout}$ = 1V < 10% from part 1.

3) **Report the percent of error in $Iout$ vs VOUT (ideal $Iout$ should be IB*2) for the two CMs in the current mirror operating region (VOUT ≈ V ∗ to VDD) overlaid in the same plot.**

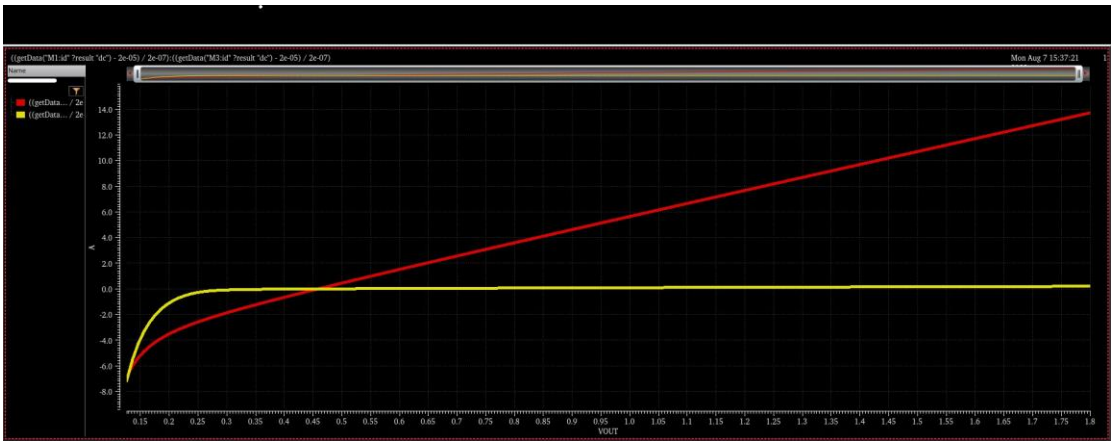


Figure 11 the percent of error in $Iout$ vs VOUT

o Comment on the difference between the two circuits.

The wide-swing current mirror has no affects by Vds compared with the simple CS current mirror, so it has better efficiency than the simple current mirror so the error in the wide-swing is less than the simple current mirror, and as the wide-swing current mirror act as cascode, so it has more Rout, and error almost equal zero, as M4&M5 make V_{DS} on M2&M3 equal.

4) **Report Rout vs VOUT (take the inverse of the derivative of $Iout$ plot) for the two CMs in the current mirror operating region (VOUT ≈ V ∗ to VDD) overlaid in the same plot. Use log scale on the y-axis. Add a cursor at VOUT = VDD/2.**

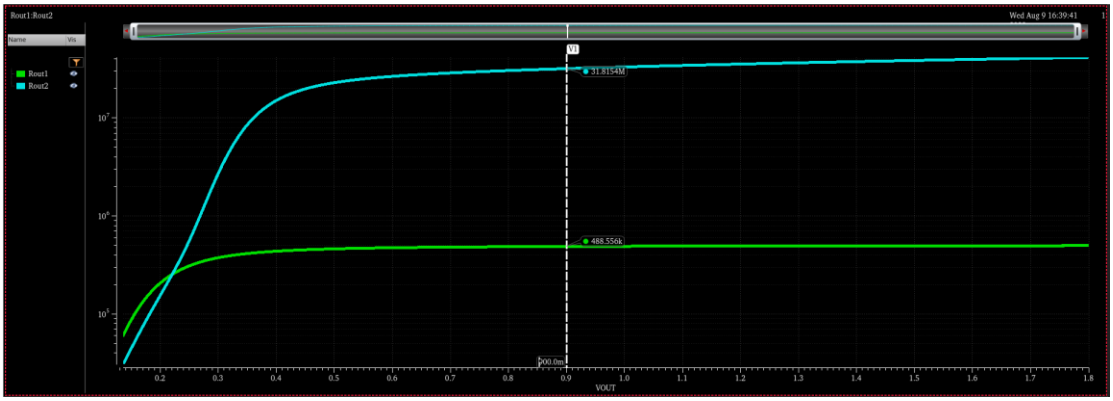


Figure 12 Figure 12 Rout VS Vout

o Comment on the difference between the two circuits.

Rout of wide-swing current mirror is more than that of simple current mirror, as output of wide swing current mirror act as a cascade amplifier that has high Rout compared with the simple current mirror.

o Does Rout change with VOUT? Why?

Yes, as Rout proportional with Vds on the transistor, for simple CS Vds is the same Vout and it directly effect on Rout, but for cascode CS there are two transistors (M3,M5) ,M3 has constant Vds, but M5 effected by Vout and that what make Rout in the second circuit changes.

5) **Analytically calculate Rout of both circuits at V results in a table.**

Hand analysis:

$$R_{out_{Simple}} = r_{o1} = \frac{1}{gds1} = \frac{1}{1.978\mu} = 505.6\ K\Omega$$

$$R_{out_{Wide}} = \frac{(g_{m5}+g_{mb5})}{g_{ds5}*g_{ds3}} = \frac{(313.6\mu+75.43\mu)}{1.987\mu*6.233\mu} = 31.41\ M\Omega$$

	Simulator	Analytical
Simple Current Mirror	488.556 KΩ	506.5KΩ
wide-swing Current Mirror	31.8154 MΩ	31.41MΩ

3. Mismatch

1) Set VMIS1 = 5m/sqrt(W*L) and VMIS2 = 0.
This models the standard deviation of the mismatch in VTH for the current mirror devices. Run OP simulation. Find the percent change in $Iout$.

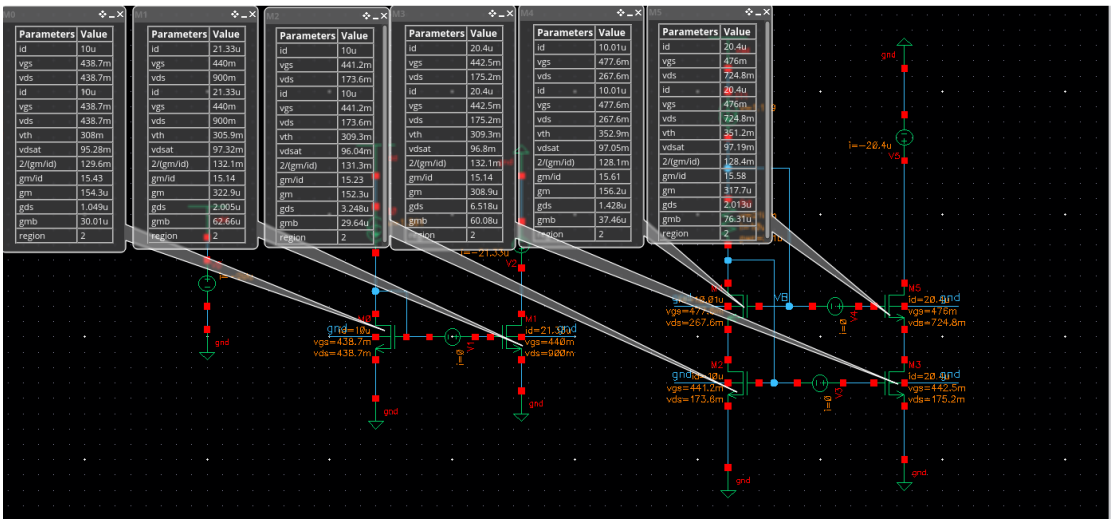


Figure 13 schematic with mismatch in VTH

For simple CS : the percent change in $Iout = \frac{21.33u-20.92u}{20.92u} = 1.96\%$

For Cascoded CS : the percent change in $Iout = \frac{20u-20.4u}{20u} = 2\%$

2) Analytically calculate the percent change in $Iout$ and compare it to the simulation result.

$$\Delta I = G_M\ \Delta V = gm\ \Delta V = \frac{2\ I_D * \Delta V}{V^*}$$

$$\frac{\Delta I}{I} = \frac{2\ \Delta V}{V^*} = \frac{2*V_{MIS}}{V^*} * 100 = 2\%$$

	Simulator	Analytical
Error %	1.96% , 2%	2%

3) Set VMIS1 = 0 and VMIS2 = 5m/sqrt(W*L). This models the standard deviation of the mismatch in VTH for the cascode devices. Run OP simulation. Find the percent change in $Iout$.

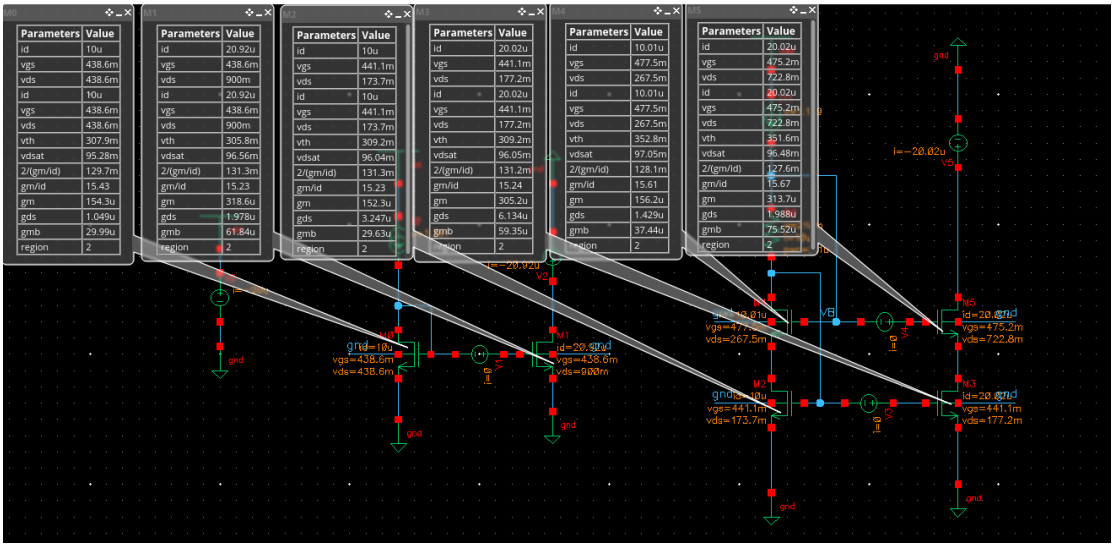


Figure 14 schematic with mismatch in VTH

For simple CS : the percent change in $Iout = \frac{20.9u - 20.9u}{20.9u} = 0$

For Cascoded CS : the percent change in $Iout = \frac{20u - 21.3u}{20u} = 0$

4) Analytically calculate the percent change in $Iout$ and compare it to the simulation result.

$$\frac{AI}{I} = G_M \, \Delta V = \frac{g_{m5} g_{ds3}}{((g_{m5} + g_{mb5}))I_D} * V_{MIS2} * 100 = \frac{313.7 * 6.13}{\big((313.7 + 75.5)\big) * 20} * V_{MIS2} * 100 = 0.031\%$$

	Simulator	Analytical
Error%	0%	0.031%

5)Which mismatch contribution is more pronounced? Why?

VMS1 in the (M0,M1) and (M2,M3) is more pronounced as it effect on the Vgs transistors that has direct effect on the current, but the mismatch VMS2 in (M4,M5) effect on Vds of the mirror that has weak effect on the current.

6) Which design decision is better: setting the same W and L for the mirror and cascode devices? Or using larger W and L for the current mirror devices? Why?

Using larger W and L for the current mirror devices is better, as increasing the area decrease the effect of the mismatch, we can't make it very large as the area of chip is proportional to the cost.