Analog IC Design

Lab 09 (Mini Project 01)

Two-Stage Miller OTA

PART 1: gm/ID Design Charts

NMOS

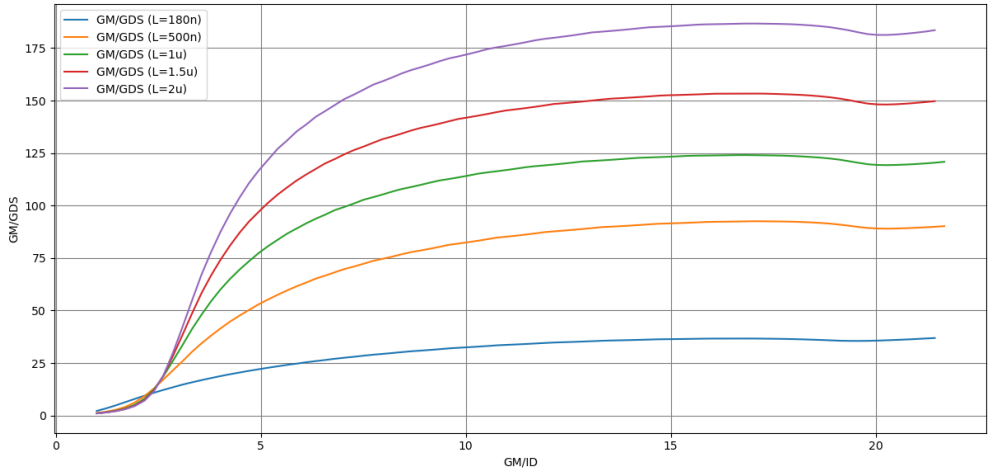


Figure 1 NMOS GM/GDS VS GM/ID

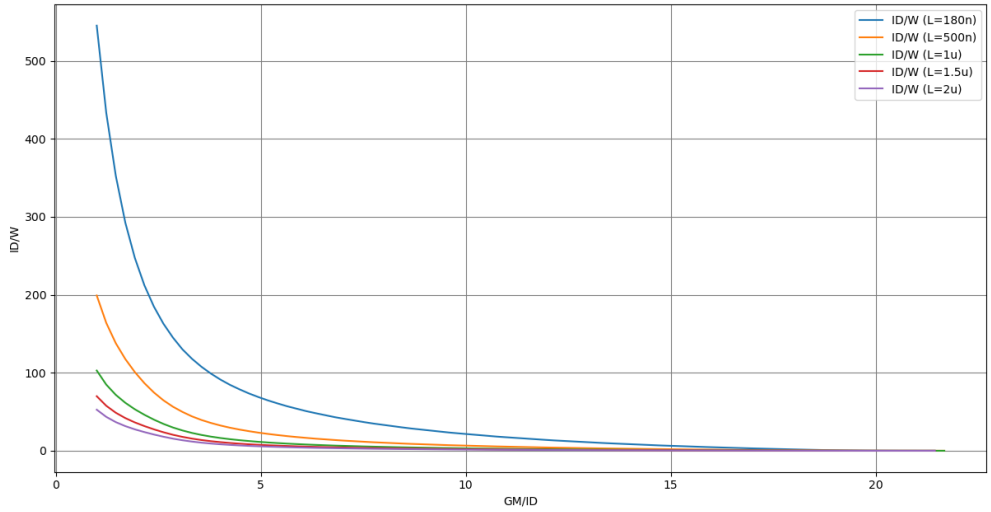


Figure 2 NMOS ID/W VS GM/ID

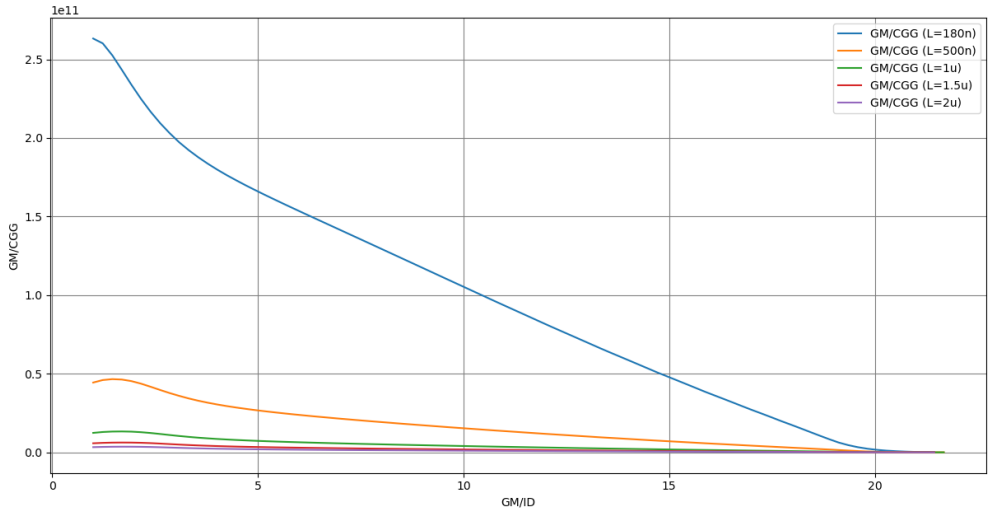


Figure 3 NMOS GM/CGG VS GM/ID

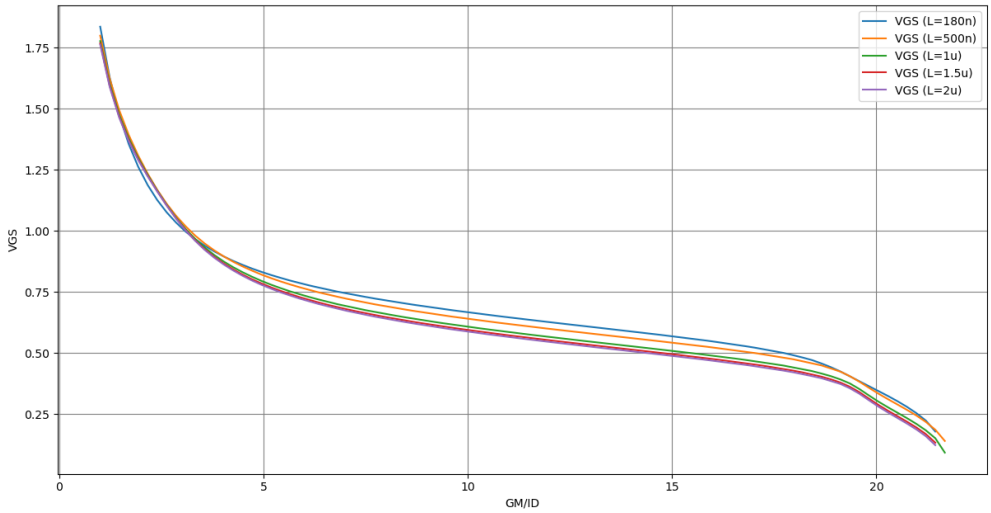


Figure 4 NMOS VGS VS GM/ID

PMOS

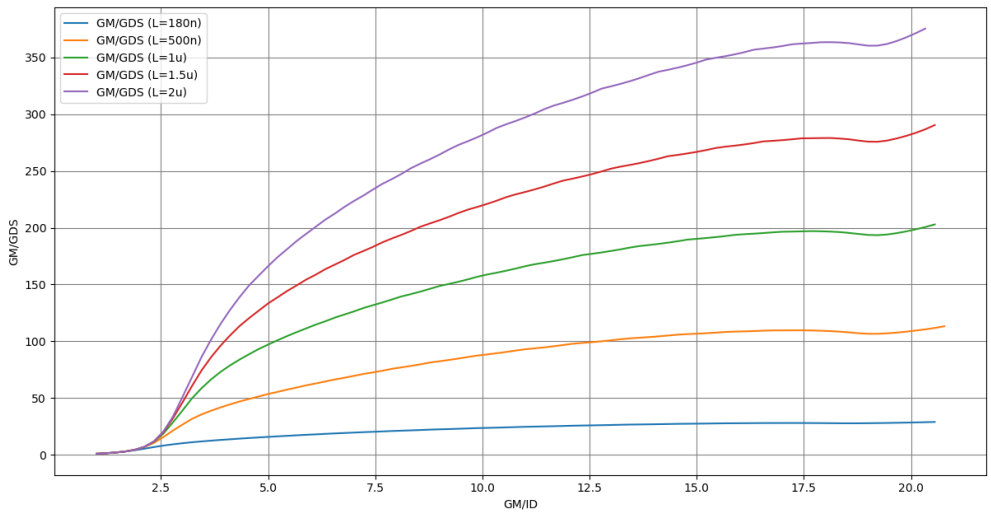


Figure 5 PMOS GM/GDS VS GM/ID

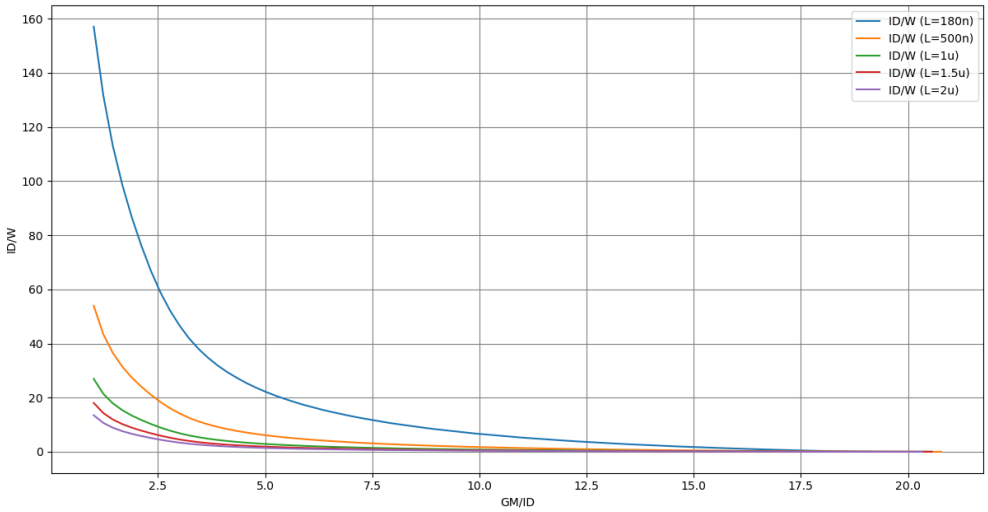


Figure 6 PMOS ID/W VS GM/ID

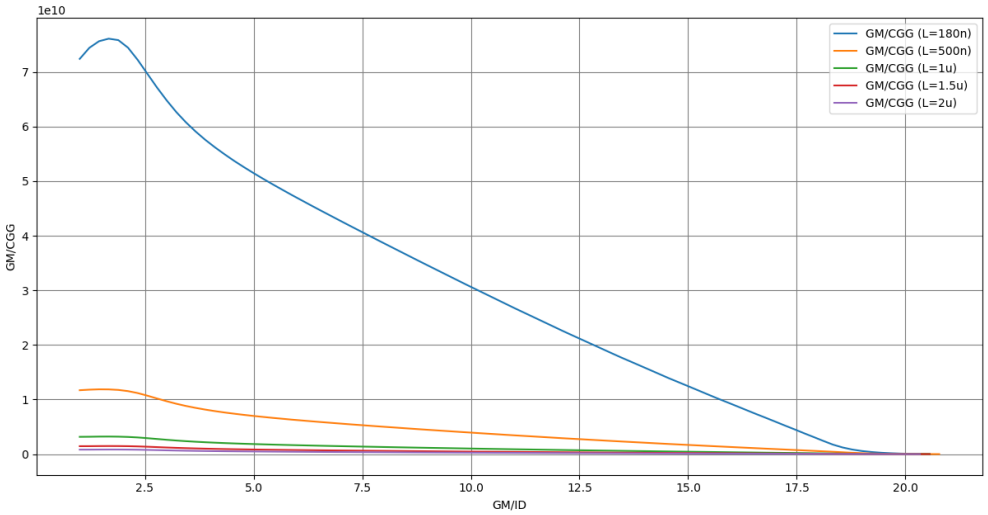


Figure 7 PMOS GM/CGG VS GM/ID

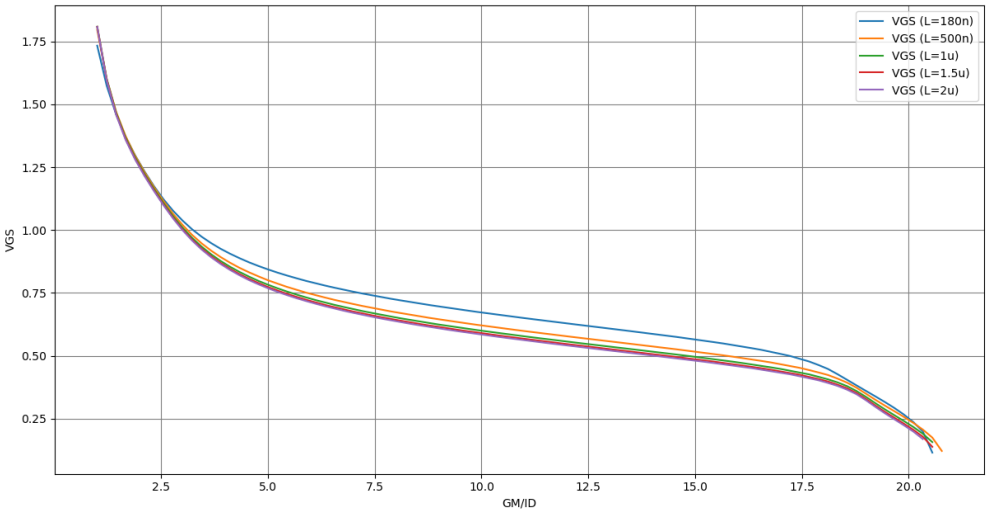


Figure 8 PMOS VGS VS GM/ID

Part 2: OTA Design

initially: Cc = 0.5*CL=2.5 pF

For the input pair

$VICM\_LOW$ = 0.2 (near to ground), so the input pair we will be used is PMOS.

$$\text{Slew rate (SR)} > \frac{\text{IB1}}{\text{CC}} = 5 = \frac{\text{IB}}{2.5}$$

$$\text{IB1} > \frac{12.5}{2} = 6.25 \text{ uA}$$

$$\text{IB2} = 60 - IB1 < 47.5$$

t (rise time) =0.35/BW =0.35Cc/gm1< 70ns

UGF = GBW = BW_cl= 5 M rad = 31.4 M

Gm1,2 = UGF * Cc = 31.4 M * 2.5 p =78.54 uS

$$\frac{\text{gm1,2}}{\text{Id1,2}} = \frac{78.54}{6.25} > 12.6$$

We will use it = 13

gain OL > 1 /0.0005 = 2000 = 66 dB

we will make the 1st stage gain = 36 and the 2nd stage =30

let Av2 = 2 * Av1

Av2 =30 dB = 31.62

Av1 = 36 dB = 63.25

CMIR – low = $-V_{GS1} + V_{dsat1} + -V_{GS3} < 0.2$

$$V_{GS3} < 0.6895$$

We will use it =0.6

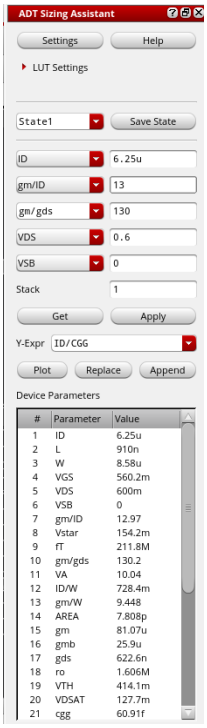


Figure 9 Sizing of the input pair

$$\text{CMRR} = \text{Avdiff in dB} - \text{Avcm in dB} > 74$$

$$\text{Avcm in dB} < -38$$

$$\text{Avcm} = \frac{1}{2 * gm3,4 * Rss} < 0.0126$$

$$Rss > \frac{1}{2 * gm3,4 * 0.0125}$$

$$\text{Let } \frac{gm3,4}{ID3,4} = 10$$

$$gm3,4 = 62.5 \text{ u}$$

$$gds = 1.575 \text{ u}$$

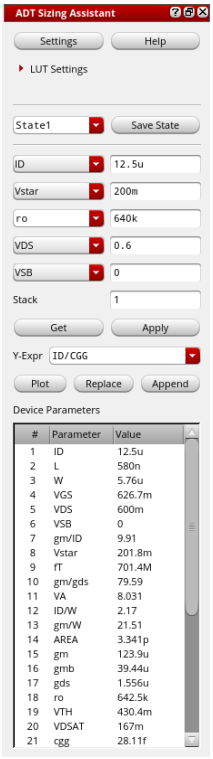


Figure 10 current mirror Iss

CMIR – high > VDD – V_5^* – Vgs1

$V_5^* > 0.117$

gm/ID5=gm/ID1

wp2 = 4 wu

gm5 = 8 gm1

I5=8I1=4Iss

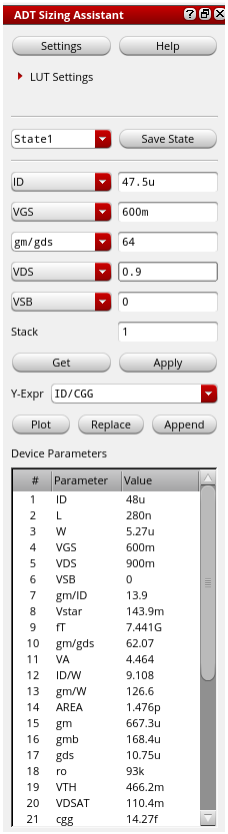


Figure 11 second stage load

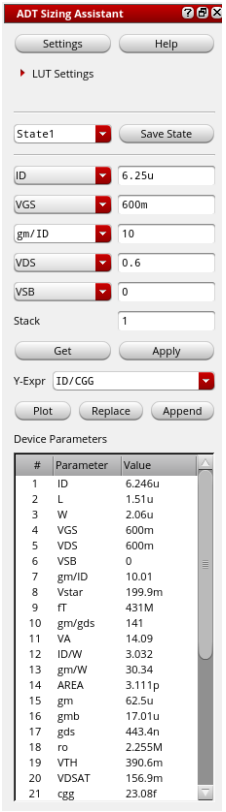


Figure 12 first stage load

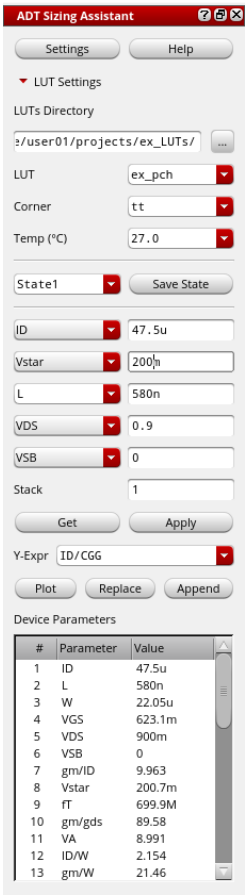


Figure 13 current source second stage

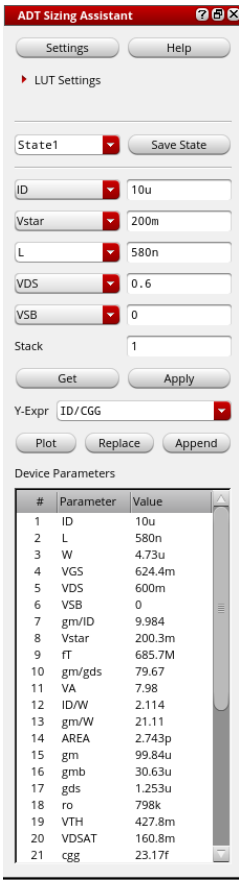


Figure 14 input source

Then we simulate and we find the current of the first stage = 12 so we increase the tail source width, then we sweep with the current mirror load of the first stage to make the output voltage =0.9 (VDD/2) at VICM = 0.6 (the middle of the CMIR) to have the MAX output swing.

And we will reduce Cc to change the slow rate, it will be about 2.1pf.

Design Variables	
IB	-10u
VICM	0.6
VICMac	1
VID	0
VIDac	0
Cc	2.5p
L_6	280n
L_Bios_IB	580n
L_Bios_in	580n
L_Bios_Iss	580n
L_in	910n
L_mirror	1.51u
Rc	1.5k
W_6	5.27u
W_Bios_IB	19.55u
W_Bios_in	4.73u
W_Bios_...	6.4u
W_in	8.58u
W_mirror	2.222u

Figure 15 Sizing results

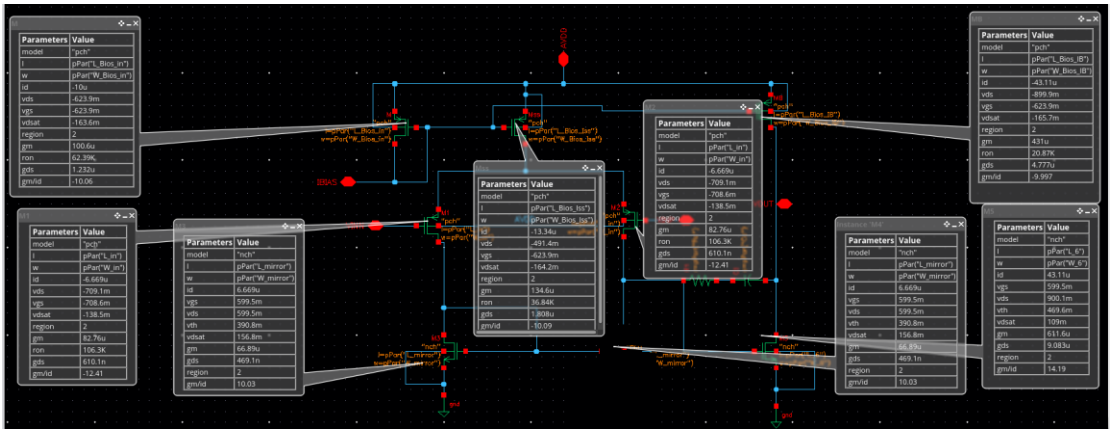


Figure 16 DC OP point

	M1,2	M3,4	Mss	M8	M5
W	8.58u	2.22u	6.4u	19.55u	5.27u
L	910n	1.51u	580n	580n	280n
gm	81u	62.5u	124u	474u	667u
ID	6.25u	6.25	12.5u	47.5	48
GM/ID	13	10	10	10	14
VDSsat	12.7m	156.9m	167m	160m	110m
Vov	146m	210m	197m	205m	134m
V*	154.2m	200m	202m	200m	144m

PART 3: Open-Loop OTA Simulation

• Is the current (and gm) in the input pair exactly equal?

Yes, as the transistors M1,2 have the same sizing and current.

- **What is DC voltage at the output of the first stage? Why?**

0.6 V , as it follow Vf and act as a perfect mirror, as the input pair have the same V_{GS} and V_{DS} and I_D, so that both voltages act as the same and Vout follow Vf.

- **What is DC voltage at the output of the second stage? Why?**

0.9 V , as it is = VDD/2 which we designed to give us MAX output swing.

1) Diff small signal ccs:

Ao_dB_MAX	expr	dB20(ymax(mag(VF("/VOUT"))))	70.56
Ao	expr	mag(VF("/VOUT"))	
Ao_MAX	expr	ymax(mag(VF("/VOUT")))	3.372K
Ao_dB	expr	dB20(mag(VF("/VOUT")))	
Ao_Phase	expr	phase(VF("/VOUT"))	
BW	expr	bandwidth(VF("/VOUT") 3 "low")	1.793K
fu	expr	unityGainFreq(VF("/VOUT"))	5.854M
GBW	expr	(Ao_MAX * BW)	6.046M
GBWo	expr	gainBwProd(VF("/VOUT"))	6.06M

Figure 17 circuit parameters

- **Plot diff gain (in dB) vs frequency.**

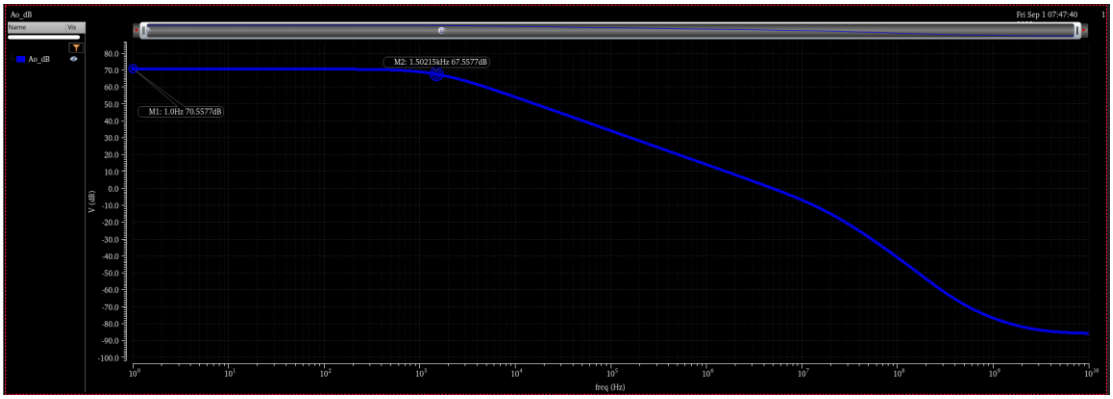


Figure 18 diff gain (in dB) vs frequency

Compare simulation results with hand calculations in a table.

Ro in the second stage is larger what we expected from SA.

DC gain= $g_{m1} * (r_1//r_4) * g_{m7} * (r_5//r_8)$

DC gain= $82.8u * \frac{1}{610+470} G * 612u * \frac{1}{4.8+9} M = 3400 = 70.63$ dB

Bandwidth= $\frac{1}{2\pi*(r_3//r_1)*g_{m7}*(r_5//r_8)*(C_c)} = 1.8k$

GBW= DC gain $*$ Bandwidth $= 6.27$M

	Simulation	Analytic
DC gain (dB)	70.56	70.63
Bandwidth	1.8k	$1.84k$
GBW	6.06M	6.275M

2) CM small signal ccs:

- **Plot CM gain in dB vs frequency.**

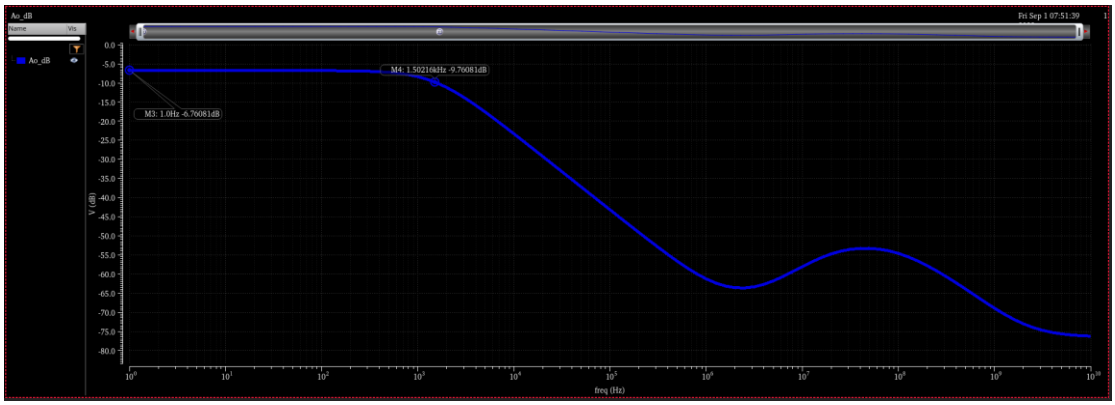


Figure 19 CM gain in dB vs frequency

Compare simulation results with hand calculations in a table.

$$\text{DC gain} = \frac{\frac{g_{m1}}{g_{m3}}}{1+2(g_{m1}+g_{mb1})R_{ss}} * g_{m7} * r_8 // r_5$$

$$\text{DC gain} = \frac{\frac{82.8}{66.9}}{1+2(82.8+18)*0.553} * 612 * \frac{1}{13.8} = 0.488 = -6.23 \text{ dB}$$

	Simulation	Hand calculations
DC gain (dB)	-6.77	-6.23

3) (Optional) CMRR:

- **Plot CMRR in dB vs frequency at VICM at the middle of the CMIR.**

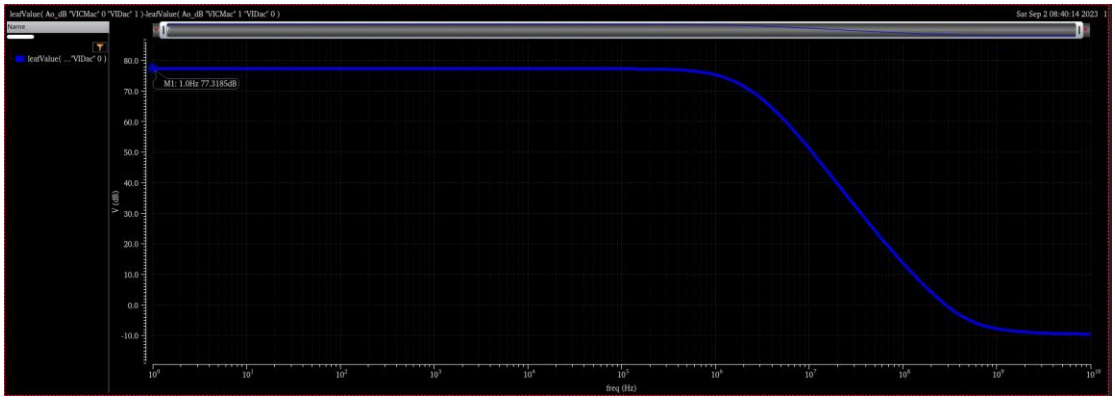


Figure 20 CMRR in dB vs frequency

Compare simulation results with hand calculations in a table.

$$CMRR = \frac{A_{vd}}{A_{vCM}} = A_{vd}(dB) - A_{vCM}(dB) = 70.63 + 6.23 = 76.86\ dB$$

	Simulation	Hand calculations
CMRR (dB)	77.3	76.86

2) (Optional) Diff large signal ccs:

- **Plot VOUT vs VID.**

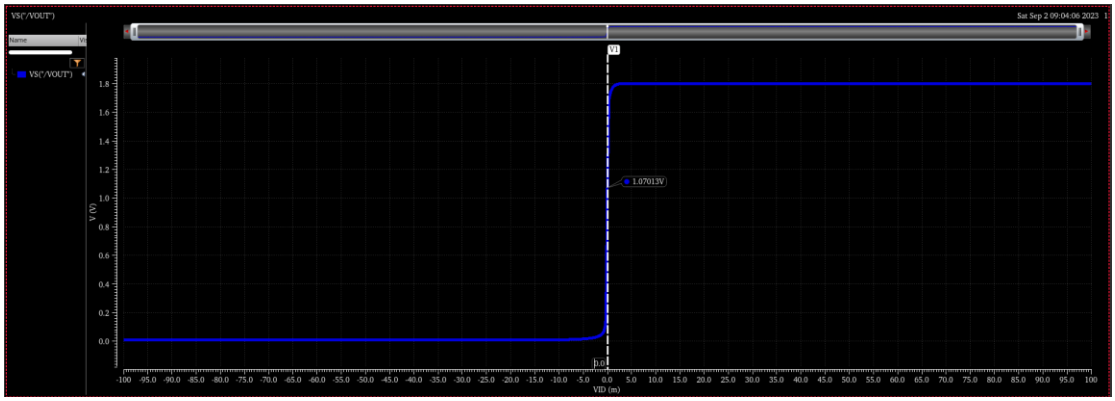


Figure 21 VOUT vs VID

- **From the plot, what is the value of Vout at VID = 0. Compare it with the value you obtained in DC OP.**

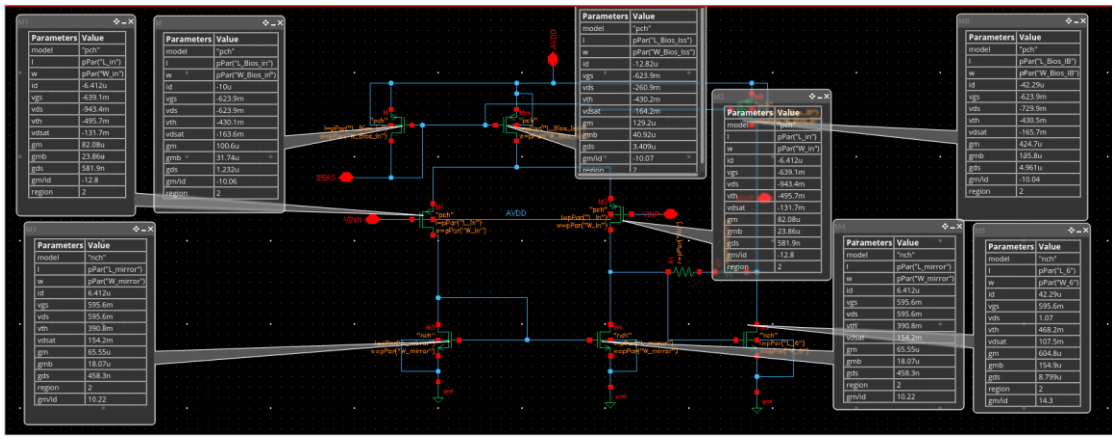


Figure 22 DC OP at VICM = 0.9

- **Plot the derivative of VOUT vs VID.**

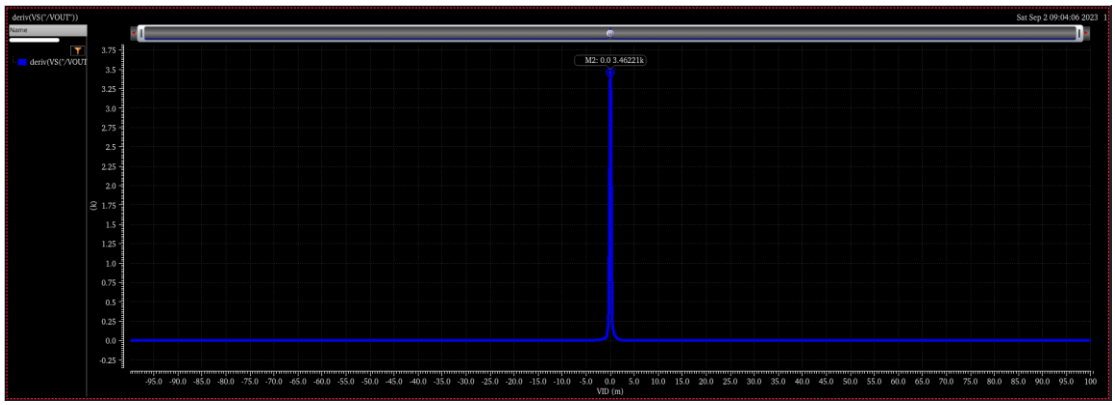


Figure 23 derivative of VOUT vs VID

Compare the peak with Avd from ac analysis. Comment on the result.

	peak	Avd
ac analysis	3.46k	3.372k

the small signal differential gain is almost The peak of the derivative (if we ignored the second order effects).

4) CM large signal ccs (region vs VICM):

• Plot "region" OP parameter vs VICM for the input pair and the tail current source.

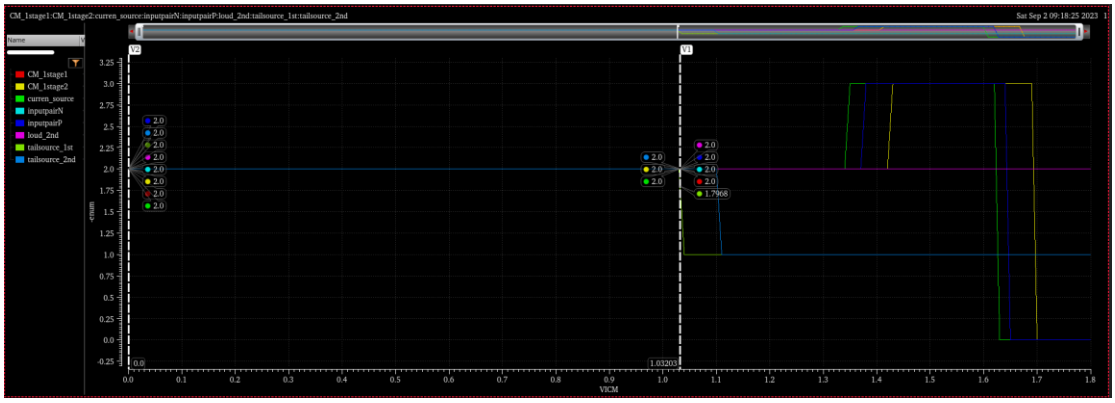


Figure 24 regions

• Find the CM input range (CMIR). Compare with hand analysis in a table.

hand analysis

$$V_{GS1} + V_{dsat1} + V_{GS3} < V_{inCM} < V_{DD} + V_{GS1} - V_{dsat5}$$

$$-639.1 - 131.7 + 0.6 < V_{inCM} < 1.8 - 639.1 - 164.2$$

$$-0.14 < V_{inCM} < 1$$

	MIN	MAX
Simulation	**0**	**1.03**
Hand analysis	**-0.14**	**1**

5) (Optional) CM large signal ccs (GBW vs VICM):

• Plot GBW vs VICM. Plot the results overlaid on the results of the previous method

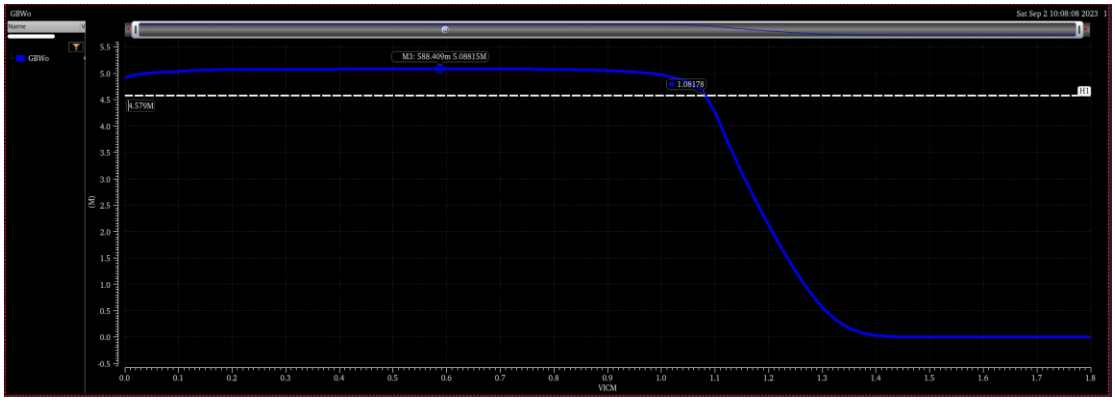


Figure 25 GBW vs VICM

the input range is from 0 V to 1.08 V

	GBW	Transistors Region
Max	1.08	1.03
Min	0	0
Range	1.08	1.03

PART 4: Closed-Loop OTA Simulation

1) Schematic of the OTA and the bias circuit with DC OP point clearly annotated in unity gain buffer configuration.

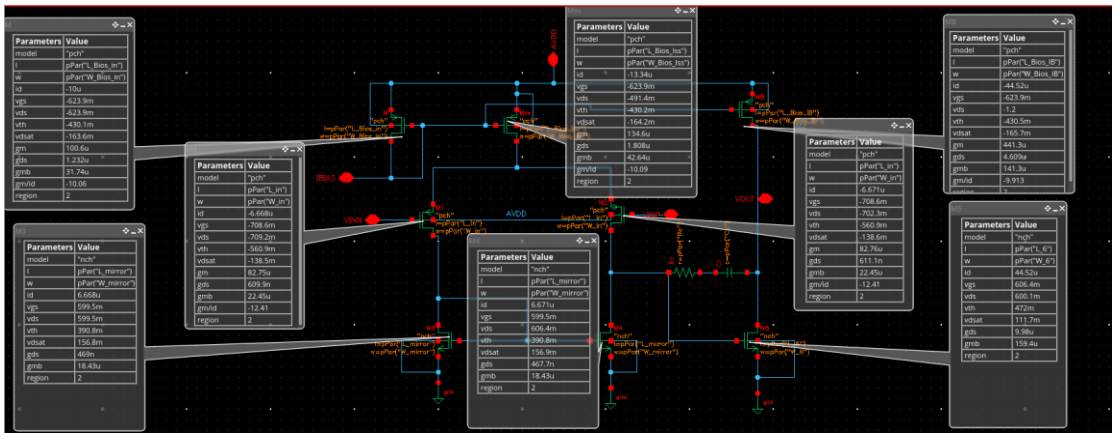


Figure 26 the bias circuit with DC OP point

- Are the DC voltages at the input terminals of the op-amp exactly equal? Why?

It is almost equal, as the amplifier has high gain Vo=**3.372k** so Verror = VOUT/Gain ≈ 0.1m

Details	Value
VDC("/VINP")	600m
VDC("/VINN")	600.1m

- Is the DC voltage at the output of the first stage exactly equal to the value in the open-loop simulation? Why?

there's a small difference in it due to the finite gain, but it almost equal as Vout of the 1st stage is still following Vf as VINN = VINP.

- Is the current (and gm) in the input pair exactly equal? Why?

the current is almost equal with a very small difference as VINN = VINP due to the high gain to give us a finite output, but if the Gain was infinite then the current and gm would be exactly the same.

2) Loop gain:

• Plot loop gain in dB and phase vs frequency.

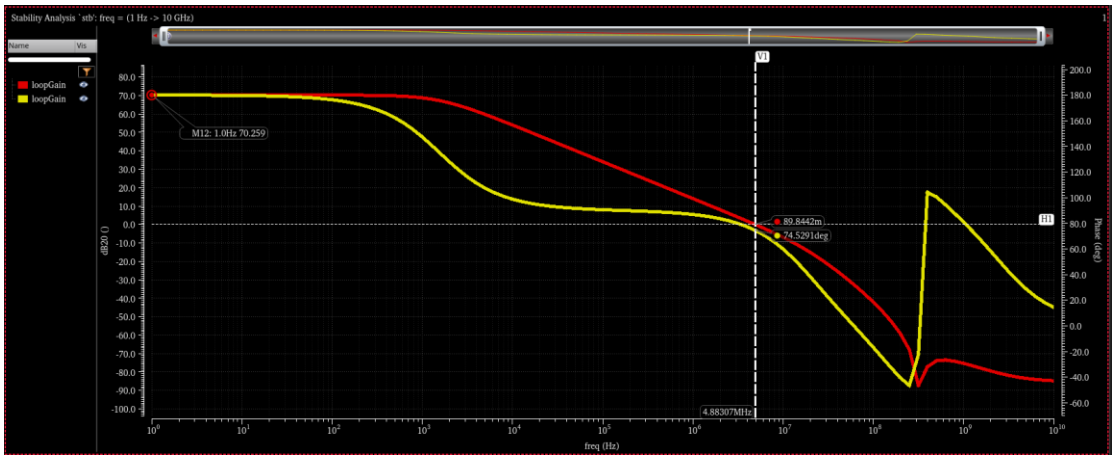


Figure 27 loop gain in dB and phase vs frequency

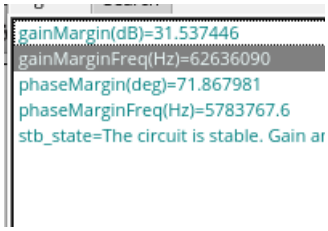
• Compare DC gain, fu, and GBW with those obtained from open-loop simulation. Comment

GPW	expr	gainBwProd(getData("loopGain" ?result "stb"))	6.052M
Phase_Margin	expr	getData("/phaseMargin" ?result "stb_margin")	71.87
UGF	expr	unityGainFreq(mag(getData("loopGain" ?result "stb")))	5.852M

	open-loop	Loop
DC gain	70.56	70.26 dB
fu	5.85M	5.85M
GBW	6.06M	6.052M

The feedback factor B=1 act as a buffer, so the loop gain and UGF is almost equal the open loop gain (there's a small difference due to the finite gain).

• Report PM.



Compare with hand calculations. Comment.

We Tring to make the Phase margin around 76 degree to make the system critical damped

	Simulation	Hand calculations
PM	$71.8\ deg$	$72.4\ deg$

$$PM = 90 - tan^{-1}\left(\frac{\omega_u}{\omega_{p2}}\right) = 90 - tan^{-1}\left(\frac{\frac{g_{m1}}{C_c}}{\frac{g_{m7}}{C_L}}\right) = 72.4\ deg$$

The system is underdamped, and an overshoot appears in time domain, the best case is to be critical damped which has no overshoot with PM = 76 deg and $\omega_{p2} = 4\omega_{u1}$.

Compare simulation results with hand calculations in a table.

$$\text{DC gain} = g_{m1} * (r_1 // r_4) * g_{m7} * (r_5 // r_8)$$

$$\text{DC gain} = 82.8u * \frac{1}{610+470} G * 612u * \frac{1}{4.8+9} M = 3400 = 70.63 \text{ dB}$$

$$\text{Bandwidth} = \frac{1}{2\pi * (r_3 // r_1) * g_{m7} * (r_5 // r_8) * (C_c)} = 1.8k$$

$$\text{GBW} = \text{DC gain} * \text{Bandwidth} = 6.27\text{M}$$

	Feedback	Hand calculations
Gain	70.26 dB	70.63 dB
GBW	6.052M	6.27M
PM	71.8 deg	72.4 deg

3) Slew rate:

- Report Vin and Vout overlaid.

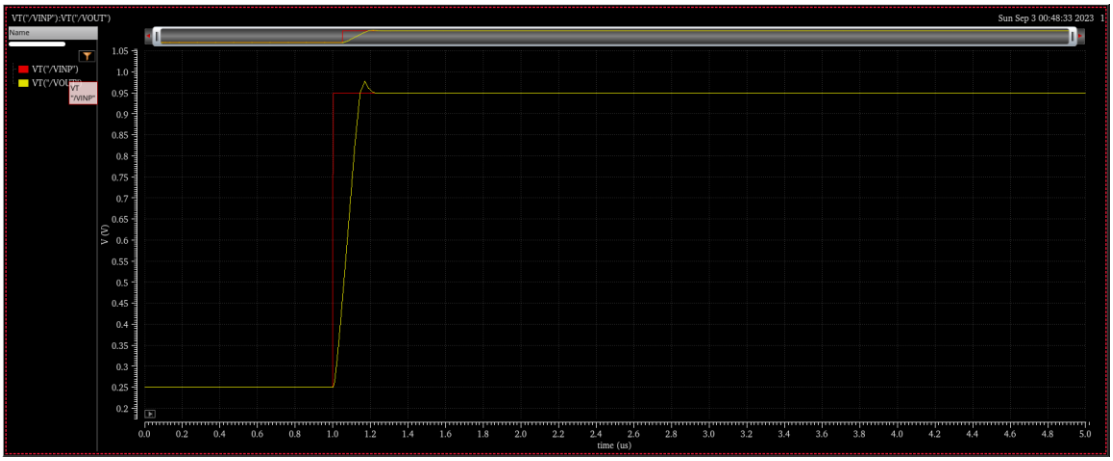


Figure 28 Vin and Vout vs time

- Report the slew rate.

	expr	ymax(slewRate(VT("/VOUT") 0.25 nil 0.95 nil 10 90 t "time"))	5.295M

- Compare simulation results with hand calculations in a table.

$$\text{SR} = \frac{I_{B1}}{C_c} = \frac{13.34u}{2.1p} = 6.3\ V/\mu s$$

	simulation	hand calculations
SR	5.295M	6.3M

4) Settling time:

• Calculate the output rise time from simulation.

riseTime(VT("/VOUT") 0.6 nil 0.605 nil 10 90 nil "time")	43.7n

• Compare simulation results with hand calculations in a table4.

	Simulation	Hand calculations
Rise time	43.7n	58n

t (rise time) =0.35/BW =0.35/6=58n

• Do you see any ringing? Why?

A small ringing, as There is just an overshoot in the output time domain as the phase margin = 71.8 < 76 so it is underdamping (it is so close to the critical damping but it is still underdamped).

Part 5 (optional): DC Closed Loop AC Open-Loop OTA Simulation

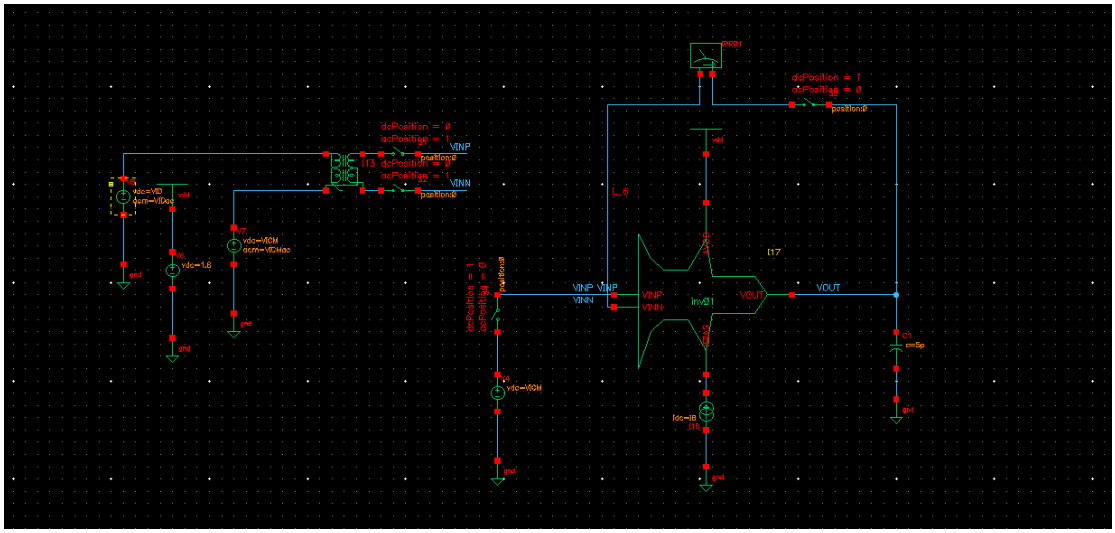


Figure 29 testBentch

Ao_2nd_dB	expr	dB20(ymax(mag(VF("/VOUT"))))	70.26
Ao_2nd	expr	ymax(mag(VF("/VOUT")))	3.258K
Ao_1st	expr	ymax(mag(VF("/I17/net4")))	76.45
Ao_1st_dB	expr	dB20(ymax(mag(VF("/I17/net4"))))	37.67
BW	expr	bandwidth(VF("/VOUT") 3 "low")	1.853K
fu	expr	unityGainFreq(VF("/VOUT"))	5.858M
GBW	expr	gainBwProd(VF("/VOUT"))	6.053M
Vout_2nd	expr	VDC("/VOUT")	600.1m
Vout_1st	expr	VDC("/I17/net4")	606.4m

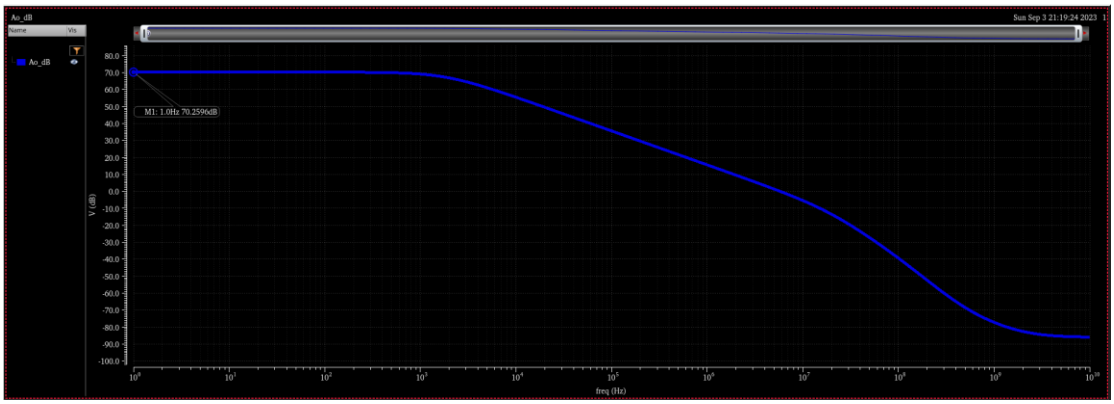


Figure 30 diff gain (in dB) vs frequency

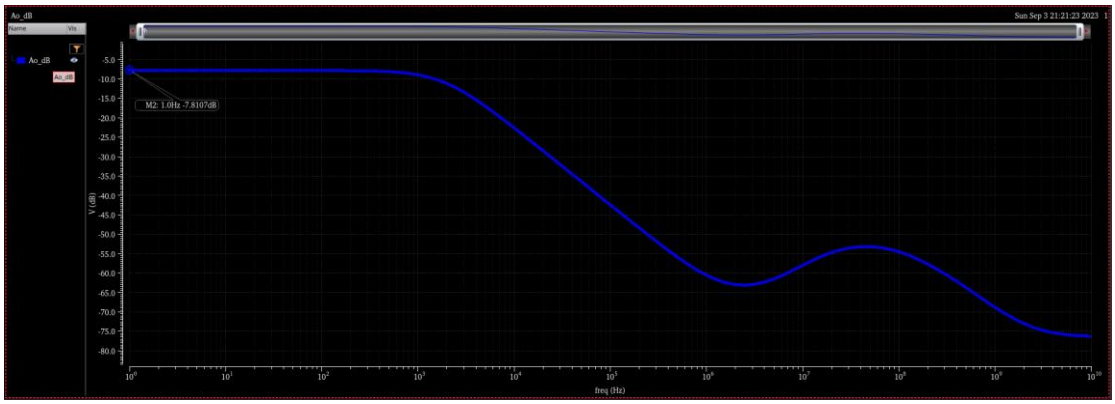


Figure 31 CM gain in dB vs frequency

CMRR at 1 Hz = diff gain (in dB) - CM gain (in dB) = 78.07 dB

It is almost the same as the outputs of part 3, as we used dc closed-loop configuration to simulate an ac open-loop one.