# Analog IC Design – Cadence Tools & SA

# Lab 06

# Differential Amplifier

## Part 1: Differential Amplifier Design

$R_D = 30\ K\Omega$

$V^* = 0.1356$

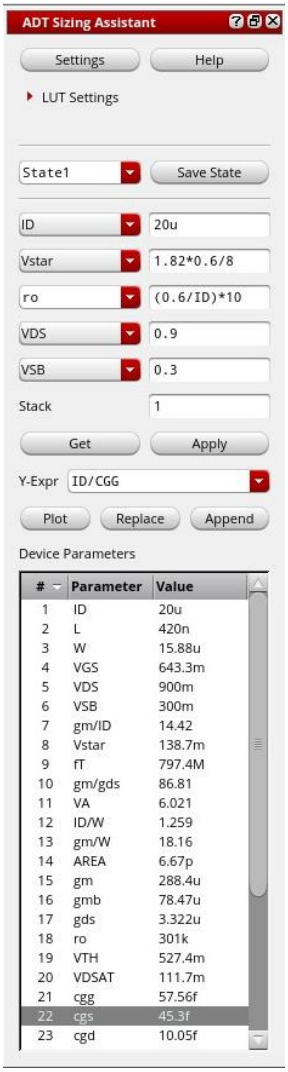


*Figure 1 the input pair sizing using SA*

L=420n , W=15.88u

**8) Give the above assumption, calculate the CM input level. Calculate the min and max CM input levels. Is the selected CM input level in the valid range?**

$ViCM = VDD - VSGdiff - VSDCS$ = 1.8– 643.3$m$– 300$m$ = 856.7 $mV$

The Input Common Code Range:

$ViCMmax = VDD - VSGdiff - V* = 1.0202\ V$

$ViCMmin = VRD - VTH = 72.6\ mV$

Yes, the selected CM input level is in the valid range as $ViCMmin < ViCM < ViCMmax$

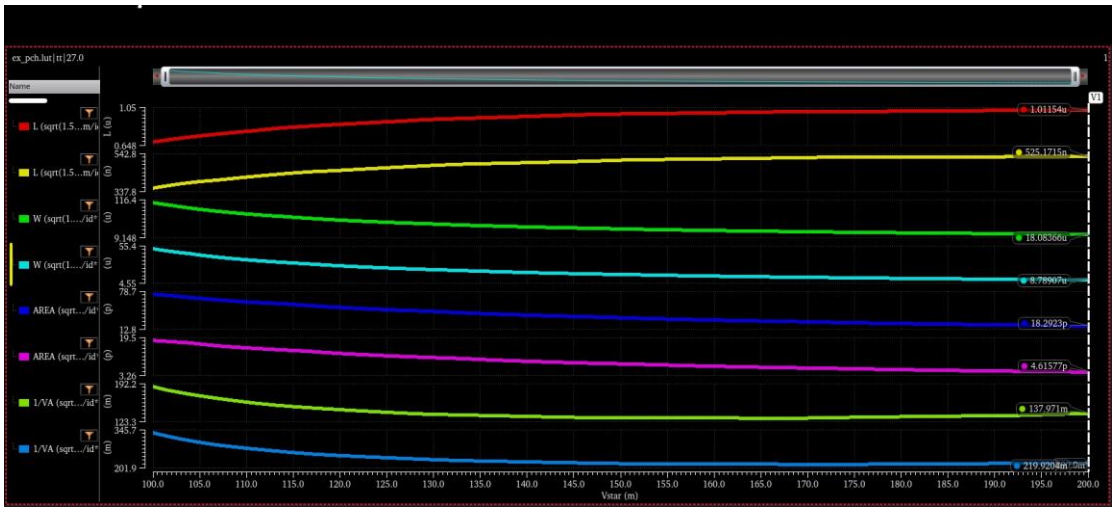


*Figure 2 sizing with (1% , 2%) mismatchVS V**

## Part 2: Differential Amplifier Simulation

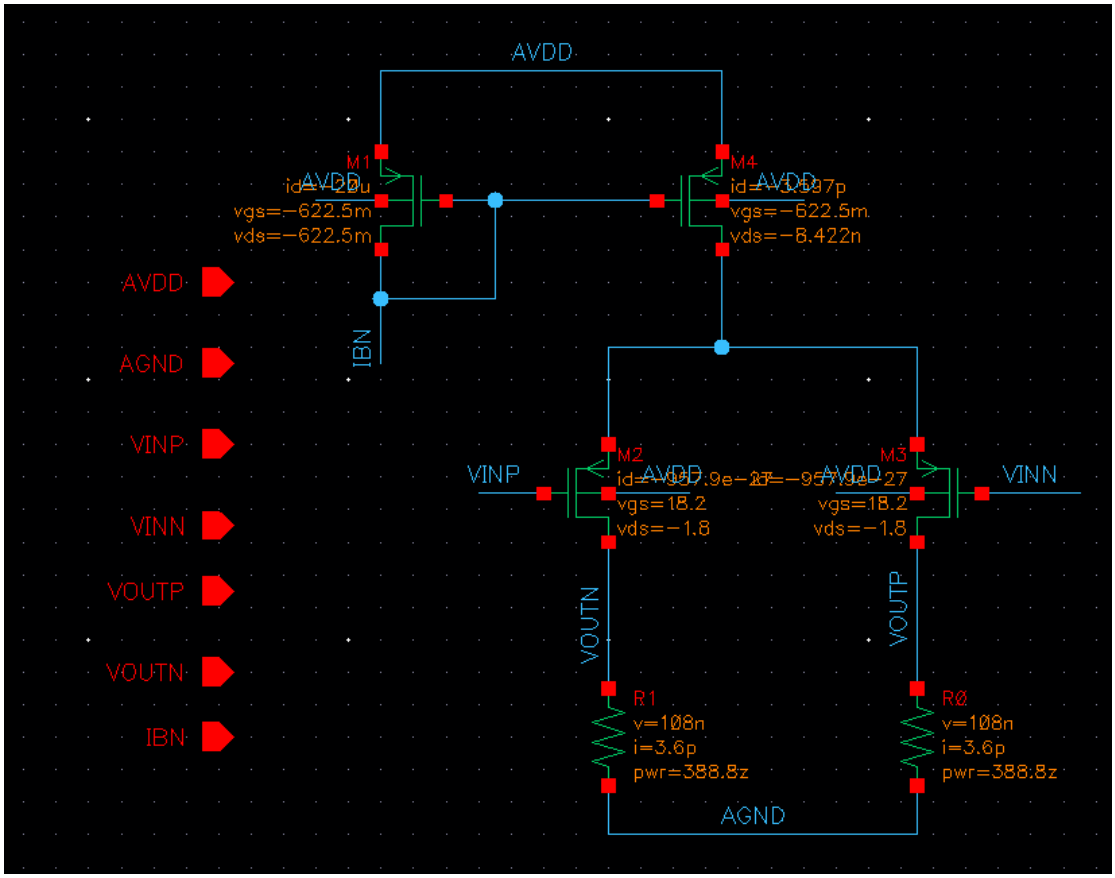


*Figure 3 the schematic of a differential amplifier*

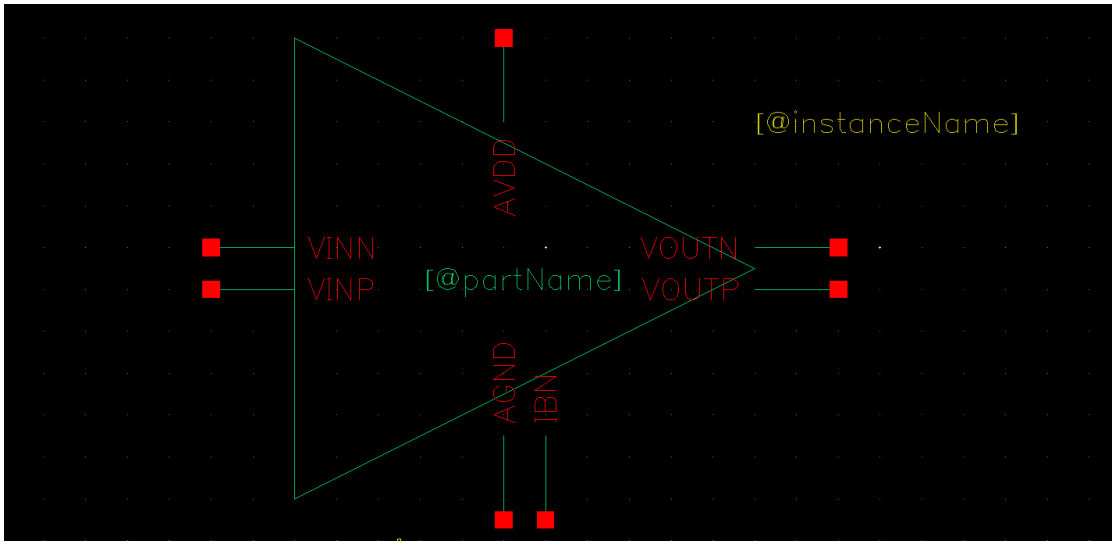


*Figure 4 symbol for the diff pair*

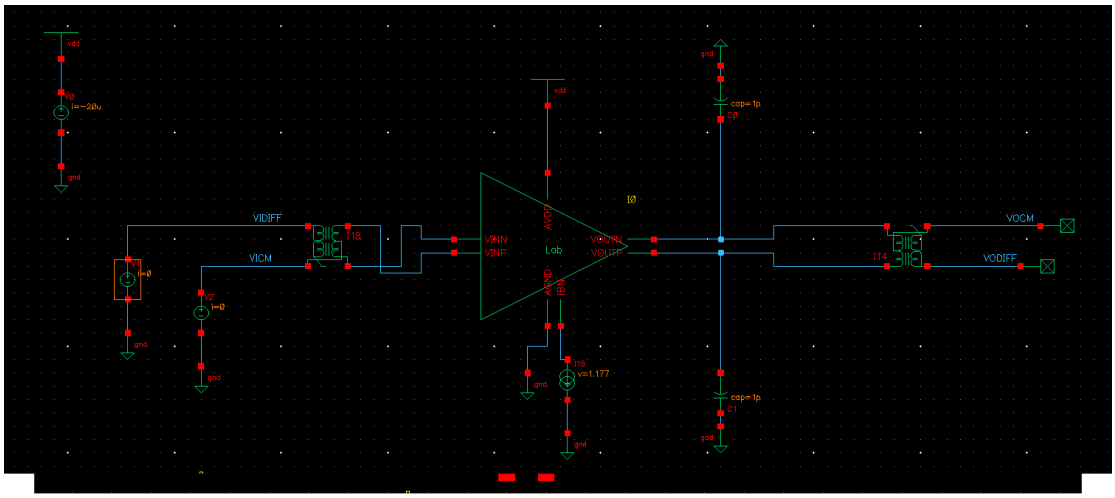


*Figure 5 the testbench schematic*

## 1) OP simulation

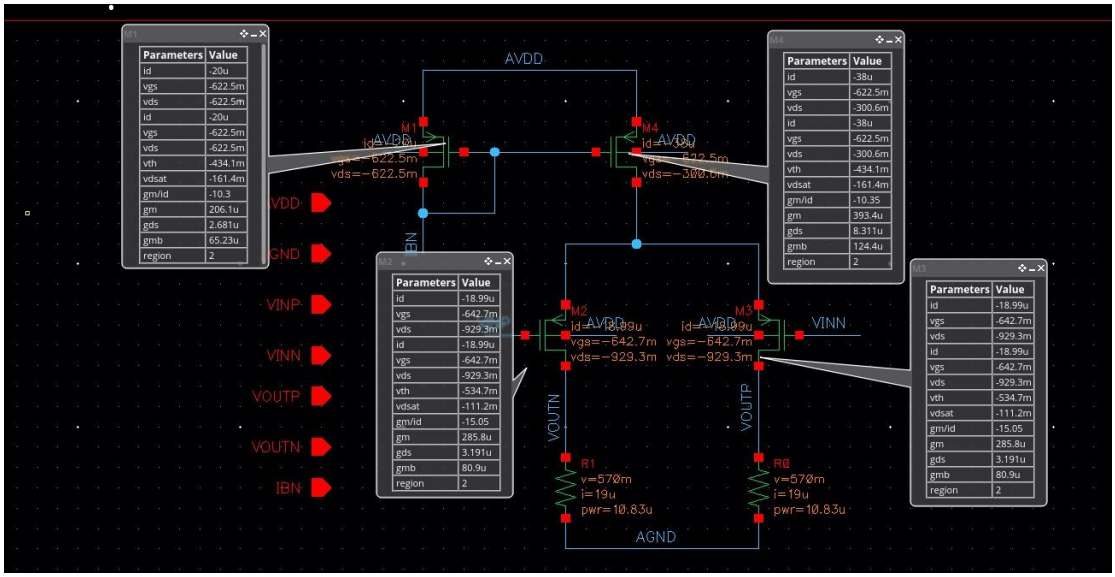


*Figure 6 DC OP point*

all transistors operate in saturation, as Region = 2

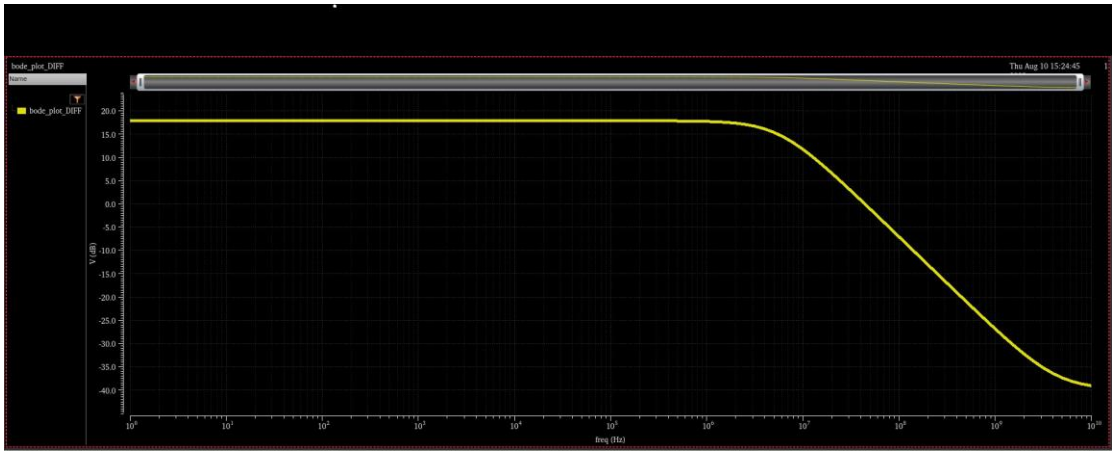


*Figure 7 the Bode plot of small signal diff gain*

Simulation gain = $10^{\frac{17.86}{20}} = 7.82$

| Name | Type | Details | Value | Plot | Save | Spec |
|---|---|---|---|---|---|---|
| | expr | VF("/VODIFF") | | ☑ | ☐ | |
| | expr | bandwidth(VF("/VODIFF") 3 "low") | 5.697M | ☑ | ☐ | |

*Figure 8 BW_DIFF*

BW (If we ignored the parasitic capacitance)=$\frac{1}{2\pi*30K*1p} = 5.305M$

The DC CM gain $\approx\ g_m * (R_D||r_o) = 7.8$

| | Simulation | Hand Analysis |
|---|---|---|
| BW | 5.7M | $5.305M$ |
| The DC diff gain | 7.8 | 7.8 |

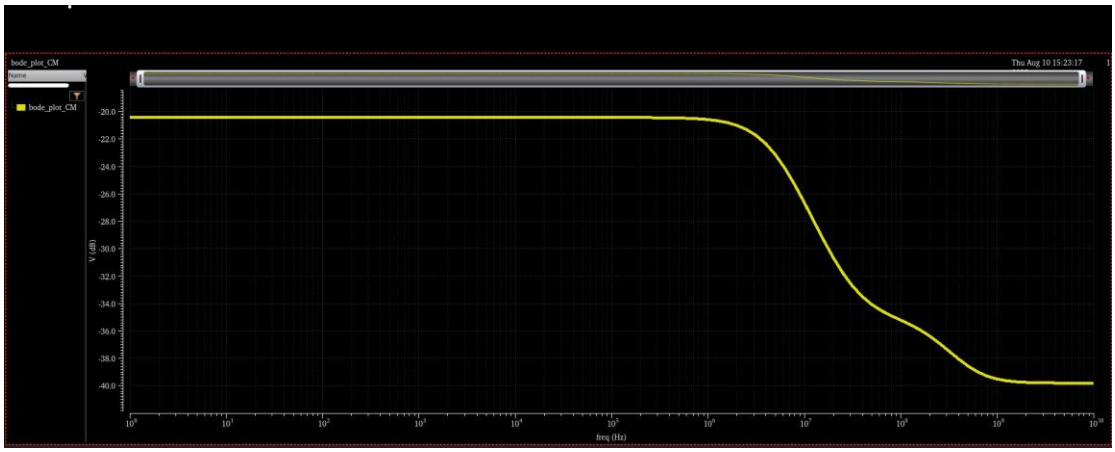


*Figure 9 the Bode plot of small signal CM gain*

| | | | |
|---|---|---|---|
| CM_BW | expr | bandwidth(VF("/VOCM") 3 "low") | 5.388M |

*Figure 10 BW_CM*

BW=$\frac{1}{2\pi*30K*1p} = 5.305M$

The DC CM gain (AvCM) $= -\frac{\mathrm{gm}\left(\mathrm{RD}//(r_o(1+(\mathrm{gm}+\mathrm{gmb})(2R_{ss}))\right)}{(1+(\mathrm{gm}+\mathrm{gmb})(2R_{ss}))} = -0.072\ \mathrm{m}$

$$R_{ss} = \frac{1}{g_{ds1,4}} = 120.3\ K\Omega$$

$$r_o = \frac{1}{g_{ds2,3}} = 313.4\ K\Omega$$

| | Simulation | Hand Analysis |
|---|---|---|
| BW | 5.388M | $5.305M$ |
| The DC diff gain | 0.08 | 0.072 |

**• Is it smaller than "1"? Why?**

Yes, due to the degeneration of the output resistance of the current source.

**• Justify the variation of Avcm vs frequency.**

Avcm has a small value, as Rss has high value, and it attenuates, due to the poles (c=1p, parasitics).

**• Plot Avd/Avcm in dB. Compare Avd/Avcm @ DC with hand analysis in a table.**

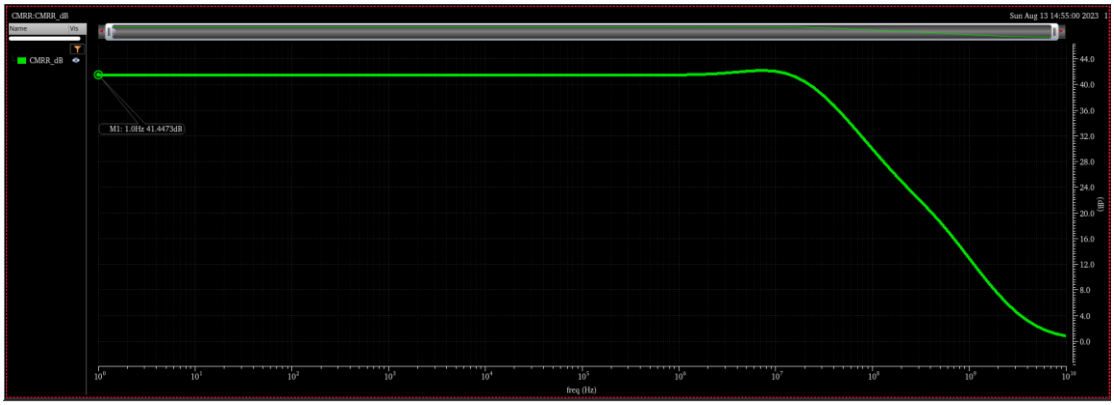


*Figure 11 CMRR dB*

Analytically Avd/AvCM = 108.33 = 40.7 dB

**• Justify the variation of Avd/Avcm with frequency**

CMRR follow Avd as it has large variation from 20dB to -40dB but Avcm has little variation from -20dB to -40dB so the variation of Avd/Avcm with frequency will be like the variation of Avd with frequency.

**4) Diff large signal ccs:**

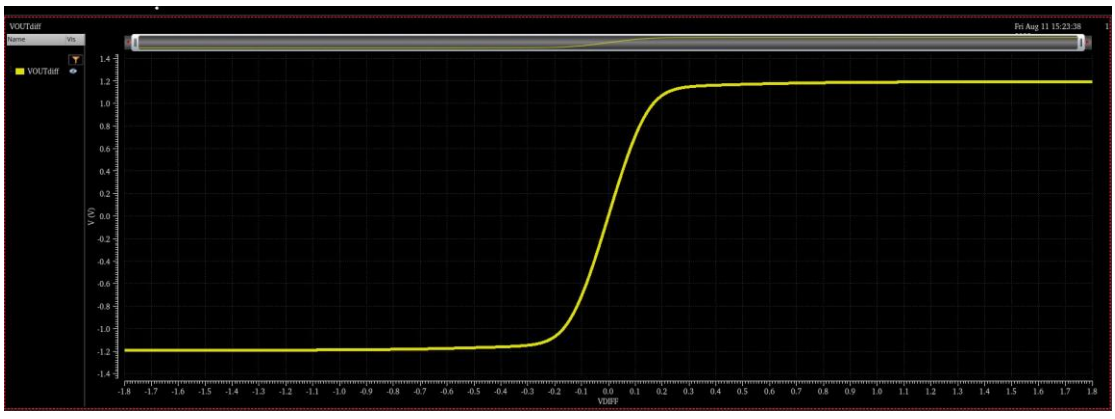


*Figure 12 VODIFF vs VIDIFF*

Analytically

The extreme values = $\pm IssRD$ = ±(40 $uA$)(30 $k\Omega$) = ±1.2 V

| | Simulation | Hand Analysis |
|---|---|---|
| Extreme Values | ±1.194 V | ±1.2 V |

**5) CM large signal ccs (region vs VICM):**


*Figure 13 Region vs Vicm*

**• The CM input range (CMIR) is from -76.85 mV to 1.04 V**

**Hand Analysis**

$ViCMmax = VDD - VSGdiff - V* = 1.0202\ V$

$ViCMmin = VRD - VTH = 72.6\ mV$

| | simulation | Hand Analysis |
|---|---|---|
| $ViCMmax$ | 1.04 V | 1.0202 $V$ |
| $ViCMmin$ | -76.85 mV | 72.6 $mV$ |

**6) CM large signal ccs (GBW vs Vicm):**

**MAX GAIN DIFF = 7.864 V**

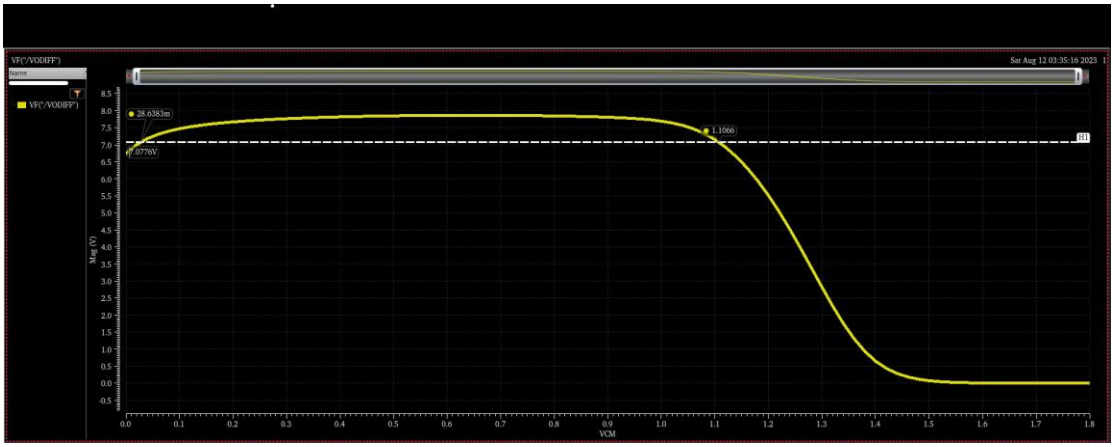


*Figure 14 Avd vs Vicm*

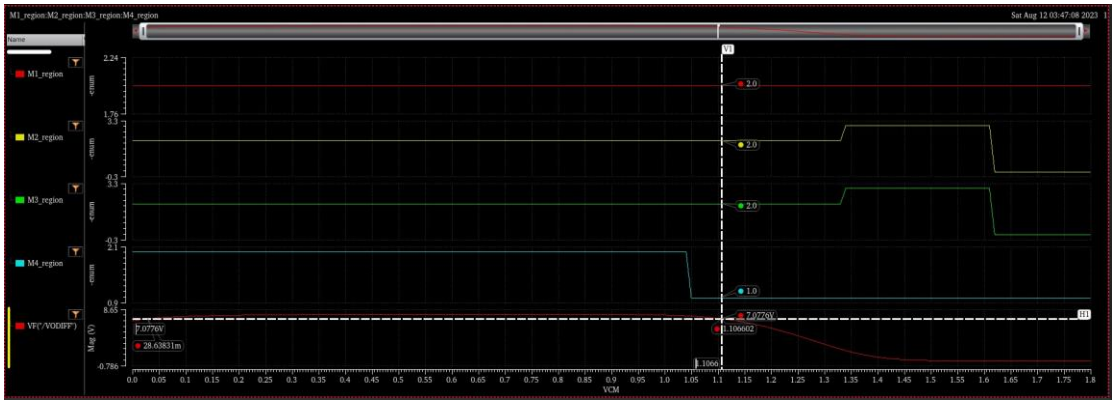


*Figure 15 Region parameter & Avd vs Vicm*

The CM input range = 28.6m : 1.1 V

| | From | TO |
|---|---|---|
| Avd 90% | 28.6m | 1.1 |
| Region | -76.85m | 1.04 |