GTU
Electronics Engineering

ELEC 331
Electronic Circuits 2

Fall Semester

Instructor: Assist. Prof. Önder Şuvak

HW 2
Questions

Updated October 20, 2017 - 13:37

Assigned:

Due:

Answers Out:

Late Due:

Contents

BJT Differential Amplifier Design

31. The circuit of Fig. 10.68 must provide a gain of 50 with $R_1 = R_2 = 5$ kΩ. If $V_{A,n} = 5$ V and $V_{A,p} = 4$ V, calculate the required tail current.

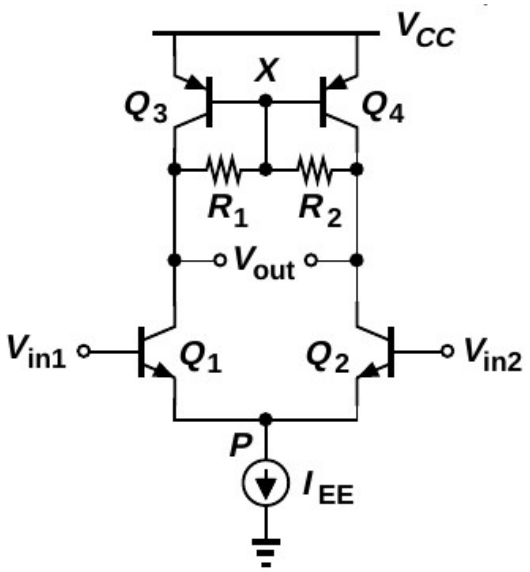


Figure 10.68

Necessary Knowledge and Skills: BJT small signal analysis, differential mode half circuit analysis, output impedance calculation, voltage gain calculation, parameter selection for design specification

MOS Amplifier

51. A student who has a single-ended voltage source constructs the circuit shown in Fig. 10.75, hoping to obtain differential outputs. Assume perfect symmetry but $\lambda = 0$ for simplicity.

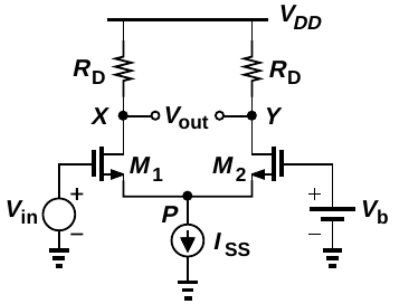


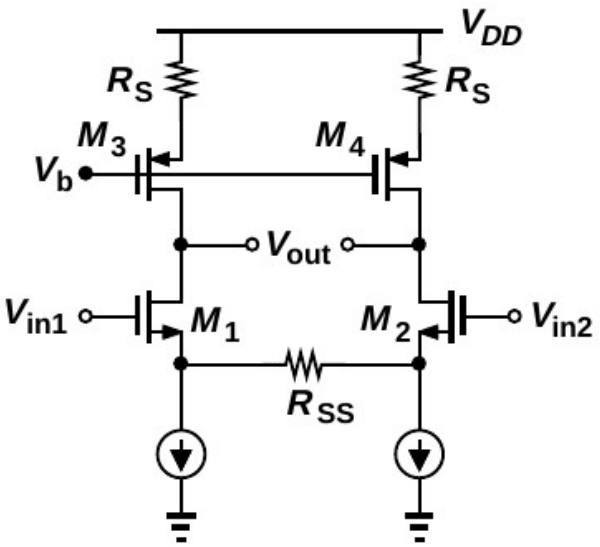
Figure 10.75

(a) Viewing M_1 as a common-source stage degenerated by the impedance seen at the source of M_2, calculate v_X in terms of v_{in}.
(b) Viewing M_1 as a source follower and M_2 as a common-gate stage, calculate v_Y in terms of v_{in}.
(c) Add the results obtained in (a) and (b) with proper polarities. If the voltage gain is defined as $(v_X - v_Y)/v_{in}$, how does it compare with the gain of differentially-driven pairs?

Necessary Knowledge and Skills: Common source/gate amplifiers, small signal equivalent MOS, differential pair gain and other calculations, performance comparisons

MOS Differential Pair

53. Calculate the differential voltage gain of the circuits depicted in Fig. 10.77. Assume perfect symmetry and $\lambda > 0$. You may need to compute the gain as $A_v = -G_m R_{out}$ in some cases.



(c)

Necessary Knowledge and Skills: MOS small signal analysis, output impedance calculation, common/differential mode half circuits, cascode structure, virtual ground in differential mode, voltage gain computation

BJT Differential Amplifier with Parasitics

55. Due to a manufacturing error, a parasitic resistance, R_P, has appeared in the circuit of Fig. 10.78. Calculate the voltage gain.

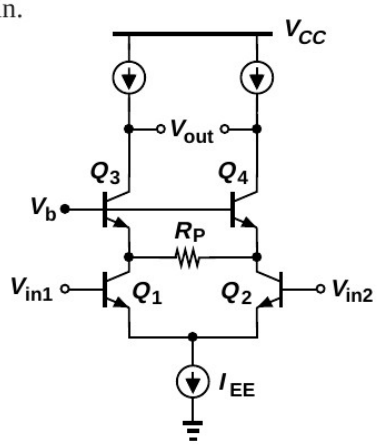


Figure 10.78

Necessary Knowledge and Skills: BJT small signal analysis, differential mode half circuit analysis, voltage gain computation, virtual ground in differential mode

MOS Diff. Amp. (Mismatch)

7.14 A design error has resulted in a gross mismatch in the circuit of Fig. P7.14. Specifically, Q_2 has twice the W/L ratio of Q_1. If v_{id} is a small sine-wave signal, find:

(a) I_{D1} and I_{D2}.
(b) V_{OV} for each of Q_1 and Q_2.
(c) The differential gain A_d in terms of R_D, I, and V_{OV}.

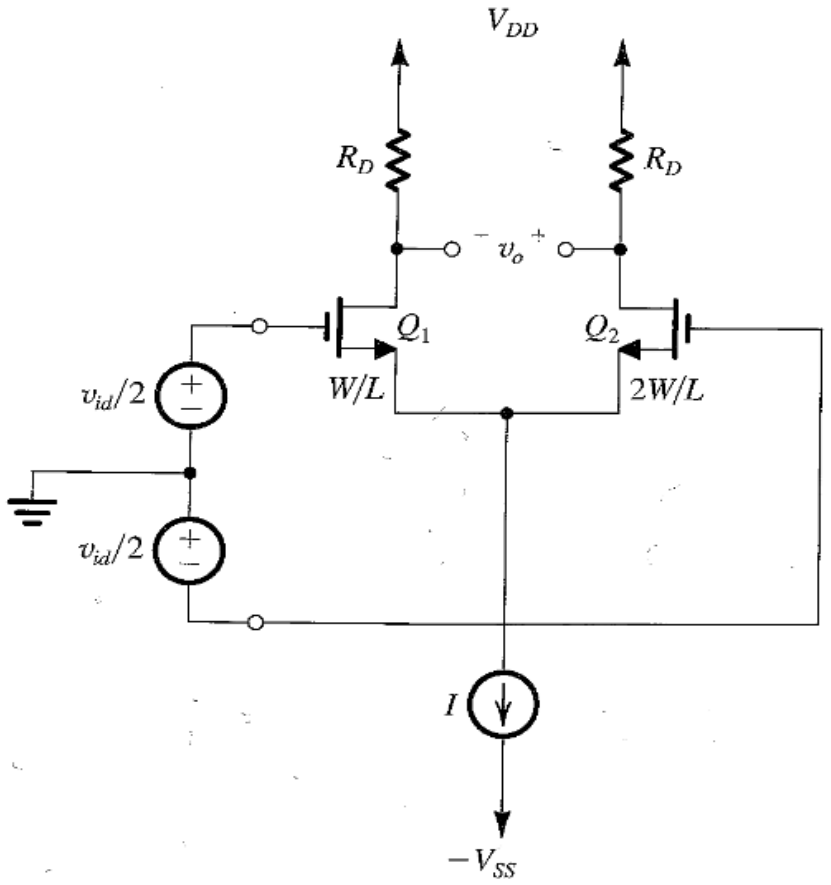


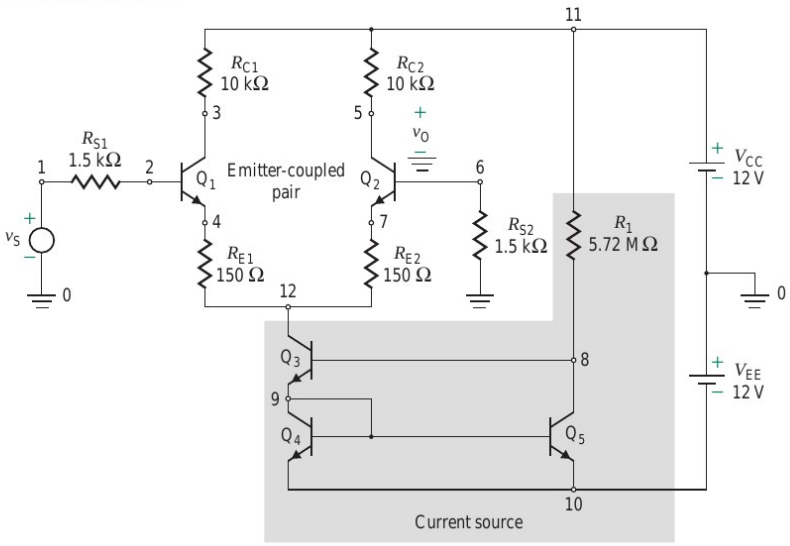
FIGURE P7.14

Necessary Knowledge and Skills: MOS differential, transistor mismatch, differential gain computation

BJT Differential Amp. With Current Source

9.39 (P) A differential amplifier is shown in Fig. P9.39. The transistors are identical. Assume $V_{BE} = 0.7$ V, $V_T = 26$ mV, $\beta_F = 50$, and $V_A = 40$ V. Calculate the values of A_d, R_{id}, A_c, R_{ic}, and CMRR.

FIGURE P9.39



Necessary Knowledge and Skills: Current source output current and impedance computation, BJT differential pair, BJT small signal analysis, common/differential mode half circuit analysis, voltage gain computations in common/differential modes, CMRR calculation

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