GYTE
Electronics Engineering

ELEC 331
Electronic Circuits 2

Fall 2014

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HW 12
Questions and Answers

Updated December 29, 2014 - 16:44

Assigned:	**20141216**
Due:	**20141229**
Answers Out:	**20141230**
Late Due:	**20150105**

Contents

Slew Rate of OpAmps

Derive an expression for the slew rate of an OpAmp, considering that an OpAmp consists of a differential amplifier stage followed by a gain stage. What is the relation between the high-frequency cut-off and the slew rate? Is there a trade-off between the slew rate and the phase/gain margins of a compensated and stable OpAmp? Could you use a compensated OpAmp as a comparator, whose responses are expected to be almost instantaneous to step inputs?

Notes: None.

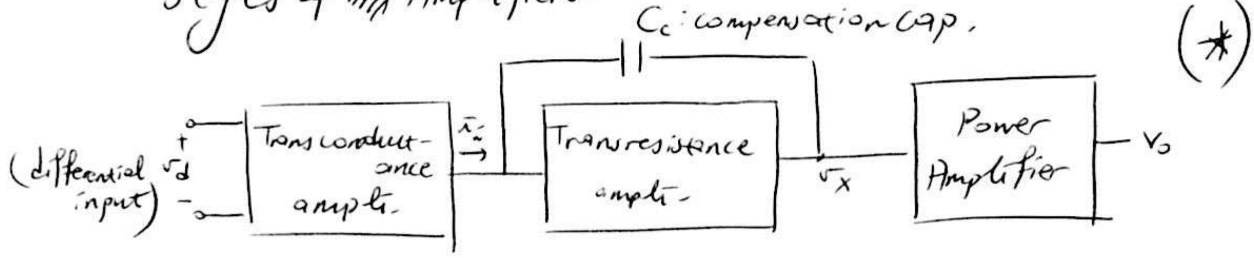
Additional Tasks: None.

Necessary Knowledge and Skills: OpAmps and cascaded stages, compensation and phase/gain margins, stability, slew rate, high-frequency cut-off, trade-offs.

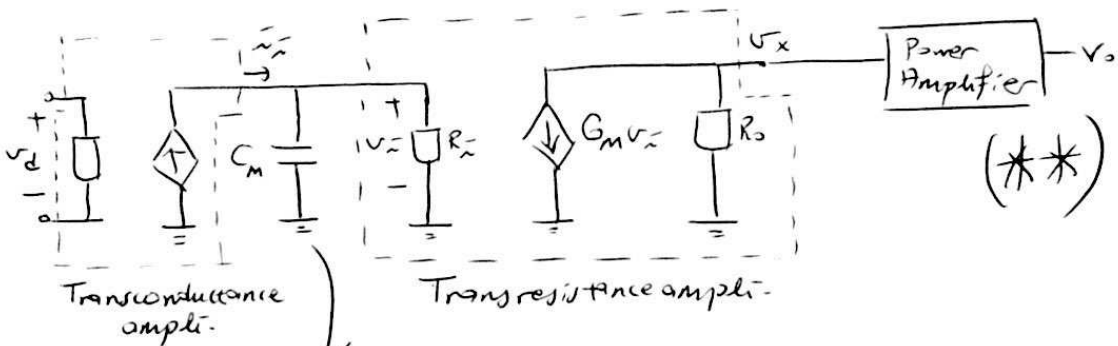
⇒ Review / Excerpt from Malik 9.6

Slew Rate of Op Amps

An OpAmp could be modeled as cascaded stages of Amplifiers.



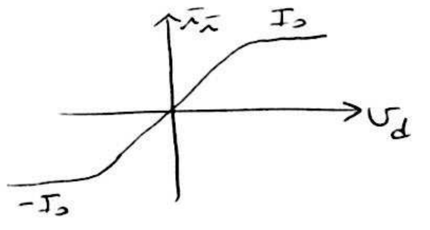
(*)



(**)

Miller capacitance (due to C_c and the gain across the nodes of i_π)

Maximum value of i_π into the second stage is I_o



I_o can be observed to be the tail current in differential amplifier stages.

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Slew rate of OpAmps

Voltage gain of the transresistance amplifier stage is $\Rightarrow -G_m R_o$

Then by the Miller effect:

$$C_M = C_c\left[1-(-G_m R_o)\right]$$

$$= C_c\left[1+G_m R_o\right]$$

By the OCTC method the high-frequency cut-off w_H of the opamp is approximately

$$w_H \cong \frac{1}{R_i C_M} \quad (C_M \text{ computed as above})$$

Refer to (**). KCL eqn:

$$C_M \frac{dv_i}{dt} + \frac{v_i}{R_i} - I_o = 0$$

Note that $I_o \gg \frac{v_i}{R_i}$

Then

$$C_M \frac{dv_i}{dt} \simeq I_o$$

Note also that $v_o \approx v_x$ (because of the power amplifier)

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Slew rate of op amps

Define Slew rate as

$$\text{Slew Rate} = \left|\frac{dv_o}{dt}\right|$$

when i_i is max (i_i is I_o) due to a large step input at v_d (the differential stage).
Also assume that C_c is initially uncharged.

Then

$$\text{Slew Rate} = \left|\frac{dv_o}{dt}\right| \cong \left|\frac{dv_x}{dt}\right|$$

$$= \left|\frac{dv_x}{dv_i}\right| \left|\frac{dv_i}{dt}\right|$$

$$= G_m R_o \left|\frac{dv_i}{dt}\right|$$

$$= G_m R_o \frac{I_o}{C_m}$$

$$= G_m R_o \frac{I_o}{C_c(1 + G_m R_o)}$$

$$\approx \frac{I_o}{C_c}$$

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Slew rate of opamps

Recall

$$w_H = \frac{1}{R_{\tilde{\,}} C_M} = \frac{1}{R_{\tilde{\,}} C_c (1+G_m R_o)}$$

Then

$$\frac{1}{C_c} = w_H R_{\tilde{\,}} (1+G_m R_o)$$

$$\approx w_H R_{\tilde{\,}} R_o G_m$$

$$\text{Slew rate} \cong \frac{I_o}{C_c} = I_o w_H R_{\tilde{\,}} R_o G_m$$

Note that the slew rate is inversely proportional to C_C and proportional to w_H.

C_C is a compensation capacitance.

If C_c is increased, the phase and gain margins will illustrate that the opamp will more away from instability, but w_H (the bandwidth) will decrease.

The ideal value of the slew rate is infinity ($+\infty$).

This shows that $C_c \to 0$ for $S.R. \to +\infty$.

But then the compensation is lost.

In All, the increase in C_C will cut the bandwidth, will make the opamp more stable, but then the slew rate will decrease.

There is a trade-off between the slew rate and the compensation capacitance

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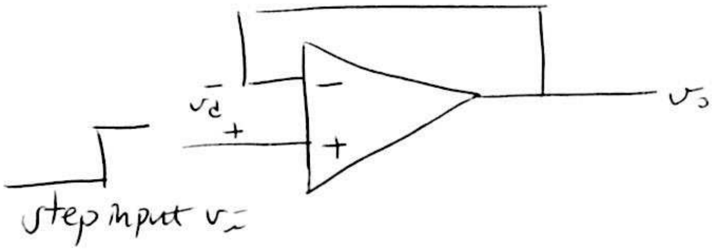
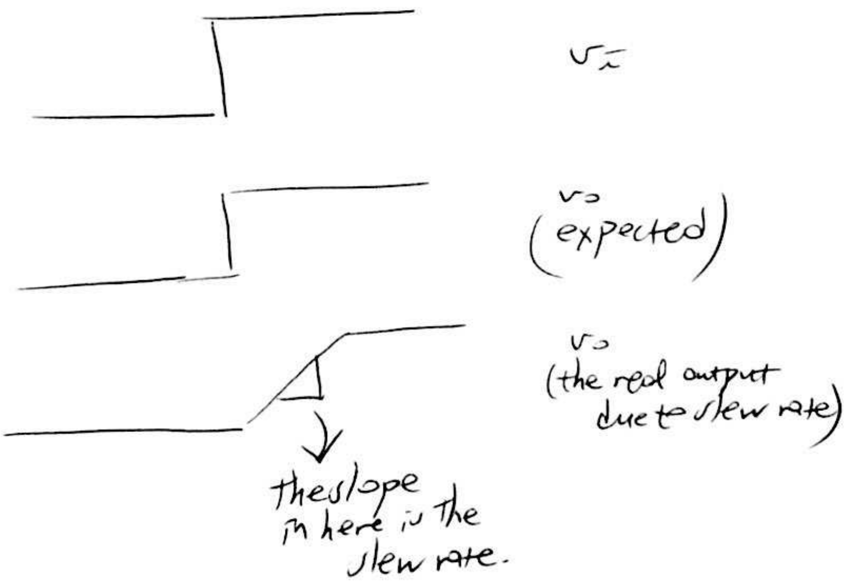
Due to the slew rate, the opamp will not respond instantaneously to a large step input.

Slew rate of opamps





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Basic CMOS OpAmp **Sedra 9.2**

9.2 The CMOS op amp of Fig. 9.1 is fabricated in a process for which $V'_{An} = 25$ V/μm and $|V'_{Ap}| = 20$ V/μm. Find A_1, A_2, and A_v if all devices are 0.8-μm long and are operated at equal overdrive voltages of 0.25-V magnitude. Also, determine the op-amp output resistance obtained when the second stage is biased at 0.4 mA. What do you expect the output resistance of a unity-gain voltage amplifier to be, using this op amp?

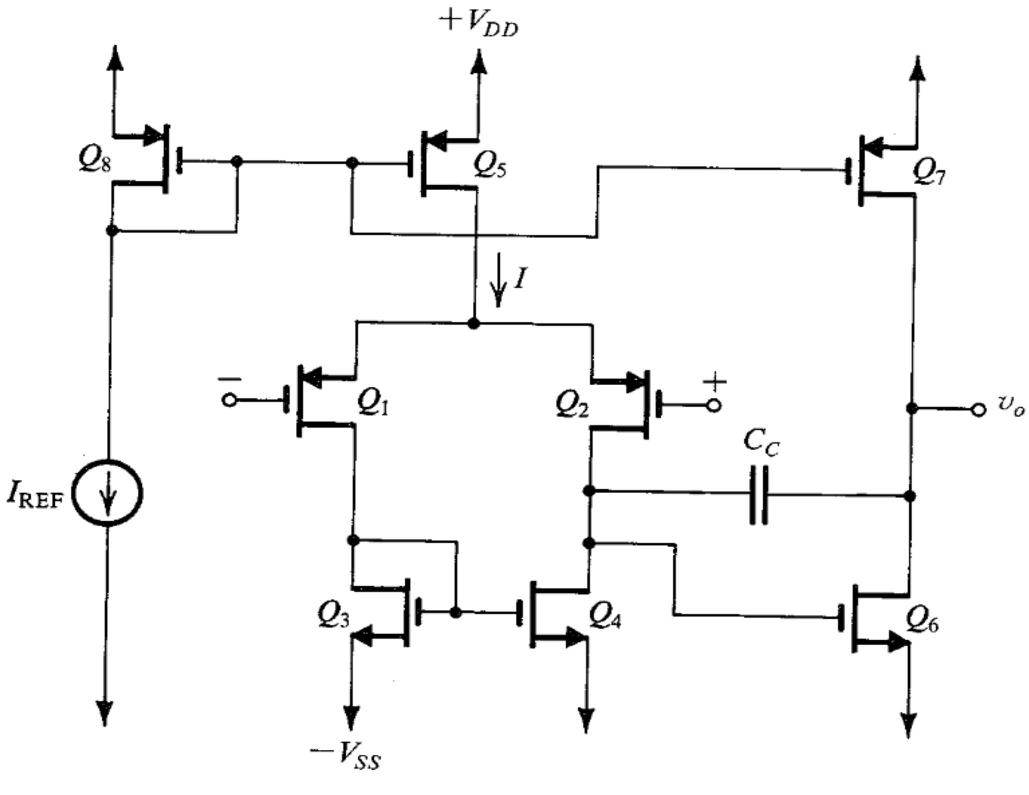


FIGURE 9.1 The basic two-stage CMOS op-amp configuration.

Basic CMOS OpAmp **Sedra 9.2**

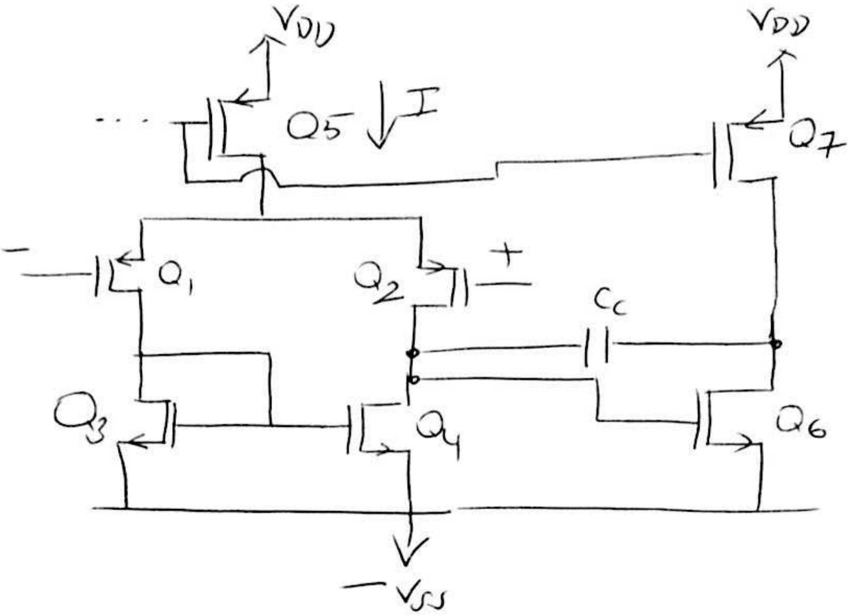
Notes: A1 is the differential amplifier gain, A2 is the common source gain. Av is their product. Also ignore the load of the feedback network on the forward amplifier when designing the unity-gain amplifier (which is a feedback amplifier) with this OpAmp.

Additional Tasks: How would you design the sizing of the transistors so that DC output offset is minimized? See Section 7.7.1 of Sedra and Smith.

Necessary Knowledge and Skills: Basic CMOS amplifier, design of transistor sizes, systematic DC output offset minimization, gain computation, differential amplifier, CS amplifier, feedback amplifiers, improvement factors.

In order to cancel the systematic DC output offset, consider the following:

Sedra 9.2



(see Sedra section 7.7.1 for an explanation, more detailed than the below)

$\Rightarrow I_{D5} = 2I_{D4} = I$

$\Rightarrow V_{D4}$ in DC bias almost the same as V_{D3}.

$\Rightarrow V_{G6} \approx V_{D4} \stackrel{\sim}{=} V_{D3}$

$\Rightarrow$ then $I_{D6} = \dfrac{(W/L)_6}{(W/L)_4} I_{D4} = \dfrac{(W/L)_6}{(W/L)_4} \dfrac{I}{2}$

$\Rightarrow$ similarly $I_{D7} = \dfrac{(W/L)_7}{(W/L)_5} I_{D5} = \dfrac{(W/L)_7}{(W/L)_5} I$

$\Rightarrow$ a deviation in I_{D7} with respect to I_{D6} will cause a deviation in V_{D6} (the output DC value)

$\Rightarrow$ to cancel the undesired deviation in $V_{D6} \Rightarrow$ set $I_{D7} = I_{D6}$

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Sedra 9.2 contin-

$$\Rightarrow I_{D6} = I_{D7}$$

$$\frac{(W/L)_6}{(W/L)_4}\,\frac{I}{2} = \frac{(W/L)_7}{(W/L)_5}\, I$$

$$\frac{(W/L)_6}{(W/L)_4} = 2\,\frac{(W/L)_7}{(W/L)_5}$$

to cancel systematic output DC offset

In the question,

$$I_{D1} = \frac{0.4mA}{2} = 0.2mA$$

$$I_{D4} = I_{D1}$$

$$I_{D6} = I_{D7} = 0.4mA$$

true considering $I_{D5} = I_{D7}$

$$g_{m1} = \frac{2I_{D1}}{V_{GS1} - V_{th,p}} = \frac{2I_{D1}}{\underbrace{V_{ov}}_{\text{overdrive}}} = \frac{2 \cdot 0.2mA}{0.25V} = 1.6mS$$

$$g_{m6} = \frac{2I_{D6}}{V_{GS,6} - V_{th,n}} = \frac{2(0.4mA)}{0.25V} = 3.2mS$$

$$r_{op} = \frac{V_{A,p}}{I_D} \Rightarrow \quad r_{o2} = \frac{V_{A,p}}{0.2mA}, \quad r_{o4} = \frac{V_{A,n}}{0.2mA}$$

for PMOS transistors

(Note that $V'_{A,n}$, $V'_{A,p}$ are per Length L)

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Sedra
9.2
contin.

$$r_{o6} = \frac{V_{A,n}}{0.4mA}$$

$$r_{o7} = \frac{V_{A,p}}{0.4mA}$$

$$V_{A,n} = V'_{A,n} \cdot L = 25\,V/\mu m \cdot 0.8\,\mu m = 20V$$

$$V_{A,p} = V'_{A,p} \cdot L = 20\,V/\mu m \cdot 0.8\,\mu m = 16V$$

$$r_{o2} = \frac{16V}{0.2mA} = 80K \qquad r_{o6} = \frac{20V}{0.4mA} = 50K$$

$$r_{o4} = \frac{20V}{0.2mA} = 100K \qquad r_{o7} = \frac{16V}{0.4mA} = 40K$$

The voltage gain $A = \underbrace{A_1}_{\text{diff stage}} \underbrace{A_2}_{\text{CS stage}}$

$$= \left[-g_{m1}\left(r_{o2} // r_{o4}\right)\right] \left[-g_{m6}\left(r_{o6} // r_{o7}\right)\right]$$

Compute the numerical values.

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Sedra 9.2
contin.

unity gain amplifier

$$1 = \frac{A}{1+A\beta}$$ $\Rightarrow$ A is known.
compute $(1+A\beta)$, the improvement factor.

R_{out} of the opamp $= r_{o6} // r_{o7}$

$R_{out,f}$ of the unity gain ampli $= \dfrac{r_{o6}//r_{o7}}{1+A\beta}$ $\Rightarrow$ compute numerical values

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