GTU
Electronics Engineering

ELEC 331
Electronic Circuits 2

Fall Semester

Instructor: Assist. Prof. Önder Şuvak

HW 3
Questions

Updated October 20, 2017 - 13:38

Assigned:

Due:

Answers Out:

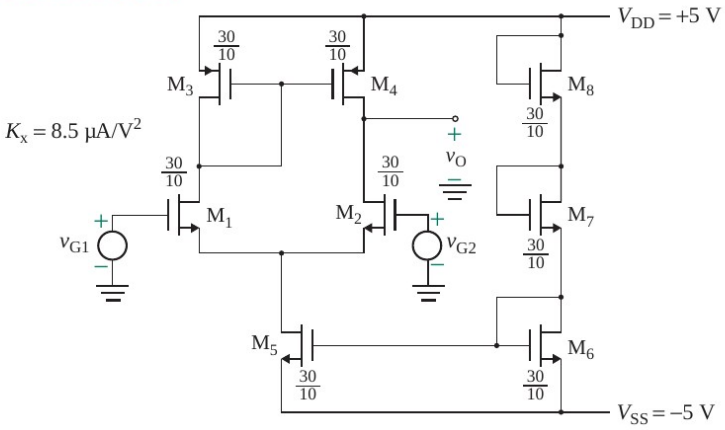
Late Due:

Contents

CMOS Differential Amplifier with Active Load

9.14 A CMOS amplifier is shown in Fig. P9.14. The parameters for the NMOS are $V_t = +2$ V, $V_M = -40$ V, and $V_{GS} = +4$ V at $I_D = 1$ mA; the parameters for the PMOS are $V_t = -3$ V, $V_M = 40$ V, and $V_{GS} = -6$ V at $I_D = 1$ mA. Calculate **(a)** A_d, A_c, and CMRR and **(b)** R_{id} and R_{ic}.

FIGURE P9.14

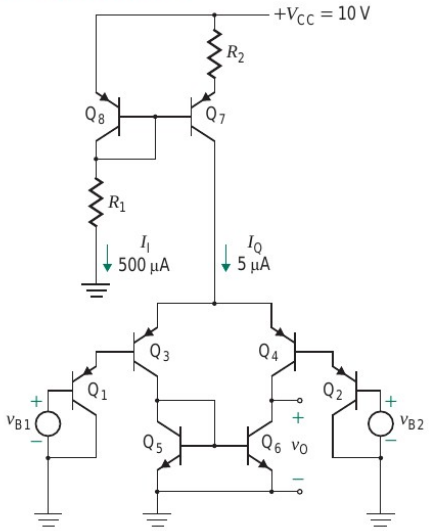


Necessary Knowledge and Skills: MOS differential amplifier, MOS active load, MOS current source, MOS nonlinear resistors (diode connected MOS), DC bias, voltage gain computation with active load, single ended amplifier with voltage gain the same as that of the fully differential amplifier, MOS small signal equivalent model, output impedance calculations.

BJT Differential Amplifier with Active Load

9.42 (P) A differential amplifier is shown in Fig. P9.42. The transistors are identical. Assume $V_{BE} = 0.7$ V, $V_T = 26$ mV, $\beta_{F(npn)} = 100$, $\beta_{F(pnp)} = 50$, $V_A = 40$ V, and $V_{CC} = 10$ V. Calculate the values of R_1, R_2, A_d, R_{id}, A_c, R_{ic}, and CMRR.

FIGURE P9.42

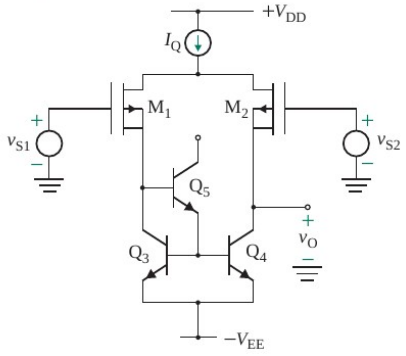


Necessary Knowledge and Skills: BJT input stages for BJT differential amplifier (for higher input impedance), BJT differential amplifier with current mirror active load, Widlar current source for tail current, single ended amplifier with the same gain as that of the fully differential amplifier, small signal equivalent model for BJT, voltage gain computations, input/output impedance computations.

PMOS Differential Amplifier with NPN BJT Active Load

9.47 A BiCMOS amplifier is shown in Fig. P9.47. The PMOS parameters are $V_t = -3$ V and $V_{GS} = -6$ V at $I_D = 1$ mA. The BJT parameters are $\beta_{F(npn)} = 100$, $\beta_{F(pnp)} = 50$, and $V_A = 40$ V. Assume $V_{DD} = -V_{EE} = 15$ V and $I_Q = 200$ μA. Calculate A_d, A_c, and CMRR.

FIGURE P9.47



Necessary Knowledge and Skills: PMOS differential amplifier, ideal current source for tail current, BJT current mirror for active load, smaller base current drawn by Q5 from the reference current at the expense of higher power and another VBE loss, single ended amplifier with a voltage gain the same as that of the fully differential amplifier, MOS and BJT small signal equivalent models, voltage gain and input/output impedance computations.

Extra Tasks: Point out the error in the schematic.

CMOS Differential Amplifier

68. Calculate the common-mode gain of the circuit depicted in Fig. 10.87. Assume $\lambda > 0$, $g_m r_O \gg 1$, and use the relationship $A_v = -G_m R_{out}$.

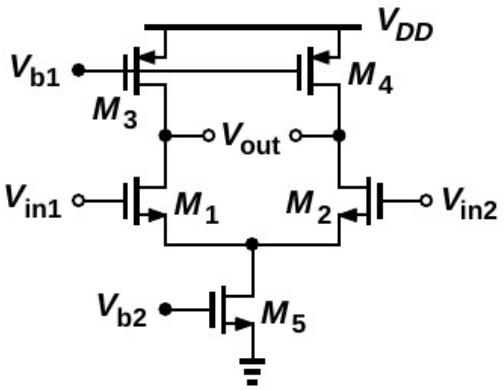


Figure 10.87

Necessary Knowledge and Skills: MOS differential amplifier, high impedance drain connections for load, single MOS transistor M5 for providing tail current, common mode gain computation, input/output impedance computation.

BJT Differential Amplifier

81. The differential pair depicted in Fig. 10.95 must provide a gain of 5 and a power budget of 4

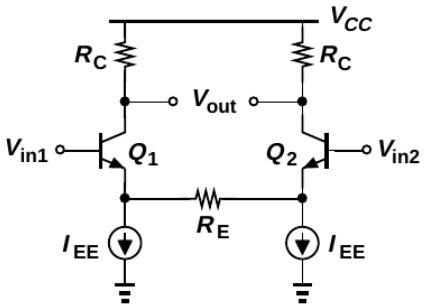


Figure 10.95

mW. Moreover, the gain of the circuit must change by less than 2% if the collector current of either transistor changes by 10%. Assuming $V_{CC} = 2.5$ V and $V_A = \infty$, design the circuit. (Hint: a 10% change in I_C leads to a 10% change in g_m.)

Necessary Knowledge and Skills: BJT differential amplifier with two tail currents, resistor loads, sensitivity computation, differential gain calculation, input/output impedance calculations, power budget in DC, design question.

BJT Differential Amplifier

7.38 Find the voltage gain and input resistance of the amplifier in Fig. P7.38 assuming that $\beta = 100$.

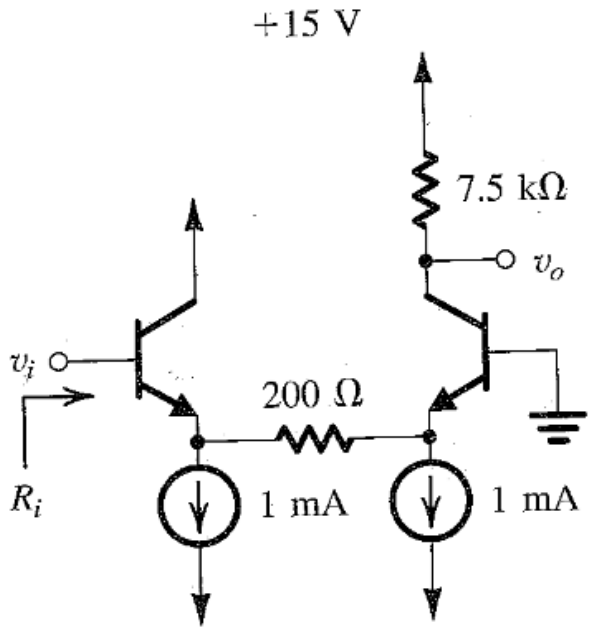


FIGURE P7.38

Necessary Knowledge and Skills: Cascaded amplifiers, common collector (emitter follower) followed by common base, input/output impedance computations, voltage gain calculations.

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