LG Electronics

LG4572B Datasheet

Mobile Display Driver IC
for a 16M-Color WVGA TFT LCD Panel with Graphic RAM

Version 1.0.2
2010-07-08

1 General Description

The LG4572B is a 16M color one-chip controller driver LSI for a-Si TFT liquid crystal display with supporting various resolutions of Max. 480RGB x 864 dots GIP[1] panel. The driver supports MIPI[2] DBI[3] Type B (8-bit). And it supports DPI[4] (VSYNC, HSYNC, PCLK, DE, and DB[23:0]) as for moving picture interface. The driver also supports MIPI DSI[5] with D-Phy interface for high-speed and low power transmission in both directions with low EMI noise. MDDI[6] is also supported by LG4572B.

The LG4572B supports dot inversion for higher image quality and moving flicker free image realizations with low power driving.

The LG4572B also supports BLU[7] control functionality by analyzing the display data properties and it helps to get lower power consumptions without image losses.

The LG4572B can operate with low I/O interface power supply down to 1.65V, with an incorporated voltage follower circuit to generate voltage levels for driving an LCD. The driver also supports functions such as 8-color displays and shut down. And these features make the LG4572B an ideal LCD driver for medium or small sized portable products supporting WWW full browsers such as smart phones or PDAs, where long battery life is a major concern.

Notice 1 : The MDDI interface supported by the LG4572B is designed and produced based on the licensing of technology from Qualcom. The MDDI interface can be adopted in the module, which incorporates a Qualcom's CDMA ASIC. Any claims, including, but not limited to the third party's right to use the MDDI interface for industrial purposes shall not be accepted by LGE.

Notice 2 : The information contained here is subject to change without notice.

The information contained here is presented only as a guide for the applications of our products. LG is not responsible for any infringement of patents or other rights of third parties that may result from the use of LG products, and the use of LG products is without any right to indemnification, or defense to any allegation of, infringement of intellectual property rights of others. No license is granted by implication of otherwise under any patent or patent rights of LG or others and by accepting possession of any LG product user acknowledges that no rights to the patents of LG or others are transferred with such product and that a separate license from LG or others may be necessary.

These LG products are intended for the exclusive use of general electronic equipment (i.e.: office equipment, communication equipment, measuring equipment, domestic electrification, etc.).

Please make sure that you consult us before you use any LG products or equipment that require special uses or exceptional applications and any equipment that may impact the welfare of human life (i.e.: atomic energy control, airplane, spaceship, traffic signal, combustion control, all types of safety devices, etc.). LG is not liable for any damage that may occur by the improper use of the equipment without consulting LG prior to its use.

Purchased LG I2C components. under the license of Philips I2C Patent Rights must be used only for an I2C system – provided that the system conforms to the I2C Standard Specification as defined by Philips.

---

[1] GIP – Gate In Panel
[2] MIPI – Mobile Industrial Processor Interface
[3] DBI – Display Bus Interface
[4] DPI – Display Pixel Interface
[5] DSI – Display Serial Interface
[6] MDDI – Mobile Display Digital Interface
[7] BLU – Backlight Unit

2 Features

- A single-chip controller driver incorporating a GIP gate circuit and a power supply circuit for maximum 480RGB x 864 dots graphics display on a-Si TFT panel in 16M colors. It supports 4N row resolutions of gate outputs in panel. In case of 854 row resolution, it is not divided by 4. But 856 row resolution could be chosen to support 854 row resolution by using dummy 2 rows.
- System interface

  Frame Buffer Mode
  - MIPI DBI Type B (8-, 9-, 16-, 18-, 24bit).
  - MIPI DSI with D-Phy (DSI : Version 1.01.00 – 21 February 2008, D-Phy : Version 0.90.00 – 8 October 2007)
  - MDDI (Mobile Display Digital Interface) V1.2

  Frame Buffer Bypass Mode
  - MIPI DPI (VSYNC, HSYNC, PCLK, DE, and DB[23:0])
  - MIPI DSI with D-Phy (DSI: Version 1.01.00 – 21 February 2008, D-PHY: Version 0.90.00 – 8 October 2007)
  - SPI
- In frame buffer mode, arbitrary number of source channels can be chosen, which is less than 480RGB, by using window mode . The unused source outputs are made floating. But, in frame buffer bypass mode, 240RGB, 320RGB, 360RGB and 480RGB source channels could be chosen for some applications. And the unused source outputs are made floating.
- Window address function to specify a rectangular area in the internal RAM to write data.
- Abundant color display and drawing functions
  - Programmable gamma correction function for 16M color display
  - Partial display function
- N-line dot inversion and column inversion, where N can be 1,2, and 3.
- Internal R, G, B independent gamma reference voltages generation function
- Contents Adaptive BLU control function for optimal power consumption
- Cst structure is only supported.
- Reversible source output shift direction by internal register setting
- Internal level shifter for GIP gate controls
- Internal power supply generations. The DC-DC charge pumping circuitry and PFM Booster with external inductor and external NMOS transistors are used.
- Internal NVM (Nonvolatile Memory) for VCOM level adjustment : 7bits x 4
- Low power consumption architecture
  - Standby function (Logic VDD is alived)
  - Deep standby function (Logic VDD is dead to be 0-volt)
- Input power supply voltage ranges
  - Interface power supply: IOVCC = 1.65 to 3.3V
  - Power supply for VDD generation: VCC = 2.6 to 3.3V
    But make sure that internally-generated logic voltage (VDD) will not exceed 1.70V
  - Analog power supply : VCI = 2.6 to 3.3V
    But make sure that Max. voltage difference of VGH and LVGL will not exceed 29.5V
- Generated power supply voltage ranges
  - Logic VDD voltage : 1.40 to 1.70V
  - Source driver power supply positive voltage : DDVDH = 4.5 to 5.5V
  - Source driver power supply negative voltage : DDVDL= -4.0 to -5.0V
  - Gate on voltage : VGH
  - Gate off voltage : VGL
  - GIP most negative reference voltage : LVGL (VGL-VCI)
  - VGH-LVGL < 29.5V, VGH-GND < 15V (Absolute Maximum)
  - VCOM voltage : 0V, -0.5V ~ -3.5V

3 Block Diagram

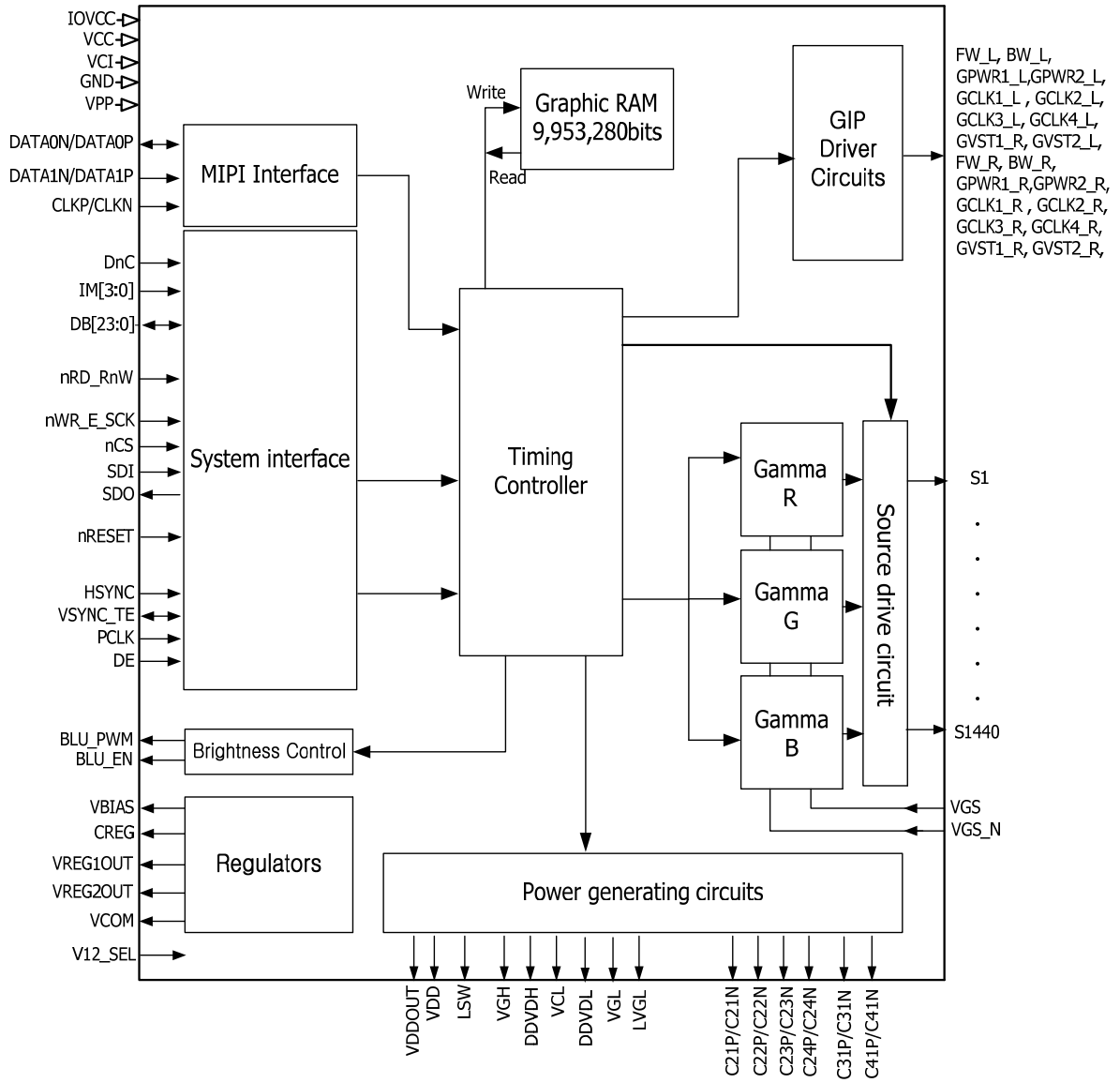


Figure 1. LG4572B Block Diagram

4 Pin Description

4.1 Pin List

<table>
<tr><th>Name</th><th># pins</th><th>I/O</th><th>Connected to</th><th>Function</th></tr>
<tr><td rowspan="14">IM3
IM2
IM1
IM0(ID)</td><td rowspan="14">4</td><td rowspan="14">I</td><td rowspan="14">MPU</td><td>MPU interface mode selection signal
<table>
<tr><th>IM[3:0]</th><th>Register Access</th><th>Pixel Data</th></tr>
<tr><td>0000</td><td rowspan="4">MIPI DBI Type A
(M68)</td><td>16</td></tr>
<tr><td>0001</td><td>8</td></tr>
<tr><td>1000</td><td>18/24</td></tr>
<tr><td>1001</td><td>9</td></tr>
<tr><td>0010</td><td rowspan="4">MIPI DBI Type B
(I80)</td><td>16</td></tr>
<tr><td>0011</td><td>8</td></tr>
<tr><td>1010</td><td>18/24</td></tr>
<tr><td>1011</td><td>9</td></tr>
<tr><td>0100</td><td rowspan="2">MIPI DBI Type C</td><td>MIPI DPI</td></tr>
<tr><td>0101</td><td>MIPI DSI
(only for PHY 2 Lane is available)</td></tr>
<tr><td>110X</td><td>SPI</td><td>MIPI DPI</td></tr>
<tr><td>0110</td><td colspan="2">MIPI DSI with PHY 1 Lane</td></tr>
<tr><td>0111</td><td colspan="2">MIPI DSI with PHY 2 Lane</td></tr>
<tr><td>111X</td><td colspan="2">MDDI</td></tr>
</table></td></tr>
<tr><td>nRESET</td><td>1</td><td>I</td><td>MPU or external RC circuit</td><td>Reset pin (active low)
Be sure to execute a power-on reset after supplying power.</td></tr>
<tr><td>nCS</td><td>1</td><td>I</td><td>MPU</td><td>Chip select (active low)
This pin should be connected to IOVCC when MIPI or MDDI I/Fs are used.</td></tr>
<tr><td>DnC</td><td>1</td><td>I</td><td>MPU</td><td>Data (1) or command (0) select</td></tr>
<tr><td>DB[23:0]</td><td>24</td><td>I/O</td><td>MPU</td><td>Parallel data bus
Unused pins must be fixed either IOVCC or GND level.</td></tr>
<tr><td>nRD_RnW</td><td>1</td><td>I</td><td>MPU</td><td>(I80 interface) nRD - Read strobe (active low)
(M68 interface) RnW - Read (1) or write (0) select</td></tr>
<tr><td>nWR_E_SCK</td><td>1</td><td>I</td><td>MPU</td><td>(I80 interface) nWR - Write strobe (active low)
(M68 interface) E - Enable
(SPI interface) SCK - Serial clock</td></tr>
<tr><td>SDI</td><td>1</td><td>I</td><td>MPU</td><td>(SPI interface) Serial data input</td></tr>
<tr><td>SDO</td><td>1</td><td>O</td><td>MPU</td><td>(SPI interface) Serial data output</td></tr>
<tr><td>PCLK</td><td>1</td><td>I</td><td>MPU</td><td>Pixel clock</td></tr>
<tr><td>VSYNC_TE</td><td>1</td><td>I/O</td><td>MPU</td><td>Frame synchronization signal.
It is Vsync input pin when MIPI DPI pixel data interface mode, but it turns out to be output pin in other modes for TE (Tearing Effect) signaling.</td></tr>
<tr><td>HSYNC</td><td>1</td><td>I</td><td>MPU</td><td>Line synchronization signal.
It is Vsync input pin when DPI pixel data interface mode.
Fix to either IOVCC or GND level when not in use.</td></tr>
</table>

Name	# pins	I/O	Connected to	Function
DE	1	I	MPU	Data enable signal in RGB interface mode. Fix to either IOVCC or GND level when not in use.
CLKN, CLKP	2	I	MPU	Differential clock or strobe pair for MIPI and/or MDDI high speed serial interface. If MIPI and/or MDDI were not used, they should be connected to GND. In MDDI Interface mode, precision 100ohm resistor should be connected between CLKN and CLKP.
DATA0N, DATA1N, DATA0P, DATA1P	4	I/O	MPU	Differential data pairs for MIPI and/or high seep serial interface. If MIPI and/or MDDI were not used, they should be connected to GND. In MDDI Interface mode, precision 100ohm resistors should be connected between DATAN0 and DATAP0, and between DATAN1 and DATAP1.
V12_SEL	1	I	IOVCC or GND	When VCI<2.9V, then V12_SEL=GND is recommended. When VCI>2.9V, then V12_SEL=IOVCC is recommended. This pin is only for MIPI interface. This pin should not be floating in any case.
TEST1	1	I	GND	Test pin Fix to GND level in normal operation mode
TEST2	1	I	GND	Test pin Fix to GND level in normal operation mode
BLU_EN	1	O	BLU	BLU enable (active High) If not used, leave this pin open
BLU_PWM	1	O	BLU	BLU PWM signal (depends on PWMP in C8h register: 0 → active High, 1 → active Low) If not used, leave this pin open
S1 to S1440	1440	O	LCD	Source driver outputs
FW_L, BW_L, GCLK#_L, GVST1_L, GVST2_L Where #=1,2,3,4	8	O	GIP	Signals for right side GIP on panel view (Left side in IC bump view) Unused pins should be left open.
FW_R, BW_R, GCLK#_R, GVST1_R, GVST2_R Where #=1,2,3,4	8	O	GIP	Signals for Right side GIP on panel view (Right side in IC bump view) Unused pins should be left open.
VBIAS	1	O	GIP	Bias voltage for some special GIP circuits. If not used, leave this pin open.
LVGL	1	I	GIP	Most negative voltage for some special GIP circuits. If not used, connect to VGL
VGL	1	I		A supply voltage to drive gate lines of the TFT panel.
VGH	1	I		A supply voltage to drive gate lines of the TFT panel.
DDVDL	1	I		Power supply for the source driver's LCD output unit

Name	# pins	I/O	Connected to	Function
DDVDH	1	I		Power supply for the source driver's LCD output unit and an input voltage to generate DDVDL voltage.
VCL	1	I		Power supply voltage for the level shifter circuits.
IOVCC	1	I	Power supply	Power supply to the interface pins: IOVCC = 1.65 to 3.3V.
VCC	1	I	Power supply	Power supply to generate the internal logic power supply VDD. VCC = 2.6 to 3.3V
VDD	1	I	Power supply	Generated power supply for the internal logic.
VDDOUT	1	I/O	Stabilizing capacitor and VDD	Internal logic regulator output. Connect VDD to a stabilizing capacitor.
VSS	1	I	Power supply	VSS=0.
VCI	1	I	Power supply	Supply voltage to the analog circuit. Connect to an external power supply of 2.6 to 3.3V.
VCOM	1	O	TFT panel common electrode	Supply voltage to the common electrode of TFT panel.
VCOMR	1	I	Variable resistor or open	Reference level to generate the VCOM level with an externally connected variable resistor. The VREG2OUT voltage could be a reference to generate VCOMR. Leave it open when not in use.
CREG	1	O	Stabilizing capacitor	Regulator output that needs to be connected with stabilizing capacitor for MIPI block. Leave it open when MIPI were not used.
GND_SH	1	I	GND	GND. This is for shielding differential clock and data signals for MIPI DSI or MDDI.
LSW	1	O	Gate terminal of external switching Tr.	External switching transistor's gate on/off control signal for the switching regulator type DC-DC converter to make DDVDH and/or DDVDL. Leave it open when not in use.
VGS	1	I	GND or external resistor	Reference level for the positive grayscale voltage generation circuit. The VGS level can be changed by connecting to an external resistor.
VGS_N	1	I	GND or external resistor	Reference level for the negative grayscale voltage generation circuit. The VGS_N level can be changed by connecting to an external resistor.
VREG1OUT	1	O	Stabilizing capacitor	VREG1OUT is a positive source driver grayscale reference voltage.
VREG2OUT	1	O	Stabilizing capacitor	VREG2OUT is a negative source driver grayscale reference voltage.
C21N, C21P C22N, C22P C23N, C23P C24N, C24P	8	I/O	Step-up capacitor	Connect step-up capacitors to generate VGH, VGL, and VCL. Leave them open when not in use.

Name	# pins	I/O	Connected to	Function
C31N, C31P	2	I/O	Step-up capacitor	Connect step-up capacitor to generate DDVDL when charge pumping method is used instead of diode-inverting. When DDVDH is supplied externally, this capacitor is necessary to generate DDVDL. Leave them open when not in use.
C41N, C41P	2	I/O	Step-up capacitor	Connect step-up capacitor to generate LVGL only for H-type panel. Leave them open when not in use.
VPP	1	I		7.75V power supply for internal OTP programming to adjust VCOM level. Leave this pin open except when OTP programming.
GOUT_TEST1, GOUT_TEST2	2		DUMMY	Dummy pads only with bump
DUM_VON	1		DUMMY	Dummy pad only with bump
DUM_DATA1, DUM_DATA2	2		DUMMY	Dummy pads only with bump They are shorted together.
DUM_GOUT	1		DUMMY	Dummy pads only with bump
OSC1,2,3	3	I/O	External resistor or capacitor	Reserved Pins for external R and C combined oscillation frequencies. They can be used to get higher and more stable oscillation frequencies.
RSDA	1	I/O	External resistor to IOVCC	Around 10kohm resistor can be connected in-between RSDA and IOVCC when I2C interface is activated by setting EEPROM=1.
RSCL	1	I/O		Reading clock to fetch register values from external EEPROM. It should not exceed 400kHz at maximum.

4.2 Pin Assignment

- Chip size : 22.35 x 1.45 mm2
  (With seal ring but without scribe line)
- Chip thickness : 250um
- PAD Coordination : PAD center
- Coordination Origin : Chip center

- Au BUMP size

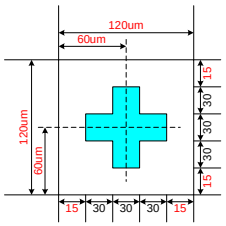
(1) 50.00um x 80.00um
No.1 ~ No.312

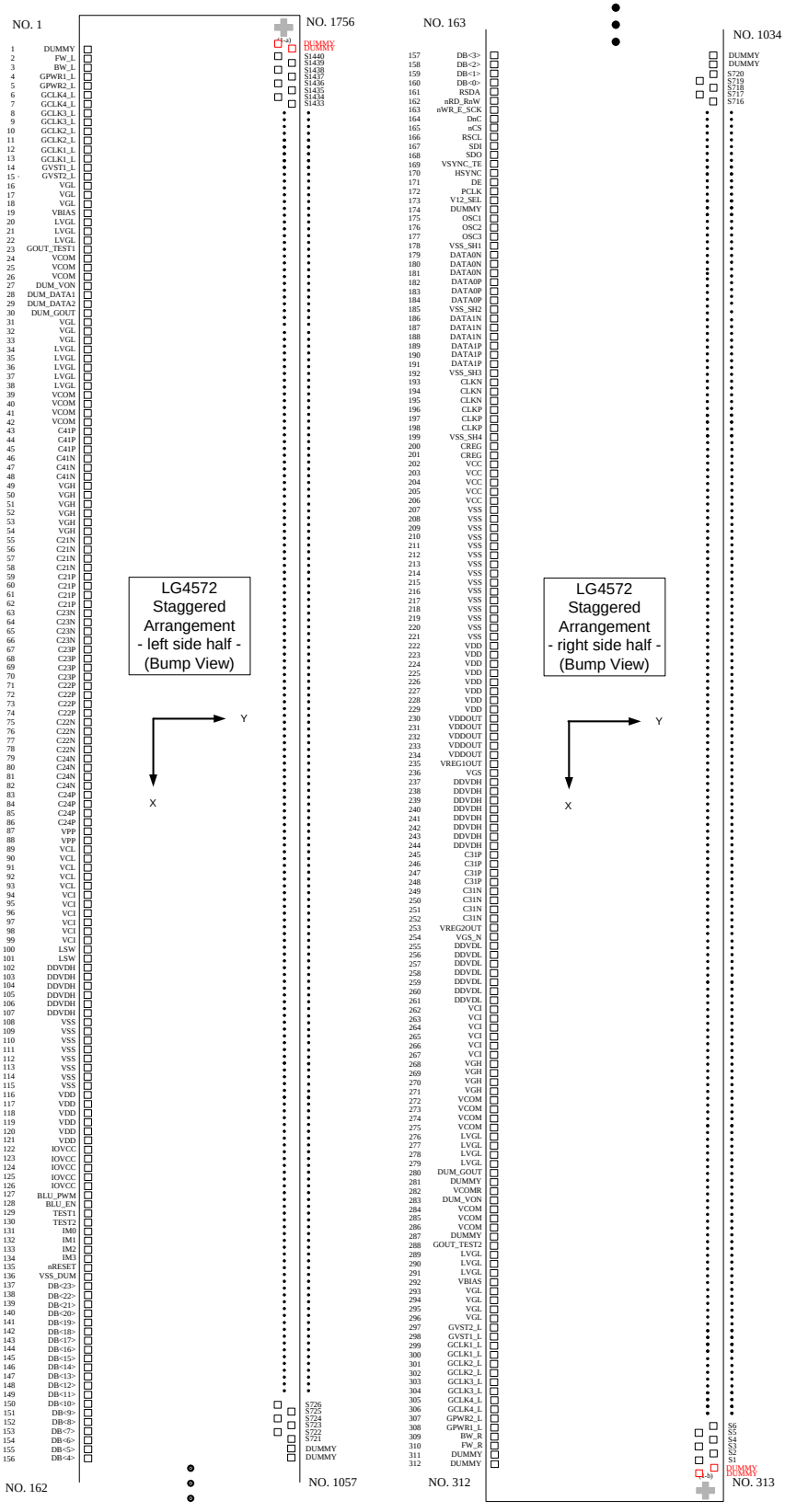
(2) 15.0um x 100.0um
No.313 ~ No.1756

- Au BUMP pitch : 15um for staggered pads and 70um for in-line pads
- Au BUMP height : 12um(typ.)
- No. in the figure corresponds to No. in the PAD coordination Table

- Alignment mark

Alignment mark	X	Y
1-a	-11060	600
1-b	11060	600





4.3 Bump Coordinates

No.	Name	X	Y
1	DUMMY	-10885	-672
2	FW_L	-10815	-672
3	BW_L	-10745	-672
4	GPWR1_L	-10675	-672
5	GPWR2_L	-10605	-672
6	GCLK4_L	-10535	-672
7	GCLK4_L	-10465	-672
8	GCLK3_L	-10395	-672
9	GCLK3_L	-10325	-672
10	GCLK2_L	-10255	-672
11	GCLK2_L	-10185	-672
12	GCLK1_L	-10115	-672
13	GCLK1_L	-10045	-672
14	GVST1_L	-9975	-672
15	GVST2_L	-9905	-672
16	VGL	-9835	-672
17	VGL	-9765	-672
18	VGL	-9695	-672
19	VBIAS	-9625	-672
20	LVGL	-9555	-672
21	LVGL	-9485	-672
22	LVGL	-9415	-672
23	GOUT_TEST1	-9345	-672
24	VCOM	-9275	-672
25	VCOM	-9205	-672
26	VCOM	-9135	-672
27	DUM_VON	-9065	-672
28	DUM_DATA1	-8995	-672
29	DUM_DATA2	-8925	-672
30	DUM_GOUT	-8855	-672
31	VGL	-8785	-672
32	VGL	-8715	-672
33	VGL	-8645	-672
34	LVGL	-8575	-672
35	LVGL	-8505	-672
36	LVGL	-8435	-672
37	LVGL	-8365	-672
38	LVGL	-8295	-672
39	VCOM	-8225	-672
40	VCOM	-8155	-672
41	VCOM	-8085	-672
42	VCOM	-8015	-672
43	C41P	-7945	-672
44	C41P	-7875	-672
45	C41P	-7805	-672
46	C41N	-7735	-672
47	C41N	-7665	-672
48	C41N	-7595	-672
49	VGH	-7525	-672
50	VGH	-7455	-672
51	VGH	-7385	-672
52	VGH	-7315	-672
53	VGH	-7245	-672
54	VGH	-7175	-672
55	C21N	-7105	-672
56	C21N	-7035	-672
57	C21N	-6965	-672
58	C21N	-6895	-672
59	C21P	-6825	-672
60	C21P	-6755	-672
61	C21P	-6685	-672
62	C21P	-6615	-672
63	C23N	-6545	-672
64	C23N	-6475	-672
65	C23N	-6405	-672
66	C23N	-6335	-672
67	C23P	-6265	-672
68	C23P	-6195	-672
69	C23P	-6125	-672
70	C23P	-6055	-672
71	C22P	-5985	-672
72	C22P	-5915	-672
73	C22P	-5845	-672
74	C22P	-5775	-672
75	C22N	-5705	-672
76	C22N	-5635	-672
77	C22N	-5565	-672
78	C22N	-5495	-672
79	C24N	-5425	-672
80	C24N	-5355	-672
81	C24N	-5285	-672
82	C24N	-5215	-672
83	C24P	-5145	-672
84	C24P	-5075	-672
85	C24P	-5005	-672
86	C24P	-4935	-672
87	VPP	-4865	-672
88	VPP	-4795	-672
89	VCL	-4725	-672
90	VCL	-4655	-672
91	VCL	-4585	-672
92	VCL	-4515	-672
93	VCL	-4445	-672
94	VCI	-4375	-672
95	VCI	-4305	-672
96	VCI	-4235	-672
97	VCI	-4165	-672
98	VCI	-4095	-672
99	VCI	-4025	-672
100	LSW	-3955	-672
101	LSW	-3885	-672
102	DDVDH	-3815	-672
103	DDVDH	-3745	-672
104	DDVDH	-3675	-672
105	DDVDH	-3605	-672
106	DDVDH	-3535	-672
107	DDVDH	-3465	-672
108	VSS	-3395	-672
109	VSS	-3325	-672
110	VSS	-3255	-672
111	VSS	-3185	-672
112	VSS	-3115	-672
113	VSS	-3045	-672
114	VSS	-2975	-672
115	VSS	-2905	-672
116	VDD	-2835	-672
117	VDD	-2765	-672
118	VDD	-2695	-672
119	VDD	-2625	-672
120	VDD	-2555	-672
121	VDD	-2485	-672
122	IOVCC	-2415	-672
123	IOVCC	-2345	-672
124	IOVCC	-2275	-672
125	IOVCC	-2205	-672
126	IOVCC	-2135	-672
127	BLU_PWM	-2065	-672
128	BLU_EN	-1995	-672
129	TEST1	-1925	-672
130	TEST2	-1855	-672
131	IM0	-1785	-672
132	IM1	-1715	-672
133	IM2	-1645	-672
134	IM3	-1575	-672
135	nRESET	-1505	-672
136	VSS_DUM	-1435	-672
137	DB<23>	-1365	-672
138	DB<22>	-1295	-672
139	DB<21>	-1225	-672
140	DB<20>	-1155	-672
141	DB<19>	-1085	-672
142	DB<18>	-1015	-672
143	DB<17>	-945	-672
144	DB<16>	-875	-672
145	DB<15>	-805	-672
146	DB<14>	-735	-672
147	DB<13>	-665	-672
148	DB<12>	-595	-672
149	DB<11>	-525	-672
150	DB<10>	-455	-672

No.	Name	X	Y
151	DB<9>	-385	-672
152	DB<8>	-315	-672
153	DB<7>	-245	-672
154	DB<6>	-175	-672
155	DB<5>	-105	-672
156	DB<4>	-35	-672
157	DB<3>	35	-672
158	DB<2>	105	-672
159	DB<1>	175	-672
160	DB<0>	245	-672
161	**RSDA**	315	-672
162	nRD_RnW	385	-672
163	nWR_E_SCK	455	-672
164	DnC	525	-672
165	nCS	595	-672
166	**RSCL**	665	-672
167	SDI	735	-672
168	SDO	805	-672
169	VSYNC_TE	875	-672
170	HSYNC	945	-672
171	DE	1015	-672
172	PCLK	1085	-672
173	V12_SEL	1155	-672
174	DUMMY	1225	-672
175	OSC1	1295	-672
176	OSC2	1365	-672
177	OSC3	1435	-672
178	VSS_SH1	1505	-672
179	DATA0N	1575	-672
180	DATA0N	1645	-672
181	DATA0N	1715	-672
182	DATA0P	1785	-672
183	DATA0P	1855	-672
184	DATA0P	1925	-672
185	VSS_SH2	1995	-672
186	DATA1N	2065	-672
187	DATA1N	2135	-672
188	DATA1N	2205	-672
189	DATA1P	2275	-672
190	DATA1P	2345	-672
191	DATA1P	2415	-672
192	VSS_SH3	2485	-672
193	CLKN	2555	-672
194	CLKN	2625	-672
195	CLKN	2695	-672
196	CLKP	2765	-672
197	CLKP	2835	-672
198	CLKP	2905	-672
199	VSS_SH4	2975	-672
200	CREG	3045	-672
201	CREG	3115	-672
202	VCC	3185	-672
203	VCC	3255	-672
204	VCC	3325	-672
205	VCC	3395	-672
206	VCC	3465	-672
207	VSS	3535	-672
208	VSS	3605	-672
209	VSS	3675	-672
210	VSS	3745	-672
211	VSS	3815	-672
212	VSS	3885	-672
213	VSS	3955	-672
214	VSS	4025	-672
215	VSS	4095	-672
216	VSS	4165	-672
217	VSS	4235	-672
218	VSS	4305	-672
219	VSS	4375	-672
220	VSS	4445	-672
221	VSS	4515	-672
222	VDD	4585	-672
223	VDD	4655	-672
224	VDD	4725	-672
225	VDD	4795	-672
226	VDD	4865	-672
227	VDD	4935	-672
228	VDD	5005	-672
229	VDD	5075	-672
230	VDDOUT	5145	-672
231	VDDOUT	5215	-672
232	VDDOUT	5285	-672
233	VDDOUT	5355	-672
234	VDDOUT	5425	-672
235	VREG1OUT	5495	-672
236	VGS	5565	-672
237	DDVDH	5635	-672
238	DDVDH	5705	-672
239	DDVDH	5775	-672
240	DDVDH	5845	-672
241	DDVDH	5915	-672
242	DDVDH	5985	-672
243	DDVDH	6055	-672
244	DDVDH	6125	-672
245	C31P	6195	-672
246	C31P	6265	-672
247	C31P	6335	-672
248	C31P	6405	-672
249	C31N	6475	-672
250	C31N	6545	-672
251	C31N	6615	-672
252	C31N	6685	-672
253	VREG2OUT	6755	-672
254	VGS_N	6825	-672
255	DDVDL	6895	-672
256	DDVDL	6965	-672
257	DDVDL	7035	-672
258	DDVDL	7105	-672
259	DDVDL	7175	-672
260	DDVDL	7245	-672
261	DDVDL	7315	-672
262	VCI	7385	-672
263	VCI	7455	-672
264	VCI	7525	-672
265	VCI	7595	-672
266	VCI	7665	-672
267	VCI	7735	-672
268	VGH	7805	-672
269	VGH	7875	-672
270	VGH	7945	-672
271	VGH	8015	-672
272	VCOM	8085	-672
273	VCOM	8155	-672
274	VCOM	8225	-672
275	VCOM	8295	-672
276	LVGL	8365	-672
277	LVGL	8435	-672
278	LVGL	8505	-672
279	LVGL	8575	-672
280	DUM_GOUT	8645	-672
281	DUMMY	8715	-672
282	VCOMR	8785	-672
283	DUM_VON	8855	-672
284	VCOM	8925	-672
285	VCOM	8995	-672
286	VCOM	9065	-672
287	DUMMY	9135	-672
288	GOUT_TEST2	9205	-672
289	LVGL	9275	-672
290	LVGL	9345	-672
291	LVGL	9415	-672
292	VBIAS	9485	-672
293	VGL	9555	-672
294	VGL	9625	-672
295	VGL	9695	-672
296	VGL	9765	-672
297	GVST2_R	9835	-672
298	GVST1_R	9905	-672
299	GCLK1_R	9975	-672
300	GCLK1_R	10045	-672
301	GCLK2_R	10115	-672
302	GCLK2_R	10185	-672
303	GCLK3_R	10255	-672
304	GCLK3_R	10325	-672
305	GCLK4_R	10395	-672
306	GCLK4_R	10465	-672
307	GPWR2_R	10535	-672
308	GPWR1_R	10605	-672
309	BW_R	10675	-672

No.	Name	X	Y
310	FW_R	10745	-672
311	DUMMY	10815	-672
312	DUMMY	10885	-672
	DUMMY	**10950**	**500**
	DUMMY	**10935**	**613**
313	S1	10920	500
314	S2	10905	613
315	S3	10890	500
316	S4	10875	613
317	S5	10860	500
318	S6	10845	613
319	S7	10830	500
320	S8	10815	613
321	S9	10800	500
322	S10	10785	613
323	S11	10770	500
324	S12	10755	613
325	S13	10740	500
326	S14	10725	613
327	S15	10710	500
328	S16	10695	613
329	S17	10680	500
330	S18	10665	613
331	S19	10650	500
332	S20	10635	613
333	S21	10620	500
334	S22	10605	613
335	S23	10590	500
336	S24	10575	613
337	S25	10560	500
338	S26	10545	613
339	S27	10530	500
340	S28	10515	613
341	S29	10500	500
342	S30	10485	613
343	S31	10470	500
344	S32	10455	613
345	S33	10440	500
346	S34	10425	613
347	S35	10410	500
348	S36	10395	613
349	S37	10380	500
350	S38	10365	613
351	S39	10350	500
352	S40	10335	613
353	S41	10320	500
354	S42	10305	613
355	S43	10290	500
356	S44	10275	613
357	S45	10260	500
358	S46	10245	613
359	S47	10230	500
360	S48	10215	613

No.	Name	X	Y
361	S49	10200	500
362	S50	10185	613
363	S51	10170	500
364	S52	10155	613
365	S53	10140	500
366	S54	10125	613
367	S55	10110	500
368	S56	10095	613
369	S57	10080	500
370	S58	10065	613
371	S59	10050	500
372	S60	10035	613
373	S61	10020	500
374	S62	10005	613
375	S63	9990	500
376	S64	9975	613
377	S65	9960	500
378	S66	9945	613
379	S67	9930	500
380	S68	9915	613
381	S69	9900	500
382	S70	9885	613
383	S71	9870	500
384	S72	9855	613
385	S73	9840	500
386	S74	9825	613
387	S75	9810	500
388	S76	9795	613
389	S77	9780	500
390	S78	9765	613
391	S79	9750	500
392	S80	9735	613
393	S81	9720	500
394	S82	9705	613
395	S83	9690	500
396	S84	9675	613
397	S85	9660	500
398	S86	9645	613
399	S87	9630	500
400	S88	9615	613
401	S89	9600	500
402	S90	9585	613
403	S91	9570	500
404	S92	9555	613
405	S93	9540	500
406	S94	9525	613
407	S95	9510	500
408	S96	9495	613
409	S97	9480	500
410	S98	9465	613
411	S99	9450	500
412	S100	9435	613
413	S101	9420	500

No.	Name	X	Y
414	S102	9405	613
415	S103	9390	500
416	S104	9375	613
417	S105	9360	500
418	S106	9345	613
419	S107	9330	500
420	S108	9315	613
421	S109	9300	500
422	S110	9285	613
423	S111	9270	500
424	S112	9255	613
425	S113	9240	500
426	S114	9225	613
427	S115	9210	500
428	S116	9195	613
429	S117	9180	500
430	S118	9165	613
431	S119	9150	500
432	S120	9135	613
433	S121	9120	500
434	S122	9105	613
435	S123	9090	500
436	S124	9075	613
437	S125	9060	500
438	S126	9045	613
439	S127	9030	500
440	S128	9015	613
441	S129	9000	500
442	S130	8985	613
443	S131	8970	500
444	S132	8955	613
445	S133	8940	500
446	S134	8925	613
447	S135	8910	500
448	S136	8895	613
449	S137	8880	500
450	S138	8865	613
451	S139	8850	500
452	S140	8835	613
453	S141	8820	500
454	S142	8805	613
455	S143	8790	500
456	S144	8775	613
457	S145	8760	500
458	S146	8745	613
459	S147	8730	500
460	S148	8715	613
461	S149	8700	500
462	S150	8685	613
463	S151	8670	500
464	S152	8655	613
465	S153	8640	500
466	S154	8625	613

No.	Name	X	Y
467	S155	8610	500
468	S156	8595	613
469	S157	8580	500
470	S158	8565	613
471	S159	8550	500
472	S160	8535	613
473	S161	8520	500
474	S162	8505	613
475	S163	8490	500
476	S164	8475	613
477	S165	8460	500
478	S166	8445	613
479	S167	8430	500
480	S168	8415	613
481	S169	8400	500
482	S170	8385	613
483	S171	8370	500
484	S172	8355	613
485	S173	8340	500
486	S174	8325	613
487	S175	8310	500
488	S176	8295	613
489	S177	8280	500
490	S178	8265	613
491	S179	8250	500
492	S180	8235	613
493	S181	8220	500
494	S182	8205	613
495	S183	8190	500
496	S184	8175	613
497	S185	8160	500
498	S186	8145	613
499	S187	8130	500
500	S188	8115	613
501	S189	8100	500
502	S190	8085	613
503	S191	8070	500
504	S192	8055	613
505	S193	8040	500
506	S194	8025	613
507	S195	8010	500
508	S196	7995	613
509	S197	7980	500
510	S198	7965	613
511	S199	7950	500
512	S200	7935	613
513	S201	7920	500
514	S202	7905	613
515	S203	7890	500
516	S204	7875	613
517	S205	7860	500
518	S206	7845	613
519	S207	7830	500

No.	Name	X	Y
520	S208	7815	613
521	S209	7800	500
522	S210	7785	613
523	S211	7770	500
524	S212	7755	613
525	S213	7740	500
526	S214	7725	613
527	S215	7710	500
528	S216	7695	613
529	S217	7680	500
530	S218	7665	613
531	S219	7650	500
532	S220	7635	613
533	S221	7620	500
534	S222	7605	613
535	S223	7590	500
536	S224	7575	613
537	S225	7560	500
538	S226	7545	613
539	S227	7530	500
540	S228	7515	613
541	S229	7500	500
542	S230	7485	613
543	S231	7470	500
544	S232	7455	613
545	S233	7440	500
546	S234	7425	613
547	S235	7410	500
548	S236	7395	613
549	S237	7380	500
550	S238	7365	613
551	S239	7350	500
552	S240	7335	613
553	S241	7320	500
554	S242	7305	613
555	S243	7290	500
556	S244	7275	613
557	S245	7260	500
558	S246	7245	613
559	S247	7230	500
560	S248	7215	613
561	S249	7200	500
562	S250	7185	613
563	S251	7170	500
564	S252	7155	613
565	S253	7140	500
566	S254	7125	613
567	S255	7110	500
568	S256	7095	613
569	S257	7080	500
570	S258	7065	613
571	S259	7050	500
572	S260	7035	613

No.	Name	X	Y
573	S261	7020	500
574	S262	7005	613
575	S263	6990	500
576	S264	6975	613
577	S265	6960	500
578	S266	6945	613
579	S267	6930	500
580	S268	6915	613
581	S269	6900	500
582	S270	6885	613
583	S271	6870	500
584	S272	6855	613
585	S273	6840	500
586	S274	6825	613
587	S275	6810	500
588	S276	6795	613
589	S277	6780	500
590	S278	6765	613
591	S279	6750	500
592	S280	6735	613
593	S281	6720	500
594	S282	6705	613
595	S283	6690	500
596	S284	6675	613
597	S285	6660	500
598	S286	6645	613
599	S287	6630	500
600	S288	6615	613
601	S289	6600	500
602	S290	6585	613
603	S291	6570	500
604	S292	6555	613
605	S293	6540	500
606	S294	6525	613
607	S295	6510	500
608	S296	6495	613
609	S297	6480	500
610	S298	6465	613
611	S299	6450	500
612	S300	6435	613
613	S301	6420	500
614	S302	6405	613
615	S303	6390	500
616	S304	6375	613
617	S305	6360	500
618	S306	6345	613
619	S307	6330	500
620	S308	6315	613
621	S309	6300	500
622	S310	6285	613
623	S311	6270	500
624	S312	6255	613
625	S313	6240	500

No.	Name	X	Y
626	S314	6225	613
627	S315	6210	500
628	S316	6195	613
629	S317	6180	500
630	S318	6165	613
631	S319	6150	500
632	S320	6135	613
633	S321	6120	500
634	S322	6105	613
635	S323	6090	500
636	S324	6075	613
637	S325	6060	500
638	S326	6045	613
639	S327	6030	500
640	S328	6015	613
641	S329	6000	500
642	S330	5985	613
643	S331	5970	500
644	S332	5955	613
645	S333	5940	500
646	S334	5925	613
647	S335	5910	500
648	S336	5895	613
649	S337	5880	500
650	S338	5865	613
651	S339	5850	500
652	S340	5835	613
653	S341	5820	500
654	S342	5805	613
655	S343	5790	500
656	S344	5775	613
657	S345	5760	500
658	S346	5745	613
659	S347	5730	500
660	S348	5715	613
661	S349	5700	500
662	S350	5685	613
663	S351	5670	500
664	S352	5655	613
665	S353	5640	500
666	S354	5625	613
667	S355	5610	500
668	S356	5595	613
669	S357	5580	500
670	S358	5565	613
671	S359	5550	500
672	S360	5535	613
673	S361	5520	500
674	S362	5505	613
675	S363	5490	500
676	S364	5475	613
677	S365	5460	500
678	S366	5445	613

No.	Name	X	Y
679	S367	5430	500
680	S368	5415	613
681	S369	5400	500
682	S370	5385	613
683	S371	5370	500
684	S372	5355	613
685	S373	5340	500
686	S374	5325	613
687	S375	5310	500
688	S376	5295	613
689	S377	5280	500
690	S378	5265	613
691	S379	5250	500
692	S380	5235	613
693	S381	5220	500
694	S382	5205	613
695	S383	5190	500
696	S384	5175	613
697	S385	5160	500
698	S386	5145	613
699	S387	5130	500
700	S388	5115	613
701	S389	5100	500
702	S390	5085	613
703	S391	5070	500
704	S392	5055	613
705	S393	5040	500
706	S394	5025	613
707	S395	5010	500
708	S396	4995	613
709	S397	4980	500
710	S398	4965	613
711	S399	4950	500
712	S400	4935	613
713	S401	4920	500
714	S402	4905	613
715	S403	4890	500
716	S404	4875	613
717	S405	4860	500
718	S406	4845	613
719	S407	4830	500
720	S408	4815	613
721	S409	4800	500
722	S410	4785	613
723	S411	4770	500
724	S412	4755	613
725	S413	4740	500
726	S414	4725	613
727	S415	4710	500
728	S416	4695	613
729	S417	4680	500
730	S418	4665	613
731	S419	4650	500

No.	Name	X	Y
732	S420	4635	613
733	S421	4620	500
734	S422	4605	613
735	S423	4590	500
736	S424	4575	613
737	S425	4560	500
738	S426	4545	613
739	S427	4530	500
740	S428	4515	613
741	S429	4500	500
742	S430	4485	613
743	S431	4470	500
744	S432	4455	613
745	S433	4440	500
746	S434	4425	613
747	S435	4410	500
748	S436	4395	613
749	S437	4380	500
750	S438	4365	613
751	S439	4350	500
752	S440	4335	613
753	S441	4320	500
754	S442	4305	613
755	S443	4290	500
756	S444	4275	613
757	S445	4260	500
758	S446	4245	613
759	S447	4230	500
760	S448	4215	613
761	S449	4200	500
762	S450	4185	613
763	S451	4170	500
764	S452	4155	613
765	S453	4140	500
766	S454	4125	613
767	S455	4110	500
768	S456	4095	613
769	S457	4080	500
770	S458	4065	613
771	S459	4050	500
772	S460	4035	613
773	S461	4020	500
774	S462	4005	613
775	S463	3990	500
776	S464	3975	613
777	S465	3960	500
778	S466	3945	613
779	S467	3930	500
780	S468	3915	613
781	S469	3900	500
782	S470	3885	613
783	S471	3870	500
784	S472	3855	613

No.	Name	X	Y
785	S473	3840	500
786	S474	3825	613
787	S475	3810	500
788	S476	3795	613
789	S477	3780	500
790	S478	3765	613
791	S479	3750	500
792	S480	3735	613
793	S481	3720	500
794	S482	3705	613
795	S483	3690	500
796	S484	3675	613
797	S485	3660	500
798	S486	3645	613
799	S487	3630	500
800	S488	3615	613
801	S489	3600	500
802	S490	3585	613
803	S491	3570	500
804	S492	3555	613
805	S493	3540	500
806	S494	3525	613
807	S495	3510	500
808	S496	3495	613
809	S497	3480	500
810	S498	3465	613
811	S499	3450	500
812	S500	3435	613
813	S501	3420	500
814	S502	3405	613
815	S503	3390	500
816	S504	3375	613
817	S505	3360	500
818	S506	3345	613
819	S507	3330	500
820	S508	3315	613
821	S509	3300	500
822	S510	3285	613
823	S511	3270	500
824	S512	3255	613
825	S513	3240	500
826	S514	3225	613
827	S515	3210	500
828	S516	3195	613
829	S517	3180	500
830	S518	3165	613
831	S519	3150	500
832	S520	3135	613
833	S521	3120	500
834	S522	3105	613
835	S523	3090	500
836	S524	3075	613
837	S525	3060	500

No.	Name	X	Y
838	S526	3045	613
839	S527	3030	500
840	S528	3015	613
841	S529	3000	500
842	S530	2985	613
843	S531	2970	500
844	S532	2955	613
845	S533	2940	500
846	S534	2925	613
847	S535	2910	500
848	S536	2895	613
849	S537	2880	500
850	S538	2865	613
851	S539	2850	500
852	S540	2835	613
853	S541	2820	500
854	S542	2805	613
855	S543	2790	500
856	S544	2775	613
857	S545	2760	500
858	S546	2745	613
859	S547	2730	500
860	S548	2715	613
861	S549	2700	500
862	S550	2685	613
863	S551	2670	500
864	S552	2655	613
865	S553	2640	500
866	S554	2625	613
867	S555	2610	500
868	S556	2595	613
869	S557	2580	500
870	S558	2565	613
871	S559	2550	500
872	S560	2535	613
873	S561	2520	500
874	S562	2505	613
875	S563	2490	500
876	S564	2475	613
877	S565	2460	500
878	S566	2445	613
879	S567	2430	500
880	S568	2415	613
881	S569	2400	500
882	S570	2385	613
883	S571	2370	500
884	S572	2355	613
885	S573	2340	500
886	S574	2325	613
887	S575	2310	500
888	S576	2295	613
889	S577	2280	500
890	S578	2265	613

No.	Name	X	Y
891	S579	2250	500
892	S580	2235	613
893	S581	2220	500
894	S582	2205	613
895	S583	2190	500
896	S584	2175	613
897	S585	2160	500
898	S586	2145	613
899	S587	2130	500
900	S588	2115	613
901	S589	2100	500
902	S590	2085	613
903	S591	2070	500
904	S592	2055	613
905	S593	2040	500
906	S594	2025	613
907	S595	2010	500
908	S596	1995	613
909	S597	1980	500
910	S598	1965	613
911	S599	1950	500
912	S600	1935	613
913	S601	1920	500
914	S602	1905	613
915	S603	1890	500
916	S604	1875	613
917	S605	1860	500
918	S606	1845	613
919	S607	1830	500
920	S608	1815	613
921	S609	1800	500
922	S610	1785	613
923	S611	1770	500
924	S612	1755	613
925	S613	1740	500
926	S614	1725	613
927	S615	1710	500
928	S616	1695	613
929	S617	1680	500
930	S618	1665	613
931	S619	1650	500
932	S620	1635	613
933	S621	1620	500
934	S622	1605	613
935	S623	1590	500
936	S624	1575	613
937	S625	1560	500
938	S626	1545	613
939	S627	1530	500
940	S628	1515	613
941	S629	1500	500
942	S630	1485	613
943	S631	1470	500

No.	Name	X	Y
944	S632	1455	613
945	S633	1440	500
946	S634	1425	613
947	S635	1410	500
948	S636	1395	613
949	S637	1380	500
950	S638	1365	613
951	S639	1350	500
952	S640	1335	613
953	S641	1320	500
954	S642	1305	613
955	S643	1290	500
956	S644	1275	613
957	S645	1260	500
958	S646	1245	613
959	S647	1230	500
960	S648	1215	613
961	S649	1200	500
962	S650	1185	613
963	S651	1170	500
964	S652	1155	613
965	S653	1140	500
966	S654	1125	613
967	S655	1110	500
968	S656	1095	613
969	S657	1080	500
970	S658	1065	613
971	S659	1050	500
972	S660	1035	613
973	S661	1020	500
974	S662	1005	613
975	S663	990	500
976	S664	975	613
977	S665	960	500
978	S666	945	613
979	S667	930	500
980	S668	915	613
981	S669	900	500
982	S670	885	613
983	S671	870	500
984	S672	855	613
985	S673	840	500
986	S674	825	613
987	S675	810	500
988	S676	795	613
989	S677	780	500
990	S678	765	613
991	S679	750	500
992	S680	735	613
993	S681	720	500
994	S682	705	613
995	S683	690	500
996	S684	675	613

No.	Name	X	Y
997	S685	660	500
998	S686	645	613
999	S687	630	500
1000	S688	615	613
1001	S689	600	500
1002	S690	585	613
1003	S691	570	500
1004	S692	555	613
1005	S693	540	500
1006	S694	525	613
1007	S695	510	500
1008	S696	495	613
1009	S697	480	500
1010	S698	465	613
1011	S699	450	500
1012	S700	435	613
1013	S701	420	500
1014	S702	405	613
1015	S703	390	500
1016	S704	375	613
1017	S705	360	500
1018	S706	345	613
1019	S707	330	500
1020	S708	315	613
1021	S709	300	500
1022	S710	285	613
1023	S711	270	500
1024	S712	255	613
1025	S713	240	500
1026	S714	225	613
1027	S715	210	500
1028	S716	195	613
1029	S717	180	500
1030	S718	165	613
1031	S719	150	500
1032	S720	135	613
1033	DUMMY	90	613
1034	DUMMY	30	613
1035	DUMMY	-30	613
1036	DUMMY	-90	613
1037	S721	-135	613
1038	S722	-150	500
1039	S723	-165	613
1040	S724	-180	500
1041	S725	-195	613
1042	S726	-210	500
1043	S727	-225	613
1044	S728	-240	500
1045	S729	-255	613
1046	S730	-270	500
1047	S731	-285	613
1048	S732	-300	500
1049	S733	-315	613

No.	Name	X	Y
1050	S734	-330	500
1051	S735	-345	613
1052	S736	-360	500
1053	S737	-375	613
1054	S738	-390	500
1055	S739	-405	613
1056	S740	-420	500
1057	S741	-435	613
1058	S742	-450	500
1059	S743	-465	613
1060	S744	-480	500
1061	S745	-495	613
1062	S746	-510	500
1063	S747	-525	613
1064	S748	-540	500
1065	S749	-555	613
1066	S750	-570	500
1067	S751	-585	613
1068	S752	-600	500
1069	S753	-615	613
1070	S754	-630	500
1071	S755	-645	613
1072	S756	-660	500
1073	S757	-675	613
1074	S758	-690	500
1075	S759	-705	613
1076	S760	-720	500
1077	S761	-735	613
1078	S762	-750	500
1079	S763	-765	613
1080	S764	-780	500
1081	S765	-795	613
1082	S766	-810	500
1083	S767	-825	613
1084	S768	-840	500
1085	S769	-855	613
1086	S770	-870	500
1087	S771	-885	613
1088	S772	-900	500
1089	S773	-915	613
1090	S774	-930	500
1091	S775	-945	613
1092	S776	-960	500
1093	S777	-975	613
1094	S778	-990	500
1095	S779	-1005	613
1096	S780	-1020	500
1097	S781	-1035	613
1098	S782	-1050	500
1099	S783	-1065	613
1100	S784	-1080	500
1101	S785	-1095	613
1102	S786	-1110	500

No.	Name	X	Y
1103	S787	-1125	613
1104	S788	-1140	500
1105	S789	-1155	613
1106	S790	-1170	500
1107	S791	-1185	613
1108	S792	-1200	500
1109	S793	-1215	613
1110	S794	-1230	500
1111	S795	-1245	613
1112	S796	-1260	500
1113	S797	-1275	613
1114	S798	-1290	500
1115	S799	-1305	613
1116	S800	-1320	500
1117	S801	-1335	613
1118	S802	-1350	500
1119	S803	-1365	613
1120	S804	-1380	500
1121	S805	-1395	613
1122	S806	-1410	500
1123	S807	-1425	613
1124	S808	-1440	500
1125	S809	-1455	613
1126	S810	-1470	500
1127	S811	-1485	613
1128	S812	-1500	500
1129	S813	-1515	613
1130	S814	-1530	500
1131	S815	-1545	613
1132	S816	-1560	500
1133	S817	-1575	613
1134	S818	-1590	500
1135	S819	-1605	613
1136	S820	-1620	500
1137	S821	-1635	613
1138	S822	-1650	500
1139	S823	-1665	613
1140	S824	-1680	500
1141	S825	-1695	613
1142	S826	-1710	500
1143	S827	-1725	613
1144	S828	-1740	500
1145	S829	-1755	613
1146	S830	-1770	500
1147	S831	-1785	613
1148	S832	-1800	500
1149	S833	-1815	613
1150	S834	-1830	500
1151	S835	-1845	613
1152	S836	-1860	500
1153	S837	-1875	613
1154	S838	-1890	500
1155	S839	-1905	613

No.	Name	X	Y
1156	S840	-1920	500
1157	S841	-1935	613
1158	S842	-1950	500
1159	S843	-1965	613
1160	S844	-1980	500
1161	S845	-1995	613
1162	S846	-2010	500
1163	S847	-2025	613
1164	S848	-2040	500
1165	S849	-2055	613
1166	S850	-2070	500
1167	S851	-2085	613
1168	S852	-2100	500
1169	S853	-2115	613
1170	S854	-2130	500
1171	S855	-2145	613
1172	S856	-2160	500
1173	S857	-2175	613
1174	S858	-2190	500
1175	S859	-2205	613
1176	S860	-2220	500
1177	S861	-2235	613
1178	S862	-2250	500
1179	S863	-2265	613
1180	S864	-2280	500
1181	S865	-2295	613
1182	S866	-2310	500
1183	S867	-2325	613
1184	S868	-2340	500
1185	S869	-2355	613
1186	S870	-2370	500
1187	S871	-2385	613
1188	S872	-2400	500
1189	S873	-2415	613
1190	S874	-2430	500
1191	S875	-2445	613
1192	S876	-2460	500
1193	S877	-2475	613
1194	S878	-2490	500
1195	S879	-2505	613
1196	S880	-2520	500
1197	S881	-2535	613
1198	S882	-2550	500
1199	S883	-2565	613
1200	S884	-2580	500
1201	S885	-2595	613
1202	S886	-2610	500
1203	S887	-2625	613
1204	S888	-2640	500
1205	S889	-2655	613
1206	S890	-2670	500
1207	S891	-2685	613
1208	S892	-2700	500

No.	Name	X	Y
1209	S893	-2715	613
1210	S894	-2730	500
1211	S895	-2745	613
1212	S896	-2760	500
1213	S897	-2775	613
1214	S898	-2790	500
1215	S899	-2805	613
1216	S900	-2820	500
1217	S901	-2835	613
1218	S902	-2850	500
1219	S903	-2865	613
1220	S904	-2880	500
1221	S905	-2895	613
1222	S906	-2910	500
1223	S907	-2925	613
1224	S908	-2940	500
1225	S909	-2955	613
1226	S910	-2970	500
1227	S911	-2985	613
1228	S912	-3000	500
1229	S913	-3015	613
1230	S914	-3030	500
1231	S915	-3045	613
1232	S916	-3060	500
1233	S917	-3075	613
1234	S918	-3090	500
1235	S919	-3105	613
1236	S920	-3120	500
1237	S921	-3135	613
1238	S922	-3150	500
1239	S923	-3165	613
1240	S924	-3180	500
1241	S925	-3195	613
1242	S926	-3210	500
1243	S927	-3225	613
1244	S928	-3240	500
1245	S929	-3255	613
1246	S930	-3270	500
1247	S931	-3285	613
1248	S932	-3300	500
1249	S933	-3315	613
1250	S934	-3330	500
1251	S935	-3345	613
1252	S936	-3360	500
1253	S937	-3375	613
1254	S938	-3390	500
1255	S939	-3405	613
1256	S940	-3420	500
1257	S941	-3435	613
1258	S942	-3450	500
1259	S943	-3465	613
1260	S944	-3480	500
1261	S945	-3495	613

No.	Name	X	Y
1262	S946	-3510	500
1263	S947	-3525	613
1264	S948	-3540	500
1265	S949	-3555	613
1266	S950	-3570	500
1267	S951	-3585	613
1268	S952	-3600	500
1269	S953	-3615	613
1270	S954	-3630	500
1271	S955	-3645	613
1272	S956	-3660	500
1273	S957	-3675	613
1274	S958	-3690	500
1275	S959	-3705	613
1276	S960	-3720	500
1277	S961	-3735	613
1278	S962	-3750	500
1279	S963	-3765	613
1280	S964	-3780	500
1281	S965	-3795	613
1282	S966	-3810	500
1283	S967	-3825	613
1284	S968	-3840	500
1285	S969	-3855	613
1286	S970	-3870	500
1287	S971	-3885	613
1288	S972	-3900	500
1289	S973	-3915	613
1290	S974	-3930	500
1291	S975	-3945	613
1292	S976	-3960	500
1293	S977	-3975	613
1294	S978	-3990	500
1295	S979	-4005	613
1296	S980	-4020	500
1297	S981	-4035	613
1298	S982	-4050	500
1299	S983	-4065	613
1300	S984	-4080	500
1301	S985	-4095	613
1302	S986	-4110	500
1303	S987	-4125	613
1304	S988	-4140	500
1305	S989	-4155	613
1306	S990	-4170	500
1307	S991	-4185	613
1308	S992	-4200	500
1309	S993	-4215	613
1310	S994	-4230	500
1311	S995	-4245	613
1312	S996	-4260	500
1313	S997	-4275	613
1314	S998	-4290	500
1315	S999	-4305	613
1316	S1000	-4320	500
1317	S1001	-4335	613
1318	S1002	-4350	500
1319	S1003	-4365	613
1320	S1004	-4380	500
1321	S1005	-4395	613
1322	S1006	-4410	500
1323	S1007	-4425	613
1324	S1008	-4440	500
1325	S1009	-4455	613
1326	S1010	-4470	500
1327	S1011	-4485	613
1328	S1012	-4500	500
1329	S1013	-4515	613
1330	S1014	-4530	500
1331	S1015	-4545	613
1332	S1016	-4560	500
1333	S1017	-4575	613
1334	S1018	-4590	500
1335	S1019	-4605	613
1336	S1020	-4620	500
1337	S1021	-4635	613
1338	S1022	-4650	500
1339	S1023	-4665	613
1340	S1024	-4680	500
1341	S1025	-4695	613
1342	S1026	-4710	500
1343	S1027	-4725	613
1344	S1028	-4740	500
1345	S1029	-4755	613
1346	S1030	-4770	500
1347	S1031	-4785	613
1348	S1032	-4800	500
1349	S1033	-4815	613
1350	S1034	-4830	500
1351	S1035	-4845	613
1352	S1036	-4860	500
1353	S1037	-4875	613
1354	S1038	-4890	500
1355	S1039	-4905	613
1356	S1040	-4920	500
1357	S1041	-4935	613
1358	S1042	-4950	500
1359	S1043	-4965	613
1360	S1044	-4980	500
1361	S1045	-4995	613
1362	S1046	-5010	500
1363	S1047	-5025	613
1364	S1048	-5040	500
1365	S1049	-5055	613
1366	S1050	-5070	500
1367	S1051	-5085	613
1368	S1052	-5100	500
1369	S1053	-5115	613
1370	S1054	-5130	500
1371	S1055	-5145	613
1372	S1056	-5160	500
1373	S1057	-5175	613
1374	S1058	-5190	500
1375	S1059	-5205	613
1376	S1060	-5220	500
1377	S1061	-5235	613
1378	S1062	-5250	500
1379	S1063	-5265	613
1380	S1064	-5280	500
1381	S1065	-5295	613
1382	S1066	-5310	500
1383	S1067	-5325	613
1384	S1068	-5340	500
1385	S1069	-5355	613
1386	S1070	-5370	500
1387	S1071	-5385	613
1388	S1072	-5400	500
1389	S1073	-5415	613
1390	S1074	-5430	500
1391	S1075	-5445	613
1392	S1076	-5460	500
1393	S1077	-5475	613
1394	S1078	-5490	500
1395	S1079	-5505	613
1396	S1080	-5520	500
1397	S1081	-5535	613
1398	S1082	-5550	500
1399	S1083	-5565	613
1400	S1084	-5580	500
1401	S1085	-5595	613
1402	S1086	-5610	500
1403	S1087	-5625	613
1404	S1088	-5640	500
1405	S1089	-5655	613
1406	S1090	-5670	500
1407	S1091	-5685	613
1408	S1092	-5700	500
1409	S1093	-5715	613
1410	S1094	-5730	500
1411	S1095	-5745	613
1412	S1096	-5760	500
1413	S1097	-5775	613
1414	S1098	-5790	500
1415	S1099	-5805	613
1416	S1100	-5820	500
1417	S1101	-5835	613
1418	S1102	-5850	500
1419	S1103	-5865	613
1420	S1104	-5880	500

No.	Name	X	Y
1421	S1105	-5895	613
1422	S1106	-5910	500
1423	S1107	-5925	613
1424	S1108	-5940	500
1425	S1109	-5955	613
1426	S1110	-5970	500
1427	S1111	-5985	613
1428	S1112	-6000	500
1429	S1113	-6015	613
1430	S1114	-6030	500
1431	S1115	-6045	613
1432	S1116	-6060	500
1433	S1117	-6075	613
1434	S1118	-6090	500
1435	S1119	-6105	613
1436	S1120	-6120	500
1437	S1121	-6135	613
1438	S1122	-6150	500
1439	S1123	-6165	613
1440	S1124	-6180	500
1441	S1125	-6195	613
1442	S1126	-6210	500
1443	S1127	-6225	613
1444	S1128	-6240	500
1445	S1129	-6255	613
1446	S1130	-6270	500
1447	S1131	-6285	613
1448	S1132	-6300	500
1449	S1133	-6315	613
1450	S1134	-6330	500
1451	S1135	-6345	613
1452	S1136	-6360	500
1453	S1137	-6375	613
1454	S1138	-6390	500
1455	S1139	-6405	613
1456	S1140	-6420	500
1457	S1141	-6435	613
1458	S1142	-6450	500
1459	S1143	-6465	613
1460	S1144	-6480	500
1461	S1145	-6495	613
1462	S1146	-6510	500
1463	S1147	-6525	613
1464	S1148	-6540	500
1465	S1149	-6555	613
1466	S1150	-6570	500
1467	S1151	-6585	613
1468	S1152	-6600	500
1469	S1153	-6615	613
1470	S1154	-6630	500
1471	S1155	-6645	613
1472	S1156	-6660	500
1473	S1157	-6675	613
1474	S1158	-6690	500
1475	S1159	-6705	613
1476	S1160	-6720	500
1477	S1161	-6735	613
1478	S1162	-6750	500
1479	S1163	-6765	613
1480	S1164	-6780	500
1481	S1165	-6795	613
1482	S1166	-6810	500
1483	S1167	-6825	613
1484	S1168	-6840	500
1485	S1169	-6855	613
1486	S1170	-6870	500
1487	S1171	-6885	613
1488	S1172	-6900	500
1489	S1173	-6915	613
1490	S1174	-6930	500
1491	S1175	-6945	613
1492	S1176	-6960	500
1493	S1177	-6975	613
1494	S1178	-6990	500
1495	S1179	-7005	613
1496	S1180	-7020	500
1497	S1181	-7035	613
1498	S1182	-7050	500
1499	S1183	-7065	613
1500	S1184	-7080	500
1501	S1185	-7095	613
1502	S1186	-7110	500
1503	S1187	-7125	613
1504	S1188	-7140	500
1505	S1189	-7155	613
1506	S1190	-7170	500
1507	S1191	-7185	613
1508	S1192	-7200	500
1509	S1193	-7215	613
1510	S1194	-7230	500
1511	S1195	-7245	613
1512	S1196	-7260	500
1513	S1197	-7275	613
1514	S1198	-7290	500
1515	S1199	-7305	613
1516	S1200	-7320	500
1517	S1201	-7335	613
1518	S1202	-7350	500
1519	S1203	-7365	613
1520	S1204	-7380	500
1521	S1205	-7395	613
1522	S1206	-7410	500
1523	S1207	-7425	613
1524	S1208	-7440	500
1525	S1209	-7455	613
1526	S1210	-7470	500
1527	S1211	-7485	613
1528	S1212	-7500	500
1529	S1213	-7515	613
1530	S1214	-7530	500
1531	S1215	-7545	613
1532	S1216	-7560	500
1533	S1217	-7575	613
1534	S1218	-7590	500
1535	S1219	-7605	613
1536	S1220	-7620	500
1537	S1221	-7635	613
1538	S1222	-7650	500
1539	S1223	-7665	613
1540	S1224	-7680	500
1541	S1225	-7695	613
1542	S1226	-7710	500
1543	S1227	-7725	613
1544	S1228	-7740	500
1545	S1229	-7755	613
1546	S1230	-7770	500
1547	S1231	-7785	613
1548	S1232	-7800	500
1549	S1233	-7815	613
1550	S1234	-7830	500
1551	S1235	-7845	613
1552	S1236	-7860	500
1553	S1237	-7875	613
1554	S1238	-7890	500
1555	S1239	-7905	613
1556	S1240	-7920	500
1557	S1241	-7935	613
1558	S1242	-7950	500
1559	S1243	-7965	613
1560	S1244	-7980	500
1561	S1245	-7995	613
1562	S1246	-8010	500
1563	S1247	-8025	613
1564	S1248	-8040	500
1565	S1249	-8055	613
1566	S1250	-8070	500
1567	S1251	-8085	613
1568	S1252	-8100	500
1569	S1253	-8115	613
1570	S1254	-8130	500
1571	S1255	-8145	613
1572	S1256	-8160	500
1573	S1257	-8175	613
1574	S1258	-8190	500
1575	S1259	-8205	613
1576	S1260	-8220	500
1577	S1261	-8235	613
1578	S1262	-8250	500
1579	S1263	-8265	613

No.	Name	X	Y
1580	S1264	-8280	500
1581	S1265	-8295	613
1582	S1266	-8310	500
1583	S1267	-8325	613
1584	S1268	-8340	500
1585	S1269	-8355	613
1586	S1270	-8370	500
1587	S1271	-8385	613
1588	S1272	-8400	500
1589	S1273	-8415	613
1590	S1274	-8430	500
1591	S1275	-8445	613
1592	S1276	-8460	500
1593	S1277	-8475	613
1594	S1278	-8490	500
1595	S1279	-8505	613
1596	S1280	-8520	500
1597	S1281	-8535	613
1598	S1282	-8550	500
1599	S1283	-8565	613
1600	S1284	-8580	500
1601	S1285	-8595	613
1602	S1286	-8610	500
1603	S1287	-8625	613
1604	S1288	-8640	500
1605	S1289	-8655	613
1606	S1290	-8670	500
1607	S1291	-8685	613
1608	S1292	-8700	500
1609	S1293	-8715	613
1610	S1294	-8730	500
1611	S1295	-8745	613
1612	S1296	-8760	500
1613	S1297	-8775	613
1614	S1298	-8790	500
1615	S1299	-8805	613
1616	S1300	-8820	500
1617	S1301	-8835	613
1618	S1302	-8850	500
1619	S1303	-8865	613
1620	S1304	-8880	500
1621	S1305	-8895	613
1622	S1306	-8910	500
1623	S1307	-8925	613
1624	S1308	-8940	500
1625	S1309	-8955	613
1626	S1310	-8970	500
1627	S1311	-8985	613
1628	S1312	-9000	500
1629	S1313	-9015	613
1630	S1314	-9030	500
1631	S1315	-9045	613
1632	S1316	-9060	500

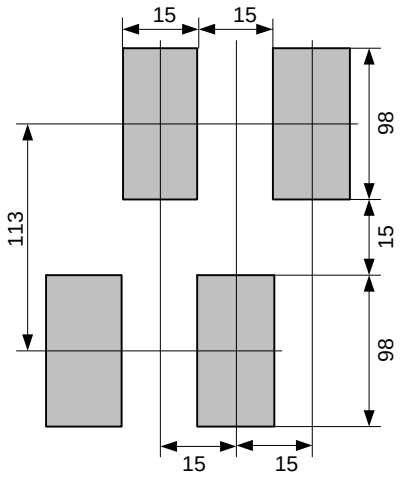
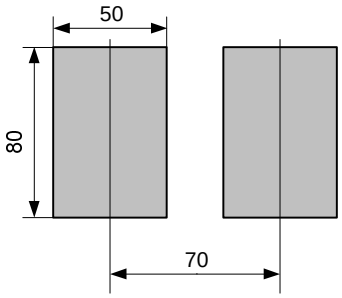
No.	Name	X	Y
1633	S1317	-9075	613
1634	S1318	-9090	500
1635	S1319	-9105	613
1636	S1320	-9120	500
1637	S1321	-9135	613
1638	S1322	-9150	500
1639	S1323	-9165	613
1640	S1324	-9180	500
1641	S1325	-9195	613
1642	S1326	-9210	500
1643	S1327	-9225	613
1644	S1328	-9240	500
1645	S1329	-9255	613
1646	S1330	-9270	500
1647	S1331	-9285	613
1648	S1332	-9300	500
1649	S1333	-9315	613
1650	S1334	-9330	500
1651	S1335	-9345	613
1652	S1336	-9360	500
1653	S1337	-9375	613
1654	S1338	-9390	500
1655	S1339	-9405	613
1656	S1340	-9420	500
1657	S1341	-9435	613
1658	S1342	-9450	500
1659	S1343	-9465	613
1660	S1344	-9480	500
1661	S1345	-9495	613
1662	S1346	-9510	500
1663	S1347	-9525	613
1664	S1348	-9540	500
1665	S1349	-9555	613
1666	S1350	-9570	500
1667	S1351	-9585	613
1668	S1352	-9600	500
1669	S1353	-9615	613
1670	S1354	-9630	500
1671	S1355	-9645	613
1672	S1356	-9660	500
1673	S1357	-9675	613
1674	S1358	-9690	500
1675	S1359	-9705	613
1676	S1360	-9720	500
1677	S1361	-9735	613
1678	S1362	-9750	500
1679	S1363	-9765	613
1680	S1364	-9780	500
1681	S1365	-9795	613
1682	S1366	-9810	500
1683	S1367	-9825	613
1684	S1368	-9840	500
1685	S1369	-9855	613

No.	Name	X	Y
1686	S1370	-9870	500
1687	S1371	-9885	613
1688	S1372	-9900	500
1689	S1373	-9915	613
1690	S1374	-9930	500
1691	S1375	-9945	613
1692	S1376	-9960	500
1693	S1377	-9975	613
1694	S1378	-9990	500
1695	S1379	-10005	613
1696	S1380	-10020	500
1697	S1381	-10035	613
1698	S1382	-10050	500
1699	S1383	-10065	613
1700	S1384	-10080	500
1701	S1385	-10095	613
1702	S1386	-10110	500
1703	S1387	-10125	613
1704	S1388	-10140	500
1705	S1389	-10155	613
1706	S1390	-10170	500
1707	S1391	-10185	613
1708	S1392	-10200	500
1709	S1393	-10215	613
1710	S1394	-10230	500
1711	S1395	-10245	613
1712	S1396	-10260	500
1713	S1397	-10275	613
1714	S1398	-10290	500
1715	S1399	-10305	613
1716	S1400	-10320	500
1717	S1401	-10335	613
1718	S1402	-10350	500
1719	S1403	-10365	613
1720	S1404	-10380	500
1721	S1405	-10395	613
1722	S1406	-10410	500
1723	S1407	-10425	613
1724	S1408	-10440	500
1725	S1409	-10455	613
1726	S1410	-10470	500
1727	S1411	-10485	613
1728	S1412	-10500	500
1729	S1413	-10515	613
1730	S1414	-10530	500
1731	S1415	-10545	613
1732	S1416	-10560	500
1733	S1417	-10575	613
1734	S1418	-10590	500
1735	S1419	-10605	613
1736	S1420	-10620	500
1737	S1421	-10635	613
1738	S1422	-10650	500

No.	Name	X	Y
1739	S1423	-10665	613
1740	S1424	-10680	500
1741	S1425	-10695	613
1742	S1426	-10710	500
1743	S1427	-10725	613
1744	S1428	-10740	500
1745	S1429	-10755	613
1746	S1430	-10770	500
1747	S1431	-10785	613
1748	S1432	-10800	500
1749	S1433	-10815	613
1750	S1434	-10830	500
1751	S1435	-10845	613
1752	S1436	-10860	500
1753	S1437	-10875	613
1754	S1438	-10890	500
1755	S1439	-10905	613
1756	S1440	-10920	500
	DUMMY	**-10935**	**613**
	DUMMY	**-10950**	**500**

Alignment mark	X	Y
✚ (1-a)	-11,060	600
✚ (1-b)	11,060	600

4.4 Bump Arrangement

Staggered (No. 313 – 1756)	 Area = 1470um^2
I/O pins In-Line (No. 1-312)	 Area = 4000um^2

5 Functional Description

5.1 MIPI DBI Type-A

The LG4572B supports MIPI DBI type-A (M68 Interface).

5.1.1 Write Cycle Sequence

During a write cycle the host processor writes commands or data to the LG4572B via the interface. Type A interface utilizes nCS, DnC, nRD_RnW and nWR_E_SCK signals as well as all eight (DB[7:0]), nine (DB[8:0]), sixteen (DB[15:0]), eighteen (DB[17:0]), or twenty-four (DB[23:0]) information signals. DnC is driven low while a command is present on the interface and pulled high when data is on the interface.

The following figure shows the write cycle for the type A interface.

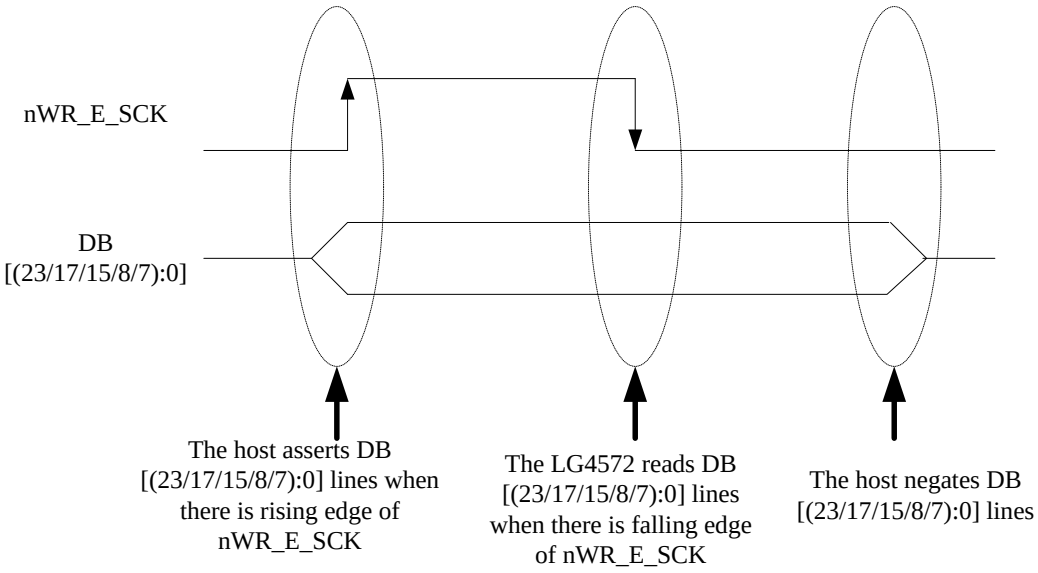


Figure 2. DBI Type A Interface Write Cycle

Note: 1. nWR_E_SCK is an unsynchronized signal; it can be stopped
2. nCS is asserted(taken low) for the same duration as the information signals

The following figure shows the example of write cycle sequence for the type A interface.

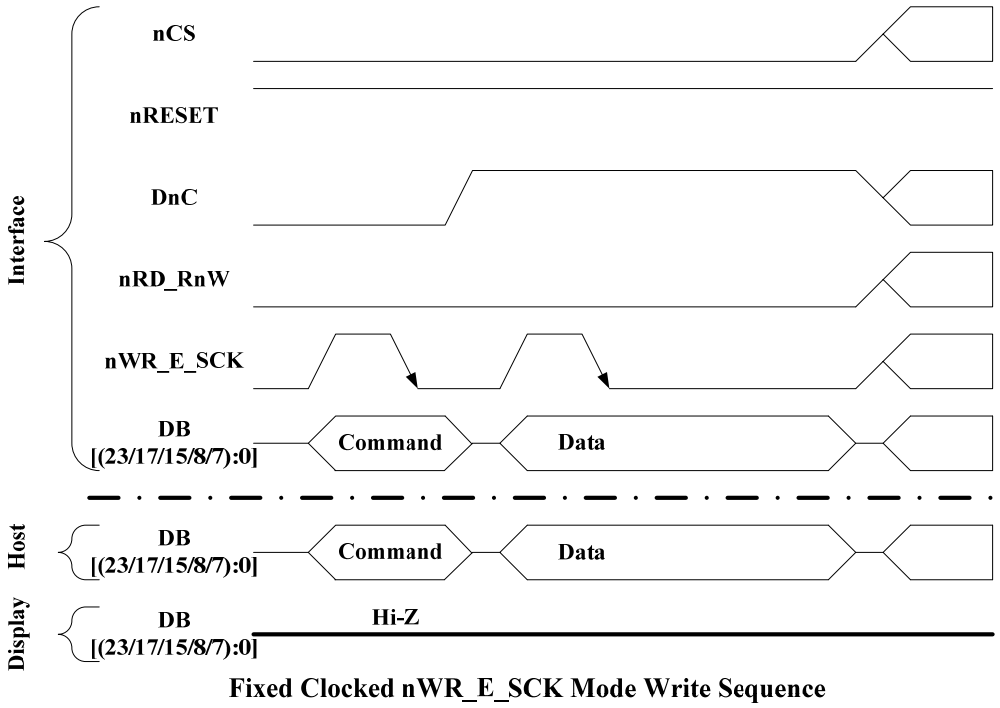


Figure 3. DBI Type A Interface Write Cycle Sequence Example

5.1.2 Read Cycle Sequence

During a read cycle the host processor reads data from the LG4572B via the interface. Type A interface utilizes nCS, DnC, RnW and nWR_E_SCK signals as well as all eight (DB[7:0]), nine (DB[8:0]), sixteen (DB[15:0]), eighteen (DB[17:0]), or twenty-four [DB[23:0]] information signals. DnC is driven low during the entire read cycle.

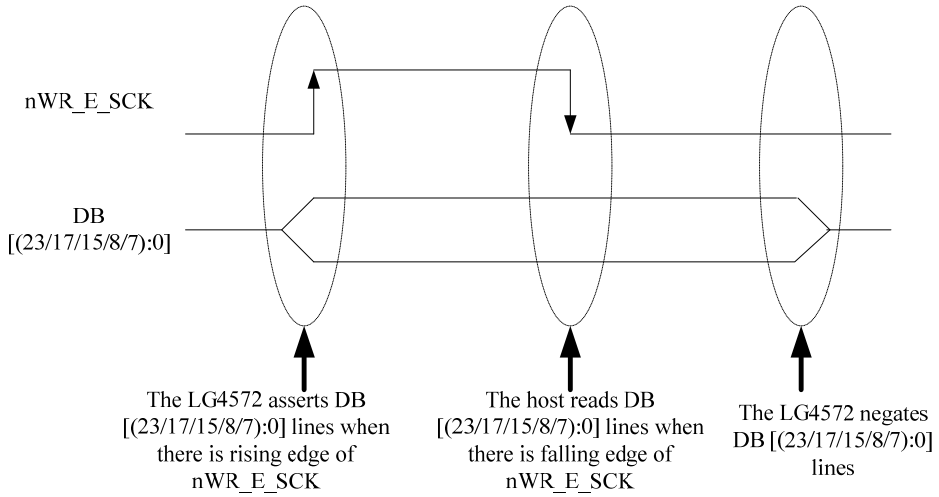


Figure 4. DBI Type A Interface Read Cycle Sequence

Note: 1. nWR_E_SCK is an unsynchronized signal; it can be stopped.
2. nCS is asserted(taken low) for the same duration as the information signals.

The following figure shows the example of write cycle sequence for the type A interface.

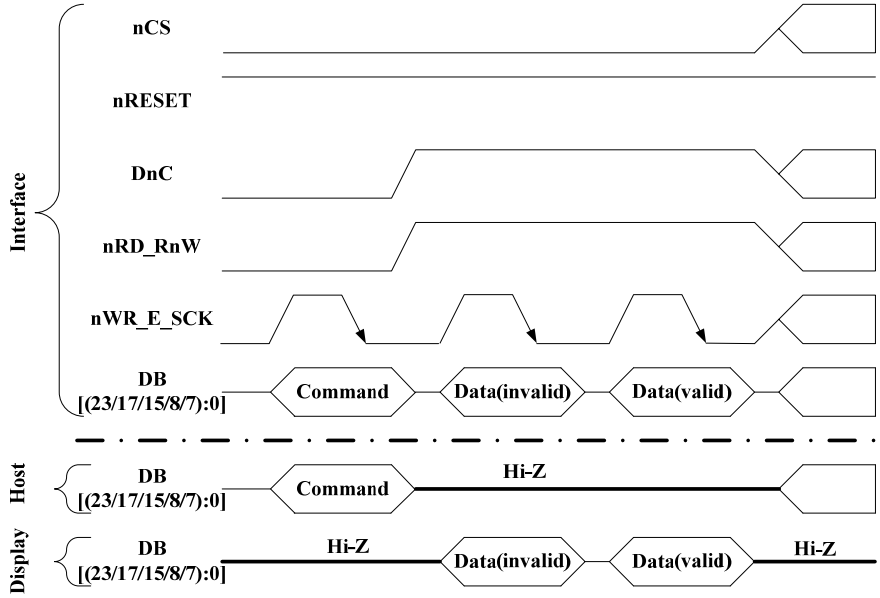


Figure 5. DBI Type A Interface Read Cycle Sequence Example

5.2 MIPI DBI Type-B

The LG4572B supports MIPI DBI type-B (I80 Interface).

5.2.1 Write Cycle Sequence

During a write cycle, data and/or command are written to the LG4572B via the interface between the LG4572B and the host processor. Each step of write cycle sequence (nWR_E_SCK high, nWR_E_SCK low, nWR_E_SCK high) comprises three control signals (DnC, nRD_RnW, nWR_E_SCK) and 8-, 9-, 16-, 18-, or 24bit data. The DnC bit indicates signal that is used to select command or data sent on the data bus.
When DnC="1", data on the above data bus is image data or command parameter. When DnC = 0, data is command. Setting nRD_RnW and nWR_E_SCK to "Low" simultaneously is prohibited. See the figure below for the write cycle sequence.

The following figure shows the write cycle for the type B interface.

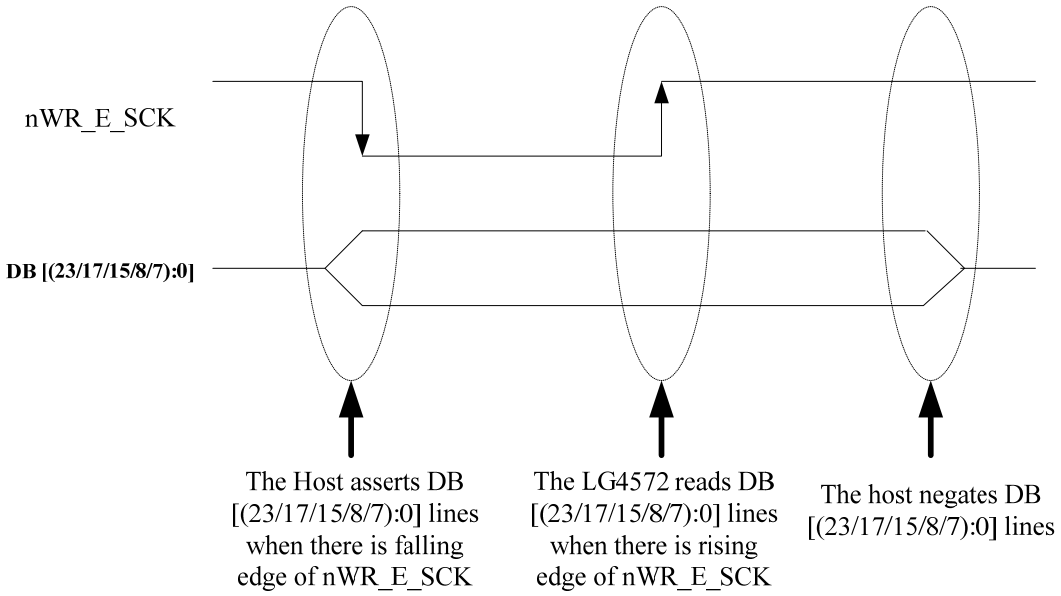


Figure 6. DBI Type B Interface Write Cycle Sequence

Note: 1. nWR_E_SCK is an unsynchronized signal; it can be stopped.

The following figure shows an example of the write cycle for the type B interface.

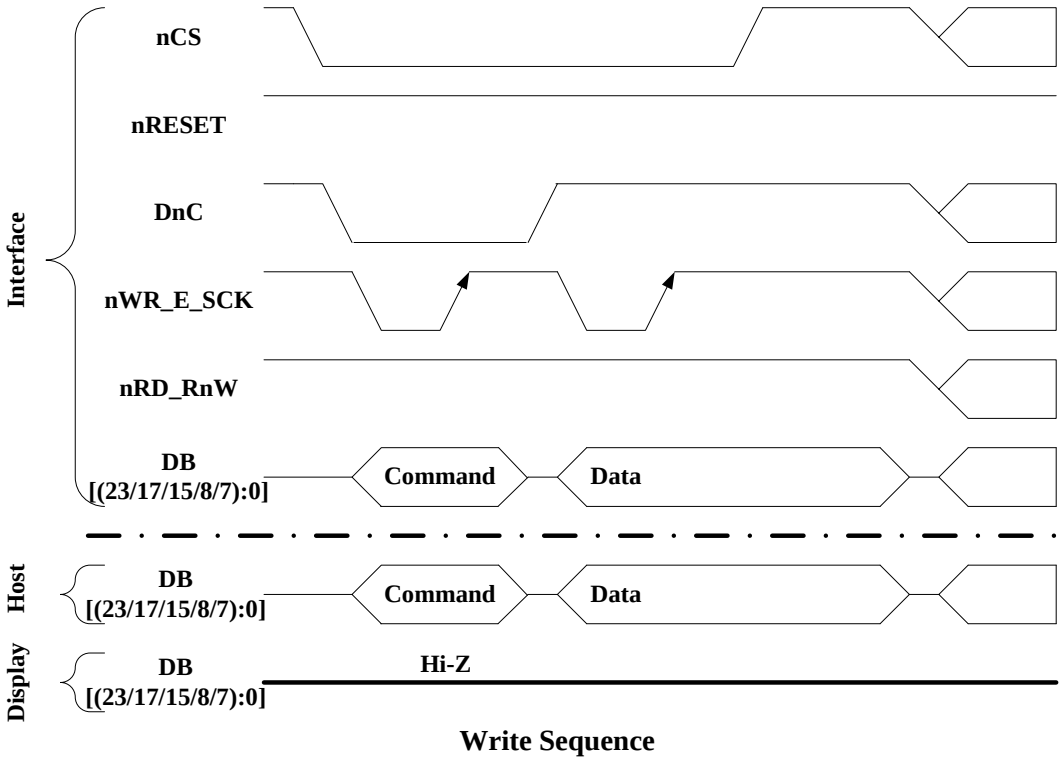


Figure 7. DBI Type B Interface Write Cycle Example

5.2.2 Read Cycle Sequence

During a read cycle, data and/or commands are read from the LG4572B via the interface between the LG4572B and the host processor. The data (DB[23:0], DB[17:0], [15:0], [8:0] or [7:0]) are

transmitted from the LG4572B to the host processor on the falling edge of nRD_RnW. The host processor reads the data on the rising edge of nRD_RnW. Setting nRD_RnW and nWR_E_SCK to Low simultaneously is prohibited. See below for the read cycle sequence.

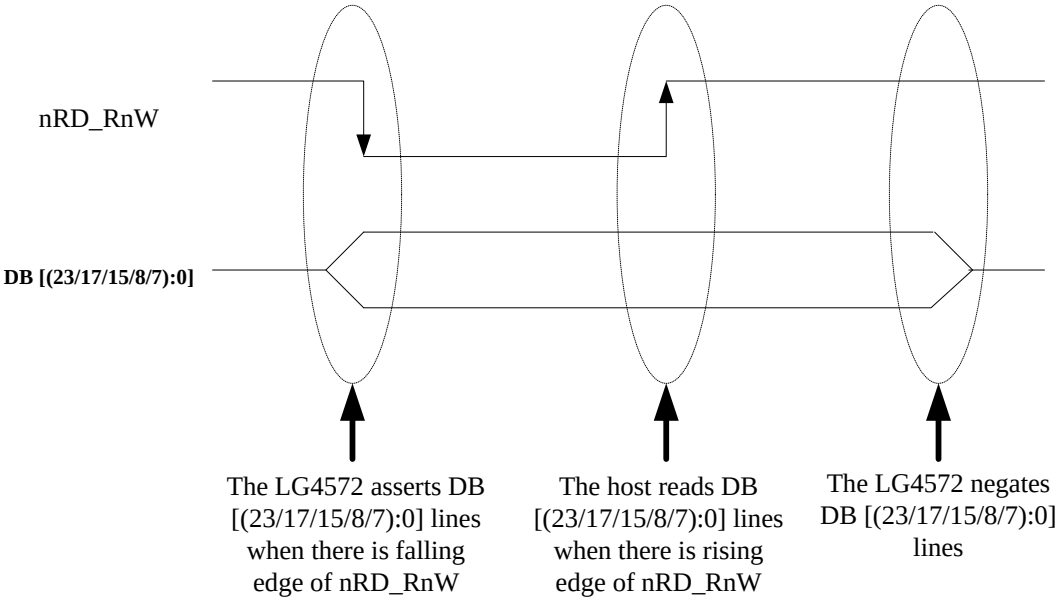


Figure 8. DBI Type B Interface Read Cycle Sequence.

Note: 1. : nRD_RnW is not a synchronous signal (can be halted).

The following figure shows an example of the read cycle for the type B interface.

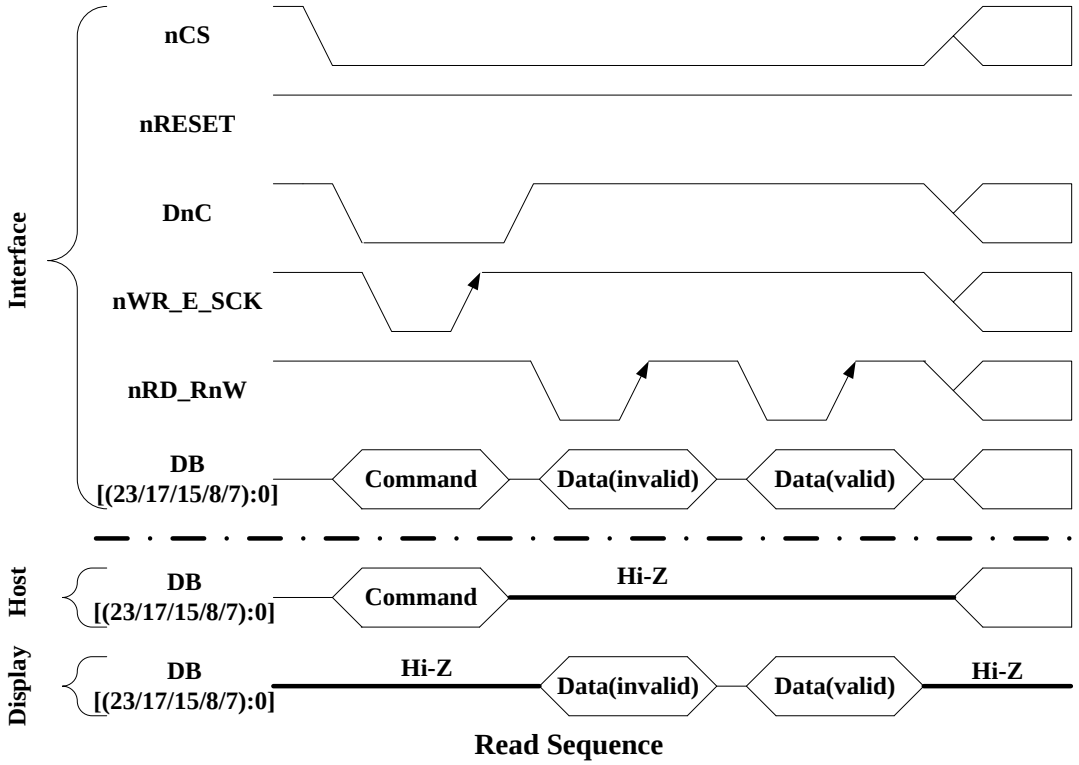


Figure 9. DBI Type B Interface Read Cycle Sequence Example

5.2.3 Interface Color Coding for DBI Type A and B

The LG4572B supports 8-bit/9-bit/16-bit/18-bit/24-bit color codings for DBI type A and B. The following figures are for them.

8-bit Interface

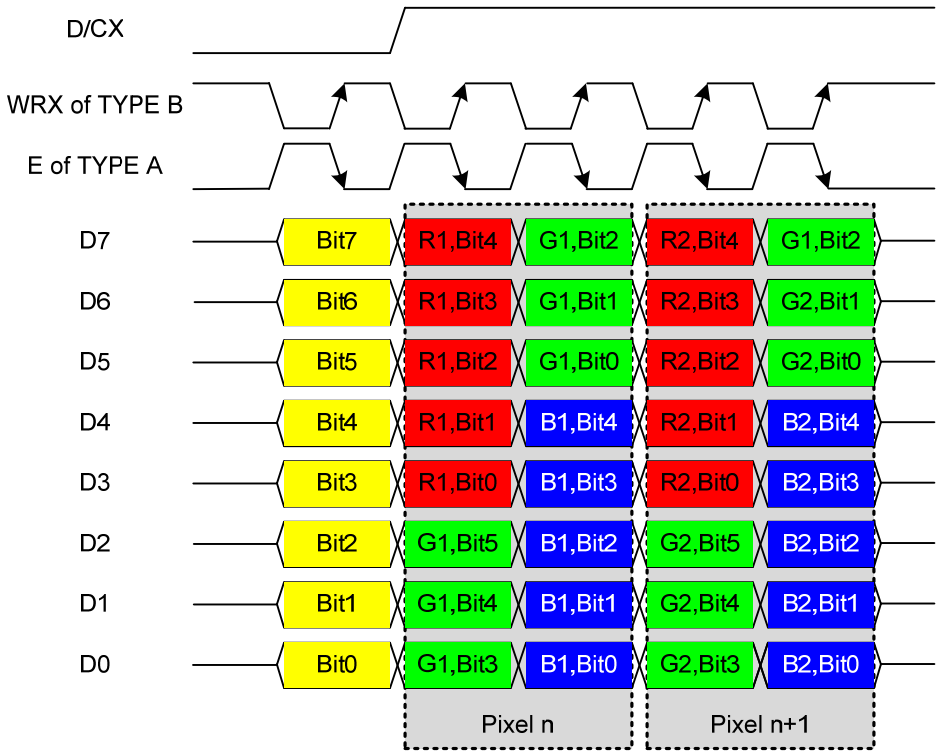


Figure 10. 16-bits/pixel(R 5-bit, G 6-bit, B 5-bit), 65,536 Colors

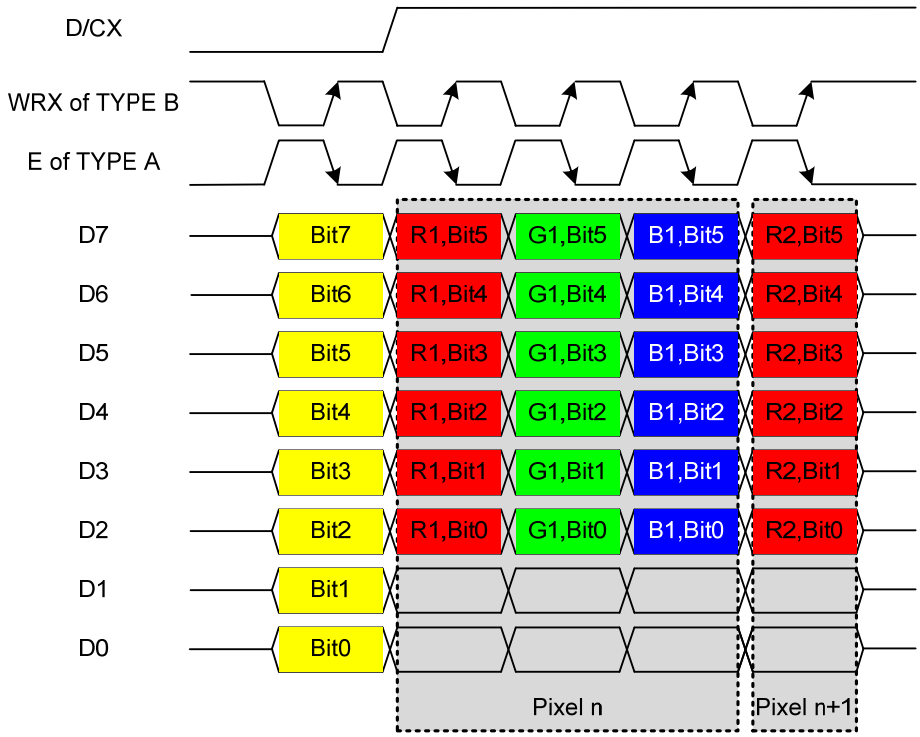


Figure 11. 18-bits/pixel(R 6-bit, G 6-bit, B 6-bit), 262,144 Colors

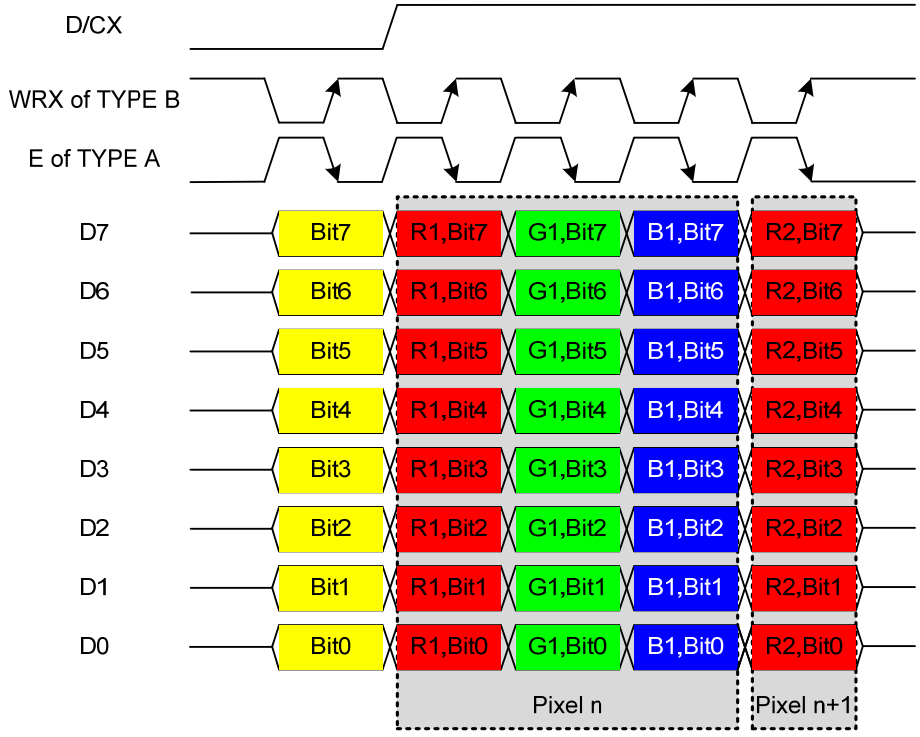


Figure 12. 24-bits/pixel(R 8-bit, G 8-bit, B 8-bit), 16,777,216 Colors

9-bit Interface

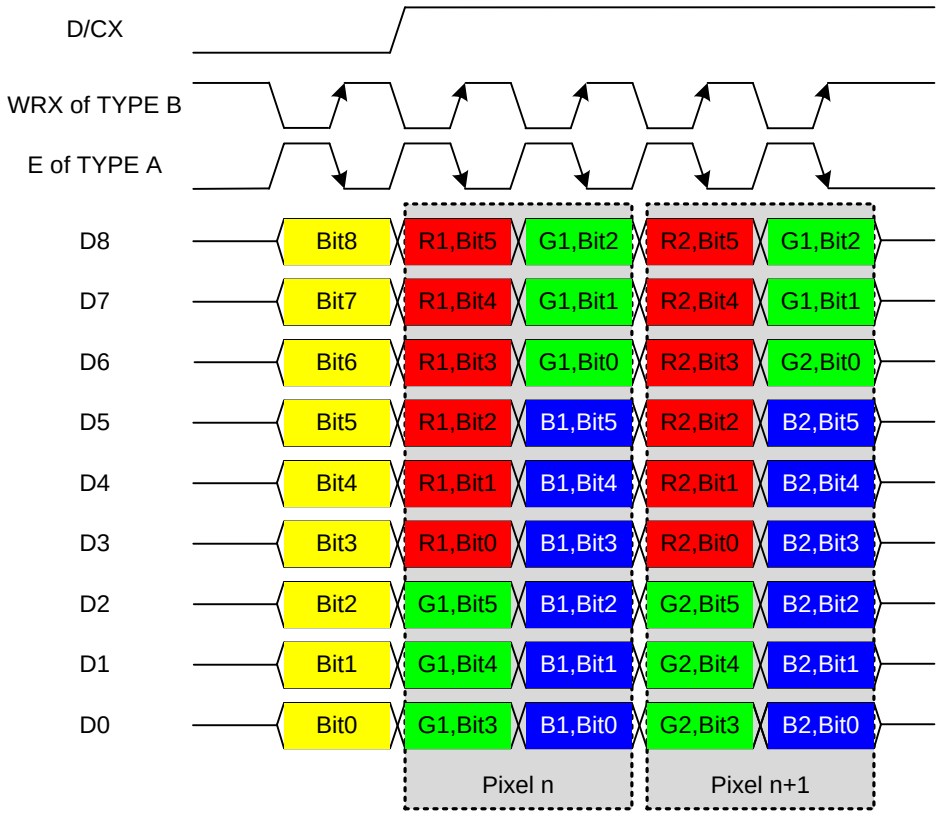


Figure 13. 18-bits/pixel(R 6-bit, G 6-bit, B 6-bit), 262,144 Colors

16-bit Interface

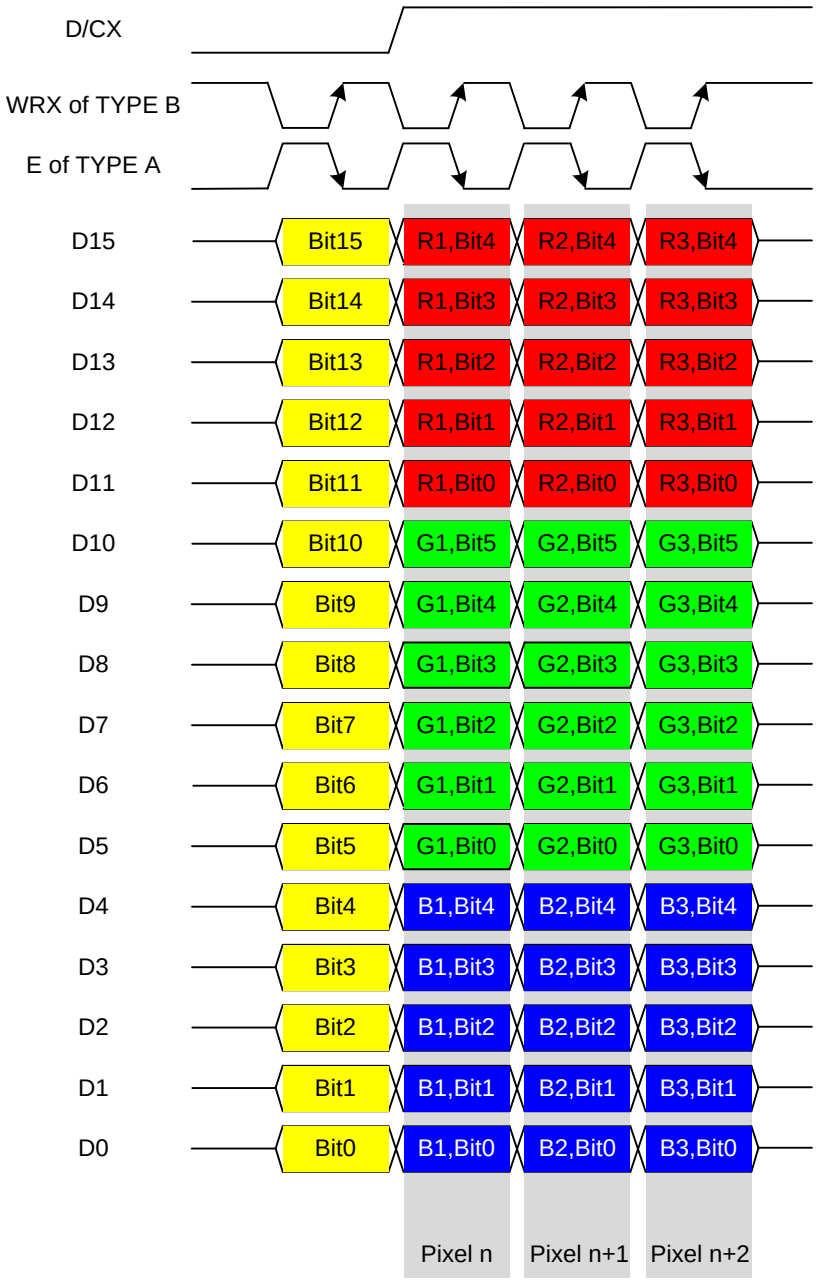


Figure 14. 16-bits/pixel(R 5-bit, G 6-bit, B 5-bit), 65,536 Colors

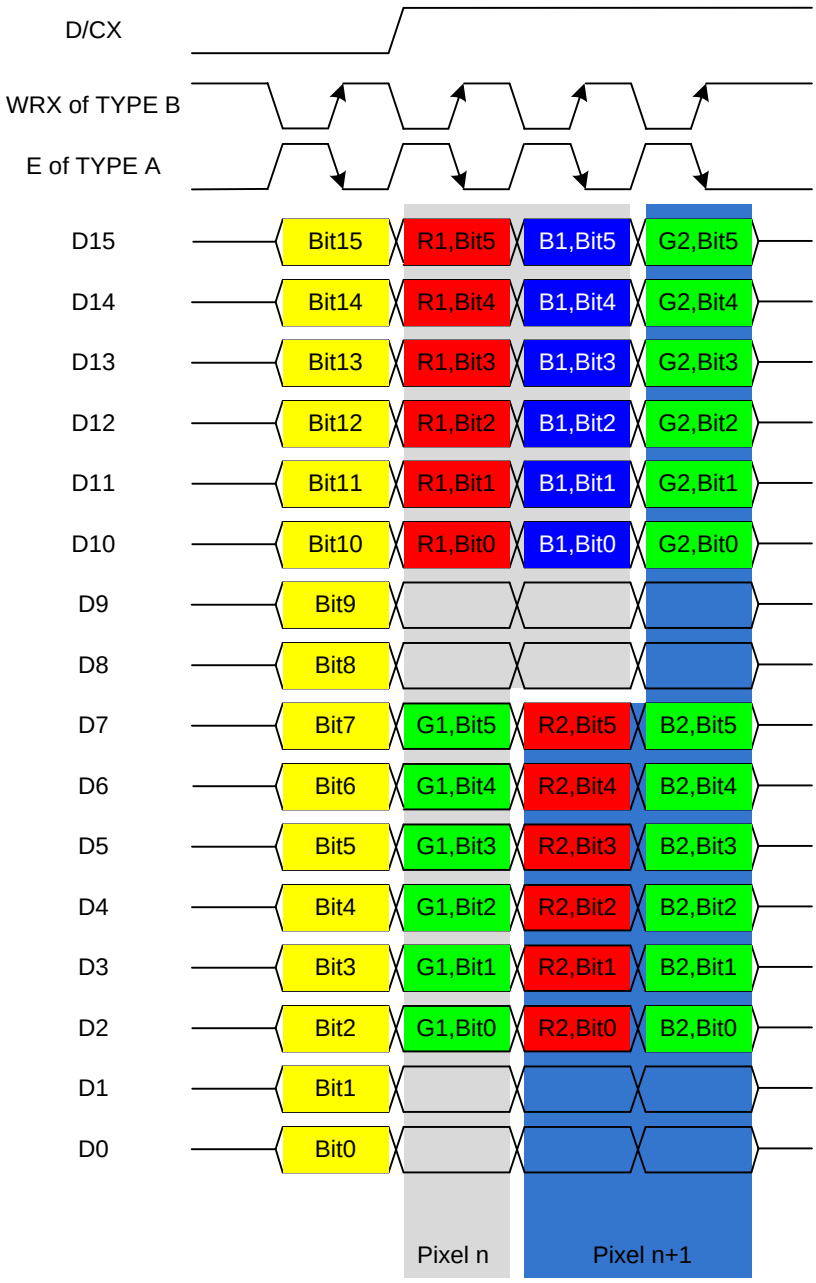


Figure 15. 18-bits/pixel(R 6-bit, G 6-bit, B 6-bit), 262,144 Colors

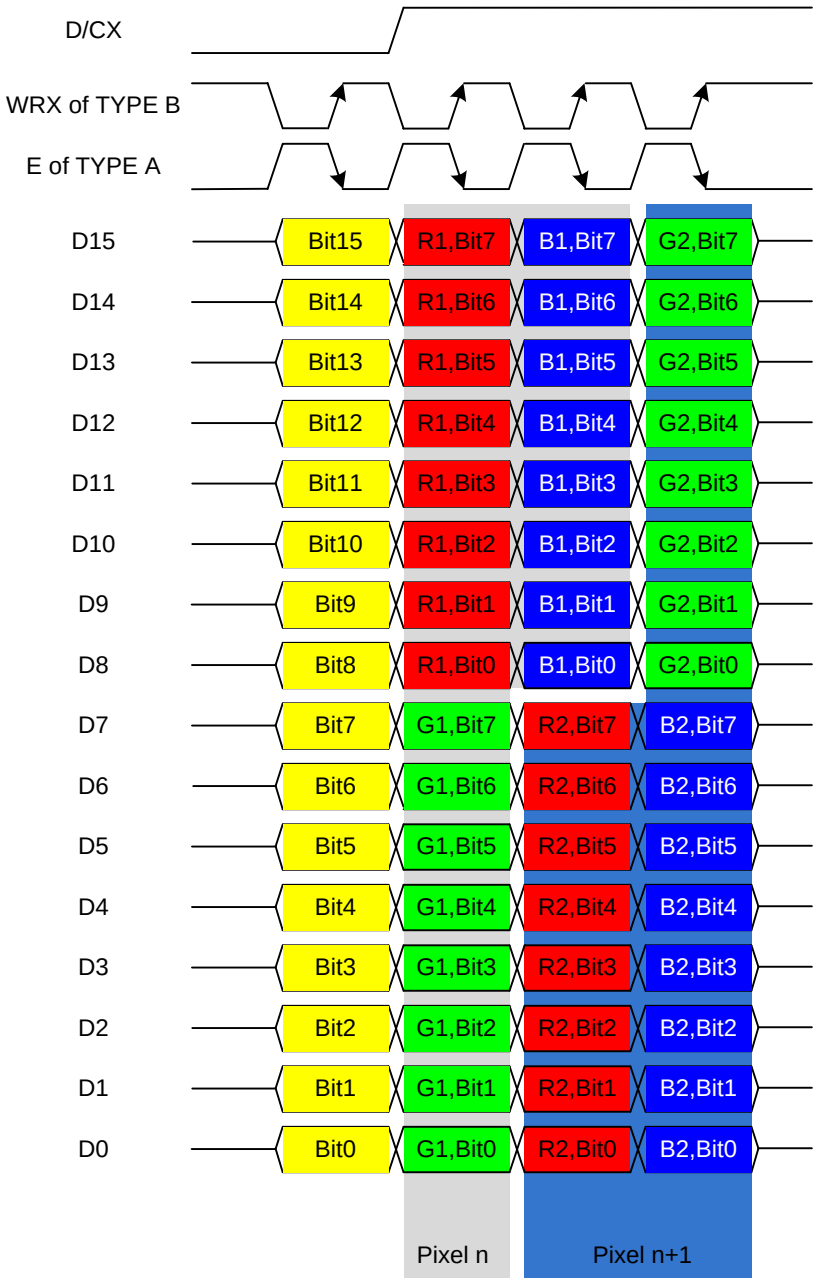


Figure 16. 24-bits/pixel(R 8-bit, G 8-bit, B 8-bit), 16,777,216 Colors

18-bit Interface

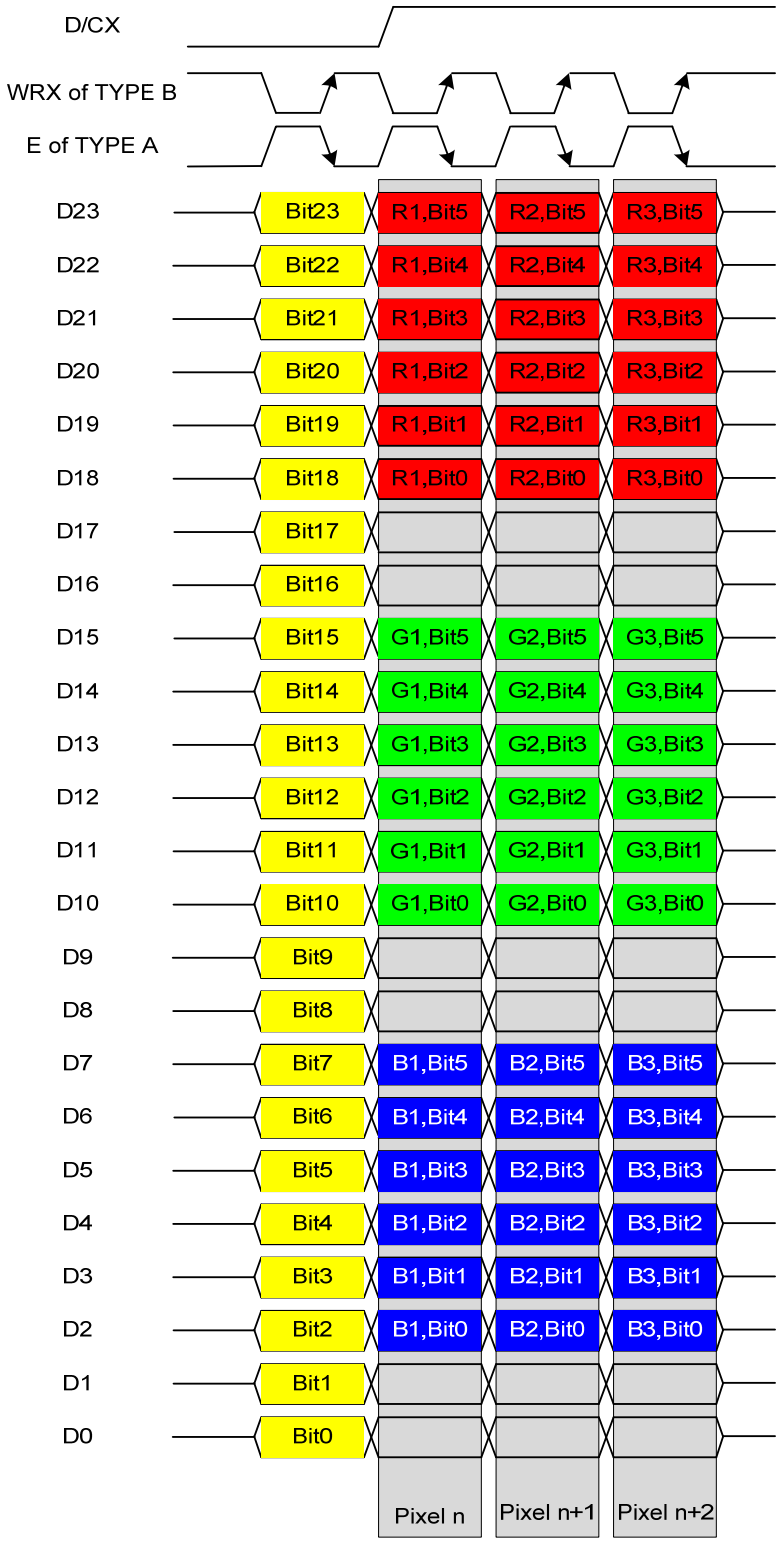


Figure 17. 18-bits/pixel(R 6-bit, G 6-bit, B 6-bit), 262,144 Colors

24-bit Interface

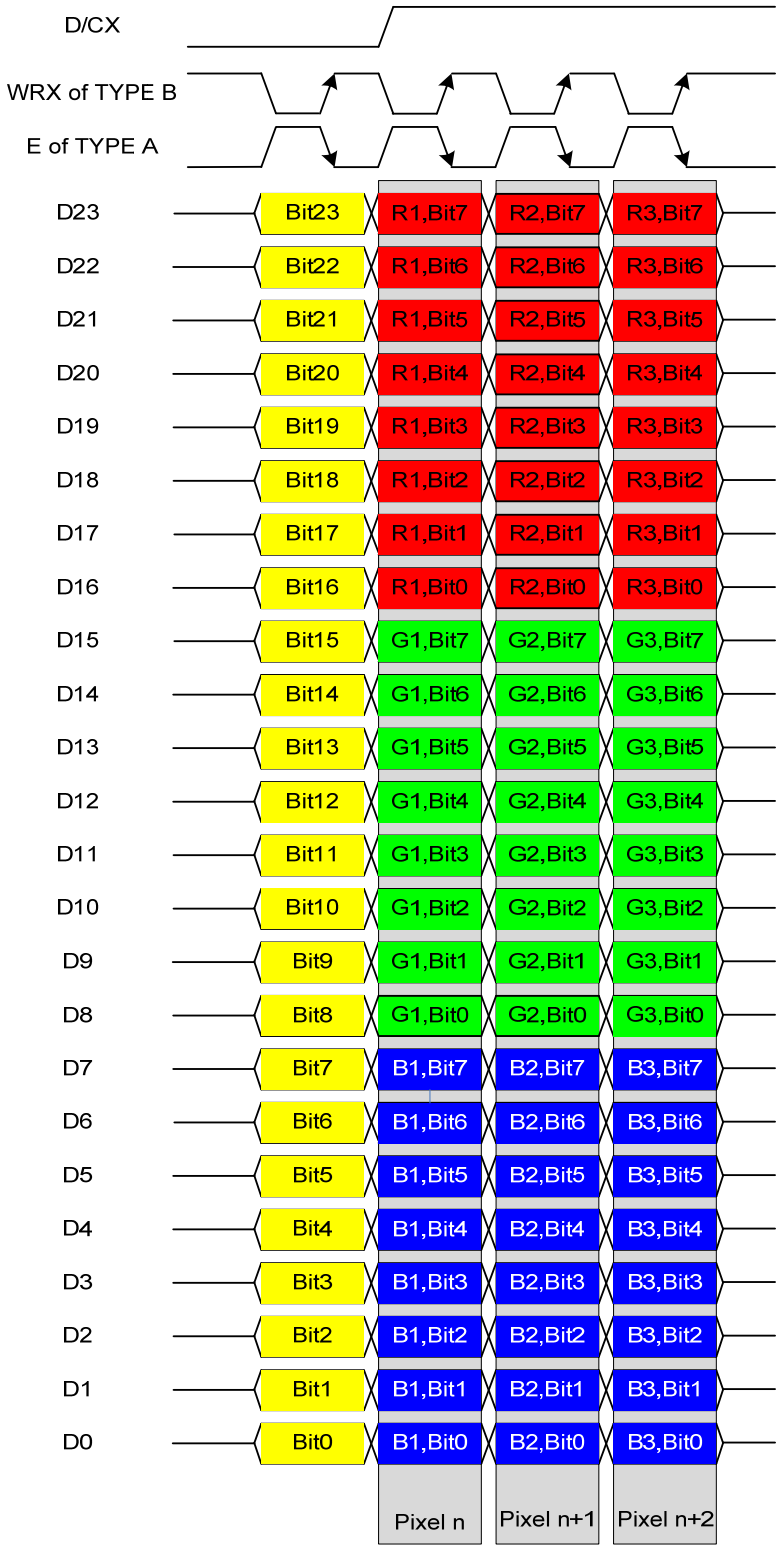


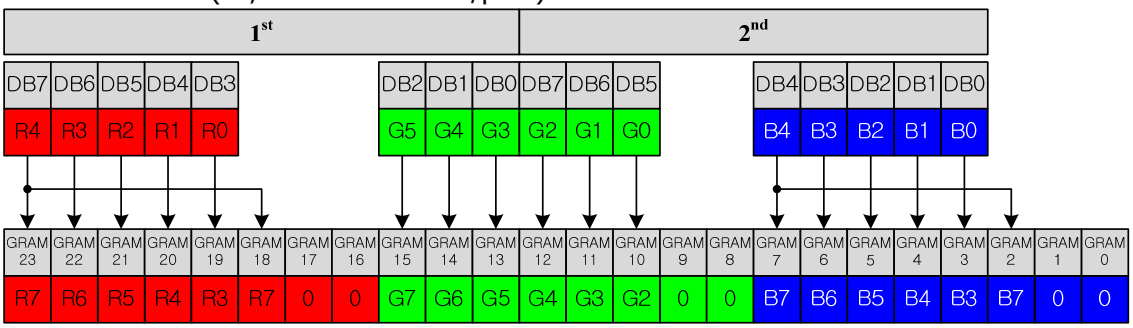
Figure 18. 24-bits/pixel(R 8-bit, G 8-bit, B 8-bit), 16,777,216 Colors

5.2.4 Interface Color Coding for GRAM Data Write

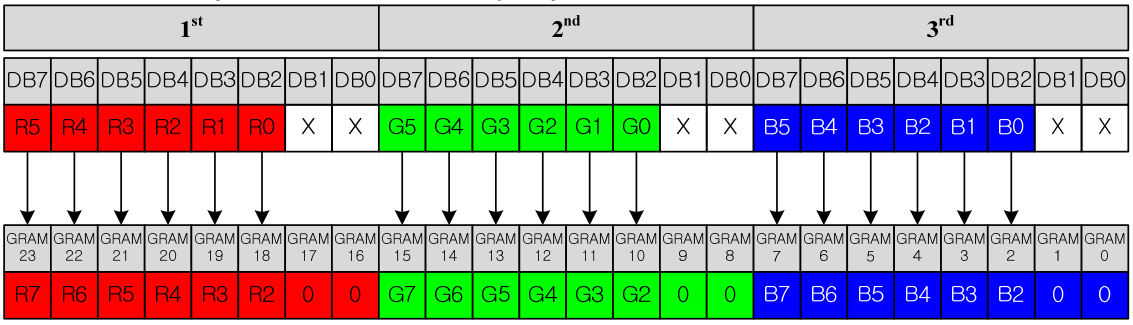
There are different possible GRAM data writing ways in the LG4572B according to each 8-bit/9-bit/16-bit/18-bit/24-bit interfaces. The following figures are for them.

8-bit Interface

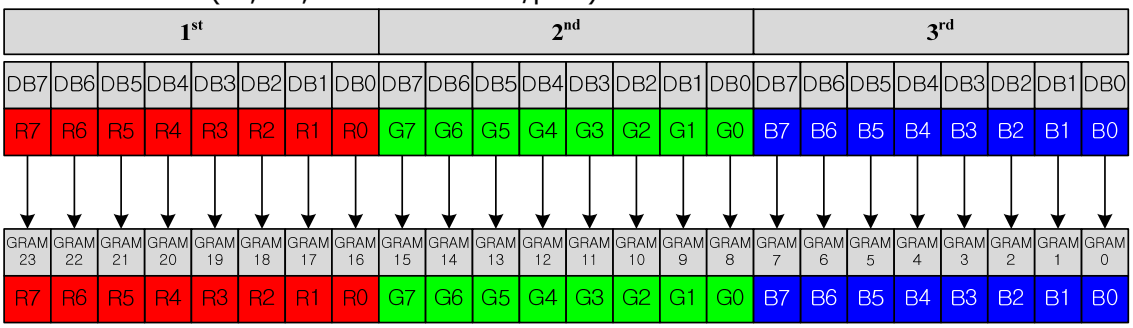
- 2-Transfers (65,536 Colors 16-bits/pixel)



- 3-Transfers (262,144 Colors 18-bits/pixel)

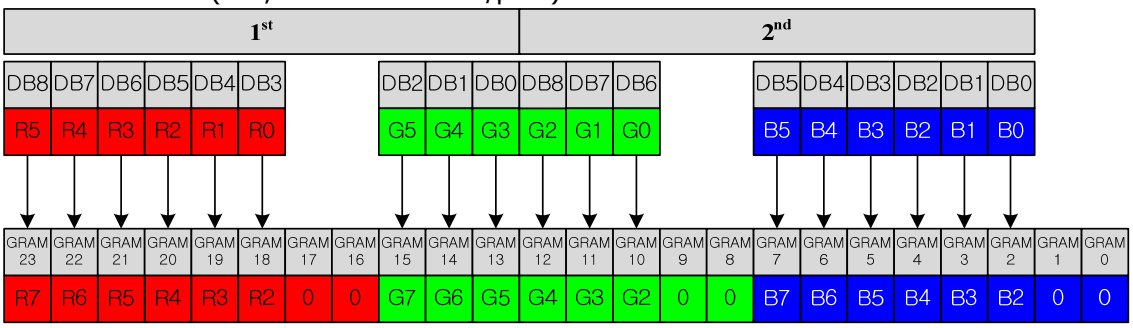


- 3-Transfers (16,777,216 Colors 24-bits/pixel)



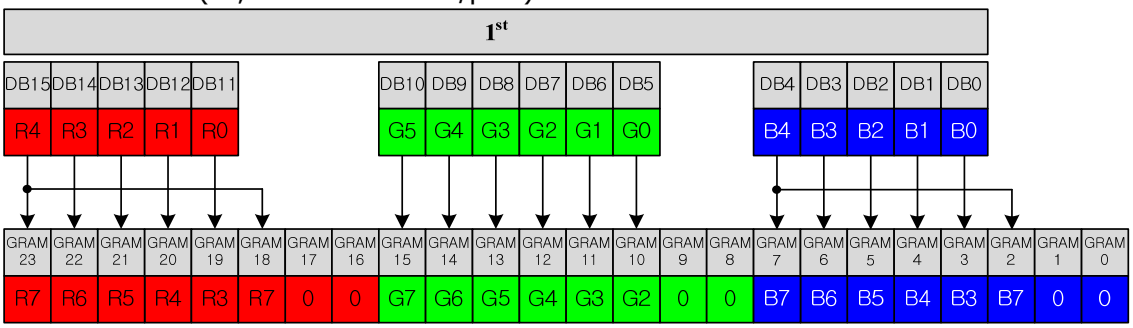
9-bit Interface

- 2-Transfers (262,144 Colors 18-bits/pixel)

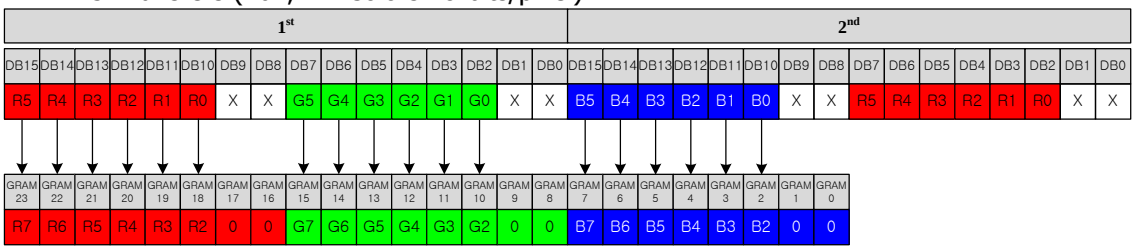


16-bit Interface

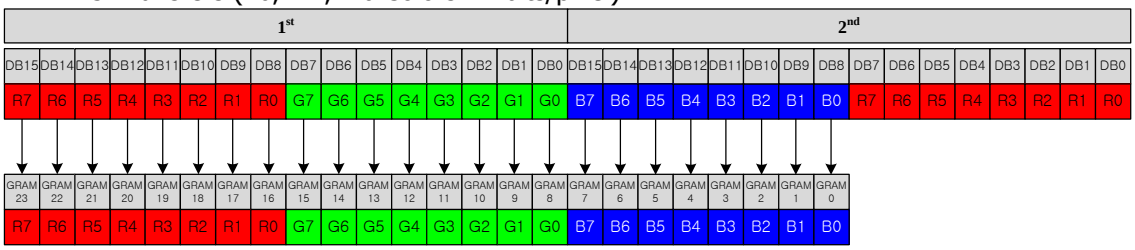
- 1-Transfer (65,536 Colors 16-bits/pixel)



- 1.5-Transfers (262,144 Colors 18-bits/pixel)

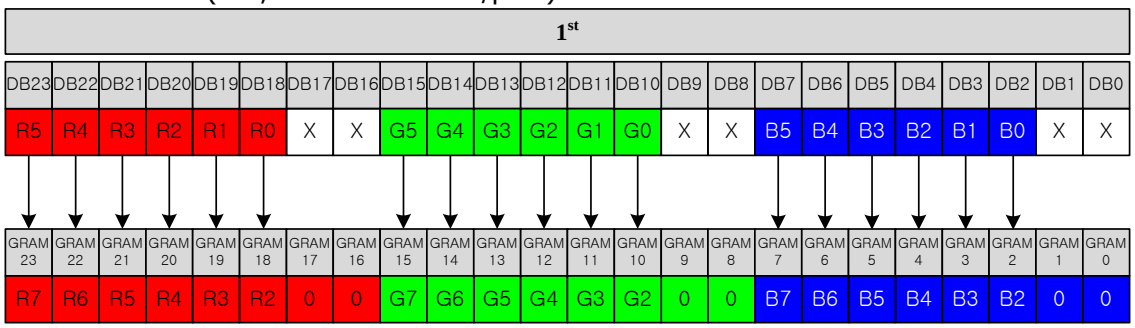


- 1.5-Transfers (16,777,216 Colors 24-bits/pixel)



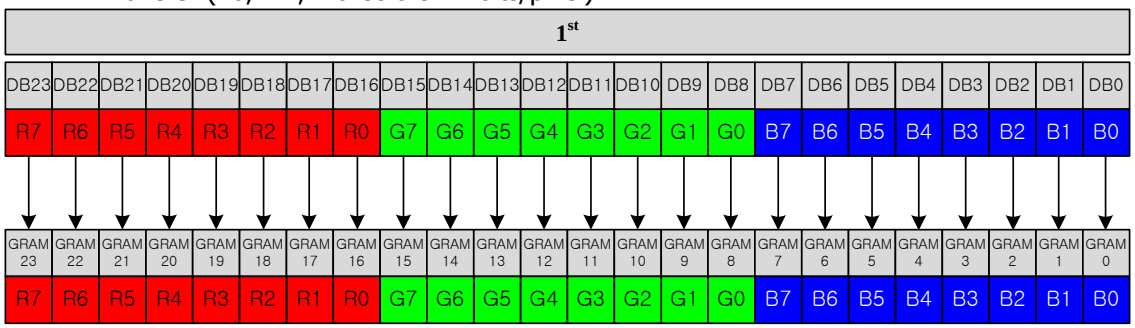
18-bit Interface

- 1-Transfer (262,144 Colors 18-bits/pixel)



24-bit Interface

- 1-Transfer (16,777,216 Colors 24-bits/pixel)



5.3 MIPI DBI Type C

The LG4572B supports MIPI DBI type C (4-wire 9-bit serial interface).

5.3.1 Write Cycle Sequence

During a write cycle the host processor sends a single bit of data to the display module via the interface. The type C interface utilizes nCS, SCK and SDI signals. SCK is driven from high to low then pulled back to high during the write cycle. The host processor provides information during the write cycle while the display module reads the host processor information on the rising edge of SCK.

The following figure shows the write cycle for the type C interface.

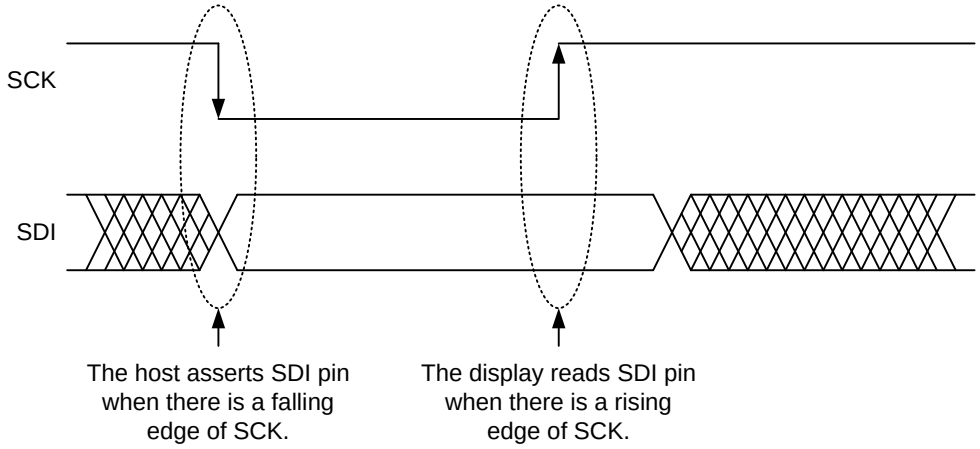


Figure 19. DBI Type C Interface Write Cycle

Note: SCK is an unsynchronized signal; it can be stopped.

During the write sequence the host processor writes one or more bytes of information to the display module via the interface. The write sequence is initiated when nCS is driven from high to low and ends when nCS is pulled high. Each byte is nine write cycles in length.

The type C interface write sequences is described in Figure 20.

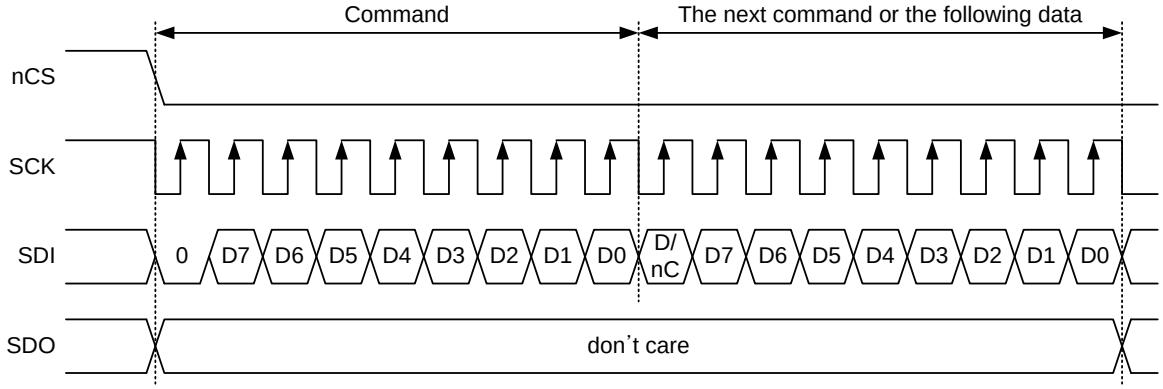


Figure 20. DBI Type C Interface Write Sequence

5.3.2 Read Cycle Sequence

During a read cycle the host processor reads a single bit of data from the display module via the interface. The type C interface utilizes nCS, SCK and SDO signals. SCK is driven from high to low then pulled back to high during the read cycle. The display module provides information during the read cycle while the host processor reads the display module information on the rising edge of SCK.

Figure 21 shows the read cycle for the type C interface.

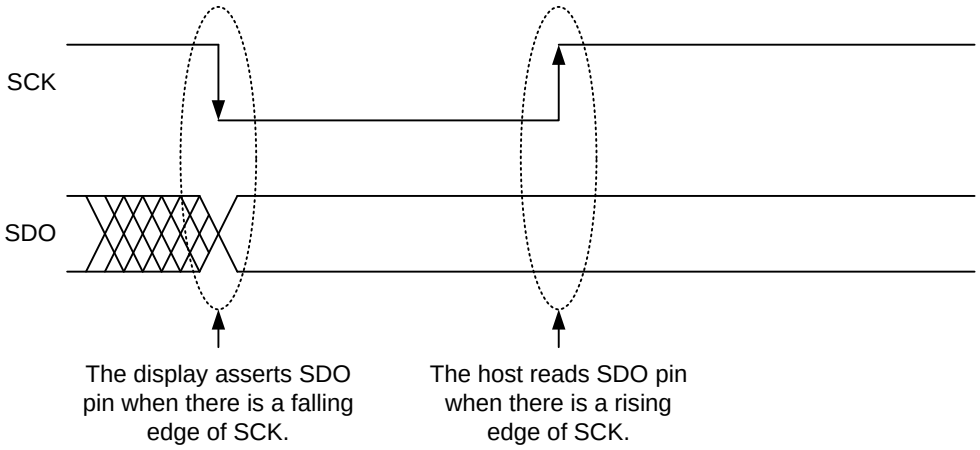


Figure 21. DBI Type C Interface Read Cycle

Note: SCK is an unsynchronized signal; it can be stopped.

During the read sequence the host processor reads one or more bytes of information from the display module via the interface. The read sequence is initiated when nCS is driven from high to low and ends when nCS is pulled high. Each byte is nine read cycles in length.

The type C interface read sequence is shown in Figure 22.

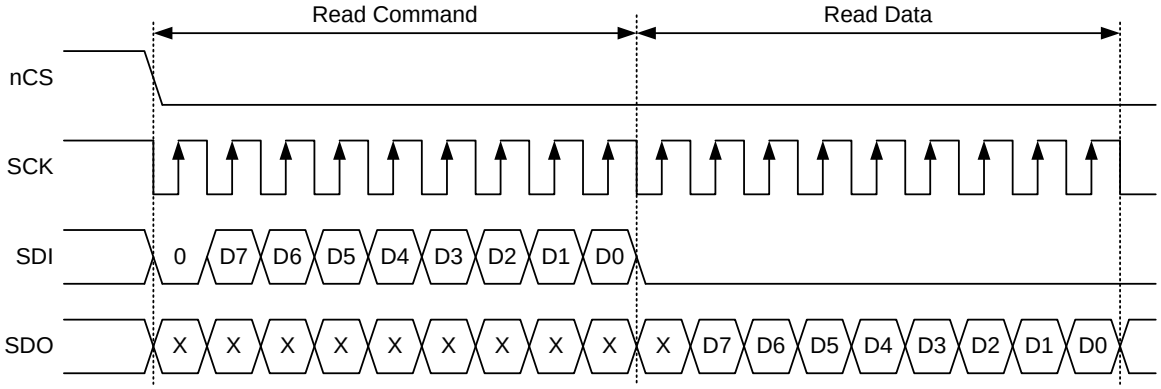


Figure 22. DBI Type C Interface Read Sequence

5.3.3 Break and Pause of Sequences

The host processor can break a read or write sequence by pulling the nCS signal high during a command or data byte. The display module shall reset its interface so it will be ready to receive the same byte when nCS is again driven low.

The host processor can pause a read or write sequence by pulling the nCS signal high between command or data bytes. The display module shall wait for the host processor to drive nCS low before continuing the read or write sequence at the point where the sequence was paused.

5.3.4 Data Transfer Break

As shown in the figure below, in the transmission of parameter for command from the host processor to the LG4572B, the command parameters sent to the LG4572B before the break occurs are stored in the register of the LG4572B when the following two conditions are met. One is that a break occurs before the last parameter of the command is sent to the LG4572B. The

other is that the host processor transmits the parameter(s) of a new command, not the parameters of the interrupted command, when the break occurs.
However, those parameters sent after the break is disregarded, and the data in the register is not overwritten.

Note : A break is occurred, for example, by other command input.

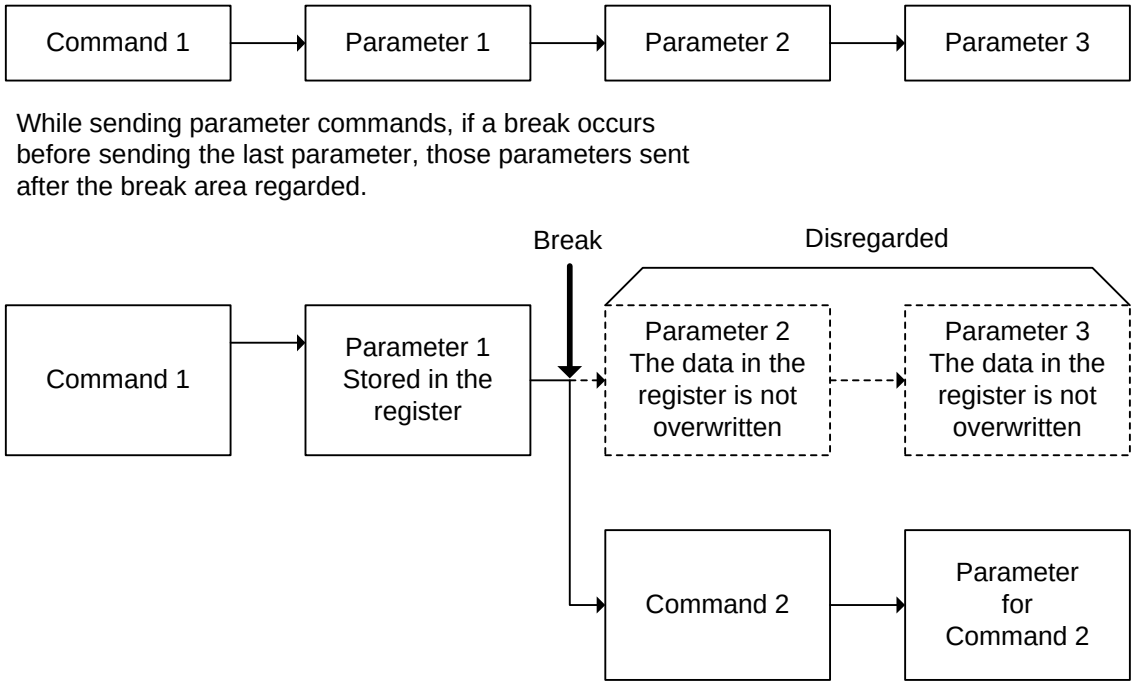


Figure 23. Diagram of data transfer break sequence

5.4 MIPI DPI-2

5.4.1 Interface Signals

Table 1. Interface Signals for DPI

Symbol	Name	I/O	Description
VSYNC	Vertical sync	I	Vertical synchronization timing signal
HSYNC	Horizontal sync	I	Horizontal synchronization timing signal
DE	Data enable	I	Data enable signal (assertion indicates valid pixels)
PCLK	Pixel Clock	I	Pixel clock for capturing pixels at display interface
DB[15:0], DB[17:0] or DB[23:0]	Pixel Data	I	Pixel data in 16-bit, 18-bit, or 24-bit format

5.4.2 Interface Color Coding

Table 2 specifies the mapping of data bits, as components of primary pixel color values R, G, and B, to signal lines at the interface.

Note: LG4572B supports configuration 1 and 3 for 16-bit pixels, configuration 1 and 2 for 18-bit pixels and 24-bit pixels. 3Ah and B1h are the related registers.

Table 2. Interface Color Coding

Signal Line	16-bit			18-bit		24-bit
	Configuration 1	Configuration 2	Configuration 3	Configuration 1	Configuration 2	
D23	(not used)	~~(not used)~~	(not used)	(not used)	(not used)	R7
D22	(not used)	~~(not used)~~	(not used)	(not used)	(not used)	R6
D21	(not used)	~~(not used)~~	R4	(not used)	R5	R5
D20	(not used)	~~R4~~	R3	(not used)	R4	R4
D19	(not used)	~~R3~~	R2	(not used)	R3	R3
D18	(not used)	~~R2~~	R1	(not used)	R2	R2
D17	(not used)	~~R1~~	R0	R5	R1	R1
D16	(not used)	~~R0~~	(not used)	R4	R0	R0
D15	R4	~~(not used)~~	(not used)	R3	(not used)	G7
D14	R3	~~(not used)~~	(not used)	R2	(not used)	G6
D13	R2	~~G5~~	G5	R1	G5	G5
D12	R1	~~G4~~	G4	R0	G4	G4
D11	R0	~~G3~~	G3	G5	G3	G3
D10	G5	~~G2~~	G2	G4	G2	G2
D9	G4	~~G1~~	G1	G3	G1	G1
D8	G3	~~G0~~	G0	G2	G0	G0
D7	G2	~~(not used)~~	(not used)	G1	(not used)	B7
D6	G1	~~(not used)~~	(not used)	G0	(not used)	B6
D5	G0	~~(not used)~~	B4	B5	B5	B5
D4	B4	~~B4~~	B3	B4	B4	B4
D3	B3	~~B3~~	B2	B3	B3	B3
D2	B2	~~B2~~	B1	B2	B2	B2
D1	B1	~~B1~~	B0	B1	B1	B1
D0	B0	~~B0~~	(not used)	B0	B0	B0

There are three mappings for 16-bit pixels to data signals, two mappings for 18-bit pixels to data signals, and one mapping for 24-bit pixels to data signals.

Notes:
Pixel values are specified as triplets for primary color components R, G, and B: R = Red, G = Green, B = Blue. R0 is the LSB for the red component, G0 is LSB for the green component, etc.
For 16-bit pixels, R primary color MSB is R4, R primary color LSB is R0; G primary color MSB is G5, G primary color LSB is G0; B primary color MSB is B4 and B primary color LSB is B0.
For 18-bit pixels, R primary color MSB is R5, R primary color LSB is R0; G primary color MSB is G5, G primary color LSB is G0; B primary color MSB is B5 and B primary color LSB is B0.
For 24-bit pixels, R primary color MSB is R7, R primary color LSB is R0; G primary color MSB is G7, G primary color LSB is G0; B primary color MSB is B7 and B primary color LSB is B0.

5.4.3 Interface Timing Parameter

In normal operation, systems based on DPI architecture rely on the host processor to continuously provide complete frames of image data at a sufficient frame rate to avoid flicker or other visible artifacts.

The displayed image, or *frame*, is comprised of a rectangular array of pixels. The frame is transmitted from the host processor to a display module as a sequence of pixels, with each horizontal line of the image data sent as a group of consecutive pixels.

Vsync indicates the beginning of each frame of the displayed image.

Hsync signals the beginning of each horizontal line of pixels.

Each pixel value (16-, 18-, or 24-bit data) is transferred from the host processor to the display module during one pixel period. The rising edge of PCLK is used by the display module to capture pixel data. Since PCLK runs continuously, control signal DE is required to indicate when valid pixel data is being transmitted on the pixel data signals. Figure 35 defines timing parameters for DPI operation.

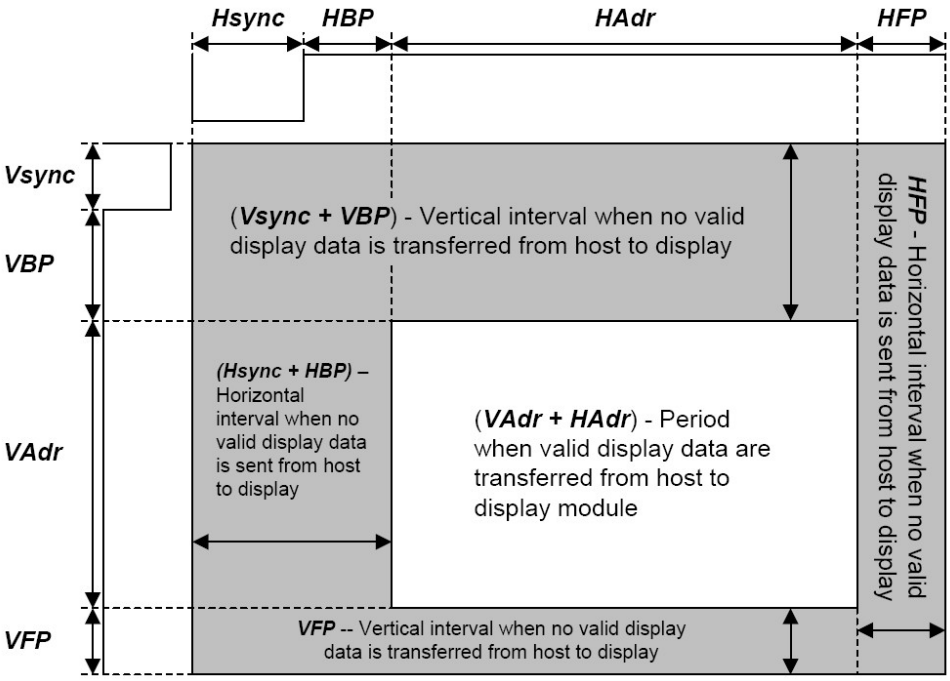


Figure 24. DPI Parameter

Table 3. Interface Signals for DPI

Parameters	Symbols	Min.	Step	Max.	Unit
Horizontal Synchronization	Hsync	1	1	-	PCLK
Horizontal Back Porch	HBP	1	1	-	PCLK
Horizontal Address	HAdr	240 (320, 360)	-	480	PCLK
Horizontal Front Porch	HFP	1	1	-	PCLK
Vertical Synchronization	Vsync	1	1	-	Line
Vertical Back Porch	VBP	1	1	-	Line
Vertical Address	VAdr	176	4	864	Line
Vertical Front Porch	VFP	1	1	-	Line

Notes:

1. Vertical period (one frame) shall be equal to the sum of Vsync + VBP + VAdr + VFP.
2. Horizontal period (one line) shall be equal to the sum of Hsync + HBP + HAdr + HFP.
3. Control signals PCLK and Hsync shall be transmitted as specified at all times while valid pixels are transferred between the host processor and the display module.

5.5 SPI (Serial Peripheral Interface)

The serial interface is selected by setting the IM[2:0] = 110x for register access while MIPI DPI/DSI is used for pixel data streaming LG4572B. The data is transferred via chip select line (nCS), serial transfer clock line (SCK), serial data input line (SDI), and serial data output line (SDO). In serial interface operation, the IM[0] pin functions as the ID pin, and the DB[23:0] pins, not used in this mode, must be fixed at either IOVCC or GND level.

The LG4572B recognizes the start of data transfer on the falling edge of nCS input and starts transferring the start byte. It recognizes the end of data transfer on the rising edge of nCS input. The LG4572B is selected when the 6-bit chip address in the start byte transferred from the transmission unit and the 6-bit device identification code assigned to the LG4572B are compared and both 6-bit data match, and then the LG4572B starts taking in data. The least significant bit of the device identification code is set with the ID pin. Send "01110" to the five upper bits of the device identification code. Two different chip addresses must be assigned to the LG4572B because the seventh bit of the start byte is assigned to the register select bit (RS). When RS = 0, an index register write operation is executed. When RS = 1, either an instruction write operation or a RAM read/write operation is executed. The eighth bit of the start byte is to select either read or write operation (R/W bit). The LG4572B receives data when the R/W = 0, and transfers data when the R/W = 1.

After receiving the start byte, the LG4572B starts transferring or receiving data in units of bytes. The LG4572B executes data transfer from the MSB.

Table 4. Start Byte Format

Transferred bits	1	2	3	4	5	6	7	8
Start byte format	Device ID code						RS	R/W
	0	1	1	1	0	IM[0]		

Note: ID bit is selected by setting the IM0/ID pin.

Table 5.

RS	R/W	Function
0	0	Set an index register
~~0~~	~~1~~	~~Read a status~~
1	0	Write an instruction or RAM data
1	1	Read an instruction or RAM data

5.5.1 Write Cycle Sequence

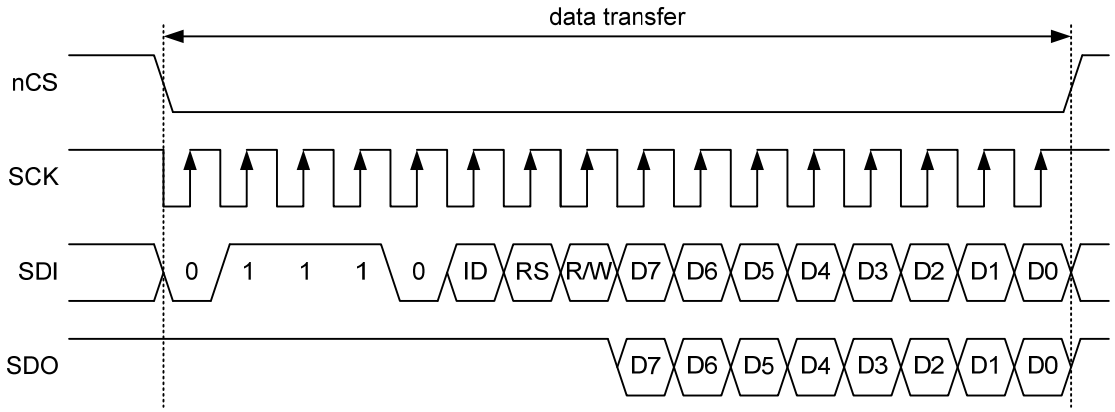


Figure 25. SPI Interface

The following figures demonstrate the serial reading operation in the FAh register for example.

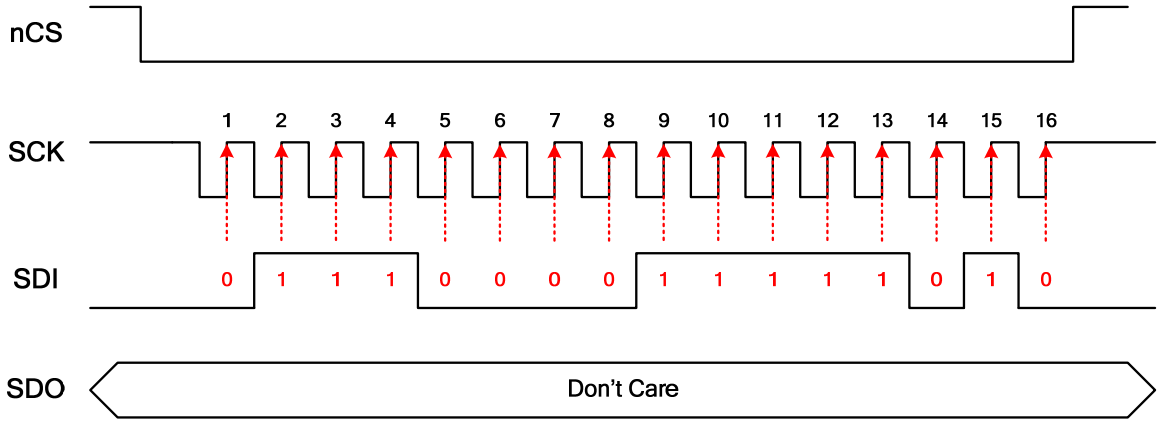


Figure 26. Example for serial data reading

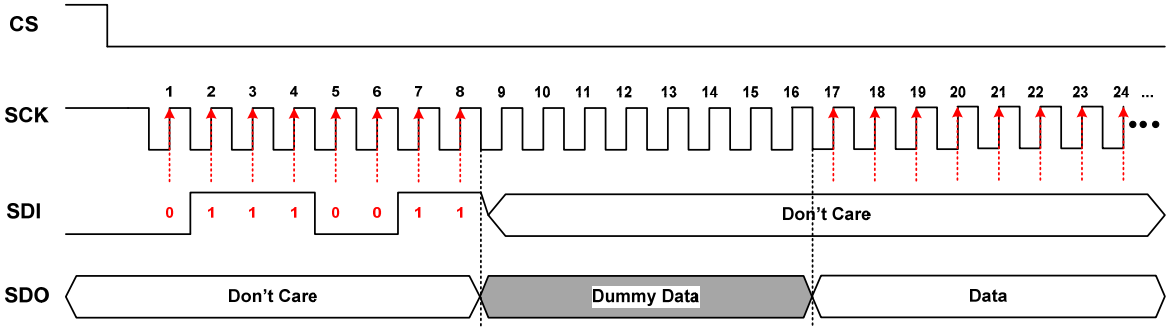


Figure 27. Example for serial data reading – continued

5.6 MIPI DSI

DSI specifies the interface between a host processor and a peripheral such as a display module. It builds on existing MIPI Alliance specifications by adopting pixel formats and command set specified in DPI-2, DBI-2 and DCS standards.

Figure 28 shows a simplified DSI interface. From a conceptual viewpoint, a DSI-compliant interface performs the same functions as interfaces based on DBI-2 and DPI-2 standards or similar parallel display interfaces. It sends pixels or commands to the peripheral, and can read back status or pixel information from the peripheral. The main difference is that DSI serializes all pixel data, commands, and events that, in traditional or legacy interfaces, are normally conveyed to and from the peripheral on a parallel data bus with additional control signals.

From a system or software point of view, the serialization and deserialization operations should be transparent. The most visible, and unavoidable, consequence of transformation to serial data and back to parallel is increased latency for transactions that require a response from the peripheral. For example, reading a pixel from the frame buffer on a display module has a higher latency using DSI than DBI. Another fundamental difference is the host processor's inability during a read transaction to throttle the rate, or size, of returned data.

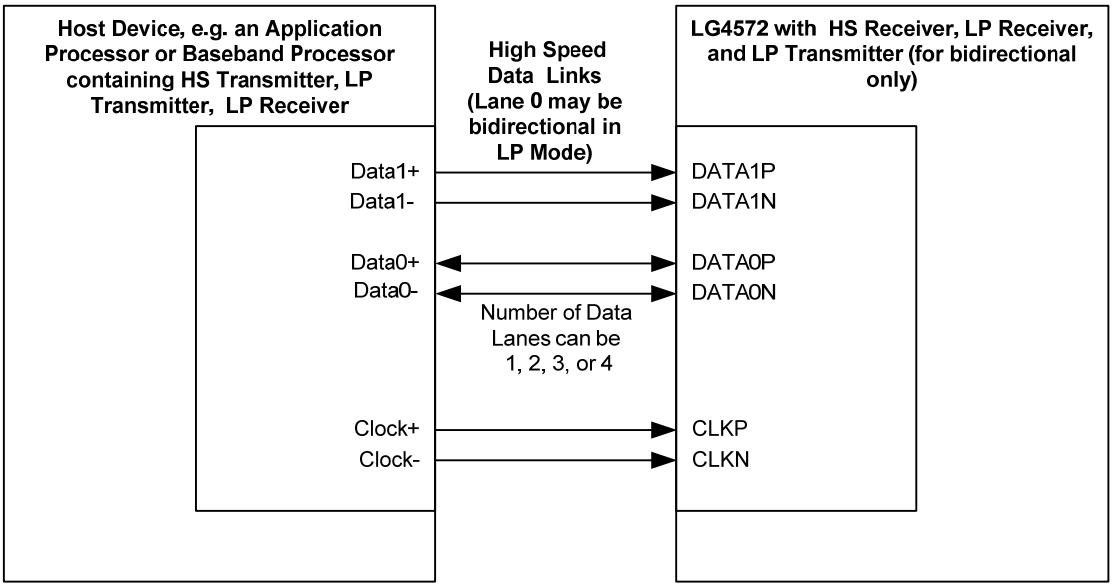


Figure 28. MIPI DSI Transmitter and Receiver Interface

5.6.1 DSI Layer Definitions

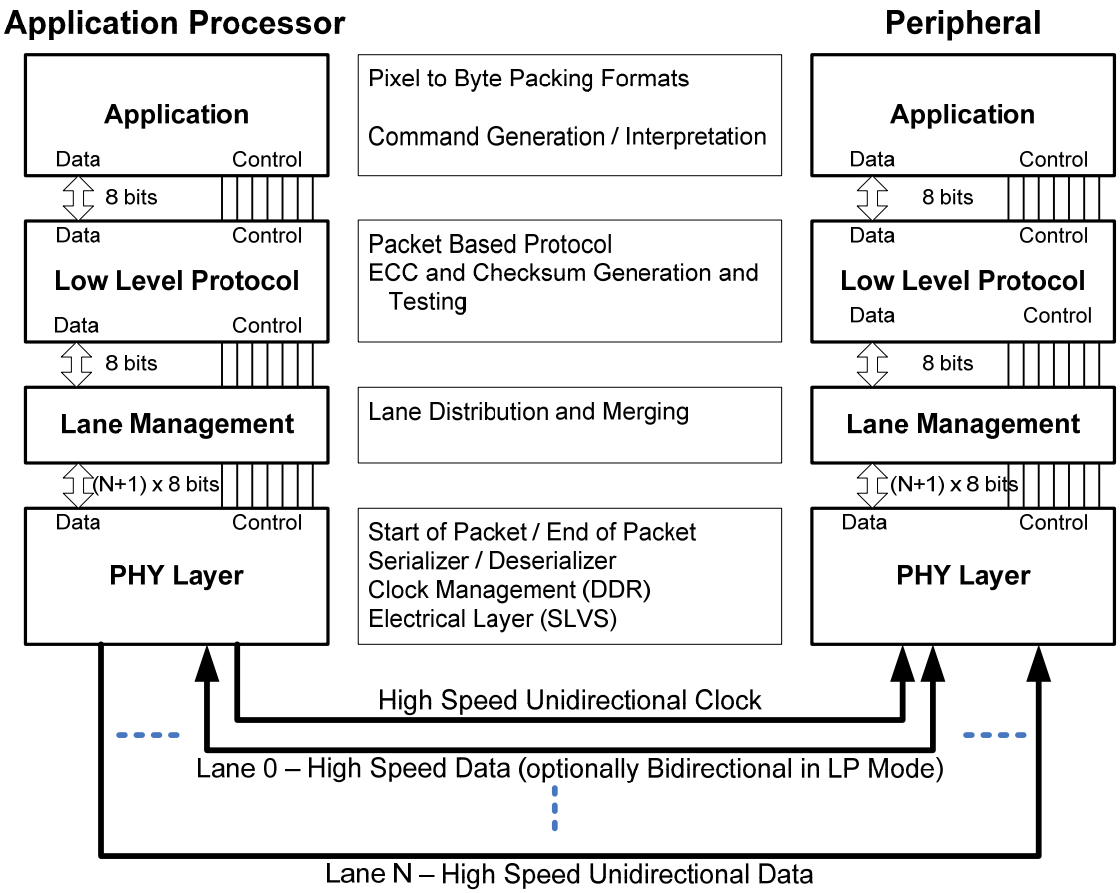


Figure 29. DSI Layers

A conceptual view of DSI organizes the interface into several functional layers. A description of the layers follows and is also shown in Figure 29.

PHY Layer: The PHY Layer specifies transmission medium (electrical conductors), the input/output circuitry and the clocking mechanism that captures "ones" and "zeroes" from the serial bit stream. This part of the specification documents the characteristics of the transmission medium, electrical parameters for signaling and the timing relationship between clock and Data Lanes.

The mechanism for signaling Start of Transmission (SoT) and End of Transmission (EoT) is specified, as well as other "out of band" information that can be conveyed between transmitting and receiving PHYs. Bit-level and byte-level synchronization mechanisms are included as part of the PHY. Note that the electrical basis for DSI (SLVS) has two distinct modes of operation, each with its own set of electrical parameters.

The PHY layer is described in *MIPI Alliance Specification for D-PHY*.

Lane Management Layer: DSI is Lane-scalable for increased performance. The number of data signals may be 1, 2, 3, or 4 depending on the bandwidth requirements of the application. The transmitter side of the interface distributes the outgoing data stream to one or more Lanes ("distributor" function). On the receiving end, the interface collects bytes from the Lanes and merges them together into a recombined data stream that restores the original stream sequence ("merger" function).

Protocol Layer: At the lowest level, DSI protocol specifies the sequence and value of bits and bytes traversing the interface. It specifies how bytes are organized into defined groups called packets. The protocol defines required headers for each packet, and how header information is generated and

interpreted. The transmitting side of the interface appends header and error-checking information to data being transmitted. On the receiving side, the header is stripped off and interpreted by corresponding logic in the receiver. Error-checking information may be used to test the integrity of incoming data. DSI protocol also documents how packets may be tagged for interleaving multiple command or data streams to separate destinations using a single DSI.

Application Layer: This layer describes higher-level encoding and interpretation of data contained in the data stream. Depending on the display subsystem architecture, it may consist of pixels having a prescribed format, or of commands that are interpreted by the display controller inside a display module. The DSI specification describes the mapping of pixel values, commands and command parameters to bytes in the packet assembly. See *MIPI Alliance Standard for Display Command Set (DCS)*.

5.6.2 Command and Video Modes

DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode. Which mode is used depends on the architecture and capabilities of the peripheral. The mode definitions reflect the primary intended use of DSI for display interconnect, but are not intended to restrict DSI from operating in other applications.

Typically, a peripheral is capable of Command Mode operation or Video Mode operation. Some Video Mode display modules also include a simplified form of Command Mode operation in which the display module may refresh its screen from a reduced-size, or partial, frame buffer, and the interface (DSI) to the host processor may be shut down to reduce power consumption.

Command Mode

Command Mode refers to operation in which transactions primarily take the form of sending commands and data to a peripheral, such as a display module, that incorporates a display controller. The display controller may include local registers and a frame buffer. Systems using Command Mode write to, and read from, the registers and frame buffer memory. The host processor indirectly controls activity at the peripheral by sending commands, parameters and data to the display controller. The host processor can also read display module status information or the contents of the frame memory. Command Mode operation requires a bidirectional interface.

Video Mode

Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode.

Some Video Mode architectures may include a simple timing controller and partial frame buffer, used to maintain a partial-screen or lower-resolution image in standby or Low Power Mode. This permits the interface to be shut down to reduce power consumption.

To reduce complexity and cost, systems that only operate in Video Mode may use a unidirectional data path.

Virtual Channel Capability

While this specification only addresses the connection of a host processor to a single peripheral, DSI incorporates a virtual channel capability for communication between a host processor and multiple, physical display modules. Display modules are completely independent, may operate simultaneously, and may be of different display architecture types, limited only by the total bandwidth available over the shared DSI Link. The details of connecting multiple peripherals to a single Link are beyond the scope of this document.

Since interface bandwidth is shared between peripherals, there are constraints that limit the physical extent and performance of multiple-peripheral systems.

The DSI protocol permits up to four virtual channels, enabling traffic for multiple peripherals to share a common DSI Link. In some high-resolution display designs, multiple physical drivers serve different areas of a common display panel. Each driver is integrated with its own display controller that connects to the host processor through DSI. Using virtual channels, the display controller directs data to the individual drivers, eliminating the need for multiple interfaces or complex multiplexing schemes.

5.6.3 DSI Physical Layer (D-PHY)

The LG4572B supports MIPI D-PHY specification of Version 0.90.00 – 8 October 2007.

The D-PHY provides a synchronous connection between Master and Slave. A practical PHY Configuration consists of a clock signal and one or more data signals. The clock signal is unidirectional, originating at the Master and terminating at the Slave. The data signals can either be unidirectional or bi-directional depending on the selected options. For half-duplex operation, the reverse direction bandwidth is one-fourth of the forward direction bandwidth. Token passing is used to control the communication direction of the Link.

The Link includes a High-Speed signaling mode for fast-data traffic and a Low-Power signaling mode for control purposes. Optionally, a Low-Power Escape mode can be used for low speed asynchronous data communication. High speed data communication appears in bursts with an arbitrary number of payload data bytes.

The PHY uses two wires per Data Lane plus two wires for the Clock Lane. This gives four wires for the minimum PHY configuration. In High-Speed mode each Lane is terminated on both sides and driven by a low-swing, differential signal. In Low-Power mode all wires are operated single-ended and non-terminated. For EMI reasons, the drivers for this mode shall be slew-rate controlled and current limited.

The maximum bit rate in High-Speed mode of the LG4572B is **330** Mbps per Lane.[8] For a fixed clock frequency, the available data capacity of a PHY Configuration can be increased by using more Data Lanes. Effective data throughput can be reduced by employing burst mode communication. The maximum data rate in Low-Power mode is 10Mbps.

5.6.4 Interconnect

The following Figure 30 and Figure 31 show the pad connection to the TFT-LCD panel which is proposed to be driven by LG4572B. From this, we recommend, for better performance, that the resistance from pads to wires is as small as possible. For the best performance, we recommend the R_{TAB} + R_{OLB} + R_{FOG} resistance values of MIPI power block pad are below 5 ohms for each. And the those of communication pad are recommended to below 5 ohms for each to minimize the influence of the impedance matching of high-speed receiver blocks, and to reduce the external resistance load of the low-power transmitter block.

[8] The actual maximum achievable bit rate in High-Speed mode is determined by the performance of transmitter, receiver and interconnect implementations. Therefore, the maximum bit rate is not specified in the D-PHY specification.

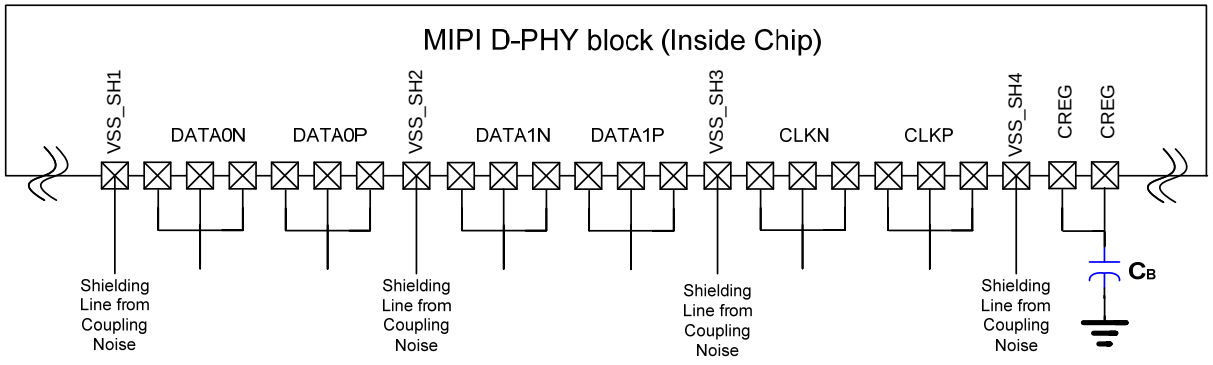


Figure 30. Pad connection from MIPI block (inside chip) to the external power capacitor of CB1 and clock/data wires.

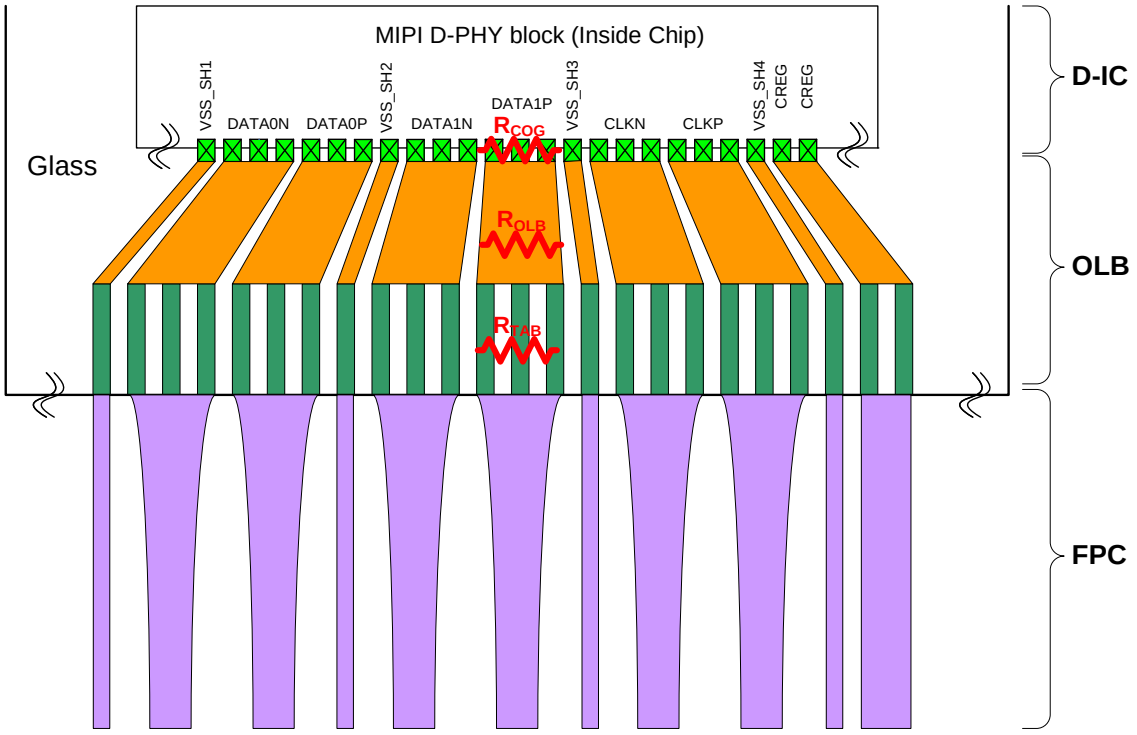


Figure 31. Consideration of the Resistance. R_{COG} + R_{OLB} + R_{FOG} < 10ohm. Assuming the other resistances of FPC patterns or connectors are negligibly small.

5.6.5 D-PHY Signal Voltage Levels & Speed

There are two signaling voltage levels for D-PHY. As shown in the following figure, one is 1.2V voltage level signaling for a low-speed data transmission(LP:Low Power, under 10Mbps) and the other is 200mV peak-to-peak voltage swing level for a high-speed data transmission(HS:High Speed, Up to **330**Mbps). Generally, the LP signaling is used for a command transmission and a read operation(from peripheral to host), and the HS signaling is used for an image data transmission.

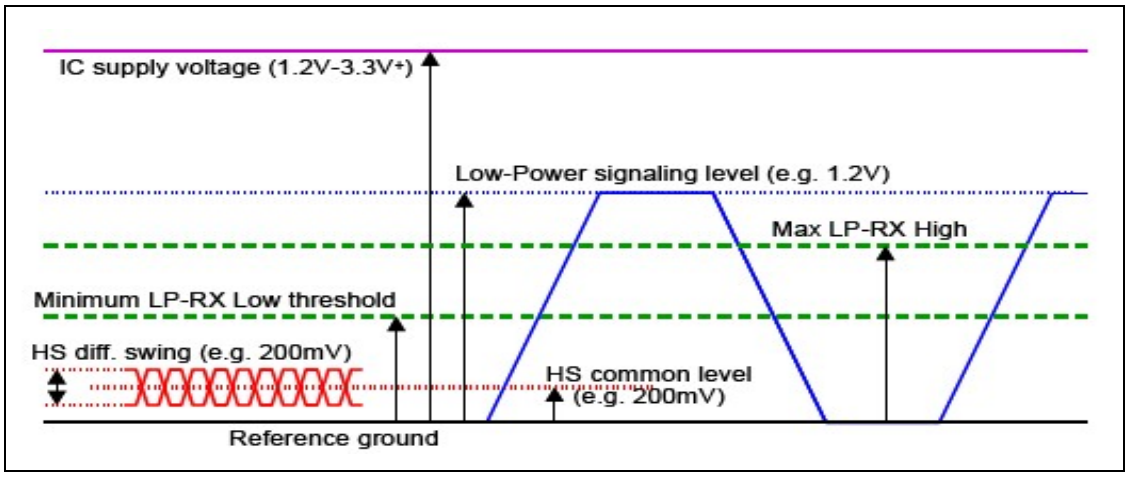


Figure 32. Line Voltage Levels of D-PHY

5.6.6 High Speed Data Transmission with D-PHY

If a host processor want to transmit some data using D-PHY in high speed mode, as shown in the following figure, the host must follow the following sequences.

- SoT sequence → DSI Data Packets → EoT sequence
- SoT sequence : LP-11 → LP-01 → LP-00($T_{HS-PREPARE}$) → HS-0($T_{HS-ZERO}$) → Sync Command '00011101'($T_{HS-SYNC}$)
- EoT sequence : Toggles the Last data and keeps for a time $T_{HS-TRAIL}$ → LP-11

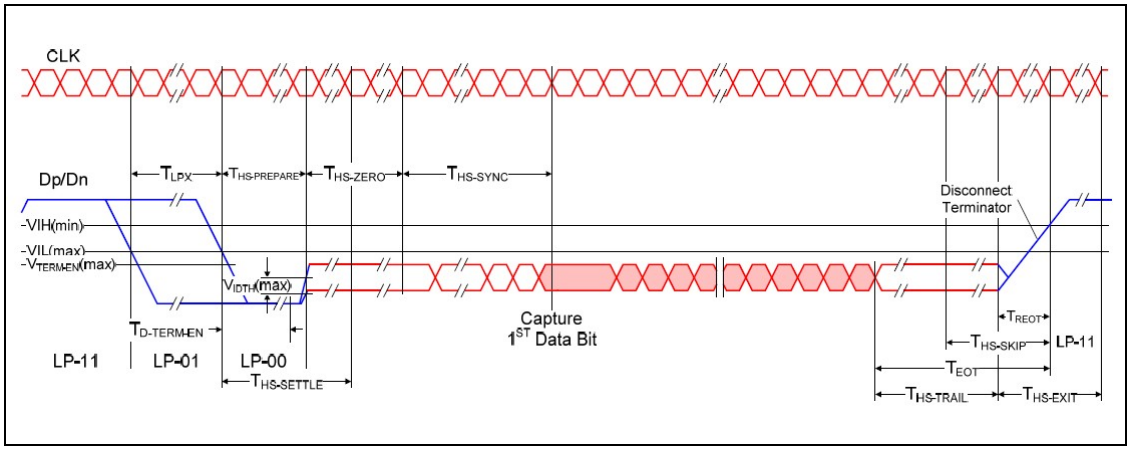


Figure 33. High Speed Data Transmission Sequence with D-PHY

5.6.7 Low Power Data Transmission with D-PHY

If a host processor want to transmit some data using D-PHY low power mode, as shown in the following figure, the host must follows the sequence below.

- Escape Mode Entry → LPDT Command '11100001' → DSI Data Packets → Exit Escape
- Escape Mode Entry : LP-11 → LP-10 → LP-00 → LP-01 → LP-00
- Exit Escape : LP-10 → LP-11

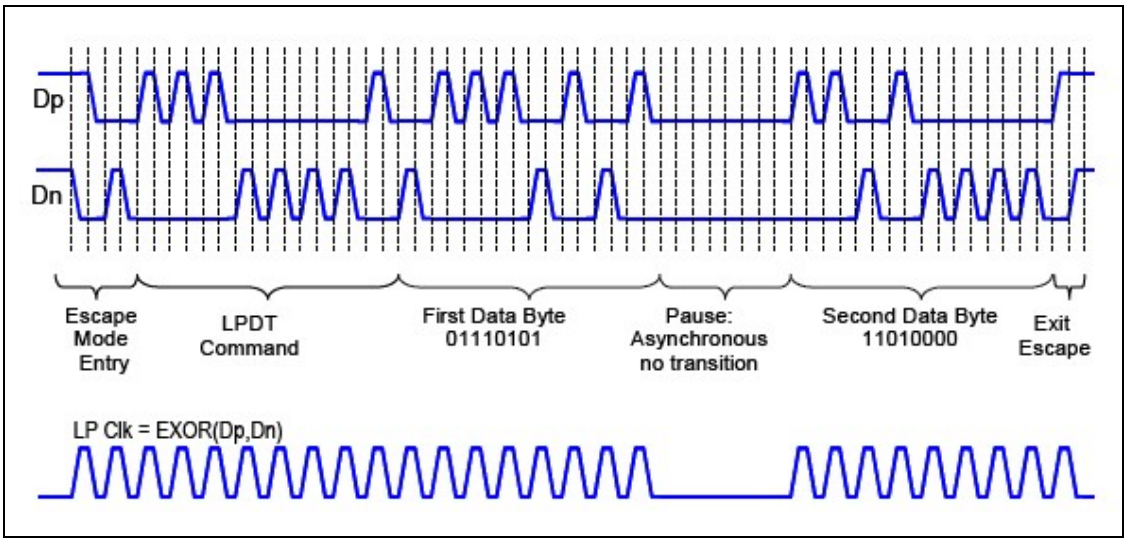


Figure 34. Low Power Data Transmission Sequence with D-PHY

5.6.8 DSI Protocol

On the transmitter side of a DSI Link, parallel data, signal events, and commands are converted in the Protocol layer to packets, following the packet organization documented in this section. The Protocol layer appends packet-protocol information and headers, and then sends complete bytes through the Lane Management layer to the PHY. Packets are serialized by the PHY and sent across the serial Link. The receiver side of a DSI Link performs the converse of the transmitter side, decomposing the packet into parallel data, signal events and commands.

General Packet Structure

Two packet structures are defined for low-level protocol communication: Long packets and Short packets. For both packet structures, the Data Identifier is always the first byte of the packet.

Long Packet Format

Figure 35 shows the structure of the Long packet. A Long packet shall consist of three elements: a 32-bit Packet Header (PH), an application-specific Data Payload with a variable number of bytes, and a 16-bit Packet Footer (PF). The Packet Header is further composed of three elements: an 8-bit Data Identifier, a 16-bit Word Count, and 8-bit ECC. The Packet Footer has one element, a 16-bit checksum. Long packets can be from 6 to 65,541 bytes in length.

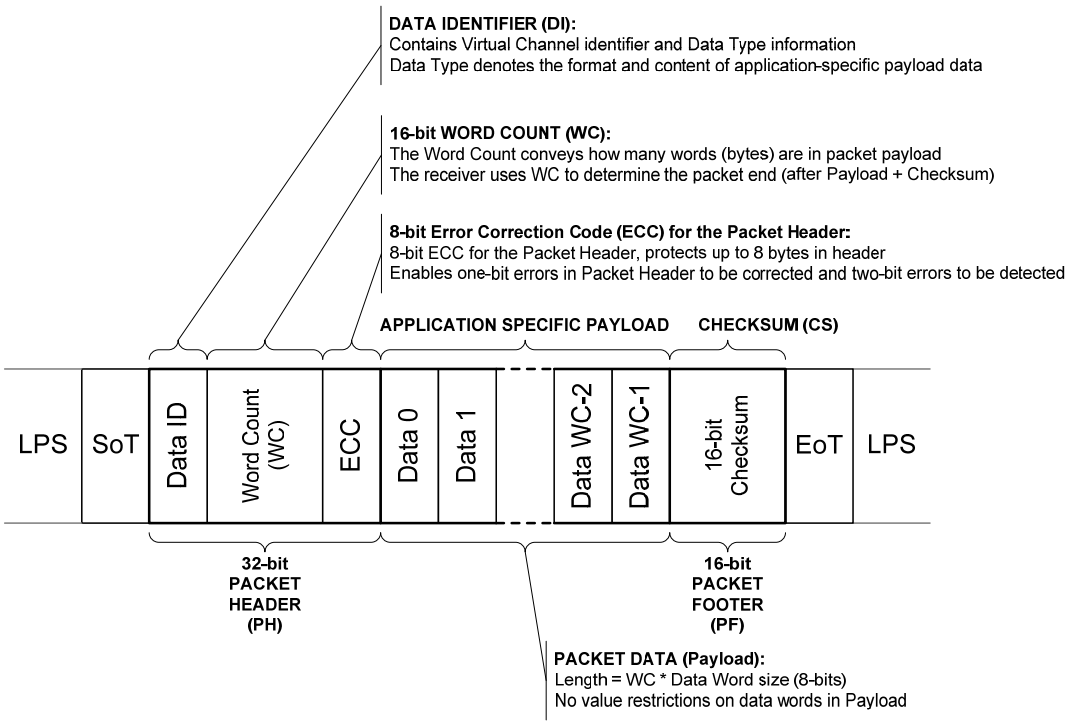


Figure 35. Long Packet Structure

Short Packet Format

Figure 36 shows the structure of the Short packet. A Short packet shall contain an 8-bit Data ID followed by two command or data bytes and an 8-bit ECC; a Packet Footer shall not be present. Short packets shall be four bytes in length.

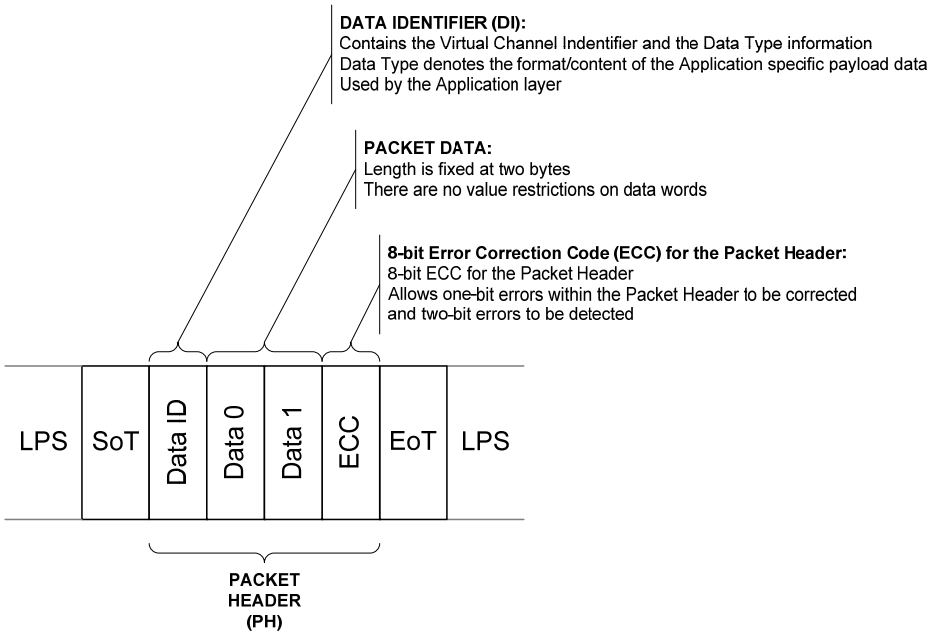


Figure 36. Short Packet Structure

Data Identifier Byte

The first byte of any packet is the DI (Data Identifier) byte.

DI[7:6]: These two bits identify the data as directed to one of four virtual channels.

DI[5:0]: These six bits specify the Data Type.

Table 6. Data Types for Processor-sourced Packets

Data Type, hex	Data Type, binary	Description	Packet Size
01h	00 0001	Sync Event, V Sync Start	Short
11h	01 0001	Sync Event, V Sync End	Short
21h	10 0001	Sync Event, H Sync Start	Short
31h	11 0001	Sync Event, H Sync End	Short
08h	00 1000	End of Transmission packet (EoTp)	Short
02h	00 0010	Color Mode (CM) Off Command	Short
12h	01 0010	Color Mode (CM) On Command	Short
22h	10 0010	Shut Down Peripheral Command	Short
32h	11 0010	Turn On Peripheral Command	Short
03h	00 0011	Generic Short WRITE, no parameters	Short
13h	01 0011	Generic Short WRITE, 1 parameter	Short
23h	10 0011	Generic Short WRITE, 2 parameters	Short
04h	00 0100	Generic READ, no parameters	Short
14h	01 0100	Generic READ, 1 parameter	Short
24h	10 0100	Generic READ, 2 parameters	Short
05h	00 0101	DCS Short WRITE, no parameters	Short
15h	01 0101	DCS Short WRITE, 1 parameter	Short
06h	00 0110	DCS READ, no parameters	Short
37h	11 0111	Set Maximum Return Packet Size	Short
09h	00 1001	Null Packet, no data	Long
19h	01 1001	Blanking Packet, no data	Long
29h	10 1001	Generic Long Write	Long
39h	11 1001	DCS Long Write/write_LUT Command Packet	Long
0Eh	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
1Eh	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
2Eh	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
3Eh	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long
x0h and xFh, unspecified	xx 0000 xx 1111	DO NOT USE All unspecified codes are reserved	

Error Correction Code

The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header. The host processor shall always calculate and transmit an ECC byte. Peripherals shall support ECC in both forward- and reverse-direction communications.

Video Mode Packed Pixel Stream

There are several data packet structure for pixel data transmission, 16-bit (5-6-5) format, two 18-bit (6-6-6) formats, 24-bit format (8-8-8) and each data packet structure is shown in the following figures.

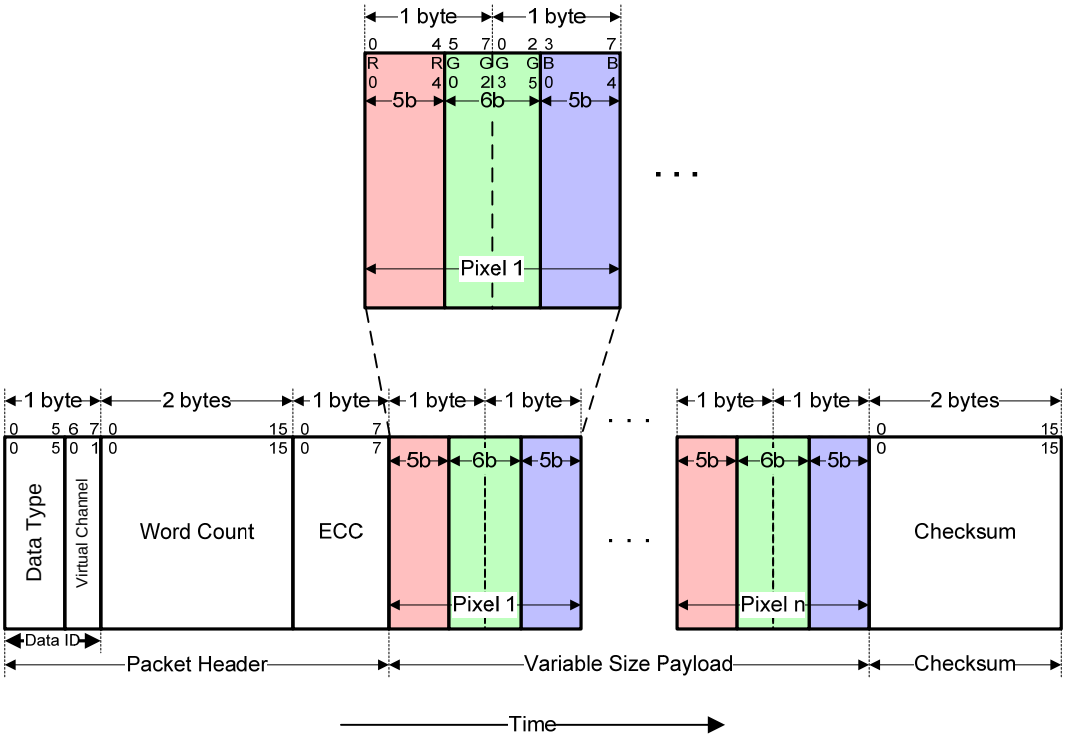


Figure 37. Packed Pixel Stream, 16-bit RGB, 5-6-5 Format

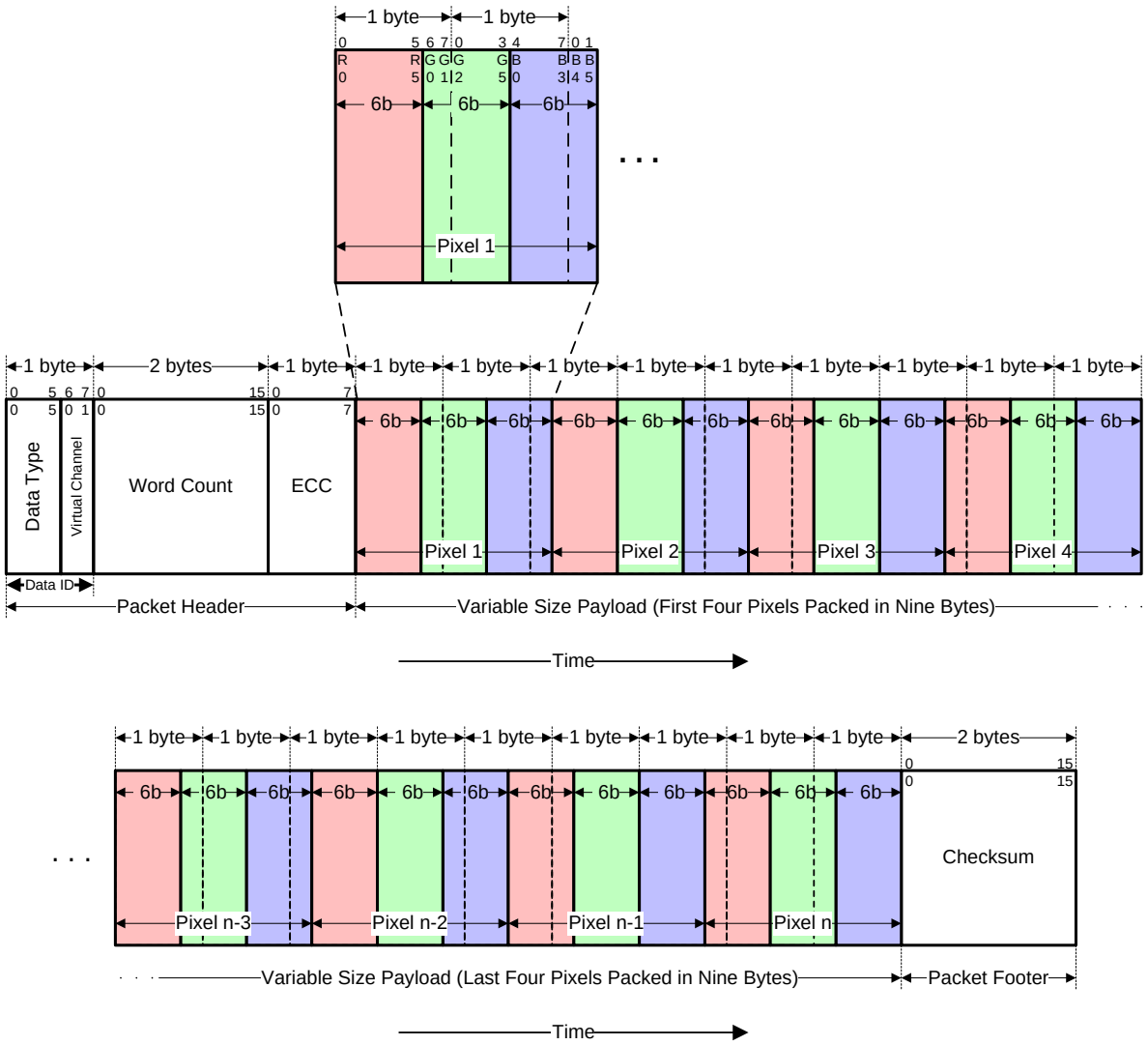


Figure 38. Packed Pixel Stream, 18-bit RGB, 6-6-6 Format

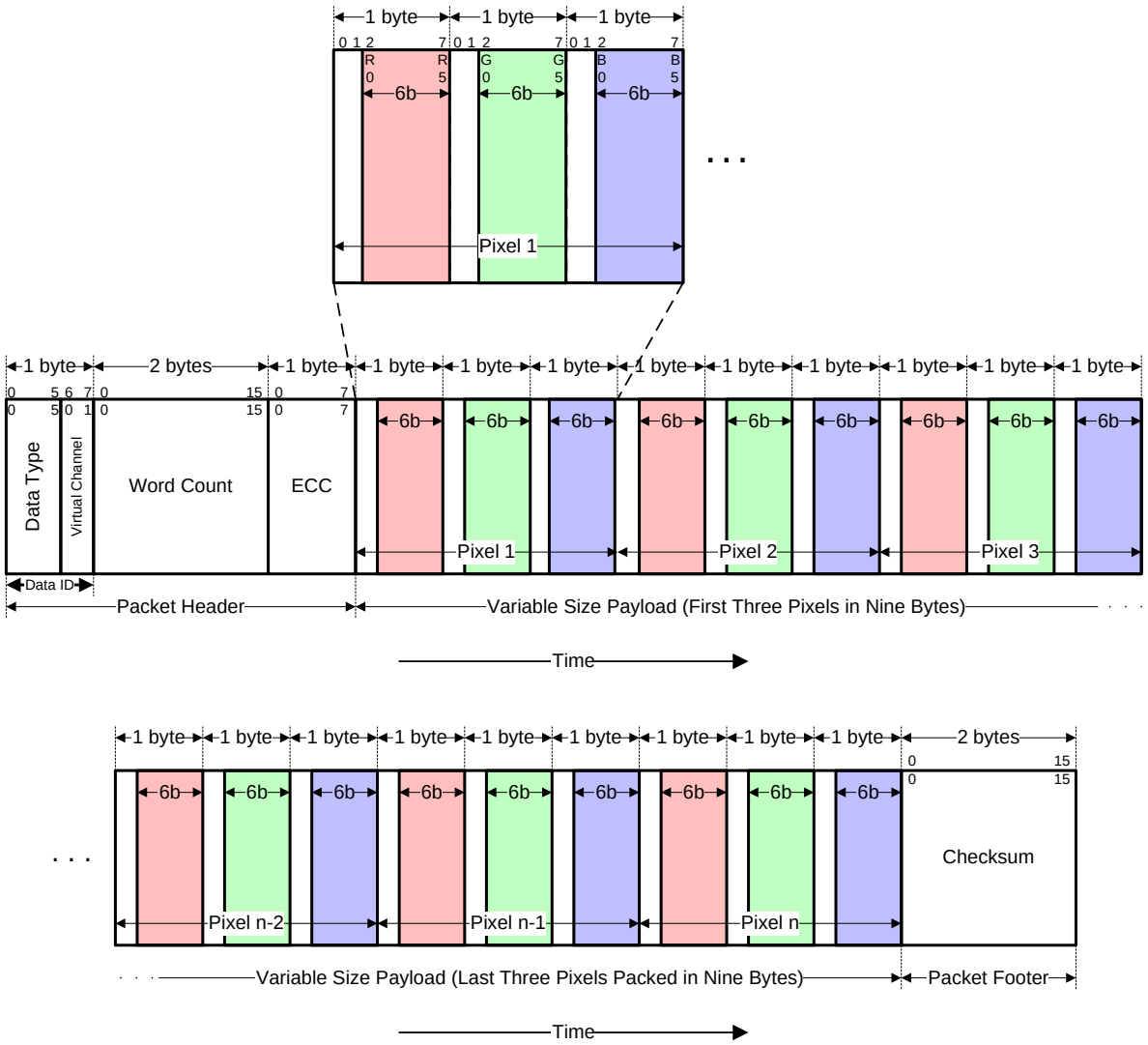


Figure 39. Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format

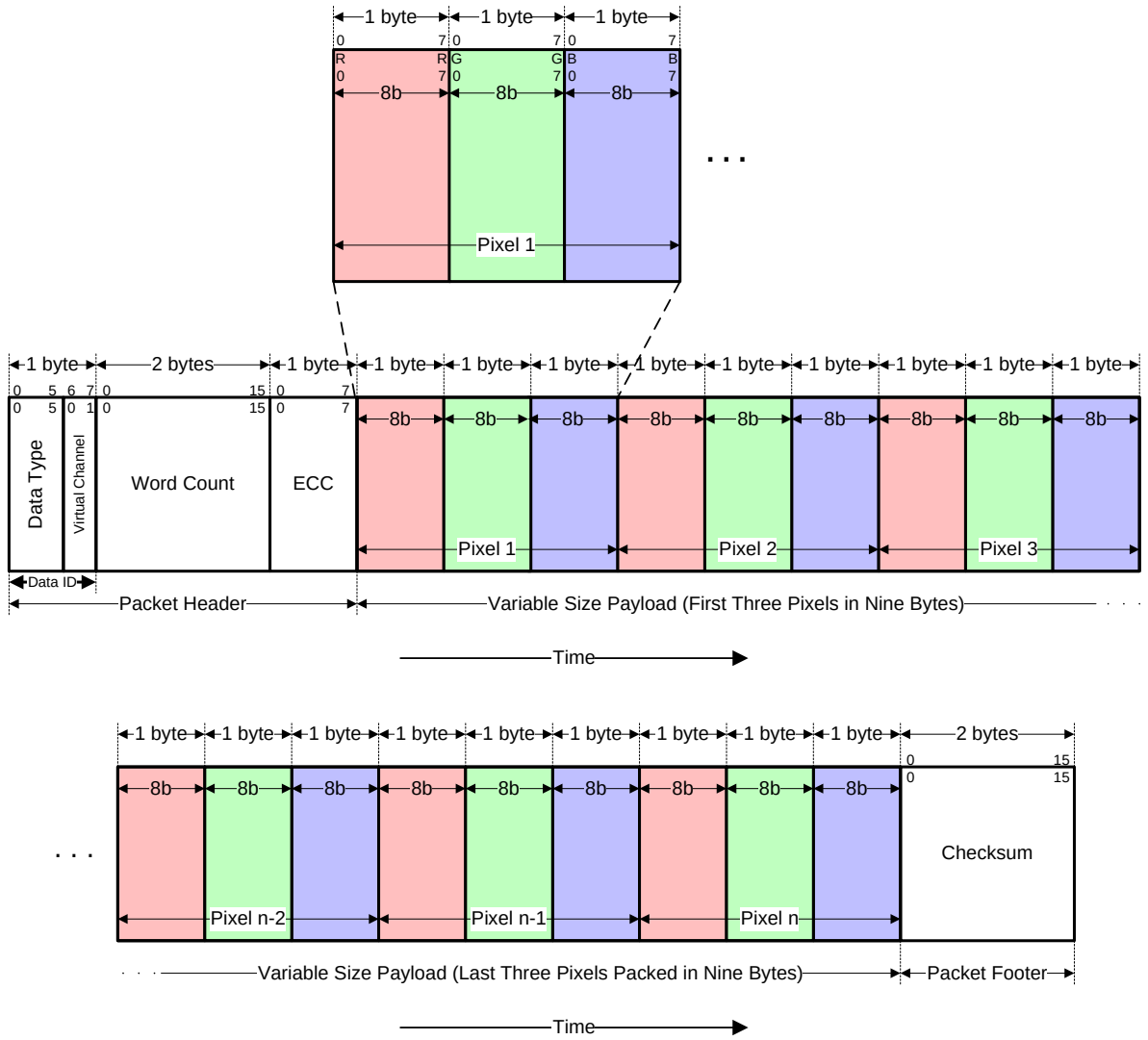


Figure 40. Packed Pixel Stream, 24-bit RGB, 8-8-8 Format

Video Mode Interface Timing

DSI supports several formats, or packet sequences, for Video Mode data transmission. The peripheral's timing requirements dictate which format is appropriate. In the following sections, Burst Mode refers to time-compression of the RGB pixel (active video) portion of the transmission. In addition, these terms are used throughout the following sections:

- Non-Burst Mode with Sync Pulses – enables the peripheral to accurately reconstruct original video timing, including sync pulse widths.
- Non-Burst Mode with Sync Events – similar to above, but accurate reconstruction of sync pulse widths is not required, so a single Sync Event is substituted.
- Burst mode – RGB pixel packets are time-compressed, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link.

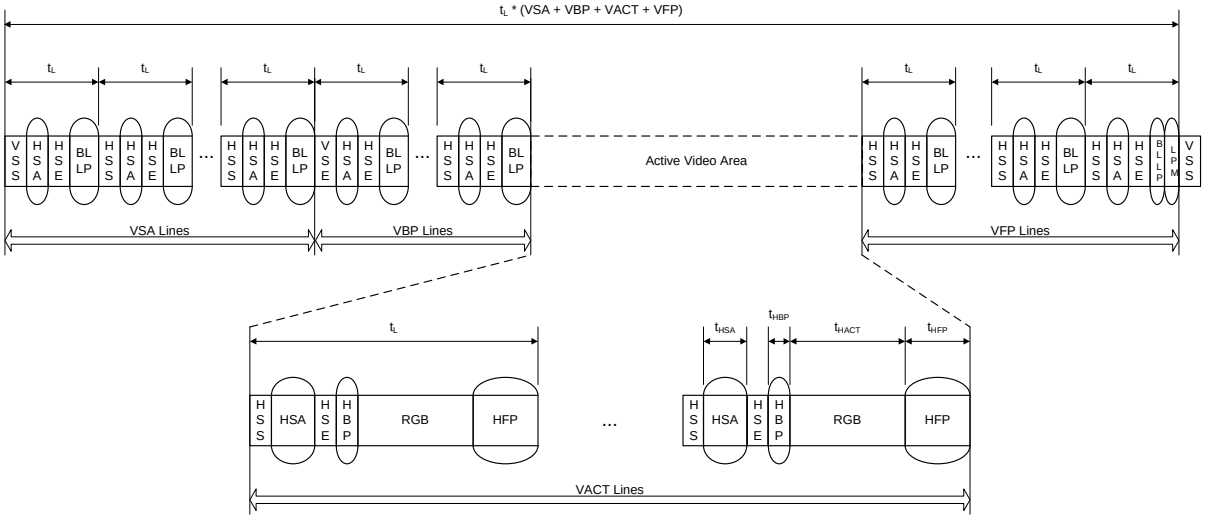


Figure 41. Non-Burst Mode with Sync Pulses

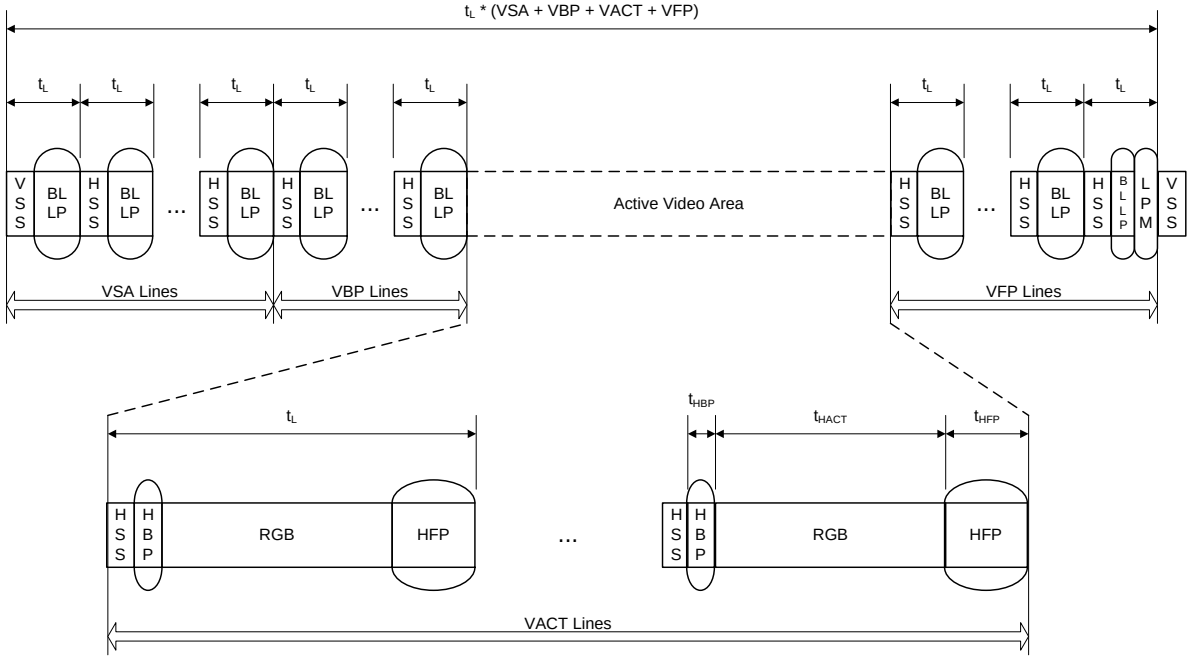


Figure 42. Non-Burst Mode with Sync Events

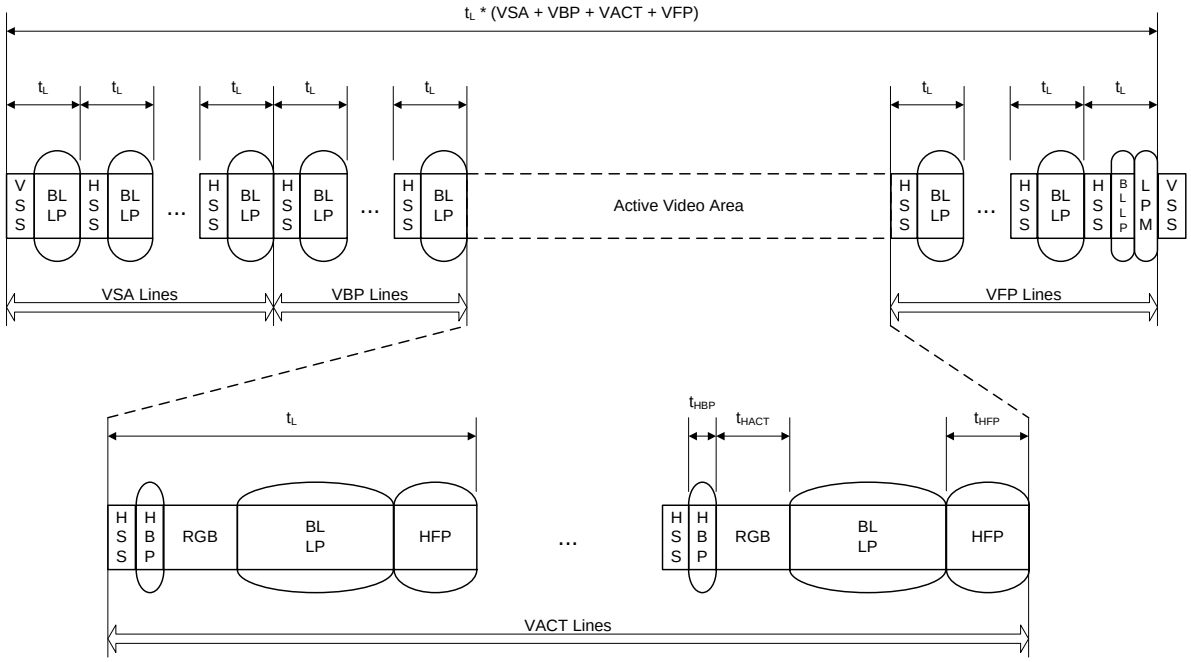


Figure 43. Burst mode

5.7 MDDI

The LG4572B supports MDDI interface. The physical layer of MDDI is based on a high-speed differential signaling. Both command and image data transfer can be achieved with MDDI.
MDDI host & client are linked by Data and STB line. Through Data line, either command or image data is transferred from MDDI host to MDDI client, and vice versa. Data is transferred by packet unit.

Through STB line, strobe signal is transferred.

When the link is in 'FORWARD direction", data is transferred from host to client, in "REVERSE direction", client transfers data to MDDI host.

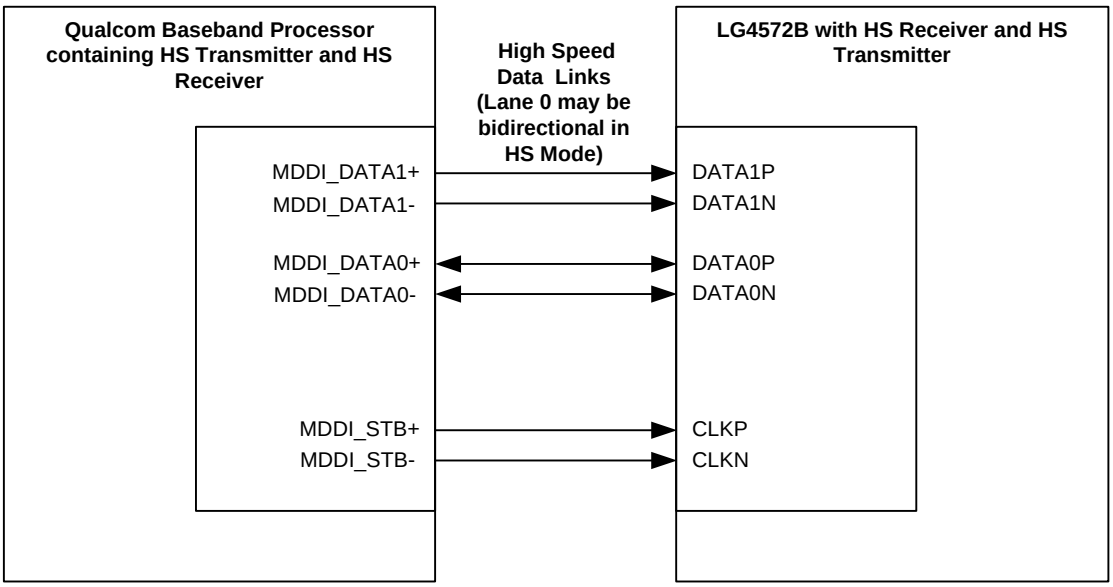


Figure 44. MDDI Transmitter and Receiver Interface

5.7.1 MDDI Data and STB

Data is encoded using DATA-STB method. Data signal is bi-direction over a pair of differential cable while STB signal in uni-directional over a pair of differential cable driven by a host as shown in the following figure, which illustrates how the data sequence "11_1000_1011" is transmitted using DATA-STB encoding.

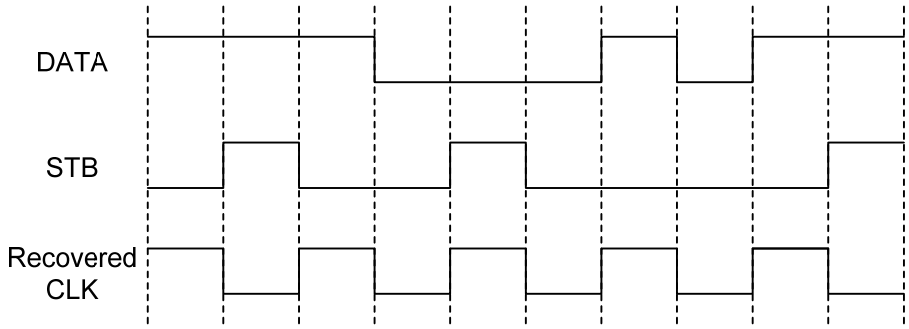


Figure 45. MDDI DATA-STB Encoding

The below figure shows a exemplary circuit to show how to generate Out DATA and Recovered Clock from host side Data and STB signals.

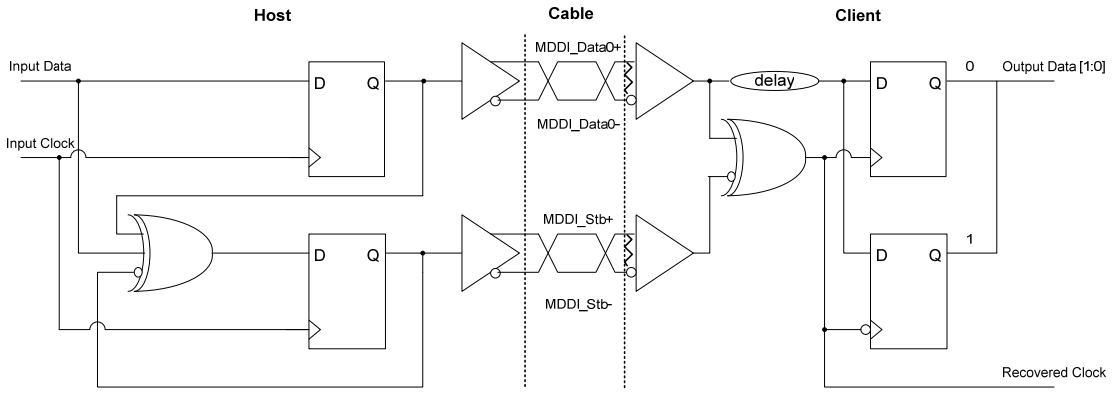


Figure 46. DATA and STB Generation & Recovery Circuits

The DATA and STB signals are always operated in a differential mode to maximize noise immunity. Each differential pair is parallel terminated with the characteristic impedance of the cable. All parallel terminations are in the client device. Figure below illustrate the configuration of the drivers, receivers, and terminations. The driver of each signal pair has a differential current output. While receiving MDDI packets, the MDDI_DATA and MDD_STB pairs use a conventional differential receiver with a differential voltage threshold of zero volts. In the hibernation state, the driver outputs are disabled and the parallel termination resistors pull the differential voltage on each signal pair to zero volts. During hibernation, a special receiver on the MDDI_DATA pairs has an offset input differential voltage threshold of positive 125mV, which cause the hibernation line receiver interpret the un-driven signal pair as logic-zero level.

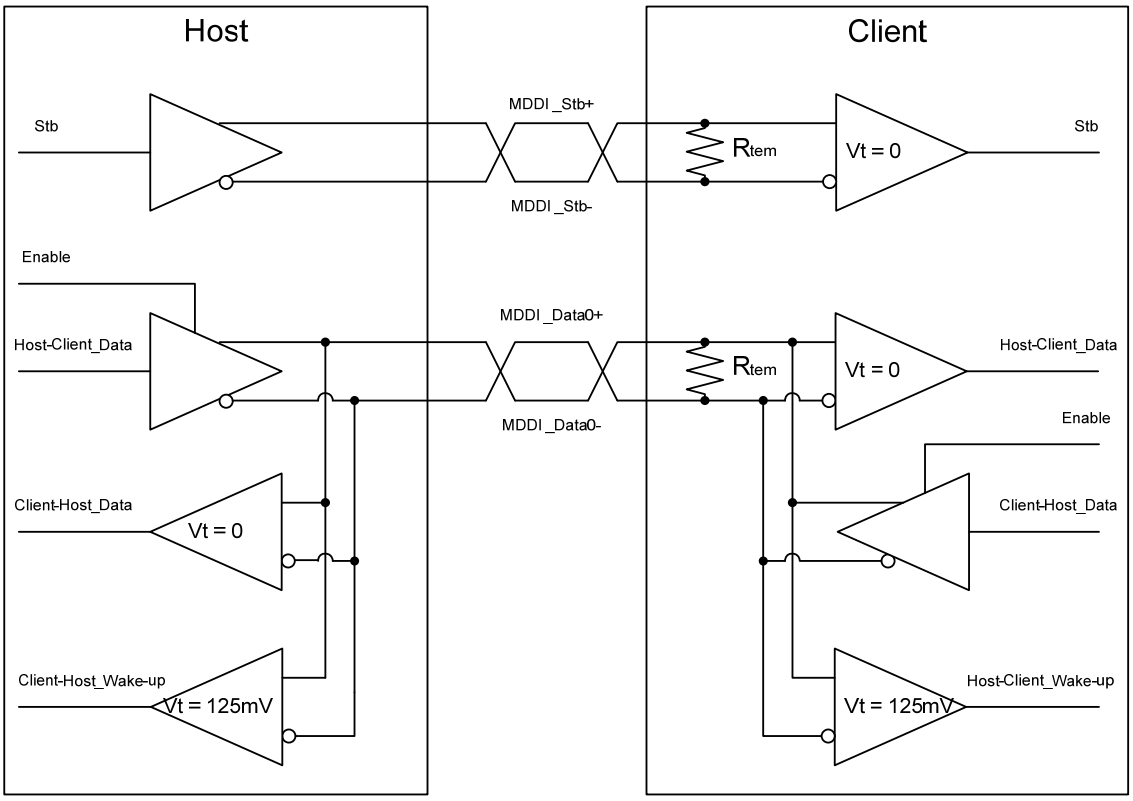


Figure 47. Differential Connection Between Host and Client

5.7.2 MDDI Packet

MDDI transfer data in a packet format. MDDT host can generate and send packets.
In LG4572B, several packet format are supported. Packets are transferred from MDDI host to client(forward direction). Burst reverse encapsulation packet is transferred from MDDI client to host(reverse direction).
A number of packets, started by sub-frame header packet, construct 1 sub frame.

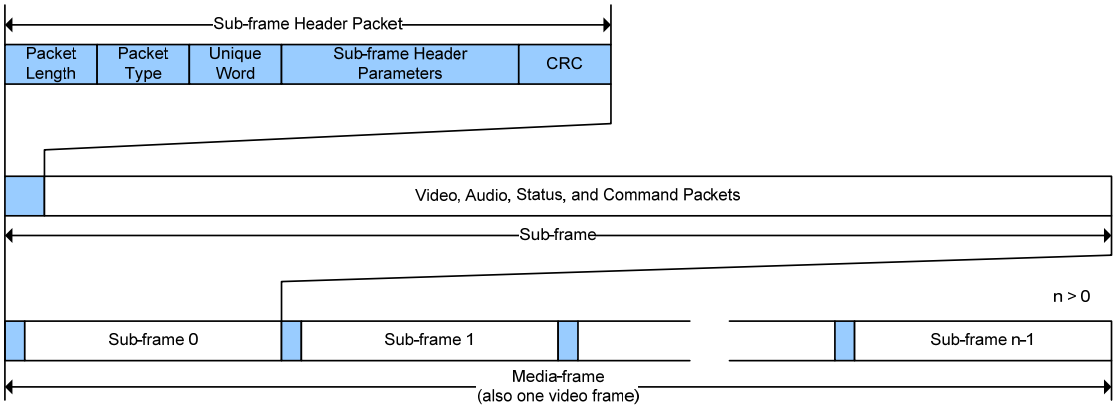


Figure 48. MDDI Packet Structure

Referring to MDDI packet structure, sub-frame header packet is placed in front of a sub-frame, and some sub-frame construct media-frame together.

Table 7. Types of packets supported by LG4572B

Packet	Function	Direction
Sub-frame header packet	Header of each sub frame	Forward
Register access packet	Register setting	Forward
Video stream packet	Video data transfer	Forward
Windowless video stream packet	Video data transfer	Forward
Filler packet	Fill empty packet space	Forward
Reverse link encapsulation packet	Reverse data packet	Reverse
Round-trip delay measurement packet	Host→ client → host delay check	Forward/Reverse
Client capability packet	Capability of client check	Reverse
Client request and status packet	Information about client status	Reverse
Link shutdown packet	End of Frame	Forward

Sub-frame Header Packet

packet length	packet type = 3bffh	unique word = 005ah	reserved 1	sub-frame length	protocol version	sub-frame count	media frame count	CRC
2 bytes	2 bytes	2 bytes	2 bytes	4 bytes	2 bytes	2 bytes	4 bytes	2 bytes

packet length : packet length not including packet length block
packet type : packet type (sub-frame header packet is 3bffh)
unique word : Identify "This packet is sub-frame header packet"
reserved 1 : not used (set zero)
protocol version : set all zero
sub-frame count : specifies number of sub-frame header packets
media frame count : specifies number of media frames
CRC : error check

Figure 49. Sub-frame Header Packet Structure

Register Access Packet

packet length	packet type = 146	bClient ID	Read / Write Info	Register Address	Parameter CRC	Register Data List	Register Data CRC
2 bytes	2 bytes	2 bytes	2 bytes	4 bytes	2 bytes	Packet Length – 14 bytes	2 bytes

packet length : packet length not including packet length block
packet type : packet type (Register Access packet is 146 (decimal))
bClinet ID : set to all zero
Read / Write Info : to write register value, bits [15:14] = "00"
to read register value, bits [15:14] = "10"
bit [13:0] refer to VESA SPEC
Register Address : Register address is written here
Parameter CRC : to check error from packet length to register address
Register Data List : A list of 4 byte register data values to be written to LDI
Register Data CRC : To error check register data list

* Basis of Register Data List is 4-byte unit. Therefore, when register parameter is not multiply of 4. Remainder bits must fill by 0.

Figure 50. Register Access Packet Structure

Video Stream Packet

packet length	packet type = 16	bClient ID	Video data format descriptor	Pixel data Attributes	X Left Edge	Y Top Edge	X Right Edge	Y Bottom Edge
2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes

X Start	Y Start	Pixel Count	Parameter CRC	Pixel Data	Pixel Data CRC
2 bytes	2 bytes	2 bytes	2 bytes	Packet Length – 26 bytes	2 bytes

packet length : packet length not including packet length block
packet type : packet type (video stream packet is 16 (decimal))
bClinet ID : set to all zero
Video Data format descriptor bits [15:13] = 010 : raw RGB format (fixed value)
bit[12] = 1 : Only packed type is available (fixed value)
bits[11:0] = 1000_1000_1000 : 24 bit pixel
~~bits[11:0] = 0110_0110_0110 : 18 bit pixel~~
bits[11:0] = 0101_0110_0101 : 16 bit pixel
Pixel data attributes bits[1:0] = 11 : displayed both eyes (fixed value)
bits[5] = 1 : X left edge, Y Start edge is not defined (fixed value)
other bits are all zero
X left edge : X coordinate of the left edge of the screen window filled by the Pixel Date field.
Y top edge : Y coordinate of the top edge of the screen window filled by the Pixel Date field.
X right edge : X coordinate of the right edge of the window being updated.
Y bottom edge : Y coordinate of the bottom edge of the window being updated.
X start : X start Pixel address.
Y start : Y start Pixel address.
Pixel count : Write number of pixel
Parameter CRC : to check error from packet length to pixel count
Pixel data : pixel data info. Number of pixel data must not be over 65509
Pixel Data CRC : To error check pixel data

Figure 51. Video Stream Packet Structure

Filler Packet

packet length	packet type = 0	Filler bytes (all zero)	CRC
2 bytes	2 bytes	Packet Length – 14 bytes	2 bytes

packet length : packet length not including packet length block
packet type : packet type (Filler packet is 0 (decimal))
Filler bytes : set to all zero (The size is under packet length available)
CRC : to error check

Figure 52. Filler Packet Structure

Link Shutdown Packet

packet length	packet type = 69	CRC	All zeros
2 bytes	2 bytes	2 bytes	16 bytes

packet length : packet length not including packet length block
packet type : packet type (Link shutdown packet is 69 (decimal))
CRC : to error check
All zeros : write all zero (size is 16 bytes)

Figure 53. Link Shutdown Packet Structure

5.7.3 Write and Read Sequences with MDDI Packet

LG4572B supports video stream packet for memory write and register access packet for register write/read. Followings are the examples of memory and register write/read sequences.

Write Video Data

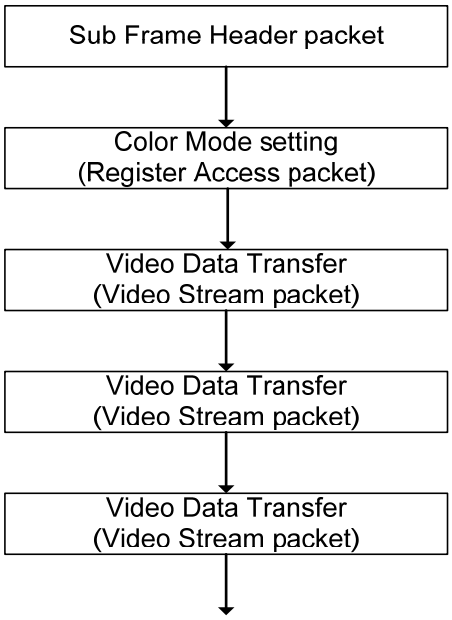
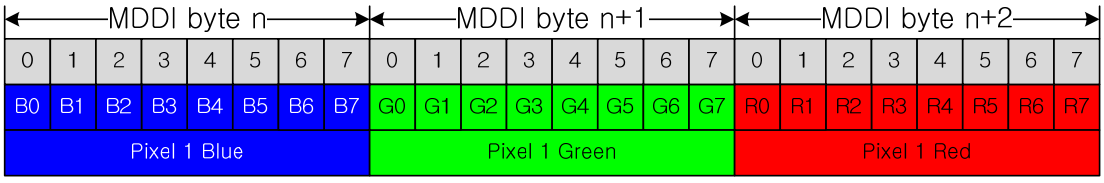


Figure 54. Video Data Write Sequence

Table 8. Color Mode setting in MDDI

Video data format descriptor[11:0]	**Color Mode**
1000_1000_1000	24 bits/ pixel
~~0110_0110_0110~~	~~18 bits/ pixel~~
0101_0110_0101	16 bits/ pixel



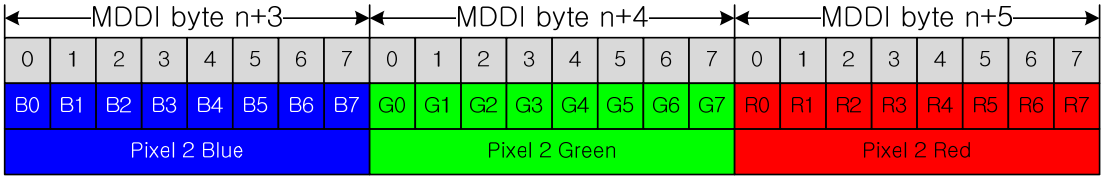
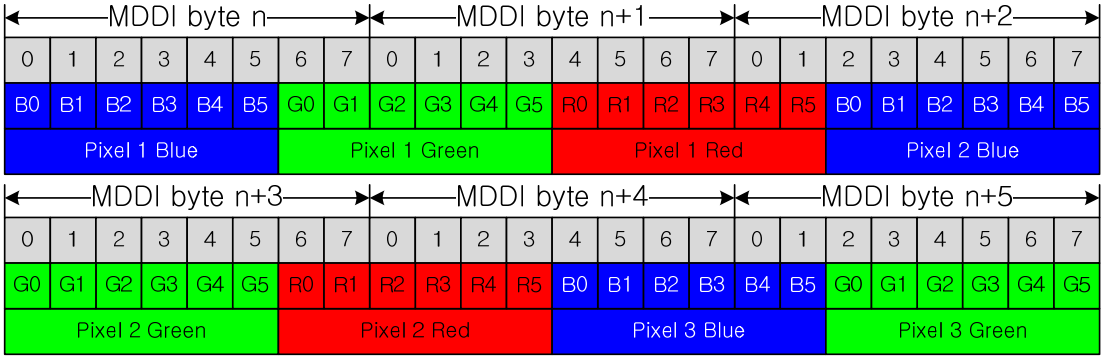


Figure 55. 24bits/pixel(B:8, G:8, R:8) data transfer format



~~*Figure 56. 18bits/pixel(B:6, G:6, R:6)) data transfer format*~~

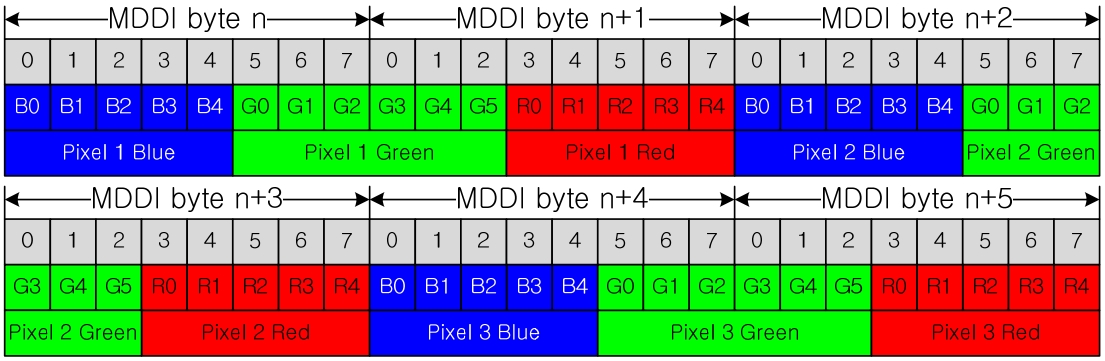


Figure 57. 16bits/pixel(B:5, G:6, R:5)) data transfer format

Write Register

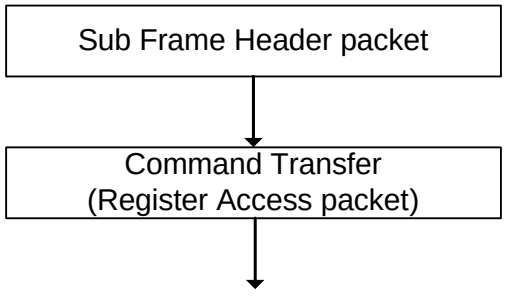


Figure 58. Writing register sequence

Read Video Data from Memory

In order to read a pixel data from memory(readable one pixel only), the following sequence should be programmed. Memory read command (2EH) is followed by reverse encapsulation packet. DDI transmits video pixel data through encapsulation packet. Please refer to VESA spec for detailed description.

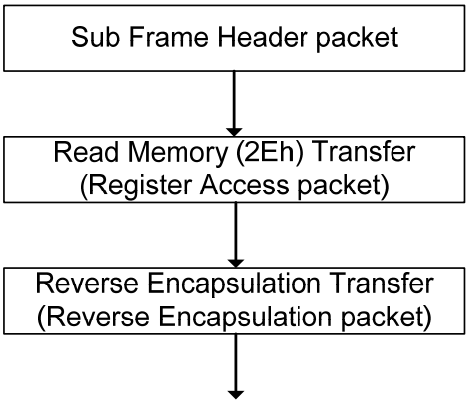


Figure 59. Read Video Data from Memory

Read Register Values

In order to read registers, the following sequence should be programmed. Register read command is followed by reverse encapsulation packet. DDI transmits register data through encapsulation packet. Please refer to VESA spec for detailed description.

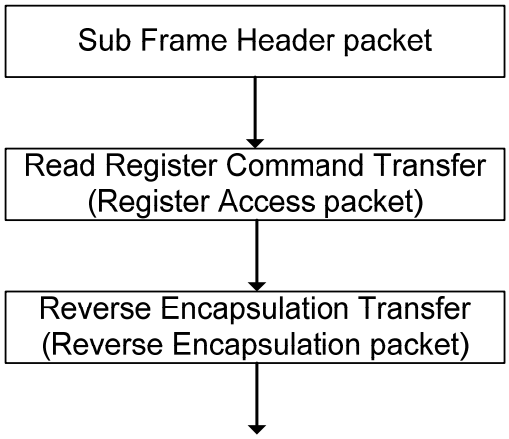


Figure 60. Read Register

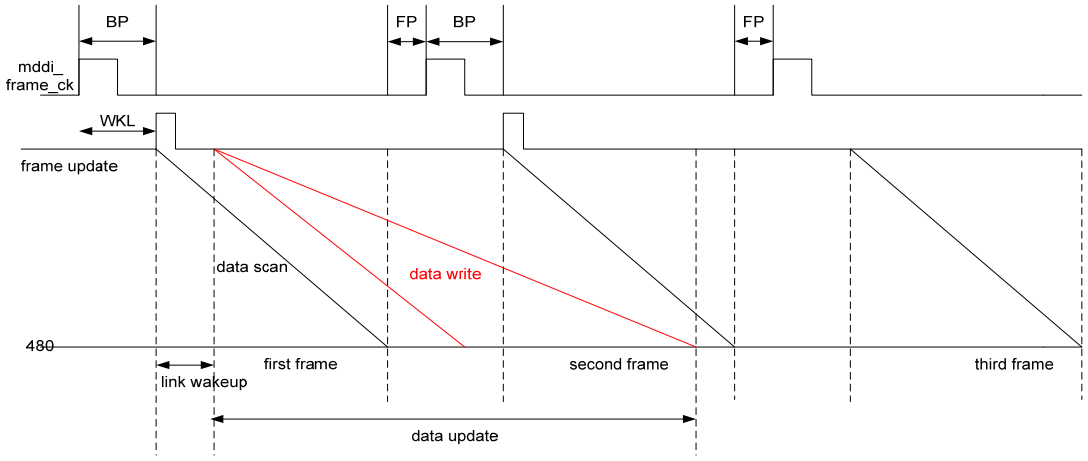
Note : Only Level 1 Registers are readable in MDDI.
Note : Not only level 1 register (ex. D5h)

5.7.4 Tearing-less Display

In LG4572B, the matching between data writes timing and written data display timing is important. If timing is mismatched, tearing effect can occur.

To avoid display tearing effect, two possible ways are suggested.

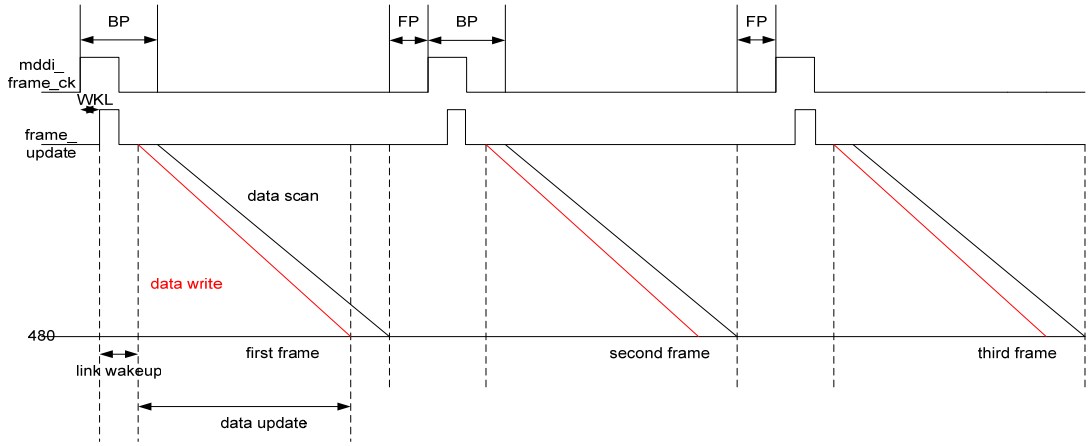
First case is that data write is slower than the speed of displaying written data as shown in the following figure. For this case, data write speed is not critical, but current consumption in interface will be increased because data transfer time is long. Data write time is selected widely in this case.



WKL is to set later than data scan and consider that data write is to be completed before next data scan is completed.

Figure 61. Tearing-less Display : Display speed is faster than data write speed.

Other case is that data write is faster than the speed of displaying written data as shown in the following figure. For this case, data update speed is very high so that transfer time is to avoid data scan conflicts with data update.



WKL is to set previously than data scan and consider the time that reverse time from client to host to send request signal.

Figure 62. Tearing-less Display : Display speed is slower than data write speed.

5.7.5 Hibernation and Wakeup

The LG4572B supports hibernation mode to save interface power consumption. MDDI link can enter the hibernation state quickly and wake up from hibernation quickly. This allows the system to force MDDI link into hibernation frequently to save power consumption.

During hibernation mode, the hi-speed transmitters and receivers are disabled and low-speed & low-power receivers are enabled in order detect wake-up sequence.

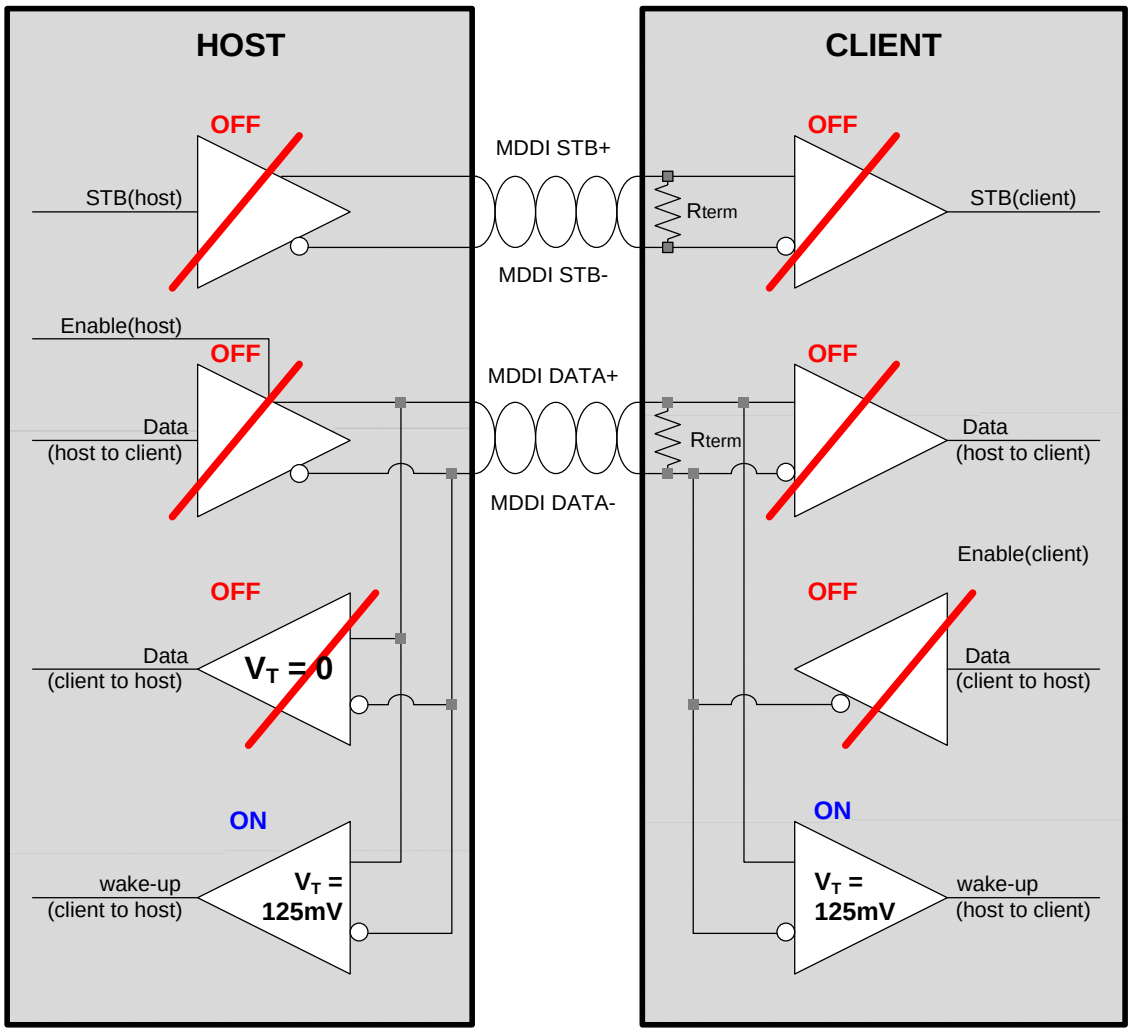


Figure 63. MDDI Transceiver and Receiver's states in Hibernation

When the link wakes up from hibernation, the host and client exchange a sequence of pulses. These pulses can be detected using low-speed, low-power receivers that consume only a fraction of the current of the differential receivers required to receive the signals at the maximum link operating speed.

Either the client or the host can wake up the link; Host-initiated link wakeup.

Host-initiated Link Wake-up Procedure

The simple case of host-initiated wake-up is described below without contention from the client trying to wake up at the same time. The following sequence of events is illustrated in the following figure.

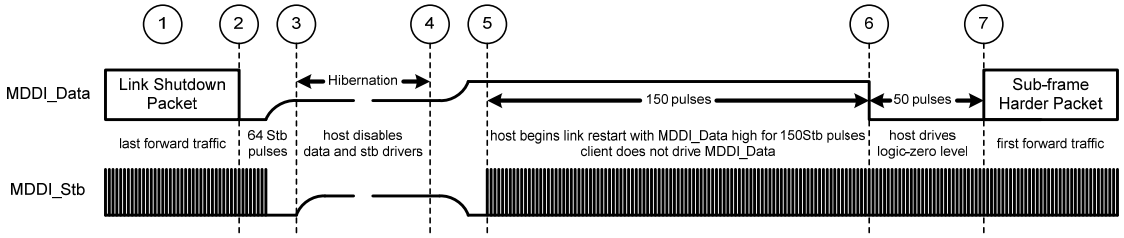


Figure 64. Host-initiated Link Wake-up Sequence

1. The host sends a Link Shutdown Packet to inform the client that the link will transition to the low-

power hibernation state.

2. Following the CRC of the Link Shutdown Packet the host toggle MDDI_STB for 64 cycles to allow processing in the client to finish before it stops MDDI_STB from toggling which stops the recovered clock in the client device. Also during this interval the host initially sets MDDI_DATA to a logic_zero level, and then disables the MDDI_DATA output in the range of 16 to 48 MDDI_STB cycles(including output disable propagation delays) after the CRC.
   It may be desirable for the client to place its high-speed receivers for MDDI_DATA and MDDI_STB into a low power state any time after 48 MDDI_STB cycles after the CRC and before point 3.

3. The host enters the low-power hibernation state by disabling the MDDI_DATA and MDDI_STB drivers and by placing the host controller into a low-power hibernation state.
   It is also allowable for MDDI_STB to be driven to logic_zero level or to continue toggling during hibernation.
   The client is also in the low-power hibernation state.

4. After a while, the host begins the link restart sequence by enabling the MDDI_DATA and MDDI_STB driver outputs.
   The host drives MDDI_DATA to a logic-one level and MDDI_STB to logic-zero level for at least the time it takes for the drivers to fully enable their outputs. The host shall wait at least 200 nsec after MDDI_DATA reaches a valid logic-one level and MDDI_STB reaches a valid logic-zero level before driving pulses on MDDI_STB. This gives the client sufficient time to prepare to receive high-speed pulses on MDDI_STB. The client first detects the wake-up pulse using a low-power differential receiver having a +125mV input offset voltage.

5. The host drivers are fully enabled and MDDI_DATA is being driven to a logic-one level. The host begins to toggle MDDI_STB in a manner consistent with having logic-zero level on MDDI_DATA for duration of 150 MDDI_STB cycles.

6. The host drives MDDI_DATA to logic-zero level for 50 MDDI_STB cycles. The client begins to look for the Sub-frame header Packet after MDDI_DATA is at logic-zero level for 40 MDDI_STB cycles.

7. The host begins to transmit data on the forward link by sending a Sub-frame Header Packet. Beginning at point 7. The MDDI host generates MDDI_STB based on the logic level on MDDI_DATA so that proper data-strobe encoding commences from point 7.

VSYNC Based Host-initiated Link Wake-up Procedure

In display-ON state, when the IC finishes displaying all internal GRAM data, data request must be transferred to MDDI host for new video data. As MDDI link is usually in hibernation for reducing interface power consumption, MDDI link wake-up must be done before internal GRAM update. In that case, client initiated link wake-up can be used as data request.

When VSYNC based link wake-up register(E0h: VWAKE_EN) is set, client initiated wake-up is executed in synchronization with the vertical-sync signal which generated in LG4572B. Using VSYNC based link wake-up, tearingless display can be accomplished if interface speed and wake-up time is well known.

The following figure shows detailed timing for VSYNC based link wake-up.

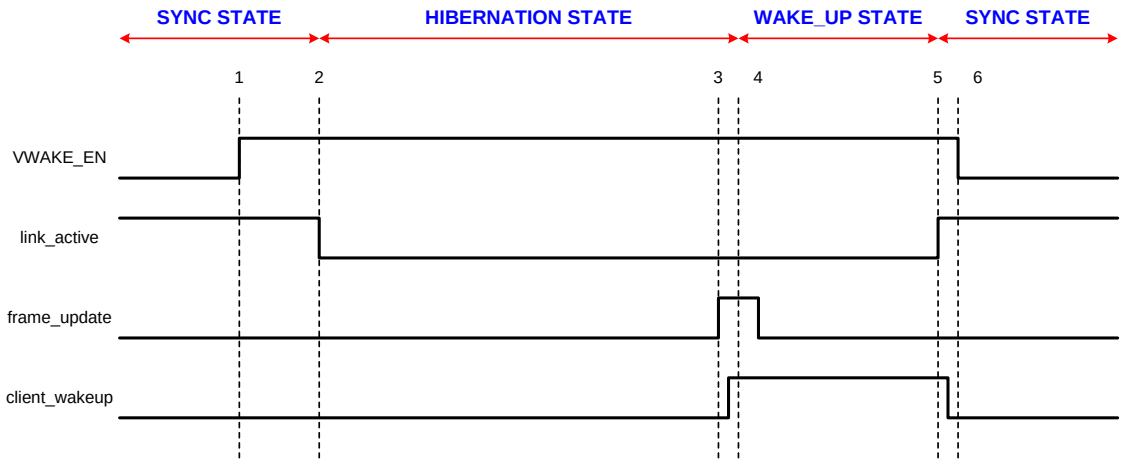


Figure 65. VSYNC Based Host-initiated Link Wake-up Sequence

The detailed description for labeled events as follows:

1. MDDI host writes to the VSYNC based link wakeup register to enable a wake-up based on internal vertical-sync signal.

2. Link_active goes low when the host puts in the link into hibernation after no more data needs to be sent to the LG4572B.

3. Frame_update, the internal vertical-sync signal goes high indicating that update pointer has wrapped around and is now reading from the beginning of the frame buffer. Link wake-up can be set using WKF and WKL(E1h) registers. WKF specifies the number of frame before wake-up; WKL specifies the number of lines before wake-up

4. Client_wakeup input to the MDDI client goes high to start the client initiated link wake-up.

5. Link_active goes high after the host brings the link out of hibernation.

6. After link wake-up, client_wakeup signal and the VWAKE_EN register are cleared automatically.

Client-initiated Link Wake-up Procedure

An example of a typical client-initiated service request event with no contention is illustrated in the following figure.

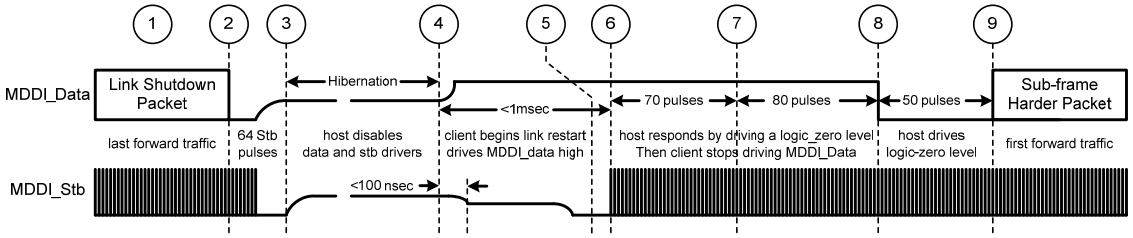


Figure 66. Client-initiated Link Wake-up Sequence

The Detailed description for labeled events are as follows;

1. The host sends a Link Shutdown Packet to inform the client that the link will transition to the low-power hibernation state.
2. Following the CRC of the Link Shutdown Packet the host toggles MDDI_STB for 64 cycles to allow processing in the client to finish before it stops MDDI_STB from toggling which stops the recovered

clock in the client device. Also during this interval the host initially sets MDDI_DATA to a logic_zero level, and then disables the MDDI_DATA output in the range of 16 to 48 MDDI_STB cycles(including output disable propagation delays) after the CRC. It may be desirable for the client to place its high-speed receivers for MDDI_DATA and MDDI_STB into a low power state any time after 48 MDDI_STB cycles after the CRC and before point 3.

3. The host enters the low-power hibernation state by disabling the MDDI_DATA and MDDI_STB drivers and by placing the host controller into a low-powre hibernation state.
   It is also allowable for MDDI_STB to be driven to logic_zero level or to continue toggling during hibernation. The client is also in the low-power hibernation state.

4. After a while, the client begins the link restart sequence by enabling the MDDI_STB receiver and also enabling an offset in its MDDI_STB receiver to guarantee the state of the received version of MDDI_STB is a logical-zero level in the client before the host enables its MDDI_STB driver. The client will need to enable the offset in MDDI_STB immediately before enabling its MDDI_STB receiver to ensure that MDDI_STB receiver in the client is always receiving a valid differential signal and to prevent erroneous received signals from propagation into the client. After that, the client enables its MDDI_DATA driver while driving MDDI_DATA to a logic-one level. It is allowed for MDDI_DATA and MDDI_STB to be enabled simultaneously if the time to enable the offset and enable the standard MDDI_STB differential receiver is less than 200 nsec.

5. Within 1 msec the host recognizes the service request pulse, and the host begins the link restart sequence by enabling the MDDI_DATA and MDDI_STB driver output. The host drivers MDDI_DATA to a logic-one level and MDDI_STB to a logic-zero level for at least the time it takes for the drivers to fully enable their outputs. The host shall wait at least 200 nsec after MDDI_DATA reaches a valid logic-one level and MDDI_STB reaches a valid fully-driven logic-zero level before diving pulses on MDDI_TSB. This gives the client sufficient time to prepare to receive high-speed pulses on MDDI_STB.

6. The host begins outputting pulses on MDDI_STB and shall keep MDDI_DATA at a logic-one level for a total duration of 150 MDDI_STB pulses through point 8. The host generates MDDI_STB in a manner consistent with sending a logical-zero level on MDDI_DATA. When the client recognizes the first pulse on MDDI_STB it shall disable the offset in its MDDI_STB receiver.

7. The client continues to drive MDDI_DATA to a logic-one level for 70 MDDI_STB pulses, and the client disables its MDDI_DATA driver at point 7. The host continues to drive MDDI_DATA to a logic-one level for duration of 80 additional MDDI_STB pulses, and at point 8 drivers MDDI_DATA to logic-zero level.

8. The host drivers MDDI_DATA to logic-zero level for 50 MDDI_STB cycles. The client begins to look for the Sub-frame header Packet after MDDI_DATA is at logic-zero level for 40 MDDI_STB cycles.

9. After asserting MDDI_DATA to logic-zero level and driving MDDI_STB for duration of 50 MDDI_STB pulses the host begins to transmit data on the forward link at point 9 by sending a Sub-frame Header Packet. The client begins to look for the Sub-frame Header Packet after MDDI_DATA is at logic-zero level for 40 MDDI_STB cycles.

5.7.6 MDDI Operation Modes

In MDDI, 6 operation modes are available. The following table describes 6 modes.

Table 9. Color Mode setting in MDDI

STATE	Oscillator	Step-up	Internal Logic Status	MDDI IO	Wake-up by
INIT_HIBER	OFF	Disable	Display OFF Internal Logic ON MDDI Link Hibernation	Hibernation driver ON	Host-initiated
WAIT	OFF	Disable	Display OFF Internal Logic ON MDDI Link SYNC	Standard driver ON	-
NORMAL	ON	Enable	Display ON Internal Logic ON MDDI Link SYNC	Standard driver ON	-
HIBER	ON	Enable	Display ON Internal Logic ON MDDI Link Hibernation	Hibernation driver ON	Host-initiated Client-initiated (VSYNC)
SLEEP	OFF	Disable	Display OFF Internal Logic ON MDDI Link SYNC	Standard driver ON	-
STOP	OFF	Disable	Display OFF Internal Logic ON MDDI Link OFF	Driver All OFF	RESET

INIT_HIBER : Initial status when external power is connected to the IC. In this state, internal oscillator is OFF, and MDDI link is hibernation state. As no command or signal is applied to the IC except RESET input and booster circuit is OFF, and internal logic is ON.

WAIT : After the wake-up sequence, the IC is in WAIT state. MDDI link is in SYNC, and internal logic is ON, and booster is still OFF because no other register access or video stream packet is transferred to the IC.

NORMAL: MDDI link, booster circuit, and internal logic circuit are ON. Register access or Video data transfer is available in NORMAL state.

HIBER: When no more video data update is needed, MDDI link is in hibernation so that interface power can be reduced. Internal booster & logic circuits are still operating. MDDI link wakeup will be accomplished when VSYNC wakeup register is set before hibernation.

SLEEP: This state is set by register access. Booster is OFF, but MDDI link and internal logic have to be in SYNC because the IC must receive commands for power save or normal operation.

STOP: STOP state is set by MDDI_SLP register access(E0h). In this state, MDDI link, internal oscillator, Booster are all OFF and internal logic is still ON. To release STOP state, input reset signal. After reset, status is INIT_HIBER state.

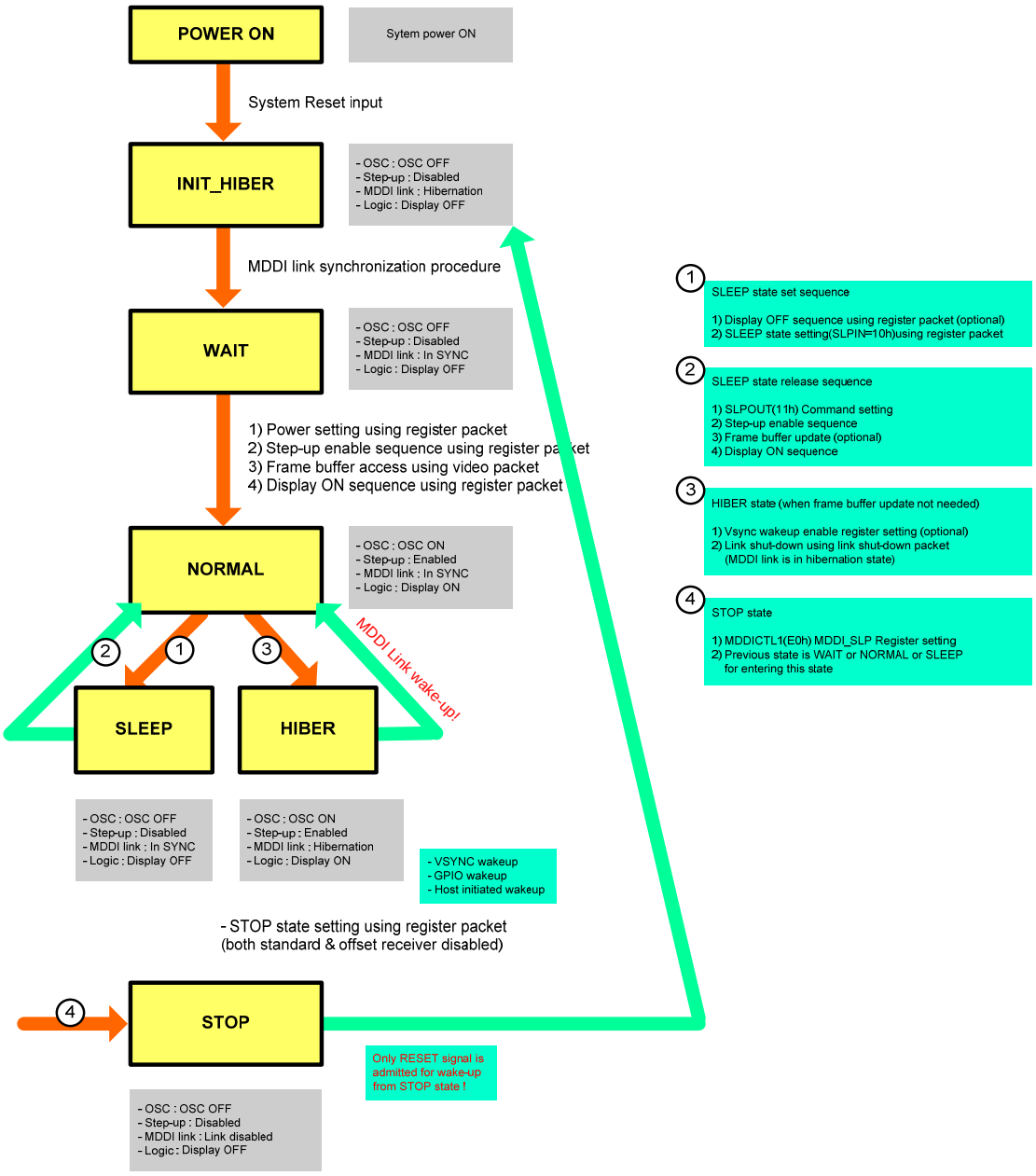


Figure 67. Operating state in MDDI modes

5.8 Backlight Control Function

5.8.1 CABC (Content Adaptive Brightness Control)

The LG4572B supports "Content Adaptive Brightness Control" function which can be used to reduce the power consumption of the luminance source. Content adaptation means that content gray scale can be increased while simultaneously lowering brightness of the backlight to achieve same perceived brightness. The adjusted gray scale and thus the power consumption reduced depend on the content of the image.

The following figure shows that how the CABC algorithm works. The CABC block accumulates the gray scales for each pixels of the image and thus CABC block comes to know the histograms about the gray scales of the image. Next, CABC block modify the original image data to have more widely spread shape while it makes the back light luminance lower so that the image luminance perceived by human becomes almost the same.

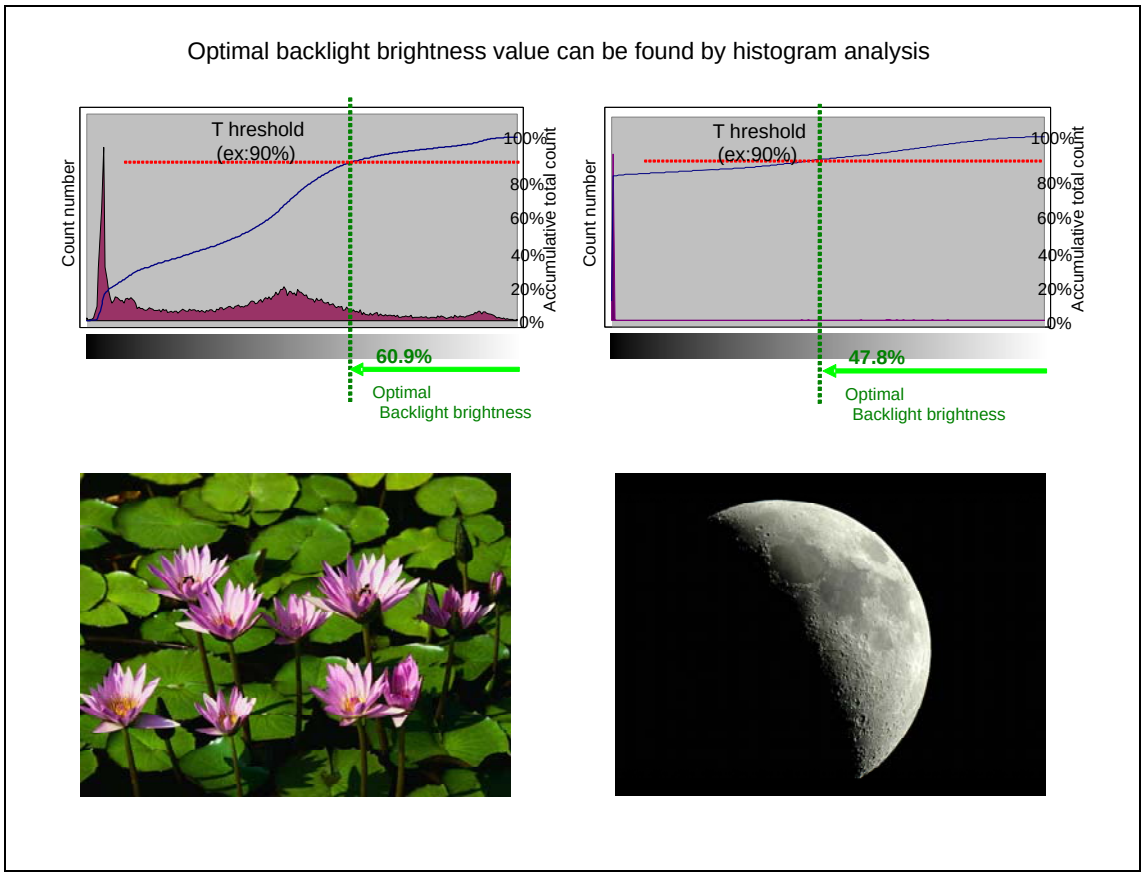


Figure 68. Content Adaptive Brightness Control

5.8.2 Brightness Control Block and CABC Block

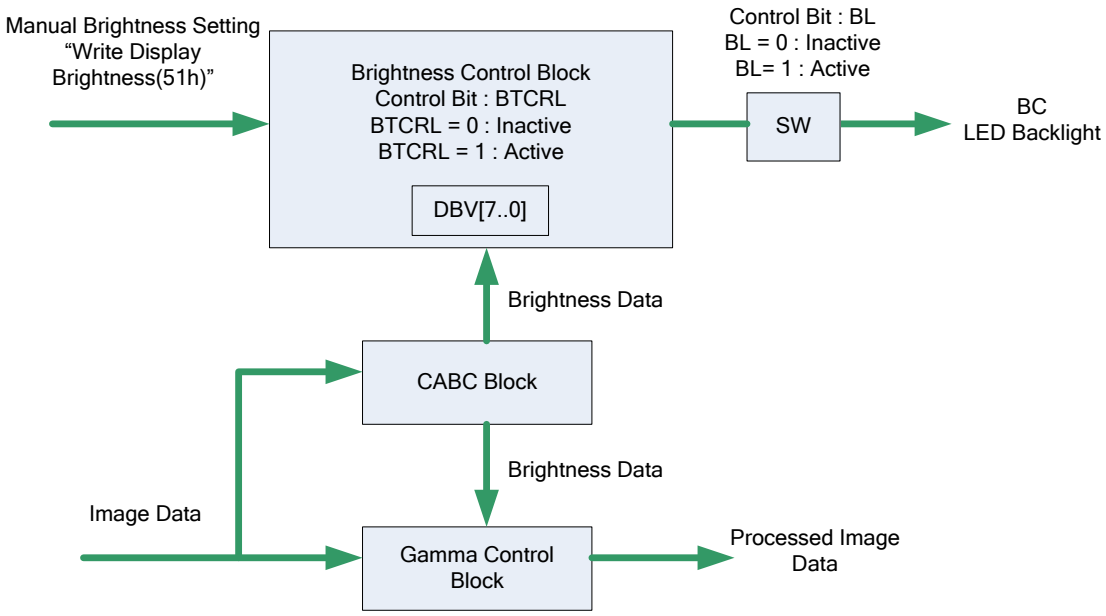


Figure 69. Block Diagram for Brightness Control Block and CABC Block

Brightness control block is used to control the display brightness as follows:

There is a resister, DBV: 8 bit, for display brightness of manual brightness setting and CABC in the display module. There is a PWM output signal, BC line, to control the LED driver IC in order to control display brightness. The brightness control method should be taken into account to avoid abnormal visible effect related with scanning frame frequency.

The brightness control block can be used in manual brightness mode and CABC mode, see "Write CTRL Display (53h)" and "Write Content Adaptive Brightness Control (55h)".

The user can adjust brightness, see "Write Display Brightness (51h)" for the display.

	WRCABC(55h)	Function	RDCABCMB(5Fh)	Image
CABC Off	00b	Disable	WRCABCMB(5Eh)	Original
CABC On	01b /10b /11b	Enable	WRCABCMB(5Eh)	CABC modified

Brightness level calculates with the following formula.

Display Output Brightness = Manual brightness setting * CABC brightness ratio

Below drawing is for the explanation of the CABC minimum brightness setting.

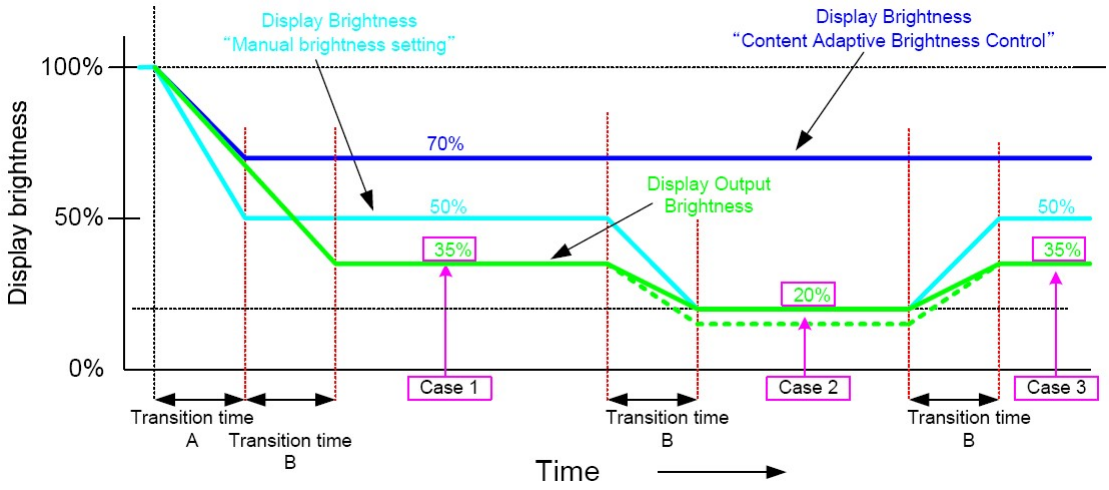


Figure 70. Controlled Display Brightness by LABC and CABC Algorithm

CABC minimum brightness value = 51 (33h: 20% display brightness)

	Display Brightness [manual setting]	Brightness Ratio[CABC]	Calculation result of the display brightness formula	Display Output Brightness	Image
Case 1	50%	70%	35%	35%	CABC modified
Case 2	20%	70%	14%	20%	CABC modified
Case 3	50%	70%	35%	35%	CABC modified

At the case 2, the calculation result of the display brightness is 14%. CABC minimum brightness value is set to 20% brightness. Actual display brightness is 20% as the CABC minimum brightness setting.

To get more easy understandings and control of this CABC function, the below conceptual control flow diagram would be a help. In the following diagram, the DD, BCTRL, and BL are control parameter in 53h register. They control the CABC paths. If DD=0, then CABC function is disabled and the manual brightness setting by DBV[7:0] in 51h register is available. If DD=1, CABC function will start to work with the maximum and minimum brightness settings respectively by DBV[7:0] and CMB[7:0] in 5Eh register. If BCTRL=1, the CABC function will go through to next path. But if BCTRL=0, GND level for BLU_PWM would be forced. If BL=1, the CABC function will go though with BCTRL=1 and controls the duties of PWM (Pulse Width Modulated) waveforms through BLU_PWM pad. Finally, the PWMP parameter in C8h register can change the polarity of BLU_PWM output. If PWMP=0, BLU_PWM waveform works as active high but if 1, then the BLU_PWM waveform works as active low.

The not-shown parameter in the following diagram to control CABC function are CDSP[3:0], CDMP[3:0], and FPWM[1:0] in C8h register, where CDSP and CDMP parameter control the dimming levels of still images and moving images, respectively. If CDSP=8, then the duties of BLU_PWM are increased or decreased by 8 levels per frame, whose total levels of this is 255, after comparing the differences between predetermined threshold value and the calculated histogram value for still images. And if CDMP=4, then the duties of BLU_PWM are increased or decreased by 4 levels per frame, whose total levels of this is 255, after comparing the differences between predetermined threshold value and the calculated histogram value for moving images. The last parameter FPWM controls the frequencies of BLU_PWM output. The setting 0 means 2 times of frame frequency, 1 means 4 times, 2 means 8

times, and 3 means 16 times of frame frequency. It goes faster according to the increased FPWM values. The tables for them are shown in C8h register description section.

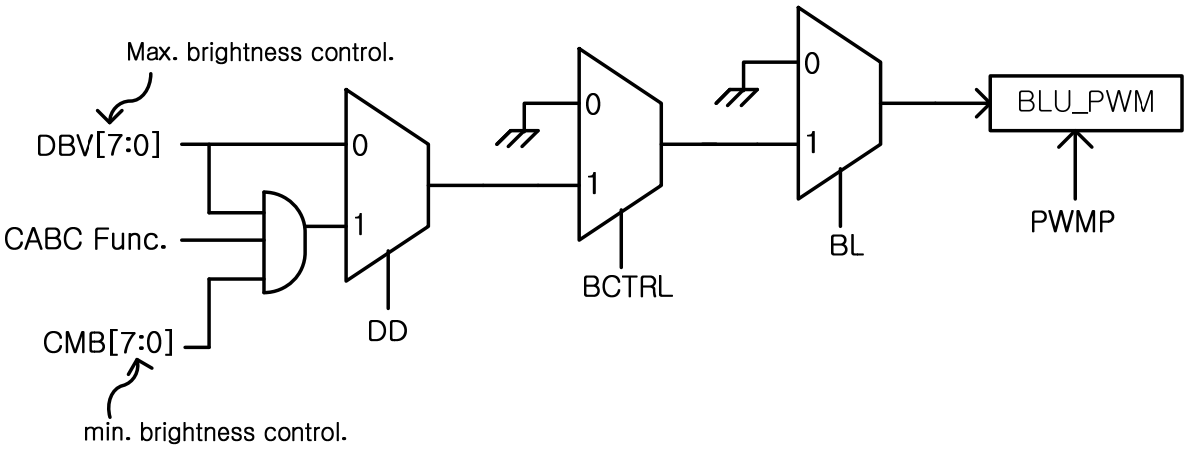


Figure 71. Conceptual control flow diagram of CABC function.

5.9 LCD Power Supply Circuit

The LCD power supply circuit generates the voltage levels of DDVDH, DDVDL, VCL, VREG1OUT, VREG2OUT, VGH, VGL, LVGL and VCOM for driving an LCD.

The internal logic power supply regulator generates internal logic power supply VDD.

5.9.1 Voltage Setting Pattern Diagram

The pattern diagram of voltage setting and waveforms of the liquid crystal application voltages are as follows.

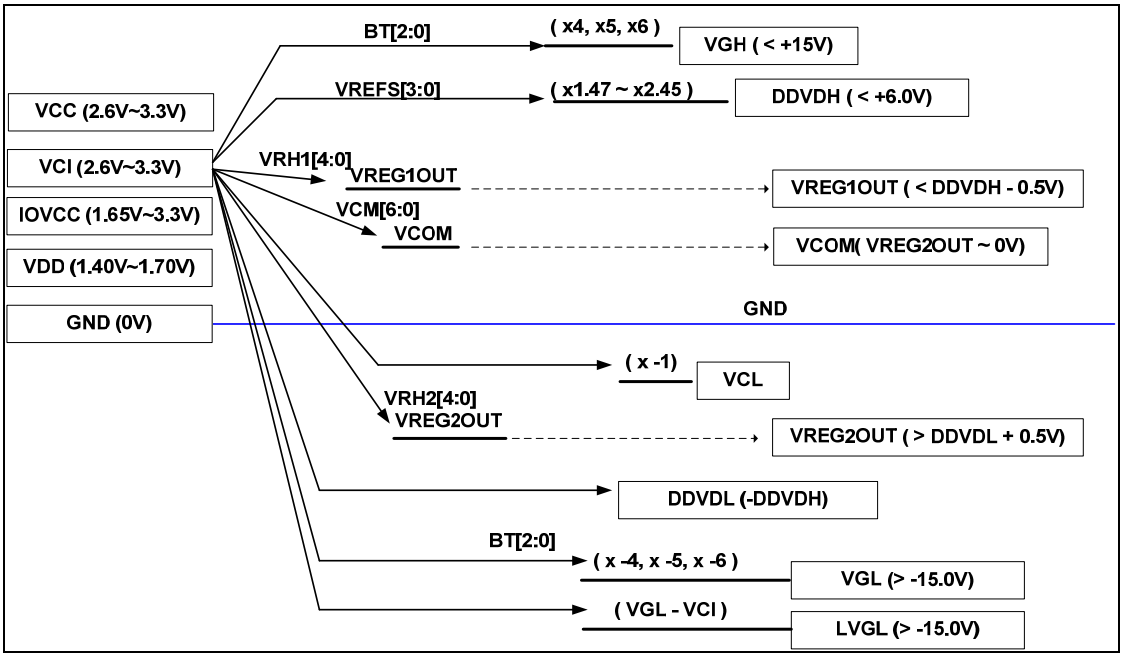
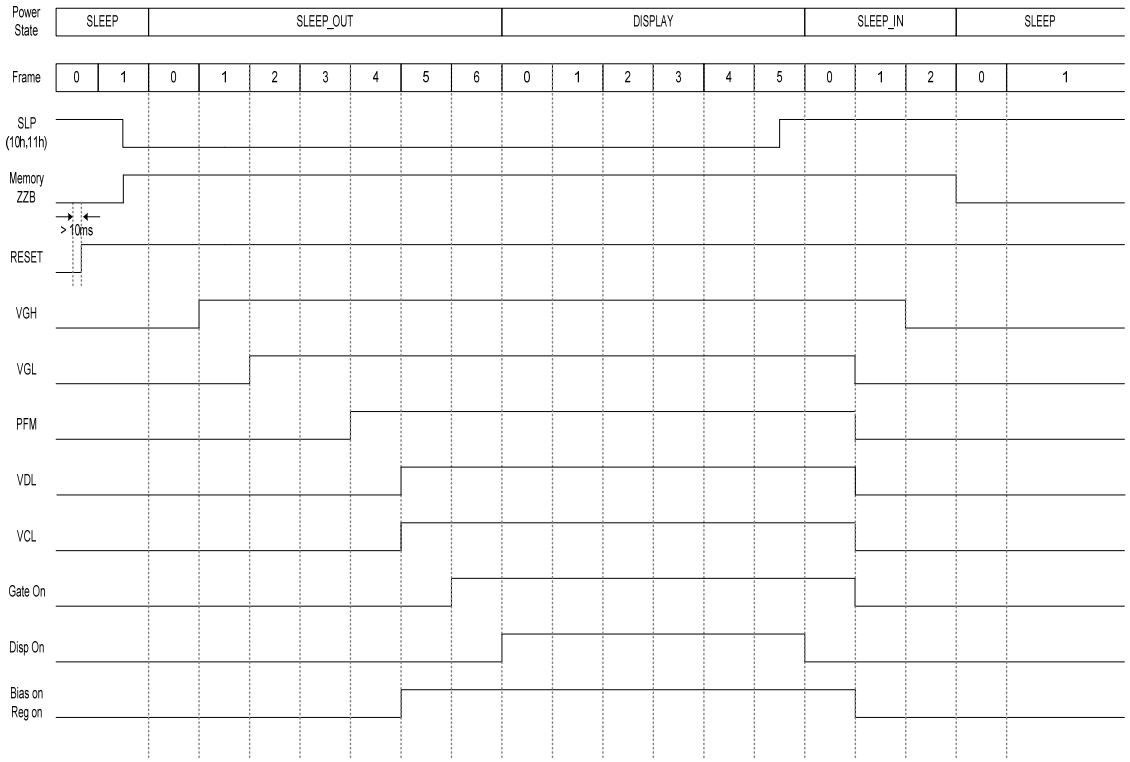


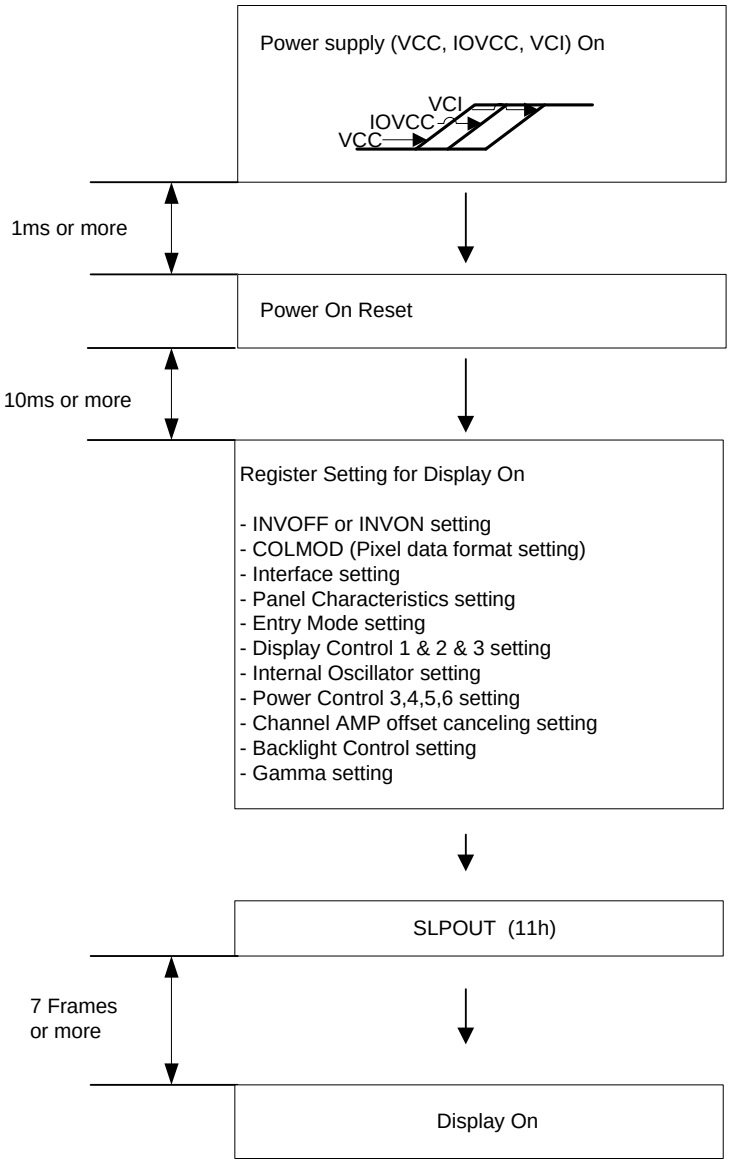
Figure 72. Pattern Diagram for Voltage Setting

5.9.2 Power On / Off Sequence



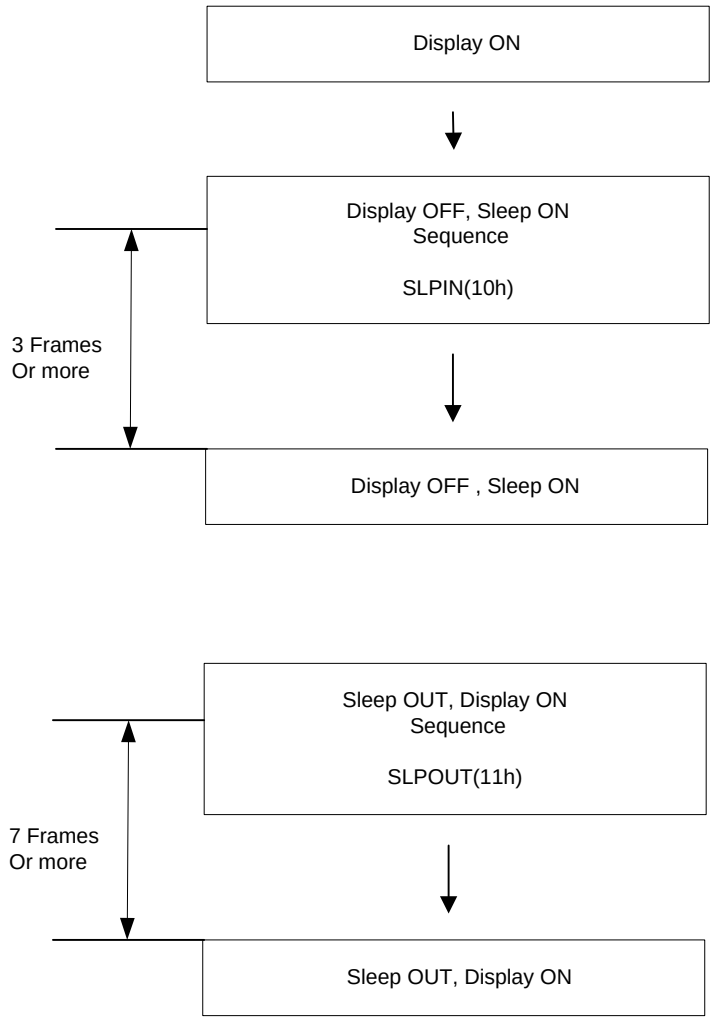
5.9.3 Display On Sequence

Display On Sequence



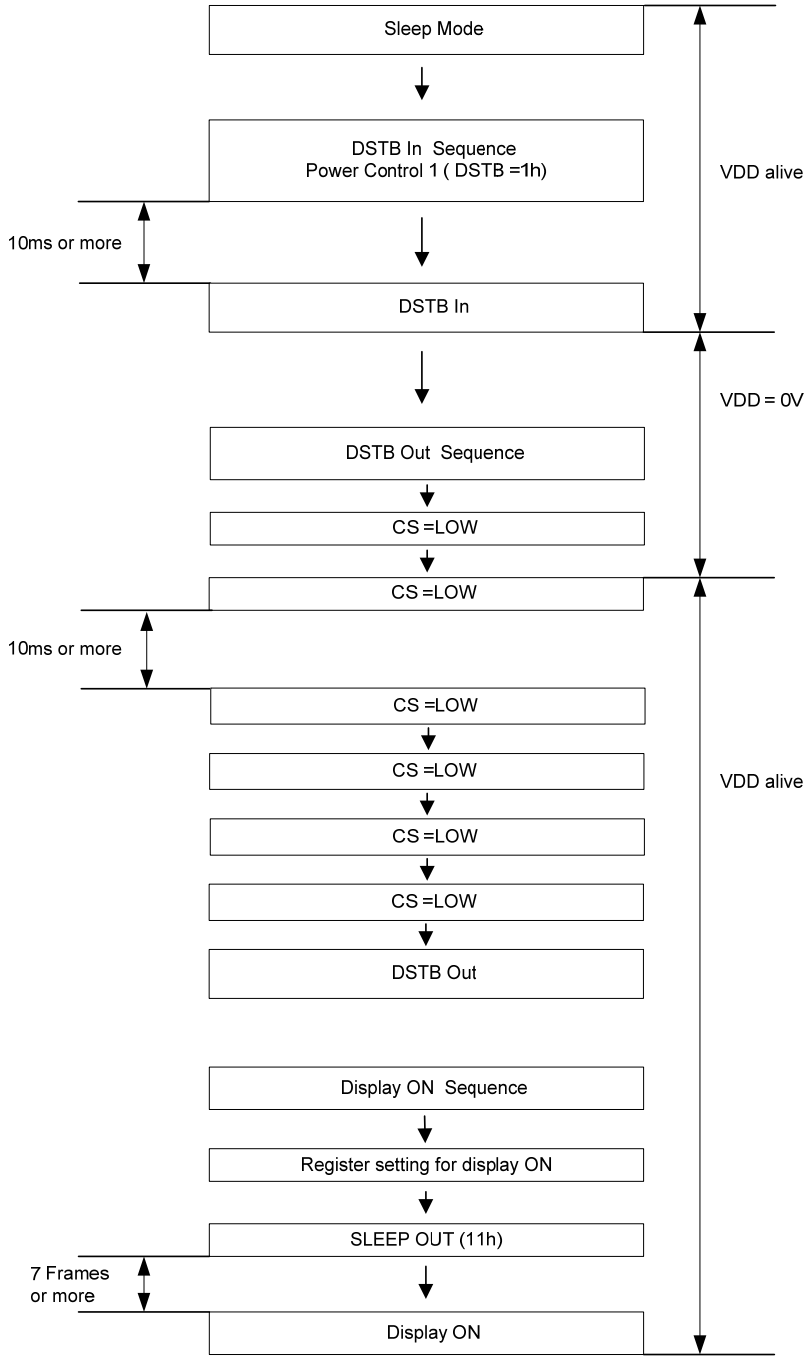
5.9.4 Sleep In, Out Sequence

Sleep In, Out Sequence



5.9.5 DSTB IN, DSTB OUT, Display On Sequence

DSTB IN, DSTB OUT, Display ON Sequences



5.10 Gamma Correction Function

The LG4572B has the gamma correction function to display in 16M colors simultaneously. The gamma correction is performed with 3 groups of registers determining eight reference grayscale levels, which are gradient adjustment, amplitude adjustment and fine-adjustment registers. Each register groups further consists of register groups of positive and negative polarities. Each register group is set independently to other register groups, making the LG4572B available with liquid crystal panels of various characteristics.

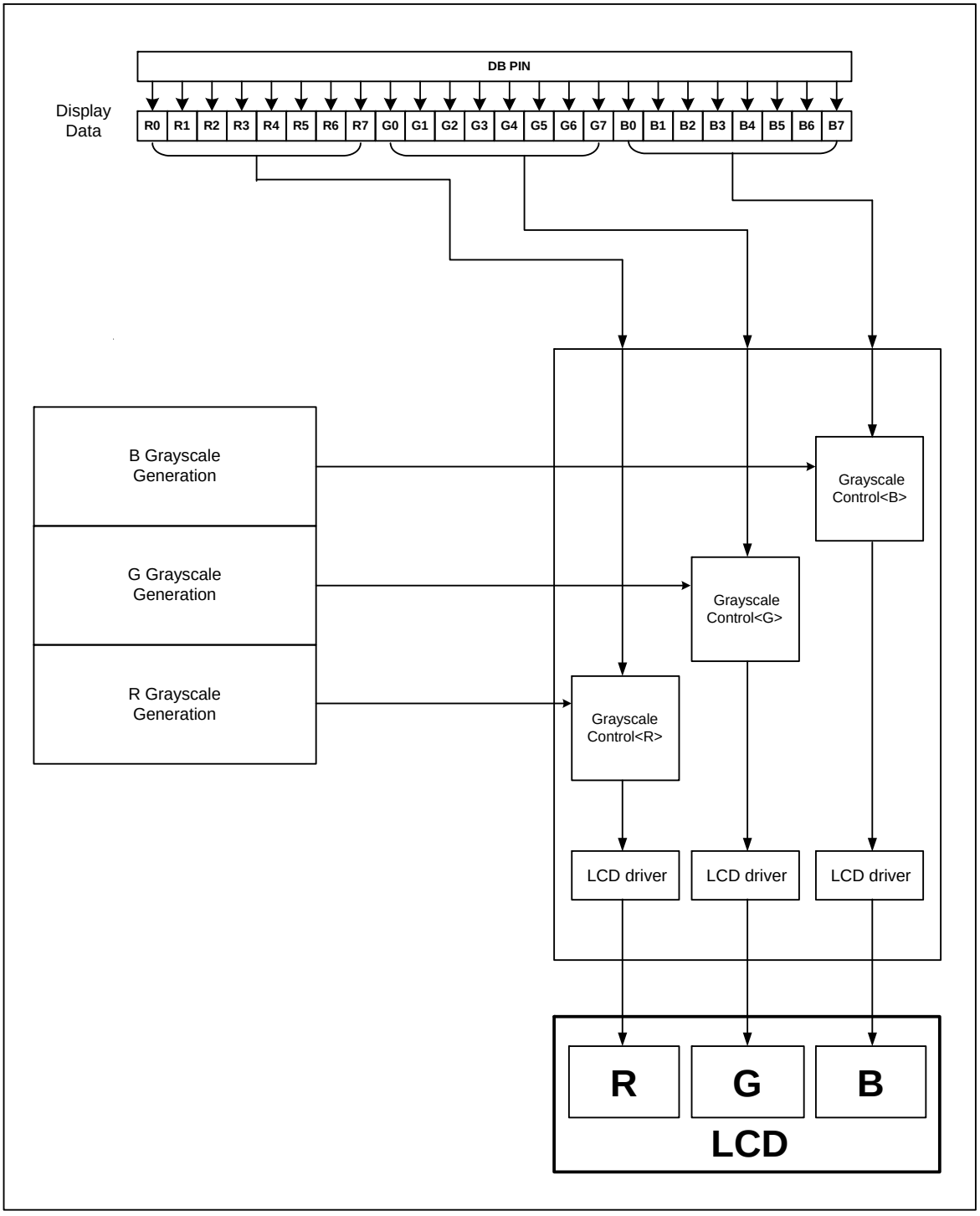


Figure 73. Grayscale Control

5.10.1 Grayscale Generation Unit Configuration

The following figure illustrates the grayscale generation unit of the LG4572B.

To generate 64 grayscale voltages (V0 to V63), the LG4572B first generates eight reference grayscale voltages (VINP0-7/VINN0-7). The grayscale generation unit then divides eight reference grayscale voltages with the ladder resistors incorporated therein.

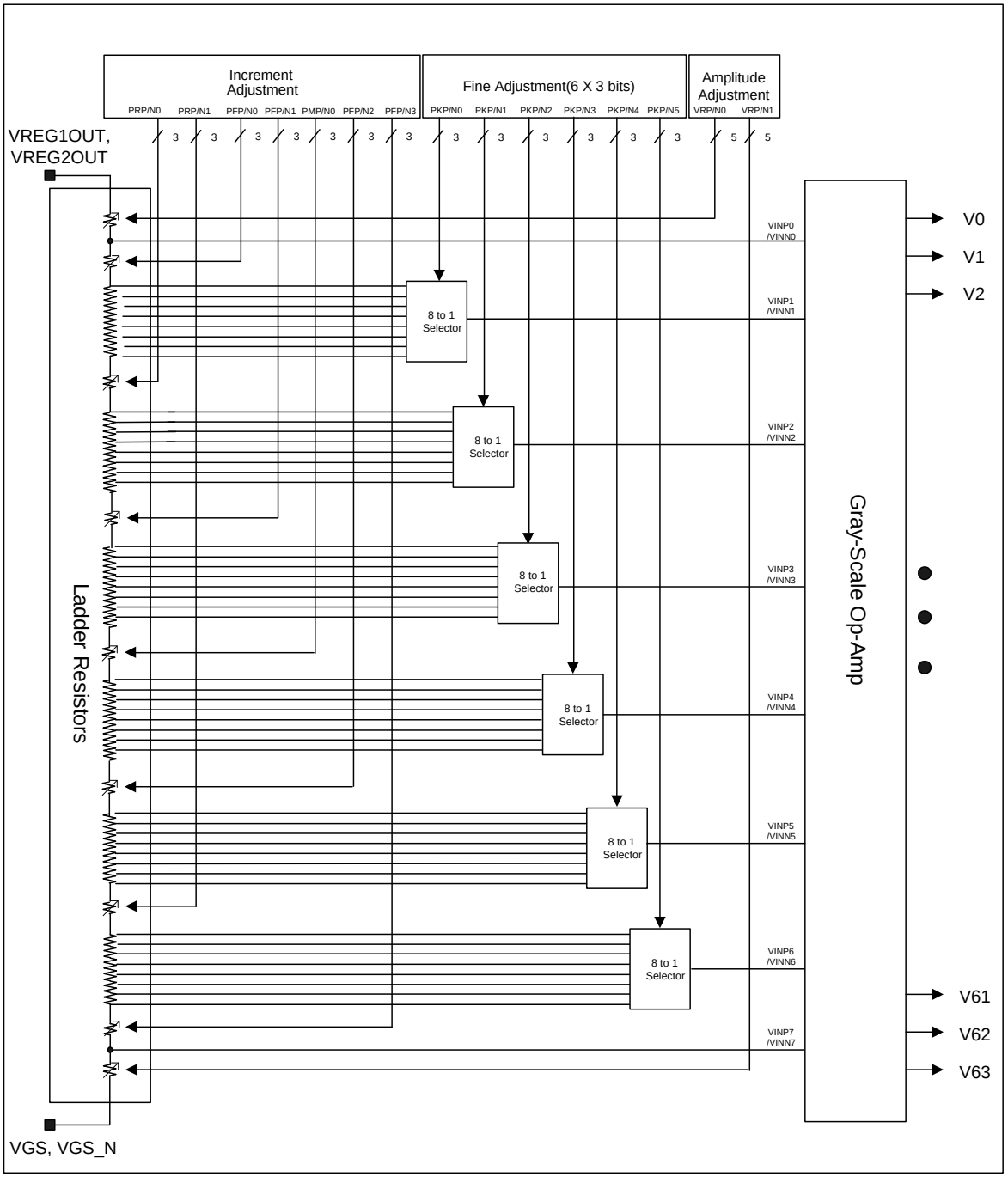


Figure 74. Grayscale Generation unit

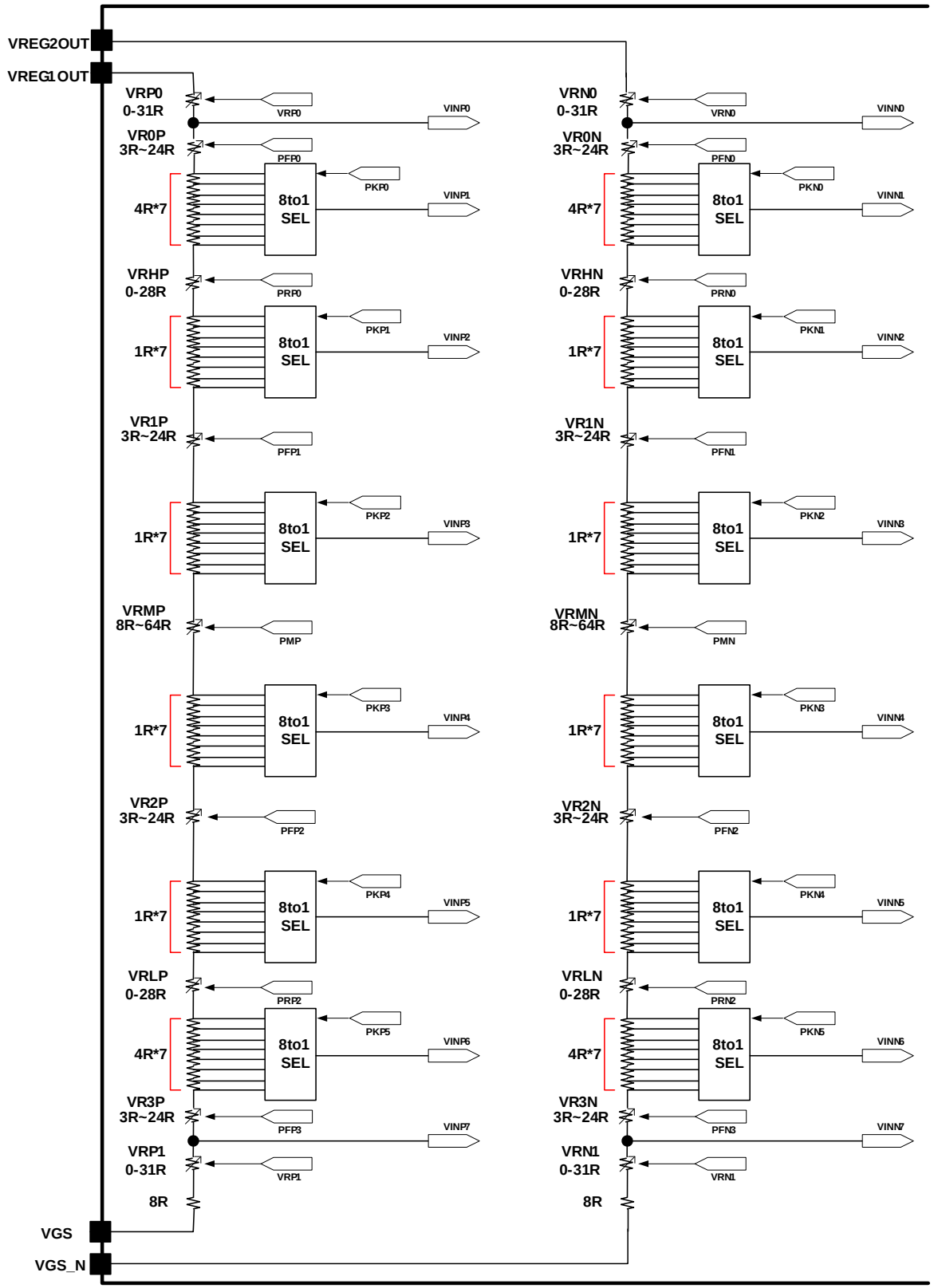


Figure 75. Ladder resistor units and 8-to-1 selectors

5.10.2 Gamma Correction Register

The gamma correction registers of the LG4572B consist of gradient adjustment, amplitude adjustment, and fine adjustment registers, each of which has registers of positive and negative polarities. Each

different register group can be set independently to others, enabling adjustment of grayscale voltage levels in relation to grayscales set optimally for gamma characteristics of a liquid crystal panel. These gamma correction register settings and the reference levels of the 64 grayscales to which the three kinds of adjustments are made (bold lines in the following figure) are common to all RGB dots.

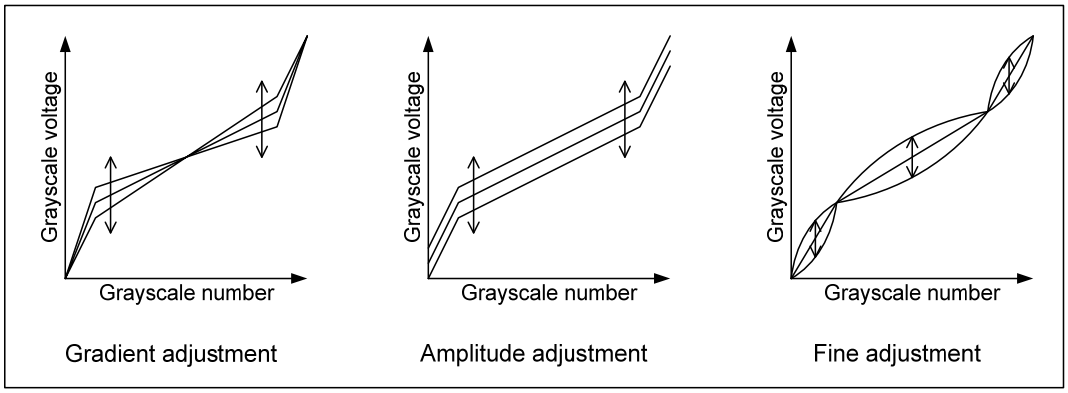


Figure 76. Gamma Adjustments

Gradient adjustment registers

The gradient adjustment registers are used to adjust the gradient of the curve representing the relationship between the grayscale and the grayscale voltage level around middle grayscales without changing the dynamic range. To adjust the gradient, the resistance values of grayscale reference voltage generating variable resistors (VRHP(N)/VRLP(N)) in the middle of the ladder resistor unit are adjusted. The registers consist of positive and negative polarity registers, allowing asymmetric drive.

Amplitude adjustment registers

The amplitude adjustment registers are used to adjust the amplitude of grayscale voltages. To adjust the amplitude, the resistance values of the grayscale voltage generating variable resistors (VRP(N)1/0) at the top and bottom of the ladder resistor unit are adjusted. Same with the gradient registers, the amplitude adjustment registers consist of positive and negative polarity registers.

Fine adjustment registers

The fine adjustment registers are used to fine-adjust grayscale voltage levels. To fine-adjust grayscale voltage levels, fine adjustment registers adjust the reference voltage levels, 8 levels for each register generated from the ladder resistor unit, in respective 8-to-1 selectors. Same with other registers, the fine adjustment registers consist of positive and negative polarity registers.

Table 10. List of registers

Register Groups	Positive Polarity	Negative Polarity	Description
Gradient adjustment	PRP0[2:0]	PRN0[2:0]	Variable resistor VRHP(N)
	PRP1[2:0]	PRN1[2:0]	Variable resistor VRHP(N)
	PFP0[2:0]	PFN0[2:0]	Variable resistor VR0P(N)
	PFP1[2:0]	PFN1[2:0]	Variable resistor VR1P(N)
	PFP2[2:0]	PFN2[2:0]	Variable resistor VR2P(N)
	PFP3[2:0]	PFN3[2:0]	Variable resistor VR3P(N)
	PMP[2:0]	PMN[2:0]	Variable resistor VRMP(N)
Amplitude adjustment	VRP0[4:0]	VRN0[4:0]	Variable resistor VRP(N)0
	VRP1[4:0]	VRN1[4:0]	Variable resistor VRP(N)1
Fine adjustment	PKP0[2:0]	PKN0[2:0]	8-to-1 selector (voltage level of grayscale 1)
	PKP1[2:0]	PKN1[2:0]	8-to-1 selector (voltage level of grayscale 8)
	PKP2[2:0]	PKN2[2:0]	8-to-1 selector (voltage level of grayscale 20)

	PKP3[2:0]	PKN3[2:0]	8-to-1 selector (voltage level of grayscale 43)
	PKP4[2:0]	PKN4[2:0]	8-to-1 selector (voltage level of grayscale 53)
	PKP5[2:0]	PKN5[2:0]	8-to-1 selector (voltage level of grayscale 62)

5.10.3 Ladder Resistors and 8-to-1 Selector

Block Configuration

The grayscale generation unit as illustrated in Figure 75 consists of two ladder resistor units including variable resistors and 8-to-1 selectors. Each 8-to-1 selector selects one of the 8 voltage levels generated from the ladder resistor unit to output as a grayscale reference voltage. Both variable resistors and 8-to-1 selectors are controlled according to the gamma correction registers. This unit has pins to connect a volume resistor externally to compensate differences in various characteristics of panels.

Variable Resistors

The LG4572B uses variable resistors of the following three purposes: gradient adjustment (VRHP(N)/VRLP(N)/VR0~4P(N)/VRMP(N)) and amplitude adjustment (VRP(N)0~1). The resistance values of these variable resistors are set by gradient adjustment registers and amplitude adjustment registers as follows.

Table 11. Amplitude adjustment

Contents of register VRP(N)0[4:0]	Resistance VRP(N)0 VRP(N)1
00000	0R
00001	1R
00010	2R
:	:
:	:
11101	29R
11110	30R
11111	31R

8-to-1 Selectors

The 8-to-1 selector selects one of eight voltage levels generated from the ladder resistor unit according to the fine adjustment register, and output the selected voltage level as a reference grayscale voltage (VINP(N)1~ VINP(N 6). The table below shows the setting in the fine adjustment register and the selected voltage levels for respective reference grayscale voltages.

Table 12. Fine adjustment registers and selected voltage

PKP(N)[2:0]	Selected Voltage					
	VINP(N)1	VINP(N)2	VINP(N)3	VINP(N)4	VINP(N)5	VINP(N)6
3'h0	KVP(N)1	KVP(N)9	KVP(N)17	KVP(N)25	KVP(N)33	KVP(N)41
3'h1	KVP(N)2	KVP(N)10	KVP(N)18	KVP(N)26	KVP(N)34	KVP(N)42
3'h2	KVP(N)3	KVP(N)11	KVP(N)19	KVP(N)27	KVP(N)35	KVP(N)43
3'h3	KVP(N)4	KVP(N)12	KVP(N)20	KVP(N)28	KVP(N)36	KVP(N)44
3'h4	KVP(N)5	KVP(N)13	KVP(N)21	KVP(N)29	KVP(N)37	KVP(N)45
3'h5	KVP(N)6	KVP(N)14	KVP(N)22	KVP(N)30	KVP(N)38	KVP(N)46
3'h6	KVP(N)7	KVP(N)15	KVP(N)23	KVP(N)31	KVP(N)39	KVP(N)47
3'h7	KVP(N)8	KVP(N)16	KVP(N)24	KVP(N)32	KVP(N)40	KVP(N)48

The grayscale voltage levels for V0~V63 grayscales are calculated from the following formula.

Table 13. Formula for calculating voltage (1)

Pin	Formula	Fine adjustment register value	Reference voltage
KVP0	VREG1OUT - ΔV x VRP0/SUMRP	-	VINP0
KVP1	VREG1OUT - ΔV x (VRP0+VR0P+0R)/SUMRP	PKP0= 3'h0	VINP1
KVP2	VREG1OUT - ΔV x (VRP0+VR0P+4R)/SUMRP	PKP0= 3'h1	
KVP3	VREG1OUT - ΔV x (VRP0+VR0P+8R)/SUMRP	PKP0= 3'h2	
KVP4	VREG1OUT - ΔV x (VRP0+VR0P+12R)/SUMRP	PKP0= 3'h3	
KVP5	VREG1OUT - ΔV x (VRP0+VR0P+16R)/SUMRP	PKP0= 3'h4	
KVP6	VREG1OUT - ΔV x (VRP0+VR0P+20R)/SUMRP	PKP0= 3'h5	
KVP7	VREG1OUT - ΔV x (VRP0+VR0P+24R)/SUMRP	PKP0= 3'h6	
KVP8	VREG1OUT - ΔV x (VRP0+VR0P+28R)/SUMRP	PKP0= 3'h7	
KVP9	VREG1OUT - ΔV x (VRP0+VR0P+28R+VRHP)/SUMRP	PKP1= 3'h0	VINP2
KVP10	VREG1OUT - ΔV x (VRP0+VR0P+29R+VRHP)/SUMRP	PKP1= 3'h1	
KVP11	VREG1OUT - ΔV x (VRP0+VR0P+30R+VRHP)/SUMRP	PKP1= 3'h2	
KVP12	VREG1OUT - ΔV x (VRP0+VR0P+31R+VRHP)/SUMRP	PKP1= 3'h3	
KVP13	VREG1OUT - ΔV x (VRP0+VR0P+32R+VRHP)/SUMRP	PKP1= 3'h4	
KVP14	VREG1OUT - ΔV x (VRP0+VR0P+33R+VRHP)/SUMRP	PKP1= 3'h5	
KVP15	VREG1OUT - ΔV x (VRP0+VR0P+34R+VRHP)/SUMRP	PKP1= 3'h6	
KVP16	VREG1OUT - ΔV x (VRP0+VR0P+35R+VRHP)/SUMRP	PKP1= 3'h7	
KVP17	VREG1OUT - ΔV x (VRP0+VR0/1P+35R+VRHP)/SUMRP	PKP2= 3'h0	VINP3
KVP18	VREG1OUT - ΔV x (VRP0+VR0/1P+36R+VRHP)/SUMRP	PKP2= 3'h1	
KVP19	VREG1OUT - ΔV x (VRP0+VR0/1P+37R+VRHP)/SUMRP	PKP2= 3'h2	
KVP20	VREG1OUT - ΔV x (VRP0+VR0/1P+38R+VRHP)/SUMRP	PKP2= 3'h3	
KVP21	VREG1OUT - ΔV x (VRP0+VR0/1P+39R+VRHP)/SUMRP	PKP2= 3'h4	
KVP22	VREG1OUT - ΔV x (VRP0+VR0/1P+40R+VRHP)/SUMRP	PKP2= 3'h5	
KVP23	VREG1OUT - ΔV x (VRP0+VR0/1P+41R+VRHP)/SUMRP	PKP2= 3'h6	
KVP24	VREG1OUT - ΔV x (VRP0+VR0/1P+42R+VRHP)/SUMRP	PKP2= 3'h7	
KVP25	VREG1OUT - ΔV x (VRP0+VR0/1P+42R+VRHP +VRMP)/SUMRP	PKP3= 3'h0	VINP4
KVP26	VREG1OUT - ΔV x (VRP0+VR0/1P+43R+VRHP +VRMP)/SUMRP	PKP3= 3'h1	
KVP27	VREG1OUT - ΔV x (VRP0+VR0/1P+44R+VRHP +VRMP)/SUMRP	PKP3= 3'h2	
KVP28	VREG1OUT - ΔV x (VRP0+VR0/1P+45R+VRHP +VRMP)/SUMRP	PKP3= 3'h3	
KVP29	VREG1OUT - ΔV x (VRP0+VR0/1P+46R+VRHP +VRMP)/SUMRP	PKP3= 3'h4	
KVP30	VREG1OUT - ΔV x (VRP0+VR0/1P+47R+VRHP +VRMP)/SUMRP	PKP3= 3'h5	
KVP31	VREG1OUT - ΔV x (VRP0+VR0/1P+48R+VRHP +VRMP)/SUMRP	PKP3= 3'h6	
KVP32	VREG1OUT - ΔV x (VRP0+VR0/1P+49R+VRHP +VRMP)/SUMRP	PKP3= 3'h7	
KVP33	VREG1OUT - ΔV x (VRP0+VR0/1/2P+49R+VRHP +VRMP)/SUMRP	PKP4= 3'h0	VINP5
KVP34	VREG1OUT - ΔV x (VRP0+VR0/1/2P+50R+VRHP +VRMP)/SUMRP	PKP4= 3'h1	
KVP35	VREG1OUT - ΔV x (VRP0+VR0/1/2P+51R+VRHP +VRMP)/SUMRP	PKP4= 3'h2	
KVP36	VREG1OUT - ΔV x (VRP0+VR0/1/2P+52R+VRHP +VRMP)/SUMRP	PKP4= 3'h3	
KVP37	VREG1OUT - ΔV x (VRP0+VR0/1/2P+53R+VRHP +VRMP)/SUMRP	PKP4= 3'h4	
KVP38	VREG1OUT - ΔV x (VRP0+VR0/1/2P+54+VRHP +VRMP)/SUMRP	PKP4= 3'h5	
KVP39	VREG1OUT - ΔV x (VRP0+VR0/1/2P+55R+VRHP +VRMP)/SUMRP	PKP4= 3'h6	
KVP40	VREG1OUT - ΔV x (VRP0+VR0/1/2P+56R+VRHP +VRMP)/SUMRP	PKP4= 3'h7	

Pin	Formula	Fine adjustment register value	Reference voltage
KVP41	VREG1OUT - ΔV x (VRP0+VR0/1/2P+56R+VRHP +VRMP+VRLP)/SUMRP	PKP5= 3'h0	VINP6
KVP42	VREG1OUT - ΔV x (VRP0+VR0/1/2P+60R+VRHP +VRMP+VRLP)/SUMRP	PKP5= 3'h1	
KVP43	VREG1OUT - ΔV x (VRP0+VR0/1/2P+64R+VRHP +VRMP+VRLP)/SUMRP	PKP5= 3'h2	
KVP44	VREG1OUT - ΔV x (VRP0+VR0/1/2P+68R+VRHP +VRMP+VRLP)/SUMRP	PKP5= 3'h3	
KVP45	VREG1OUT - ΔV x (VRP0+VR0/1/2P+72R+VRHP +VRMP+VRLP)/SUMRP	PKP5= 3'h4	
KVP46	VREG1OUT - ΔV x (VRP0+VR0/1/2P+76R+VRHP+VRMP +VRLP)/SUMRP	PKP5= 3'h5	
KVP47	VREG1OUT - ΔV x (VRP0+VR0/1/2P+80R+VRHP+VRMP +VRLP)/SUMRP	PKP5= 3'h6	
KVP48	VREG1OUT - ΔV x (VRP0+VR0/1/2P+84R+VRHP+VRMP +VRLP)/SUMRP	PKP5= 3'h7	
KVP49	VREG1OUT - ΔV x (VRP0+VR0/1/2/3P+84R+VRHP+VRMP +VRLP)/SUMRP	-	VINP7

SUMRP: Sum of positive ladder resistors =
92R+VRHP+VRLP+VRP0+VRP1+VR0P+VR1P+VR2P+VR3P+VRMP
ΔV: Difference in electrical potential between VREG1OUT and VGS

Table 14. Formula for calculating voltage (2)

Grayscale voltage	Formula
V0	VINP0
V1	VINP1
V2	VINP2+(VINP1-VINP2) x (30/48)
V3	VINP2+(VINP1-VINP2) x (23/48)
V4	VINP2+(VINP1-VINP2) x (16/48)
V5	VINP2+(VINP1-VINP2) x (12/48)
V6	VINP2+(VINP1-VINP2) x (8/48)
V7	VINP2+(VINP1-VINP2) x (4/48)
V8	VINP2
V9	VINP3+(VINP2-VINP3) x (22/24)
V10	VINP3+(VINP2-VINP3) x (20/24)
V11	VINP3+(VINP2-VINP3) x (18/24)
V12	VINP3+(VINP2-VINP3) x (16/24)
V13	VINP3+(VINP2-VINP3) x (14/24)
V14	VINP3+(VINP2-VINP3) x (12/24)
V15	VINP3+(VINP2-VINP3) x (10/24)
V16	VINP3+(VINP2-VINP3) x (8/24)
V17	VINP3+(VINP2-VINP3) x (6/24)
V18	VINP3+(VINP2-VINP3) x (4/24)
V19	VINP3+(VINP2-VINP3) x (2/24)
V20	VINP3
V21	VINP4+(VINP3-VINP4) x (22/23)
V22	VINP4+(VINP3-VINP4) x (21/23)
V23	VINP4+(VINP3-VINP4) x (20/23)
V24	VINP4+(VINP3-VINP4) x (19/23)
V25	VINP4+(VINP3-VINP4) x (18/23)
V26	VINP4+(VINP3-VINP4) x (17/23)
V27	VINP4+(VINP3-VINP4) x (16/23)
V28	VINP4+(VINP3-VINP4) x (15/23)
V29	VINP4+(VINP3-VINP4) x (14/23)
V30	VINP4+(VINP3-VINP4) x (13/23)
V31	VINP4+(VINP3-VINP4) x (12/23)

Grayscale voltage	Formula
V32	VINP4+(VINP3-VINP4) x (11/23)
V33	VINP4+(VINP3-VINP4) x (10/23)
V34	VINP4+(VINP3-VINP4) x (9/23)
V35	VINP4+(VINP3-VINP4) x (8/23)
V36	VINP4+(VINP3-VINP4) x (7/23)
V37	VINP4+(VINP3-VINP4) x (6/23)
V38	VINP4+(VINP3-VINP4) x (5/23)
V39	VINP4+(VINP3-VINP4) x (4/23)
V40	VINP4+(VINP3-VINP4) x (3/23)
V41	VINP4+(VINP3-VINP4) x (2/23)
V42	VINP4+(VINP3-VINP4) x (1/23)
V43	VINP4
V44	VINP5+(VINP4-VINP5) x (22/24)
V45	VINP5+(VINP4-VINP5) x (20/24)
V46	VINP5+(VINP4-VINP5) x (18/24)
V47	VINP5+(VINP4-VINP5) x (16/24)
V48	VINP5+(VINP4-VINP5) x (14/24)
V49	VINP5+(VINP4-VINP5) x (12/24)
V50	VINP5+(VINP4-VINP5) x (10/24)
V51	VINP5+(VINP4-VINP5) x (8/24)
V52	VINP5+(VINP4-VINP5) x (6/24)
V53	VINP5+(VINP4-VINP5) x (4/24)
V54	VINP5+(VINP4-VINP5) x (2/24)
V55	VINP5
V56	VINP6+(VINP5-VINP6) x (44/48)
V57	VINP6+(VINP5-VINP6) x (40/48)
V58	VINP6+(VINP5-VINP6) x (36/48)
V59	VINP6+(VINP5-VINP6) x (32/48)
V60	VINP6+(VINP5-VINP6) x (25/48)
V61	VINP6+(VINP5-VINP6) x (18/48)
V62	VINP6
V63	VINP7

Notes:

1. Make sure DDVDH-V0 > 0.5V
2. Based on the generated 64 gray levels above, interpolated 4 levels are newly generated. Eventually total 253 gray levels are generated to acquire 16.2M color depth.

5.11 Oscillator

LG4572B could generate RC oscillation with an internal oscillation resistor and capacitor for the main display clock and power boosting circuit, like as step-up and step-down.

5.12 OTP Control

LG4572B has an embedded OTP which is a 32-bit one-time programmable (OTP) IP from eMemory Technology Inc. (EO01X32BDV6).

EO01X32BDV6 is a CMOS, 1bit (1-bit) program OTP logic device. The main memory block is organized as 8-bits by 4 banks. See the data sheet of EO01X32BDV6.

The pins of the embedded OTP can be controlled using the OTP control 1 (C4h) register as shown below.

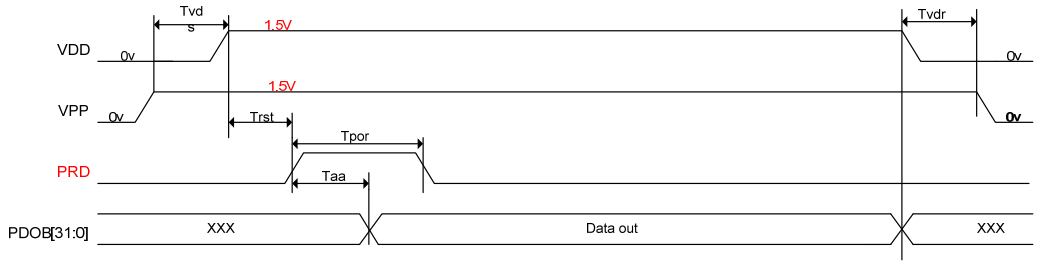
Table 15. OTP Setting Conditions

EO01X32BDV6	Bit fields of register C4h
PTM = 0V/VDD	PTM[1:0] = 00/11
PRD = 0V/VDD	PRD = 0/1
VPP = VDD/7.75V	VPP = 0/1
PPROG = 0V/VDD	PPROG = 0/1
PWE = 0V/VDD	PWE = 0/1
PA[1:0] = 0V/VDD	PA[1:0] = 0/1
PDIN[7:0] = 0V/VDD	PDIN[7:0] = 0/1

The RA[1:0] of register F9h selects one of four OTP bytes.

Accessing OTP control registers, follow the timing requirements of read and program cycles.

Read Cycle



Program Cycle

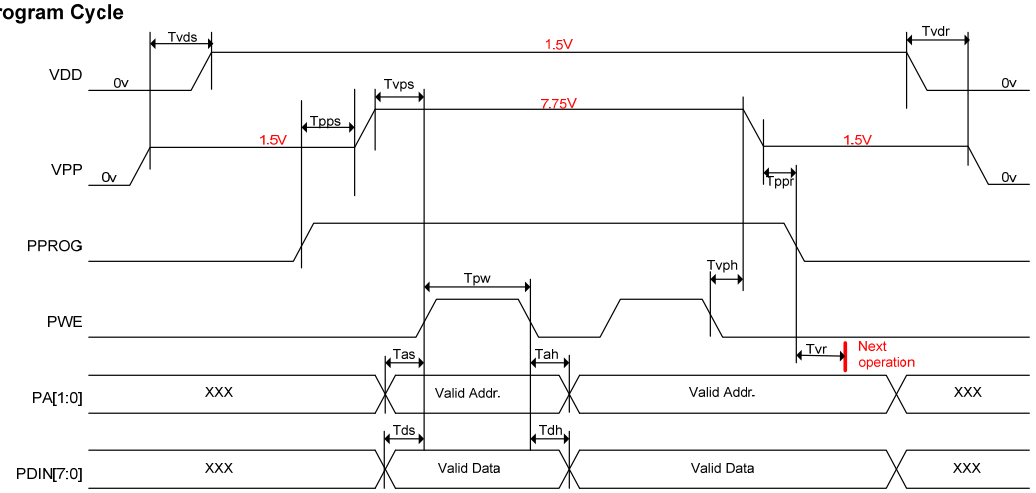


Figure 77. OTP Timing

Table 16. OTP timing characteristics

Parameter	Symbol	EO01X32BDV6		Unit
		Min	Max	
Rising Time / Falling Time	Tr / Tf	-	1	ns
Data Access Time	Taa	-	70	ns
Power-on Pulse Width Time	TPRD	200	-	ns
Address / Data Setup Time	Tas / Tds	4	-	ns
Address / Data Hold Time	Tah / Tdh	9	-	ns
External VPP Setup Time	Tvps	0	-	ns
External VPP Hold Time	Tvph	0	-	ns
Program Recovery Time	Tvr	10	-	µs
Program Pulse Width	Tpw	300	350	µs
VDD Setup Time	Tvds	0	-	ms
VDD Recovery Time	Tvdr	0	-	ms
PPROG Setup Time	Tpps	10	-	ns
PPROG Recovery Time	Tppr	10	-	ns
Power on Read Time	Trst	20	-	ns

Notes:

1. All electrical and timing parameters listed above are based on SPICE (or equivalent) simulations and subject to changes after silicon verification.
2. All program signals that align together in the timing diagrams should be derived from the rising clock edge.
3. All timing measurements are from the 50% of the input to 50% of the output.
4. All input waveforms have rising time (tr) and falling time (tf) of 1ns from 10% to 90% of the input waveforms.
5. For capacitive loads greater than 1pF, access time will increase by 1ns per pF of additional loading.
6. Program time means one byte program time in user mode

The following sequences are for writing and reading data into and/or from OTP.

OTP Programming Sequence

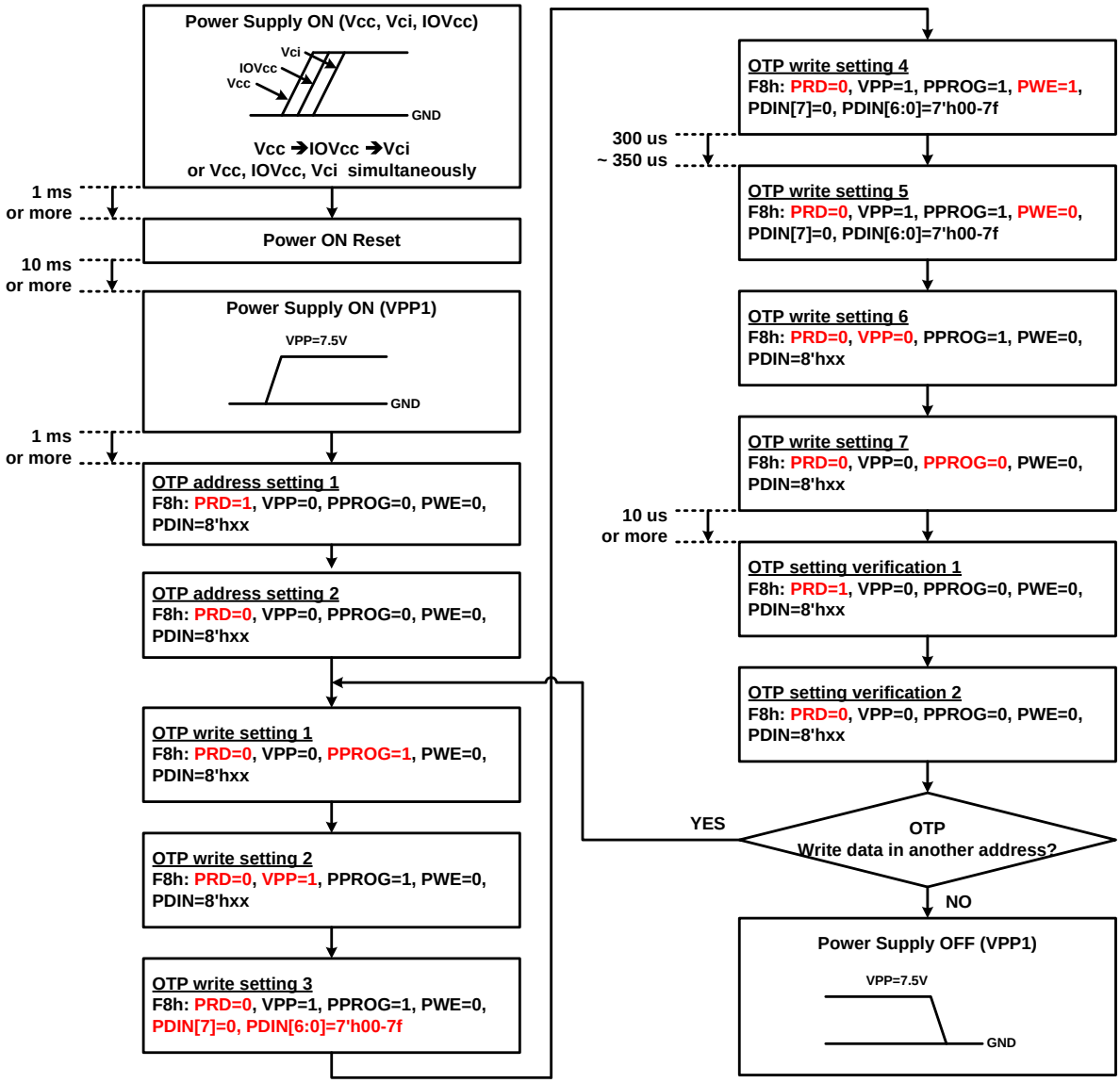


Figure 78. OTP Programming Sequence

OTP Read Sequence

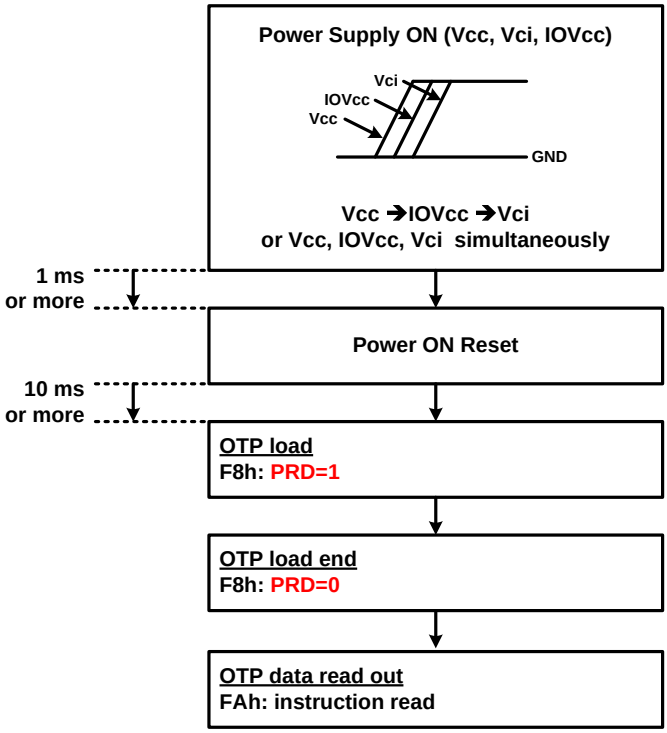


Figure 79. OTP Read Sequence

5.13 EEPROM Control

If there is an external EEPROM connected to LG4572B, LG4572B can do register writing through EEPROM reading function via I2C interface. Only data reading from EEPROM is available in LG4572B. Data writing to EEPROM device from LG4572B is not supported.

After SLEEP OUT, ROM data reading operation will start according to the following format. Only if this format of data written in EEPROM can be read into LG4572B, which means register writing.

{ Length, Address, Data }

For example, if user wants to do register writing of BGAMMAP and BGAMMAN in the Manufacture command set, the ROM data should be written as following pattern.

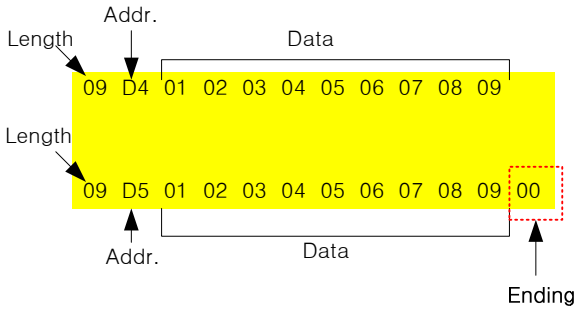


Figure 80. One Example of EEPROM Data Format to be read by LG4572B

There are two PADs in LG4572B for I2C interface. They are RSDA and RSCL. The RSDA is for reading data from EEPROM. This pad should be connected to external pull-up resistor with around 10kohm. And the other node of this pull-up resistor 10kohm is connected to IOVCC. The application is as follows.

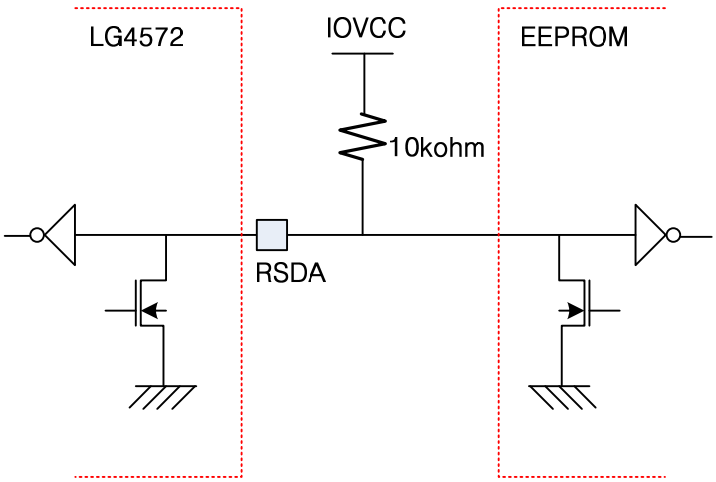


Figure 81. Connection Diagram of EEPROM and LG4572B with 10kohm external resistor between RSDA and IOVCC.

The RSCL is a clock for data reading from EERPOM and is an output signal. The maximum frequency of RSCL should be less than 400kHz. To set the frequency of RSCL, the following equation can be used.

RSCL Frequency = (RC OSC Frequency) / (16 – RFCLK)

Where the RFCLK can be set from 0 to 12 using RFCLK[3:0] register. The other values of 13, 14, and 15 are not valid. The frequency of RC OSC can be set by using FRS[4:0] register. The following is for easy reading data from external EEPROM. The maximum RSCL frequency can limit the number of writable registers in LG4572B. Because the wait time in the following EEPROM Read Operation diagram is less than 5ms normally. But the system allows the longer wait time, the number of writable registers in LG4572B can be increased.

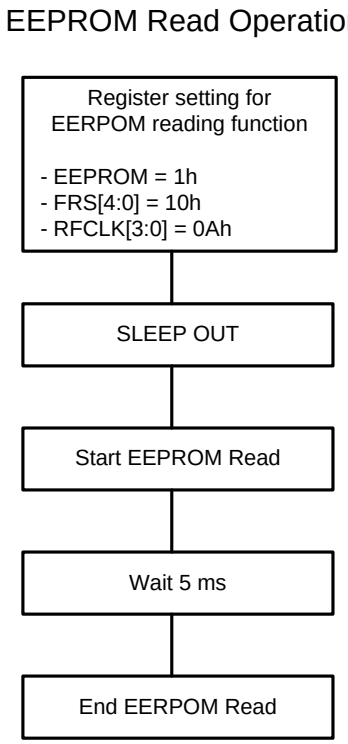


Figure 82. EERPOM Read Operation by LG4572B

6 Commands

6.1 Command List

User Command Set

Name	Addr	Size	R/nW	D/nC	b7	b6	b5	b4	b3	b2	b1	b0	Default	Description
NOP	00h	0	W	0										No Operation
SWRESET	01h	0	W	0	SWRST = 1 (self cleared after a fixed delay)								0	Software Reset
RDDPM	0Ah	1	R	0										Read Display Power Mode
				1	0	~~IDM~~	PTL	nSLP	NOR	DISP	0	0	08h	
RDDMADCTL	0Bh	1	R	0										Read Display MADCTL
				1	MY	MX	MV	0	BGR	0	~~FH~~	FV	00h	
RDDCOLMOD	0Ch	1	R	0										Read Display Pixel Format
				1	0	DPIPF[2:0]			0	DBIPF[2:0]			77h	
RDDIM	0Dh	1	R	0										Read Display Image Mode
				1	0	0	INV	0	0	0	0	0	00h	
RDDSM	0Eh	1	R	0										Read Display Signal Mode
				1	TE	TEM							00h	
SLPIN	10h	0	W	0	nSLP = 1								0	Sleep In Powers for the display are off
SLPOUT	11h	0	W	0	nSLP = 0									Sleep Out Powers for the display are on
PTLON	12h	0	W	0	PTL = 1								0	Partial Mode On
NRTON	13h	0	W	0	NOR = 1 (equivalently PTL = 0 and VSCR = 0)								1	Normal Display Mode On
INVOFF	20h	0	W	0	INV = 0								0	Display Inversion Off
INVON	21h	0	W	0	INV = 1									Display Inversion On
DISPOFF	28h	0	W	0	DISP = 0								0	Display Off
DISPON	29h	0	W	0	DISP = 1									Display On
CASET	2Ah	4	W	0										Set column address
				1							SC[9:8]		00h	SC – Start column address EC – End column address
				1	SC[7:0]								00h	
				1							EC[9:8]		01h	
				1	EC[7:0]								DFh	
PASET	2Bh	4	W	0										Set page address
				1							SP[9:8]		00h	SP – Start page address EP – End page address
				1	SP[7:0]								00h	
				1							EP[9:8]		03h	
				1	EP[7:0]								5fh	
RAMWR	2Ch	variable	W	0	DB[23:0]									Write Memory Start
RAMRD	2Eh	variable	R	0	DB[23:0]									Read Memory Start
PTLAR	30h	4	W	0										Partial Area Definition
				1							SR[9:8]		00h	SR – Start row ER – End row
				1	SR[7:0]								00h	
				1							ER[9:8]		03h	
				1	ER[7:0]								5Fh	
TEOFF	34h	0	W	0	TE = 0								00h	Tearing Effect Line Off
TEON	35h	1	W	0	TE = 1									Tearing Effect Line On
				1								TEM	00h	TEM - mode of the TE output line
MADCTL	36h	1	W	0										Memory Access Control

				1	MY	MX	MV		BGR		~~FH~~	FV	00h	MY – Page Address Order MX – Column Address Order MV – Page/Column Addressing Order BGR – RGB/BGR order ~~FH – Flip horizontal (=DIR)~~ FV – Flip vertical (=GS)
~~IDMOFF~~	~~38h~~	~~0~~	~~W~~	~~0~~	~~IDM = 0~~									~~Idle Mode Off~~ ~~Full color depth is used on the display panel.~~
~~IDMON~~	~~39h~~	~~0~~	~~W~~	~~0~~	~~IDM = 1~~									~~Idle Mode On~~ ~~Reduced color depth is used on the display panel.~~
COLMOD	3Ah	1	W	0										Interface Pixel Format
				1		DPIPF[2:0]				DBIPF[2:0]			77h	DPIPF[2:0] - DPI pixel format DPIPF[2:0] - DBI pixel format
RAMWRC	3Ch	variable	W	0	DB[23:0]									Write Memory Continue
RAMRDC	3Eh	variable	R	0	DB[23:0]									Read Memory Continue
TELINE	44h	2	W	0										Set tear Scanline
				1	TELINE[15:8]								00h	TELINE - tear scanline
				1	TELINE [7:0]								00h	
SCANLINE	45h	2	R	0										Get Scanline
				1	SCANLINE[15:8]								xxh	SCANLINE – Read display scanline
				1	SCANLINE [7:0]								xxh	
WRDISBV	51h	1	W	0										Write Display Brightness
				1	DBV [7:0]								00h	DBV - manual display brightness
RDDISBV	52h	1	R	0										Read Display Brightness Value
				1	DBV [7:0]								00h	
WRCTRLD	53h	1	W	0										Write Control Display
				1			BCTRL		DD	BL			00h	BCTRL – brightness control block on/off DD – display dimming for manual brightness setting BL – backlight control on/off
RDCTRLD	54h	1	R	0										Read Control Display
				1			BCTRL		DD	BL			xxh	
WRCABC	55h	1	W	0										Write content Adaptive Brightness Control
				1								CABC[1:0]	00h	CABC - content adaptive brightness control mode
RDCABC	56h	1	R	0										Read content Adaptive Brightness Control
				1								CABC[1:0]	00h	
WRCABCMB	5Eh	1	W	0										Write CABC Minimum Brightness
				1	CMB[7:0]								00h	CMB - minimum brightness
RDCABCMB	5Fh	1	R	0										Read CABC Minimum Brightness
				1	CMB[7:0]								00h	
RDDDB	A1h	variable	R	0										Read DDB Start
				1	DB[23:0]								-	
RDDDBC	A8h	variable	R	0										Read DDB Continue
				1	DB[23:0]								-	

Manufacturer Command Set

Name	Addr	Size	R/nW	D/nC	b7	b6	b5	b4	b3	b2	b1	b0	Default	Description
RGBIF	B1	3	R/W	0										RGB Interface setting
				1	DPICC			SYNC	CKPL	HSPL	VSPL	DEPL	06h	DPICC - DPI color coding (see Table 6) 0: config 1 for both 16bpp and 18bpp, 1: config 3 for 16bpp and config 2 for 18bpp SYNC – Sync mode, 0: VS+HS+DE , 1: VS+HS CKPL – PCLK polarity. Rising(0) or Falling (1) edge. HSPL – HSYNC polarity. Active high(0) or low(1) VSPL – VSYNC polarity. Active high(0) or low(1) DEPL – DE polarity. Active high(0) or low(1)
				1		HBP[6:0]							1Eh	HBP – H back porch in PCLK (Used only if RGBIF , SYNC = 1)
				1	VBP[7:0]								0Ch	VBP – V back porch in line (Used only if RGBIF , SYNC = 1)
PANELSET	B2h	2	R/W	0										Panel Characteristics Setting
				1			LR	SELP		HRS[1:0]		REV	10h	HRS – H resolution. 0: 480 pixels, 1: 360 pixels, 2: 320, 3:240 REV – Normally black (0) or white (1) panel SELP – panel 1: Hydis 0 : LGD LR – gate L/R signal control
				1	VRS[7:0]								D8h	VRS – V resolution divided by 4(NL)
PANELDRV	B3h	1	R/W	0										Panel Drive Setting
				1							DINV[1:0]		02h	DINV – dot inversion mode 0: column inversion, 1: 1-dot, 2: 2-dot, 3: 3-dot
DISPMODE	B4h	1	R/W	0										Display Mode Control
				1						DITH			04h	DITH – dither enable (1:enable, 0:truncation)
DISPCTL1	B5	5	R/W	0										Display Control 1 (Source Output Control)
				1	SDT[7:0]								10h	SDT – Source output delay; [1:255] pixel clocks
				~~1~~		~~SHPN[6:0]~~							~~10h~~	~~SHPN – equalize level period; [0..127] pixel clocks~~
				~~1~~		~~ENGND[6:0]~~							~~10h~~	~~ENGND – GND level period; [1..127] pixel clocks~~
				~~1~~	~~SHIZ[7:0]~~								~~00h~~	~~SHIZ – source output Hi-Z control via SAP~~
				1			PTS[1:0]					SLT	20h	PTS – source output in non-display area 0 : black, 10 : GND, 11 : High-Z SLT – spread source outputs
DISPCTL2	B6h	6	R/W	0										Display Control 2 (Gate Output Control)
				1				GSWAP	FVST	ASG	SDM	FHN	01h	GSWAP – 1: enable GCLK swap, 0:Normal GCLK FVST – 1 : 2-phase advanced, 0:Normal phase ASG – 1: single drive, 0: dual drive FHN – 1: overlap, 0: non overlap SDM – 1: 8 phases, 0: 4 phases
				1	CLW[7:0]								18h	CLW – GCLK non-overlap timing; [1..255] pixel clocks
				1			GTO[5:0]						02h	GTO – GPWR toggle frequency; [1..63] frames
				1	GNO[7:0]								40h	GNO – GPWR non-overlap timing; [1..255] pixel clocks
				1	FTI[7:0]								10h	FTI – GVST output delay; [1..255] pixel clocks
				1	GPM[7:0]								00h	GPM – Duration of gate pulse modulation
DISPCTL3	B7h	5	R/W	0										Display Control 3 (Command Mode Display)

				1	RTN[7:0]								46h	RTN – Sets 1H(line) period. [70~255]
				1	FP[7:0]								06h	FP - vertical front porch of command mode display
				1	BP[7:0]								0Ch	BP - vertical back porch of command mode display
				1							DIV[1:0]		00h	DIV - division ratio of the internal oscillator
				1						TEI[2:0]			00h	TEI - TE output interval in frames
OSCSET	C0h	2	R/W	0										Internal Oscillator Setting
				1						OSC SYNC	EXT OSC	OSC	01h	OSCSYNC – Osc Sync mode control EXTOSC – Use the external osc instead of internal osc OSC – use the internal osc instead of PCLK for step-up circuits
				1				FRS[4:0]					00h	FRS – Oscillator frequency control
PWRCTL1	C1h	1	R/W	0										Power Control 1 (Power State Selection)
				1					DTE		STB	DSTB	02h	DTE – Manual gate output enable DSTB – Deep standby mode STB – Standby bias state disable
PWRCTL2	C2h	1	R/W	0										Power Control 2 (Manual Step-up Circuit Enable)
				1			LVGL	VDL	VCL	VGL	VGH	VDH	00h	LVGL - Enable step-up circuit for LVGL VDL - Enable step-up circuit for VDL VCL - Enable step-up circuit for VCL (= VCOMG) VGL - Enable step-up circuit for VGL (= PON) VGH - Enable step-up circuit for VGH VDH - Enable PFM boost circuit for DDVDH
PWRCTL3	C3h	5	R/W	0										Power Control 3 (Step-up Circuit Control)
				1						STMODE[2:0]			00h	Step-up auto power mode
				1						DC1[2:0]			04h	Frequency of the step-up circuit 2
				1						DC2[2:0]			03h	Frequency of the step-up circuit 3
				1						DC3[2:0]			03h	Frequency of the step-up circuit 4
				1						DCPFM[2:0]			04h	Frequency of the PFM boost circuit
PWRCTL4	C4h	6	R/W	0										Power Control 4 (Regulator Control)
				1			OPB	BMB		BDC[2:0]			00h	OPB – Normal & Buffered Bias Selection BMB – Bias Line Current Adjustment BDC – Channel Amp bias current control
				1		GDC[2:0]				AP[2:0]			00h	GDC – Gray – scale Amp bias current control AP – Adjusts the constant current in the operational amplifier circuit in the LCD power supply circuit.
				1				VRH1[4:0]					00h	VREG1OUT level control
				1				VRH2[4:0]					00h	VREG2OUT level control
				1				REG PD		BT[2:0]			05h	REGPD – Regulator Power Down BT – VGH/VGL level control
				1		VBS[2:0]			VREF[3:0]				0Bh	VBS – Set the VBIAS level. VREF – Set the reference voltage of DDVDH.
PWRCTL5	C5h	1	R/W	0										Power Control 5 (Vcom Control)
				1		VCM[6:0]							00h	VCM – Vcom level control
PWRCTL6	C6h	3	R/W	0										Power Control 6 (VDD Regulator Control)

				1		RI[2:0]				RV[2:0]			23h	RI – VDD current control RV – VDD voltage control
				1		RSET[2:0]				RCONT[2:0]			40h	RCONT – Main bias voltage control RSET – Main bias current control
OFCCTL	C7h	3	R/W	0										Source Channel Amp Offset Cancelling control
				1								OFCEN	00h	OFCEN – Offset canceling enable
				1	OFCTSW[7:0]								30h	OFCTSW – Offset sampling time control [1..255]
				1	OFCTD2[3:0]				OFCTD1[3:0]				10h	OFCTD1 – Offset sampling time delay [0..15] OFCTD2 – Offset canceling time delay [0..15]
BLCTL	C8h	2	R/W	0										Backlight Control
				1	CDSP[3:0]				CDMP[3:0]				82h	CDSP – dimming control of still picture CDMP – dimming control of moving picture
				1	PWMP						FPWM[1:0]		01h	PWMP - PWM polarity. 0: active H, 1: active L FPWM - PWM frequency setting
RGAMMAP	D0h	9	R/W	0										Set Positive Gamma Curve for Red
				1		PKP1[2:0]				PKP0[2:0]			00h	
				1		PKP3[2:0]				PKP2[2:0]			00h	
				1		PKP5[2:0]				PKP4[2:0]			00h	
				1		PRP1[2:0]				PRP0[2:0]			00h	
				1				VRP0[4:0]					00h	
				1				VRP1[4:0]					00h	
				1		PFP1[2:0]				PFP0[2:0]			00h	
				1		PFP3[2:0]				PFP2[2:0]			00h	
				1				PMP[2:0]					00h	
RGAMMAN	D1h	9	R/W	0										Set Negative Gamma Curve for Red
				1		PKN1[2:0]				PKN0[2:0]			00h	
				1		PKN3[2:0]				PKN2[2:0]			00h	
				1		PKN5[2:0]				PKN4[2:0]			00h	
				1		PRN1[2:0]				PRN0[2:0]			00h	
				1				VRN0[4:0]					00h	
				1				VRN1[4:0]					00h	
				1		PFN1[2:0]				PFN0[2:0]			00h	
				1		PFN3[2:0]				PFN2[2:0]			00h	
				1				PMN[2:0]					00h	
GGAMMAP	D2h	9	R/W	0										Set Positive Gamma Curve for Green
				1		PKP1[2:0]				PKP0[2:0]			00h	
				1		PKP3[2:0]				PKP2[2:0]			00h	
				1		PKP5[2:0]				PKP4[2:0]			00h	
				1		PRP1[2:0]				PRP0[2:0]			00h	

				1				VRP0[4:0]		00h		
				1				VRP1[4:0]		00h		
				1		PFP1[2:0]		PFP0[2:0]		00h		
				1		PFP3[2:0]		PFP2[2:0]		00h		
				1				PMP[2:0]		00h		
GGAMMAN	D3h	9	R/W	0								Set Negative Gamma Curve for Green
				1		PKN1[2:0]		PKN0[2:0]		00h		
				1		PKN3[2:0]		PKN2[2:0]		00h		
				1		PKN5[2:0]		PKN4[2:0]		00h		
				1		PRN1[2:0]		PRN0[2:0]		00h		
				1				VRN0[4:0]		00h		
				1				VRN1[4:0]		00h		
				1		PFN1[2:0]		PFN0[2:0]		00h		
				1		PFN3[2:0]		PFN2[2:0]		00h		
				1				PMN[2:0]		00h		
BGAMMAP	D4h	9	R/W	0								Set Positive Gamma Curve for Blue
				1		PKP1[2:0]		PKP0[2:0]		00h		
				1		PKP3[2:0]		PKP2[2:0]		00h		
				1		PKP5[2:0]		PKP4[2:0]		00h		
				1		PRP1[2:0]		PRP0[2:0]		00h		
				1				VRP0[4:0]		00h		
				1				VRP1[4:0]		00h		
				1		PFP1[2:0]		PFP0[2:0]		00h		
				1		PFP3[2:0]		PFP2[2:0]		00h		
				1				PMP[2:0]		00h		
BGAMMAN	D5h	9	R/W	0								Set Negative Gamma Curve for Blue
				1		PKN1[2:0]		PKN0[2:0]		00h		
				1		PKN3[2:0]		PKN2[2:0]		00h		
				1		PKN5[2:0]		PKN4[2:0]		00h		
				1		PRN1[2:0]		PRN0[2:0]		00h		
				1				VRN0[4:0]		00h		
				1				VRN1[4:0]		00h		
				1		PFN1[2:0]		PFN0[2:0]		00h		
				1		PFN3[2:0]		PFN2[2:0]		00h		
				1				PMN[2:0]		00h		

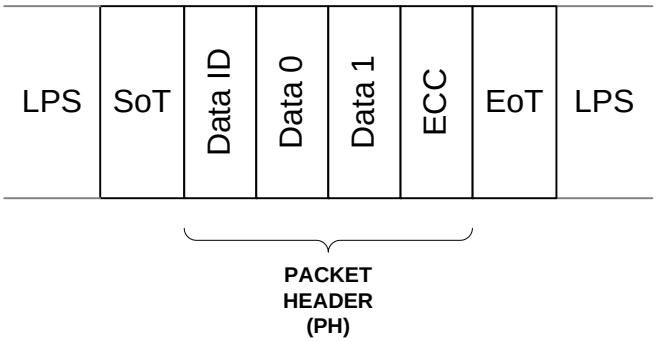
MDDI	E0h	6	R/W	0															MDDI interface Control
				1		REF[2:0]											LPM	30h	REF – LPM=1: Low power mode enabled LPM=0: Normal mode
				1										TXEMP[1:0]			TXEN	03h	TXEMP - 00 : Normal Operation Mode (2 ㎃) - 01, 10 : Overdrive Mode (2.5 ㎃) - 11 : Overdrive Mode (3 ㎃)
				1										DATA0_RESET[5:0]				00h	Set Data0 Delay Reset Value
				1										DATA1_RESET[5:0]				04h	Set Data1 Delay Reset Value
				1										DATA1_OFFSET[5:0]				02h	Set Data1 Delay Offset Value
				1										STB_RESET[5:0]				00h	Set Strobe Delay Reset Value
MEMORY	E1h	4	R/W	0															Frame Memory Control
				1												DCMR[1:0]		02h	DCMR - memory refresh clock frequency 0: 1/48, 1: 1/64, 2: 1/96, 3: 1/128 of oscillator freq
				1													ECCBYP	00h	ECCBYP – Bypass ECC
				1										SS[2:0]				02h	SS - LCD clock frequency selection
				1										OPT [4:0]				00h	OPT – Programmable options
EEPROM	E2h	1	R/W	0															
				1		RFCLK[3:0]											EEPROM	00h	RFCLK - I2C clock frequency [0..12] = (oscillator frequency)/ (16 – RFCLK) EEPROM – 1: external EEPROM can be read, 0: external EEPROM cannot be read.
TEST1	F0h	1	W	0															Test Register 1
				1	HIZ											TPOL[1:0]		00h	HIZ – VLOUT3 and VLOUT4 outputs to Hi-Z TPOL – LCD polarity inversion control
TEST2	F1h	1	W	0															Memory BIST Control
				1										BALG[2:0]				00h	BALG - BIST algorithm
				2	ERRTHR[7:0]													80h	ERRTHR - Error count threshold
				3	MDRT[7:0]													00h	MDRT - Memory data retention time
OTP1	F8h	3	W	0															
				1	PTM[1:0]								PRD	PWE	VPP	PPROG		00h	PTM – Pins for enabling test mode PWE – Write enable PPROG – Program mode enable PRD – Read enable VPP – Power control switch
				1	APRG										PA[1:0]			00h	APRG – enable automatic program address decision ignoring register PA PA – Write address
				1	PDIN[7:0]													00h	PDIN – Data input
OTP2	F9h	1	W	0															OTP Control 2
				1	VCMSEL[1:0]										RA[1:0]			00h	VCMSEL – Set Vcom level from either the register C5h or the OTP. RA – Read address
OTP3	FAh	4	R	0															OTP Control 3
				1	PDOUT[7:0]													xxh	PDOUT – OTP Read Data output
				1	PDOUT[15:8]													xxh	

				1	PDOUT[23:16]	xxh	
				1	PDOUT[31:24]	xxh	

Special Command Set for MIPI DSI Configuration

Data 0	Data 1								Default
	b7	b6	b5	b4	b3	b2	b1	b0	
01h	NO_BTA	MODE	-	HRX_FREQ	LTX_CLK	LTX_CTL	LTX_FREQ[1:0]		07h
02h								IGN_CERR	00h
03h	HRX_TO[7:0]								80h
04h	LTX_TO[7:0]								C0h

Note : This special command set for MIPI DSI configuration can only be set by DSI Generic Short Write with 2 parameters. The DSI generic short write with 2 parameters packet form is as follows as shown earlier in MIPI DSI introduction page.



The descriptions for the above parameters are as follows.

Parameter Name	Description
NO_BTA	BTA (Bus Turn Around) disable (default : 0) 0 : enable, 1 : disable
MODE	DSI operation mode (default : 0) 0 : command mode, 1 : video mode This only applicable to frame memory inside IC such as LG4572B.
HRX_FREQ	HS-RX frequency (default 0) Write this, if needed, using LPDT prior to any HS-TX. This is used to detect HS SoT and EoT sequences 0 : 2.5ns ≤ UI < 4ns, 1 : 4ns ≤ UI ≤ 6ns
LTX_CLK	Selects LP-TX clock source (default : 0) 0 : HS-RX clock, 1 : Pin PCLK
LTX_CTL	LP-TX drivability control (default : 1) 0 : low drivability for C_{Load} < 5pF, 1 : normal drivability
LTX_FREQ [1:0]	LP-TX frequency (default : 11b) 00 : LP-TX clock = 1/4 of HS-RX DDR clock 01 : LP-TX clock = 1/6 of HS-RX DDR clock 10 : LP-TX clock = 1/8 of HS-RX DDR clock 11 : LP-TX clock = 1/12 of HS-RX DDR clock
IGN_CERR	Ignore checksum error on the Null packet and the blanking packet. (default : 0) 0 : checksum error ignored, 1 : checksum error cared. This bit is to support Intel specific item (#9).

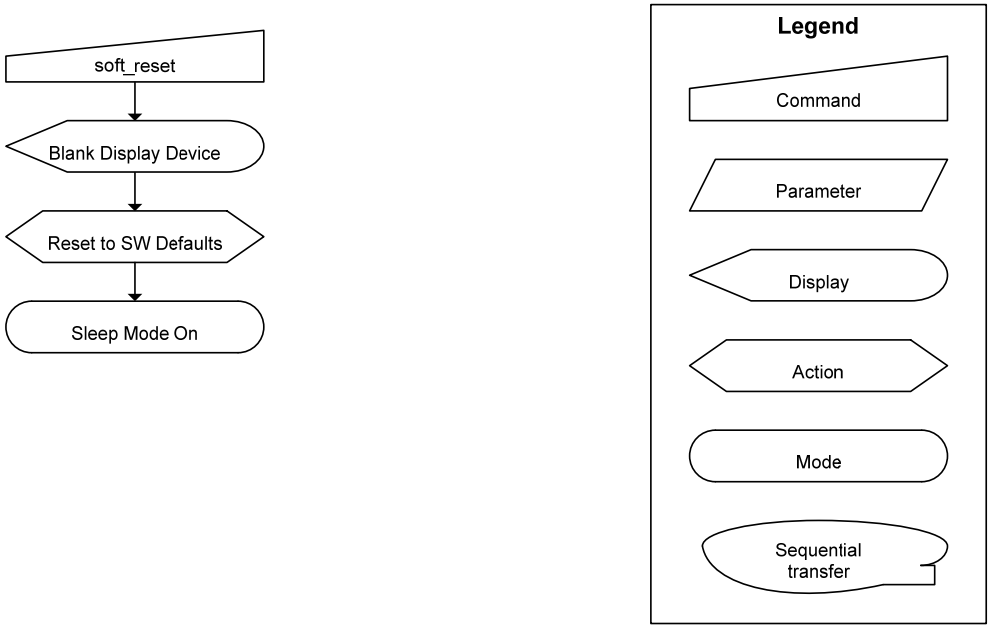
HRX_TO[7:0]	HS-RX timeout value in 16*RxByteClkHS (default : 80h) RxByteClkHS is a byte clock after multi-lane merge.
LTX_TO[7:0]	LP-TX timeout value in 16*TxClkEsc (default : C0h)

6.2 Command Description

6.2.1 00h – No Operation

00h	No Operation												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	0	0	0	0	0	0	0	0	-
Parameter	None												
Description	This command is an empty command; it does not have any effect on the display module. However, it can be used to terminate Memory Write, Memory Read, Memory Write Continue or Memory Read Continue as described in RAMWR (Memory Write), RAMRD (Memory Read), RAMWRC (Memory Write Continue) and RAMRDC (Memory Read Continue) Commands.												
Restriction	-												
Flow Chart	-												

6.2.2 01h – Software Reset

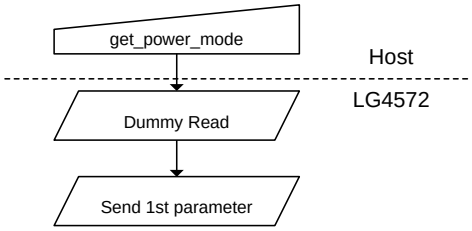
01h	Software Reset												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	0	0	0	0	0	0	0	1	-
Parameter	None												
Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their default values. The display is blank immediately.												
Restriction	If a soft_reset is sent when the display module is in Sleep Mode, the host processor must wait 120 milliseconds before sending an exit_sleep_mode command. Soft_reset should not be sent during exit_sleep_mode sequence. No new command setting is allowed until the LG4572B enters the Sleep Mode. See "Display ON/OFF Sequence" for sequence to enter Sleep Mode. If a soft_reset is sent when the display module is in Sleep Mode, data in NVM are read. No new command setting is inhibited when data are read (5ms).												
Flow Chart													

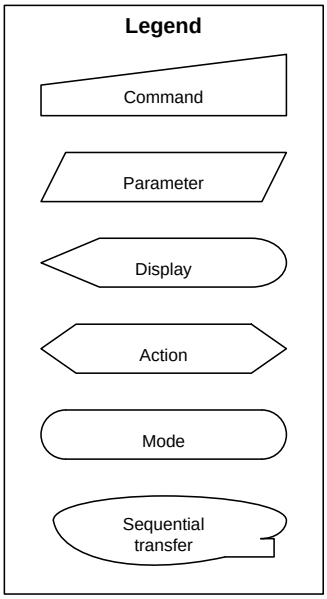
6.2.3 0Ah – Read Display Power Mode

<table>
<tr><td>0Ah</td><td colspan="13">Read Display Power Mode</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D [23:8]</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Reset</td></tr>
<tr><td>command</td><td>0</td><td>1</td><td>↑</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0Ah</td></tr>
<tr><td>Parameter</td><td>1</td><td>↑</td><td>1</td><td>X</td><td>0</td><td>~~IDM~~</td><td>PTL</td><td>nSLP</td><td>NOR</td><td>DISP</td><td>0</td><td>0</td><td>08h</td></tr>
<tr><td>Description</td><td colspan="13">This command indicates the current status of the display as described below:
<table>
<tr><th>Bit</th><th>Description</th><th>Comment</th><th>Command list Symbol</th></tr>
<tr><td>D6</td><td>~~Idle Mode On/Off~~</td><td></td><td>~~IDM~~</td></tr>
<tr><td>D5</td><td>Partial Mode On/Off</td><td></td><td>PTL</td></tr>
<tr><td>D4</td><td>Sleep Mode On/Off</td><td></td><td>nSLP</td></tr>
<tr><td>D3</td><td>Display Normal Mode On/Off</td><td></td><td>NOR</td></tr>
<tr><td>D2</td><td>Display On/Off</td><td></td><td>DISP</td></tr>
</table>

~~Bit D6 – Idle Mode On/Off~~
~~'0' = Idle Mode Off~~
~~'1' = Idle Mode On~~
Bit D5 – Partial Mode On/Off
'0' = Partial Mode Off
'1' = Partial Mode On
Bit D4 – Sleep Mode
'0' = Sleep Mode On
'1' = Sleep Mode Off
Bit D3 – Display Normal Mode On/Off
'0' = Display Normal Mode Off
'1' = Display Normal Mode On
Bit D2 – Display On/Off
'0' = Display Off
'1' = Display On
</td></tr>
<tr><td>Restriction</td><td colspan="13">-</td></tr>
</table>

Flow Chart


get_power_mode
Host
LG4572
Dummy Read
Send 1st parameter


Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.4 0Bh – Read Display MADCTL

0Bh	Read Display MADCTL												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	0	0	0	0	1	0	1	1	0Bh
Parameter	1	↑	1	X	MY	MX	MV	0	BGR	0	~~FH~~	FV	00h

Description

This command indicates the current status of the display as described below:

Bit	Description	Comment	Command list Symbol
D7	Page Address Order		MY
D6	Column Address Order		MX
D5	Page/Column Order		MV
D3	RGB/BGR Order		BGR
~~D1~~	~~Flip Horizontal~~		~~FH~~
D0	Flip Vertical		FV

- Bit D7 – Page Address Order
  '0' = Top to Bottom (When set_address_mode D7= '0')
  '1' = Bottom to Top (When set_address_mode D7= '1')

- Bit D6 – Column Address Order
  '0' = Left to Right (When set_address_mode D6= '0')
  '1' = Right to Left (When set_address_mode D6= '1')

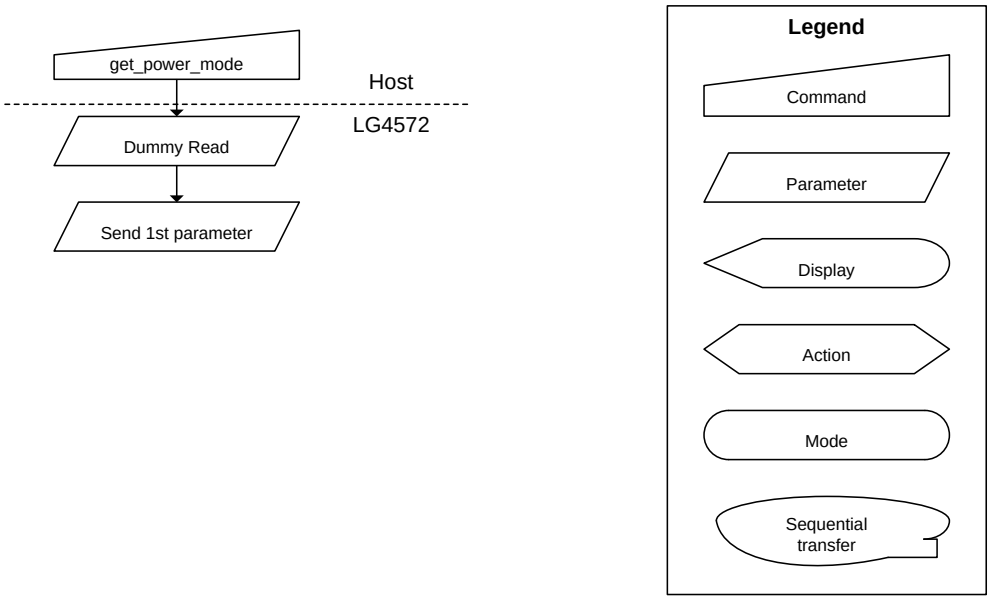
- Bit D5 – Page/Column Order
  '0' = Normal Mode (When set_address_mode D5= '0')
  '1' = Reverse Mode (When set_address_mode D5= '1')

- Bit D3 – RGB/BGR Order
  '0' = Pixel in RGB order (When set_address_mode D3= '0')
  '1' = Pixel in BGR order (When set_address_mode D3= '1')

- Bit D1 – Flip Horizontal
  '0' = Normal (When set_address_mode D1= '0')
  '1' = Flip (When set_address_mode D1= '1')

- Bit D0 – Flip Vertical
  '0' = Normal (When set_address_mode D0= '0')
  '1' = Flip (When set_address_mode D0= '1')

X = Don't care

Restriction	-
Flow Chart	

6.2.5 0Ch – Read Display Pixel Format

0Ch	Read Display Pixel Format												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	0	0	0	0	1	1	0	0	0Ch
Parameter	1	↑	1	X	0	DPIPF[2:0]			0	DBIPF[2:0]			77h

Description

This command indicates the current status of the display as described below:

Bit	Description	Comment	Command list Symbol
D6	DPIPF (RGB Interface Color Format)		
D5			
D4			
D2	DBIPF (System Interface Color Format)		
D1			
D0			

- Bit D[6:4] – DPI Pixel Format (RGB Interface Color Format Selection)
- Bit D[2:0] – DBI Pixel Format(System Interface Color Format Selection)

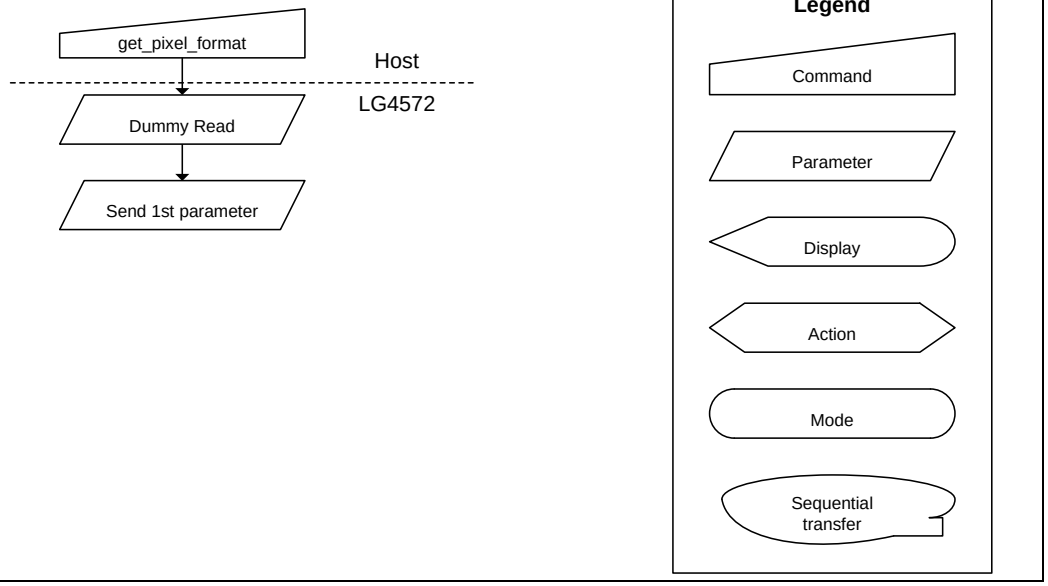
See description of command set_pixel_format(3Ah).

Control Interface Color Format	D6/D2	D5/D1	D4/D0
Setting disabled	0	0	0
Setting disabled	0	0	1
Setting disabled	0	1	0
Setting disabled	0	1	1
Setting disabled	1	0	0
16bit/pixel (65k colors)	1	0	1
18bit/pixel (262k colors)	1	1	0
24bit/pixel (16M clors)	1	1	1

X = Don't care

Restriction -

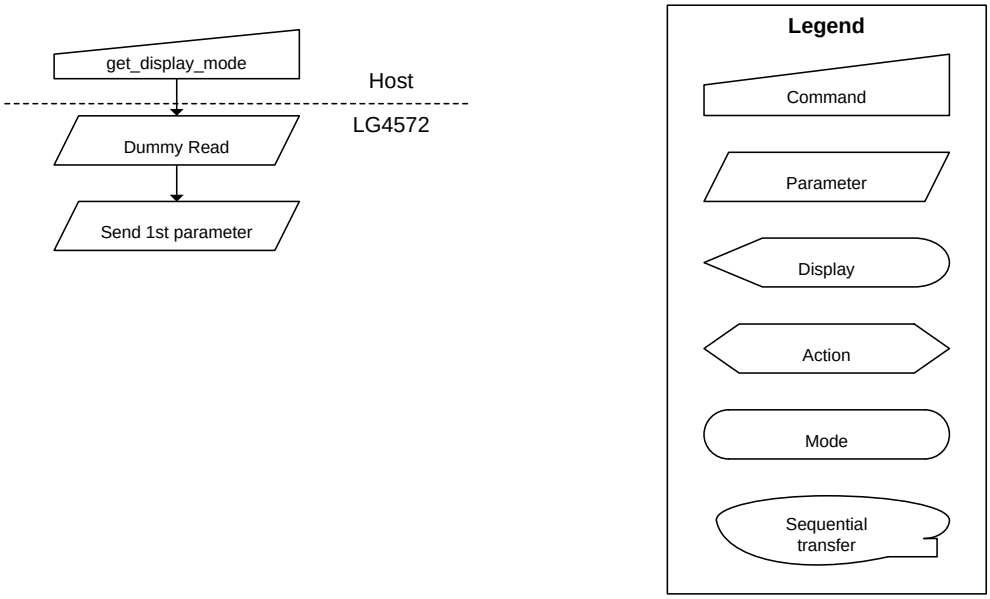
Flow Chart


get_pixel_format
Host
LG4572
Dummy Read
Send 1st parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.6 0Dh – Read Display Image Mode

<table>
<tr><td>0Dh</td><td colspan="13">Read Display Image Mode</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D [23:8]</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Reset</td></tr>
<tr><td>command</td><td>0</td><td>1</td><td>↑</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0Dh</td></tr>
<tr><td>Parameter</td><td>1</td><td>↑</td><td>1</td><td>X</td><td>0</td><td>0</td><td>INV</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="13">The display module returns the current status of the display as described in the table below.

<table><tr><th>Bit</th><th>Description</th><th>Comment</th><th>Command list Symbol</th></tr><tr><td>D5</td><td>Inversion On/Off</td><td></td><td>INV</td></tr></table>
• ‘Bit D5 – Inversion On/Off
‘0’ = Inversion Off
‘1’ = Inversion On

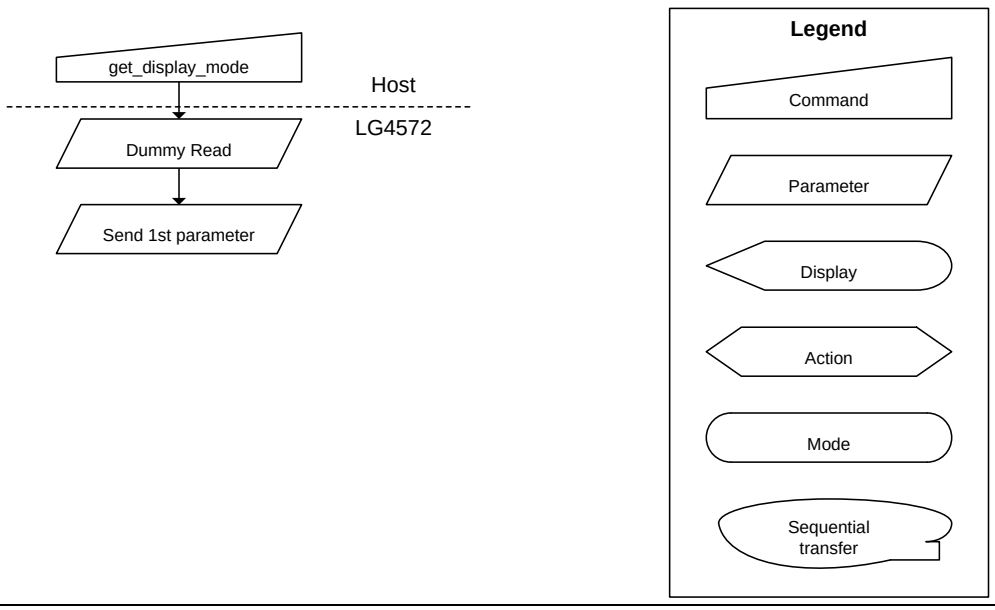
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">-</td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

6.2.7 0Dh – Read Display Image Mode

<table>
<tr><td>0Dh</td><td colspan="13">Read Display Image Mode</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D [23:8]</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Reset</td></tr>
<tr><td>command</td><td>0</td><td>1</td><td>↑</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0Dh</td></tr>
<tr><td>Parameter</td><td>1</td><td>↑</td><td>1</td><td>X</td><td>0</td><td>0</td><td>INV</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="13">The display module returns the current status of the display as described in the table below.

<table>
<tr><th>Bit</th><th>Description</th><th></th><th>Comment</th><th>Command list Symbol</th></tr>
<tr><td>D5</td><td>Inversion On/Off</td><td></td><td></td><td>INV</td></tr>
</table>

• ‘Bit D5 – Inversion On/Off
‘0’ = Inversion Off
‘1’ = Inversion On

X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">-</td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

6.2.8 0Eh – Read Display Signal Mode

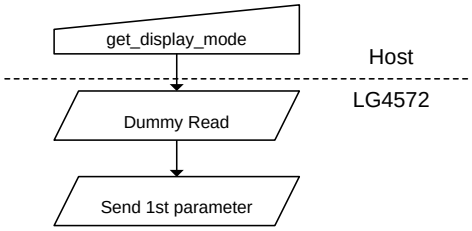
<table>
<tr><td>0Eh</td><td colspan="13">Read Display Signal Mode</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D [23:8]</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Reset</td></tr>
<tr><td>command</td><td>0</td><td>1</td><td>↑</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0Eh</td></tr>
<tr><td>Parameter</td><td>1</td><td>↑</td><td>1</td><td>X</td><td>TE</td><td>TEM</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="13">The display module returns the current status of the display as described in the table below.

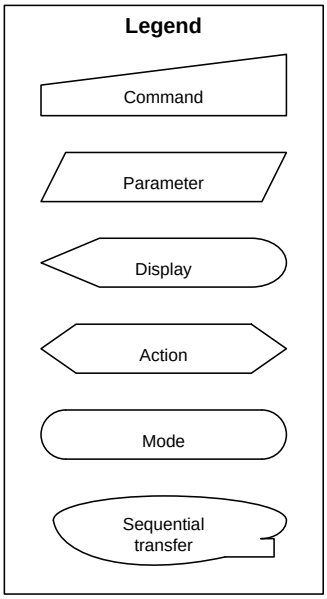
<table><tr><th>Bit</th><th>Description</th><th>Comment</th><th>Command list Symbol</th></tr><tr><td>D7</td><td>Tearing Effect line On/Off</td><td></td><td>TE</td></tr><tr><td>D6</td><td>Tearing Effect line Output Mode</td><td></td><td>TEM</td></tr></table>
• ‘Bit D7 – Tearing Effect Line On/Off
‘0’ = Tearing Effect line Off
‘1’ = Tearing Effect On

• Bit D6 – Tearing Effect Line Output Mode
‘0’ = Mode 1
‘1’ = Mode 2

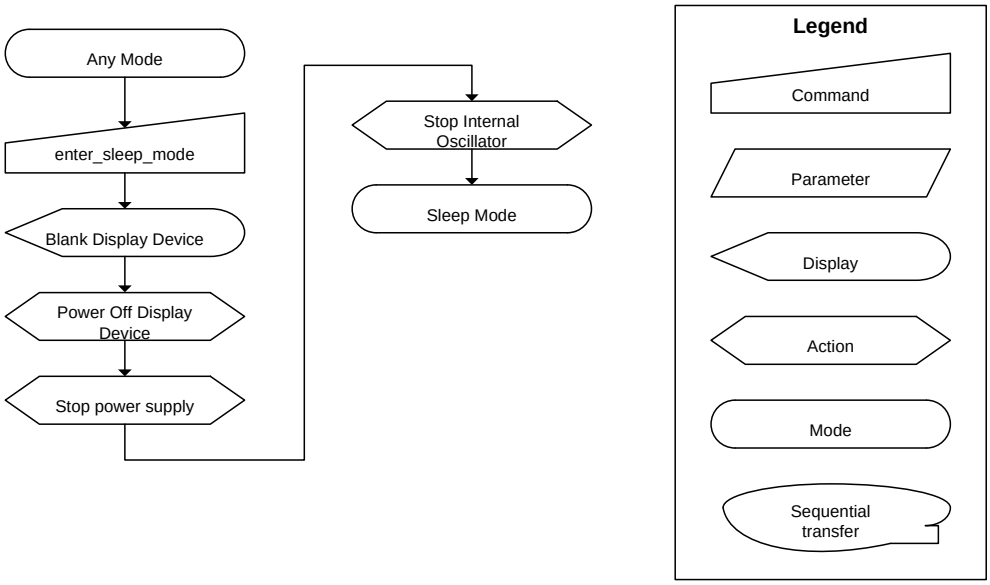
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">-</td></tr>
</table>

Flow Chart

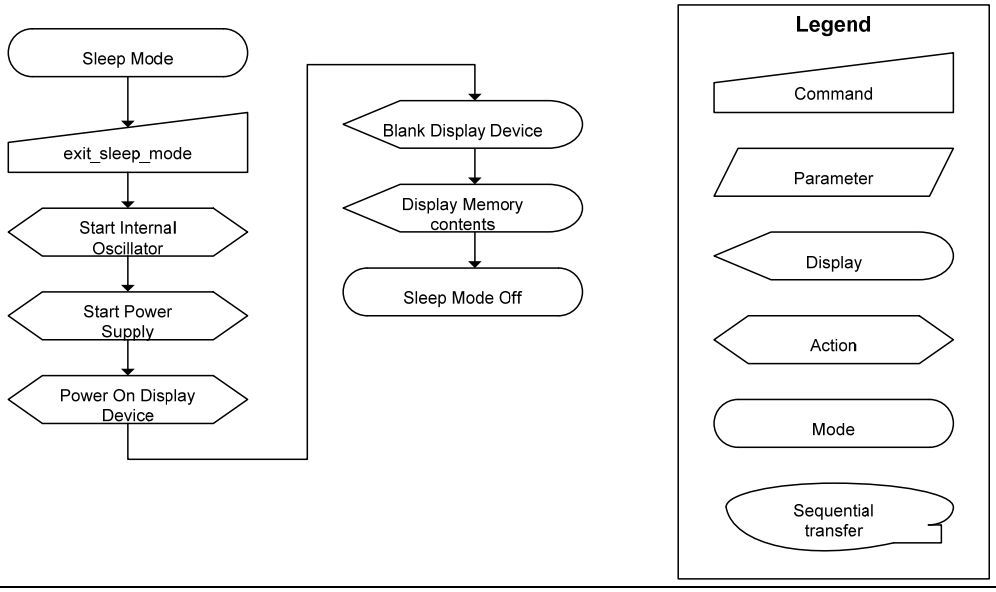

get_display_mode
Host
LG4572
Dummy Read
Send 1st parameter


Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.9 10h – Sleep In

10h	Sleep In												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	0	0	0	1	0	0	0	0	10h
Parameter	None												
Description	This command causes the display module to enter the minimum power consumption mode. In this mode e.g. the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped. Host interface and memory are still working and the memory can or cannot keep its contents. Backlights, display and keyboard, are off. Dimming function does not work when there is changing mode from Sleep Out to Sleep In.												
Restriction	This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.												
Flow Chart													

6.2.10 11h – Sleep Out

11h	Sleep Out												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	0	0	0	1	0	0	0	1	11h
Parameter	None												
Description	This command turns off sleep mode. In this mode e.g. the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.												
Restriction	This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h), SW Reset Command (01h) or HW Reset. It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. The display module loads all display supplier's factory default values to the registers during this time and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out mode. The display module is doing self-diagnostic functions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.												
Flow Chart													

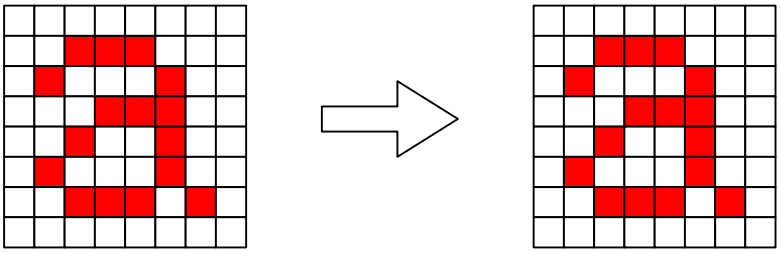
6.2.11 12h – Partial Mode On

12h	Partial Mode On												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	0	0	0	1	0	0	1	0	12h
Parameter	None												
Description	This command causes the LCD module to enter the Partial mode. The Partial Display Mode window is described by the set_partial_area command (30h). To leave Partial Display Mode, the enter_normal_mode (13h) should be written.												
Restriction	This command has no effect when Partial mode is active.												
Flow Chart	See flow chart of command set_partial_area(30h).												

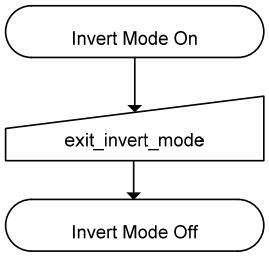
6.2.12 13h – Normal Display Mode On

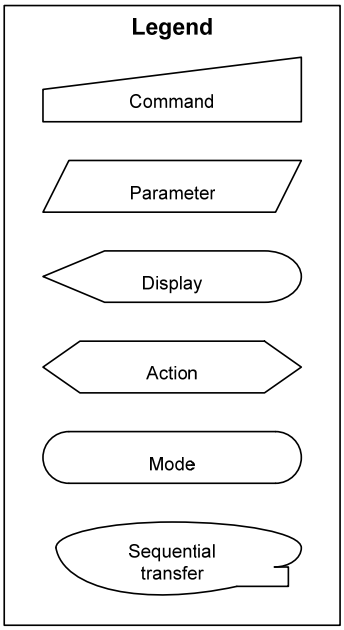
13h	Normal Display Mode On												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	0	0	0	1	0	0	1	1	13h
Parameter	None												
Description	This command returns the display to normal mode. Normal display mode on means Partial mode off. Note : When a command breaks in the middle of frame period in Partial mode, that command becomes valid from the next frame period.												
Restriction	This command has no effect when Normal mode is already active.												
Flow Chart	See flow chart of command set_partial_area(30h).												

6.2.13 20h – Display Inversion Off

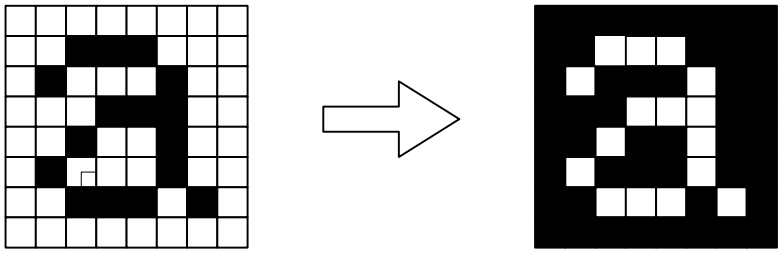
20h	Display Inversion Off												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	0	0	1	0	0	0	0	0	20h
Parameter	None												
Description	This command is used to recover from display inversion mode. This command makes no change of contents of frame memory. This command does not change any other status. (Example) Memory display  X = Don't care												
Restriction	This command has no effect when the module is already in Inversion Off.												

Flow Chart

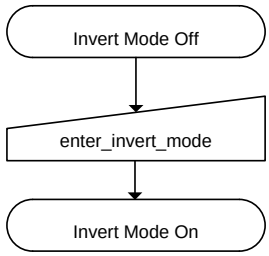

Invert Mode On
exit_invert_mode
Invert Mode Off

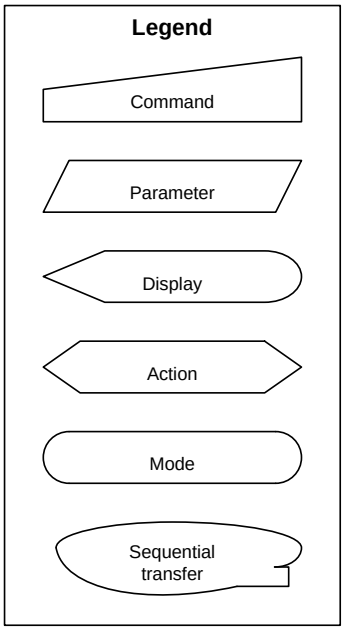

Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.14 21h – Display Inversion On

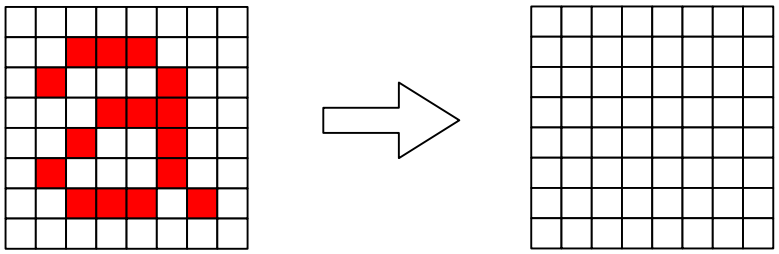
21h	Display Inversion On												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	0	0	1	0	0	0	0	1	21h
Parameter	None												
Description	This command is used to enter into display inversion mode. This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display. This command does not change any other status. (Example) Memory display  X = Don't care												
Restriction	This command has no effect when the display module is already inverting the display image.												

Flow Chart

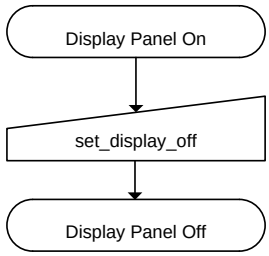

Invert Mode Off
enter_invert_mode
Invert Mode On

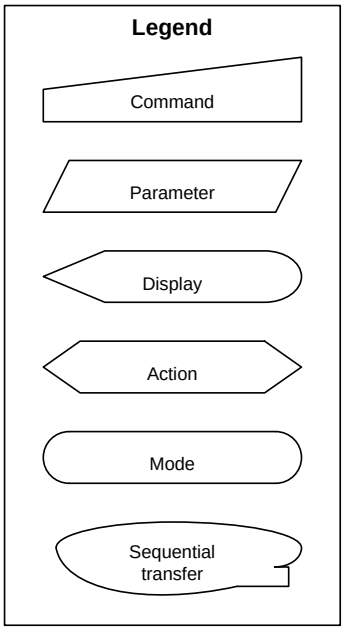

Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.15 28h – Display Off

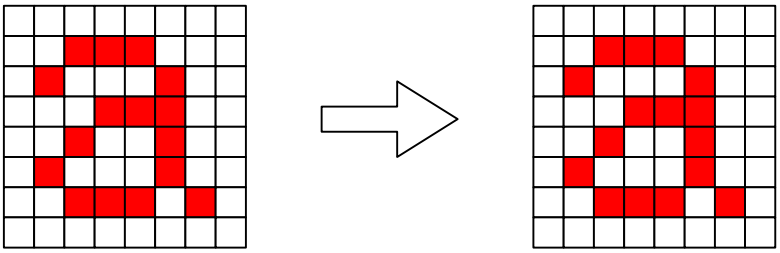
28h	Display off												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	0	0	1	0	1	0	0	0	28h
Parameter	None												
Description	This command is used to enter into Display Off mode. In this mode, the output from frame memory is disabled and either normal white or normal black display will be made. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display. (Example) Memory display  X = Don't care												
Restriction	This command has no effect when the display panel is already off.												

Flow Chart

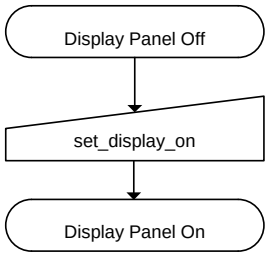

Display Panel On
set_display_off
Display Panel Off

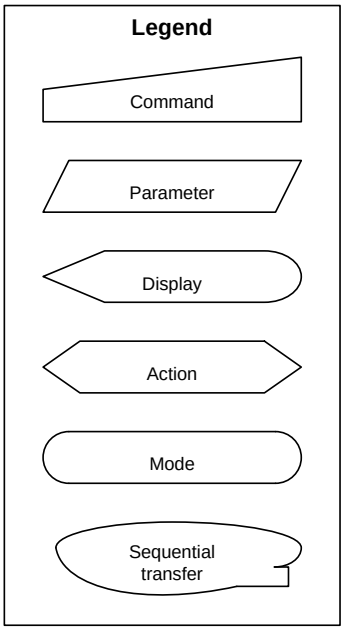

Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.16 29h – Display On

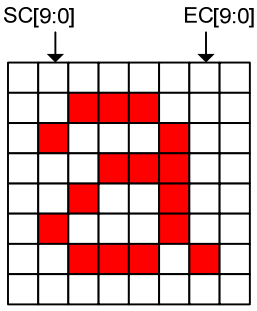
29h	Display on												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	0	0	1	0	1	0	0	1	29h
Parameter	None												
Description	This command is used to recover from Display Off mode. Output from the Frame Memory is enabled. This command makes no change of contents of frame memory. This command does not change any other status. (Example) Memory → display  X = Don't care												
Restriction	This command has no effect when module is already in display on mode.												

Flow Chart

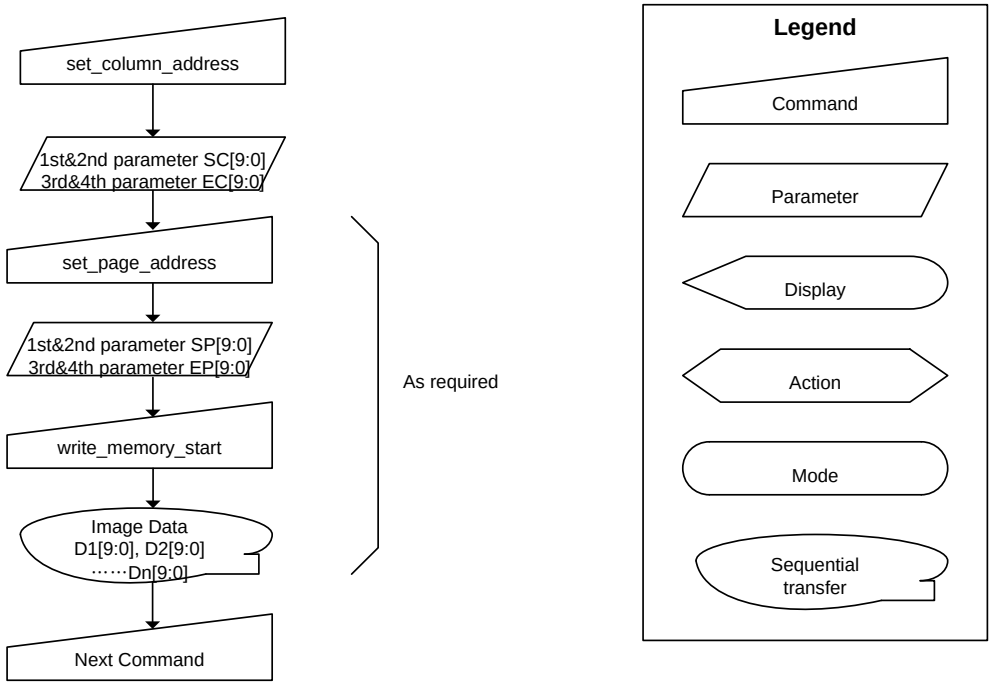

Display Panel Off
set_display_on
Display Panel On


Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

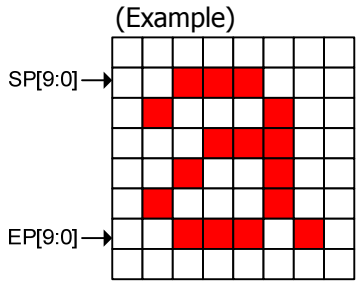
6.2.17 2Ah – Column Address Set

2Ah	Column Address Set												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	0	0	1	0	1	0	1	0	2Ah
1st parameter	1	1	↑	X	0	0	0	0	0	0	SC[9:8]		000h
2nd parameter	1	1	↑	X	SC[7:0]								
3rd parameter	1	1	↑	X	0	0	0	0	0	0	EC[9:8]		1DFh
4th parameter	1	1	↑	X	EC[7:0]								
Description	This command defines the column extent of the frame memory accessed by the host processor. The values of SC[9:0] and EC[9:0] are referred when write_memory_start (2Ch) and read_memory_start (2Eh) commands are written. No status bits are changed. (Example)  X = Don't care												
Restriction	SC [9:0] must be equal to or less than EC[9:0]. If SC[9:0] or EC[9:0] is greater than the available frame memory then the parameter is not updated. Set the 1st parameter B5 in set_address_mode (36h) in advance. Note: The parameters are disregarded in following cases. • If set_address_mode B5 = 0: SC[9:0] or EC[9:0] ≥ 1DFh • If set_address_mode B5 = 1: SC[9:0] or EC[9:0] ≥ 35Fh												

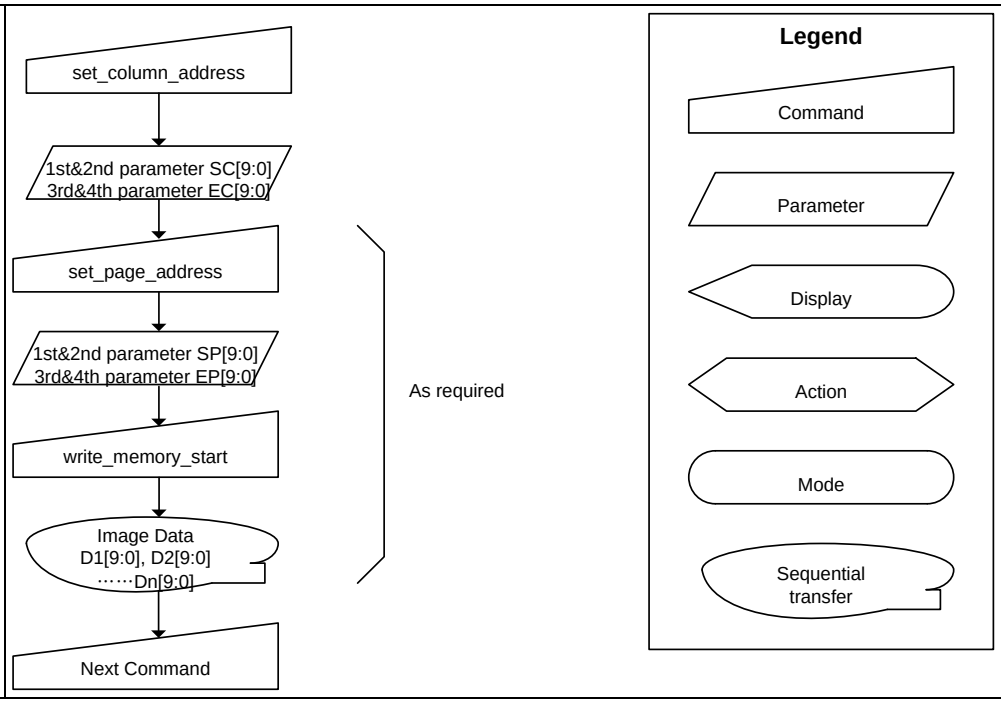
Flow Chart


set_column_address
1st&2nd parameter SC[9:0]
3rd&4th parameter EC[9:0]
set_page_address
1st&2nd parameter SP[9:0]
3rd&4th parameter EP[9:0]
write_memory_start
Image Data
D1[9:0], D2[9:0]
·····Dn[9:0]
Next Command
As required
Legend
Command
Parameter
Display
Action
Mode
Sequential
transfer

6.2.18 2Bh – Page Address Set

2Bh	Page Address Set												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	0	0	1	0	1	0	1	1	2Bh
1st parameter	1	1	↑	X	0	0	0	0	0	0	SP[9:8]		000h
2nd parameter	1	1	↑	X	SP[7:0]								
3rd parameter	1	1	↑	X	0	0	0	0	0	0	EP[9:8]		35Fh
4th parameter	1	1	↑	X	EP[7:0]								
Description	This command defines the page extent of the frame memory accessed by the host processor. No status bits are changed. The values of SP[9:0] and EP[9:0] are referred when write_memory_start (2Ch) and read_memory_start (2Eh) commands are written.  X = Don't care												
Restriction	SP[9:0] must always be equal to or less than EP[9:0]. If SP[9:0] or EP[9:0] is greater than the available frame memory then the parameter is not updated. Set the 1st parameter B5 in set_address_mode (36h) in advance. Note: The parameters are disregarded in following cases. • If set_address_mode B5 = 0: SP[9:0] or EP[9:0] ≥ 35Fh • If set_address_mode B5 = 1: SP[9:0] or EP[9:0] ≥ 1DFh												

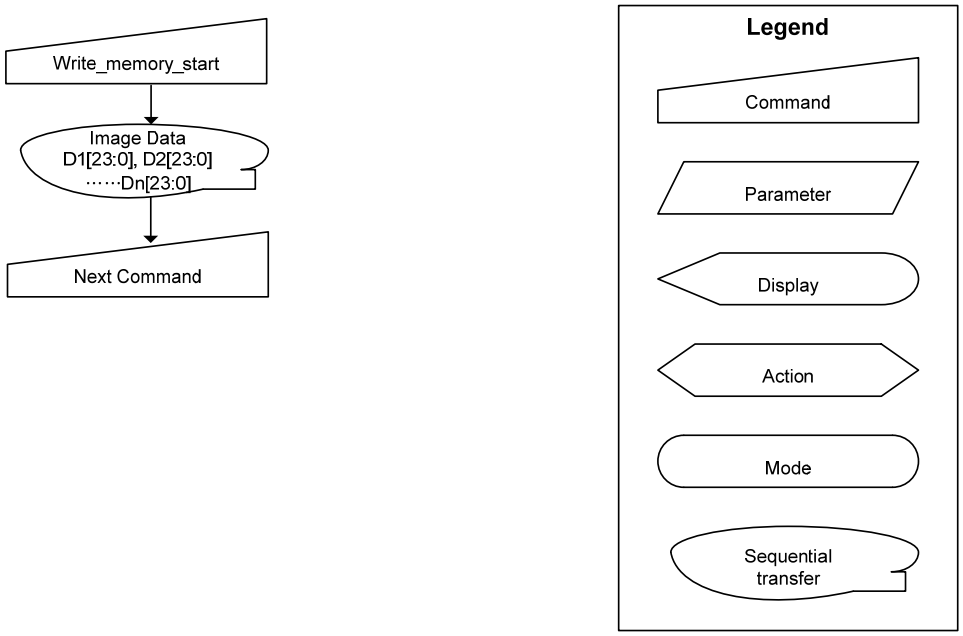
Flow Chart


set_column_address
1st&2nd parameter SC[9:0]
3rd&4th parameter EC[9:0]
set_page_address
1st&2nd parameter SP[9:0]
3rd&4th parameter EP[9:0]
write_memory_start
Image Data
D1[9:0], D2[9:0]
·····Dn[9:0]
Next Command
As required
Legend
Command
Parameter
Display
Action
Mode
Sequential
transfer

6.2.19 2Ch – Write Memory Start

2Ch	Write Memory Start												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	0	0	1	0	1	1	0	0	2Ch
1st parameter	1	1	↑	D1[23:0]									-
2nd parameter	1	1	↑	D2[23:0]									-
⋮	1	1	↑	⋮									-
Nth parameter	1	1	↑	Dn[23:0]									-
Description	This command transfers image data from the host processor to the display module's frame memory starting at the pixel location specified by preceding set_column_address and set_page_address commands. The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixel Data 1 is stored in frame memory at (SC, SP). The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are over write.												
Restriction	A write_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the write location. Otherwise, data written with write_memory_start and any following write_memory_continue commands is written to undefined locations.												

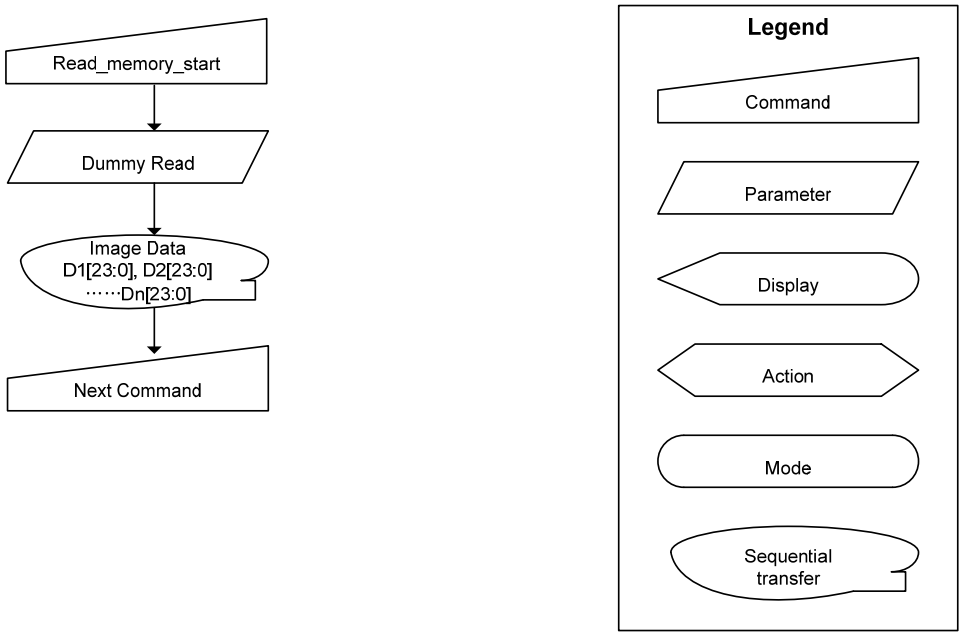
Flow Chart


Write_memory_start
Image Data
D1[23:0], D2[23:0]
……Dn[23:0]
Next Command
Legend
Command
Parameter
Display
Action
Mode
Sequential
transfer

6.2.20 2Eh – Read Memory Start

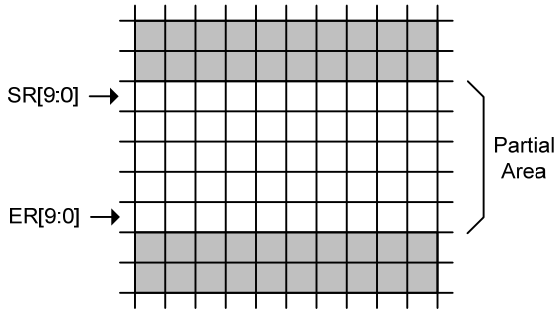
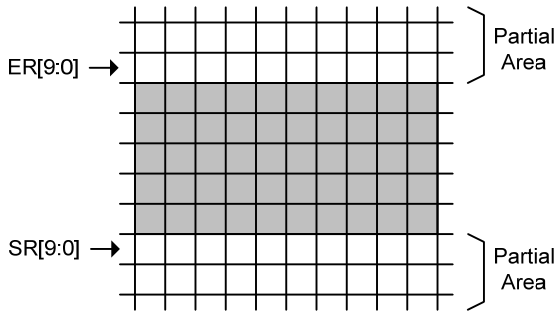
2Eh	Read Memory Start												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	0	0	1	0	1	1	1	0	2Eh
1st parameter	1	↑	1	D1[23:0]									-
2nd parameter	1	↑	1	D2[23:0]									-
⋮	1	↑	1	⋮									-
Nth parameter	1	↑	1	Dn[23:0]									-
Description	This command transfers image data from the display module's frame memory to the host processor starting at the pixel location specified by preceding set_column_address and set_page_address commands. The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The column register is then incremented and pixels read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command.												
Restriction	Regardless of the color mode set in set_pixel_format, the pixel format returned by read_memory_continue is always 24-bit so there is no restriction on the length of data.												

Flow Chart


Read_memory_start
Dummy Read
Image Data
D1[23:0], D2[23:0]
·····Dn[23:0]
Next Command
Legend
Command
Parameter
Display
Action
Mode
Sequential
transfer

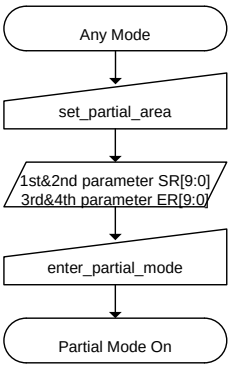
6.2.21 30h – Partial Area Definition

30h	Partial Area Definition												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	0	0	1	1	0	0	0	0	30h
1st parameter	1	1	↑	X	0	0	0	0	0	0	SR[9:8]		000h
2nd parameter	1	1	↑	X	SR[7:0]								
3rd parameter	1	1	↑	X	0	0	0	0	0	0	ER[9:8]		35Fh
4th parameter	1	1	↑	X	ER[7:0]								

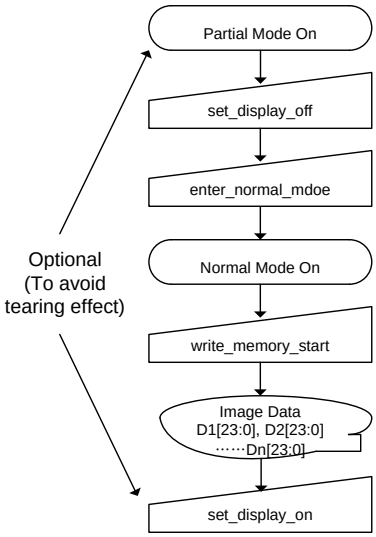
Description	This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer. End Row > Start Row  End Row < Start Row  If End Row = Start Row, the partial area will be one row deep. X = Don't care
Restriction	SR[9:0] and ER[9:0] must not be greater than 35Fh. The bits other than SR[9:0] and ER[9:0] are "Don't care".

Flow Chart

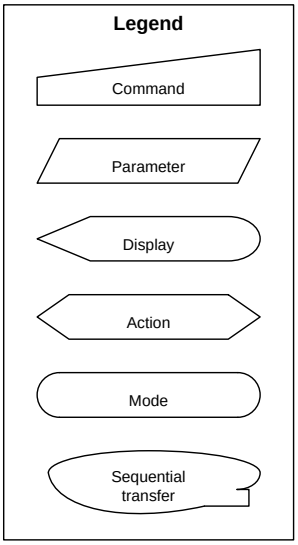
1. To enter Partial mode



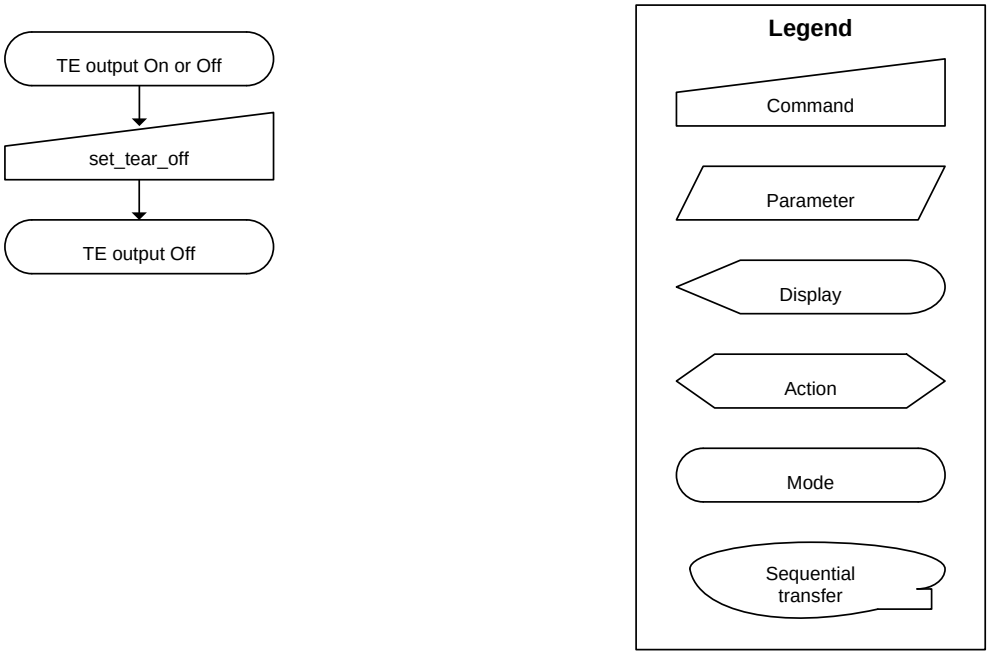
2. To exit Partial mode



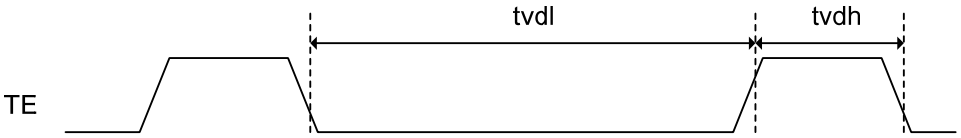
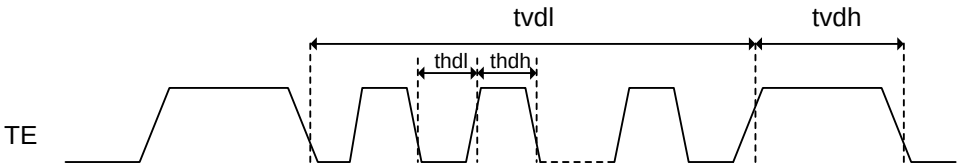
Enter Normal Mode
turns Partial Mode off



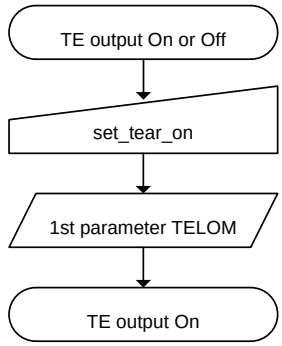
6.2.22 34h – Tearing Effect Line Off

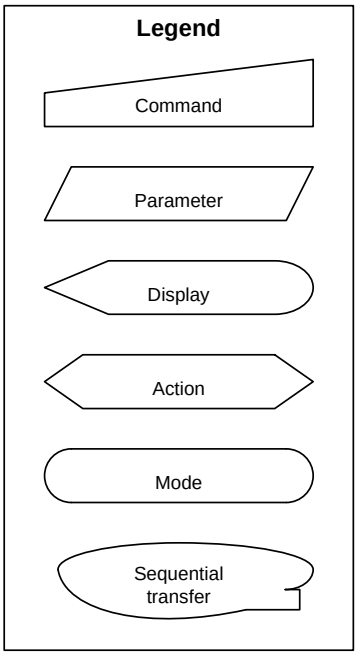
34h	Tearing Effect Line Off												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	0	0	1	1	0	1	0	0	34h
Parameter	None												
Description	This command turns off the Tearing Effect output signal from the TE signal line. X = Don't care												
Restriction	This command has no effect when Tearing Effect output is already off.												
Flow Chart													

6.2.23 35h – Tearing Effect Line On

35h	Tearing Effect Line On												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	0	0	1	1	0	1	0	1	35h
Parameter	1	1	↑	X	0	0	0	0	0	0	0	TEM	00h
Description	This command turns on the display module's Tearing Effect output signal on the TE signal line. The Tearing Effect Line On has one parameter, TE ON, that describes the Tearing Effect Output Line mode. See TE Pin Output Signal" for detail. TEM = 0: The Tearing Effect Output line consists of V-Blanking information only. The Tearing Effect Output line shall be high during vertical blanking period.  TEM = 1: The Tearing Effect Output line consists of both V-blanking and H-blanking information.  Vertical blanking period: Non-lit display period in (back porch + front porch) Note: The Tearing Effect Output line shall be active low when the display module is in Sleep mode. X = Don't care												
Restriction	This command has no effect when Tearing Effect output is already ON. Changes in parameter TEM is ENABLE from the next frame period.												

Flow Chart


TE output On or Off
set_tear_on
1st parameter TELOM
TE output On

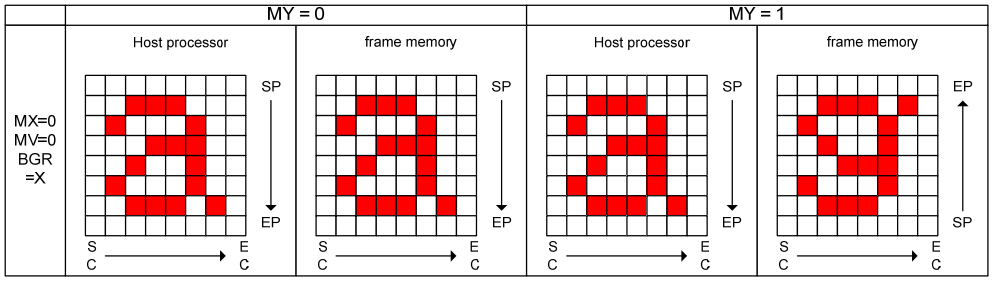

Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.24 36h – Memory Access Control

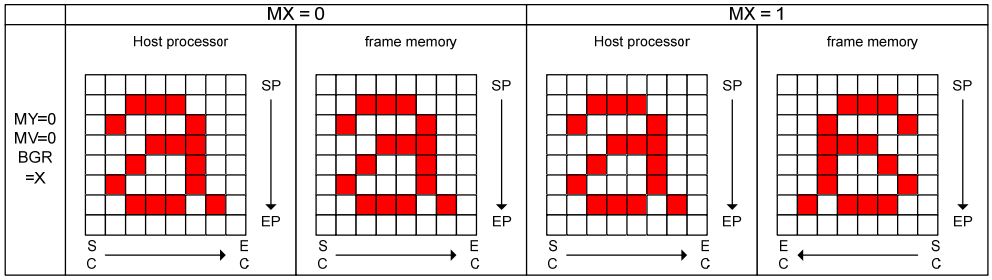
36h	Memory Access Control												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	0	0	1	1	0	1	1	0	36h
Parameter	1	1	↑	X	MY	MX	MV	0	BGR	0	FH	FV	00h
36Description	The display module returns the current power mode.												

	Description	Comment	Command list Symbol
D7	Page Address Order		MY
D6	Column Address Order		MX
D5	Page/Column Order		MV
D3	RGB/BGR Order		BGR
D1	Flip Horizontal		FH
D0	Flip Vertical		FV

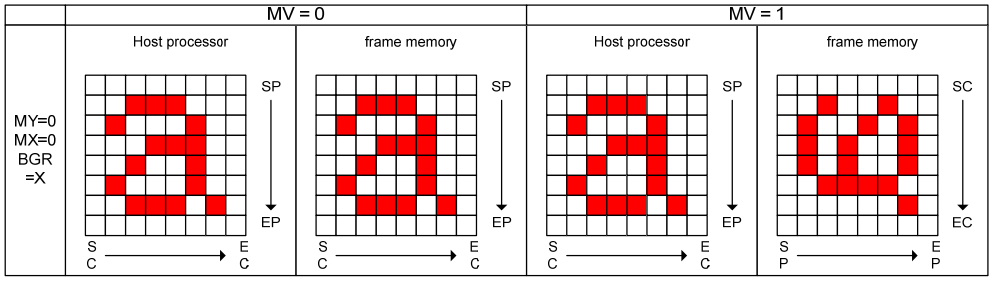
- MY – Page Address Order
  '0' = Top to Bottom
  '1' = Bottom to Top



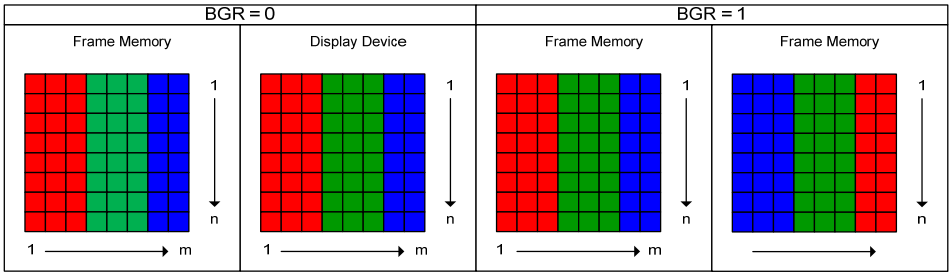
- MX – Column Address Order
  '0' = Left ro Right
  '1' = Right to Left



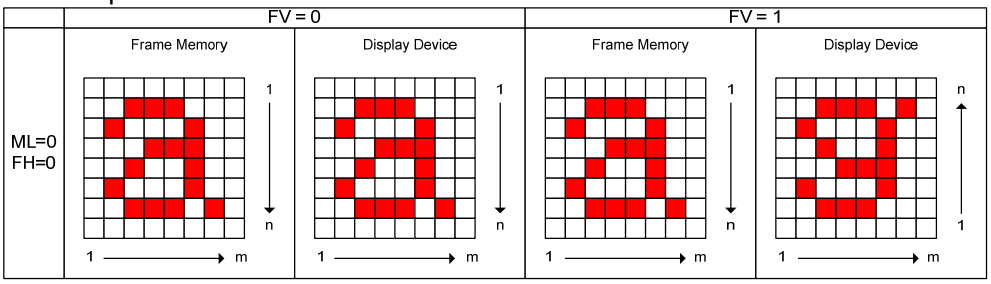
- MV – Page/Column Order
  '0' = Normal Mode
  '1' = Reverse Mode



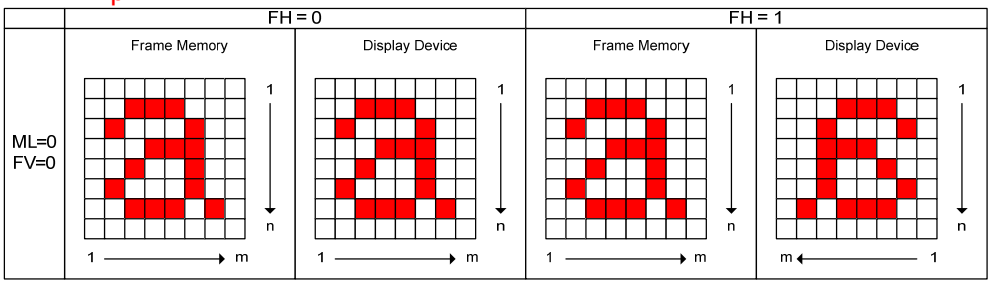
- BGR – RGB/BGR Order
  '0' = Pixel in RGB order
  '1' = Pixel in BGR order

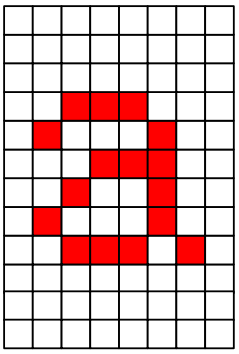
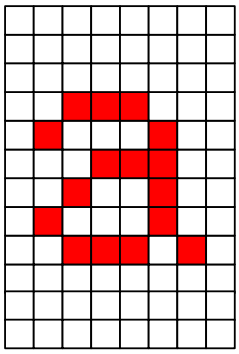
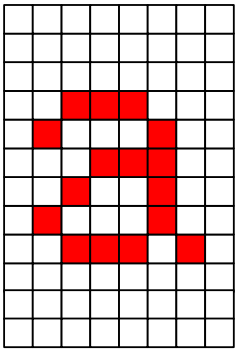
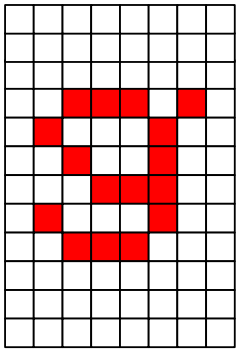
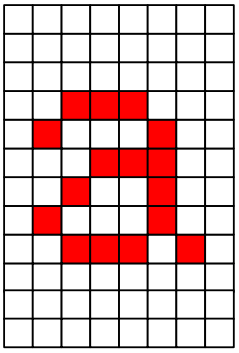
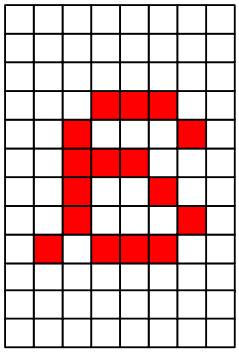


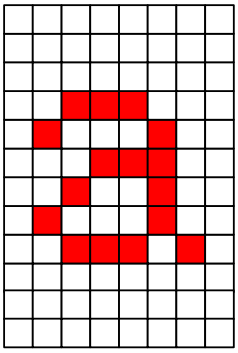
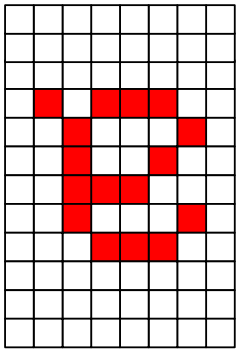
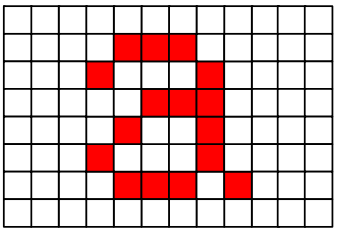
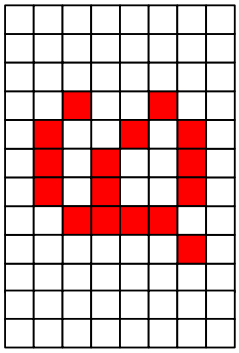
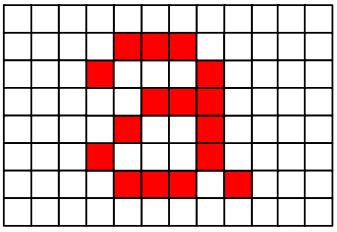
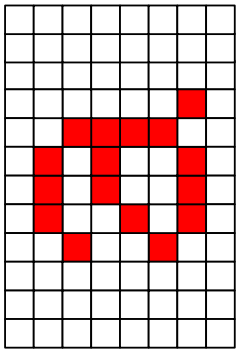
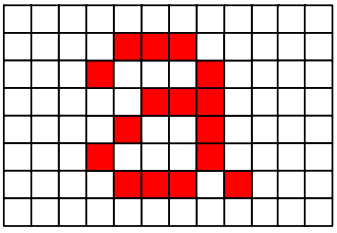
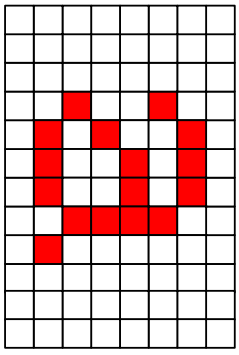
- FV – Flip Vertical
  '0' = Normal
  '1' = Flip

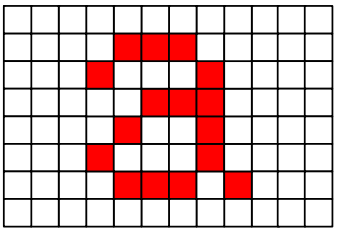
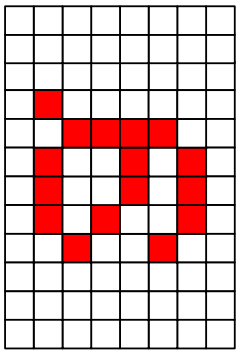
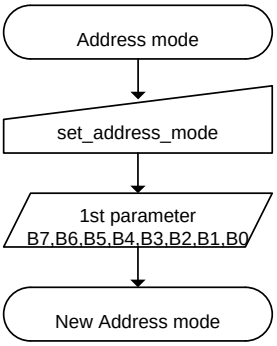
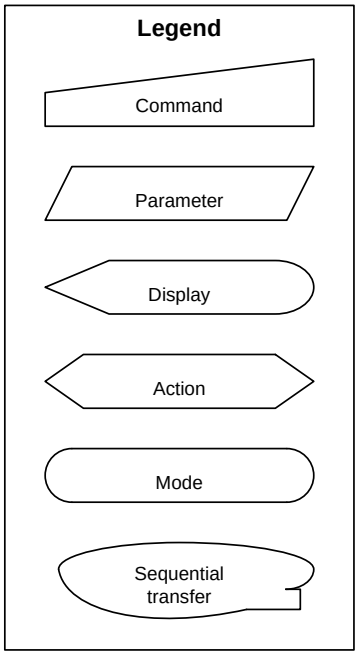


- FH – Flip Horizontal
  '0' = Normal
  '1' = Flip



	Host Processor	Display Image	D7 MY	D6 MX	D5 MV	Note
			0	0	0	Normal
			1	0	0	Flip Vertical
			0	1	0	Flip Horizontal

			1	1	0	180° Rotate
			0	0	1	
			1	0	1	
			0	1	1	

			1	1	1	
Flow Chart						

6.2.25 3Ah – Interface Pixel Format

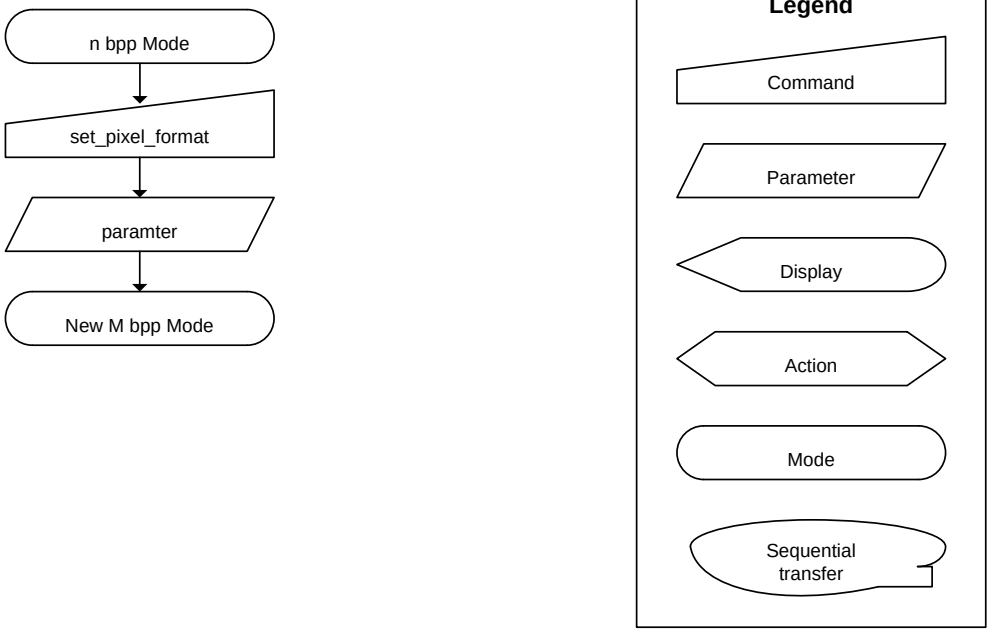
<table>
<tr><td>3Ah</td><td colspan="13">Interface Pixel Format</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D [23:8]</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Reset</td></tr>
<tr><td>command</td><td>0</td><td>1</td><td>↑</td><td>X</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>3Ah</td></tr>
<tr><td>Parameter</td><td>1</td><td>↑</td><td>1</td><td>X</td><td>0</td><td colspan="3">DPIPF [2:0]</td><td>0</td><td colspan="3">DBIPF [2:0]</td><td>77h</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to define the format of RGB picture data, which are to be transferred via the DBI/DPI.

The formats are shown in the following table:
Bit D[6:4] – DPI Pixel Format (RGB Interface Color Format Selection)
Bit D[2:0] – DBI Pixel Format (I80, M68 Interface Color Format Selection)
<table>
<tr><th>Control Interface Color Format</th><th>D6/D2</th><th>D5/D1</th><th>D4/D0</th></tr>
<tr><td>Setting disabled</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Setting disabled</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>Setting disabled</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>Setting disabled</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>Setting disabled</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>16bit/pixel (65k colors)</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>18bit/pixel (262k colors)</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>24bit/pixel (16M colors)</td><td>1</td><td>1</td><td>1</td></tr>
</table>
See “DPI Data Format” “Data Format List” for each type of interfaces.
See “DBI Data Format” “Data Format List” for each type of interfaces.

Note 1: When the setting disabled bits are set, undesirable image will be displayed on the panel.

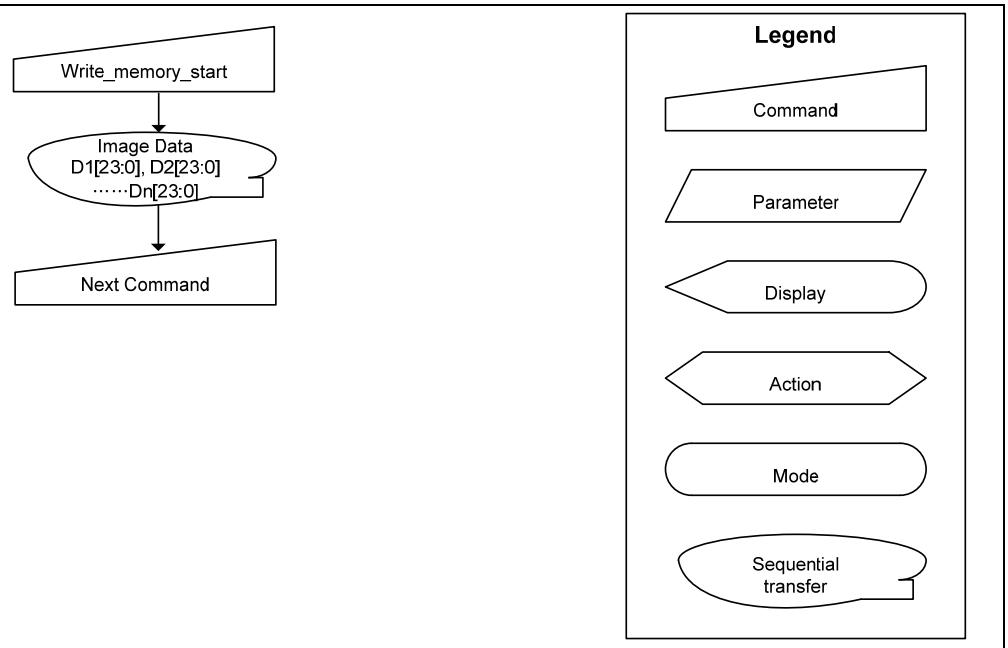
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">-</td></tr>
</table>

Flow Chart


n bpp Mode
set_pixel_format
paramter
New M bpp Mode
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.26 3Ch – Write Memory Continue

3Ch	Write Memory Continue												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	0	0	1	0	1	1	0	0	2Ch
1st parameter	1	1	↑	D1[23:0]									-
2nd parameter	1	1	↑	D2[23:0]									-
⋮	1	1	↑	⋮									-
Nth parameter	1	1	↑	Dn[23:0]									-
Description	This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command. Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are over write.												
Restriction	A write_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the write address. Otherwise, data written with write_memory_continue is written to undefined addresses.												

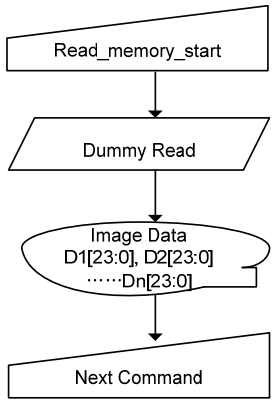
Flow Chart	

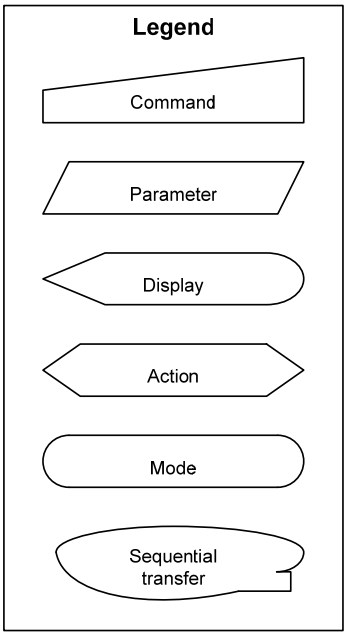
Write_memory_start
Image Data
D1[23:0], D2[23:0]
·····Dn[23:0]
Next Command
Legend
Command
Parameter
Display
Action
Mode
Sequential
transfer

6.2.27 3Eh – Read Memory Continue

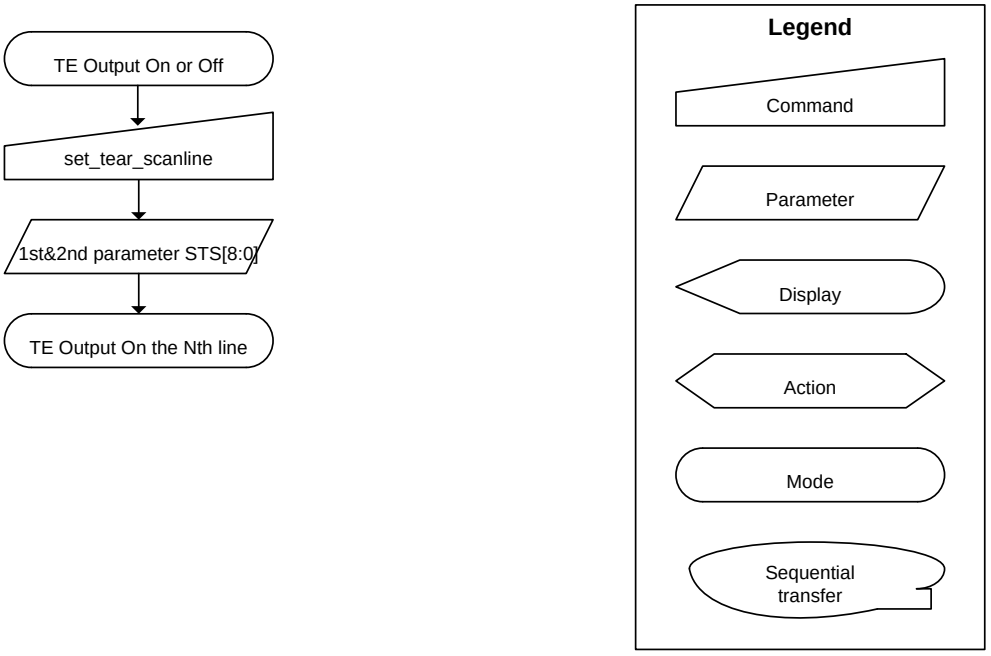
3Eh	Read Memory Continue												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	0	0	1	0	1	1	1	0	3Eh
1st parameter	1	↑	1	D1[23:0]									-
2nd parameter	1	↑	1	D2[23:0]									-
⋮	1	↑	1	⋮									-
Nth parameter	1	↑	1	Dn[23:0]									-
Description	This command transfers image data from the display module's frame memory to the host processor continuing from the location following the previous read_memory_continue or read_memory_start command. Pixels are read continuing from the pixel location after the read range of the previous read_memory_start or read_memory_continue. The column register is then incremented and pixels are read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command.												
Restriction	Regardless of the color mode set in set_pixel_format, the pixel format returned by read_memory_continue is always 24-bit so there is no restriction on the length of data.												

Flow Chart

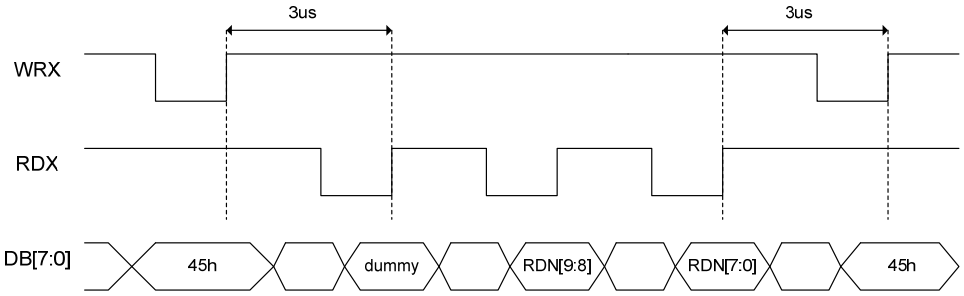

Read_memory_start
Dummy Read
Image Data
D1[23:0], D2[23:0]
·····Dn[23:0]
Next Command


Legend
Command
Parameter
Display
Action
Mode
Sequential
transfer

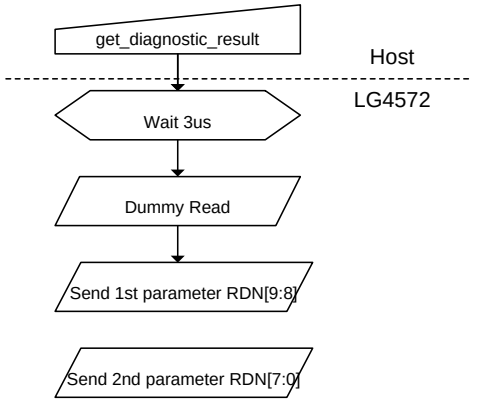
6.2.28 44h – Set Tear Scan line

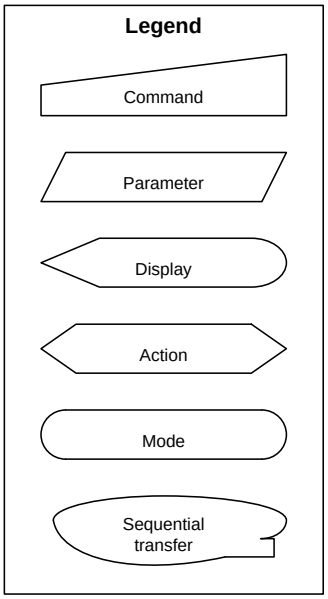
44h	Set Tear Scan line												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	0	1	0	0	0	1	0	0	44h
1st parameter	1	1	↑	X	0	0	0	0	0	0	TEN[9:8]		00h
2nd parameter	1	1	↑	X	TEN [7:0]								00h
Description	This command turns on the display module's Tearing Effect output signal on the TE signal line when the display module reaches line N defined by TEL [9:0]. TE line is unaffected by change in B4 bit of set_address_mode command. See figure in "TE Pin Output Signal". X = Don't care												
Restriction	The command takes affect on the frame following the current frame. Therefore, if the TE signal is already ON, TE signal is output according to the old set_tear_on and set_tear_scanline commands until the end of currently scanned frame. Setting is disabled when TEM=1 of set_tear_on (35h). Make sure that TEN [9:0] < NL (number of line).												
Flow Chart													

6.2.29 45h – Get Scan line

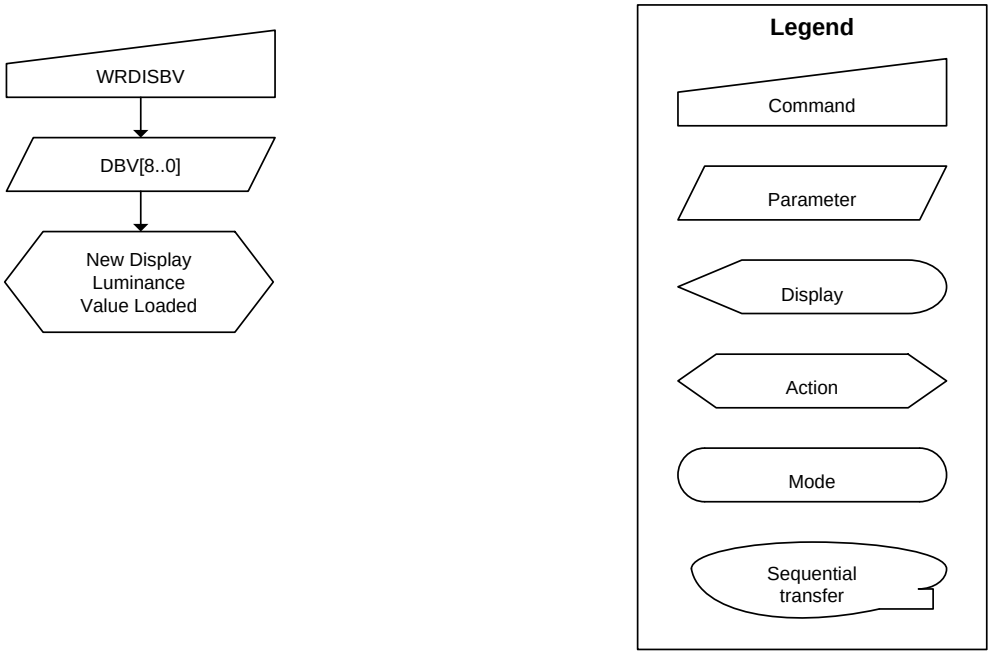
45h	Get Scan line												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	0	1	0	0	0	1	0	1	45h
1st parameter	1	1	↑	X	0	0	0	0	0	0	RDN[9:8]		xxh
2nd parameter	1	1	↑	X	RDN[7:0]								xxh
Description	The display module returns the current scan line. The total number of scan lines is defined as (BP + NL + FP). The first scan line of back portch period is defined as line 0. In sleep mode, the value returned by get_scanline is undefined. X = Don't care												
Restriction	After get_scanline command is input, it takes 3us or more to read it. After parameters are read, wait 3 us or more to reinput this command.  												

Flow Chart


get_diagnostic_result
Host
LG4572
Wait 3us
Dummy Read
Send 1st parameter RDN[9:8]
Send 2nd parameter RDN[7:0]


Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

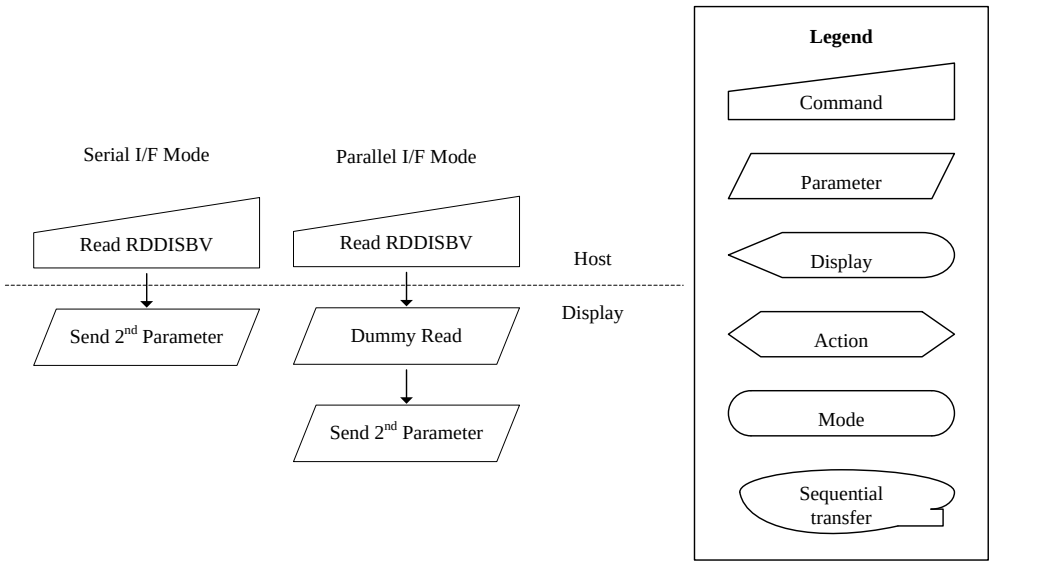
6.2.30 51h – Write Display Brightness

51h	Write Display Brightness												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	0	1	0	1	0	0	0	1	51h
1st parameter	1	1	↑	X	DBV [7:0]								00h
Description	This command is used to adjust the brightness value of the display. It should be checked what the relationship between this written value and output brightness of the display is. This relationship is defined on the display module specification. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. X = Don't care												
Restriction	-												
Flow Chart													

6.2.31 52h – Read Display Brightness Value

52h	Read Display Brightness Value												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	0	1	0	1	0	0	1	0	52h
1st parameter	1	↑	1	X	x	x	x	x	x	x	x	x	xxh
2nd parameter	1	↑	1	X	DBV[7:0]								00h
Description	This command returns the brightness value of the display. It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification is. In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. X = Don't care												
Restriction	-												

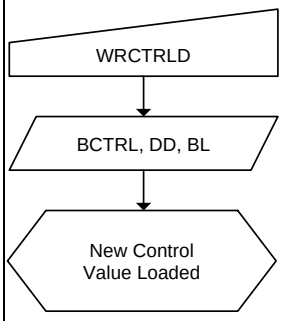
Flow Chart

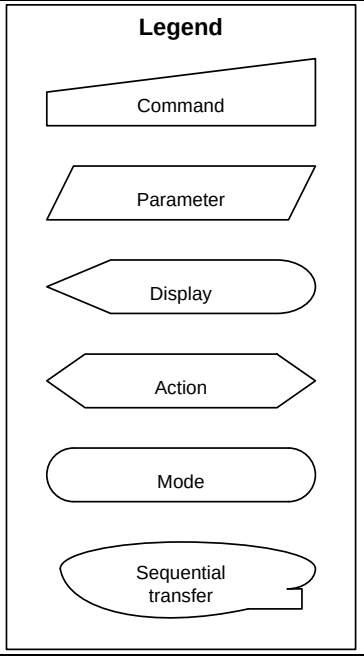

Serial I/F Mode
Parallel I/F Mode
Read RDDISBV
Read RDDISBV
Host
Display
Send 2nd Parameter
Dummy Read
Send 2nd Parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.32 53h – Write Control Display

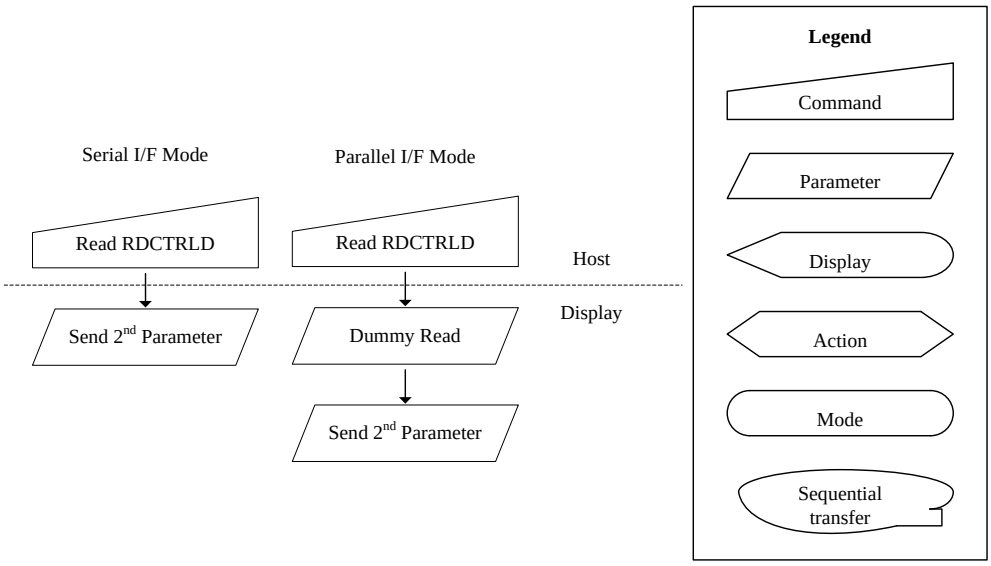
53h	Write Control Display												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	0	1	0	1	0	0	1	1	53h
1st parameter	1	1	↑	X	0	0	BCTRL	0	DD	BL	0	0	00h
Description	This command is used to control display brightness. **BCTRL:** Brightness Control Block On/Off, This bit is always used to switch brightness for display. 0 = Off (Brightness registers are 00h, DBV[7..0]) 1 = On (Brightness registers are active, according to the other parameters.) Display Dimming (**DD**): (Only for manual brightness setting) DD = 0: Display Dimming is off DD = 1: Display Dimming is on **BL**: Backlight Control On/Off 0 = Off (Completely turn off backlight circuit. Control lines must be low.) 1 = On Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 → 1 or 1 → 0. When BL bit change from "On" to "Off", backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected. X = Don't care.												
Restriction	-												

Flow Chart


WRCTRLD
BCTRL, DD, BL
New Control
Value Loaded


Legend
Command
Parameter
Display
Action
Mode
Sequential
transfer

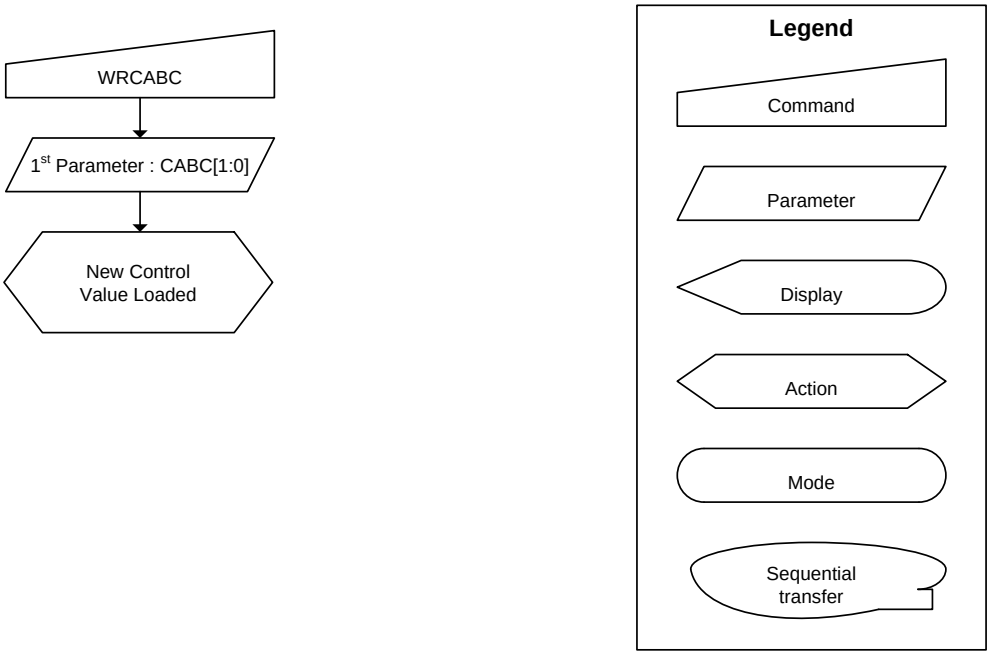
6.2.33 54h – Read Control Display

54h	Read Control Display												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	0	1	0	1	0	1	0	0	54h
1st parameter	1	↑	1	X	x	x	x	x	x	x	x	x	xxh
2nd parameter	1	↑	1	X	0	0	BCTRL	0	0	DD	BL	0	00h
Description	This command returns ambient light and brightness control values. **BCTRL** : Brightness Control Block On/Off, This bit is always used to switch brightness for display. 0 = Off 1 = On Display Dimming (**DD**): DD = 0: Display Dimming is off DD = 1: Display Dimming is on **BL :** Backlight Control On/Off 0 = Off (completely turn off backlight circuit) 1 = On X = Don't care.												
Restriction	-												
Flow Chart													

6.2.34 55h – Write Content Adaptive Brightness Control

<table>
<tr><td>55h</td><td colspan="13">Write Content Adaptive Brightness Control</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D [23:8]</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Reset</td></tr>
<tr><td>command</td><td>0</td><td>1</td><td>↑</td><td>X</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>55h</td></tr>
<tr><td>1st parameter</td><td>1</td><td>1</td><td>↑</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="2">CABC[1:0]</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to set parameters for image content based adaptive brightness control functionality.

There is possible to use 4 different modes for content adaptive image functionality,

<table><tr><th>CABC[1:0]</th><th>Description</th></tr><tr><td>2’h0</td><td>Off</td></tr><tr><td>2’h1</td><td>User Interface Image</td></tr><tr><td>2’h2</td><td>Still Picture</td></tr><tr><td>2’h3</td><td>Moving Image</td></tr></table>
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">-</td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

6.2.35 56h – Read Content Adaptive Brightness Control

56h	Read Content Adaptive Brightness Control												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	0	1	0	1	0	1	1	0	56h
1st parameter	1	↑	1	X	x	x	x	x	x	x	x	x	xxh
2nd parameter	1	↑	1	X	0	0	0	0	0	0	CABC [1:0]		00

Description

This command is used to read the settings for image content based adaptive brightness control functionality.

There is possible to use 4 different modes for content adaptive image functionality,

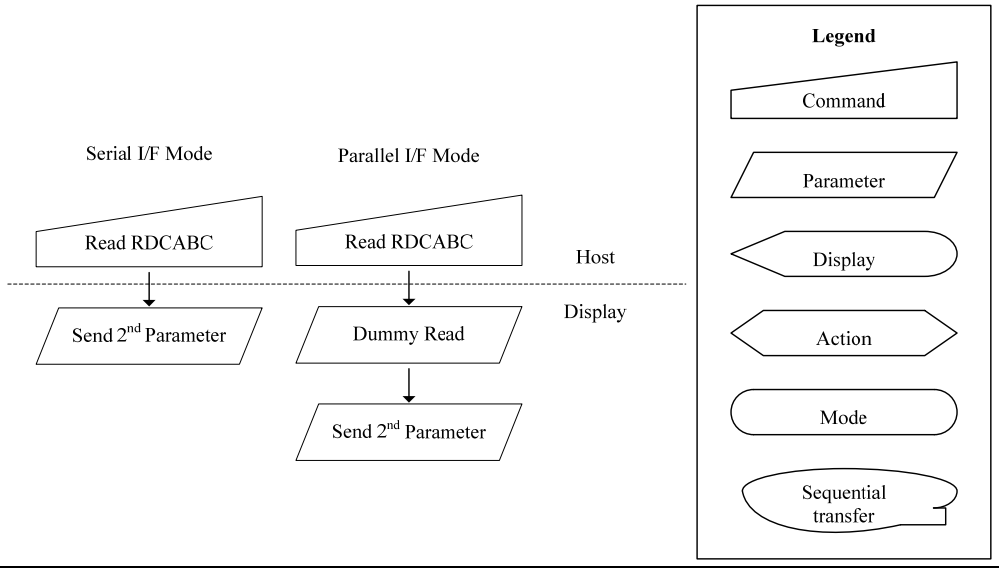
CABC[1:0]	Description
2'h0	Off
2'h1	User Interface Image
2'h2	Still Picture
2'h3	Moving Image

X = Don't care

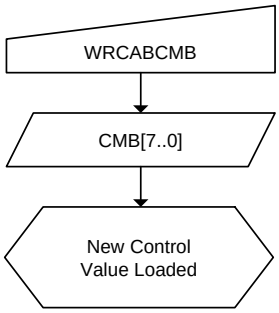
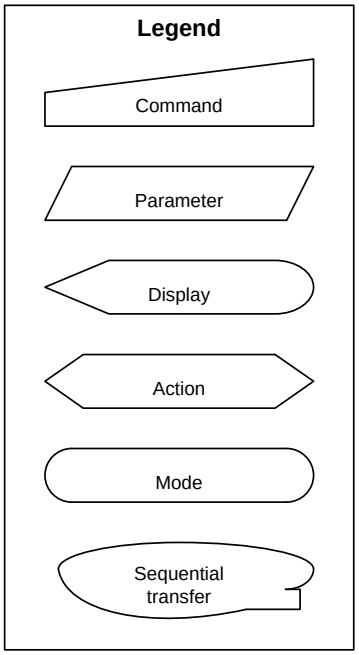
Restriction

-

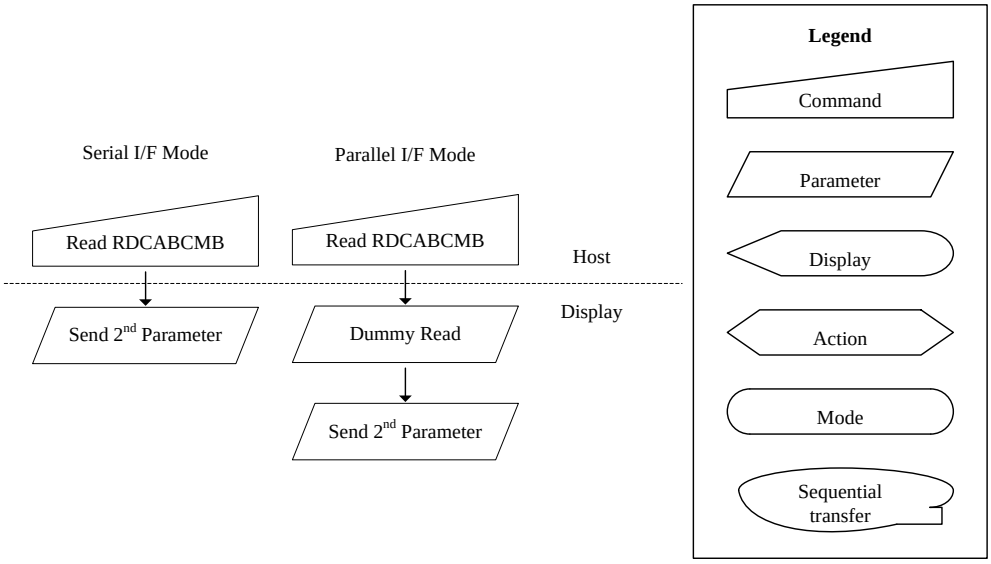
Flow Chart



6.2.36 5Eh – Write CABC Minimum Brightness

5Eh	Write CABC Minimum Brightness												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	0	1	0	1	1	1	1	0	5Eh
1st parameter	1	1	↑	X	CMB[7:0]								00h
Description	This command is used to set the minimum brightness value of the display for CABC function. In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC. X = Don't care												
Restriction	-												
Flow Chart	 												

6.2.37 5Fh – Read CABC Minimum Brightness

5Fh	Read CABC Minimum Brightness												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	0	1	0	1	1	1	1	1	5Fh
1st parameter	1	↑	1	X	x	x	x	x	x	x	x	x	xxh
2nd parameter	1	↑	1	X	CMB[7:0]								00
Description	This command returns the minimum brightness value of CABC function. In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. CMB[7:0] is CABC minimum brightness specified with "9.2.45 Write CABC Minimum Brightness (5Eh)" command.												
Restriction	-												
Flow Chart													

6.2.38 A1h – Read DDB Start

Mnemonic RDDDB

Type Read

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	DDB[7:0] : Revision								10h
2	DDB[7:0] : Level								01h
3	DDB[7:0] : Not used								00h
4	DDB[7:0] : Not used								00h
5	DDB[7:0] : Manufacture ID (MSB)								01h
6	DDB[7:0] : Manufacture ID (LSB)								2Ah
7	DDB[7:0] : Device Code (MSB)								45h
8	DDB[7:0] : Device Code (LSB)								72h
9	DDB[7:0] : Length of DDB Level 2 Data (MSB)								00h
10	DDB[7:0] : Length of DDB Level 2 Data (LSB)								2Ah
…	…								…

Description

This command returns the DDB (Device Descriptor Block) values. For further DDB values in level 2 (larger number than 10) are not described here in detail.

6.2.39 B1h – RGB Interface Setting

B1h	RGB Interface Setting												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	1	0	1	1	0	0	0	1	B1h
1st parameter	1	#A	#B	X	DPICC			SYNC	CKPL	HSPL	VSPL	DEPL	06h
2nd parameter	1	#A	#B	X		HBP [6:0]							1Eh
3rd parameter	1	#A	#B	X	VBP [7:0]								0Ch

Description

This command is used to set registers related with RGB (MIPI DPI) interface.

SYNC – Sync mode
0 = VSYNC+HSYNC+DE
1 = VSYNC+HSYNC
If SYNC is 1, the DE pin is ignored and a corresponding signal is internally generated using the registers HBP and VBP.

CKPL – PCLK pin polarity
0 = Rising edge
1 = Falling edge

HSPL – HSYNC pin polarity
0 = Active high
1 = Active low

VSPL – VSYNC pin polarity
0 = Active high
1 = Active low

DEPL – DE pin polarity
0 = Active high
1 = Active low

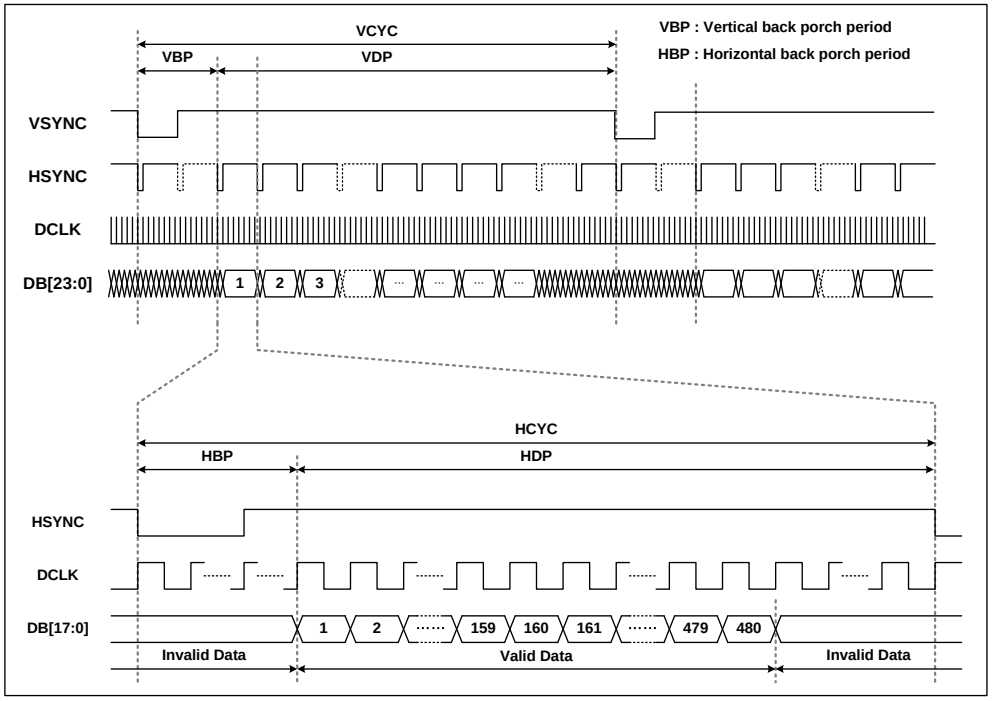
HBP[6:0] – Horizontal back porch in PCLK(Used only if RGBIF, SYNC=1, HBP > SDT)

HBP[6:0]	Horizontal back porch
7'h0	0
7'h1	1 x PCLK
7'h2	2 x PCLK
:	:
:	:
7'h7D	125 x PCLK

7'h7E	126 x PCLK
7'h7F	127 x PCLK

VBP[7:0] : Vertical back porch in line (Used only if RGBIF, SYNC = 1)

VBP[7:0]	Vertical back porch
8'h0	0 line
8'h1	1 line
8'h2	2 line
:	:
:	:
8'hFD	253 line
8'hFE	254 line
8'hFF	255 line



6.2.40 B2h – Panel Characteristics Setting

B2h	Panel Characteristics Setting												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	1	0	1	1	0	0	1	0	B2h
1st parameter	1	#A	#B	X	0	0	LR	SELP	0	HRS [1:0]		REV	10h
2nd parameter	1	#A	#B	X	VRS [7:0]								D8h

Description

Write #A="1" #B="↑"
Read #A="↑" #B=" 1" & Insert dummy read

LR – Left & right control signals for GIP circuits can be exchanged by using this register. If LR is high, then left and right signals are exchanged. But if low, then they remain as they are.

SELP – Panel Select
0 : L-type panel
1 : H-type panel

HRS[1:0]	H resolution in pixels
2'h0	480 pixels
2'h1	360 pixels (1~180 non-used, 181~1260 used, 1261~1440 non-used)
2'h2	320 pixels. (1~240 non-used, 241~1200 used, 1201~1440 non-used)
2'h3	240 pixels. (1~360 non-used, 361~1080 used, 1081~1440 non-used)

REV –
0 : Normally Black panel
1 : Normally White panel

VRS[7:0] – V resolution divided by 4.

For example, if VRS is C8h (200 in decimal), vertical resolution is 864.

VRS[7:0]	Vertical Line
8'h0	0 line
8'h1	4 line
8'h2	8 line
:	:
:	:

	8'hD6	856 line
	8'hD7	860 line
	8'hD8	864 line

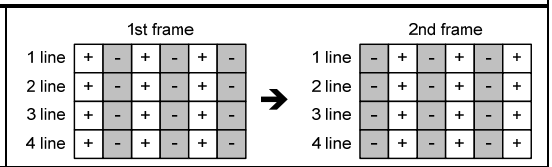
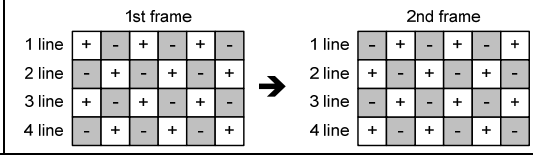
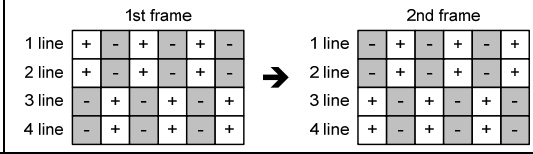
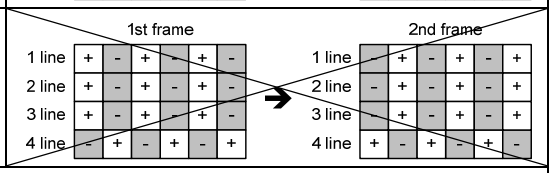
6.2.41 B3h – Panel Drive Setting

B3h	Panel Drive Setting												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	1	0	1	1	0	0	1	1	B3h
1st parameter	1	#A	#B	X	0	0	0	0	0	0	DINV [1:0]		02h

Description

Write #A="1" #B="↑"
Read #A="↑" #B=" 1" & Insert dummy read

DINV[1:0] – Set the inversion mode.

DINV[1:0]	Dot inversion mode	
2'h0	Column inversion	
2'h1	1-dot	
2'h2	2-dot	
~~2'h3~~	~~3-dot~~	

6.2.42 B4h – Display Mode Control

B4h	Display Mode Control												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	1	0	1	1	0	1	0	0	B4h
1st parameter	1	#A	#B	X	0	0	0	0	0	DITH	0	0	04h
Description	Write #A="1" #B="↑" Read #A="↑" #B=" 1" & Insert dummy read **DITH** – Dither enable.(24bit → 18bit) 1 : Dither enable. 0 : Dither disable.												

6.2.43 B5h – Display Control 1

B5h	Display Control 1(Source Output Control) (See below note)												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	1	0	1	1	0	1	0	1	B5h
1st parameter	1	#A	#B	X	SDT [7:0]								10h
2nd parameter	1	#A	#B	X	0	~~SHPN[6:0]~~							~~10h~~
3rd parameter	1	#A	#B	X	0	~~ENGND [6:0]~~							~~10h~~
4th parameter	1	#A	#B	X	~~SHIZ[7:0]~~								~~00h~~
5th parameter	1	#A	#B	X	0	0	PTS[1:0]		0	0	0	SLT	20h

Description

Write #A="1" #B="↑"
Read #A="↑" #B=" 1" & Insert dummy read

SDT[7:0] – Source output delay, [1..255] pixel clocks

DPI , MIPI Video		I80, M68, MDDI, MIPI command	
SDT[7:0]	**Source output delay time.**	**SDT[7:0]**	**Source output delay time.**
8'h00	Setting disabled	8'h00~8'h07	Setting disabled
8'h01	1 x PCLK	8'h08~8'h17	1 x OSC
8'h02	2 x PCLK	8'h18~8'h27	3 x OSC
:	:	:	:
:	:	:	:
8'hFD	253 x PCLK	8'hD8~8'hE7	27 x OSC
8'hFE	254 x PCLK	8'hE8~8'hF7	29 x OSC
8'hFF	255 x PCLK	8'hF8~8'hFF	31 x OSC

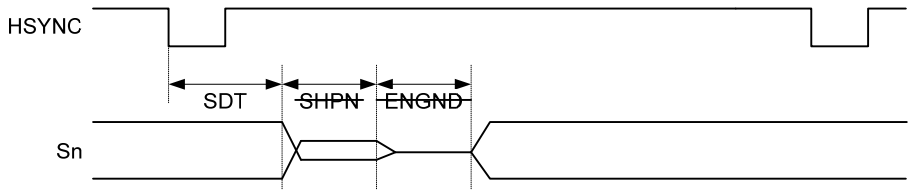
~~**SHPN[6:0]** – Set the equalize level period~~

~~SHPN[6:0]~~	~~Set the equalize level period~~
~~7'h00~~	~~0~~
~~7'h01~~	~~1 x PCLK~~
~~7'h02~~	~~2 x PCLK~~
~~:~~	~~:~~
~~:~~	~~:~~
~~7'h7D~~	~~125 x PCLK~~

7'h7E	126 x PCLK
7'h7F	127 x PCLK

ENGND[6:0] – Set the GND level period.

ENGND [6:0]	Set the GND level period
7'h00	0
7'h01	1 x PCLK
7'h02	2 x PCLK
÷	÷
÷	÷
7'h7D	125 x PCLK
7'h7E	126 x PCLK
7'h7F	127 x PCLK



SHIZ[7:0] – Source output Hi-Z control via GDC, BDC

SHIZ[7:0]	Source output Hi-Z control
8'h00	0
8'h01	1 x PCLK
8'h02	2 x PCLK
÷	÷
÷	÷
8'hFD	253 x PCLK
8'hFE	254 x PCLK
8'hFF	255 x PCLK

SLT – Source output enable signal

0 : 1 signal / 1 line

1 : 2 signal / 1 line

PTS[1:0] – Set the source output in non-display drive period.₩

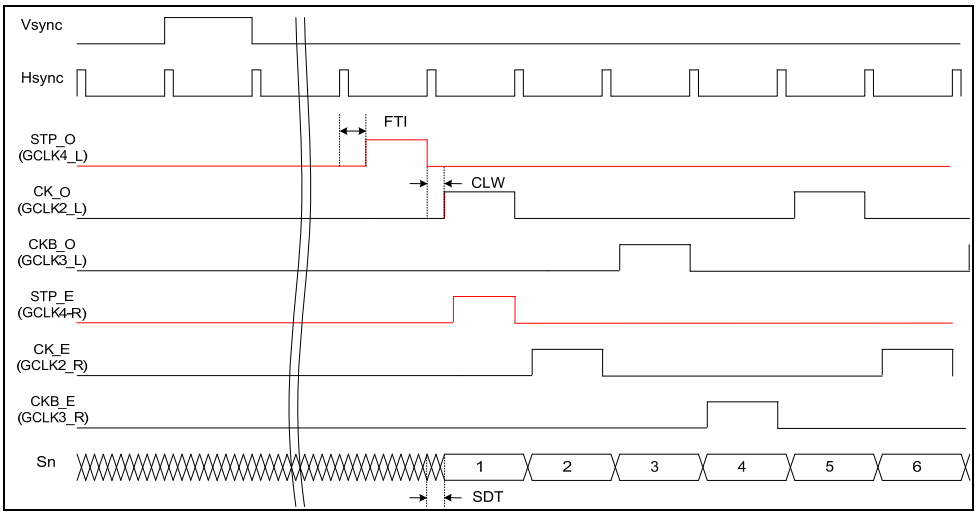
PTS[1:0]	Source output in non-display drive period

	2'h0, 2'h1	black
	2'h2	GND
	2'h3	High-Z

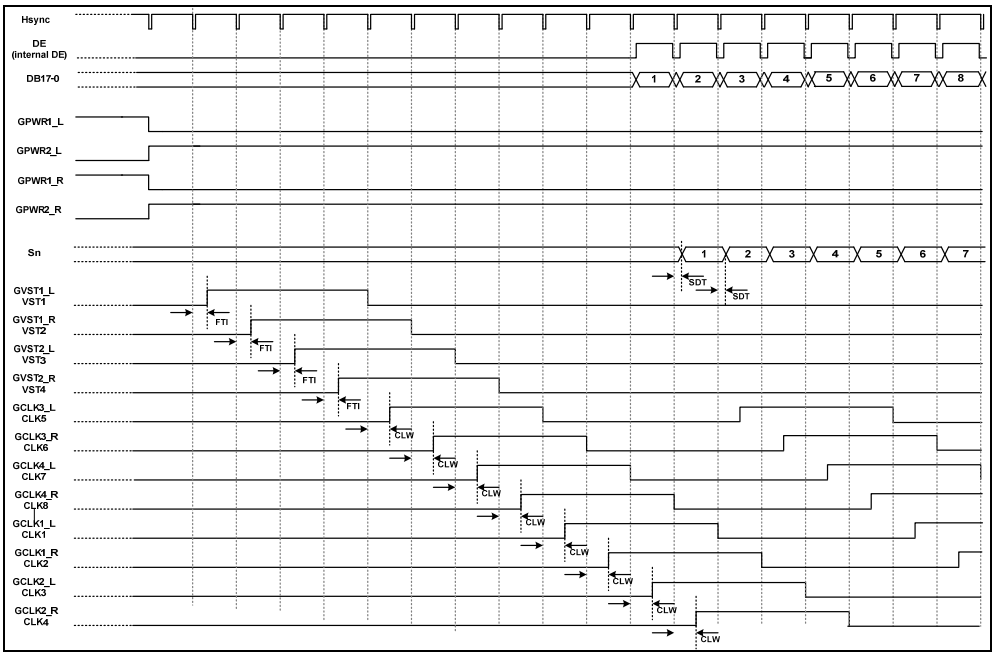
Note) SHPN, ENGND, and SHIZ don't have to be changed. Their changes must be done with very care. So, they should be left just for engineering mode not for the general IC users. This deletion doesn't mean not settable. They can be set but recommended not being changed! The default settings for them are highly recommended.

6.2.44 B6h – Display Control 2

B6h	Display Control 2 (Gate Output Control)												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	1	0	1	1	1	0	1	0	B6h
1st parameter	1	#A	#B	X	0	0	0	GSWAP	FVST	ASG	SDM	FHM	01h
2nd parameter	1	#A	#B	X	CLW [7:0]								18h
3rd parameter	1	#A	#B	X	0	0	GTO [5:0]						02h
4th parameter	1	#A	#B	X	GNO[7:0]								40h
5th parameter	1	#A	#B	X	FTI [7:0]								10h
6th parameter	1	#A	#B	X	GPM[7:0]								00h

Description	Write #A="1" #B="↑" Read #A="↑" #B=" 1" & Insert dummy read In case of H-type panel (SELP=1), ASG and FHN are the related registers. According to ASG, dual mode (ASG=0) or single mode (ASG=1) is selected. According to the FHN, non-overlap (FHN=0) or overlap (FHN=1) mode is selected. The FTI determines the delay time of starting signal (STPO or STPE) referring to Hsync. And the CLW determines the non-overlapping time between CLKs.. The following timing diagram and is for them. 

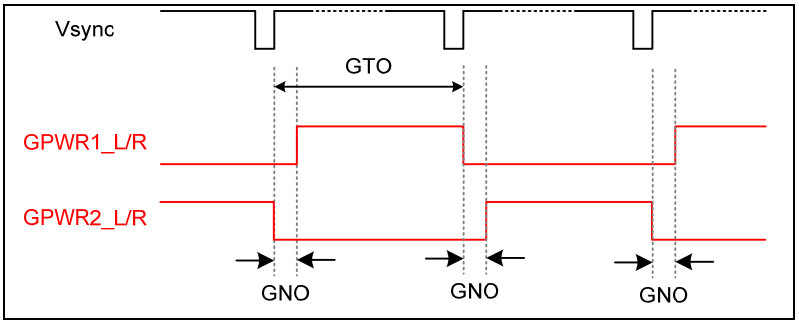
In case of L-type panel (SELP=0), FHN, SDM, , GSWAP, FVST, and FV (in 36h) are the related registers. According to the FHN, non-overlapping (FHN=0) or overlapping (FHN=1) mode is selected. According to the SDM, 4-phase (SDM=0) or 8-phase mode (SDM=1) is selected. Finally according to the FV, forward scan mode (FV=0) or reverse scan mode (FV=1) is selected. By using this reversed scan direction, flip vertical image can be gotten. But it should be noted that some L-type panels do not support this bi-directional scanning feature. Non-overlapping control is done by using FTI and CLW registers. GVSTs output delay timing referred to Hsync can be set by FTI register. And non-overlapping intervals between nearby GCLKs can be set by CLW register. The setting choices are same as in the H-type panel case.



DPI , MIPI Video		I80, M68, MDDI, MIPI command	
CLW[7:0]	**GCLK non-overlap timing**	**CLW[7:0]**	**GCLK non-overlap timing**
8'h00	0	8'h00~8'h07	0
8'h01	1 x PCLK	8'h08~8'h17	1 x OSC
8'h02	2 x PCLK	8'h18~8'h27	3 x OSC
:	:	:	:
:	:	8'hD8~8'hE7	27 x OSC
:	:	8'hE8~8'hF7	29 x OSC
:	:	8'hF8~8'hFF	31 x OSC
:	:		
8'hFD	253 x PCLK		
8'hFE	254 x PCLK		
8'hFF	255 x PCLK		

DPI , MIPI Video		I80, M68, MDDI, MIPI command	
FTI[7:0]	**GVST output delay**	**FTI[7:0]**	**GVST output delay**
7'h00	0	8'h00~8'h07	0
7'h01	1 x PCLK	8'h08~8'h17	1 x OSC
7'h02	2 x PCLK	8'h18~8'h27	3 x OSC
:	:	:	:
:	:	8'hD8~8'hE7	27 x OSC
:	:	8'hE8~8'hF7	29 x OSC
:	:	8'hF8~8'hFF	31 x OSC
:	:		
7'h7D	125 x PCLK		
7'h7E	126 x PCLK		
7'h7F	127 x PCLK		

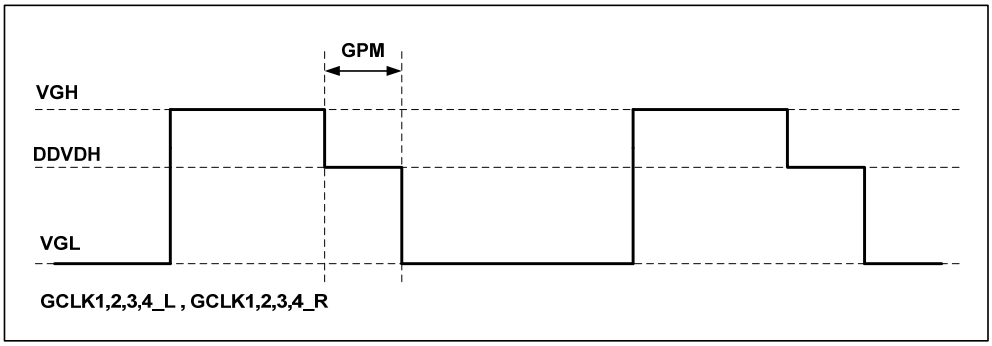
To get more stable panel electrical characteristics, GNO and GTO registers are used only for the L-type panel. GTO determines GPWRs toggle frequency and the GNO determines the non-overlap timing between nearby GPWRs. The following timing diagram and the tables defines this.



GTO[5:0]	GPWR toggle frequency
6'h00	0
6'h01	1 x Frame
6'h02	2 x Frame
:	:
:	:
6'hFD	61 x Frame
6'hFE	62 x Frame
6'h3F	63 x Frame

DPI , MIPI Video		I80, M68, MDDI, MIPI command	
GNO[7:0]	**GPWR non-overlap timing**	**GNO[7:0]**	**GPWR non-overlap timing**
7'h00	0	8'h00~8'h07	0
7'h01	1 x PCLK	8'h08~8'h17	1 x OSC
7'h02	2 x PCLK	8'h18~8'h27	3 x OSC
:	:	:	:
:	:	8'hD8~8'hE7	27 x OSC
:	:	8'hE8~8'hF7	29 x OSC
:	:	8'hF8~8'hFF	31 x OSC
:	:		
7'h7D	125 x PCLK		
7'h7E	126 x PCLK		
7'h7F	127 x PCLK		

For both H- and L- type panel cases, gate pulse modulation can be adopted to reduce source data sampling errors at the edge of gate falling by reducing the VGH and VGL voltage level difference when pixel data sampling. See the following functional diagram. The gate pulse modulated period (=GPM) can be controlled by using GPM register.



DPI , MIPI Video		I80, M68, MDDI, MIPI command	
GPM[7:0]	**Duration of gate pulse modulation**	**GPM[7:0]**	**Duration of gate pulse modulation**
8'h00	0	8'h00~8'h07	0
8'h01	1 x PCLK	8'h08~8'h17	1 x OSC
8'h02	2 x PCLK	8'h18~8'h27	3 x OSC
:	:	:	:
:	:	8'hD8~8'hE7	27 x OSC
:	:	8'hE8~8'hF7	29 x OSC

	:	:	8'hF8~8'hFF	31 x OSC
	:	:		
	8'hFD	253 x PCLK		
	8'hFE	254 x PCLK		
	8'hFF	255 x PCLK		

Detailed waveforms with each cases are illustrated in the following figures. According to SELP setting, either H-type panel (SELP=1) or L-type panel (SELP=0) case is selected.

H-Type Panel (SELP = 1)

The three following figures are for the H-type panel. They vary their waveforms according to the FHN and ASG register settings.

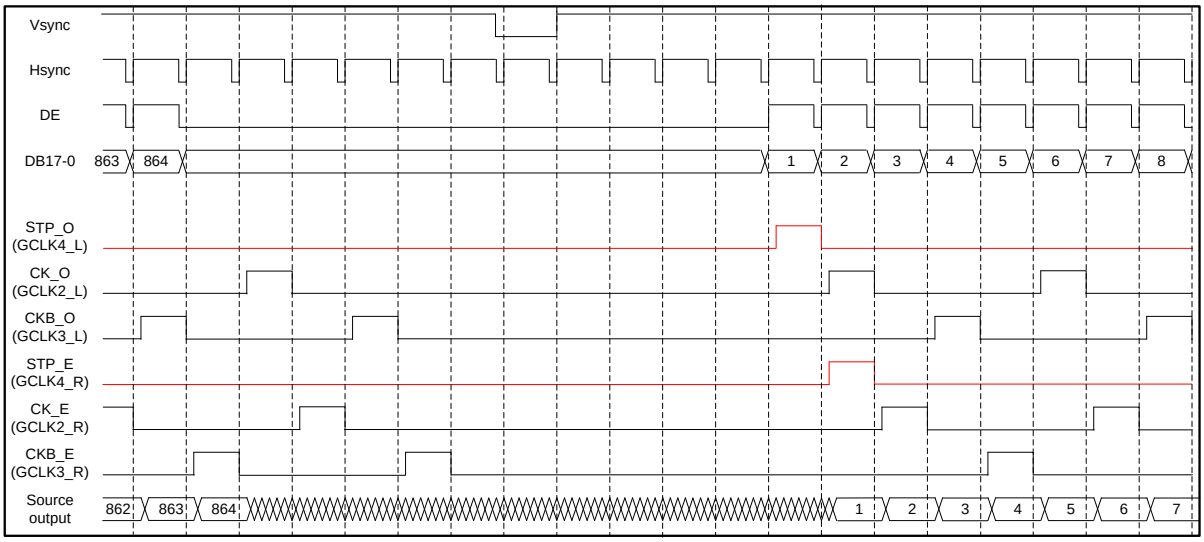


Figure 83. Non-overlap, dual scan (FHN=0, ASG=0)

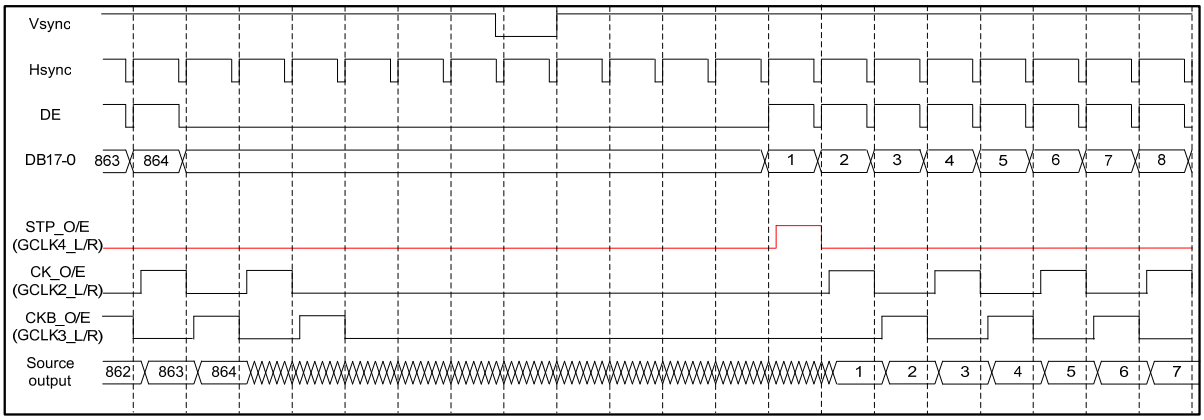


Figure 84. Non-overlap, single scan (FHN=X, ASG=1)

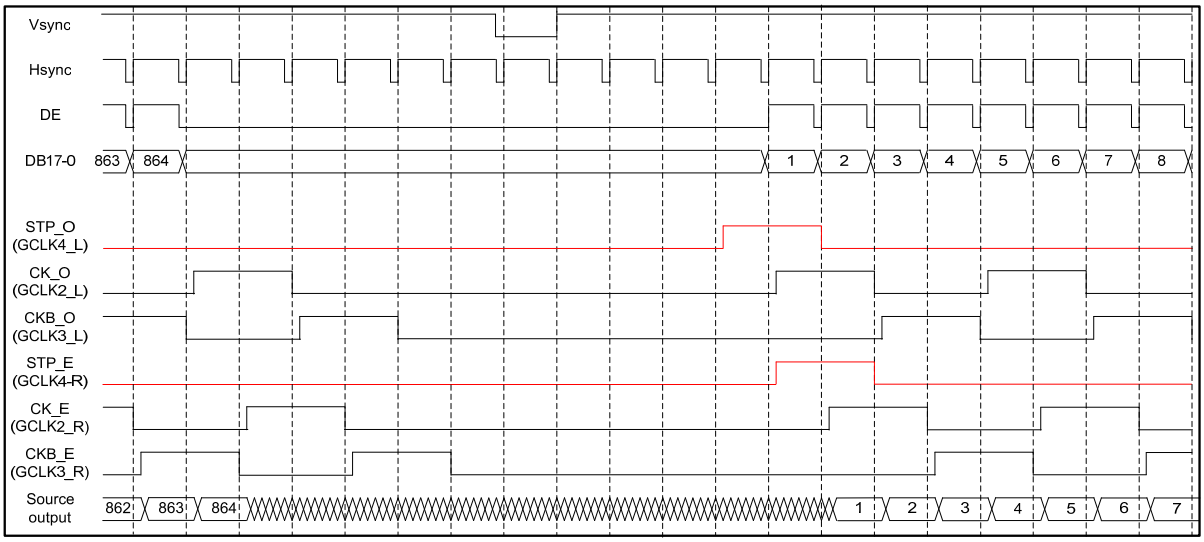


Figure 85. Overlap, dual scan (FHN=0, ASG=1)

L-Type Panel (SELP = 0)

The following figures are for the L-type panel. They vary their waveforms according to the FHN, SDM, FV and FVST register settings. When GSWAP register is set to high, GCLK waveform swapping happens for each modes.

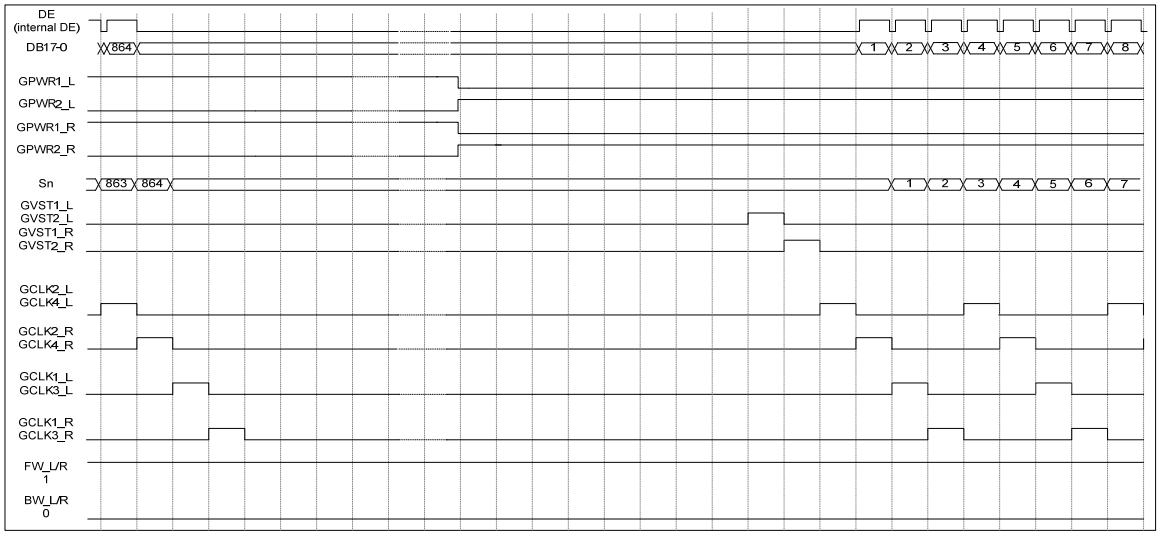


*Figure 86. Non-overlap, 4-phase, forward mode (**FHN=0, SDM=0, FV=0, FVST=0**)*

Note) GSWAP = 1 : GCLK2_L(4_L) ⇔GCLK1_L(3_L) Swap, GCLK1_R(3_R) ⇔GCLK2_R(4_R) Swap

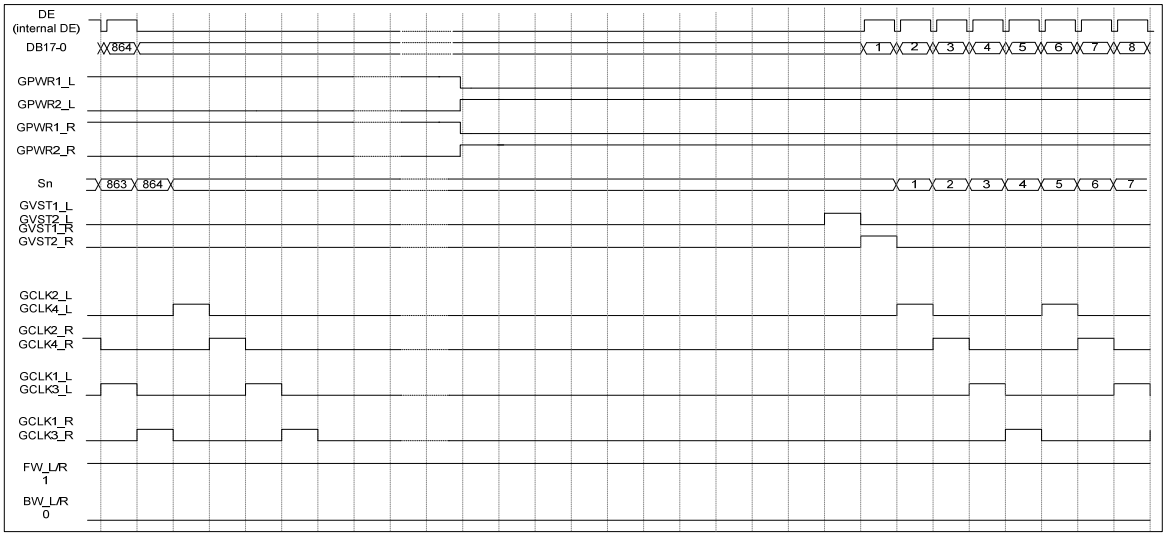


*Figure 87. Non-overlap, 4-phase, forward, advanced DE mode (**FHN=0, SDM=0, FV=0, FVST=1**)*

Note) GSWAP = 1 : GCLK2_L(4_L) ⇔GCLK1_L(3_L) Swap, GCLK1_R(3_R) ⇔GCLK2_R(4_R) Swap

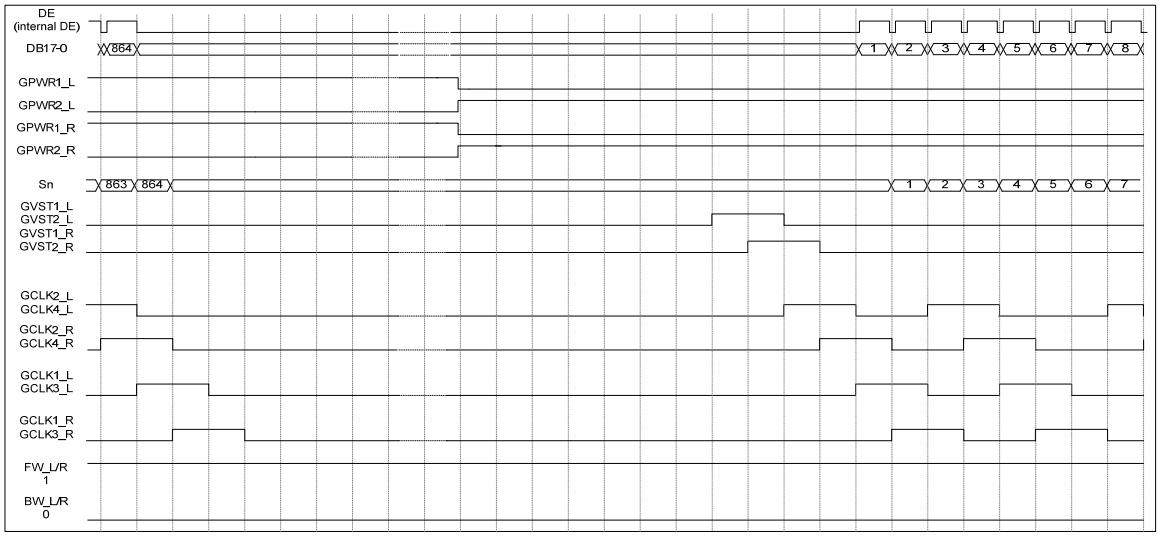


Figure 88. Overlap, 4-phase, forward mode ***(FHN=1, SDM=0, FV=0, FVST=0)***

Note) GSWAP = 1 : GCLK2_L(4_L) ⇔GCLK1_L(3_L) Swap, GCLK1_R(3_R) ⇔GCLK2_R(4_R) Swap

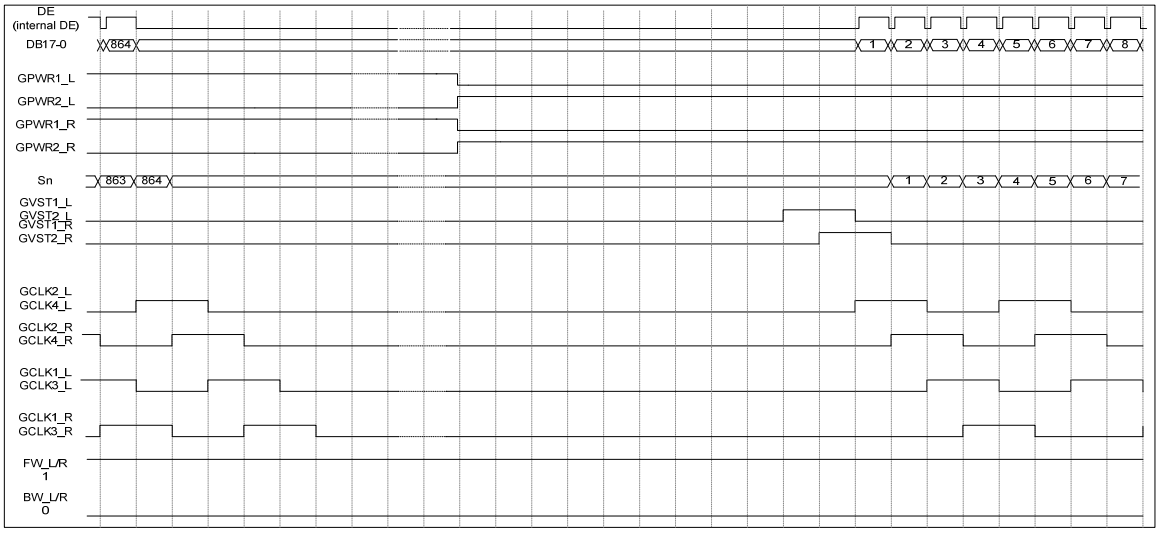


*Figure 89. Overlap, 4-phase, forward, advanced DE mode (****FHN=1, SDM=0, FV=0, FVST=1)***

Note) GSWAP = 1 : GCLK2_L(4_L) ⇔GCLK1_L(3_L) Swap, GCLK1_R(3_R) ⇔GCLK2_R(4_R) Swap

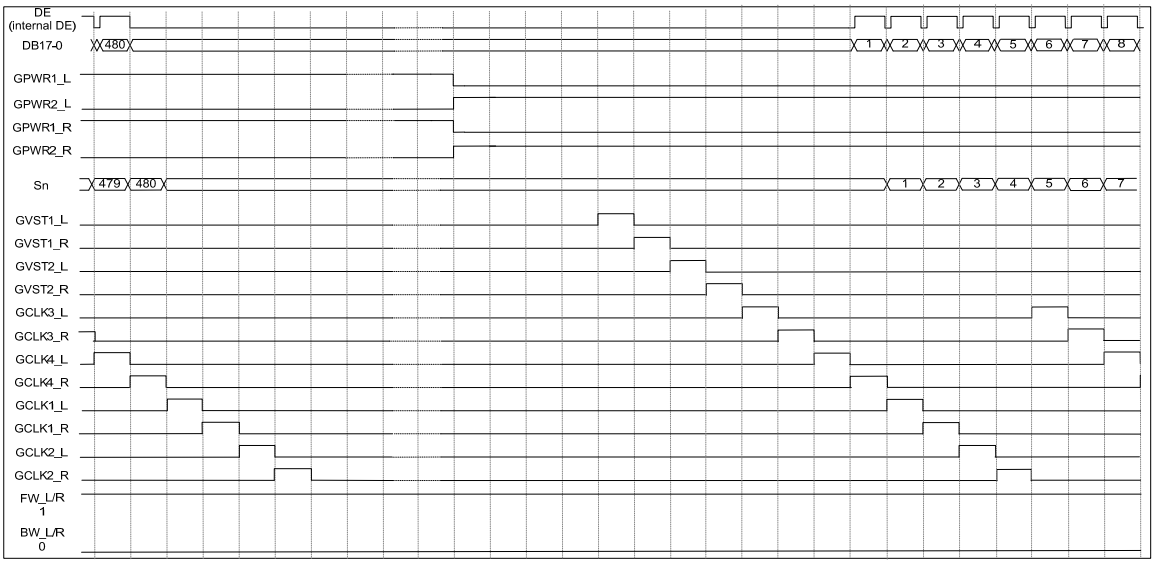


*Figure 90. Non-overlap, 8-phase, forward mode (**FHN=0, SDM=1, FV=0, FVST=0**)*

Note) GSWAP = 1 : GCLK3_L/4_L ⇔GCLK1_L/2_L Swap, GCLK3_R/4_R ⇔GCLK1_R/2_R Swap

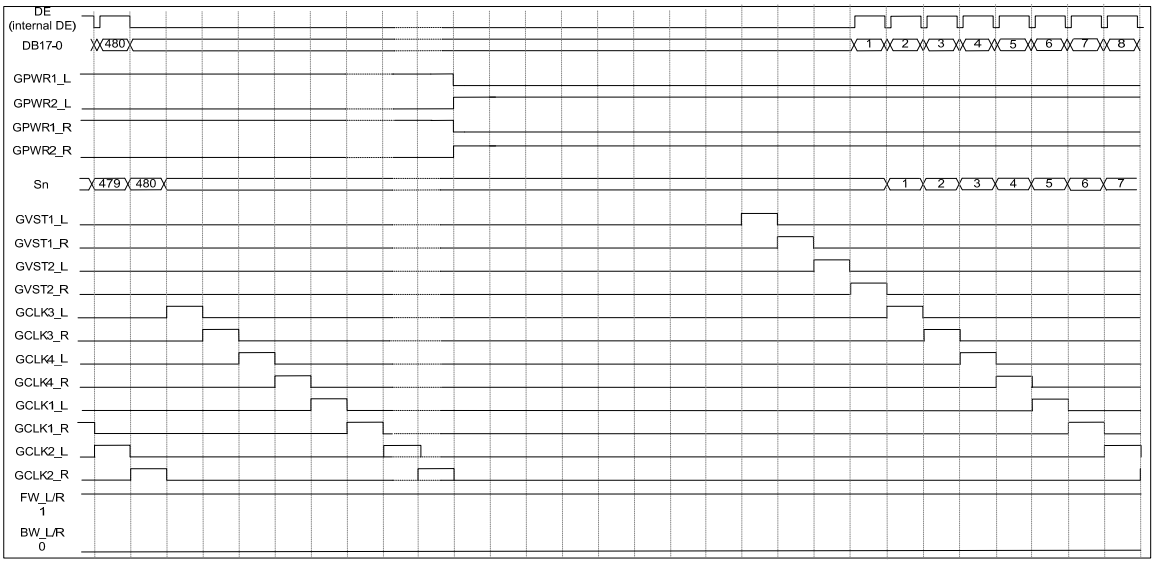


*Figure 91. Non-overlap, 8-phase, forward, advanced DE mode (**FHN=0, SDM=1, FV=0, FVST=1**)*

Note) GSWAP = 1 : GCLK3_L/4_L ⇔GCLK1_L/2_L Swap, GCLK3_R/4_R ⇔GCLK1_R/2_R Swap

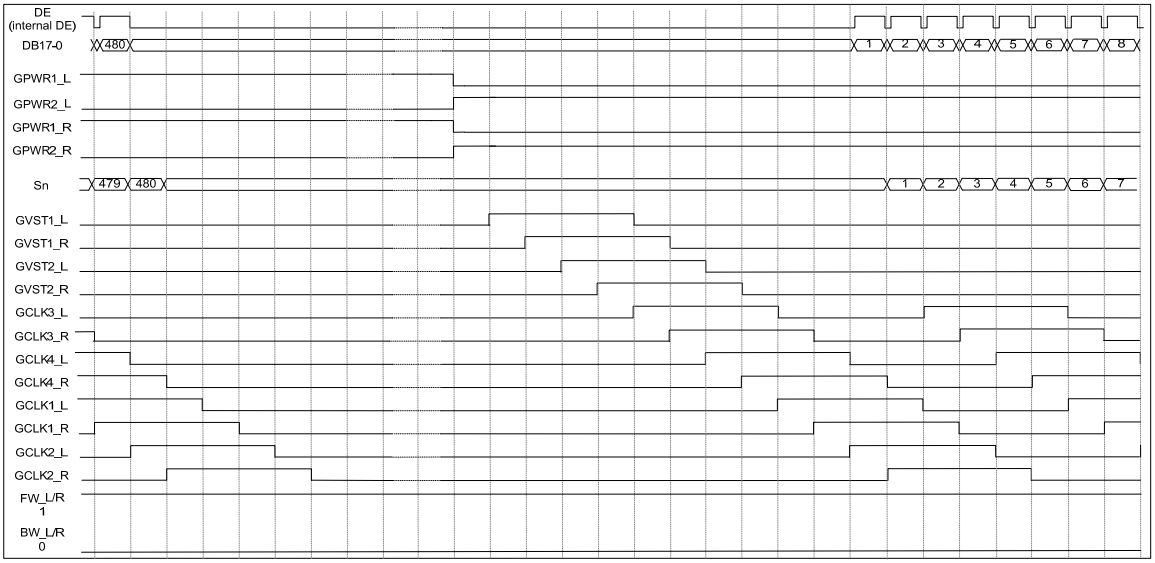


*Figure 92. Overlap, 8-phase, forward mode (**FHN=1, SDM=1, FV=0, FVST=0**)*
Note) GSWAP = 1 : GCLK3_L/4_L ⇔GCLK1_L/2_L Swap, GCLK3_R/4_R ⇔GCLK1_R/2_R Swap

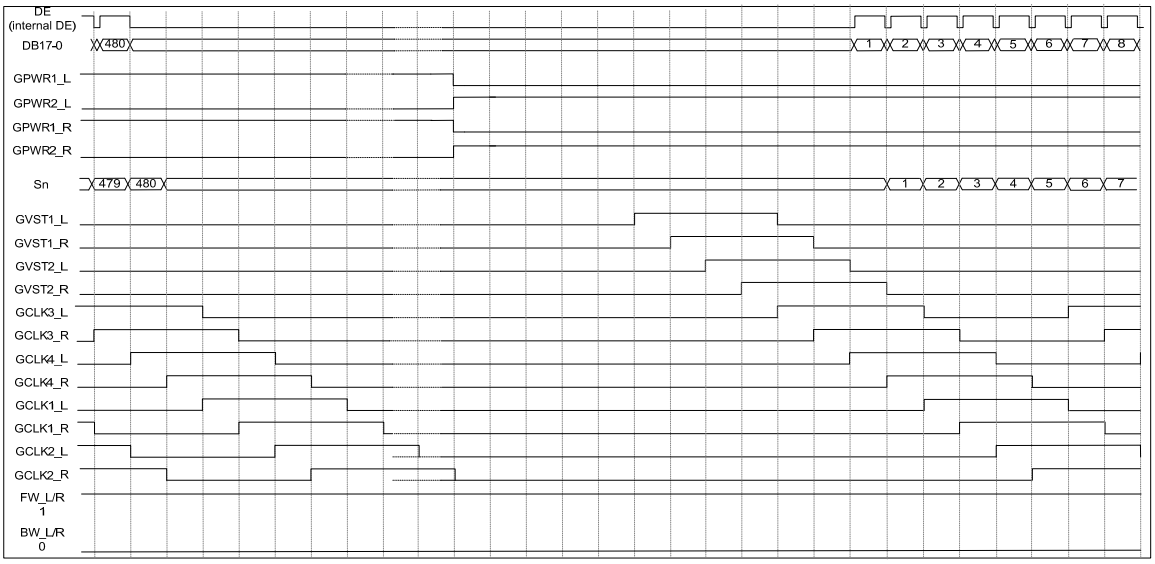


*Figure 93. Overlap, 8-phase, forward, advanced DE mode (**FHN=1, SDM=1, FV=0, FVST=1**)*
Note) GSWAP = 1 : GCLK3_L/4_L ⇔GCLK1_L/2_L Swap, GCLK3_R/4_R ⇔GCLK1_R/2_R Swap

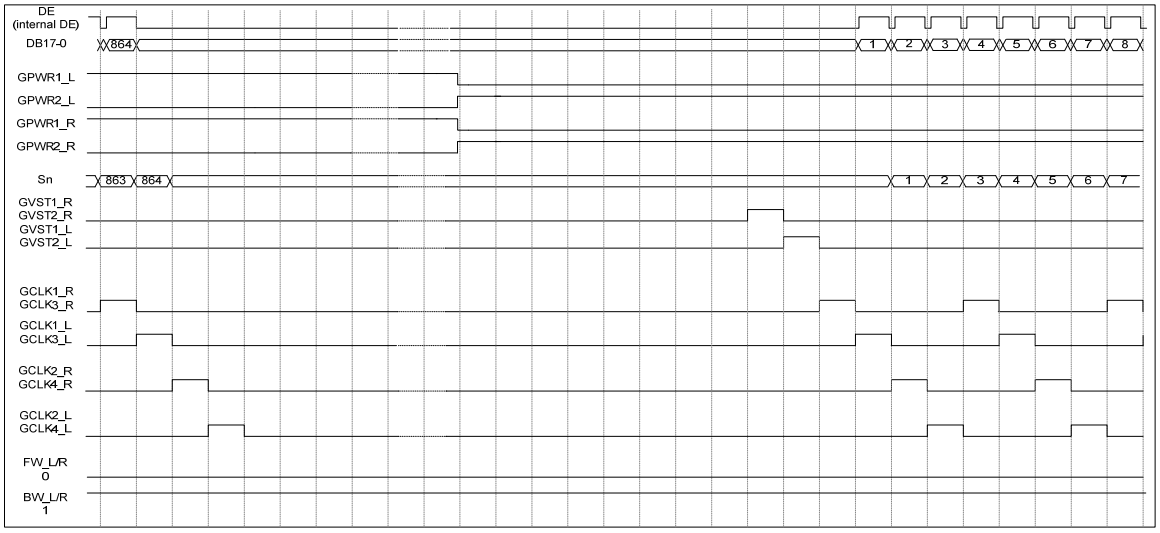


*Figure 94. Non-overlap, 4-phase, backward mode (**FHN=0, SDM=0, FV=1, FVST=0**)*

Note) GSWAP = 1 : GCLK2_L(4_L) ⇔GCLK1_L(3_L) Swap, GCLK1_R(3_R) ⇔GCLK2_R(4_R) Swap

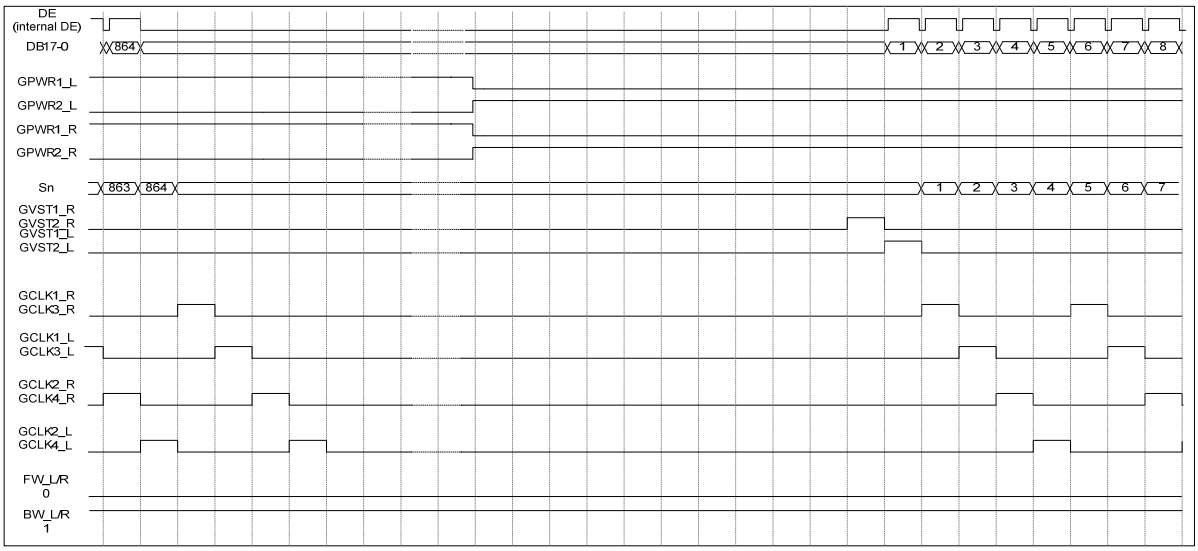


*Figure 95. Non-overlap, 4-phase, backward, advanced DE mode (**FHN=0, SDM=0, FV=1, FVST=1**)*

Note) GSWAP = 1 : GCLK2_L(4_L) ⇔GCLK1_L(3_L) Swap, GCLK1_R(3_R) ⇔GCLK2_R(4_R) Swap

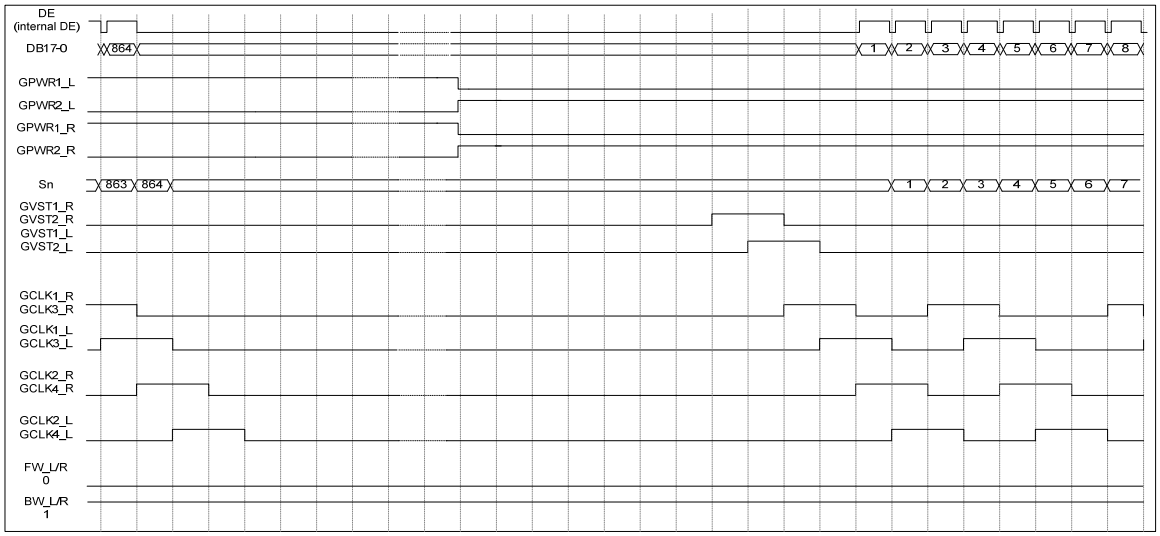


*Figure 96. Overlap, 4-phase, backward mode (**FHN=1, SDM=0, FV=1, FVST=0**)*

Note) GSWAP = 1 : GCLK2_L(4_L) ⇔GCLK1_L(3_L) Swap, GCLK1_R(3_R) ⇔GCLK2_R(4_R) Swap

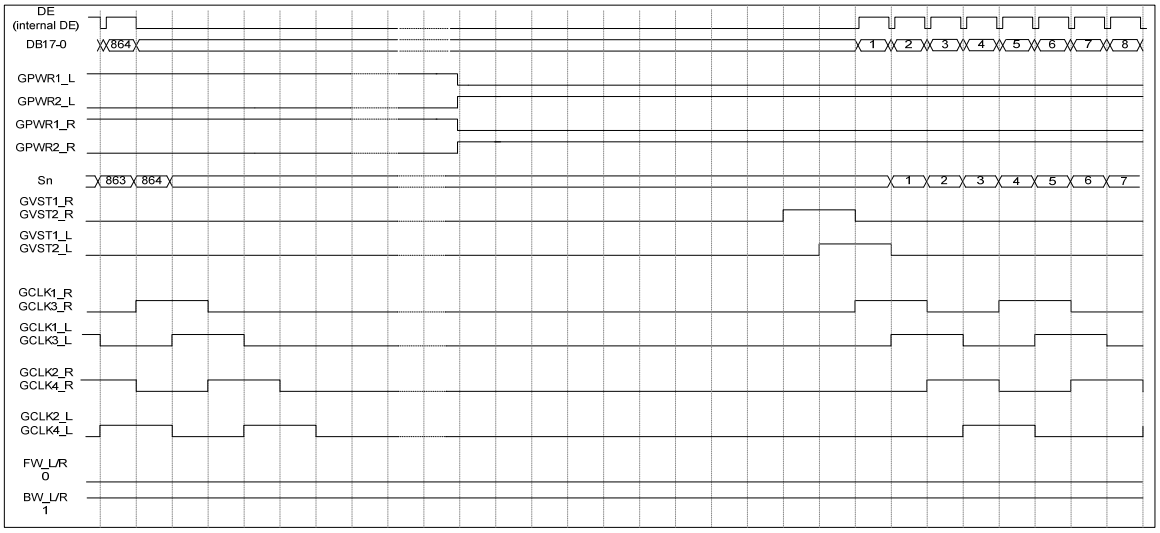


*Figure 97. Overlap, 4-phase, backward, advanced DE mode (**FHN=1, SDM=0, FV=1, FVST=1**)*

Note) GSWAP = 1 : GCLK2_L(4_L) ⇔GCLK1_L(3_L) Swap, GCLK1_R(3_R) ⇔GCLK2_R(4_R) Swap

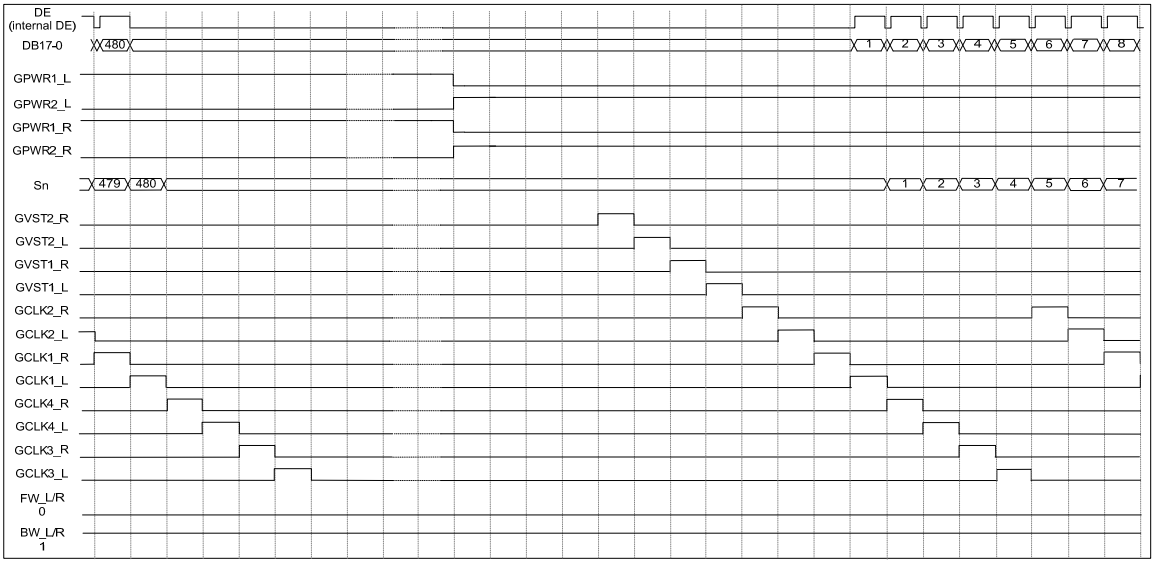


*Figure 98. Non-overlap, 8-phase, backward mode (**FHN=0, SDM=1, FV=1, FVST=0**)*

Note) GSWAP = 1 : GCLK3_L/4_L ⇔GCLK1_L/2_L Swap, GCLK3_R/4_R ⇔GCLK1_R/2_R Swap

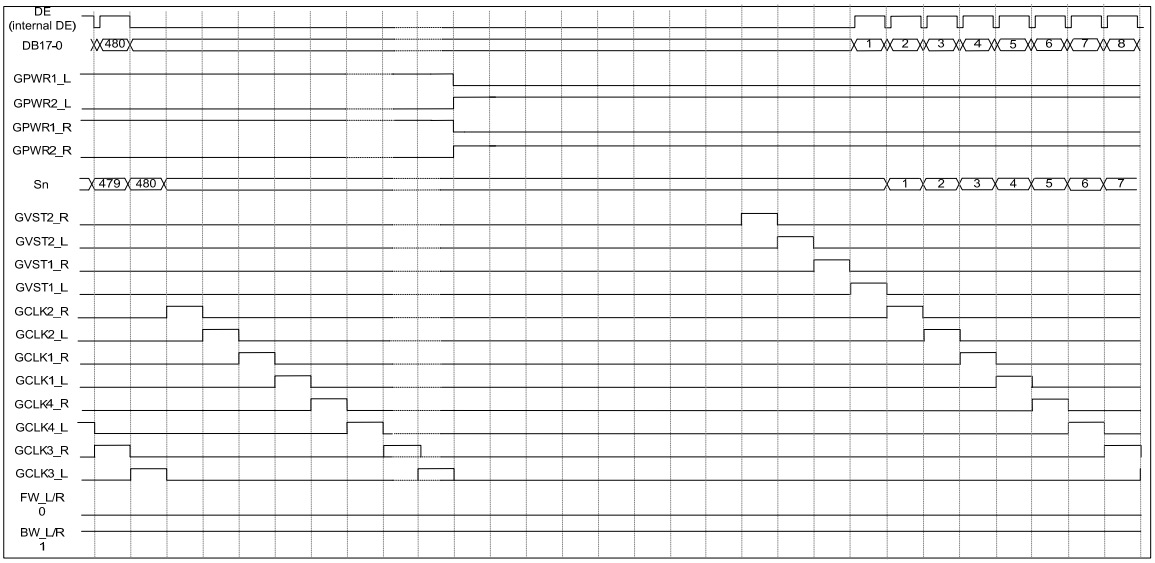


*Figure 99. Non-overlap, 8-phase, backward, advanced DE mode (**FHN=0, SDM=1, FV=1, FVST=1**)*

Note) GSWAP = 1 : GCLK3_L/4_L ⇔GCLK1_L/2_L Swap, GCLK3_R/4_R ⇔GCLK1_R/2_R Swap

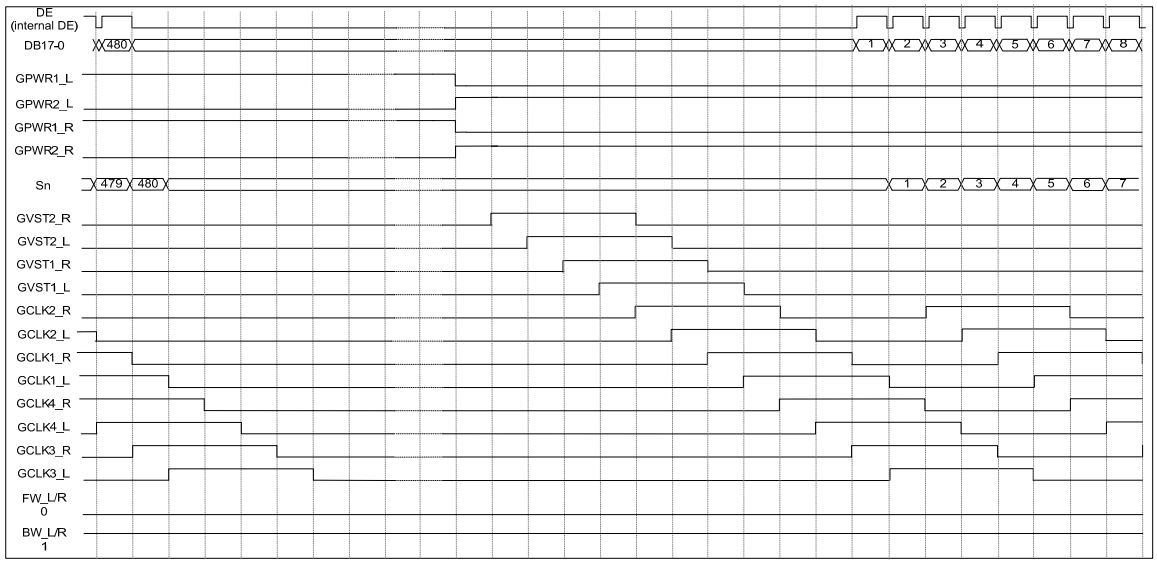


*Figure 100. Overlap, 8-phase, backward mode (**FHN=1, SDM=1, FV=1, FVST=0**)*

Note) GSWAP = 1 : GCLK3_L/4_L ⇔GCLK1_L/2_L Swap, GCLK3_R/4_R ⇔GCLK1_R/2_R Swap

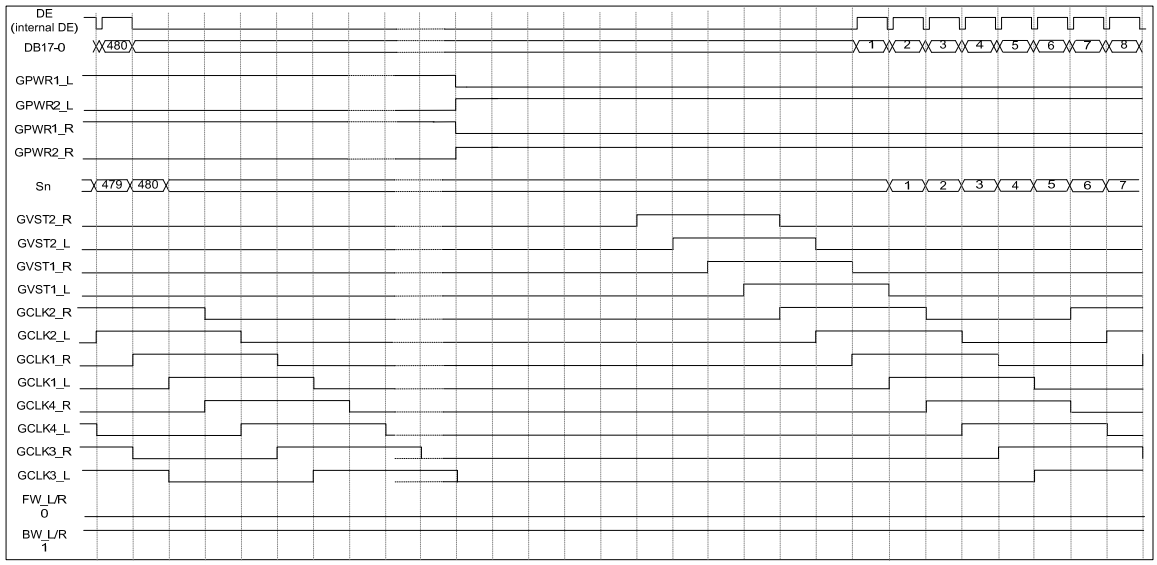


*Figure 101. Overlap, 8-phase, backward, advanced DE mode (**FHN=1, SDM=1, FV=1, FVST=1**)*

Note) GSWAP = 1 : GCLK3_L/4_L ⇔GCLK1_L/2_L Swap, GCLK3_R/4_R ⇔GCLK1_R/2_R Swap

6.2.45 B7h – Display Control 3

B7h	Display Control 3												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	1	0	1	1	0	1	1	1	B7h
1st parameter	1	#A	#B	X	RTN[7:0]								46h
2nd parameter	1	#A	#B	X	FP[7:0]								06h
3rd parameter	1	#A	#B	X	BP[7:0]								0Ch
4th parameter	1	#A	#B	X						DIV[1:0]			00h
5th parameter	1	#A	#B	X					TEI[2:0]				00h

Description

Write #A="1" #B="↑"
Read #A="↑" #B=" 1" & Insert dummy read

RTN[7:0] – Sets 1H (line) period. This setting is enabled while the LG4572B's display operation is synchronized with internal clock. RTN[7:0] should be greater than or equal to 70 (=46h).

RTN[7:0]	Clock per Line
8'h00 – 8'h45	Setting disabled
8'h46	70 clocks
8'h47	71 clocks
8'h48	72 clocks
:	:
8'hFC	252 clocks
8'hFE	254 clocks
8'hFF	255 clocks

BP[7:0], FP[7:0] – These parameters define the retrace period (i.e. front and back porches) which appears before and after the display area. FP[7:0] bits define number of front porch lines while BP[7:0] bits define number of back porch lines.

Description

BP[7:0] / FP[7:0]	Number of lines for the back/front porches
8'h0	Setting disabled
8'h1	Setting disabled
8'h2	2 lines
8'h3	3 lines
8'h4	4 lines
:	:
8'hFD	253 lines
8'hFE	254 lines
8'hFF	255 lines

DIV[1:0] – Sets the division ratio of the internal clock frequency. The LG4572B's internal operation is synchronized with the frequency divided display clock. When changing the DIV[1:0] bits, the width of the reference clock for liquid crystal panel control signals is changed. The frame frequency can be adjusted by register setting (RTN and DIV bits). When changing the number of lines to drive the liquid crystal panel, adjust the frame frequency too.

DIV[1:0]	Division Ratio	Internal operation clock unit
2'h0	1/1	1 clocks
2'h1	1/2	2 clocks
2'h2	1/4	4 clocks
2'h3	1/8	8 clocks

TEI[2:0] – Set the output interval of TE signal according to the display data rewrite cycle and data transfer rate.

TEI[2:0]	TE output interval in frames
3'h0	1 frame
3'h1	2 frames
3'h2	3 frames
:	:
3'h6	7 frames
3'h7	8 frames

6.2.46 C0h – Internal Oscillator Setting

C0h	Internal Oscillator Setting												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	1	1	0	0	0	0	0	0	C0h
1st parameter	1	#A	#B	X	0	0	0	0	0	OSC SYNC	EXT OSC	OSC	01h
2nd parameter	1	#A	#B	X	0	0	0	FRS [4:0]					00h

Description

Write #A="1" #B="↑"
Read #A="↑" #B=" 1" & Insert dummy read

LG4572B supports OSCSYNC mode, where one IC's internally generated oscillation frequency can be shared to others through OSC3 pin.

OSCSYNC – OSC Sync mode control

OSCSYNC	Description
1'h0	OCS Sync mode Enable
1'h1	OCS Sync mode Disable

LG4572B supports external OSC mode, where external R and C components are used for determining oscillation frequency in case higher frequencies than 6.28MHz are needed. In external OSC mode, internal oscillator cannot operate any more.

EXTOSC – use the external OSC

EXTOSC	Description
1'h0	Internal OSC
1'h1	External OSC

OSC – OSC control

HATLOSC	Description
1'h0	Halt OSC
1'h1	Normal Operation

FRS[4:0] – Internal oscillator frequency control.

LG4572B supports various oscillation frequencies as bellows.

FRS[4:0]	Frequency [MHz]	FRS[4:0]	Frequency [MHz]
5'h00	0.23	5'h10	3.37
5'h01	0.47	5'h11	3.56
5'h02	0.56	5'h12	3.63
5'h03	0.81	5'h13	3.79
5'h04	0.90	5'h14	3.92

	5'h05	1.15	5'h15	4.08
	5'h06	1.24	5'h16	4.17
	5'h07	1.45	5'h17	4.31
	5'h08	1.66	5'h18	4.57
	5'h09	1.87	5'h19	4.71
	5'h0A	1.95	5'h1A	4.79
	5'h0B	2.15	5'h1B	4.92
	5'h0C	2.27	5'h1C	5.09
	5'h0D	2.47	5'h1D	5.21
	5'h0E	2.56	5'h1E	5.28
	5'h0F	2.74	5'h1F	5.40

6.2.47 C1h – Power Control 1

C1h	Power Control 1(Power State Selection)												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	1	1	0	0	0	0	0	1	C1h
1st parameter	1	#A	#B	X	0	0	0	0	DTE	0	STB	DSTB	02h

Description

Write #A="1" #B="↑"
Read #A="↑" #B=" 1" & Insert dummy read

DSTB – When DSTB = 1, the LGD4572B enters the deep standby mode. In deep standby mode, the internal logic power supply is turned off to reduce power consumption. In the Deep Standby mode, data stored in the Instructions are not retained. Rewrite them after the Deep Standby mode is exited.

DSTB	Description
1'h0	Normal operation
1'h1	Deep Standby mode.

STB – When STB = "1", the LG4572B enters the standby mode. In standby mode, the display operation completely halts, and the internal operation, including internal RC oscillation and reception of external clock pulses, completely halts. Only instructions to release the LG4572B from the standby mode (STB = "0") and to start oscillators are accepted during the standby mode. To set the standby mode, follow the sequence of standby mode setting.

STB	Description
1'h0	Normal operation
1'h1	Standby mode

DTE – Manual gate output enable

DTE	Description
1'h0	Gate output Disable
1'h1	Gate output Enable

6.2.48 C2h – Power Control 2

C2h	Power Control 2(Manual Step-up Circuit Enable)												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	1	1	0	0	0	0	1	0	C2h
1st parameter	1	#A	#B	X	0	0	LVGL	VDL	VCL	VGL	VGH	VDH	00h

Description

Write #A="1" #B="↑"
Read #A="↑" #B=" 1" & Insert dummy read

VDH – Enable the operation Switching Regulator to generate DDVDH.

VDH	Description
1'h0	DDVDH OFF
1'h1	DDVDH ON

VDL – Enable the operation to generate DDVDL.

VDL	Description
1'h0	DDVDL OFF
1'h1	DDVDL ON

VCL – Enable the operation to generate VCL.

VCL	Description
1'h0	VCL OFF
1'h1	VCL ON

VGL – Enable the operation to generate VGL.

VGL	Description
1'h0	VGL OFF
1'h1	VGL ON

VGH – Enable the operation to generate VGH.

VGH	Description
1'h0	VGH OFF
1'h1	VGH ON

	LVGL – Enable the operation to generate LVGL.

LVGL	Description
1'h0	LVGL OFF
1'h1	LVGL ON

6.2.49 C3h – Power Control 3

C3h	Power Control 3(Step-up Circuit Control)												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	1	1	0	0	0	0	1	1	C3h
1st parameter	1	#A	#B	X	0	0	0	0	0	STMODE[2:0]			00h
2nd parameter	1	#A	#B	X	0	0	0	0	0	DC1[2:0]			04h
3rd parameter	1	#A	#B	X	0	0	0	0	0	DC2[2:0]			03h
4th parameter	1	#A	#B	X	0	0	0	0	0	DC3[2:0]			03h
5th parameter	1	#A	#B	X	0	0	0	0	0	DCPFM[2:0]			04h

Description

Write #A="1" #B="↑"
Read #A="↑" #B=" 1" & Insert dummy read

STMODE [2:0] – These bits set the step-up auto power generation modes. 1~3 are for H-type panel and 5~7 are for L-type panel. 0 and 4 are for manual power generation settings.

STMODE [2:0]	DDVDH circuit	DDVDL circuit	Power Setting
3'h0	Manual	Manual	Manual
3'h1	External DDVDH	STEP-UP3	Auto
3'h2	PFM Boosting	STEP-UP3	Auto
3'h3	PFM Boosting	Diode inverting	Auto
3'h4	Manual	Manual	Manual
3'h5	External DDVDH	STEP-UP3	Auto
3'h6	PFM Boosting	STEP-UP3	Auto
3'h7	PFM Boosting	Diode inverting	Auto

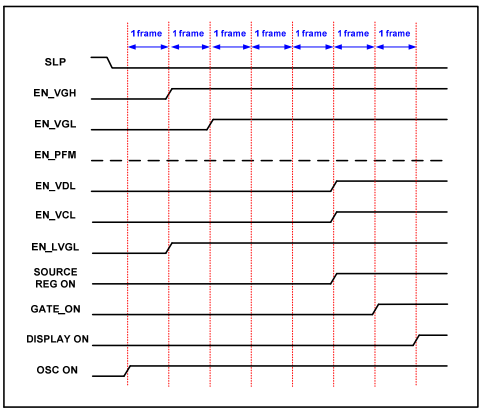
DC1[2:0] – These bits set the step-up clock frequency of the step-up circuit 2.

DC1[2:0]	Step-up circuit 2 : step-up frequency (fDCDC2)	
	OSC = 1	OSC = 0
3'h0	fosc/8	fpclk / 64
3'h1	fosc/16	fpclk / 128
3'h2	fosc/32	fpclk / 256
3'h3	fosc/64	fpclk / 512
3'h4	fosc/128	fpclk / 1024

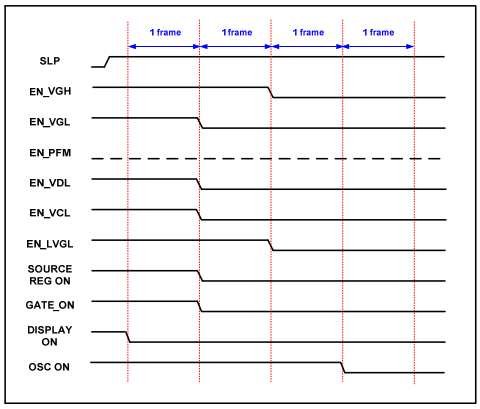
	3'h5	fosc/256	fpclk / 2048
	3'h6	fosc/512	fpclk / 4096
	3'h7	Setting disable	Setting disable
	DC2[2:0] – These bits set the step-up clock frequency of the step-up circuit 3.		
	DC2[2:0]	**Step-up circuit 3 : step-up frequency (fDCDC3)**	
		OSC = 1	**OSC = 0**
	3'h0	fosc/8	fpclk / 64
	3'h1	fosc/16	fpclk / 128
	3'h2	fosc/32	fpclk / 256
	3'h3	fosc/64	fpclk / 512
	3'h4	fosc/128	fpclk / 1024
	3'h5	fosc/256	fpclk / 2048
	3'h6	fosc/512	fpclk / 4096
	3'h7	Setting disable	Setting disable
	DC3[2:0] – These bits set the step-up clock frequency of the step-up circuit 4.		
	DC3[2:0]	**Step-up circuit 4 : step-up frequency (fDCDC4)**	
		OSC = 1	**OSC = 0**
	3'h0	fosc/8	fpclk / 64
	3'h1	fosc/16	fpclk / 128
	3'h2	fosc/32	fpclk / 256
	3'h3	fosc/64	fpclk / 512
	3'h4	fosc/128	fpclk / 1024
	3'h5	fosc/256	fpclk / 2048
	3'h6	fosc/512	fpclk / 4096
	3'h7	Setting disable	Setting disable
	DCPFM[2:0] – These bits set the step-up clock frequency of the PFM circuit.		
	DCPFM[2:0]	**PFM circuit : step-up frequency (fDCDC_PFM)**	
		OSC = 1	**OSC = 0**
	3'h0	Setting disabled	fpclk / 4
	3'h1	Setting disabled	fpclk / 6
	3'h2	fosc/1	fpclk / 8
	3'h3	Setting disabled	fpclk / 12
	3'h4	Fosc/2	fpclk / 16
	3'h5	Setting disabled	fpclk / 24

	3'h6	fosc/4	fpclk / 32
	3'h7	Setting disabled	fpclk / 48
	The followings are for understanding the operations of each auto power generation modes.		

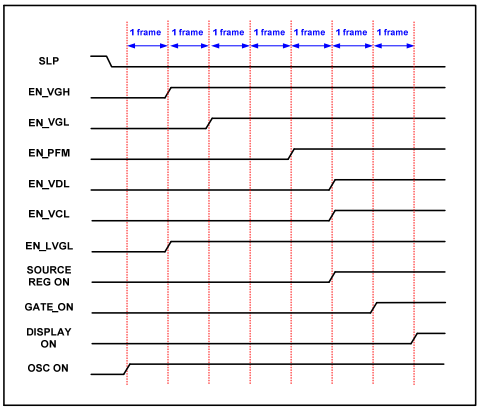
Restriction



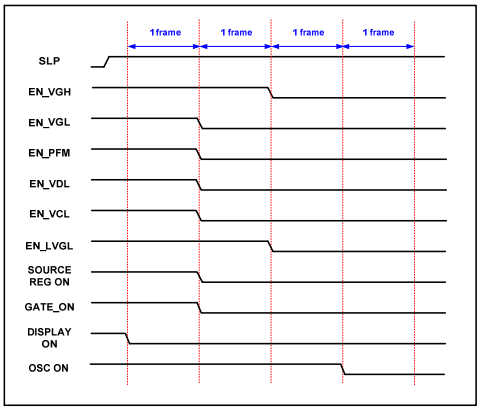
Power ON
STMODE[2:0]=1h



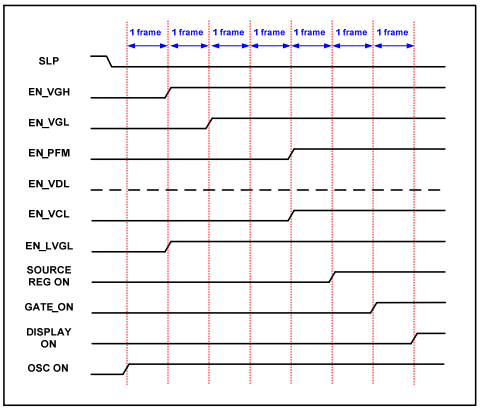
Power OFF
STMODE[2:0]=1h



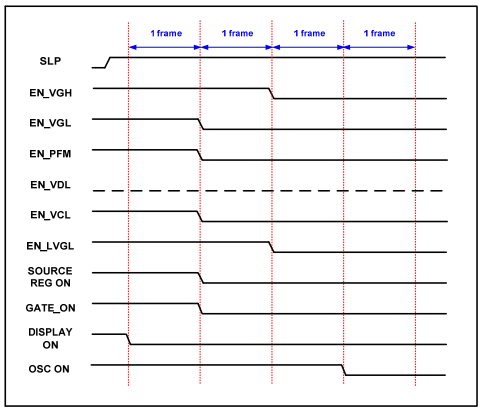
Power ON
STMODE[2:0]=2h



Power OFF
STMODE[2:0]=2h

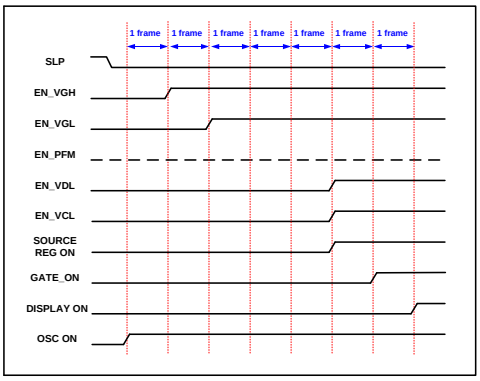


Power ON
STMODE[2:0]=3h

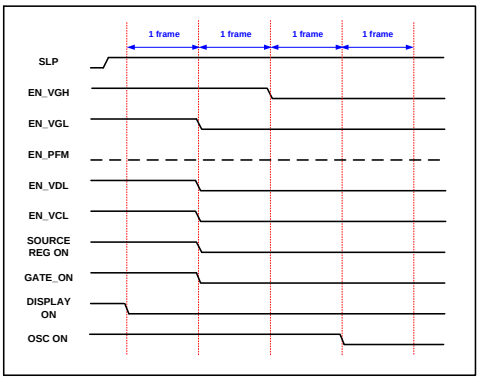


Power OFF
STMODE[2:0]=3h

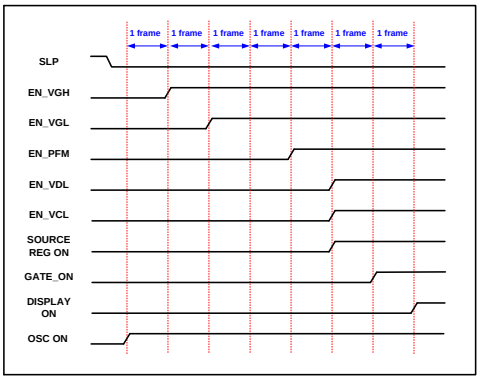
Restriction



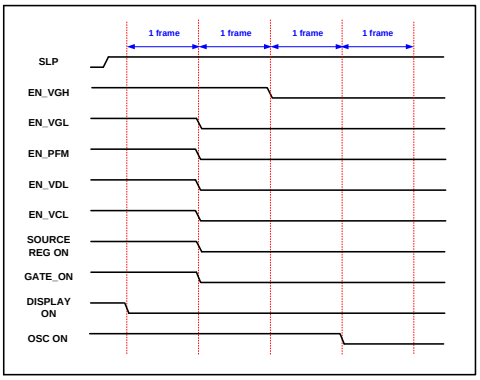
Power ON
STMODE[2:0]=5h



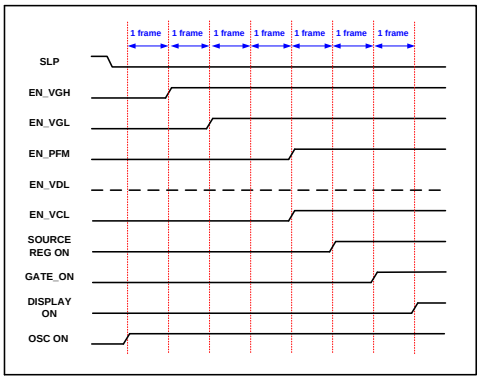
Power OFF
STMODE[2:0]=5h



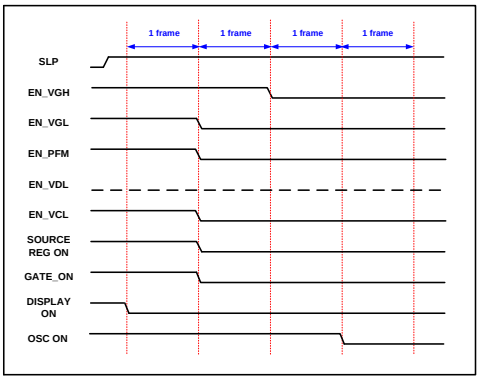
Power ON
STMODE[2:0]=6h



Power OFF
STMODE[2:0]=6h



Power ON
STMODE[2:0]=7h



Power OFF
STMODE[2:0]=7h

6.2.50 C4h – Power Control 4

C4h	Power Control 4(Regulator Control)												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	1	1	0	0	0	1	0	0	C4h
1st parameter	1	#A	#B	X	0	0	OPB	BMB	0	BDC [2:0]			00h
2nd parameter	1	#A	#B	X	0	GDC[2:0]			0	AP[2:0]			00h
3rd parameter	1	#A	#B	X	0	0	0	VRH1[4:0]					00h
4th parameter	1	#A	#B	X	0	0	0	VRH2[4:0]					00h
5th parameter	1	#A	#B	X	0	0	0	REGPD	0	BT[2:0]			05h
6th parameter	1	#A	#B	X	0	VBS [2:0]			VREFS [3:0]				0Bh

Description

Write #A="1" #B="↑"
Read #A="↑" #B=" 1" & Insert dummy read

OPB – Normal & Buffered Bias Selection

OPB	Channel Amp bias
1'h0	Buffered Bias
1'h1	Normal Bias

BMB – Bias Line Current Adjustment.

BMB	Line Current
1'h0	2
1'h1	1

BDC[2:0] – Channel Amp Quiescent current adjustment.

BDC[2:0]	Channel Amp bias
3'h0	Channel Amp halt
3'h1	0.5
3'h2	1
3'h3	1.5
3'h4	2
3'h5	2.5
3'h6	3
3'h7	3.5

GDC[2:0] – Gray-Scale Amp Quiescent Adjustment

GDC[2:0]	Gray Amp bias
3'h0	Gray AMP halt
3'h1	0.5
3'h2	1
3'h3	1.5
3'h4	2
3'h5	2.5
3'h6	3
3'h7	4.5

AP[2:0] – Adjusts the constant current in the operational amplifier circuit in the LCD power supply circuit.

AP[2:0]	Bias of regulator
3'h0	Halt
3'h1	0.25
3'h2	0.5
3'h3	0.75
3'h4	1
3'h5	1.25
3'h6	1.5
3'h7	1.75

VRH1[4:0] – Set the VREG1OUT output level , which is a reference level for the grayscale voltage level.

VRH1[4:0]	Vreg1out Level	VRH1[4:0]	Vreg1out Level
5'h00	Halt (Vreg1out =Hiz)	5'h10	VCI x 1.533
5'h01	VCI x 1.133	5'h11	VCI x 1.56
5'h02	VCI x 1.16	5'h12	VCI x 1.587
5'h03	VCI x 1.187	5'h13	VCI x 1.613
5'h04	VCI x 1.213	5'h14	VCI x 1.64
5'h05	VCI x 1.24	5'h15	VCI x 1.667
5'h06	VCI x 1.267	5'h16	VCI x 1.693
5'h07	VCI x 1.293	5'h17	VCI x 1.72
5'h08	VCI x 1.32	5'h18	VCI x 1.747
5'h09	VCI x 1.347	5'h19	VCI x 1.773
5'h0A	VCI x 1.373	5'h1A	VCI x 1.8
5'h0B	VCI x 1.4	5'h1B	VCI x 1.827
5'h0C	VCI x 1.427	5'h1C	VCI x 1.853
5'h0D	VCI x 1.453	5'h1D	VCI x 1.88
5'h0E	VCI x 1.48	5'h1E	VCI x1.907
5'h0F	VCI x 1.507	5'h1F	VCI x 1.933

VRH2[4:0] – Set the VREG2OUT output level , which is a reference level for the grayscale voltage.

VRH2[4:0]	Vreg2out Level	VRH2[4:0]	Vreg2out Level
5'h00	Halt (Vreg2out =Hiz)	5'h10	VCI x - 1.533
5'h01	VCI x - 1.133	5'h11	VCI x - 1.56
5'h02	VCI x - 1.16	5'h12	VCI x - 1.587
5'h03	VCI x - 1.187	5'h13	VCI x - 1.613
5'h04	VCI x - 1.213	5'h14	VCI x - 1.64
5'h05	VCI x - 1.24	5'h15	VCI x - 1.667
5'h06	VCI x - 1.267	5'h16	VCI x - 1.693
5'h07	VCI x - 1.293	5'h17	VCI x - 1.72
5'h08	VCI x - 1.32	5'h18	VCI x - 1.747
5'h09	VCI x - 1.347	5'h19	VCI x - 1.773
5'h0A	VCI x - 1.373	5'h1A	VCI x - 1.8
5'h0B	VCI x - 1.4	5'h1B	VCI x - 1.827
5'h0C	VCI x - 1.427	5'h1C	VCI x - 1.853
5'h0D	VCI x - 1.453	5'h1D	VCI x - 1.88
5'h0E	VCI x - 1.48	5'h1E	VCI x - 1.907
5'h0F	VCI x - 1.507	5'h1F	VCI x - 1.933

REGPD – Regulator Power down.

BT[2:0] – Changes the rate applied to the step-up circuit. Adjust the step-up rate according to the voltage in use. To reduce current consumption, set a smaller step-up rate.

BT[2:0]	DDVDH	DDVDL	VGH	VGL	Capacitor connection Pins
3'h0	VCI x 2 [x 2]	-(VCI x 2) [x 2]	DDVDH x 3[x 6]	–(DDVDH x 3) [x –6]	Application circuit C21 not use
3'h1				–(VCI+ DDVDH x 2) [x –5]	Application circuit
3'h2				–(DDVDH x 2) [x –4]	Application circuit
3'h3			VCI + DDVDH x 2 [x 5]	–(DDVDH x 3) [x –6]	Application circuit C21 not use
3'h4				–(VCI+ DDVDH x 2) [x –5]	Application circuit
3'h5				–(DDVDH x 2) [x –4]	Application circuit
3'h6			DDVDH x 2[x 4]	–(VCI+DDVDH x 2) [x –5]	Application circuit
3'h7				–(DDVDH x 2) [x –4]	Application circuit

Notes:

1. The step-up rate from the VCI level is shown in the bracket [ ] in the above table.
2. When using the DDVDH, DDVDL, VCL, VGH and VGL voltage levels, connect a capacitor to each capacitor connection pin.
   Set the following voltages within the limits: DDVDH = max 6V, VCL = min –3V, VGH = max 18V, VGL = min –18V

VBS[2:0] – Set the VBIAS level. The VBS bits can set the VBIAS level 1.3 to 1.9 times the VCI level.

VBS[2:0]	VBIAS
3'h0	Halt
3'h1	VCI x 1.3
3'h2	VCI x 1.36
3'h3	VCI x 1.44
3'h4	VCI x 1.5
3'h5	VCI x 1.56
3'h6	VCI x 1.64
3'h7	VCI x 1.9

VREFS[3:0] – Selects the reference voltage of the switching regulator citcuit. Adjust the reference voltage according to the VCI voltage in use. The output voltage of the switching regulator is four times of the reference voltage.

VREFS[3:0]	DDVDH voltage	VREFS[3:0]	DDVDH voltage
4'h0	VCI x 2.45	4'h8	VCI x 2.05
4'h1	VCI x 2.4	4'h9	VCI x 2.0
4'h2	VCI x 2.35	4'hA	VCI x 1.95
4'h3	VCI x 2.3	4'hB	VCI x 1.9
4'h4	VCI x 2.25	4'hC	VCI x 1.85
4'h5	VCI x 2.2	4'hD	VCI x 1.8
4'h6	VCI x 2.15	4'hE	VCI x 1.75
4'h7	VCI x 2.1	4'hF	VCI x 1.7

6.2.51 C5h – Power Control 5

C5h	Power Control 5(VCOM Control)												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	1	1	0	0	0	1	0	1	C5h
1st parameter	1	#A	#B	X	0	VCM [6:0]							00h

Description

Write #A="1" #B="↑"
Read #A="↑" #B=" 1" & Insert dummy read

Note : Set the VCOML voltage from VREG2OUT level to 0V

VCM[6:0] – Sets the VCOM level . VCM[6:0] specifies the voltage by VREG2OUT x n, where n can change from 0.1 to 1 as shown in below table. To halt internal setting and adjust VCOM through VCOMR pad, set VCM[6:0] = "1111111". Then, VCOM level follows VCOMR level.

VCM [6:0]	VCOM	VCM [6:0]	VCOM	VCM [6:0]	VCOM	VCM [6:0]	VCOM
7'h00	Halt(VCOM=GND)	7'h20	VREG2OUT x 0.779	7'h40	VREG2OUT x 0.550	7'h60	VREG2OUT x 0.321
7'h01	VREG2OUT x 1	7'h21	VREG2OUT x 0.771	7'h41	VREG2OUT x 0.543	7'h61	VREG2OUT x 0.314
7'h02	VREG2OUT x 0.993	7'h22	VREG2OUT x 0.764	7'h42	VREG2OUT x 0.536	7'h62	VREG2OUT x 0.307
7'h03	VREG2OUT x 0.986	7'h23	VREG2OUT x 0.757	7'h43	VREG2OUT x 0.529	7'h63	VREG2OUT x 0.3
7'h04	VREG2OUT x 0.979	7'h24	VREG2OUT x 0.750	7'h44	VREG2OUT x 0.521	7'h64	VREG2OUT x 0.293
7'h05	VREG2OUT x 0.971	7'h25	VREG2OUT x 0.743	7'h45	VREG2OUT x 0.514	7'h65	VREG2OUT x 0.286
7'h06	VREG2OUT x 0.964	7'h26	VREG2OUT x 0.736	7'h46	VREG2OUT x 0.507	7'h66	VREG2OUT x 0.279
7'h07	VREG2OUT x 0.957	7'h27	VREG2OUT x 0.729	7'h47	VREG2OUT x 0.5	7'h67	VREG2OUT x 0.271
7'h08	VREG2OUT x 0.950	7'h28	VREG2OUT x 0.721	7'h48	VREG2OUT x 0.493	7'h68	VREG2OUT x 0.264
7'h09	VREG2OUT x 0.943	7'h29	VREG2OUT x 0.714	7'h49	VREG2OUT x 0.486	7'h69	VREG2OUT x 0.257
7'h0A	VREG2OUT x 0.936	7'h2A	VREG2OUT x 0.707	7'h4A	VREG2OUT x 0.479	7'h6A	VREG2OUT x 0.250
7'h0B	VREG2OUT x 0.929	7'h2B	VREG2OUT x 0.7	7'h4B	VREG2OUT x 0.471	7'h6B	VREG2OUT x 0.243
7'h0C	VREG2OUT x 0.921	7'h2C	VREG2OUT x 0.693	7'h4C	VREG2OUT x 0.464	7'h6C	VREG2OUT x 0.236
7'h0D	VREG2OUT x 0.914	7'h2D	VREG2OUT x 0.686	7'h4D	VREG2OUT x 0.457	7'h6D	VREG2OUT x 0.229
7'h0E	VREG2OUT x 0.907	7'h2E	VREG2OUT x 0.679	7'h4E	VREG2OUT x 0.450	7'h6E	VREG2OUT x 0.221
7'h0F	VREG2OUT x 0.9	7'h2F	VREG2OUT x 0.671	7'h4F	VREG2OUT x 0.443	7'h6F	VREG2OUT x 0.214
7'h10	VREG2OUT x 0.893	7'h30	VREG2OUT x 0.664	7'h50	VREG2OUT x 0.436	7'h70	VREG2OUT x 0.207
7'h11	VREG2OUT x 0.886	7'h31	VREG2OUT x 0.657	7'h51	VREG2OUT x 0.429	7'h71	VREG2OUT x 0.2
7'h12	VREG2OUT x 0.879	7'h32	VREG2OUT x 0.650	7'h52	VREG2OUT x 0.421	7'h72	VREG2OUT x 0.193
7'h13	VREG2OUT x 0.871	7'h33	VREG2OUT x 0.643	7'h53	VREG2OUT x 0.414	7'h73	VREG2OUT x 0.186
7'h14	VREG2OUT x 0.864	7'h34	VREG2OUT x 0.636	7'h54	VREG2OUT x 0.407	7'h74	VREG2OUT x 0.179
7'h15	VREG2OUT x 0.857	7'h35	VREG2OUT x 0.629	7'h55	VREG2OUT x 0.4	7'h75	VREG2OUT x 0.171
7'h16	VREG2OUT x 0.850	7'h36	VREG2OUT x 0.621	7'h56	VREG2OUT x 0.393	7'h76	VREG2OUT x 0.164
7'h17	VREG2OUT x 0.843	7'h37	VREG2OUT x 0.614	7'h57	VREG2OUT x 0.386	7'h77	VREG2OUT x 0.157
7'h18	VREG2OUT x 0.836	7'h38	VREG2OUT x 0.607	7'h58	VREG2OUT x 0.379	7'h78	VREG2OUT x 0.150
7'h19	VREG2OUT x 0.829	7'h39	VREG2OUT x 0.6	7'h59	VREG2OUT x 0.371	7'h79	VREG2OUT x 0.143
7'h0A	VREG2OUT x 0.821	7'h3A	VREG2OUT x 0.593	7'h5A	VREG2OUT x 0.364	7'h7A	VREG2OUT x 0.136

	7'h0B	VREG2OUT x 0.814	7'h3B	VREG2OUT x 0.586	7'h5B	VREG2OUT x 0.357	7'h7B	VREG2OUT x 0.129
	7'h0C	VREG2OUT x 0.807	7'h3C	VREG2OUT x 0.579	7'h5C	VREG2OUT x 0.350	7'h7C	VREG2OUT x 0.121
	7'h0D	VREG2OUT x 0.8	7'h3D	VREG2OUT x 0.571	7'h5D	VREG2OUT x 0.343	7'h7D	VREG2OUT x 0.114
	7'h0E	VREG2OUT x 0.793	7'h3E	VREG2OUT x 0.564	7'h5E	VREG2OUT x 0.336	7'h7E	VREG2OUT x 0.107
	7'h0F	VREG2OUT x 0.786	7'h3F	VREG2OUT x 0.557	7'h5F	VREG2OUT x 0.329	7'h7F	VCOMR

6.2.52 C6h – Power Control 6

C6h	Power Control 6(VDD Regulator Control)												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	1	1	0	0	0	1	1	0	C6h
1st parameter	1	#A	#B	X	0	RI[2:0]			0	RV [2:0]			23h
2nd parameter	1	#A	#B	X	0	RESET [2:0]			0	RCONT [2:0]			40h

Description

Write #A="1" #B="↑"
Read #A="↑" #B=" 1" & Insert dummy read

RI[2:0] – These bits control the bias current of internal logic regulator.

RI[2:0]	Logic regulator bias current
3'h0	x 0.2
3'h1	x 1
3'h2	x 2
3'h3	x 3
3'h4	x 3
3'h5	x 4
3'h6	x 5
3'h7	x 6

RV[2:0] – These bits control the output voltage of internal logic regulator.

RV[2:0]	VDD Voltage
3'h0	VCI x 0.60
3'h1	VCI x 0.575
3'h2	VCI x 0.55
3'h3	VCI x 0.525
3'h4	VCI x 0.50
3'h5	VCI x 0.474
3'h6	VCI x 0.45
3'h7	VCI x 0.425

RESET[2:0] – These bits control the main bias.

RESET[2:0]	Main bias current
3'h0	x 0.39
3'h1	x 0.43
3'h2	x 0.48
3'h3	x 0.56
3'h4	x 0.65
3'h5	x 0.79
3'h6	x 1.00 (default)
3'h7	x 1.36

RCONT[2:0] – These bits control the input voltage of main bias op_amp.

RCONT[2:0]	Main bias voltage
3'h0	VCI x 0.25
3'h1	Setting disabled
3'h2	Open
3'h3	VCI x 0.30
3'h4	Setting disabled
3'h5	Setting disabled
3'h6	VCI x 0.20
3'h7	Setting disabled

6.2.53 C7h Offset Cancelling Control

C7h	Source Channel Amp Offset Cancelling Control (See note below)												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	1	1	0	0	0	1	1	1	C7h
1st parameter	1	#A	#B	X	0	0	0	0	0	0	0	OFCEN	00h
2nd parameter	1	#A	#B	X	OFCTSW[7:0]								30h
3rd parameter	1	#A	#B	X	OFCTD2 [3:0]				OFCTD1 [3:0]				10h

Description

Write #A="1" #B="↑"
Read #A="↑" #B=" 1" & Insert dummy read

OFCEN – Offset cancelling enable/disable

OFCEN	Offset Cancelling
1'h0	Offset canceling disable
1'h1	Offset canceling enable

OFCTSW[6:0] – Set the offset sampling period.

OFCTSW[7:0]	Offset sampling period
7'h00	0
7'h01	1 x PCLK
7'h02	2 x PCLK
7'h03	3 x PCLK
⋮	⋮
⋮	⋮
7'hFC	252 x PCLK
7'hFD	253 x PCLK
7'hFE	254 x PCLK
7'hFF	255 x PCLK

OFCTD1[3:0] – Set the delay of the offset sampling start

OFCTD1[3:0]	Delay of the offset sampling start	OFCTD1[3:0]	Delay of the offset sampling start
4'h0	0	4'h8	8 x PCLK
4'h1	1 x PCLK	4'h9	9 x PCLK
4'h2	2 x PCLK	4'hA	10 x PCLK
4'h3	3 x PCLK	4'hB	11 x PCLK
4'h4	4 x PCLK	4'hC	12 x PCLK
4'h5	5 x PCLK	4'hD	13 x PCLK
4'h6	6 x PCLK	4'hE	14 x PCLK
4'h7	7 x PCLK	4'hF	15 x PCLK

~~OFCTD2[3:0]~~ ~~Set the delay between offset sampling period and compensating period~~

~~OFCTD2[3:0]~~		**~~OFCTD2[3:0]~~**	
~~4'h0~~	~~0~~	~~4'h8~~	~~8 x PCLK~~
~~4'h1~~	~~1 x PCLK~~	~~4'h9~~	~~9 x PCLK~~
~~4'h2~~	~~2 x PCLK~~	~~4'hA~~	~~10 x PCLK~~
~~4'h3~~	~~3 x PCLK~~	~~4'hB~~	~~11 x PCLK~~
~~4'h4~~	~~4 x PCLK~~	~~4'hC~~	~~12 x PCLK~~
~~4'h5~~	~~5 x PCLK~~	~~4'hD~~	~~13 x PCLK~~
~~4'h6~~	~~6 x PCLK~~	~~4'hE~~	~~14 x PCLK~~
~~4'h7~~	~~7 x PCLK~~	~~4'hF~~	~~15 x PCLK~~

Note) The C7h register is recommended to use the default settings.

6.2.54 C8h – Backlight Control

C8h	Backlight Control												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	1	1	0	0	1	0	0	0	C8h
1st parameter	1	#A	#B	X	CDSP[3:0]				CDMP[3:0]				82h
2nd parameter	1	#A	#B	X	PWMP	0	0	0	0	0	FPWM[1:0]		01h

Description

Write #A="1" #B="↑"
Read #A="↑" #B=" 1" & Insert dummy read

CDSP[3:0] – Dimming control of still image.

CDSP[3:0]	Dimming Control Step	CDSP[3:0]	Dimming Control Step
4'h0	0	4'h8	8
4'h1	1	4'h9	9
4'h2	2	4'hA	10
4'h3	3	4'hB	11
4'h4	4	4'hC	12
4'h5	5	4'hD	13
4'h6	6	4'hE	14
4'h7	7	4'hF	15

CDMP[3:0] – Dimming control of moving image.

CDMP[3:0]	Dimming Control Step	CDMP[3:0]	Dimming Control Step
4'h0	0	4'h8	8
4'h1	1	4'h9	9
4'h2	2	4'hA	10
4'h3	3	4'hB	11
4'h4	4	4'hC	12
4'h5	5	4'hD	13
4'h6	6	4'hE	14
4'h7	7	4'hF	15

PWMP – PWM output polarity.

PWMP	PWMP polarity
0	Active High
1	Active Low

FPWM[1:0] – PWM frequency setting.

FPWM[1:0]	PWM frequency
2'h0	Frame frequency x 2
2'h1	Frame frequency x 4
2'h2	Frame frequency x 8
2'h3	Frame frequency x 16

6.2.55 D0h – Positive Gamma Curve for Red

Mnemonic RGAMMAP

Type Read/Write

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	-	PKP1[2:0]			-	PKP0[2:0]			00h
2	-	PKP3[2:0]			-	PKP2[2:0]			00h
3	-	PKP5[2:0]			-	PKP4[2:0]			00h
4	-	PRP1[2:0]			-	PRP0[2:0]			00h
5	-	-	-	VRP0[4:0]					00h
6	-	-	-	VRP1[4:0]					00h
7	-	PFP1[2:0]			-	PFP0[2:0]			00h
8	-	PFP3[2:0]			-	PFP2[2:0]			00h
9	-	-	-	-	-	PMP[2:0]			00h

Description

PKP0-5[2:0] – Gamma fine-adjustment register for positive polarity

PRP0-1[2:0] – Gamma gradient-adjustment register for positive polarity

VRP0-1[3:0] – Gamma amplitude-adjustment register for positive polarity

PFP0-3[2:0] – Gamma fine adjustment register bits for positive polarity

PMP[2:0] – Gamma fine adjustment register bits for positive polarity

For details, see "Gamma Correction Function" section.

6.2.56 D1h – Negative Gamma Curve for Red

Mnemonic RGAMMAN

Type Read/Write

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	-	PKN1[2:0]			-	PKN0[2:0]			00h
2	-	PKN3[2:0]			-	PKN2[2:0]			00h
3	-	PKN5[2:0]			-	PKN4[2:0]			00h
4	-	PRN1[2:0]			-	PRN0[2:0]			00h
5	-	-	-	VRN0[4:0]					00h
6	-	-	-	VRN1[4:0]					00h
7	-	PFN1[2:0]			-	PFN0[2:0]			00h
8	-	PFN3[2:0]			-	PFN2[2:0]			00h
9	-	-	-	-	-	PMN[2:0]			00h

Description

PKN0-5[2:0] – Gamma fine-adjustment register for negative polarity

PRN0-1[2:0] – Gamma gradient-adjustment register for negative polarity

VRN0-1[3:0] – Gamma amplitude-adjustment register for negative polarity

PFN0-3[2:0] – Gamma fine adjustment register bits for negative polarity

PMN[2:0] – Gamma fine adjustment register bits for negative polarity

For details, see "Gamma Correction Function" section.

6.2.57 D2h – Positive Gamma Curve for Green

Mnemonic GGAMMAP

Type Read/Write

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	-	PKP1[2:0]			-	PKP0[2:0]			00h
2	-	PKP3[2:0]			-	PKP2[2:0]			00h
3	-	PKP5[2:0]			-	PKP4[2:0]			00h
4	-	PRP1[2:0]			-	PRP0[2:0]			00h
5	-	-	-	VRP0[4:0]					00h
6	-	-	-	VRP1[4:0]					00h
7	-	PFP1[2:0]			-	PFP0[2:0]			00h
8	-	PFP3[2:0]			-	PFP2[2:0]			00h
9	-	-	-	-	-	PMP[2:0]			00h

Description

PKP0-5[2:0] – Gamma fine-adjustment register for positive polarity

PRP0-1[2:0] – Gamma gradient-adjustment register for positive polarity

VRP0-1[3:0] – Gamma amplitude-adjustment register for positive polarity

PFP0-3[2:0] – Gamma fine adjustment register bits for positive polarity

PMP[2:0] – Gamma fine adjustment register bits for positive polarity

For details, see "Gamma Correction Function" section.

6.2.58 D3h – Negative Gamma Curve for Green

Mnemonic GGAMMAN

Type Read/Write

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	-	PKN1[2:0]			-	PKN0[2:0]			00h
2	-	PKN3[2:0]			-	PKN2[2:0]			00h
3	-	PKN5[2:0]			-	PKN4[2:0]			00h
4	-	PRN1[2:0]			-	PRN0[2:0]			00h
5	-	-	-	VRN0[4:0]					00h
6	-	-	-	VRN1[4:0]					00h
7	-	PFN1[2:0]			-	PFN0[2:0]			00h
8	-	PFN3[2:0]			-	PFN2[2:0]			00h
9	-	-	-	-	-	PMN[2:0]			00h

Description

PKN0-5[2:0] – Gamma fine-adjustment register for negative polarity

PRN0-1[2:0] – Gamma gradient-adjustment register for negative polarity

VRN0-1[3:0] – Gamma amplitude-adjustment register for negative polarity

PFN0-3[2:0] – Gamma fine adjustment register bits for negative polarity

PMN[2:0] – Gamma fine adjustment register bits for negative polarity

For details, see "Gamma Correction Function" section.

6.2.59 D4h – Positive Gamma Curve for Blue

Mnemonic BGAMMAP

Type Read/Write

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	-	PKP1[2:0]			-	PKP0[2:0]			00h
2	-	PKP3[2:0]			-	PKP2[2:0]			00h
3	-	PKP5[2:0]			-	PKP4[2:0]			00h
4	-	PRP1[2:0]			-	PRP0[2:0]			00h
5	-	-	-	VRP0[4:0]					00h
6	-	-	-	VRP1[4:0]					00h
7	-	PFP1[2:0]			-	PFP0[2:0]			00h
8	-	PFP3[2:0]			-	PFP2[2:0]			00h
9	-	-	-	-	-	PMP[2:0]			00h

Description

PKP0-5[2:0] – Gamma fine-adjustment register for positive polarity

PRP0-1[2:0] – Gamma gradient-adjustment register for positive polarity

VRP0-1[3:0] – Gamma amplitude-adjustment register for positive polarity

PFP0-3[2:0] – Gamma fine adjustment register bits for positive polarity

PMP[2:0] – Gamma fine adjustment register bits for positive polarity

For details, see "Gamma Correction Function" section.

6.2.60 D5h – Negative Gamma Curve for Blue

Mnemonic BGAMMAN

Type Read/Write

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	-	PKN1[2:0]			-	PKN0[2:0]			00h
2	-	PKNP3[2:0]			-	PKN2[2:0]			00h
3	-	PKN5[2:0]			-	PKN4[2:0]			00h
4	-	PRN1[2:0]			-	PRN0[2:0]			00h
5	-	-	-	VRN0[4:0]					00h
6	-	-	-	VRN1[4:0]					00h
7	-	PFN1[2:0]			-	PFN0[2:0]			00h
8	-	PFN3[2:0]			-	PFN2[2:0]			00h
9	-	-	-	-	-	PMN[2:0]			00h

Description

PKN0-5[2:0] – Gamma fine-adjustment register for negative polarity

PRN0-1[2:0] – Gamma gradient-adjustment register for negative polarity

VRN0-1[3:0] – Gamma amplitude-adjustment register for negative polarity

PFN0-3[2:0] – Gamma fine adjustment register bits for negative polarity

PMN[2:0] – Gamma fine adjustment register bits for negative polarity

For details, see "Gamma Correction Function" section.

6.2.61 E0h – MDDI Control

E0h	MDDI Control												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	1	1	1	0	0	0	0	0	E0h
1st parameter	1	#A	#B	X	0	REF[2:0]			0	0	0	LPM	30h
2nd parameter	1	#A	#B	X	0	0	0	0	0	TXEMP[1:0]		TXEN	03h
3rd parameter	1	#A	#B	X	0	0	DATA0_RESET[5:0]						00h
4th parameter	1	#A	#B	X	0	0	DATA1_RESET[5:0]						04h
5th parameter	1	#A	#B	X	0	0	DATA1_OFFSET[5:0]						02h
6th parameter	1	#A	#B	X	0	0	STB_RESET[5:0]						00h

Description

Write #A="1" #B="↑"
Read #A="↑" #B=" 1" & Insert dummy read

REF[2:0] – Common mode voltage level control for TX in MDDI

REF[2:0]	TX driver common mode voltage level
2'h0	VCI x 0.33
2'h1	VCI x 0.32
2'h2	VCI x 0.31
2'h3	VCI x 0.30
2'h4	VCI x 0.29
2'h5	VCI x 0.28
2'h6	VCI x 0.27
2'h7	VCI x 0.26

LPM – Low Power Mode enable
0 : Normal Mode
1 : Low Power Mode (enabled)

TXEMP[1:0] – TX driver output overdrive

TXEMP[1:0]	TX driver output overdrive
2'h0	Normal Operation Mode (2 ㎃)
2'h1	Overdrive Mode (2.5 ㎃)
2'h2	Overdrive Mode (2.5 ㎃)
2'h3	Overdrive Mode (3 ㎃)

	TXEN – TX enable 0 : TX disabled 1 : TX enabled **DATA0_RESET[5:0]** – Set Data0 Delay Reset Value **DATA1_RESET[5:0]** – Set Data1 Delay Reset Value **DATA1_OFFSET[5:0]** – Set Data1 Delay Offset Value **STB_RESET[5:0]** – Set Strobe Delay Reset Value

6.2.62 E1h – Frame Memory Control

E1h	Frame Memory Control												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	1	1	1	0	0	0	0	1	E1h
1st parameter	1	#A	#B	X	0	0	0	0	0	0	DCMR[1:0]		02h
2nd parameter	1	#A	#B	X	0	0	0	0	0	0	0	ECC BYP	00h
3rd parameter	1	#A	#B	X	0	0	0	0	0	0	SS[2:0]		02h
4th parameter	1	#A	#B	X	0	0	0	~~OPT[4:0]~~					00h

Description

Write #A="1" #B="↑"
Read #A="↑" #B=" 1" & Insert dummy read

ECCBYP – Memory ECC bypass
0 : ECC enabled
1 : ECC bypass (Test Mode Only)

SS[2:0] – Memory LCD clock frequency selection

SS[2:0]	Memory LCD clock frequency(MHz)	
	Max	Min
3'h0	Setting disabled	Setting disabled
3'h1	Setting disabled	Setting disabled
3'h2	2.556	4.666
3'h3	2.4	4.32
3'h4	1.92	3.456
3'h5	1.5	2.592
3'h6	Setting disabled	Setting disabled
3'h7	Setting disabled	Setting disabled

DCMR[1:0] – Sets the Memory Refresh clock division ratio of the internal clock frequency.

DCMR[1:0]	Memory Refresh clock frequency
2'h0	fosc/48
2'h1	fosc/64
2'h2	fosc/96
2'h3	fosc/128

~~**OPT [4:0]** – Programmable options. Static mode only.~~

6.2.63 E2h – EEPROM READ CONTROL

E2h	EEPROM READ CONTROL												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	1	1	1	0	0	0	1	0	E2h
1st parameter	1	#A	#B	X	RFCLK[3:0]				0	0	0	EEP ROM	00h
Description	Write #A="1" #B="↑" Read #A="↑" #B=" 1" & Insert dummy read **RFCLK[3:0]** – I2C clock frequency for EEPROM reading access. It can be set from 0 to 12 and the other settings are not allowed. The equation of RSCL frequency for register reading from EEPROM is as follows. RSCLK = (Oscillator Frequency) / (16 – RFCLK)												

6.2.64 F0h – Test Register 1

F0h	Test Register 1												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	1	1	1	1	0	0	0	0	F0h
1st parameter	1	#A	#B	X	HIZ	0	0	0	0	0	TPOL[1:0]		00h
Description	Write #A="1" #B="↑" Read #A="↑" #B=" 1" & Insert dummy read **TPOL[1:0]** – LCD polarity inversion control. (Test Mode) **HIZ** – VLOUT3 and VLOUT4 outputs to Hi-Z.												

6.2.65 F1h – Test Register 2

F1h	Memory BIST Control												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	1	1	1	1	0	0	0	1	F1h
1st parameter	1	#A	#B	X						BALG[2:0]			00h
2nd parameter	1	#A	#B	X	EDTHR[7:0]								80h
3rd parameter	1	#A	#B	X	MDRT[7:0]								00h
Description	Write #A="1" #B="↑" Read #A="↑" #B=" 1" & Insert dummy read **BALG[2:0]** – BIST algorithm **EDTHR[7:0] –** Error detect threshold(test only) **MDRT[7:0]** – Memory data retention time												

6.2.66 F8h – OTP 1

F8h	OTP Programming Control												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	1	1	1	1	1	0	0	0	F8h
1st parameter	1	#A	#B	X	PTM [1:0]		0	0	PRD	PWE	VPP	PPROG	00h
2nd parameter	1	#A	#B	X	APRG	0	0	0	0	0	PA[1:0]		00h
3rd parameter	1	#A	#B	X	PDIN [7:0]								00h

Description

Write #A="1" #B="↑"
Read #A="↑" #B=" 1" & Insert dummy read

PPROG – Program mode enable.

VPP : Power switch control for the VPP pin of the embedded OTP. When VPP = "1", the internal VPP is set to 7.75V; otherwise it is set to VDD. This VPP register parameter is different from VPP in PAD.

PWE – Write enable.

PRD – Pin for power-on rest.

PTM[1:0] – Pins for enabling test mode.

PA[1:0] – Address input. This selects one of four banks of the EPROM.

PA[1:0]	Write Data Input	Write OPT Cell
2'h0	PDIN[6:0]	Cell[6:0]
2'h1	PDIN[6:0]	Cell[14:8]
2'h2	PDIN[6:0]	Cell[22:16]
2'h3	PDIN[6:0]	Cell[30:24]

APRG – Select the method of write operation

APRG	Write Operation
1'h0	Write address is PA.
1'h0	Write address is auto select address.

PDIN[7:0] – Data input.

6.2.67 F9h – OTP 2

F9h	OTP Read Control												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	1	1	1	1	1	0	0	1	F9h
1st parameter	1	#A	#B	X	VCMSEL [1:0]		0	0	0	0	RA[1:0]		

Description

Write #A="1" #B="↑"
Read #A="↑" #B=" 1" & Insert dummy read

RA[1:0] – Read address input. This selects one of four banks of the EPROM.

RA[1:0]	Read Data Input	Read OPT Cell
2'h0	PDOUT [6:0]	Cell[6:0]
2'h1	PDOUT [6:0]	Cell[14:8]
2'h2	PDOUT [6:0]	Cell[22:16]
2'h3	PDOUT[6:0]	Cell[30:24]

VCMSEL[1:0] – Sets Vcom level from either the register C5h or the EPROM.

VCMSEL[1:0]	Vcom Level adjustment
2'h0	VCM[6:0] of the register C5h
2'h1	EPROM data at first if EPROM has data. Otherwise, VCM[6:0] of the register C5h
2'h2	EPROM data selected by RA[1:0]
2'h3	EPROM data selected by RA[1:0]

6.2.68 FAh – OTP 3

FAh	Read OTP Data												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Reset
command	0	1	↑	X	1	1	1	1	1	0	1	0	FAh
1st parameter	1	#A	#B	X	PDOUT [7:0]								-
2nd parameter	1	#A	#B	X	PDOUT [15:8]								-
3rd parameter	1	#A	#B	X	PDOUT [23:16]								-
4th parameter	1	#A	#B	X	PDOUT [31:24]								-
Description	Write #A="1" #B="↑" Read #A="↑" #B=" 1" & Insert dummy read **PDOUT[31:0]** – EEPROM Read Data												

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Table 17. Absolute Maximum Ratings.

Item	Symbol	Unit	Min	Max	Notes
Power supply voltage (1)	VDD	V	-0.3	2.6	1
Power supply voltage (2)	VCC, IOVCC – GND	V	-0.3	4.5	1, 2
Power supply voltage (3)	VCI – GND	V	-0.3	4.5	1, 2
Power supply voltage (4)	DDVDH	V	-0.3	8.0	1, 3, 4
Power supply voltage (5)	VGND – VCL	V	-0.3	4.5	1
Power supply voltage (6)	VGH – AGND	V	-0.3	15	1, 5
Power supply voltage (7)	AGND – VGL (or LVGL)	V	-0.3	14.5	1, 6
Input voltage	Vt	V	-0.3	IOVCC+0.3	1
Operating temperature	Topr	°C	-40	85	1, 7
Storage temperature	Tstg	°C	-55	125	1

Notes:
1. If used beyond the absolute maximum ratings, the LSI may permanently be damaged. It is strongly recommended to use the LSI at a condition within the electrical characteristics for normal operation. Exposure to a condition not within the electrical characteristics may affect device reliability.
2. Make sure (High) VCI ≥ GND (Low). (High) IOVCC ≥ GND (Low). (High) VCC ≥ GND (Low).
3. Make sure (High) DDVDH ≥ AGND (Low).
4. Make sure (High) DDVDH ≥ VCI (Low).
5. Make sure (High) VGH ≥ GND (Low).
6. Make sure (High) GND ≥ VGL (or LVGL) (Low).
7. The DC/AC characteristics of die and wafer products is guaranteed at 85°C.
8. Make sure (High) VGH – VGL (or LVGL) < 29.5V.

7.2 Power Supply Specifications

Table 18. Power Supply Specifications

No.	Item		LG4572B
1	TFT source lines		1440 pins (480 x RGB)
2	GIP control signals		FW_L, BW_L, GPWR1_L, GPWR2_L, GCLK4_L, GCLK3_L, GCLK2_L, GCLK1_L, GVST1_L, GVST2_L, FW_R, BW_R, GPWR1_R, GPWR2_R, GCLK4_R, GCLK3_R, GCLK2_R, GCLK1_R, GVST1_R, GVST2_R,
3	Input voltages	IOVCC	1.65 to 3.30 V
		VCC	2.60 to 3.30 V
		VCI	2.60 to 3.30 V
4	Internal logic voltages	VDD	1.40 to 1.70 V
5	Internal step-up circuits	DDVDH	VCI x (1.47 to 2.45)
		DDVDL	-DDVDH
		VGH	DDVDH x 2, DDVDH x 2 + VCI, DDVDH x 3
		VGL	-(DDVDH x 2), -(DDVDH x 2 + VCI), -(DDVDH x 3)
		LVGL	VGL - VCI
		VCL	VCI x -1

7.3 DC Characteristics

Table 19. DC Characteristics

Item	Symbol	Unit	Test Condition	Min	Typ	Max	Notes
Input high voltage	V_{IH}	V	IOVCC = 1.65~3.3	0.8*IOVCC	-	IOVCC	
Input low voltage	V_{IL}	V	IOVCC = 1.65~3.3	-0.3	-	0.2*IOVCC	
Output high voltage (1) (DB17-0, SDO)	V_{OH1}	V	IOVCC = 1.65~3.3 IOH = 0.1mA	0.8*IOVCC	-	-	
Output low voltage (1) (DB17-0, SDO)	V_{OL1}	V	IOVCC = 1.65~3.3 IOL = 0.1mA	-	-	0.2*IOVCC	
I/O leakage current	I_{Li}	µA	Vin = 0~IOVCC	-1	-	1	
Current consumption during standby mode: (IOVCC - GND)	I_{ST_IOVCC}	µA	IOVCC = 2.8V Ta = 25°C	-	1.4	10	
Current consumption during standby mode: (VCC - GND) + (VCI - GND)	I_{ST_VCC} + I_{ST_VCI}	µA	VCC = VCI = 2.8V Ta = 25°C		100	150	1, MDDI
					20	30	RGB
					20	30	MIPI
					20	30	CPU
Current consumption during deep standby mode: (VCC - GND) + (VCI - GND) + (IOVCC – GND)	I_{DST}	µA	IOVCC = VCC = VCI = 2.8V Ta = 25°C		0	2	MDDI, RGB, MIPI, CPU

Notes:
1. The standby current in MDDI interface case should be update later. This typical value is based on the simulation results temporarily just for a reference.

7.4 AC Characteristics

7.4.1 MIPI HS Receiver Characteristics

Table 20. DC Characteristics of MIPI HS Receiver

Parameter	Description	Min	Nom	Max	Units	Notes
$V_{CMRX(DC)}$	Common-mode voltage HS receive mode	70		330	mV	
V_{IDTH}	Differential input high threshold			100	mV	
V_{IDTL}	Differential input low threshold	-100			mV	
V_{IHHS}	Single-ended input high voltage			460	mV	
V_{ILHS}	Single-ended input low voltage	-40			mV	
$V_{TERM-EN}$	Single-ended threshold for HS termination enable			450	mV	
Z_{ID}	Differential input impedance	80	100	125	ohm	

The differential input high and low threshold voltages of the HS receiver are denoted by V_{IDTH} and V_{IDTL}, respectively. V_{ILHS} and V_{IHHS} are the single-ended, input low and input high voltages, respectively. $V_{CMRX(DC)}$ is the differential input common-mode voltage.

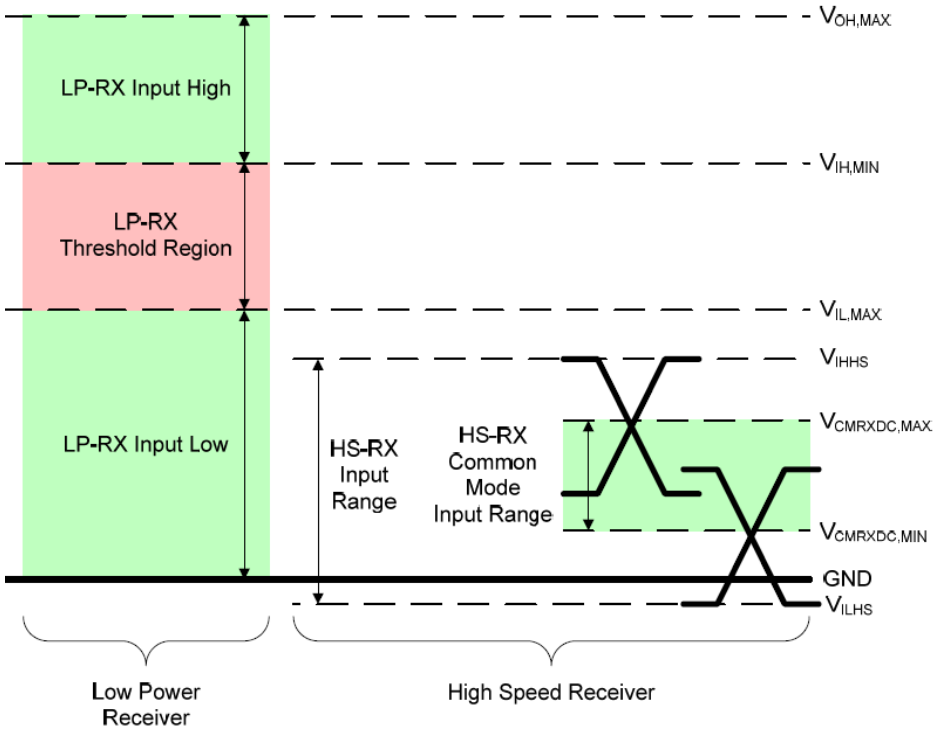


Figure 102. Signaling voltage levels.

Table 21. AC Characteristics of MIPI HS Receiver

Parameter	Description	Min	Nom	Max	Units	Notes
UI_{INST}	Data Rate (UI instantaneous)	3.0		12.5	ns	
T_{SETUP}	Data to Clock Setup Time	0.15			UI_{INST}	1
T_{SHOLD}	Clock to Data Hold Time	0.15			UI_{INST}	1
T_{SKEW}	Data to Clock Skew	-0.15		0.15	UI_{INST}	

Notes :

1. Total setup and hold window for receiver of $0.3*UI_{INST}$

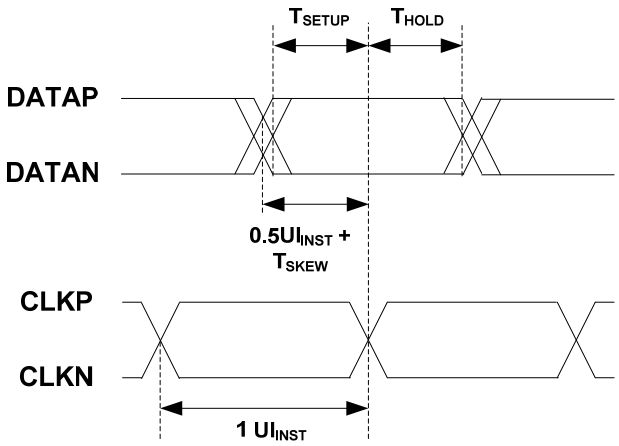


Figure 103. AC Timing Waveform for HS Mode MIPI Operation

7.4.2 MIPI LP Receiver Characteristics

Table 22. DC Characteristics of MIPI LP Receiver

Parameter	Description	Min	Nom	Max	Unit	Notes
V_{IH}	Logic 1 input voltage	880			mV	
V_{IL}	Logic 0 input voltage			550	mV	
$V_{IL-ULPS}$	Logic 0 input voltage, ULP State			300	mV	
V_{HYST}	Input Hysteresis	25			mV	

Table 23. AC Characteristics of MIPI LP Receiver

Parameter	Description	Min	Nom	Max	Unit	Notes
e_{SPIKE}	Input pulse rejection			300	Vp-s	1, 2
T_{MIN-RX}	Minimum pulse width response	20			ns	3
V_{INT}	Peak interference amplitude			200	mV	
f_{INT}	Interference frequency	450			MHz	

Notes:
1. Time-voltage integration of a spike above V_{IL} when being in LP-0 state or below V_{IH} when being in LP-1 state.
2. An impulse less than this will not change the receiver state.
3. An input pulse greater than this shall toggle the output.

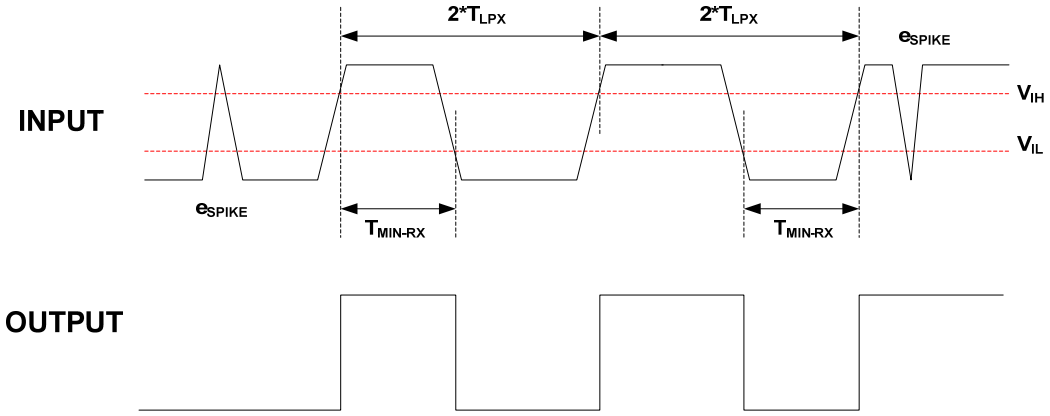


Figure 104. AC Timing Waveform for LP Mode MIPI Operation

7.4.3 MIPI LP Transmitter Characteristics

Table 24. DC Characteristics of MIPI LP Transmitter.

Parameter	Description	Min	Nom	Max	Unit	Notes
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V	
V_{OL}	Thevenin output low level	-50		50	mV	
Z_{OLP}	Output impedance of LP transmitter	110			ohm	1

Notes:

1. Though no maximum value for Z_{OLP} is specified, the LP transmitter output impedance shall ensure the T_{RLP}/T_{FLP} specification is met.

V_{OL} is the Thevenin output, low-level voltage in the LP transmit mode. This is the voltage at an unloaded pad pin in the low-level state. V_{OH} is the Thevenin output, high-level voltage in the high-level state, when the pad pin is not loaded.

Table 25. AC Characteristics of MIPI LP Transmitter

Parameter	Description		Min	Nom	Max	Units	Notes
T_{RLP}/T_{FLP}	15%-85% rise time and fall time				25	ns	1
T_{REOT}	Thevenin output low level				35	ns	1, 5, 6
$T_{LP-PULSE-TX}$	Pulse width of the LP exclusive-OR clock	First LP exclusive-OR clock pulse after Stop state or last pulse before Stop state	40			ns	4

		All other pulses	20			ns	4
$T_{LP\text{-}PER\text{-}TX}$	Period of the LP exclusive-OR clock		90			ns	
$\delta V/\delta t_{SR}$	Slew rate @ C_{LOAD} = 0pF		30		500	mV/ns	1, 2, 3
	Slew rate @ C_{LOAD} = 5pF		30		200	mV/ns	1, 2, 3
	Slew rate @ C_{LOAD} = 20pF		30		150	mV/ns	1, 2, 3
	Slew rate @ C_{LOAD} = 70pF		30		100	mV/ns	1, 2, 3
C_{LOAD}	Load capacitance		0		70	pF	1

Notes:

1. C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.
2. When the output voltage is between 15% and below 85% of the fully settled LP signal levels.
3. Measured as average across any 50 mV segment of the output signal transition.
4. This parameter value can be lower then T_{LPX} due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters.
5. The rise-time of T_{REOT} starts from the HS common-level at the moment the differential amplitude drops below 70mV, due to stopping the differential drive.
6. With an additional load capacitance C_{CM} between 0-60pF on the termination center tap at RX side of the Lane

The times T_{RLP} and T_{FLP} are the 15%–85% rise and fall times, respectively, of the output signal voltage, when the LP transmitter is driving a capacitive load C_{LOAD}. The 15%–85% levels are relative to the fully settled V_{OH} and V_{OL} voltages. The slew rate $\delta V/\delta t_{SR}$ is the derivative of the LP transmitter output signal voltage over time. The slew rate specification shall be met for the 15%–85% range while driving a capacitive load, C_{LOAD}.

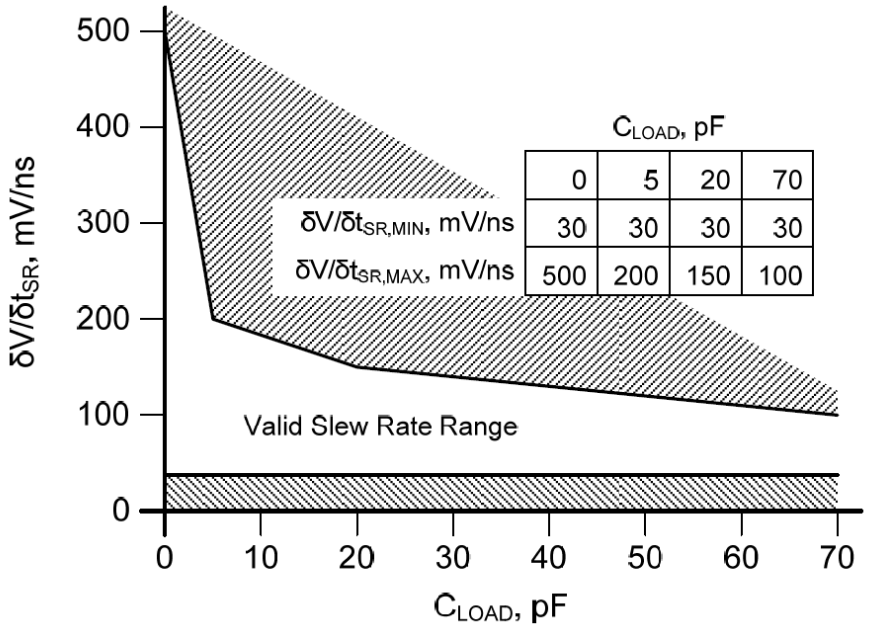


Figure 105. Slew rate of LP TX vs. C_{Load}

7.4.4 MDDI Transmitter Characteristics

The requirements of transmitter are listed in the table below. The load capacitance of the measurement probe must be less than 10 pF between each signal and the client ground, and less than 5 pF across each signal of a differential pair. No load must be present on the differential pairs other than the parasitic capacitance of the measurement probe.

Table 26. Electrical Specification of MDDI Transmitter in LG4572B

Parameter	Description	MDDI 1.2			Unit
		Min	Typ	Max	
$V_{output\text{-}Range\text{-}Int}$	Allowable client driver output voltage range with respect to client ground (Internal Mode)	0.6		1.1	V
I_{OD+}	Driver differential output high current corresponding to logic-one level (while driving the equivalent of the pull-up and pull-down circuits that exist at the host and client)	1.5	2	2.5	mA
I_{OD-}	Driver differential output high current corresponding to logic-zero level (while driving the equivalent of the pull-up and pull-down circuits that exist at the host and client)	-2.5	-2	-1.5	mA
$Z_{Out\text{-}Client}$	Minimum differential output impedance of the MDDI_Data drivers in the client device	1			kohm
$t_{Rise\text{-}Fall}$	Rise and fall time (between 20% and 80% amplitude) of driver output, measured in differential mode	200		Note 1	psec
$t_{skew\text{-}pair}$	Skew between positive and negative outputs of the same differential pair			50	psec
$t_{B\text{-}DRVR}$	Jitter, bit boundary to minimum output level			$0.15t_{BIT}$	

Note 1 : The maximum rise and fall time is either 35% of the interval to transmit one bit on one differential pair or 100nsec, whichever smaller.

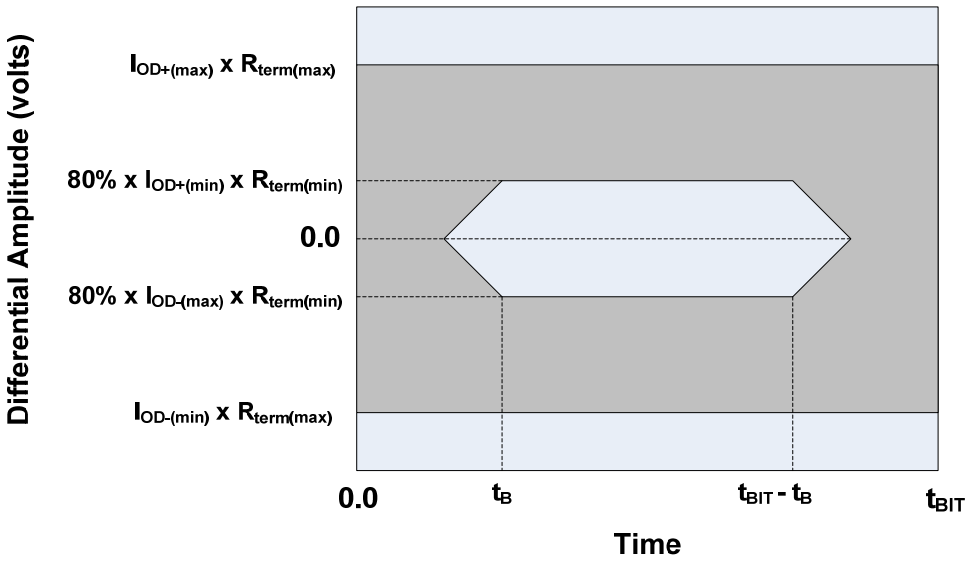


Figure 106. Transmitter Eye Diagram (R_{term} is defined in the receiver specification)

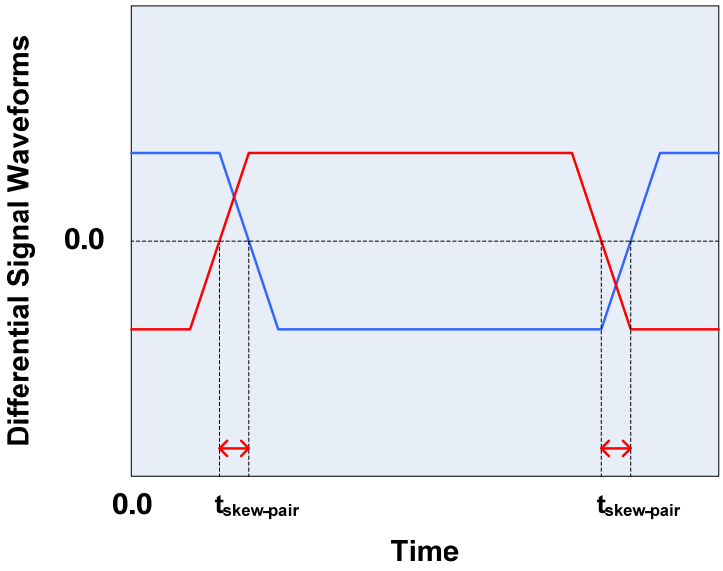


Figure 107. Skew between positive and negative outputs

7.4.5 MDDI Receiver Characteristics

The requirements are listed in the table below. The load capacitance of the measurement probe must be less than 10 pF between each signal and the host ground, and less than 5 pF across each signal of a differential pair. No load must be present on the differential pairs other than the parasitic capacitance of the measurement probe.

Table 27. Electrical Specification of MDDI Receiver in LG4572B

Parameter	Description	MDDI 1.2			Unit
		Min	Typ	Max	
V_{IT+}	Receiver differential input high threshold voltage. Above this differential voltage the input signal must be interpreted as a logic-one level		0	50	mV
V_{IT-}	Receiver differential input low threshold voltage. Above this differential voltage the input signal must be interpreted as a logic-zero level	-50	0		mV
V_{IT+}	Receiver differential input high threshold voltage (offset for hibernation wake-up). Above this differential voltage the input signal must be interpreted as a logic-one level		100	125	mV
V_{IT-}	Receiver differential input low threshold voltage (offset for hibernation wake-up). Above this differential voltage the input signal must be interpreted as a logic-zero level	75	100		mV
R_{term}	Parallel termination resistance value	98	100	102	Ohm
$V_{Input-Range}$	Allowable receiver input voltage range with respect to client ground.	0.5		1.2	V
$t_{Diff-Skew}$	Peak delay skew between one differential pair and any other differential pair			$0.45t_{BIT}$	
t_A	Jitter, bit boundary to center crossing			$0.1t_{BIT}$	
t_{B-RCVR}	Jitter, bit boundary to minimum input level			$0.15t_{BIT}$	
t_{BIT}	Receiver maximum operation speed ($1/t_{BIT}$= bps)	2.5			ns

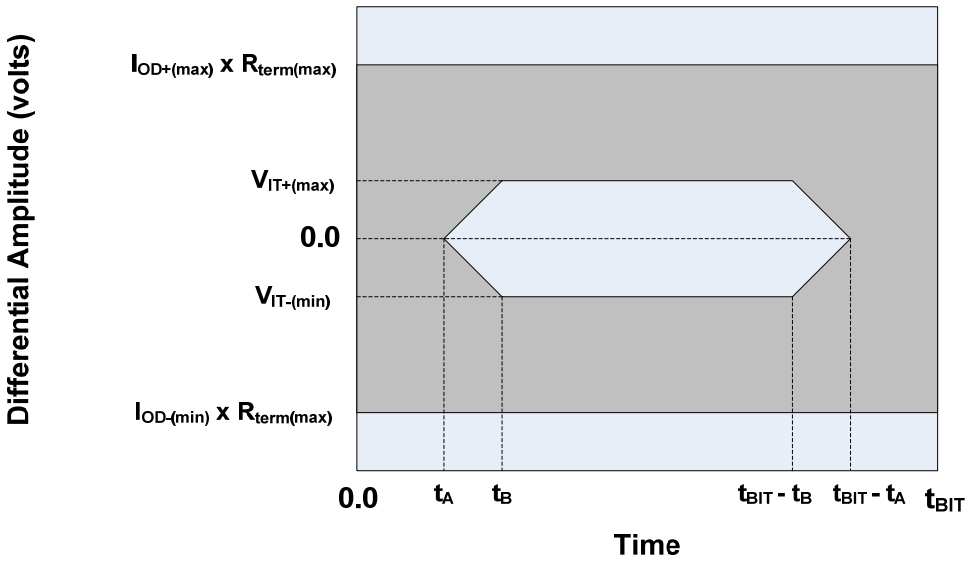


Figure 108. Receiver Eye Diagram

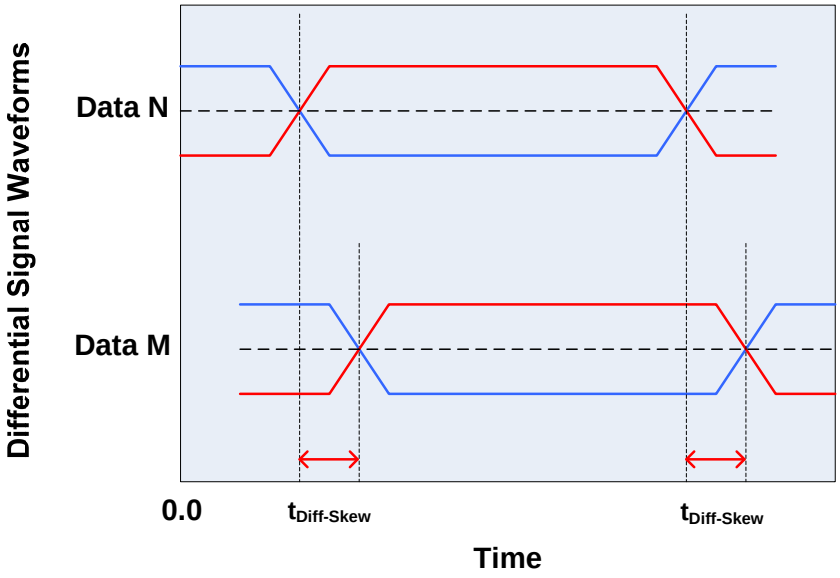


Figure 109. Peak delay skew between differential pairs

7.4.6 Interconnect Network Requirement for MDDI

Interconnect network characteristics for MDDI are described as follows.

Table 28. Interconnect Network Characteristics for MDDI

Parameter	Description	MDDI 1.2	Unit

		MDDI 1.2			
		Min	Typ	Max	
Z_0	Transmission line differential impedance of each differential pair	80	100	120	ohm
t_{prop}	Propagation time of a differential signal through the Interconnect Network	0		1.5	nsec
$t_{skew-pair}$	Skew between positive and negative output of the same differential pair(intra-pair skew)			50	psec
$t_{Diff-Skew}$	Peak delay skew between one differential pair and any other differential pair(inter-pair skew)			100	psec
$R_{DC-Signal}$	Series resistance of each wire in a differential pair of the MDDI_Stb+/-, or MDDI_Data0+/- through MDDI_Data#+/- signals on the interconnect network, includes resistance of conductors and EMI filtering components	0		4	ohm
V_{DC-Pwr}	Voltage drop in Host_Gnd in the cable between Host and Receiver	0		110	mV
C_{diff}	Capacitance between the two signals of a differential pair in the matched line in the internal network			7.5	pF

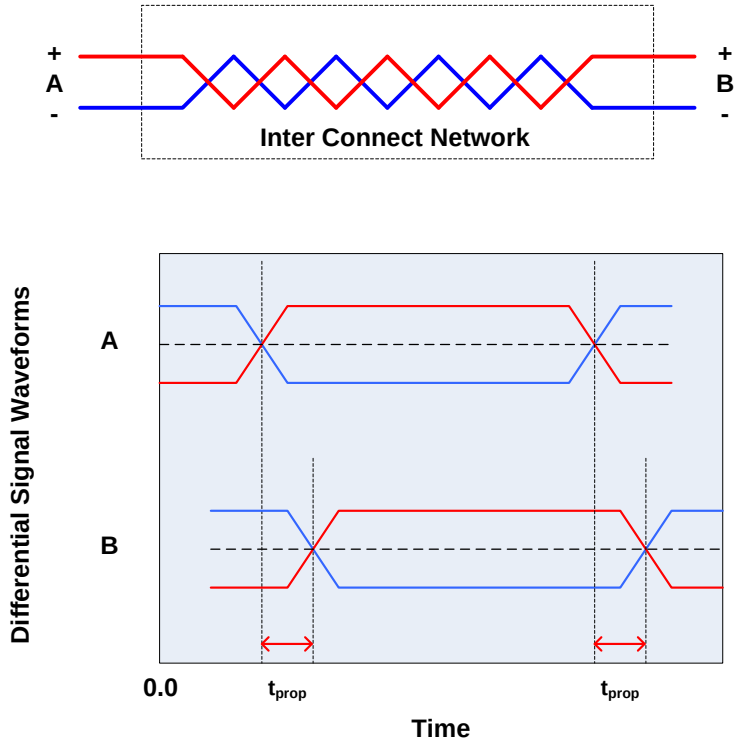


Figure 110. Propagation time through Interconnect Network

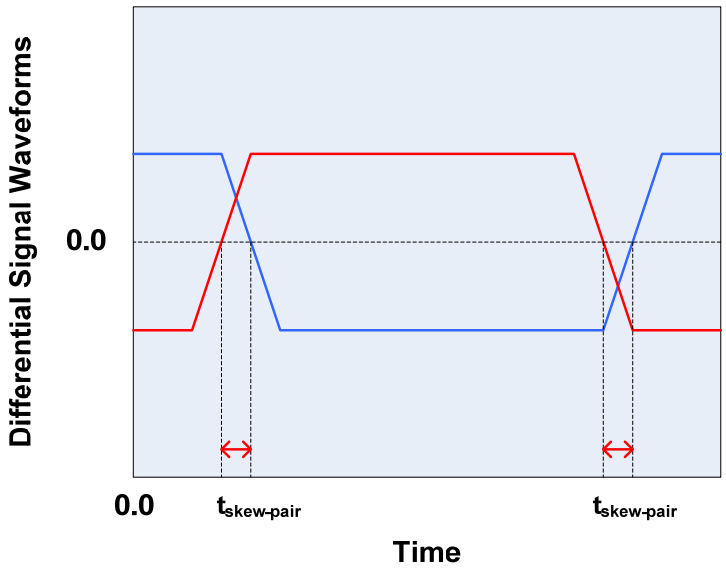


Figure 111. Interconnect Network skew between positive and negative outputs

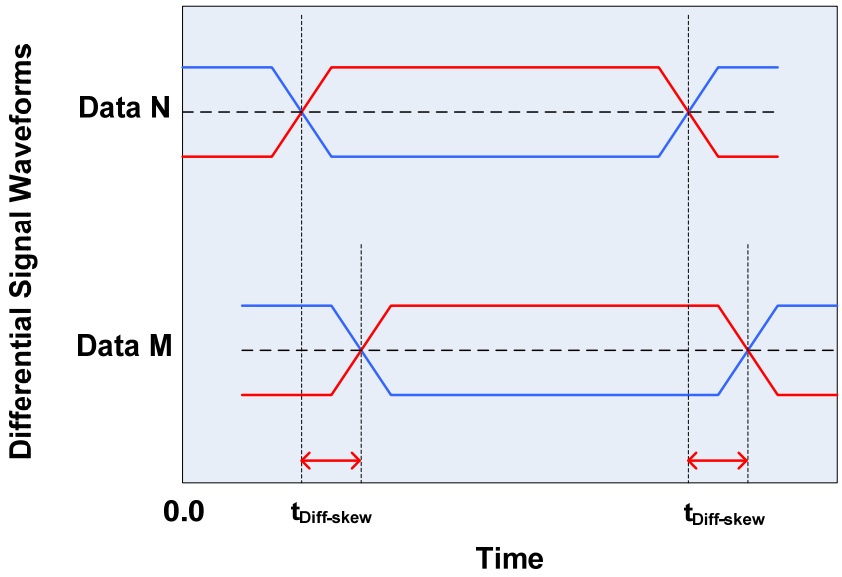


Figure 112. Interconnect Network peak delay skew between differential pairs

7.4.7 Serial Peripheral Interface Characteristics

Table 29. (Condition: IOVCC = 1.65 to 3.30V, VCC = 2.60 to 3.30V)

Item		Symbol	Unit	Min	Typ	Max
Serial clock cycle time	Write (received)	tSCYC	ns	20	-	-
	Read (transmitted)			100	-	-
Serial clock "High" level pulse width	Write (received)	tSCH	ns	10	-	-
	Read (transmitted)			50	-	-
Serial clock "Low" level pulse width	Write (received)	tSCL	ns	10	-	-
	Read (transmitted)			50	-	-
Serial clock rise/fall time		tscr, tscf	ns	-	-	20
Chip select setup time		tCSU	ns	20	-	-
Chip select hold time		tCH	ns	10	-	-
Serial input data setup time		tSISU	ns	5	-	-
Serial input data hold time		tSIH	ns	10	-	-
Serial output data setup time		tSOD	ns	80	-	150
Serial output data hold time		tSOH	ns	-	-	80

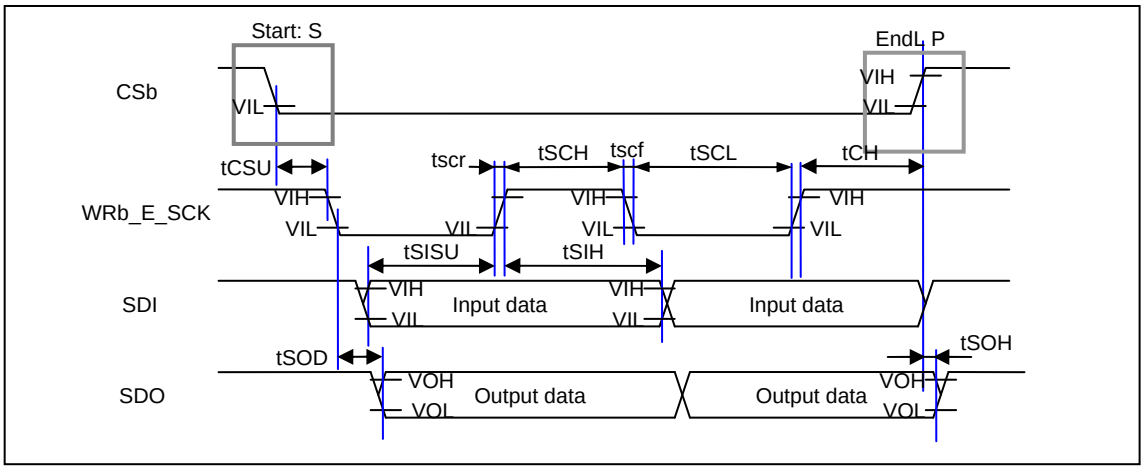


Figure 113. Serial peripheral interface operation

7.4.8 Reset Timing Characteristics

Table 30. (Condition: IOVCC = 1.65 to 3.30V, VCC = 2.60 to 3.30V)

Item	Symbol	Unit	Min	Typ	Max
Reset "Low" level width	tRES	ms	1	-	-
Reset rise time	trRES	µs	-	-	10

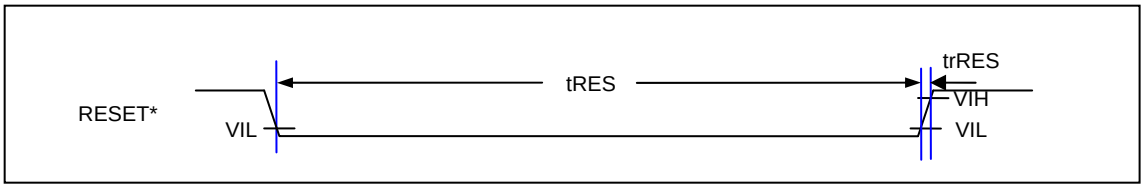


Figure 114. Reset operation

7.4.9 RGB Interface Timing Characteristics

Table 31. (24/18/16-bit I/F, IOVCC = 1.65 to 3.30V, VCC = 2.60 to 3.30V)

Item	Symbol	Unit	Min	Typ	Max
VSYNC/HSYNC setup time	tSYNCS	ns	10	-	-
VSYNC/HSYNC hold time	tSYNCH	ns	10	-	-
DE setup time	tENS	ns	10	-	-
DE hold time	tENH	ns	10	-	-
PCLK "Low" level pulse width	PWDL	ns	20	-	-
PCLK "High" level pulse width	PWDH	ns	20	-	-
PCLK cycle time	tCYCD	ns	40	-	-
Data setup time	tPDS	ns	10	-	-
Date hold time	tPDH	ns	10	-	-
PCLK, VSYNC, HSYNC, DE rise/fall time	trgbr, trgbf	ns	-	-	13

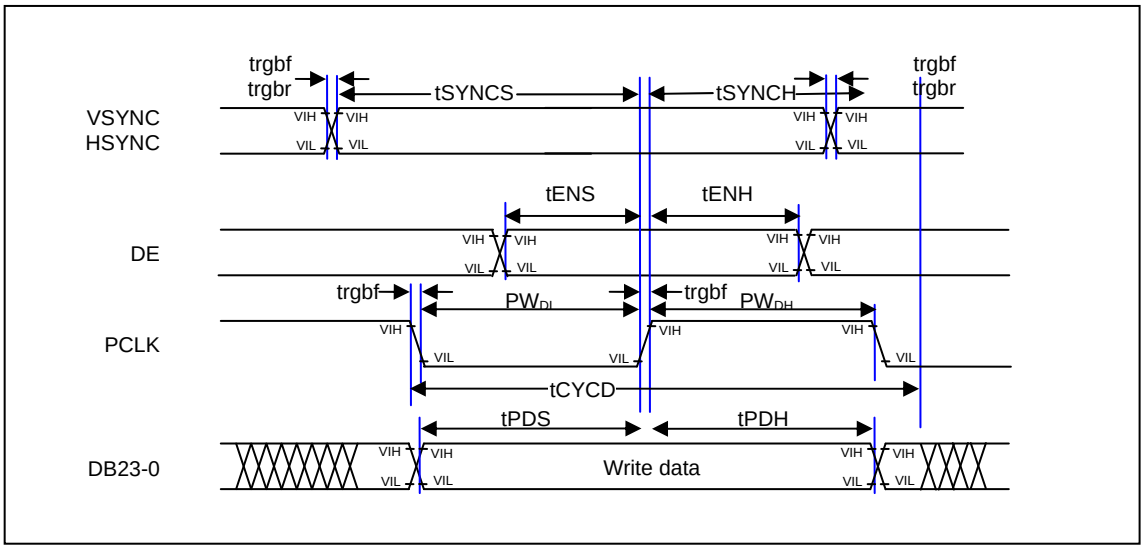


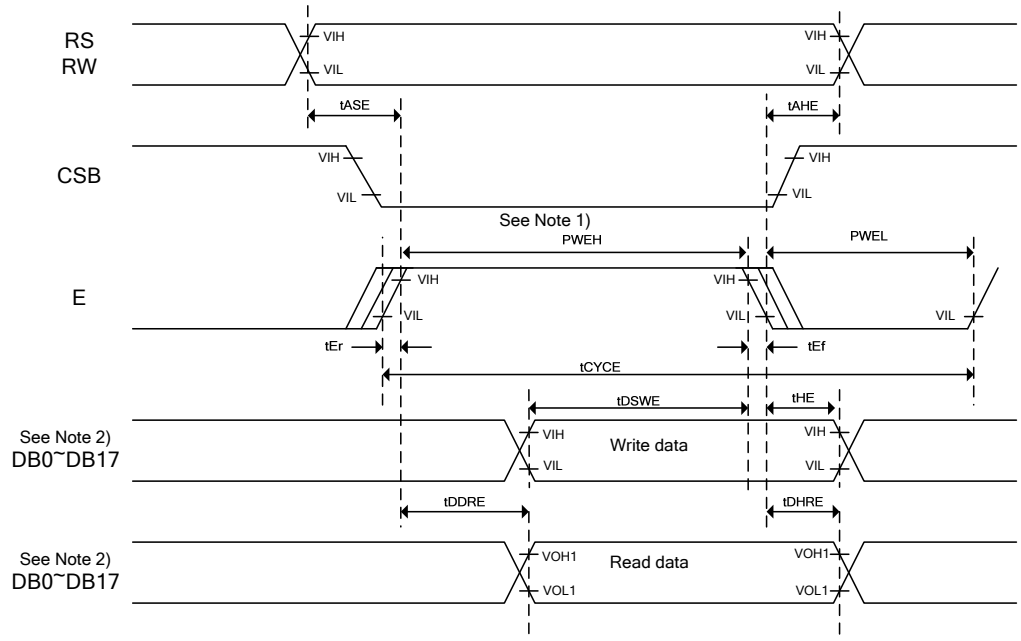
Figure 115. RGB interface

7.4.10 68-System Bus Interface Timing Characteristics (18/16-Bit Bus)

Table 32. 68-System Bus Interface Timing (Condition: IOVCC = 1.65 to 3.30V, VCC = 2.60 to 3.30V)

Item	Symbol	Unit	Min.	Typ.	Max.

Bus Cycle time		Write	tCYCE	ns	40	-	-
		Read	tCYCE	ns	300	-	-
Write "Low" level pulse width Read "Low" level pulse width		Write	PWEL	ns	20	-	-
		Read	PWEL	ns	150	-	-
Write "High" level pulse width Read "High" level pulse width		Write	PWEH	ns	20	-	-
		Read	PWEH	ns	150	-	-
Write/Read rise/fall time			tEr, tEf	ns		-	10
Setup time	Write (RS, RW to E)		tASE	ns	0	-	-
	Read (RS, RW to E)				10	-	-
Address hold time			tAHE	ns	5	-	-
Write data setup time			tDSWE	ns	10	-	-
Write data hold time			tHE	ns	5	-	-
Read data delay time			tDDRE	ns	-	-	100
Read data hold time			tDHRE	ns	5	-	-



Note 1) PWEW is defined by the overlap period when CSB is "Low" and E is "High".
Note 2) Unused DB pins must be fixed at "IOVCC" or "GND".

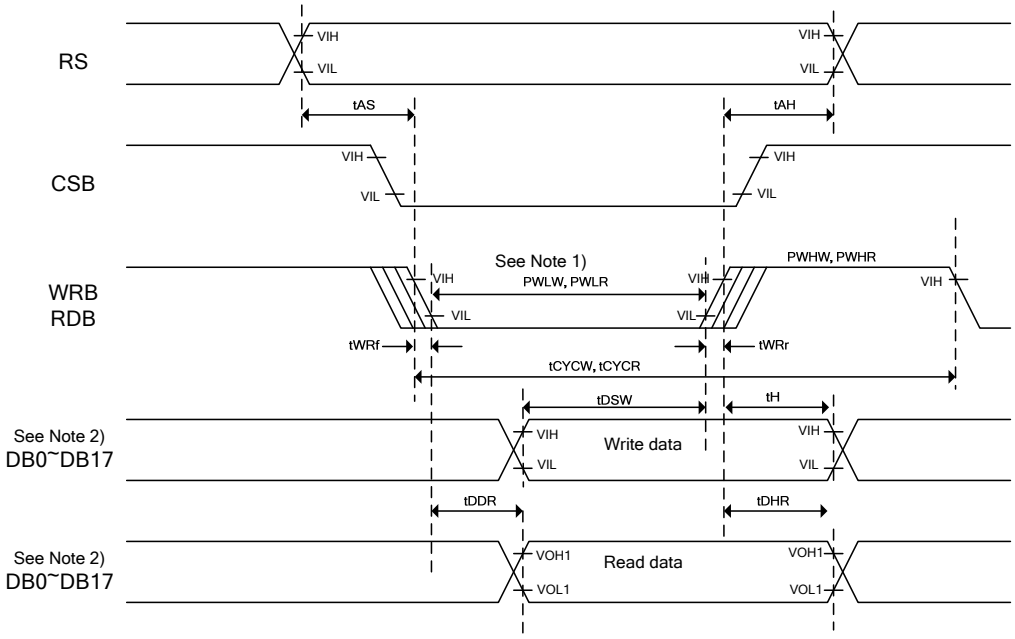
Figure 116. 68-system bus interface operation

7.4.11 80-System Bus Interface Timing Characteristics (18/16-Bit Bus)

Table 33. 80-System Bus Interface Timing (Condition: IOVCC = 1.65 to 3.30V, VCC = 2.60 to 3.30V)

Item		Symbol	Unit	Min.	Typ.	Max.
Bus Cycle time	Write	tCYCW	ns	40	-	-
	Read	tCYCW	ns	300	-	-
Write "Low" level pulse width Read "Low" level pulse width	Write	PWLW	ns	20	-	-
	Read	PWLR	ns	150	-	-

Write "High" level pulse width Read "High" level pulse width	Write	PWHW	ns	20	-	-
	Read	PWHR	ns	150	-	-
Write/Read rise/fall time		tWRr,tWRf	ns		-	10
Setup time	Write (RS, RW to E)	tAS	ns	0	-	-
	Read (RS, RW to E)			10	-	-
Address hold time		tAH	ns	5	-	-
Write data setup time		tDSW	ns	10	-	-
Write data hold time		tH	ns	5	-	-
Read data delay time		tDDR	ns	-	-	100
Read data hold time		tDHR	ns	5	-	-



Note 1) PWLW and PWLR are defined by the overlap period when CSB is "Low" and WRB or RDD is "Low".
Note 2) Unused DB pins must be fixed at "IOVCC" or "GND".

Figure 117. 80-system bus interface operation

8 Reference Applications

8.1 Configuration of Power Supply Circuit

Figure 118 is one of the configurations of power supply circuits to generate liquid crystal panel drive levels.

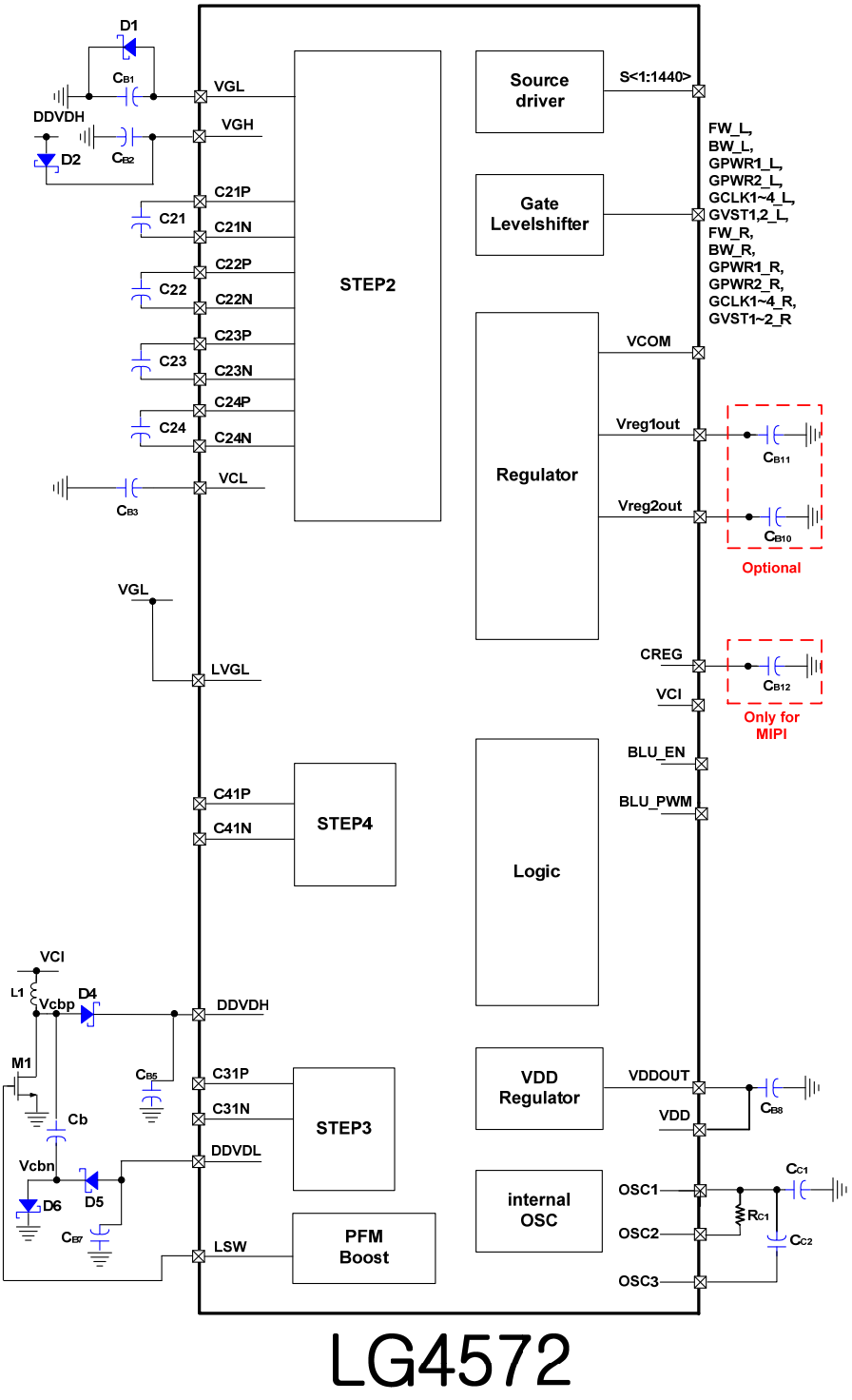
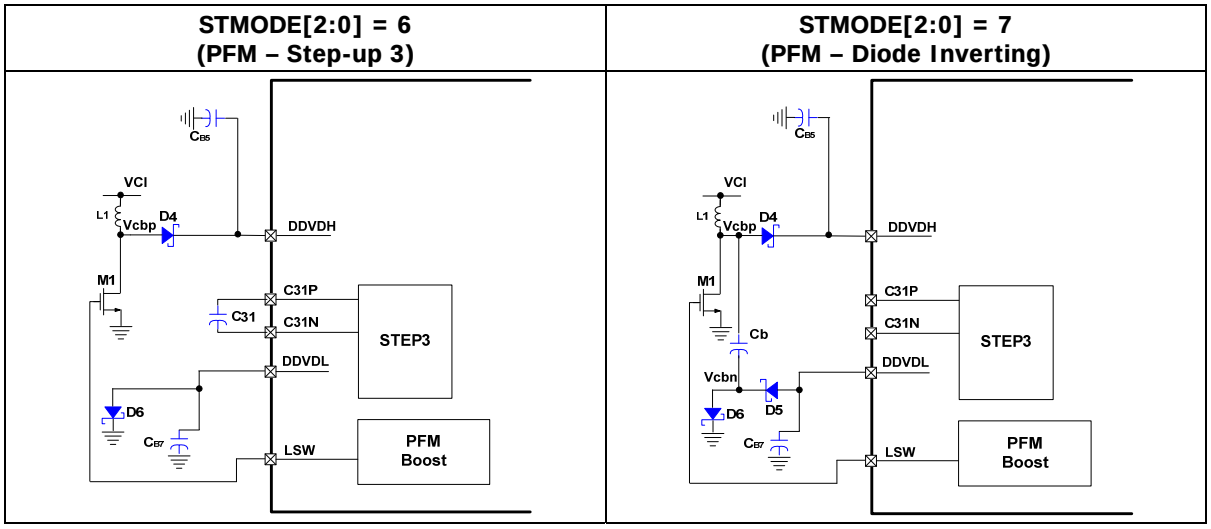


Figure 118. One example of application circuits for the STMODE=7 case.

Some application circuitries in the above power supply circuit configuration should be changed according to the below setting modes. Please see the followings.



Under some abnormal situations, such as no power-on reset in the system or as un-kept power on/off sequences or as something else, external MOS switch should be protected by inserting high pass filter between LSW and MOS gate node of n1 in the following figure. The HPF circuits in the following figure is a recommended one. The connection of 1uF capacitance near to inductor and/or MOS switch could help to reduce the noises from VCI power node. But they are all optionals for special cases.

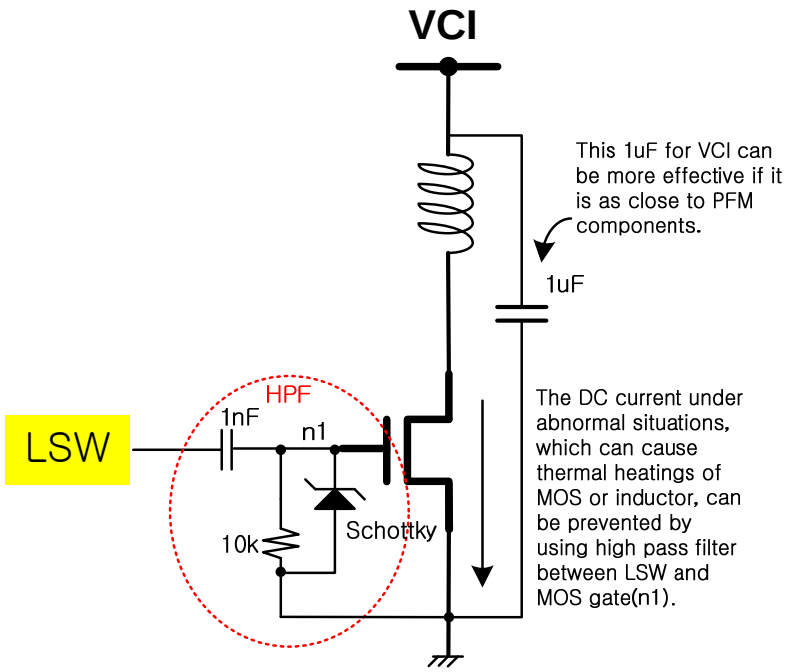


Figure 119. HPF (High Pass Filter) application circuits for protecting external MOS Tr.

Specification of External Elements Connected to LG4572B Power Supply

The following tables show specifications of external element connected to the LG4572B's power supply circuit.

Table 34. Capacitor

Capacity	Recommended voltage	Pin connection
1uF (B characteristics)	6V	C24, CB3, CB10**, CB11**, CB12
	10V	C21, C22, C23, C31*
	25V	CB1, CB2
1.0uF	10V	CB5, CB7
1.0uF	6V	CB8
0.47uF	10V	Cb*

Note: Some components* are optional according to the specific usages and some components** would be eliminated after reliability test.

Table 35. Resistor

Resistor value	Recommended voltage	Pin connection
10KΩ	6V	R_{C1}* (< 1% error tolerant resistor)

Note: Some components* are optional according to the specific usages and some componts** would be eliminated after reliability test.

Table 36. Schottky diode

Feature	Pin connection
VF < 0.4V/20mA at 25°C , VR>30V	D1**, D2, D4, D5*, D6**

Note: Some components* are optional according to the specific usages and some components** would be eliminated after reliability test.

Table 37. N-ch MOSFET

Feature	Specification
M1	IDSS<1μA at VDS>16V, VGS=0V, and 25°C Ron<1.25Ω at VGS=2.5V and ID=300mA ton<30ns(Typ.) toff<30ns(Typ.)

Note: Recommended N-ch MOSFETs:

1. Si1012R/X (Vishay Siliconix)
2. RUM003N02 (ROHM)

Table 38. Inductor for Booster

Feature	Inductance Specification
L1	Inductance value = 4.7uH Inductance tolerance < ± 20% DC resistance (± 30%) < 0.24ohm Max. rated current > 145mA at saturation Max. rated current > 470mA at temperature rise

Note: Recommended inductor components:

1. CBMF1608T4R7M (TAIYO YUDEN)
2. VLF3010AT-4R7MR70 (TDK)

9 History of Revision

Ver.	Date	Note
0.5	2009.05.04	Initial release of official version.
0.8	2009.10.20	The data sheet format is reorganized. -Electrical Characteristics are added.
0.8.2	2009.11.17	IM mode setting is changed. Hsync functionality for setting MIPI lane number is changed. Several typing errors are fixed
0.8.3	2009.11.25	36h memory access control spec is updated. Electrical DC characteristics are updated.
0.8.6	2009.12.09	- Windowless video stream packet in MDDI I/F is not supported. - 36h memory access control spec is updated - MIPI DSI configurations are newly added after manufacture command set - M68 & I80 I/Fs for frame memory writing are not supported anymore.
0.8.7	2009.12.23	- Several parameters in B5h register are deleted. They are just for engineering modes not for IC general users. - VDD voltage range is changed to guarantee more stable operation in memory. There is no side effects even though the VDD voltage range is changed. - POR type error in OTP write sequence is fixed to be PDR.
0.8.8	2010.01.18	- VDD voltage range is re-changed. - Absolute Max. values for VGH, LVGL, and VGH-LVGL are changed. - Electrical characteristics of RGB interface are updated. - Electrical characteristics of MIPI interface are updated. - Examples for parameter read from specific register through SPI I/F are added for better understanding.
0.8.9	2010.02.26	- Chip thickness is changed from 300um to 250um
0.9.0	2010.03.06	- Notice 2 regarding the usage of LG products is newly added in page 4. - MDDI max. operation speed is updated in 7.4.5. - GPWR signal waveforms are corrected in page 187. - HPF (High Pass Filter) application circuits are newly added in page 259 to protect external MOS transistor of PFM circuits under some abnormal conditions, such as no hardware reset supported by MPU side or as else. It's an optional for special case. - Typing Errors are fixed in 5.12 - 4.7uF capacitance values are changed to 1uF in page 260.
1.0.0	2010.04.12	- Pin descriptions are modified from page 7-8 in red colors. - 5.2.4 revived. - FH function is revived in page 150 and 152. - Type error is fixed in page 162 regarding TEN. - Descriptions are updated in page 165.

1.0.1	2010.05.06	- CABC function descriptions are updated in 5.8 - Some comments on IOVCC in page 9 are deleted to avoid unnecessary misunderstanding.
1.0.2	2010.07.08	- Description on A1h register is added in page 176. - Default setting value for LPM is fixed in page 231. - Typo max. allowable setting values for VGH and VGL/LVGL are fixed in page 82. - MDDI 18bit interface is not supported anymore in page 67-69.