Digital Logic Design

STOPWATCH PROJECT

Haroon Ul Haq - 240692
Ahmed Saleem - 242348
Muhammad Haseeb - 242292
Syed Ahtsham Hussain Shah - 242364

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Digital Stopwatch Project Report

1. Introduction

This report details the design and simulation of a digital stopwatch using Proteus software for a Digital Logic Design (DLD) course. The stopwatch counts time in hours (H1, H2), minutes (M1, M2), and seconds (S1, S2), displaying the results on 7-segment displays. The circuit uses JK flip-flops, decoders, logic gates, and a custom clock circuit to achieve timekeeping functionality. This report also covers the reset and clock control logic, as well as the standalone clock circuit.

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2. Project Objectives

- Design a digital stopwatch to count and display hours, minutes, and seconds.
- Use BCD counters to drive 7-segment displays for digits H1, H2, M1, M2, S1, and S2.
- Implement reset and clock control logic for starting, stopping, and resetting the stopwatch.
- Simulate and verify the design in Proteus.

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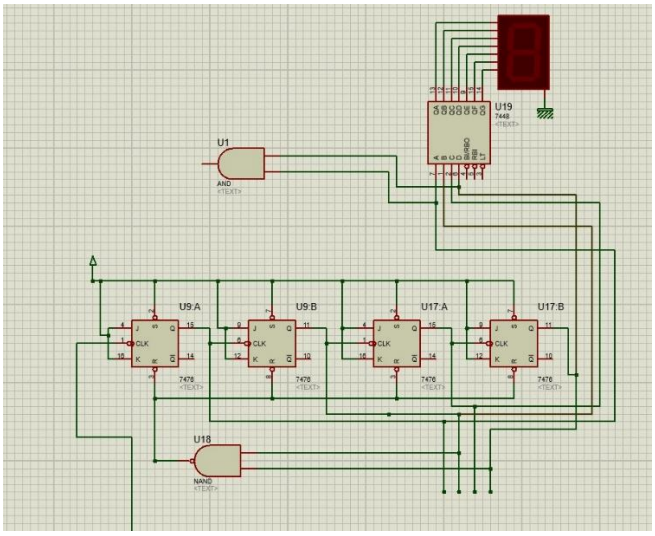
3. Display Units: Detailed Breakdown

The stopwatch uses six 7-segment displays to show time in the format HH:MM:SS, where H1 and H2 represent hours, M1 and M2 represent minutes, and S1 and S2 represent seconds. Each display is driven by a BCD counter and decoder.

3.1 S1 (Units of Seconds)

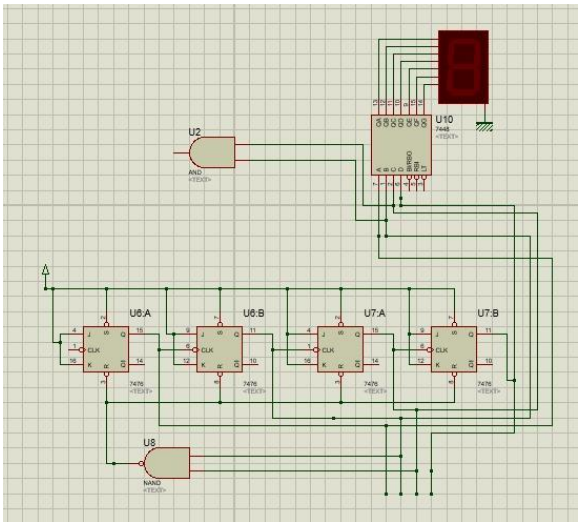
- **Description**: S1 displays the units of seconds (0-9).
- **Components**:
    - JK Flip-Flops: U4A, U4B (likely part of a 7473 dual JK flip-flop IC).
    - Decoder: U4 (likely a 7447 BCD to 7-segment decoder).
    - 7-Segment Display: Connected to U4 outputs.
- **Logic**:
    - The JK flip-flops form a 4-bit BCD counter, counting from 0 to 9.

- The clock input to U4A comes directly from the clock source (1 Hz), incrementing the counter every second.
- 

- The Q outputs (Q0-Q3) of the flip-flops feed into the decoder, which drives the 7-segment display to show the digit.

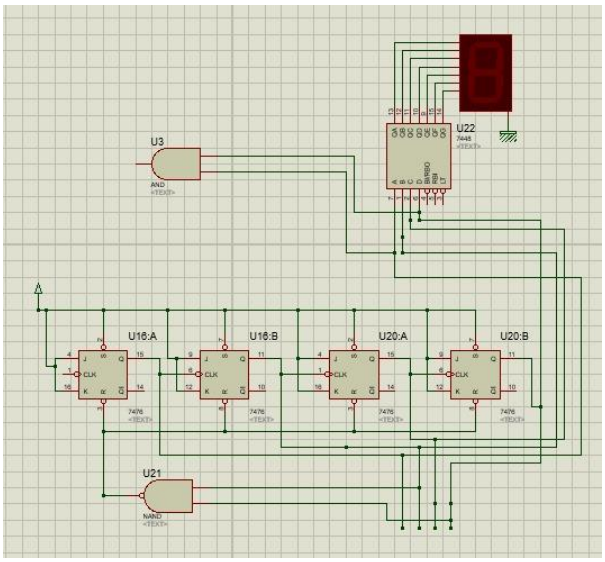
- **Operation**:
  - Starts at 0 and increments to 9, then resets to 0, generating a carry signal to S2.

3.2 S2 (Tens of Seconds)

- **Description**: S2 displays the tens of seconds (0-5).
- **Components**:
  - JK Flip-Flops: U47A, U47B.
  - Decoder: U4 (shared with S1 via multiplexing).
  - 7-Segment Display: Connected to U4 outputs.
  - 

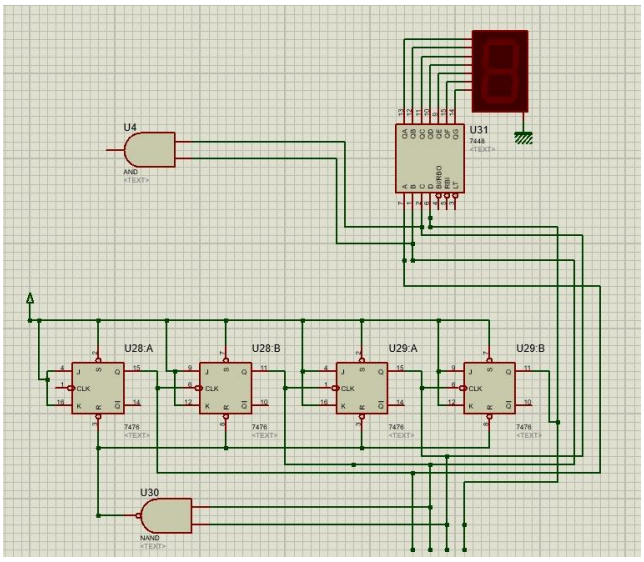
- **Logic**:
    - This stage counts from 0 to 5 (BCD 0000 to 0101).
    - The clock input to U47A is the carry output from S1 (generated when S1 resets from 9 to 0).
    - The decoder converts the BCD value to the 7-segment display pattern.
- **Operation**:
    - Increments every 10 seconds (when S1 resets), resetting to 0 after 5 and sending a carry to M1.

3.3 M1 (Units of Minutes)

- **Description**: M1 displays the units of minutes (0-9).
- **Components**:
    - JK Flip-Flops: U37A, U37B.
    - Decoder: U40 (likely a 7447 IC, separate from S1/S2 in the second configuration).
    - 7-Segment Display: Connected to U40 outputs.
    - 

- **Logic**:
    - Similar to S1, this is a 4-bit BCD counter.
    - The clock input is the carry from S2 (every 60 seconds).
    - The decoder drives the display to show the digit.
- **Operation**:
    - Increments every minute, resetting to 0 after 9 and sending a carry to M2.

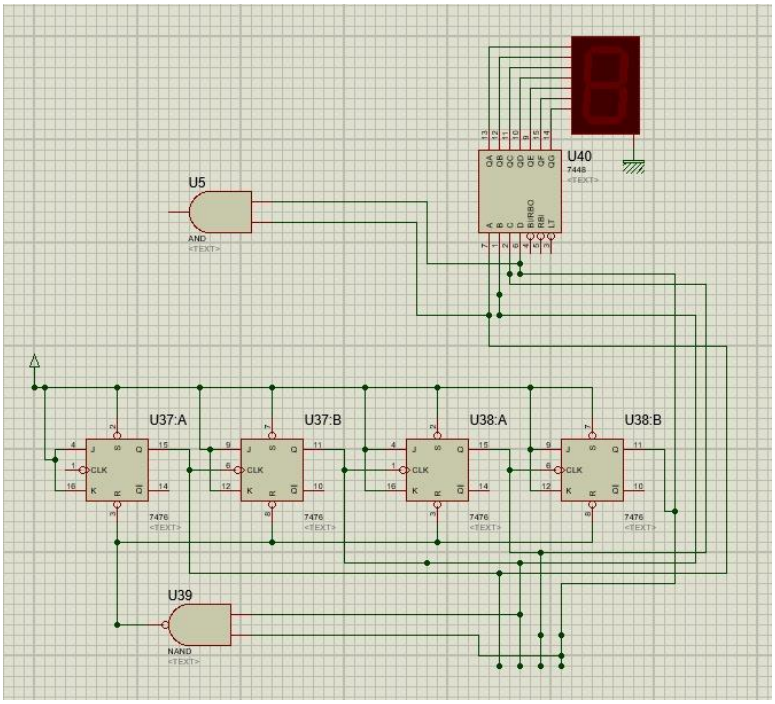
3.4 M2 (Tens of Minutes)

- **Description**: M2 displays the tens of minutes (0-5).
- **Components**:
  - JK Flip-Flops: U38A, U38B.
  - Decoder: U40 (shared with M1 via multiplexing).
  - 7-Segment Display: Connected to U40 outputs.
  - 

- **Logic**:
  - Counts from 0 to 5, resetting after 5.
  - The clock input is the carry from M1.
  - The decoder converts the BCD value to the display pattern.
- **Operation**:
  - Increments every 10 minutes, resetting to 0 after 5 and sending a carry to H1.

3.5 H1 (Units of Hours)

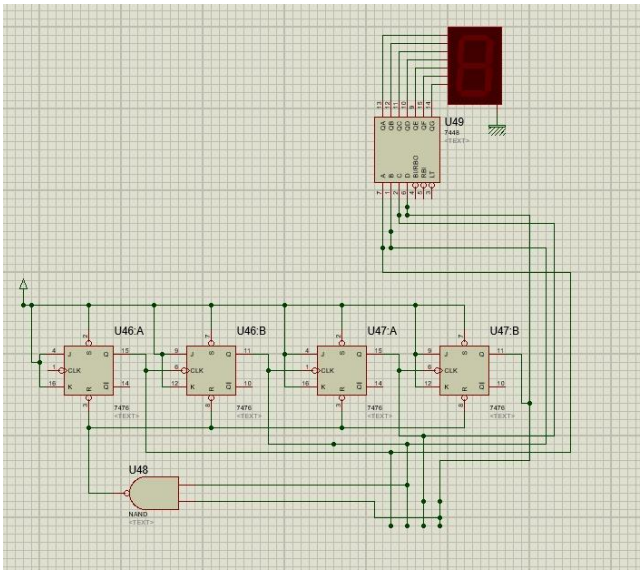
- **Description**: H1 displays the units of hours (0-9).
- **Components**:
  - JK Flip-Flops: Not explicitly labeled but implied in the hierarchy.
  - Decoder: U40 (shared with M1/M2).
  - 7-Segment Display: Connected to U40 outputs.

- 

- **Logic**:
  - A 4-bit BCD counter, similar to previous stages.
  - The clock input is the carry from M2 (every hour).
  - The decoder drives the display.
- **Operation**:
  - Increments every hour, resetting to 0 after 9 and sending a carry to H2.

3.6 H2 (Tens of Hours)

- **Description**: H2 displays the tens of hours (0-2 for a 24-hour clock).
- **Components**:
  - JK Flip-Flops: Implied in the hierarchy.
  - Decoder: U40 (shared with other displays).
  - 7-Segment Display: Connected to U40 outputs.

- 

- **Logic**:
  - Counts from 0 to 2 (BCD 0000 to 0010) for a 24-hour format.
  - The clock input is the carry from H1.
  - Resets to 0 after 2 (at 24 hours).
- **Operation**:
  - Increments every 10 hours, resetting the entire clock to 00:00:00 after 23:59:59.

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4. Reset Logic

- **Description**: The reset logic initializes the stopwatch to 00:00:00.
- **Components**:
  - NAND Gates: Used to generate the reset signal.
  - Clear Inputs: CLR pins on all JK flip-flops (e.g., U4A, U47A, etc.).
- **Logic**:
  - A NAND gate takes inputs from a manual reset switch or a counter overflow condition (e.g., after 23:59:59).
  - When the NAND gate output goes low (all inputs high), it asserts the CLR pins of all flip-flops, setting their Q outputs to 0.
- **Operation**:
  - When the reset signal is triggered, all counters (S1, S2, M1, M2, H1, H2) reset to 0, and the displays show 00:00:00.

- **Role in Project**: Ensures the stopwatch can be restarted from zero, either manually or at the end of a 24-hour cycle.

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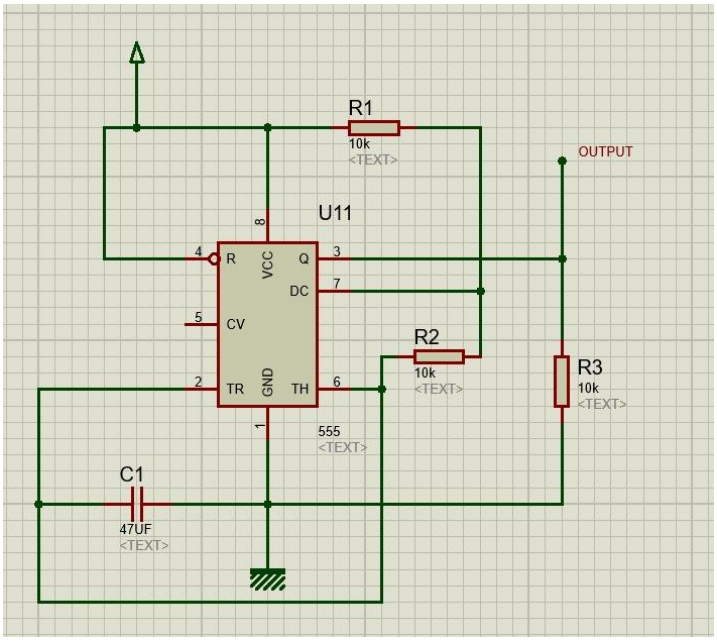
5. Clock Control Logic

- **Description**: The clock control logic manages the start/stop functionality of the stopwatch.
- **Components**:
  - AND Gate: U5 (used to gate the clock signal).
  - Clock Source: U48, U39 (or the custom clock circuit in the second image).
  - 

- **Logic**:
  - The AND gate takes the clock signal and an enable signal as inputs.
  - When the enable signal is high, the clock signal passes through to the counters, allowing counting.
  - When the enable signal is low, the clock signal is blocked, pausing the count.
- **Operation**:
  - Start: Enable signal set to 1, allowing the clock to drive the counters.
  - Stop: Enable signal set to 0, stopping the clock signal and pausing the count.
- **Role in Project**: Provides user control over the stopwatch, enabling it to start or pause as needed.

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6. Clock Circuit (Standalone Analysis)

The second image shows a custom clock circuit based on a 555 timer IC, which generates the 1 Hz signal for the stopwatch.

6.1 Components

- **555 Timer IC (U11)**: Configured in astable mode to generate a square wave.
- **Resistors**:
    - R1: 10kΩ (connected between Vcc and pin 7).
    - R2: 10kΩ (connected between pins 7 and 6).
    - R3: 10kΩ (connected between pin 5 and ground).
- **Capacitor**:
    - C1: 47µF (connected between pin 6 and ground).
- **Connections**:
    - Pin 1: Ground.
    - Pin 2 (TR): Connected to pin 6 (TH).
    - Pin 3 (OUT): Outputs the clock signal.
    - Pin 4 (R): Connected to Vcc (reset pin, active low, tied high to disable reset).
    - Pin 5 (CV): Connected to ground via R3.
    - Pin 8 (Vcc): Connected to the power supply.

6.2 Logic and Operation

- **Astable Mode**: The 555 timer operates in astable mode, producing a continuous square wave.
- **Role in Project**: The 555 timer generates a stable 1 Hz clock signal, which drives the S1 counter stage, with subsequent stages dividing the frequency for tens of seconds, minutes, and hours.

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7. Simulation in Proteus

- The stopwatch circuit was simulated in Proteus, with images showing the main circuit and a separate clock circuit.
- The simulation confirmed that:
    - Each display (S1, S2, M1, M2, H1, H2) incremented correctly.
    - The reset logic initialized the time to 00:00:00.

- The clock control logic allowed starting and stopping the count.
- The 555 timer clock circuit produced a stable 1 Hz signal.

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8. Challenges and Solutions

- **Challenge**: Achieving a precise 1 Hz clock frequency.
  - **Solution**: Adjusted the 555 timer components (R1, R2, C1) to produce approximately 1 Hz.
- **Challenge**: Coordinating multiple counter stages and displays.
  - **Solution**: Used BCD counters and multiplexing to manage the six displays efficiently.

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9. Conclusion

The digital stopwatch project successfully demonstrated the application of digital logic design principles. Each display unit (H1, H2, M1, M2, S1, S2) accurately counted and displayed time, supported by robust reset and clock control logic. The custom 555 timer clock circuit provided a stable 1 Hz signal, ensuring accurate timekeeping. The Proteus simulation validated the design, offering valuable insights into counter design, display interfacing, and timing control.
