Level Shifting Interfaces for Low Voltage Logic[1]

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Abstract – **Efforts are underway to develop CMOS integrated circuits that operate at supply voltages well under** 1 V**. For a variety of reasons it is often desirable to interface these low voltage devices to conventional electronics operating with nominal supply voltages of** 5 V **or** 3.3 V**. This paper examines circuit techniques used to create such interfaces.**

1 Introduction

Driven by the need to reduce power consumption and maintain high reliability in leading edge integrated circuits, the nominal operating supply voltage for these devices is falling steadily [1–3]. Complex integrated circuits operating with supply voltages as low as 0.5 V have been demonstrated. In order to test these devices or insert them into existing systems it is usually necessary to provide interfaces from the low voltage logic to conventional logic devices operating at 5 V or 3.3 V. Commercially available logic interfaces do not support these very low logic levels, and solutions based on discrete components or analog circuits tend to be large and slow.

This paper describes level shifters that have been manufactured using commercial CMOS processes for use as stand-alone interface components. Prototype shifters that can be integrated into the I/O pads on low voltage circuits are also presented. In each case both a *downshifter* and an *upshifter* have been implemented. The downshifter converts a high voltage logic level in the range of 2.5 V to 4.0 V down to a low voltage logic level of around 0.5 V. Similarly, the upshifter converts a low voltage logic signal to a high voltage signal.

2 Level Shifters in Conventional CMOS

In order to resolve a classic "chicken and egg" predicament we needed interfaces to low voltage logic before the low voltage devices themselves were available. These interfaces were required to build test fixtures for low voltage devices, and could not themselves depend on the low voltage process. A generic interface device was designed, which is similar in function and pinout to the

[1]This research was supported by NASA under Space Engineering Research Grants NAG5-8392 and NAG5-7360.

venerable 74LS245 octal, bidirectional buffer. The primary difference in the new interface device is that it requires two supply voltages as the pins on one side of the interface operate at a much lower voltage than the pins on the other side. Commercial CMOS processes with feature sizes of 0.50 μm and 0.35 μm were successfully used to fabricate the interface devices.

The basic downshifter circuit is shown in Figure 1, which is based on a very common design [4, 5]. When driving a high voltage output a normal inverter can be used, where a PMOS transistor is used as a pullup device. However, a conventional inverter does not work well when the low output voltage, V_{DDLO}, is likely to be lower than the threshold voltage, V_T, of a PMOS transistor. Since the transistor gate is driven no lower than ground its gate to source voltage, V_{GS}, will always be less than V_T and the pullup transistor will have very poor drive.

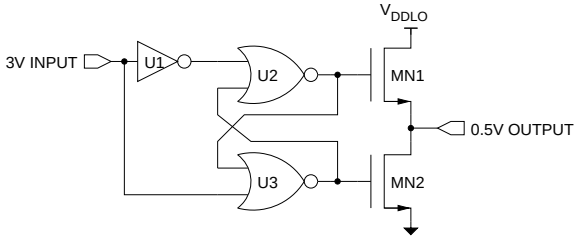

Figure 1: Schematic of Down Shifter

The solution to this problem is to use an NMOS transistor as a pullup device in a source-follower configuration. As long as the difference between the high supply voltage and the low supply voltage is significantly greater than the V_T for an NMOS transistor then the NMOS can provide a strong pullup capability. This output driver arrangement requires complementary drive signals for the two NMOS transistors, which can be accomplished by simply adding an inverter, U1. However, if the raw input and its complement were used to drive the NMOS transistors directly there would be a significant short circuit current during switching. When the input rises there is a brief period of time, equal to the delay through the inverter, when the input signal and its complement signal are both high. If these two signals drove the NMOS transistors directly then both transistors would be enabled at the same time, providing a low impedance path from V_{DDLO} to ground. The resulting current spikes would introduce considerable noise into the power supply rails and would increase the chip's power consumption. Therefore, the cross coupled NOR gates, U2 and U3, are added to prevent an overlap between the gate drive signals for the NMOS output transistors.

Figure 2 shows measured waveforms for this circuit implemented in a commercial 0.35 μm, 3.3 V process. Note that the vertical scales are different for the input and output traces. The input signal is a typical 3.3 V signal while the output has a nominal high level of only 0.5 V. The total propagation delay through the interface, including a standard 3.3 V input pad and a downshifting output pad, is about 3 ns.

Implementing the up shift function is considerably more difficult. When using a typical commercial 3.3 V process the low voltage signals are smaller than the V_T of a transistor, making it very difficult to achieve high speed switching. A simplified schematic of the circuit that is used in our interface is shown in Figure 3. Transistors MP1 and MP3 act as source followers, with MP1 shifting the input signal up by the value of the PMOS V_T. The gate of MP3 is driven from a resistor

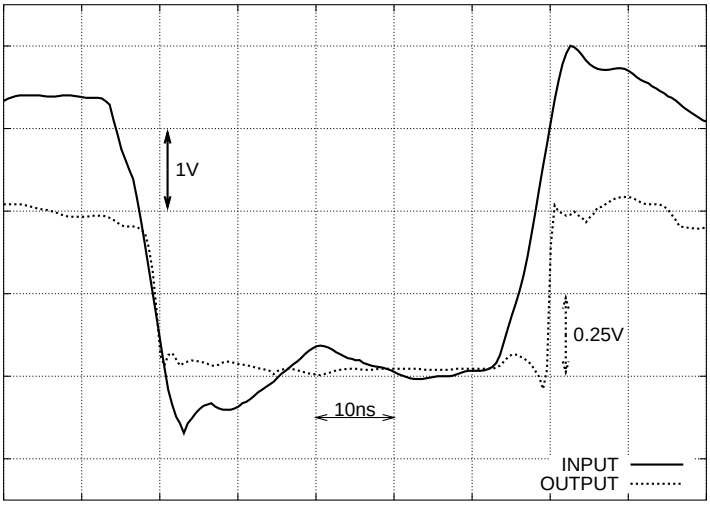

Figure 2: Oscilloscope Data for Down Shifter

divider that produces $V_{DDLO}/2$, so its source will be at a constant level of $V_T + V_{DDLO}/2$. Transistors MN1, MN2, MP2, and MP4 form a differential amplifier that compares the constant voltage at the gate of MN2 with the varying input at the gate of MN1. The output of the differential stage is then buffered to create a usable 3.3 V logic signal.

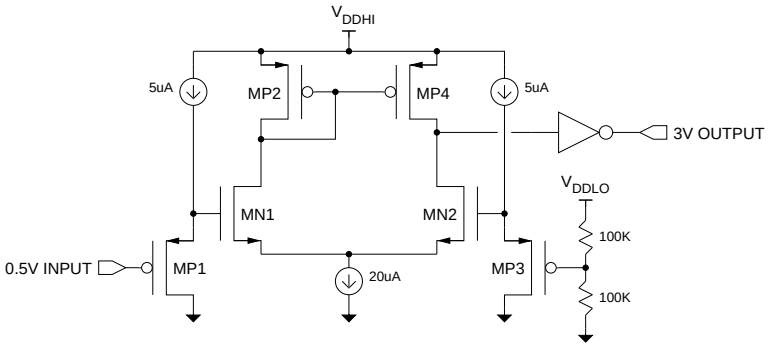

Figure 3: Simplified Schematic of Up Shifter

The resistor divider shown in the schematic is formed from the lightly doped N-Well. A single divider is shared by all eight of the upshifters on the same die, so the total static current consumption is just a few microamps. The absolute value of these resistors is not critical as long as their values are reasonably well matched.

Typical measured waveforms for the upshifter are shown in Figure 4. The added complexity of the upshifter causes it to be slower than the downshifter, but the delay is still only about 10 ns.

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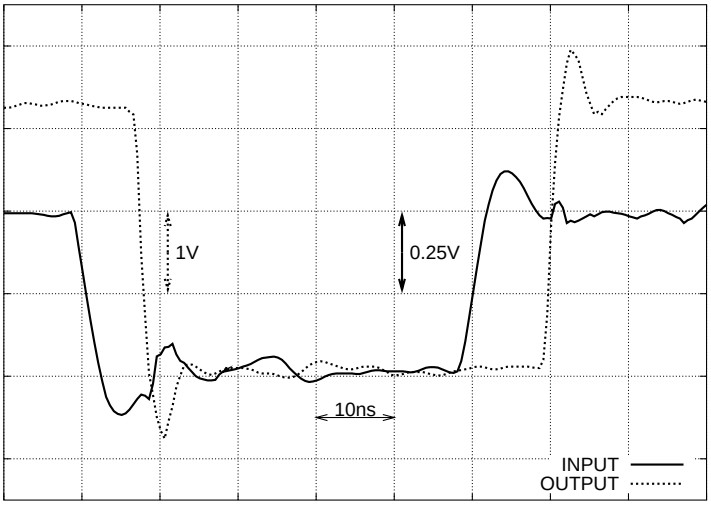

Figure 4: Oscilloscope Data for Up Shifter

3 Level Shifters in Low Voltage CMOS

In some situations it may be desirable to have the level shifting function integrated into the low voltage integrated circuit rather than using a separate interface device. We have also implemented prototype level shifters in a process where the target supply voltage level is only 0.5 V. The basic design of the down shifter remains the same as Figure 1. However, the transistor thresholds in the low voltage process are quite low and as a result there is significant subthreshold leakage. The inverter and NOR gates operate with a supply voltage of 3.3 V so this subthreshold leakage can cause significant static power consumption. The transistors in these gates should be designed with the minimum gate width that will allow the circuit to meet its timing requirements, and the gate length can be increased above the minimum to provide a small increase in V_T. Measured waveforms for this downshifter are shown in Figure 5, where the signal path includes a downshifting input pad and a low voltage (non-level-shifting) output pad.

Designing an upshifter in a low voltage process is not as cumbersome as the circuit given in Figure 3. Low voltage signals are capable of driving NMOS transistors into saturation, so the simplified differential circuit shown in Figure 6 can be used. The low voltage logic on the left provides non-overlapping drive signals to NMOS transistors MN1 and MN2. The cross-coupled PMOS transistors, MP1 and MP2, provide the differential amplification to produce high voltage logic signals. The high voltage inverters shown on the right simply provide sufficient drive for the output pad and external load. The transistors that operate at high voltage levels are optimized to reduce static power consumption, as described above. The measured waveforms for this upshifter, and the non-level-shifting low voltage input pad that drives it, are shown in Figure 7. The propagation delay for this path is considerably improved over the version that used the conventional 3.3 V process.

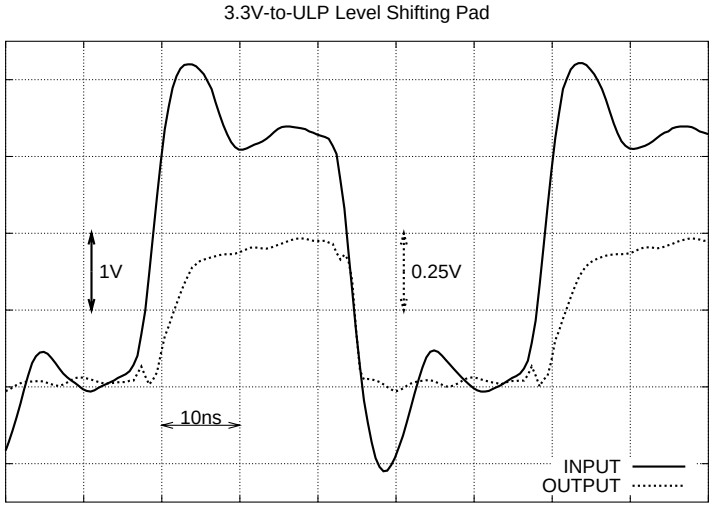

Figure 5: Oscilloscope Data for Down Shifter

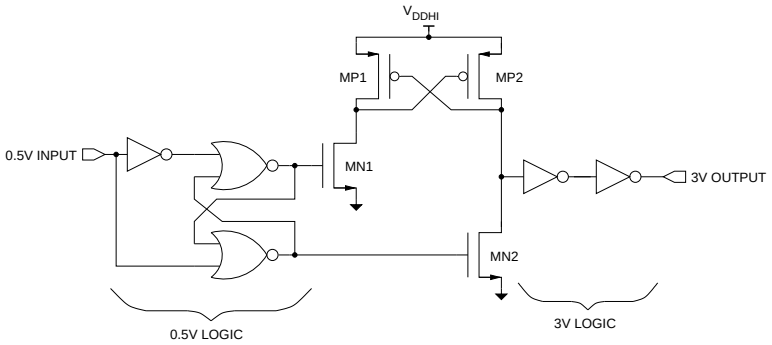

Figure 6: Schematic of Low Voltage Up Shifter

4 Reliability Considerations

The low voltage process used here is derived from a conventional 3.3 V, 0.35 μm process. Since the gate oxide is designed to allow voltages of up to 4.0 V we need not be concerned about the reliability of these oxides when the transistors are used in level shifters.

However, the low voltage process does not use, or need, lightly doped drains (LDD). LDD structures are added to reduce the maximum field at the transistor drain. High fields in this region can give electrons sufficient energy that they are injected into the gate oxide and cause permanent damage, also known as hot electron effects or hot carrier effects. For production circuits it will be necessary to modify the circuits where low voltage transistors are exposed to high drain voltages. Cascode circuits are typically used to accomplish this, as shown in Figure 8 [6–8]. The gates of MN1 and MP1 are biased to $V_{DDHI}/2$ by the resistor divider. When the 3-Volt input is high transistor MN2 conducts and pulls its drain low. As soon as the source of MN1 is pulled below $V_{DDHI}/2 - V_T$ it will also begin conducting and will pull the 3-Volt output node low. Since V_T for the low voltage transistors is quite low with respect to V_{DDHI} MN1 easily reaches saturation and does not seriously compromise the switching speed of the circuit. When the 3-Volt input is

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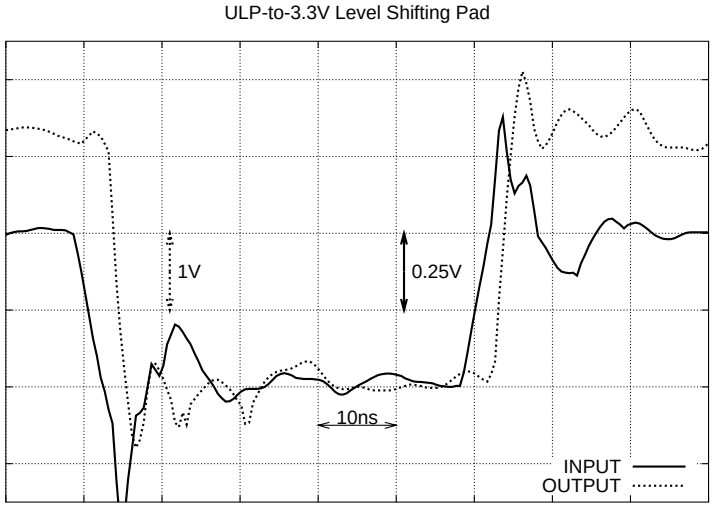

Figure 7: Oscilloscope Data for Up Shifter

then brought low transistor MN2 will be disabled and MP2 will now conduct. MP1 then pulls the output node high. Since the gate of MN1 is at $V_{DDHI}/2$ and its source was left near ground, it will continue to conduct current and the voltage at its source (also the drain of MN2) will rise. Once the voltage at this node rises to approximately $V_{DDHI}/2$ transistor MN1 will be disabled. Thus, V_{DS} for both MN1 and MN2 is roughly half of V_{DDHI} which greatly decreases hot electron damage.

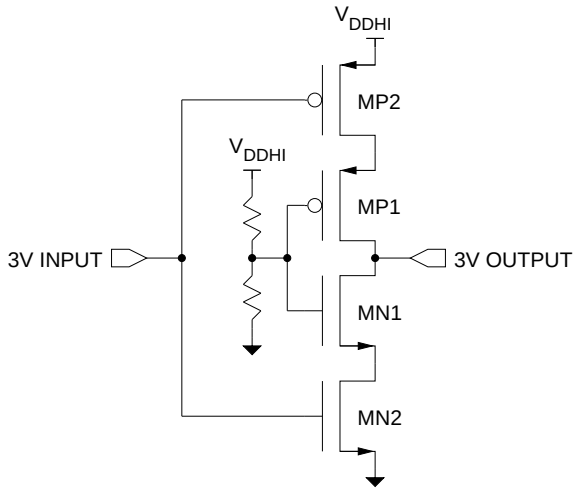

Figure 8: Schematic of Cascode Inverter

5 Conclusion

Level shifting interfaces between 3.3 V and 0.5 V logic have been demonstrated. These circuits can be fabricated in conventional CMOS as standalone interfaces, or they can be integrated into

low voltage CMOS devices operating at very low supply voltages.

6 Acknowledgments

The authors wish to thank Dr. James Murguia of Solid State Scientific for his efforts to develop the low voltage process technology and for his helpful discussions.

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