Power Mixing DAC

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***Abstract*—This is the abstract**

I. Introduction

For this design there is chosen to create a combined traditional DAC, mixer and power amplifier (PA), because this leads to several advantages. One thing is that it results in a more compact solution. A compact solution allows the system to be faster, because there are less parasitic capacitances between the structures. Also the need of matching to 50 ohm between these structures becomes superfluous. Using such a combined system solution has a disadvantage that it is hard to generate high power, because power leakage generates heat which can damage the transistors. Moreover the use of large capacitors or inductors is not possible, because these require too much space to create in silicon. Normally they are placed on the PCB.

Such a solution could be useful for several systems. Mainly for systems that require high speed, low power or lack of sufficient available space for a PCB. One example for such a system is the WiFi connection in a mobile phone.

ll

II. Hardware module

The architecture of this differential system can be separated in several functional blocks: the DAC, mixer, level shifter and amplifier.

PLAATJE

Whereby the DAC translates a 15 bit unary coded digital signal with a sample frequency of maximum 500MHz to an analogue signal. There is chosen for unary coding to increase linearity compared to binary coded signals. One of the reasons is that in the creation process of the transistors, it is more precise to make to transistors of the same size, than to make one with exactly two times the size. This means that the maximum theoretical SNR is 25.8dB.

SNR = 6.02 x n + 1.761 = 25.841dB

The mixer will synchronised the data and up-modulate it with a local oscillator of a 2 GHz square wave. To synchronise the date, a D flip flops will be used. The D flip flop will have two outputs: Q and Q bar. Q will be connect to a NAND port that will mix the LO signal and this signal goes to the level shifter that goes to the PMOS of the end stage. The Q bar will be connected to the NOR port that is connected to the level shifter that goes to the NMOS of the end stage.

The level shifter is responsible for the change of the 1.1V power supply for the thin-oxide transistors to the 5V power supply for the thick-oxide transistors.

The final functional block of this design, the amplifier, should provide enough output power to drive the antenna. The specified output current is 50mA, which means that the output power on the 50 ohm matched antenna should be 20.97dBm.

The aim is to get a IMD3 of at least ...and an efficiency of ...

Sensitivity ...

Noise Floor ...

III. System Components

A. Digital front end

The digital front end (DFE) consist of three parts, D flip flop with a NAND and a NOR port. This can been seen in Fig. 1. The D flip flop will synchronise the incoming data and the NAND/NOR gate will up-modulate the signal with the local oscillator in the digital domain. In comparison with the global schematic of the previous group (Appendix: Fig. 18) the DFE consist of one less D flip flop in the diagram. This will increase the synchronisation of nmos and pmos of the current sources. The DFE works in a high frequency domain and it needs to switch fast. Therefore thin oxide transistors are used. The drawback of this kind of transistors is that they operate at low voltages (max 1.2V), so less power at the output stage. To solve this problem a level shifter is used to increase the power at the output stage. In total 30 DFE circuit and level shifter are made to make the 4 bit power dac, this can be seen in the high level diagram in fig (This diagram will be in the final report).The level shifter will be described in paragraph III-B. The digital front end will be described in this paragraph.

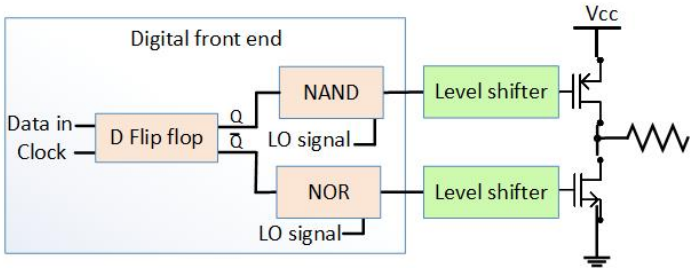


Fig. 1: One side of the diagram of the new digital front end.

1) D flip flop: A D flip flop will be used to synchronise the incoming thermometer coded data to ensure that the transistors of the output stage switch at the same time. There are a couple of challenges that are important to take into account when designing a D flip flop, for example the operation speed and the transition time of the output at the rising clock.

A flip flop can be made in different ways. The two main technologies are in CMOS and CML. The CMOS design is relatively less complex in compare to CML, but in CML there are more parameters that can be modified to tune the output. In this project the CMOS design is used, because it is less

complex, single-ended and it can be realised in a short time period.

The CMOS circuit of previous group is been used as basic circuit. [1] - [2]. The old schematic can been seen in the appendix Fig. 19. The new schematic consist of 32 transistors and is showed in Fig. 2. There are three changes made in compare with the old schematic. The first changes is that a second output is been added to flip flop, as mentioned before to reduce one flip flop in the total schematic. The second changes is a cmos switch is added to improve the synchronisation between the output and the input. The last changes is that the sizes of the nmos and the pmos transistors are changed, to reduce the delay of the output. The size of the nmos and pmos will be further discussed, first the basic principle of a D flip flop will be explained.

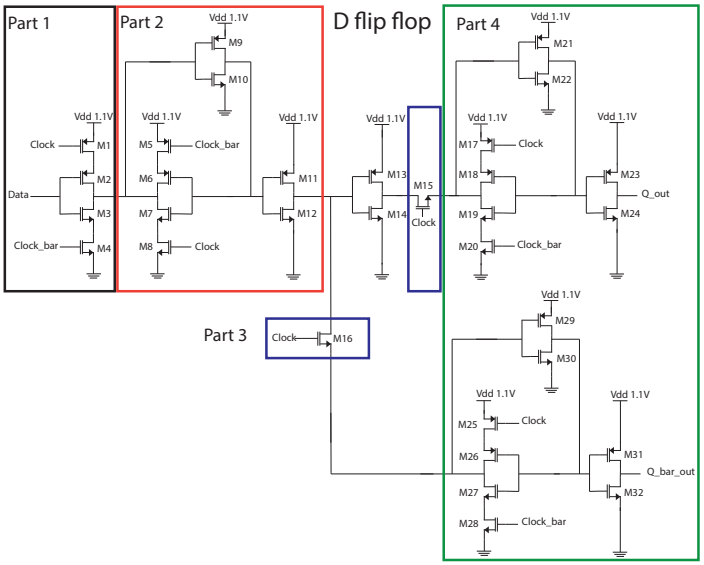


Fig. 2: The improved D flip flop schematic.

The D flip flop works with a master-slave principal. The master will set the data on the rising clock and it will hold the data until the clock is low. The slave will copy the data when the clock is high and hold the data when the clock is low.

To explain this principle, the schematic can be divided into four parts, settle time of the data, master latch, two switches and slave latch. In the first part the data will be set when the clock is low. The second part, the master will follow the signal of the first part when the clock is low and hold the data when the clock is high. In the third part the switches will be closed when the clock is high. The slave latch(part 4) can set the data and when the clock is high it will hold the data.

The size of the pmos and nmos of part one, two and four are the same. The size of the nmos is set on 50nmx90nm (length x width). The length of the pmos is the same, but the width of the pmos is determined with a parameter sweep to get the lowest delay of transition. In the parameter sweep the clock frequency is set on 1 GHz and the data frequency is set on 500MHz. The results are showed in the appendix in Fig. 21 and Fig. 20. The optimal width of the pmos is 180nm. It has the best average delay of transition from high to low and low to high.

With the sizes of the master and slave set, the width of the switching nmos (part 3) needs to be determined. This is also done with a parameter sweep with the same clock and data frequency. The results of the parameter sweep are shown in Fig. 22 and Fig. 23 in the appendix. The optimal value of the width is 360nm. The results of this value is compared with the previous schematic and is shown in Fig. 4 and Fig. 3. The delay of transmission is reduced 18.5ps for Q and 3.64ps for Q bar when the output goes from high to low and when the output goes from low to high the delay is reduced with 20.4ps for Q and 13.5ps. With this result the synchronisation will be improved.

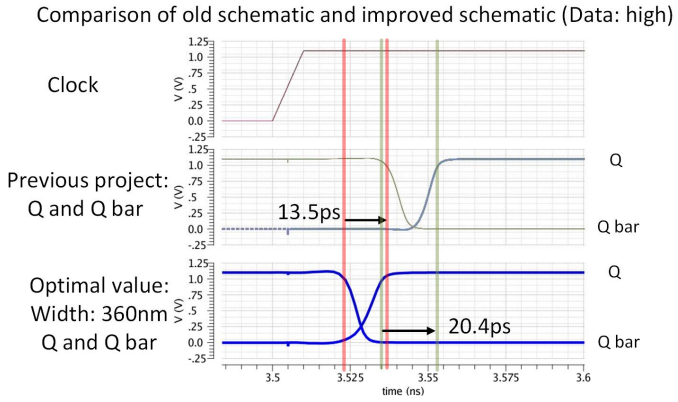


Fig. 3: Comparison of the delay of transition between the old schematic and the new schematic when the data is high

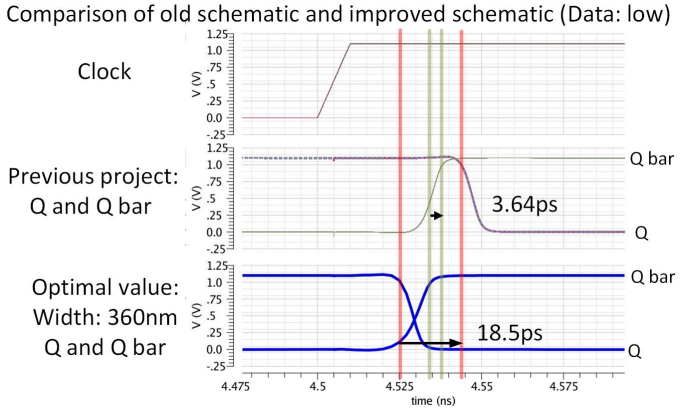


Fig. 4: Comparison of the delay of transition between the old schematic and the new schematic when the data is low.

With all the transistors size known the critical point can be measured. The minimal time that the data needs to be set is 40ps before the clock is high. The transition delay of Q is 26.46ps and Q bar is 20.7ps when the data is high. When the data is low the delay of Q is 22ps and Q bar is 25ps. This is shown in Fig. 5 and Fig. 6.

2) NAND/NOR gate: The NAND and NOR will up-modulate the local oscillator signal (LO) with the data from the D flip flop. This will happen in the digital domain with an LO signal of 2Ghz square wave.

The design of a NAND and NOR is shown in Fig. 7 and Fig. 8.

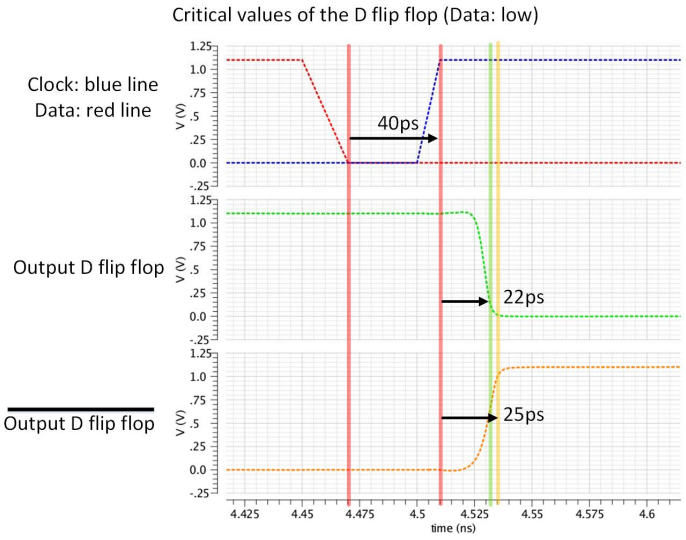


Fig. 5: The critical values when the data goes from high to low

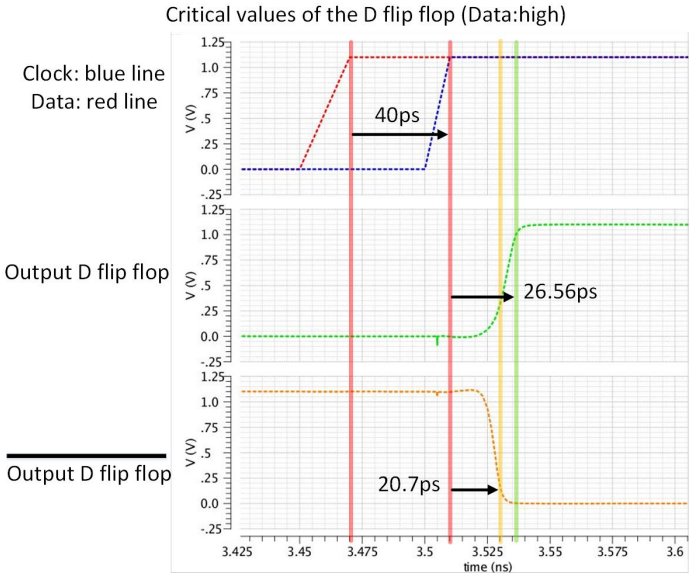


Fig. 6: The critical values when the data goes from high to low.

The NAND port has two pmos in parallel and 2 nmos in series. In a normal cmos inverter the size of the pmos is 2 times larger than the nmos. In this situation two nmos transistors are in series, so the width of the nmos needs to be 2 times larger to get an equal resistance. The two pmos remains the same value as in a normal cmos inverter, thus the nmos and pmos have the same size of transistor of 50nmx180nm (length x width).

The NOR port has two pmos in serie and 2 nmos in parallel. The width of the PMOS is 4 times larger than the nmos, because the two pmos are in serie and of the relation between the nmos and pmos mobility factor. The size of the nmos will be 50nmx90nm (length x width) and pmos 50nmx360nm (length x width).

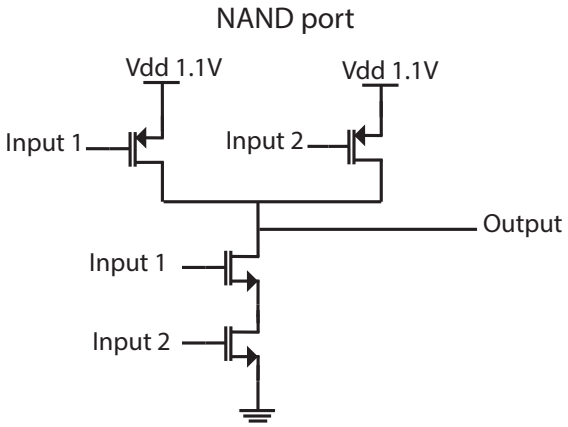


Fig. 7: The schematic of the NAND port.

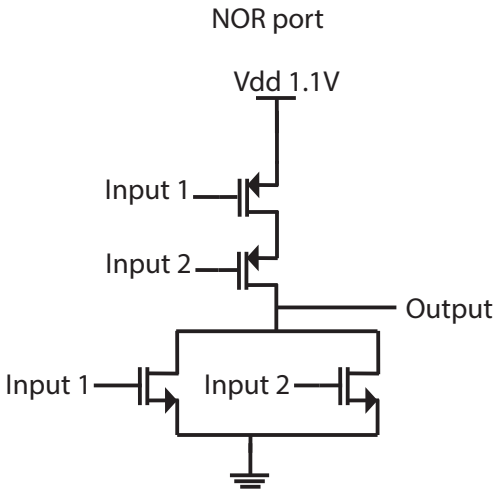


Fig. 8: The schematic of the NAND port.

B. *Levelshifters*

To generate sufficiënt output power thick oxide transitors are used at the output stage. One of the problems with this is that these transistors have a much larger threshold voltage and that they operate at larger supply voltages than the low voltage transistors. Because of this the fast low voltage transitors used in the digital front end and for mixing cannot generate a large enough V_{ON}. Raising the supply voltage to the low voltage transistors in order to increase the output voltage of the mixers will break them. So special care has to be taken when a transition from a low voltage circuit to high voltage thick oxide transistors. To this end a level shifter is designed. In this design special care will be taken to ensure that the voltages across any low voltage transistor will not exceed 1.1V, so they will not break. On the output side it has to be able to drive very large transistors. The driven NMOS transistors will have to be supplied with a voltage of 0V(off) to 2V(on) and the driven PMOS transistors with a voltage of 5V(off) to 3V(on).

In [2] a design for the levelshifter was proposed, but they were not able to integrate it with the rest of their design. However, they did show work that it worked in a standalone simulation. The main problem are difficulties with the cadence models of the thick oxide transistors used for

simulation. These models show strange behavior and have an unrealistically high threshold voltage of 1.5V. In order to create a functioning simulation this was changed to a more realistic threshold voltage of 0.7V. This gives a larger VON, making the transistors conduct more current for a smaller size. This is necessary, because the transistors being driven by the level shifter will be very large. Therefore a large driving current must be supplied by the levelshifter. Another problem with the models is that they breakdown with too high VON and starts flowing through the base. This also limits the driving capability of the levelshifter. Also a design proposed in [3] was considered. But due to the increased complexity combined with our models and its multiple stages, which are bad for timing performance, this design was not used. That design has an propagation delay of roughly 10 ns, which is not acceptable for this paper's design.

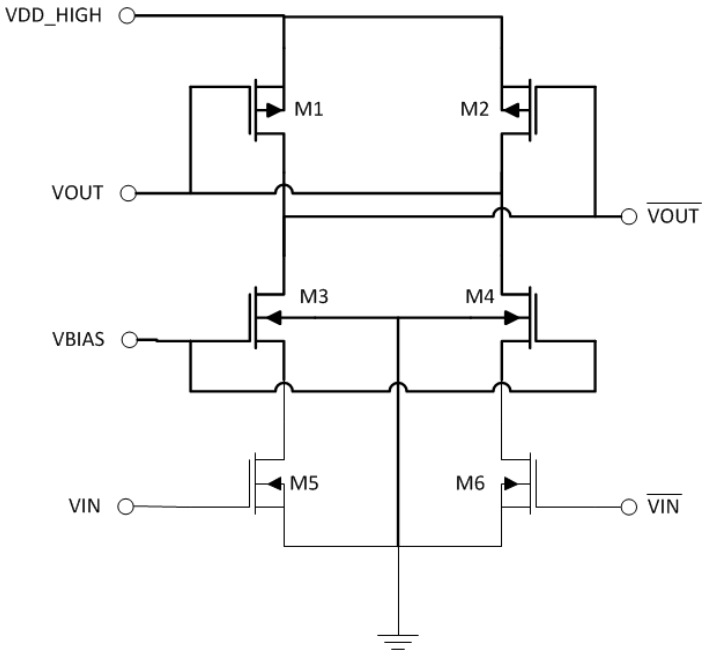


Fig. 9: Schematics of the levelshifter, thick wires indicate a high voltage regime and thing the low voltage transistors

The chosen design is a modified version of the one proposed in [2] and is shown in Fig. 9. The inputs are connected to the gates of the low voltage transistors M5 and M6 and have an input range of 0V(off) to 1.1V(on). For correct operation VIN and $\overline{VIN}$ must be each other's logical inverse. VBIAS is set to ??V and is connected to the gates of M3 and M4. These transistors protect M5 and M6 from the high supply voltage. M1 and M2 provide an positive feed back loop, which makes the circuit function. Its operation is explained using a low to high transition, so initially VIN is 0V, $\overline{VIN}$ is 1.1V, VOUT is on its off value and $\overline{VOUT}$ is 2V. In this situation only the right branch is conducting current, because $\overline{VIN}$ is high and since there is no current in the left branch $\overline{VOUT}$ is low. When VIN transitions to a high state, it starts conducting current, forcing VM5 to go a bit higher, as well as $\overline{VOUT}$. Because $\overline{VOUT}$ increases, the current through the right branch decreases as well as VOUT. The decreased VOUT makes the left branch conduct more current and $\overline{VOUT}$ go higher. Due to this postive feedback loop VOUT will go to VDD. To drive the NMOS transistors the levelshifter also needs another output stage, which can consist of a thick oxide PMOS and an NMOS transistor. the PMOS will be driven by VOUT and the NMOS by VIN. To gether the can rase the ON voltage to 2V compared to the output voltage of 1.1V from the low voltage transistors.

A parameter sweep is shown in Fig. 10. It shows that the circuit should be able to function. The sweep is simulated while the level shifter is driving the gate of a thick oxide PMOS transistor that is 60 μm wide and 300 nm long. In this sweep the width of transistor M2 is swept from 30 to 60 μm and it shows the impact of this parameter on the rise time. Using this simulation the width of M2 is chosen to be 45 μm, because it sets the on voltage close to the desired 3V and the difference in risetime compared to larger widths is very small. However, to meet the requirments of a 2 GHz LO frequency, the circuit still must become significantly faster.

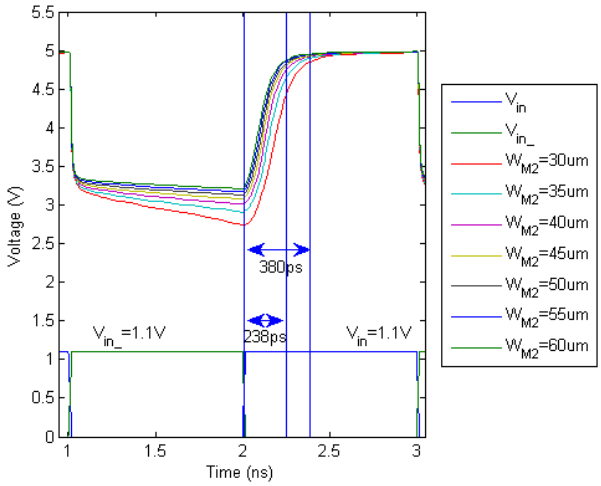


Fig. 10: Early simulation results of the levelshifter

A final aspect of interest is the power consumption of the levelshifter. This is determined mostly by the current necessary for driving the load transistor. The gates of the load are both charged and discharged via the levelshifter, causing most of the powerconsumption. But also the levelshifter's transistors are relatively large and cost significant power to switch. Simulation results are not available yet.

C. Current Sources

The final stage of the power DAC are the current sources. They provide a differential output over a 50Ω resistor. This setup is shown in Fig. 11.

Due to the local oscillator, the current will alternate between the path through CS1 and CS4 (see Fig. 12a) and the the path through C3 and C2. (see Fig. 12b).

The first design parameters are the voltage supply and the switching devices. Because the DAC should be able to produce 50mA through a 50Ω resistor, the maximum voltage drop will be 2.5V. This already cancels out lower voltage supplies such as 1.2V and 2.5V. The resulting options are 3.3V and 5V. Because the stage consist of two current sources, the voltage headroom will be very limited in the 3.3V voltage supply. Therefore a 5V supply will be used as V_{dd}. This, along with the high switching speeds, limits the switching

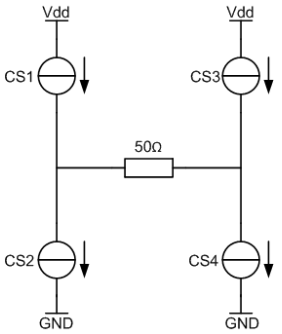
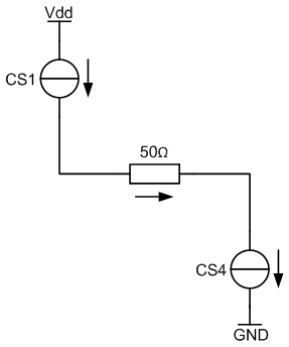
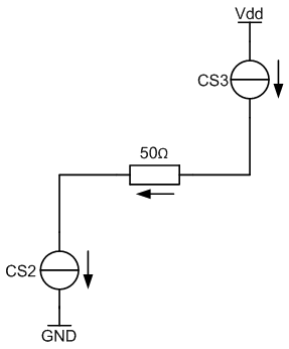


Fig. 11: The final stage of the power DAC: The current sources which will provide the differential output through the resistor.



(a) One current-steered cycle.



(b) The other current-steered cycle. Vdd is 5V and the maximum current is 50mA.

devices to the thick-oxide CMOS technology.

Due to the thick-oxide CMOS technology, the width and length of the CMOS are the only parameters. The most straightforward design method subscribes that the CMOS should always be in saturation so that the current through the CMOS is nearly independent, without channel-length modulation taken into account, of the drain-source voltage of the CMOS. This is directly related to the output impedance of the the switched current source. Therefore Eq. 1 should be valid whatever the drain-source voltage.

$$\mathrm{V}_{DS} > V_{TH} + V_{GS} \quad (1)$$

The drain-source voltage of both the NMOS is minimal when the current through the resistor is maximal. This results in a minimum drain-source voltage of 1.25V. Because Eq. 1 should be valid independent of the output, the maximum gate-source provided by the level shifter should be 1.95V, because the threshold voltage of the thick-oxide CMOS is 0.7V. Along with Eq. 2, this would provide a viable current sink.

$$\mathrm{I}_D = \tfrac{1}{2}\mu_n C_{ox}\tfrac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \quad (2)$$

So by designing a current sink which operates at a V_{gs} of 1.95V, the switching current sink wil always be in saturation. This provides a high output impedance and thus a high IMD3. Another advantage is the increase in efficiency.

Due to the difference in mobility of electrons and holes, the mobility of a electron is three times higher than the mobility of a hole, the length of the NMOS transistor will be three times higher then the length of the PMOS transistor. Though an larger length has some advantages, decrease in mismatch en less noise, it also means a larger width to maintain the required current through the transistor. A larger width however, means increasing inputcapacitance. To decrease the needed specifications on the level shifter, the length of the PMOS has been chosen to be the minimum possible with the thick-oxide technology, i.e. 300nm. The length of the NMOS is then 900nm.

The width of the NMOS transistors has been determined by a parametric sweep. The width can then be determined so that the current through the transistor is 3.3mA. With the circuit found in Fig. 13 the result is found in Fig. 14.

So the width of the first NMOS should be 30um to guarantee that it will sink 3.3mA when the V_{GS} is 1.95V. Due to the channel-length modulation, it is not sufficient to copy the transistor 15 times. So to determine the width of the second transistor, another transistor will be added to the circuit in Fig. 13 and the V_{out-} will be altered to 2.333V. Then the sweep will take place again until the width has been found for which the circuit sinks 6.667mA. This will be repeated until 15 transistor are switched in parallel and are able to sink 50mA. The list of all widths can be found in table I in the appendix.

The same technique has been used for the PMOS transistors. Due to the dummy technology, which was not able to simulate width over 100um, each bit will be represented by to PMOS in parallel so that the width is maintained within the 100um. This list can also be found in the appendix, table II.

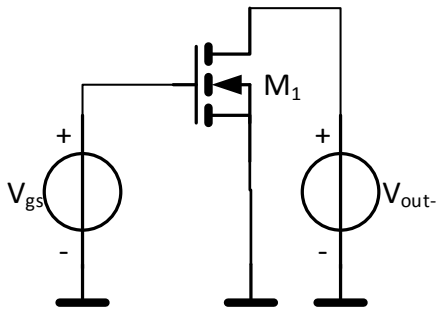


Fig. 13: The circuit used to determine the required width of the transistor to sink 3.3mA. Vout- is 2.4167V ans Vgs is 1.95V.

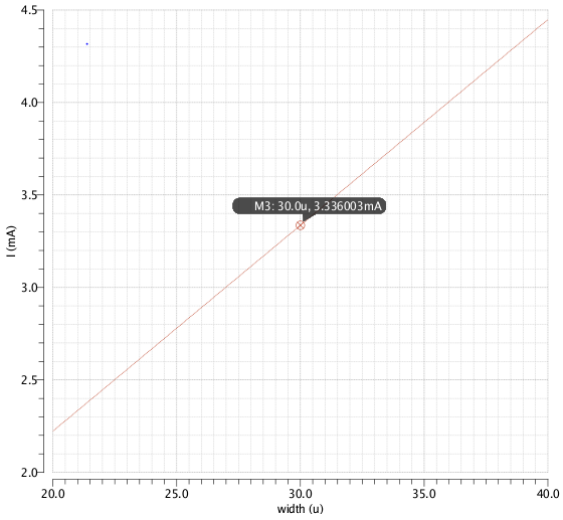


Fig. 14: The current through the transistor versus its width. To make sure that the current through the transistor is 3.3mA, the width should be 30um.

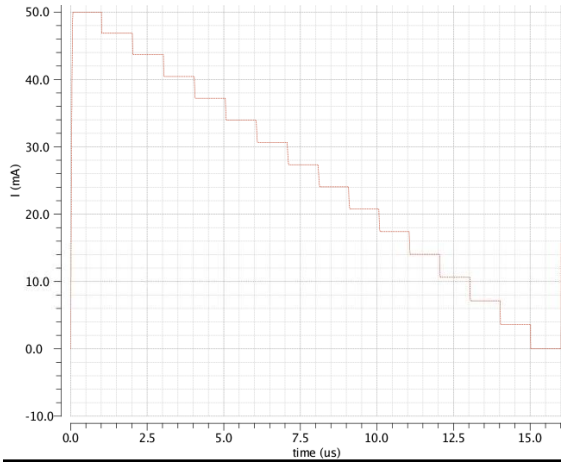


Fig. 15: A sweep through all possible currents, with a maximum of 50mA and a minimum of 0mA.

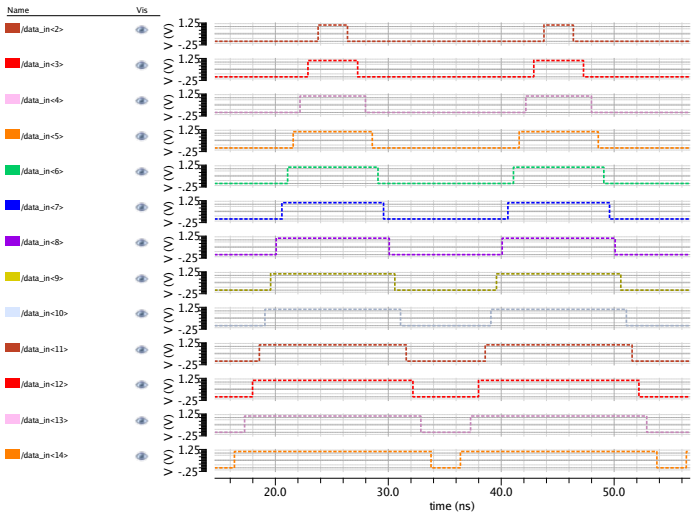


Fig. 16: Thermometer single tone voltage output.

When all of these transistors are designed in a single set-up, that is a setup as seen in 12a, a sweep can be made through all bits. The results can be found in Fig. 15.

Next paper I will elaborate on the results with the chosen transistors.

IV. Results and Analysis

The specified specifications are verified by the use of simulations. While providing a one tone signal, a transient measurement of the output power is simulated. This to verify a correct functioning DAC, that translates the digitals signals as supposed. This holds that the 15 bit digital unary code is translated to an analogue signal with 16 level resolution.

Next a DFT of the output voltage is simulated to see the spectral content of the one tone model. This to find the power of the harmonic distortion and the spurious-free dynamic range (SFDR). The SFDR describes the power of the fundamental signal to the strongest spurious signal at the output, which is most commonly the second harmonic.

Furthermore a two tone test is simulated, the two tone test is useful test the linearity of the DAC. Non-linear behaviour generates intermodulation products at the output of the DAC. The power of these intermodulation products will examined, especially the third intermodulation product (IM3). Because the IM3 frequencies are very close to the fundamental frequency (at 2f2-f1 and 2f1-f2), it is almost impossible to filter it out of the output signal; therefore, it is better to prevent creating them.

V. Conclusion

This is the conclusion

Acknowlegdements

Dr. G. Radulov

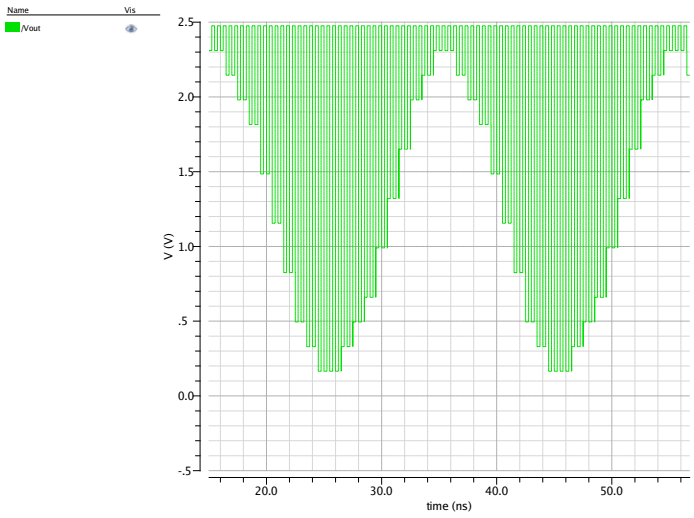


Fig. 17: SoC voltage output.

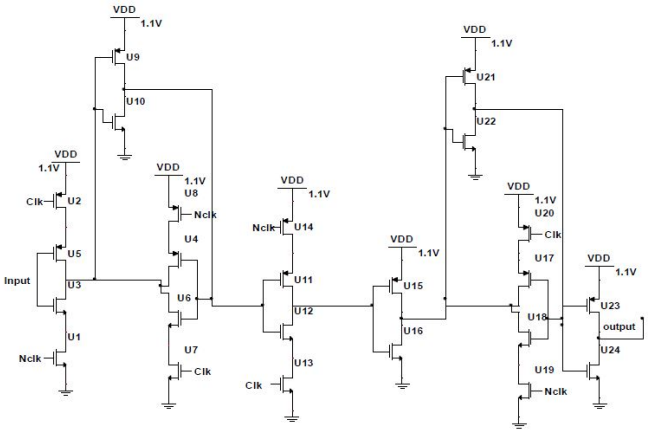


Fig. 19: D flip flop schematic from previous group

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VI. APPENDIX

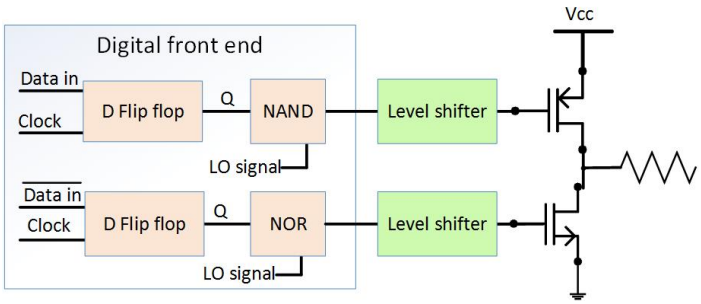

Fig. 18: Global schematic of the previous group.

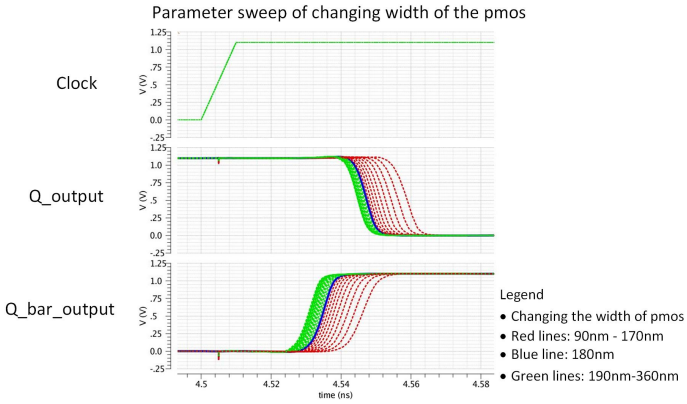

Fig. 20: Parametersweep of changing the width of the pmos when the data is low.

TABLE I: This table describes which widths and lengths are used for which NMOS transistors. M1 is the MOSFET which is associated with the lowest current while M15 is associated with the highest current.

NMOS	Width(um)	Length (um)
M1	30.00	0.9
M2	30.17	0.9
M3	30.30	0.9
M4	30.30	0.9
M5	30.36	0.9
M6	30.44	0.9
M7	30.49	0.9
M8	30.57	0.9
M9	30.66	0.9
M10	30.74	0.9
M11	30.83	0.9
M12	30.95	0.9
M13	31.05	0.9
M14	31.18	0.9
M15	31.33	0.9

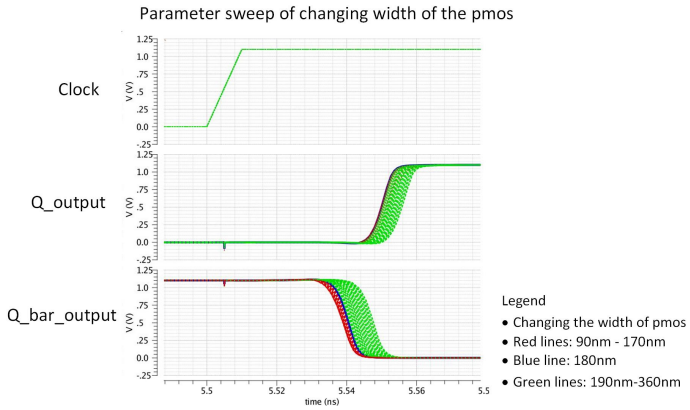

Fig. 21: Parametersweep of changing the width of the pmos when the data is high.

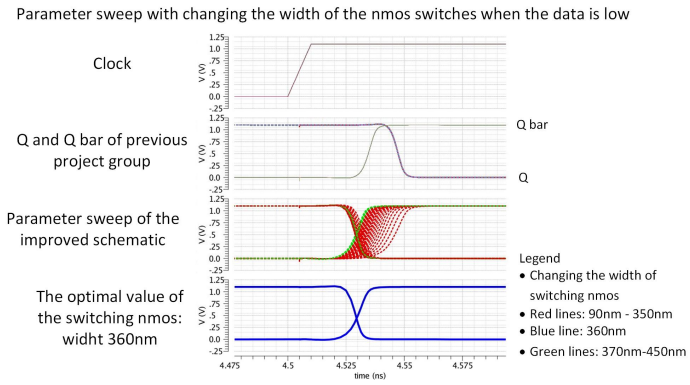

Fig. 22: Parameter sweep of changing the width of the switching nmos when the data is low.

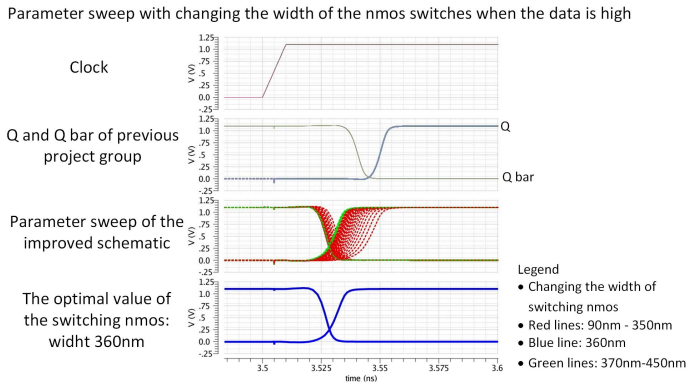

Fig. 23: Parameter sweep of changing the width of the switching nmos when the data is high

TABLE II: This table describes which widths and lengths are used for which PMOS transistors. M1 is the MOSFET which is associated with the lowest current while M15 is associated with the highest current.

PMOS	Width(um)	Length (um)
M1	56.23	0.3
M2	57.25	0.3
M3	57.63	0.3
M4	57.84	0.3
M5	58.04	0.3
M6	58.28	0.3
M7	58.56	0.3
M8	58.87	0.3
M9	59.21	0.3
M10	59.57	0.3
M11	59.95	0.3
M12	60.36	0.3
M13	60.82	0.3
M14	61.31	0.3
M15	61.87	0.3