Power Mixing DAC

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***Abstract*—This is the abstract**

I. INTRODUCTION

For this design there is chosen to create a combined traditional DAC, mixer and power amplifier (PA), because this leads to several advantages. One thing is that it results in a more compact solution. A compact solution allows the system to be faster, because there are less parasitic capacitances between the structures. Also the need of matching to 50 ohm between these structures becomes superfluous. Using such a combined system solution has a disadvantage that it is hard to generate high power, because power leakage generates heat which can damage the transistors. Moreover the use of large capacitors or inductors is not possible, because these require too much space to create in silicon. Normally they are placed on the PCB.

Such a solution could be useful for several systems. Mainly for systems that require high speed, low power or lack of sufficient available space for a PCB. One example for such a system is the WiFi connection in a mobile phone.

II. HARDWARE MODULE

The architecture of this differential system can be separated in several functional blocks: the DAC, mixer, level shifter and amplifier.

PLAATJE

Whereby the DAC translates a 15 bit unary coded digital signal with a sample frequency of maximum 500MHz to an analogue signal. There is chosen for unary coding to increase linearity compared to binary coded signals. One of the reasons is that in the creation process of the transistors, it is more precise to make to transistors of the same size, than to make one with exactly two times the size. This means that the maximum theoretical SNR is 25.8dB.

$$SNR = 6.02 \times n + 1.761 = 25.841 dB$$

The mixer will synchronised the data and up-modulate it with a local oscillator of a 2 GHz square wave. To synchronise the date, a D flip flops will be used. The D flip flop will have two outputs: Q and Q bar. Q will be connect to a NAND port that will mix the LO signal and this signal goes to the level shifter that goes to the PMOS of the end stage. The Q bar will be connected to the NOR port that is connected to the level shifter that goes to the NMOS of the end stage.

The level shifter is responsible for the change of the 1.1V power supply for the thin-oxide transistors to the 5V power supply for the thick-oxide transistors.

The final functional block of this design, the amplifier, should provide enough output power to drive the antenna. The specified output current is 50mA, which means that the output power on the 50 ohm matched antenna should be 20.97dBm.

The aim is to get a IMD3 of at least âĂę and an efficiency of âĂę

SensitivityâĂę

Noise FloorâĂę

III. SYSTEM COMPONENTS

A. *Digital front end*

The digital front end (DFE) consist of three parts, D flip flop with a NAND and a NOR port. This can been seen in Fig. 1. The D flip flop will synchronise the incoming data and the NAND/NOR gate will up-modulate the signal with the local oscillator in the digital domain. In comparison with the global schematic of the previous group (Appendix: Fig. 15) the DFE consist of one less D flip flop in the diagram. This will increase the synchronisation of nmos and pmos of the current sources. The DFE works in a high frequency domain and it needs to switch fast. Therefore thin oxide transistors are used. The drawback of this kind of transistors is that they operate at low voltages (max 1.2V), so less power at the output stage. To solve this problem a level shifter is used to increase the power at the output stage. In total 30 DFE circuit and level shifter are made to make the 4 bit power dac, this can be seen in the high level diagram in fig (This diagram will be in the final report).The level shifter will be described in paragraph III-B. The digital front end will be described in this paragraph.

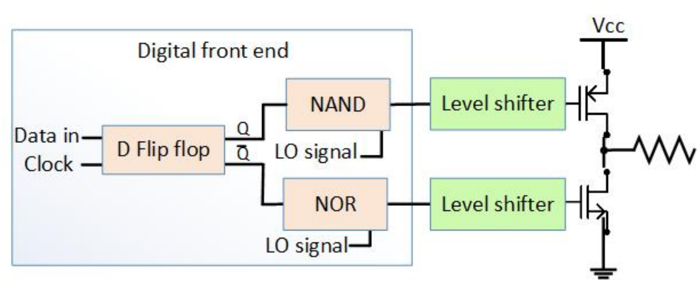


Fig. 1: One side of the diagram of the new digital front end.

1) D flip flop: A D flip flop will be used to synchronise the incoming thermometer coded data to ensure that the transistors of the output stage switch at the same time. There are a couple of challenges that are important to take into account when designing a D flip flop, for example the operation speed and the transition time of the output at the rising clock.

A flip flop can be made in different ways. The two main technologies are in CMOS and CML. The CMOS design is relatively less complex in compare to CML, but in CML there are more parameters that can be modified to tune the output. In this project the CMOS design is used, because it is less complex, single-ended and it can be realised in a short time period.

The CMOS circuit of previous group is been used as basic circuit. [1] - [2]. The old schematic can been seen in the appendix Fig. 16. The new schematic consist of 32 transistors and is showed in Fig. 2. There are three changes made in compare with the old schematic. The first changes is that a second output is been added to flip flop, as mentioned before to reduce one flip flop in the total schematic. The second changes is a cmos switch is added to improve the synchronisation between the output and the input. The last changes is that the sizes of the nmos and the pmos transistors are changed, to reduce the delay of the output. The size of the nmos and pmos will be further discussed, first the basic principle of a D flip flop will be explained.

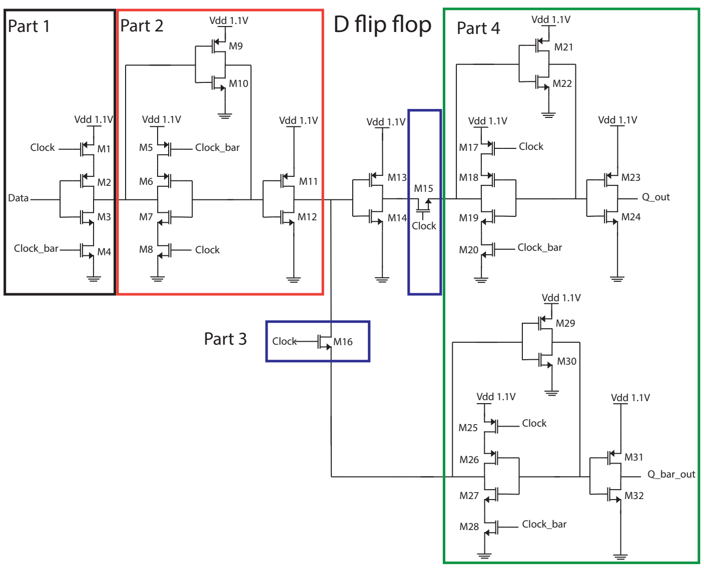


Fig. 2: The improved D flip flop schematic.

The D flip flop works with a master-slave principal. The master will set the data on the rising clock and it will hold the data until the clock is low. The slave will copy the data when the clock is high and hold the data when the clock is low.

To explain this principle, the schematic can be divided into four parts, settle time of the data, master latch, two switches and slave latch. In the first part the data will be set when the clock is low. The second part, the master will follow the signal of the first part when the clock is low and hold the data when the clock is high. In the third part the switches will be closed when the clock is high. The slave latch(part 4) can set the data and when the clock is high it will hold the data.

The size of the pmos and nmos of part one, two and four are the same. The size of the nmos is set on 50nmx90nm (length x width). The length of the pmos is the same, but the width of the pmos is determined with a parameter sweep to get the lowest delay of transition. In the parameter sweep the clock frequency is set on 1 GHz and the data frequency is set on 500MHz. The results are showed in the appendix in Fig. 18 and Fig. 17. The optimal width of the pmos is 180nm. It has the best average delay of transition from high to low and low to high.

With the sizes of the master and slave set, the width of the switching nmos (part 3) needs to be determined. This is also done with a parameter sweep with the same clock and data frequency. The results of the parameter sweep are shown in Fig. 19 and Fig. 20 in the appendix. The optimal value of the width is 360nm. The results of this value is compared with the previous schematic and is shown in Fig. 4 and Fig. 3. The delay of transmission is reduced 18.5ps for Q and 3.64ps for Q bar when the output goes from high to low and when the output goes from low to high the delay is reduced with 20.4ps for Q and 13.5ps. With this result the synchronisation will be improved.

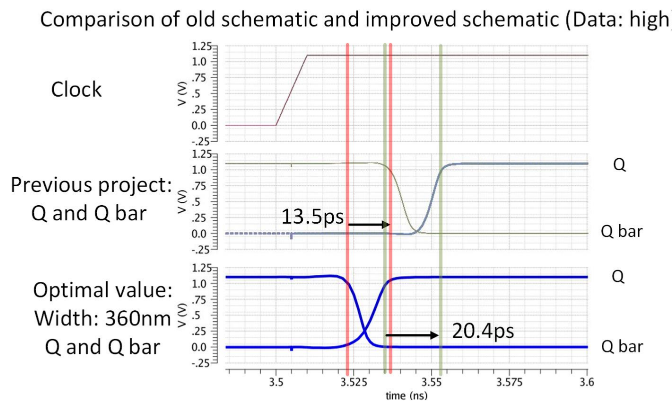


Fig. 3: Comparison of the delay of transition between the old schematic and the new schematic when the data is high

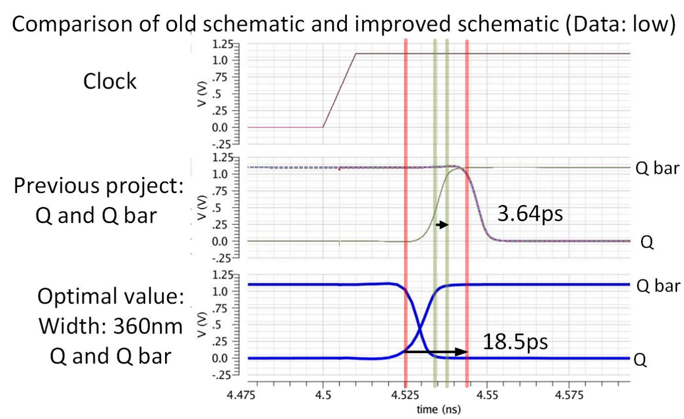


Fig. 4: Comparison of the delay of transition between the old schematic and the new schematic when the data is low.

With all the transistors size known the critical point can be measured. The minimal time that the data needs to be set is 40ps before the clock is high. The transition delay of Q is 26.46ps and Q bar is 20.7ps when the data is high. When the data is low the delay of Q is 22ps and Q bar is 25ps. This is shown in Fig. 5 and Fig. 6.

2) NAND/NOR gate: The NAND and NOR will up-modulate the local oscillator signal (LO) with the data from the D flip flop. This will happen in the digital domain with an LO signal of 2Ghz square wave.

The design of a NAND and NOR is shown in Fig. 7 and Fig. 8.

The NAND port has two pmos in parallel and 2 nmos in series. In a normal cmos inverter the size of the pmos is 2 times larger than the nmos. In this situation two nmos transistors are

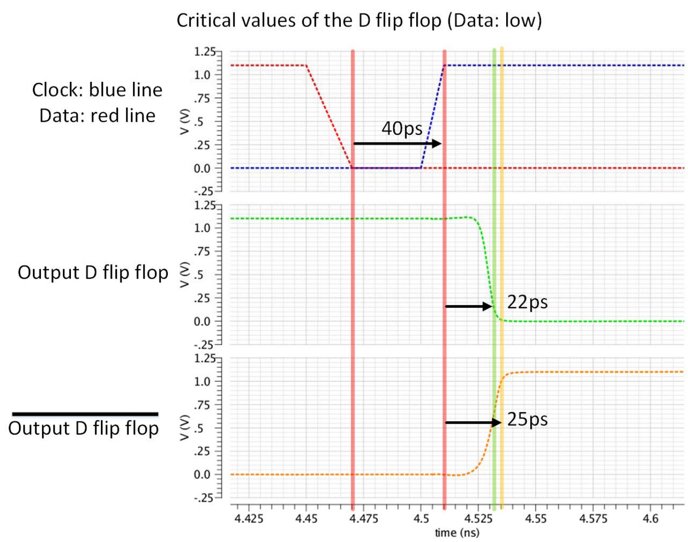


Fig. 5: The critical values when the data goes from high to low

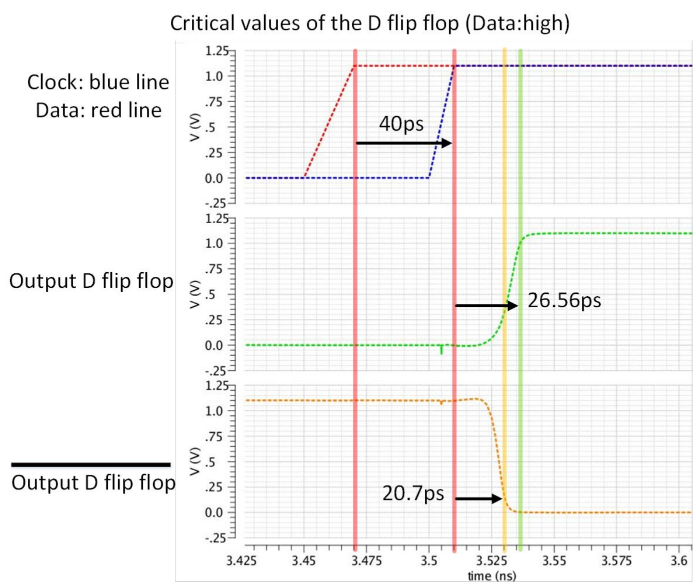


Fig. 6: The critical values when the data goes from high to low.

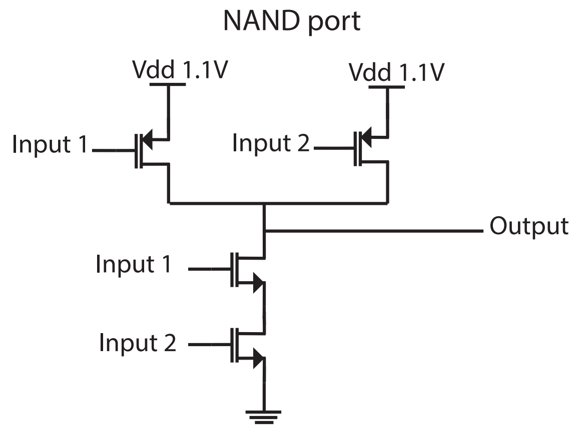


Fig. 7: The schematic of the NAND port.

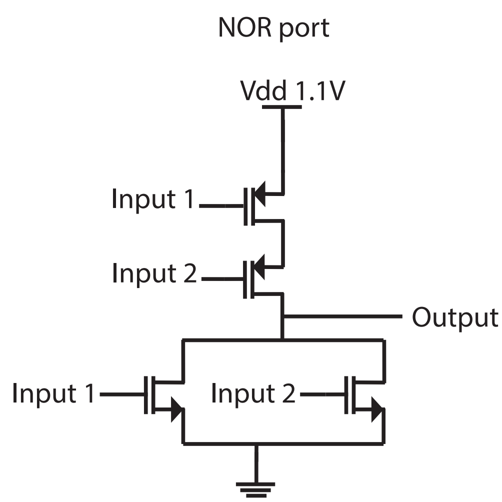


Fig. 8: The schematic of the NAND port.

in series, so the width of the nmos needs to be 2 times larger to get an equal resistance. The two pmos remains the same value as in a normal cmos inverter, thus the nmos and pmos have the same size of transistor of 50nmx180nm (length x width).

The NOR port has two pmos in serie and 2 nmos in parallel. The width of the PMOS is 4 times larger than the nmos, because the two pmos are in serie and of the relation between the nmos and pmos mobility factor. The size of the nmos will be 50nmx90nm (length x width) and pmos 50nm0x360nm (length x width).

B. Levelshifters

To generate sufficië output power thick oxide transitors are used at the output stage. One of the problems with this is that these transistors have a much larger threshold voltage and that they operate at larger supply voltages than the low voltage transistors. Because of this the fast low voltage transitors used in the digital front end and for mixing cannot generate a large enough V_{ON}. Raising the supply voltage to the low voltage transistors in order to increase the output voltage of the mixers will break them. So special care has to be taken when a transition from a low voltage circuit to high voltage thick oxide transistors. To this end a level shifter is designed. In this design special care will be taken to ensure that the voltages accros any low voltage transistor will not exceed 1.1V, so they will not break. On the output side is has to be able to drive relatively large transistors. Also in the on state it must supply a voltage of approximately 2V and in the offstate a voltage smaller than 0.7V.

In [2] a design for the levelshifter was proposed, but they were not able to integrate it with the rest of their design. However, they did show work that it worked in a standalone simulation. The main problem are difficulties with the cadence models of the thick oxide transistors used for simulation. These models show strange behavior and have an unrealistically high threshold voltage of 1.5V. Also a design proposed in [3] was considered. But due to the increased complexity combined with our models and its multiple stages, which are bad for timing performance, this design was not used. That design has an propagation delay of roughly 10 ns, which is not acceptable for this paper's design.

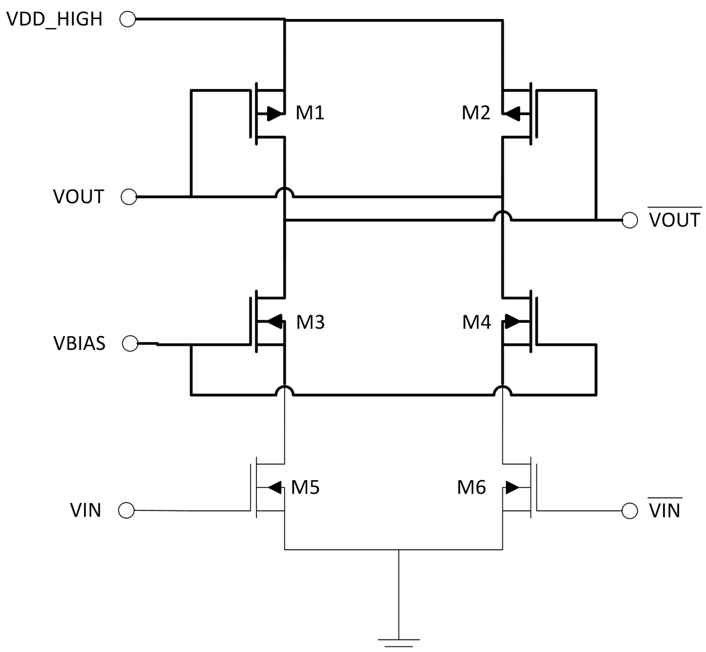


Fig. 9: Schematics of the levelshifter, thick wires indicate a high voltage regime and thing the low voltage transistors

The chosen design is a modified version of the one proposed in [2] and is shown in Fig. 9. The inputs are connected to the gates of the low voltage transistors M5 and M6 and have an input range of 0V(off) to 1.1V(on). For correct operation VIN and $\overline{\text{VIN}}$ must be each other's logical inverse. VBIAS is set to ??V and is connected to the gates of M3 and M4. These transistors protect M5 and M6 from the high supply voltage. M1 and M2 provide an positive feed back loop, which makes the circuit function. Its operation is explained using a low to high transition, so initially VIN is 0V, $\overline{\text{VIN}}$ is 1.1V, VOUT is on its off value and $\overline{\text{VOUT}}$ is 2V. In this situation only the right branch is conducting current, because $\overline{\text{VIN}}$ is high and since there is no current in the left branch $\overline{\text{VOUT}}$ is low. When VIN transitions to a high state, it starts conducting current, forcing VM5 to go a bit higher, as well as $\overline{\text{VOUT}}$. Because $\overline{\text{VOUT}}$ increases, the current through the right branch decreases as well as VOUT. The decreased VOUT makes the left branch conduct more current and $\overline{\text{VOUT}}$ go higher. Due to this postive feedback loop VOUT will go to VDD.

Early simulation results are shown in Fig. 10. It shows that the circuit should be able to function. However in this simulation it is till far to slow with a rise time of about 200 ps, while it is not loaded by the output stage. In the final implementation it should operate at a frequency of 2 GHz, which means that it should be able to transition from low to high and back every 500 ps. This is still being worked on and an issue for further investigation.

C. Current Sources

The final stage of the power DAC are the current sources. They provide a differential output through a 50Ω resistor. This setup is shown in Fig. 11.

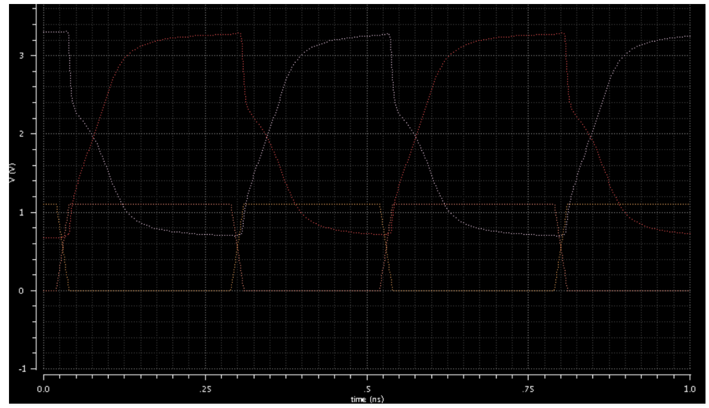


Fig. 10: Early simulation results of the levelshifter

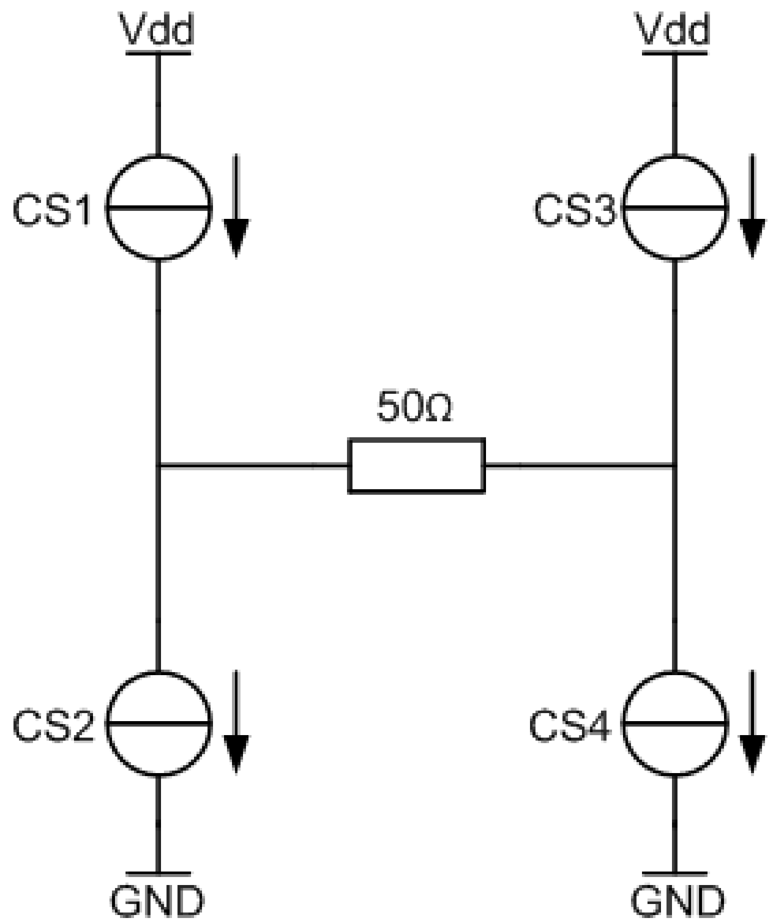
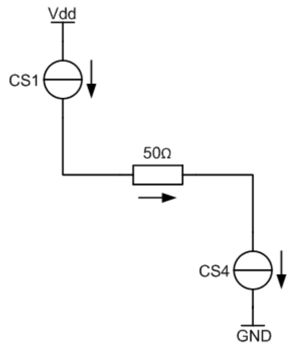


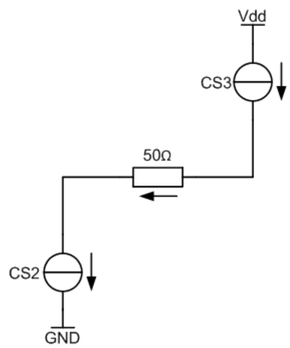
Fig. 11: The final stage of the power DAC: The current sources which will provide the differential output through the resistor.

Due to the local oscillator, the current will alternate between $V_{dd} \rightarrow CS1 \rightarrow CS4 \rightarrow GND$ (see Fig.**??**) and $V_{dd} \rightarrow CS3 \rightarrow CS2 \rightarrow GND$ (see Fig.**??**).

The first design parameters are the voltage supply and which switching devices are to be used. Because the DAC should be able to produce 50mA through a 50Ω resistor, the maximum voltage drop will be 2.5V. This already cancels out



(a) One current-steered cycle.



(b) The other current-steered cycle.

lower voltage supplies such as 1.2V and 2.5V. The resulting options are 3.3V and 5V. Because the stage consist of two current sources, the voltage headroom will be very limited in the 3.3V voltage supply. Therefor a 5V supply will be used as V_{dd}. This, along with the high switching speeds, limits the switching devices to the thick-oxide CMOS technology.

Because thick-oxide CMOS technology has been chosen, the width and length of the CMOS are the only parameters. The most straightforward design method subscribes that the CMOS should always be in saturation so that the current through the CMOS is independent of the drain-source voltage of the CMOS. Therefore Eq.**??** should be valid whatever the drain-source voltage.

$$V_{DS} > V_{TH} + V_{GS}$$

The drain-source voltage of the NMOS is minimal when the current through the resistor is maximal. This results in a minimum drain-source voltage of 1.25V. Because Eq.**??** should be valid independent of the output, the maximum gate-source provided by the level shifter should be 1.95V, because the threshold voltage of the thick-oxide CMOS is 0.7V. Along with Eq.**??**, this would provide the perfect current sources.

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$$

The main disadvantage of this straightforward approach is that this leads to significant speed restrictions. The small overdrive voltage, $V_{DS} - V_{TH}$, will require large width and thus large input capacitances. Due to the large input capacitance the level shifter will not be able to drive the gate-source voltage to the appropriate voltage level. So for the level shifter to work properly, the width of the NMOS should be increased. This will lead to a signal dependent error in the current. This can be seen from the FFT of the total system, the IMD3-level will increase due to this signal-dependence. So the trade-off will be to maximize the width of the NMOS, and therefor also the PMOS, while keeping the level-shifter in its desired working area.

Another aspect which has not been accounted for, is the channel-length modulation. As can be seen from Eq.**??**, the channel length modulation depend on both intrinsic parameters, λ, and extrinsic parameters, V_{DS}. The drain-source voltage is signal dependent. Each active stage of NMOS, will decrease the drain-source voltage. Because the intrinsic parameter λ is inverse proportional to the length of the NMOS, the length of the NMOS can be also be decreased so that the current delivered by the NMOS does not alter for different signals.

The next paper will contain information about the IMD3 - width trade-off and corresponding simulations. It will also contain viable designs.

IV. Results and Analysis

The specified specifications are verified by the use of simulations. While providing a one tone signal, a transient measurement of the output power is simulated. This to verify a correct functioning DAC, that translates the digitals signals as supposed. This holds that the 15 bit digital unary code is translated to an analogue signal with 16 level resolution.

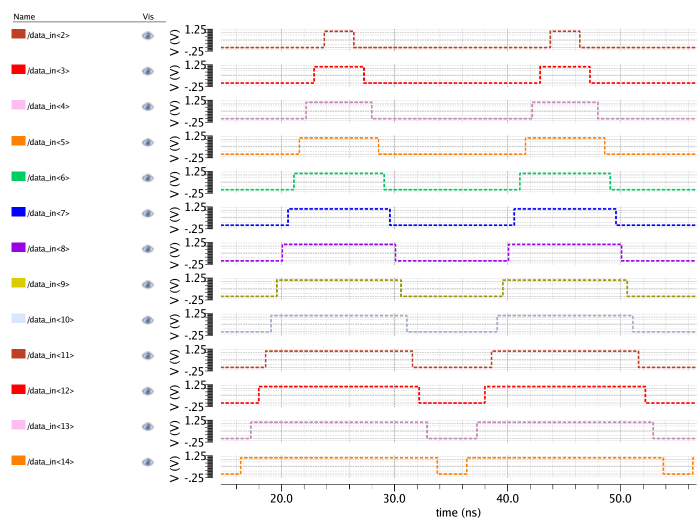


Fig. 13: Thermometer single tone voltage output.

Next a DFT of the output voltage is simulated to see the spectral content of the one tone model. This to find the power of the harmonic distortion and the spurious-free dynamic range (SFDR). The SFDR describes the power of the fundamental signal to the strongest spurious signal at the output, which is most commonly the second harmonic.

Furthermore a two tone test is simulated, the two tone test is useful test the linearity of the DAC. Non-linear behaviour generates intermodulation products at the output of the DAC. The power of these intermodulation products will examined, especially the third intermodulation product (IM3). Because the IM3 frequencies are very close to the fundamental frequency (at 2f2-f1 and 2f1-f2), it is almost impossible to filter

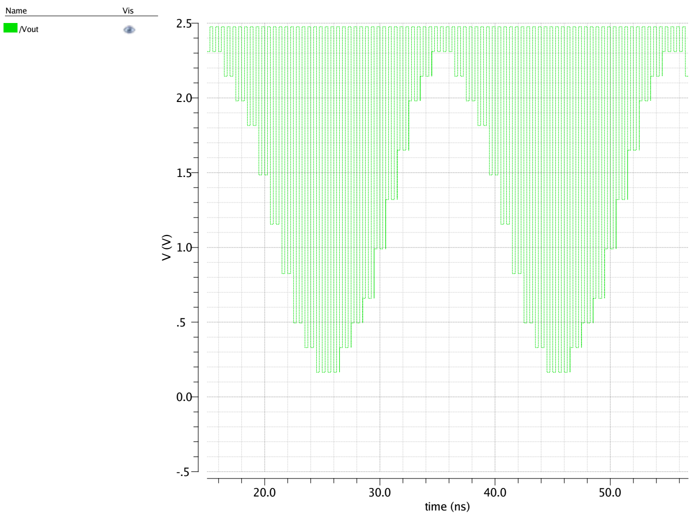


Fig. 14: SoC voltage output.

it out of the output signal; therefore, it is better to prevent creating them.

V. Conclusion

This is the conclusion

Acknowledgements

Dr. G. Radulov

References

[1] G. Radulov, "Course book 5tt50, tu/e," 2014.

[2] H. Li, B.Yin, J. Cao, Y. Zhang, and R. Wang, "Design of a 4-bit power dac achieving the output power of 16.59dbm with imd3<-31dbc up to 5ghz," 2014.

[3] K. J. Hass and D. F. Cox, "Level shifting interfaces for low voltage logic," in *9th NASA Symposium on VLSI Design*. Citeseer, 2000, pp. 3–1.

VI. Appendix

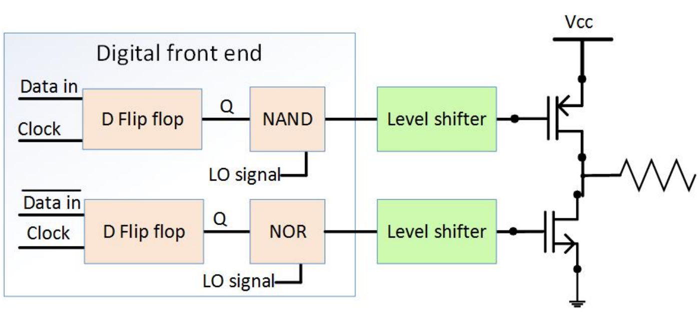


Fig. 15: Global schematic of the previous group.

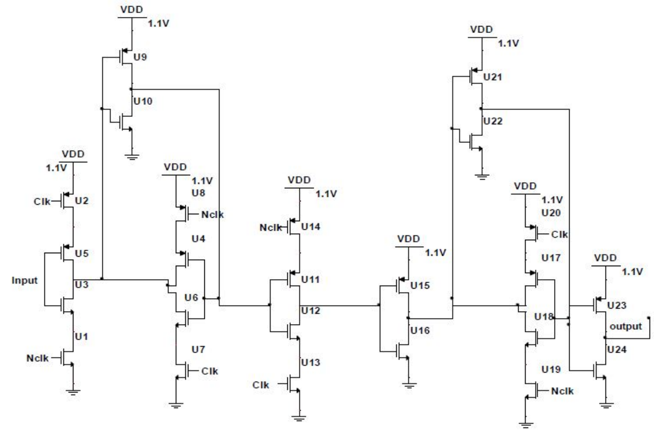


Fig. 16: D flip flop schematic from previous group

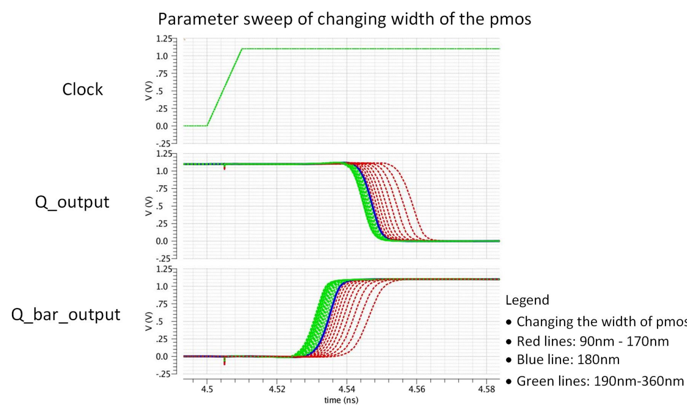


Fig. 17: Parametersweep of changing the width of the pmos when the data is low.

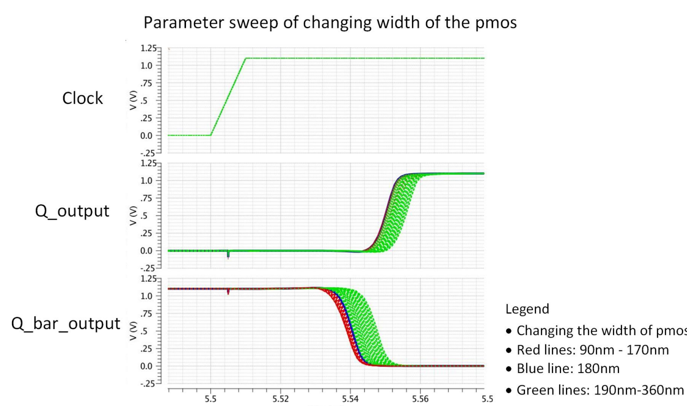


Fig. 18: Parametersweep of changing the width of the pmos when the data is high.

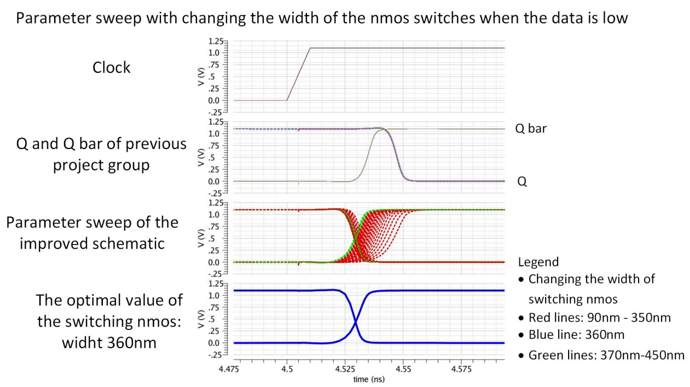


Fig. 19: Parameter sweep of changing the width of the switching nmos when the data is low.

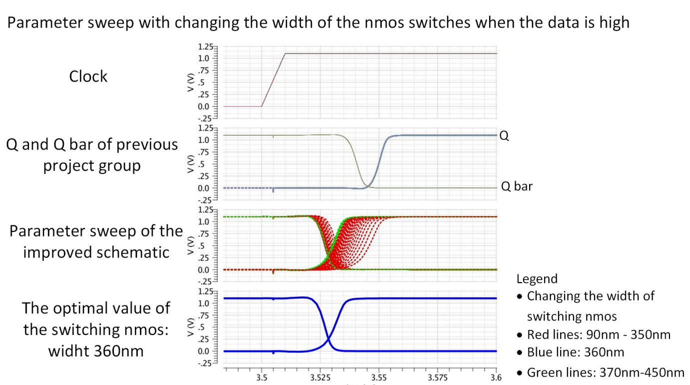


Fig. 20: Parameter sweep of changing the width of the switching nmos when the data is high