4-bit Power-Mixing-DAC delivering a peak power of 20 dBm with an IMD3 above 20 dBc

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***Abstract*—Modern integrated communication devices often require a power mixing Digital-to-Analog Converter (DAC), which is capable of producing a radio signal with enough power to be directly connected to an antenna. This paper presents a 4-bit Power-Mixing-DAC. The goals to mix a signal with a maximum bandwidth of 500 MHz with a 2 GHz carrier wave, and to deliver a full swing output current of 50 mA to a 50Ω load with an IMD3 > 20 dBc. First the system and its requirements will be discussed. This is followed by a breakdown of the system in components. Finally the results will be presented and analyzed.**

I. Introduction

In telecommunication applications there is the need to translate digital information to an analogue signal that can be send by an antenna. Nowadays many architectures exist that accomplish this, where most are derived from a more traditional architecture (see Fig. 1a). One of these architectures combines the DAC, mixer and power amplifier (PA) in a CMOS structure (Power-Mixing-DAC) Fig. 1b. Such a solution could be useful for several systems. Mainly for systems that require high speed, low power consumption or lack of sufficient available space for a PCB. One example for such a system is the Wi-Fi connection in a mobile phone.

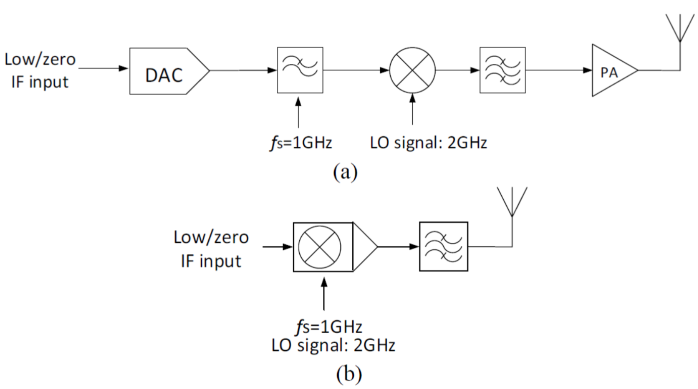

Fig. 1: A traditional transmitter stage (a) and the combined Power-Mixing-DAC (b). [1]

Because the Power-Mixing-DAC is fitted in a CMOS structure, it requires less space than a traditional system. This allows the system to be faster because there are less parasitic capacitances between the structures. Also the need to match to 50 ohm between these structures becomes superfluous, because all components can be tuned to each other. No particular standard has to be followed to combine components to those of other manufacturers therefore the system requires less components. Moreover the use of large capacitors or inductors is not possible, because these require too much space to create in silicon. Normally these are placed on the PCB.

This paper shows the design and analysis of a Power-Mixing-DAC in a 45 nm CMOS dummy technology, with as goal to mix a signal with maximum bandwidth of 500 MHz with a local oscillator (LO) with a frequency of 2 GHz and reach a 20.97 dBm output power and a IMD3 above 20 dBc. The design and analysis is divided in two steps. The first step is to create the Power-Mixing-DAC with ideal components, to determine the theoretical boundaries, this design is used as reference. The second step is to replace the ideal components with (non-ideal) transistors, where the parameters are designed to come as close as possible to the ideal-component design.

II. Hardware module

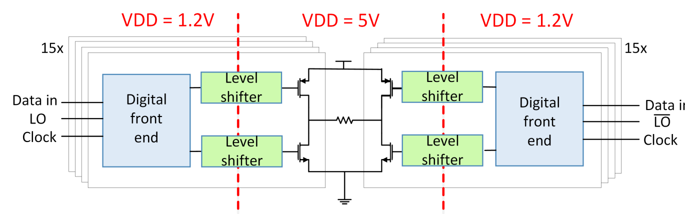

Fig. 2: The Power-Mixing-DAC is build out of 15 branches all connected to the resistor.

When looking inside Fig.1b, the architecture of the Power-Mixing-DAC becomes clear (see Fig. 2). It is composed out of several functional blocks: a digital front end structure, a level shifter and an amplifier.

The digital front end synchronizes the data and modulates it with a local oscillator, which operates as square wave at 2GHz. To synchronise the data, D flip-flops will be used. The D flip-flop has two outputs: Q and $\overline{Q}$. A NAND gate mixes Q and LO for the PMOS end stage and a NOR gate mixes $\overline{Q}$ and LO for the NMOS end stage. Before the mixed signals reach the final amplification stage, a level shifter translates the signals from a 1.2V V_{DD} which are used for the thin-oxide transistors in the digital front end to a 5V V_{DD} which is used in the final amplification stage. This amplifications stage provides the output power to the 50 Ω matched antenna.

The Power-Mixing-DAC translates a 15 bit unary coded digital signal with a maximum bandwidth of 500MHz to an analogue signal. Unary coded signals can provide higher linearity compared to binary coded signals. One of the reasons is that in the creation process of the transistors, it is more precise to make two transistors of the same size, than to make one with exactly two times the size. Due to the maximum resolution of 16 bits the signal to noise ratio (SNR) is limited to a theoretical maximum of 25.8 dB, see Eq. 1.

$$SNR = 6.02 \times n + 1.76 = 25.8dB \tag{1}$$

The specified output current is 50 mA, which means that the output power on the 50 Ω matched antenna should be 20.97 dBm. The aim is to get an IMD3 of at least 30 dBc.

III. System Components

A. Digital front end

The digital front end (DFE) consist of three parts, D flip-flop with a NAND gate and a NOR gate. This can been seen in Fig. 3. The D flip-flop synchronizes the incoming data and the NAND/NOR gates mixes the signal with the local oscillator in the digital domain. The DFE works in a high frequency domain and it needs to switch fast; therefore thin oxide transistors are used. The drawback of this kind of transistors is that they allow a low maximum Vds (max 1.2V), that limits the maximum output power. To solve this problem a level shifter is used to increase the power at the output stage. The level shifter is discussed in section III-B.

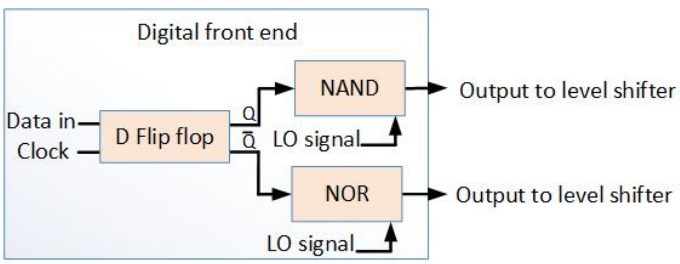

Fig. 3: One side of the diagram of the new digital front end.

1) D flip-flop: The two main technologies to create a flip flop are CMOS and CML. CMOS is relatively less complex in comparison to CML, therefore it covers less space. The main advantage for CML design is that the complex structure gives more degrees of freedom to tune the output. In this project the CMOS design is used, because it is less complex, single-ended and it can be realised in a short time period.There are a couple of challenges when designing a D flip-flop, for example the operation speed and the transition time of the output at the rising clock.

The CMOS D flip-flop shown on page 2 in [1] and page 17 in [2] is used as starting point in the project. The schematic of their circuit is shown in Appendix A, Fig. 18. The schematic of the new, improved, circuit consists of 32 transistors and is showed in Fig. 4. There are three changes made in comparison with the old schematic to improve the synchronization. The first change is that a second output has been added to flip-flop, to reduce the amount of the D flip-flops. The second change holds an additional NMOS transistor that is used as a switch and the last change is related to different transistor sizes, to reduce output delay.

To explain the principle of a master-slave D flip-flop, the schematic can be divided into four parts,the settle time of the data, master latch, two switches and slave latch. In the first part, the data will be set when the clock is low. The second part, the master will follow the signal of the first part when the clock is low and hold the data when the clock is high. In the third part, the switches will be closed when the clock is high and the slave latch, which is part four, sets the data. When the clock is low the NMOS transistor in part three is open en the slave latch holds the data.

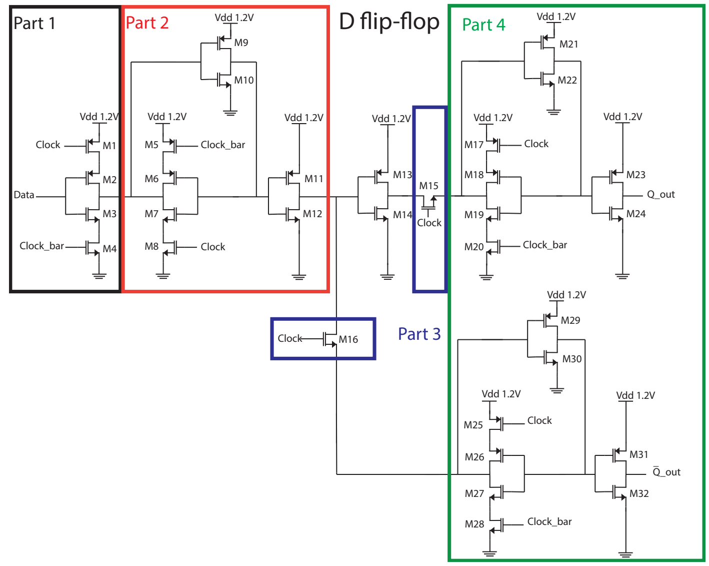

Fig. 4: The improved D flip-flop schematic.

The size of the PMOS and NMOS transistors in the master latch, slave latch and settling of the data are the same. The size of the NMOS transistor is set on 50nm x 90nm (length x width). The length of the PMOS transistor is the same, but the width of the PMOS transistor is determined with a parameter sweep to get the smallest delay of transition. In the parameter sweep the clock frequency is set to 1 GHz and the data frequency is set to 500 MHz. The results are shown in the Appendix A, Fig. 19 and 20. The optimal width of the PMOS transistor is 120nm, because it gives the smallest transition delay. The ratio of the widths of the PMOS and NMOS transistors is 1.33:1. (Wp:Wn)

The size of the switching NMOS transistors (part 3, transistor M16 and M15) are also determined with a parameter sweep with the same settings. The results are shown in Appendix A Fig. 21 and 22 in Appendix A. The optimal value of the width is 280nm. A comparison is made with the results of this value and the D flip-flop schematic of [1]. The result is shown in Fig. 5 and 6. The overall delay of the rise and fall time is reduced with 12ps to 13ps of Q and $\overline{Q}$, but at the cost of 2ps in the transition from low tow high of $\overline{Q}$.

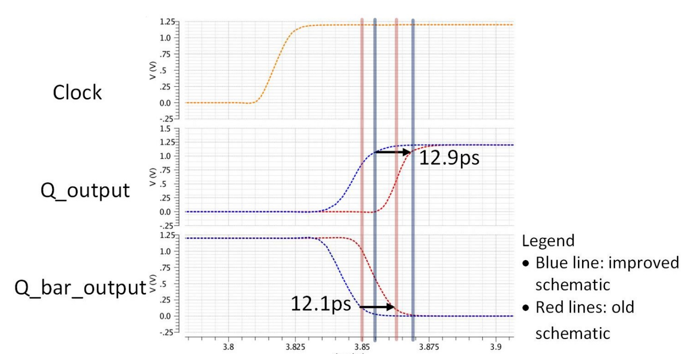

Fig. 5: Comparison of the transition delay before and after improvements when the data is high

With all the transistors sizes chosen, the critical point can

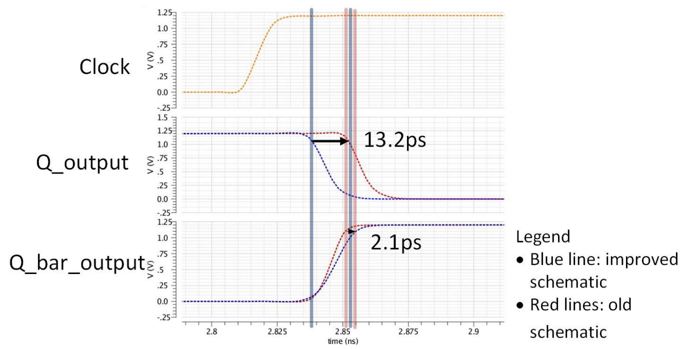

Fig. 6: Comparison of the transition delay before and after improvements when the data is low.

be measured to measure the minimum time that is needed to set the data before the clock is high. The minimal time that the data needs to be set is 40ps. The transition delay of Q and $\overline{Q}$ is 29ps when the data is high. When the data is low the delay of Q is 27ps and $\overline{Q}$ is 32ps. This is shown in Fig. 7.The final sizes of transistors in the D flip-flop are listed in Appendix A in Tables I.

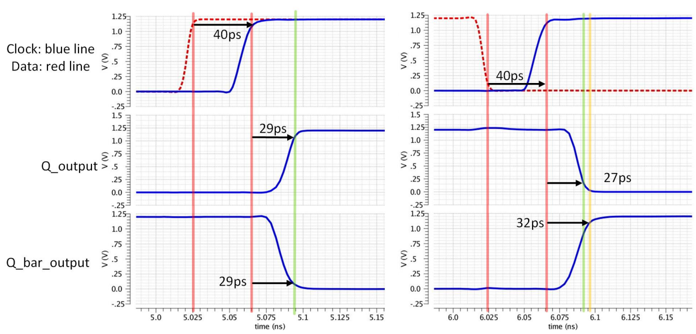

Fig. 7: Critical values of the settling time of the date and the delay of the transition of the output signal

2) NAND and NOR gates: The NAND and NOR gates mix LO signal with the data from the D flip-flop. This happens with an LO signal consisting of a 2GHz square wave.

The NAND gate has two PMOS transistors in parallel and 2 NMOS transistors in series. The schematic is shown in Appendix A, Fig. 23. In a normal CMOS inverter the width of the PMOS transistors is 2 to 3 times larger than the NMOS transistors, because the mobility of the NMOS transistor is larger than the PMOS transistor. The size of the PMOS transistor is 50nm x 180nm (length x width). In this situation two NMOS transistors are in series. The width of the NMOS has been determined with a parameter sweep and the length is set to 50nm. The result is shown in Appendix A, Fig. 24. The optimal value for the width is 180nm, because it has the same fall and rise times. The size of the NMOS transistor and PMOS transistor is 50nm x 180nm (length x width).

The NOR gate has two PMOS transistors in series and 2 NMOS transistors in parallel.The schematic is shown in Appendix A, Fig. 25. The size of the NMOS transistor is set on the smallest size of a NMOS transistor: 50nm x 90nm (length x width). The width of the PMOS transistor is determined with a parameter sweep and the length is set to 50nm. The result is shown in Appendix, Fig. 26. The optimal value for the width is 280nm is, because it has the same fall and rise time. The size of the PMOS transistor is 50nm x 280nm (length x width).

In the simulation of the total system the load of the level shifter has increased. The NAND gates and NOR gates could not provide the required current to drive the levels shifter, therefore a CMOS buffer is placed behind the NAND and NOR gate. The width of the PMOS transistor is set to 900nm and the NMOS transistor is set to 500nm. The length of both transistors is set to 50nm. The results of the buffer is shown Appendix A, Fig. 27.

B. *Levelshifters*

To generate sufficient output power thick-oxide transistors are used at the output stage. They can generate larger currents compared to thin oxide transistors and support a larger supply voltage. Thick-oxide transistors have the problem that their threshold voltage is too large to drive them with thin-oxide transistors. Also, the desired gate voltages for the thick-oxide PMOS transistors is entirely out of the DFE's output voltage range. Increasing the supply voltage of the thin-oxide transistors is not possible, since any supply voltage above 1.2V breaks them. Therefore a levelshifter is designed to drive the thick-oxide transistors. In this design special care is taken to ensure that the voltages across any thin-oxide transistor do not exceed 1.2V, so they do not break. On the output side the levelshifter has to be able to drive very large transistors. The driven NMOS transistors has to be supplied with a voltage of 0V(off) to 2V(on) and the driven PMOS transistors with a voltage of 5V(off) to 3V(on).

In [1] a design for the levelshifter was proposed, but they were not able to integrate it with the rest of their design. Some other designs that were looked at are proposed in [3] and [4]. In this paper the design from [1] is chosen, because the others did not look as promising and are intended for different scenarios compared to the situation in this paper. Designing the levelshifter caused some major problems. First the cadence models originally used have have an unrealistically high threshold voltage of 1.5V, this makes it difficult to drive them with the thin oxide transistors. In order to create a functioning simulation this was changed to a more realistic threshold voltage of 0.7V. This gives a larger V_{ON}, making the transistors conduct more current for a smaller size. This is necessary, because the transistors being driven by the levelshifter are very large. Therefore a large driving current must be supplied by the levelshifter.

The levelshifter design started with the design of the PMOS driver, which should have an output voltage of 3(off) to 5V(on). As a starting point the design from [1] was used, it is shown on the right in Fig. 8. In this design the thick oxide transistors M3 and M4 serve to protect the thin oxide transistors M5 and M6 from too high voltages. M1 and M2 form a current sensing circuit that charge the output node and each other's gates when switching. Their most important parameter is their width, the larger they are the quicker they charge the output. But a larger M1 and M2 also means that the M3-6 need to be larger to discharges the nodes. Since M2 must drive both M1 and the load it must be bigger than M1. The next most important parameters are the lengths of M3 and M4 and widths of M5 and M6. Together they determine the speed at which the output nodes are discharged and the voltage level of the output nodes when M3 and M5 or M4 and M6 are active. The circuit operates as follows. Assume initially VIN is high and $\overline{\text{VIN}}$ is low. Node $\overline{\text{VOUT}}$ will be pulled low by the left branch and the right branch will not conduct any current. Then $\overline{\text{VOUT}}$ is pulled towards 3V and M2 will start conducting and charging node VOUT towards 5V. This will make M1 stop conducting current, causing $\overline{\text{VOUT}}$ to be pulled even closer to 3V. In this way M2 and M1 drive each other's gate and amplify each other, enabling fast switching. When everything is settled VOUT should be near 5V and $\overline{\text{VOUT}}$ near 3V. When the input switches (VIN goes low and $\overline{\text{VIN}}$ goes high) the process is reversed. Node VOUT will be pulled towards 3V and no current will be conducted by the left branch, enabling $\overline{\text{VOUT}}$ to be driven towards 5V. Again, M1 and M2 will amplify this process and switch VOUT from 5V to 3V and vice versa for $\overline{\text{VOUT}}$.

To drive the NMOS transistors of the DAC's output current sources an extra stage is added to the levelshifter. Because the threshold voltage is lowered to 0.7V the VIN signal can drive M8 to pull the output to 0V when VIN is high. However this is not ideal since VIN does not create a large V_{ON}. VOUT is high then, so M7 will not conduct current. When VIN is low, VOUT is near 3V and M7 will conduct current, pulling VOUT_NMOS to 2V. For the NMOS driver important parameters were the length of M7, which largely determines the maximum voltage of the output, and the widths of both M7 and M8, which mostly detemine the speed at which it can switch the load. For both the PMOS and NMOS drivers VBIAS determines the maximum $V_{DS_{5,6}}$ and is set to make sure $V_{DS_{5,6}}$ has a maximum value of 1.2V.

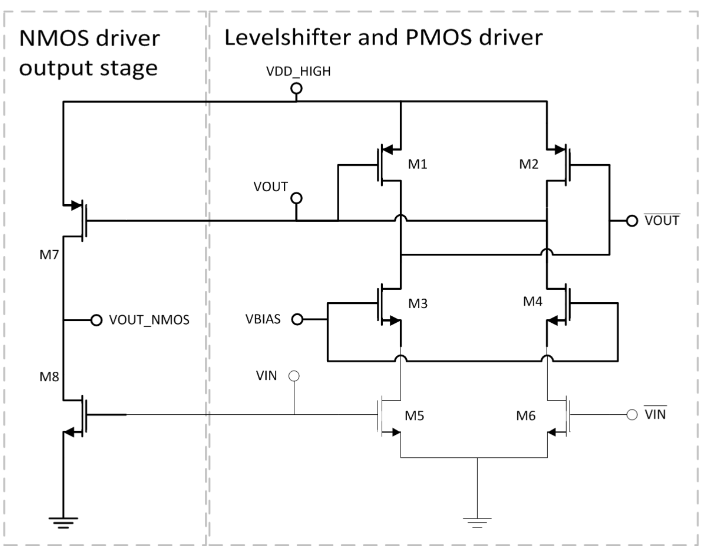

Fig. 8: Schematics of the levelshifter, thick wires indicate a high voltage regime and thin lines the low voltage transistors. On the right the up-shifting PMOS driver is shown. Its output VOUT can drive a PMOS transistor. The NMOS driver's layout is the same with an extra stage added on the left side. The node VOUT_NMOS can drive a NMOS transistor.

The final sizes of transistors in the PMOS and NMOS driving levelshifters are listed in Appendix A in Tables II and III respectively. How these sizes have been determines is discussed next. Both M1 and M2 should have a V_{DS} as low as possible, so their length is set to the minimum of 200n. Their widths determines how fast they can charge the load and each other and were determined using a sweep over both the widths and choosing the best result. Other important parameters are the lengths of M3 and M4, widths of M5 and M6 and V_{BIAS}. These have been determined by sweeping over all three parameters and choosing the best options. The result of this simulation is shown in Fig. 9. The configuration with the steepest edges that comes closest to 3V, to keep the load PMOS in saturation, has been chosen. Finally the other parameters are finetuned.

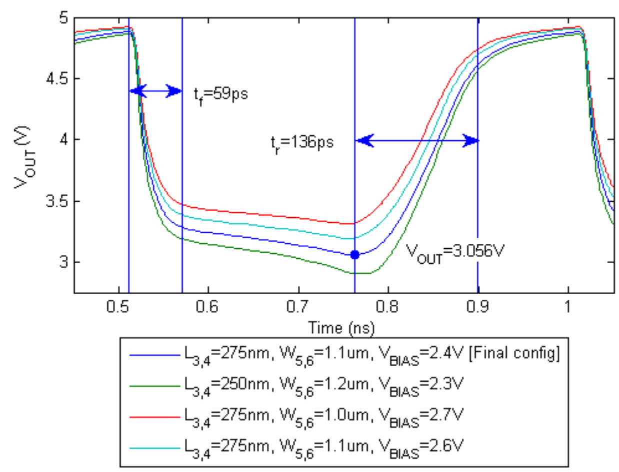

Fig. 9: Parameter sweep over the of the lengths of M3 and 4, widths of M5 and 6 and V_{BIAS}. For clarity only a selection and the chosen configuration are shown. The load is a thick oxide PMOS transistor of 200nm by 60μm.

To determine the sizes of the transistors of the NMOS driver the PMOS driver is used a starting point. This works since the original circuit still only drives one PMOS transistor. So initial tuning of M7 and M8 will have little effect on the behaviour of the original circuit. The maximum output voltage level is determined mostly by the dimensions of M7. The dimensions of M8 determine how fast the output voltage drops. Because the off voltage must be as close to 0V as possible, the length of M8 is set to the minimum of 200nm. Its width and the dimensions of M7 are chosen using a combined sweep. A selection of some resulting characteristic curves are shown in Fig. 10. The output voltage is mostly determined by L_7. The ratio between W_7 and W_8 largely determines the output characteristic. The chosen parameters are $L_7 = 1.4\mu m, W_7 = 20\mu m$ and $W_8 = 25\mu m$.

C. Current Sources

The final stage of the Power-Mixing–DAC are the current sources. They provide a differential output over a 50Ω resistor. This setup is shown in Fig.11.

Due to the local oscillator, the current alternates between the path through CS1 and CS4 (see the red route in Fig. 11) and the the path through C3 and C2. (see the blue route in Fig. 11).

The first design parameters are the supply volage and the switching devices. Because the DAC should be able to produce 50mA through a 50Ω resistor, the maximum voltage

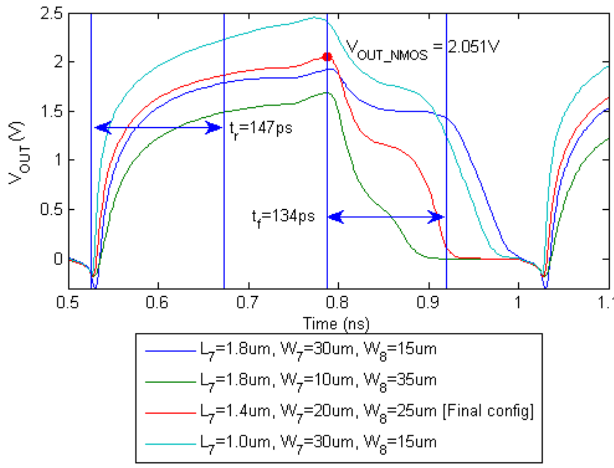

Fig. 10: Parameter sweep over the of the length of M7 and widths of M7 and 8. For clarity only a selection with characteristic curves and the chosen configuration are shown. The load is a thick oxide NMOS transistor of 300nm by 12μm.

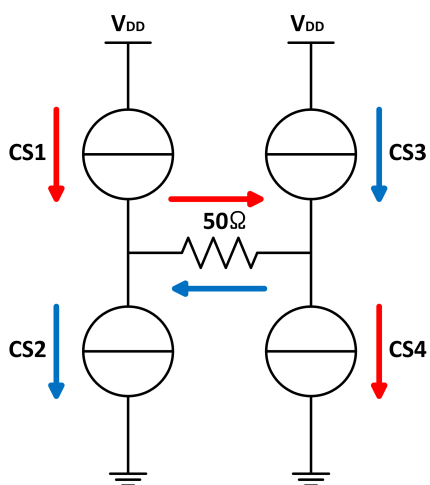

Fig. 11: The final stage of the Power-Mixing–DAC: The current sources which will provide the differential output through the resistor.

drop will be 2.5V. This already cancels out lower voltage supplies such as 1.2V and 2.5V. The resulting options are 3.3V and 5V. Because the stage consist of two current sources, the voltage headroom will be very limited in the 3.3V voltage supply. Therefore a 5V supply will be used as V_{DD}. This, along with the high switching speeds, limits the switching devices to the thick-oxide CMOS technology.

Due to the Power-Mixing- DAC design, the width and length of the CMOS are the only parameters. The most straightforward design method subscribes that the CMOS should always be in saturation so that the current through the CMOS is nearly independent, without channel-length modulation taken into account, of the drain-source voltage of the CMOS. This is directly related to the output impedance of the switched current source. Therefore Eq. 2 should be valid whatever the drain-source voltage.

$$V_{DS} > V_{ON} = V_{GS} - V_{TH} \tag{2}$$

The drain-source voltage of both the NMOS and PMOS are minimal when the current through the resistor is maximal. In case of the NMOS this results in a minimum drain-source voltage of 1.25V. Because Eq. 2 should be valid independent of the output, the maximum gate-source provided by the level shifter should be 1.95V, because the threshold voltage of the thick-oxide CMOS is 0.7V. Along with Eq. 3, this provides a viable current sink.

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \tag{3}$$

So by designing a current sink which operates at a V_{GS} of 1.95V, the switching current sink will always be either in saturation or off. This provides a high output impedance and thus a high IMD3. Another advantage is the increase in efficiency.

For the PMOS the same design equations hold and thus they require a V_{SG} of 1.95V to remain in saturation mode. So for the current source to provide current, the gate voltage should be witched between 3.05V (sourcing mode) and 5V (off mode).

The thick-oxide technology however, limits other parameters. The length of the thick-oxide CMOS transistor has as minimum of 200nm when the maximum available voltage headroom is 2.5V. In this configuration however, the maximum available voltage headroom needs to be minimal 2.5V. This limits the length of the transistor to a minimum of 300nm. Although a longer transistor has some advantages, such as a decrease in mismatch, it also mean a wider transistor to conduct the required current. A larger width however, results in higher input capacitance. To decrease the load on the level shifter, the length of both the PMOS ans the NMOS has been chosen to be optimized within the thick-oxide technology, i.e. 300nm.

The primary focus on each transistor is to make sure that it is able to handle the needed amount of current. As has been mentioned before, due to the channel-length modulation, M1 must be able to handle more current when the load is conducting 50mA as M15. Therefore every transistor has to be redesigned. The first transistor has been designed with the circuit found in Fig.28. With this circuit a parametric sweep will be conducted to find the minimum width, to decrease the input capacitance of the transistor, to be able to conduct the required amount of current. This parametric sweep can be found in Fig. 12.

So the width of the first NMOS should be 10.96μm to guarantee that it will sink 3.3mA when the V_{GS} is 1.95V.

For the second transistor, a similar approach has been taken. Because the drain-source current will decrease, the current through M1 will increase. Therefore the second transistor is placed in parallel with M1, as it will be in the final design, and the width of the second transistor will be swept so that

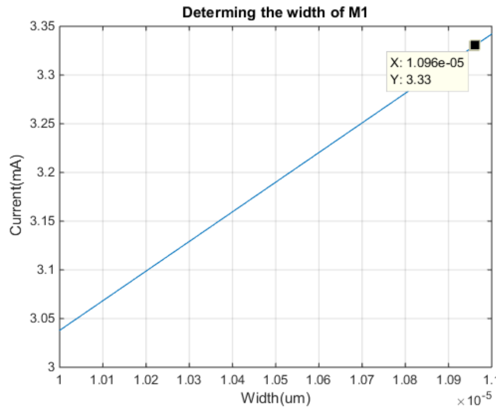

Fig. 12: The current through the transistor versus its width. To make sure that the current through the transistor is 3.3mA, the width should be 10.96μm.

the transistors together will conduct 6.66mA. This technique will be repeated for each transistor. The list of all width and lengths of all NMOS thick-oxide transistors can be found in the appendix, table IV.

The same technique has been used for the PMOS transistors. Due to the dummy technology, which was not able to simulate width over 100μm, each bit will be represented by two PMOS in parallel so that the width is maintained within the 100μm. This list can also be found in the appendix, table V.

When all of these transistors are designed in a single set-up, that is a setup as seen in Fig. 11, a sweep can be made through all bits. The results can be found in Fig. 13. However, due to the switching and imperfections in both the NMOS and the PMOS, a error is present in the current. This error is signal dependent, as can be seen in Fig.14.

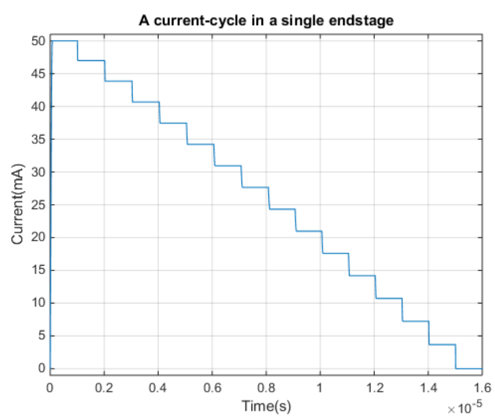

Fig. 13: A sweep through all possible currents, with a maximum of 50mA and a minimum of 0mA.

IV. Results and Analysis

The specifications are verified by comparing simulations results with the expectations. The goal is to verify a correct

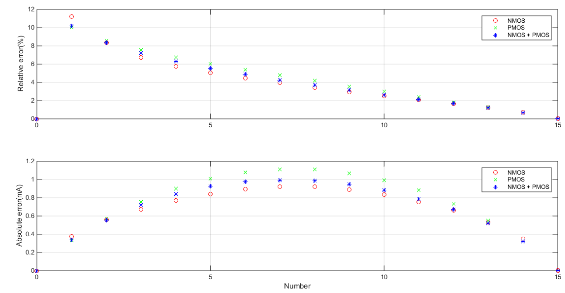

Fig. 14: The absolute and the relative current error in the endstage versus the input number of the DAC.

functioning system, however due to unexpected simulation errors this is not possible. The thick-oxide transistor models in the level shifter cause a simulation crash, therefore the rest of the system is tested with ideal level shifters.

While providing a one tone signal, a transient response of the output power is simulated see Fig. 29.

Next, a DFT of the output voltage is simulated to see the spectral content of the one tone model. To simulate such a DFT the simulation duration should be chosen wisely, an integer number multiple of the period time, otherwise a single tone will not be shown as a single frequency in the spectrum. The simulation time is 256ns (512 LO periods) and the first 15 periods are neglected to filter out settling issues. To fit exactly 11 data periods in this timespan the data frequency should be 42.97 MHz. In Fig. 15 shows the 2 GHz carrier frequency and the third and fifth harmonic.

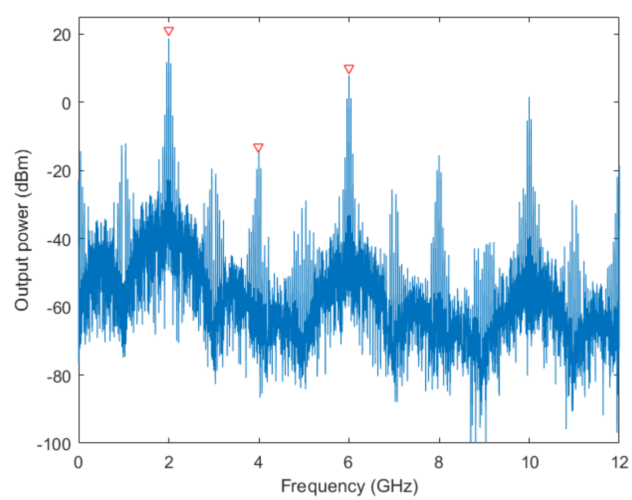

Fig. 15: The output power spectrum of a single tone test at 42.97MHz.

Furthermore, a two-tone test is simulated. The period time of the second tone fits 14 times in the simulation time, which means that the data frequency of the second tone is equal to 54.69 MHz see Fig. 30. A two-tone test is useful test the linearity of the DAC, non-linear behaviour generates intermodulation products at the output of the DAC. The power of these intermodulation products should be low, because they interfere with the modulated data tones. Especially the third intermodulation product (IM3), because the IM3 frequencies are very close to the fundamental frequency (at $2f_2 - f_1$ and $2f_1 - f_2$). It is almost impossible to filter the IM3 noise out of the output signal, therefore it is better to prevent creating IM3 noise. There are more options to express the amount of IM products. For example the spurious-free dynamic range (SFDR) describes power of the fundamental signal to the strongest spurious signal at the output, which is in this case the IM3. Whereas IMD3 describes the difference of the fundamental signal and the IM3.

The spectral constant visualised in Fig. 16 shows the 2 GHz carrier frequency and the modulated signals around it. Also the IMD3 is visualised, for these two input signals an IMD3 of 22.59 dBc is measured.

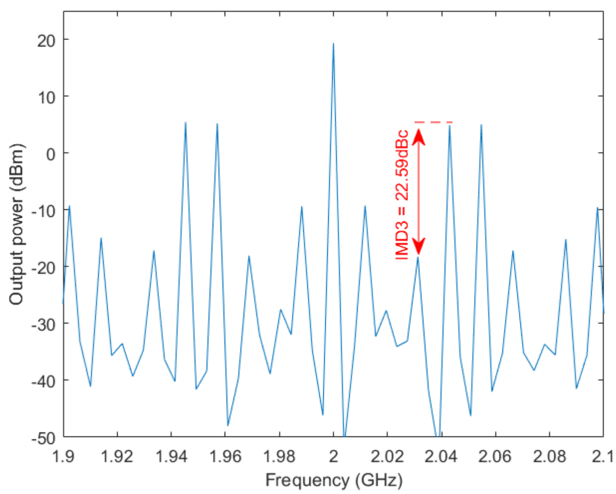

Fig. 16: The output power spectrum of a two-tone test (42.97MHz and 54.69MHz) shows an IMD3 of 22.59 dBc.

V. Conclusion

So the main goal of the research was the design and analysis of a power-mixing DAC which works on a LO frequency of 2GHz, a data-bandwidth of 500MHz while providing 20.97dBm output power and a IMD3 higher than 30dBc. This was achieved by designing a D-flip-flop for synchronization, a NAND and a NOR port for mixing the data with the LO, a levelshifter which was able to drive the large and high voltage current sinks/sources and the current sinks and sources to provide a current through a matched 50Ohm antenna. As a result the power-mixing DAC was able to reach a data-bandwidth of 500MHz while providing an peak output power of 20 dBm. This all has lead to an IMD3 of at least 20 dBc. So this Power-Mixing-DAC is able to be used in the wifi-antenna in mobile phones.

References

[1] H. Li, B.Yin, J. Cao, Y. Zhang, and R. Wang, "Design of a 4-bit power dac achieving the output power of 16.59dbm with imd3<-31dbc up to 5ghz," 2014.

[2] G. Radulov, "Course book 5tt50, tu/e," 2014.

[3] K.-H. Koo, J.-H. Seo, M.-L. Ko, and J.-W. Kim, "A new level-up shifter for high speed and wide range interface in ultra deep sub-micron," in *Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on*. IEEE, 2005, pp. 1063–1065.

[4] K. J. Hass and D. F. Cox, "Level shifting interfaces for low voltage logic," in *9th NASA Symposium on VLSI Design*. Citeseer, 2000, pp. 3–1.

Appendix A

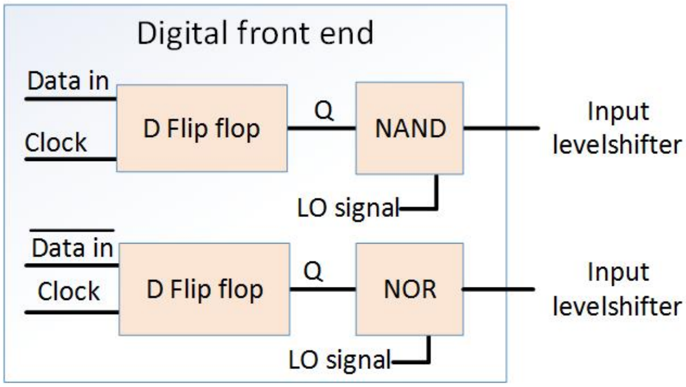

Fig. 17: Global schematic of the previous group. [1].

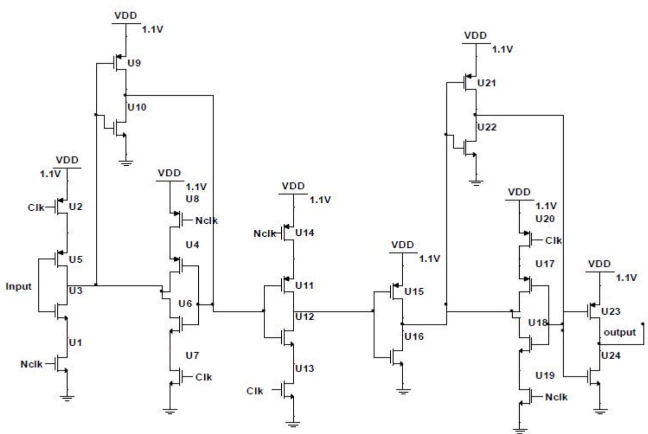

Fig. 18: D flip-flop schematic from previous group [1].

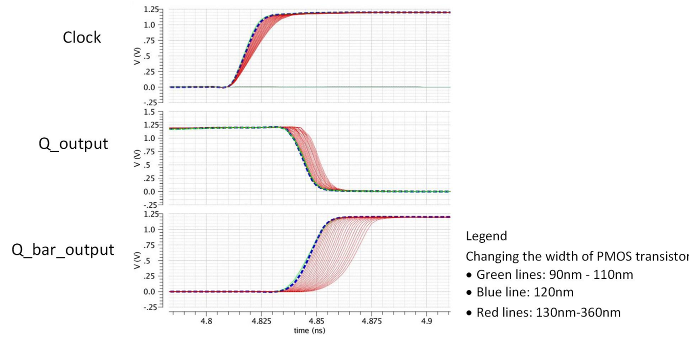

Fig. 19: A Parameter sweep of changing the width of the PMOS transistor when the data is low. The PMOS transistors of part 1,2 and 4 of 4 are part of the parameter sweep. The frequency of the clock is set to 1 GHz and the frequency of the data is set to 500MHz.

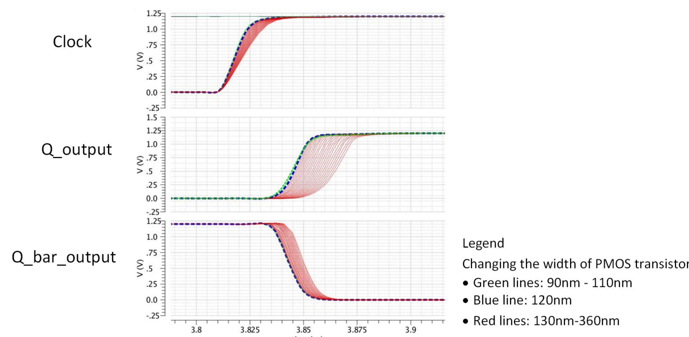

Fig. 20: A Parameter sweep of changing the width of the PMOS transistor when the data is high. The PMOS transistors of part 1,2 and 4 of 4 are part of the parameter sweep. The frequency of the clock is set to 1 GHz and the frequency of the data is set to 500MHz.

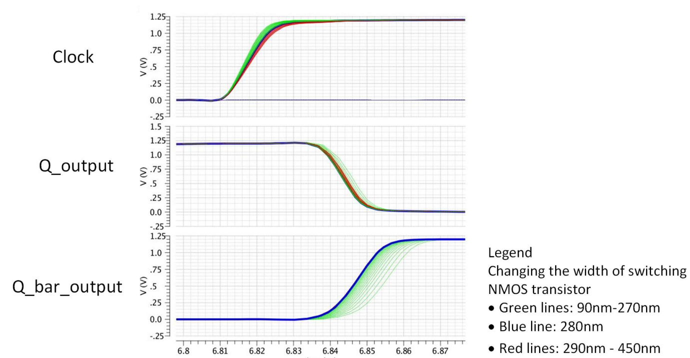

Fig. 21: Parameter sweep of changing the width of the NMOS transitor of part 3 in Fig.4 when the data is low.

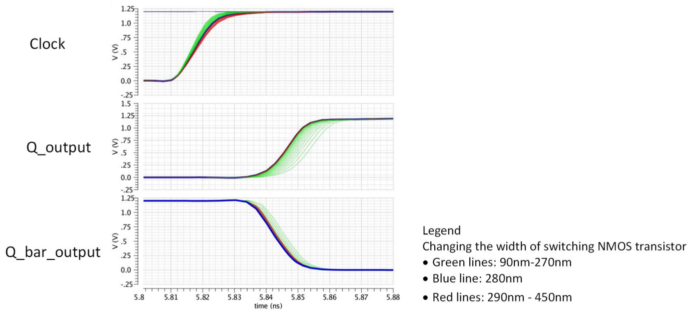

Fig. 22: Parameter sweep of changing the width of the NMOS transitor of part 3 in Fig.4 when the data is high.

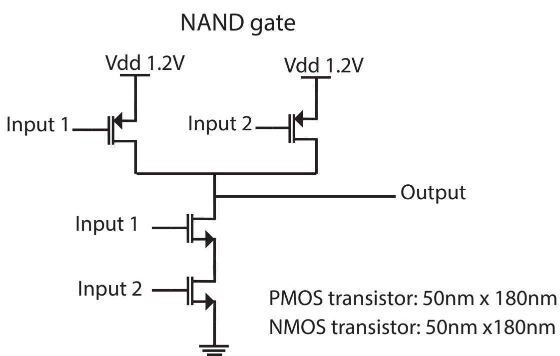

Fig. 23: The schematic of the NAND gate.

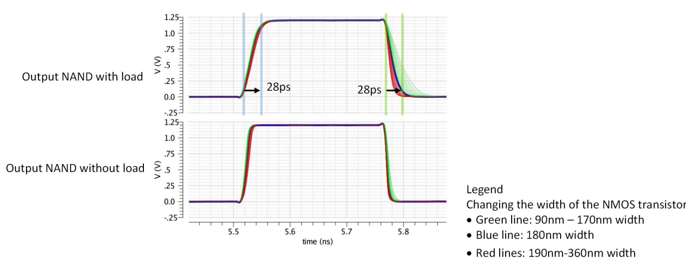

Fig. 24: Parameter sweep of changing the width NMOS transistor of the NAND gate.

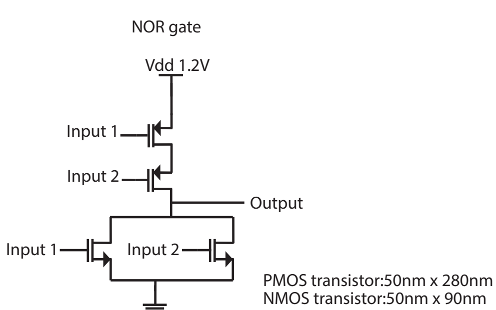

Fig. 25: The schematic of the NOR gate.

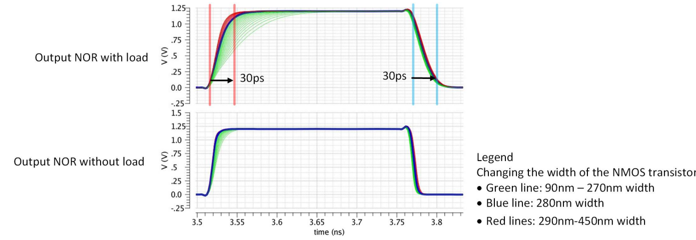

Fig. 26: Parameter sweep of changing the width NMOS transistor of the NOR gate.

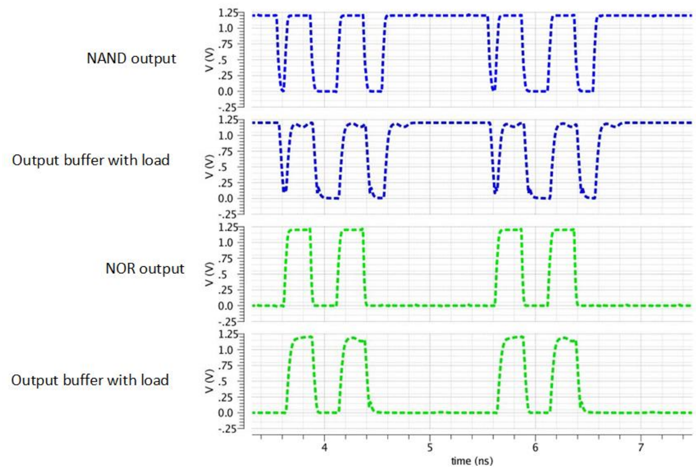

Fig. 27: Results of the output of the NAND and NOR with a buffer.

TABLE I: This table lists the dimensions of the transistors of the D flip-flops.

Transistor	Width(nm)	Length (nm)
M1	120	50
M2	120	50
M3	90	50
M4	90	50
M5	120	50
M6	120	50
M7	90	50
M8	90	50
M9	120	50
M10	90	50
M11	120	50
M12	90	50
M13	120	50
M14	90	50
M15	280	50
M16	280	50
M17	120	50
M18	120	50
M19	90	50
M20	90	50
M21	120	50
M22	90	50
M23	120	50
M24	90	50
M25	120	50
M26	120	50
M27	90	50
M28	90	50
M29	120	50
M30	90	50
M31	120	50
M32	90	50

TABLE II: This table lists the dimensions of the transistors in the levelshifter that drives the PMOS current sources.

Transistor	Width(um)	Length (nm)
M1	10	200
M2	50	200
M3	10	275
M4	10	275
M5	1.1	50
M6	1.1	50

TABLE III: This table lists the dimensions of the transistors in the levelshifter that drives the NMOS current sources.

Transistor	Width(um)	Length (nm)
M1	10	200
M2	50	200
M3	10	275
M4	10	275
M5	1.1	50
M6	1.1	50
M7	20	1400
M8	25	200

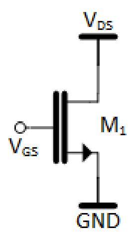

Fig. 28: The circuit used to determine the required width of the transistor to sink 3.3mA. V_{DS} is 2.4167V and V_{GS} is 1.95V.

TABLE IV: This table describes which widths and lengths are used for which NMOS transistors. M1 is the MOSFET which is associated with the lowest current while M15 is associated with the highest current.

NMOS	Width(um)	Length (um)
M1	10.97	0.3
M2	11.47	0.3
M3	11.60	0.3
M4	11.53	0.3
M5	11.52	0.3
M6	11.63	0.3
M7	11.67	0.3
M8	11.71	0.3
M9	11.76	0.3
M10	11.83	0.3
M11	11.88	0.3
M12	11.96	0.3
M13	12.03	0.3
M14	12.11	0.3
M15	12.20	0.3

TABLE V: This table describes which widths and lengths are used for which PMOS transistors. M1 is the MOSFET which is associated with the lowest current while M15 is associated with the highest current.

PMOS	Width(um)	Length (um)
M1	56.23	0.3
M2	57.25	0.3
M3	57.63	0.3
M4	57.84	0.3
M5	58.04	0.3
M6	58.28	0.3
M7	58.56	0.3
M8	58.87	0.3
M9	59.21	0.3
M10	59.57	0.3
M11	59.95	0.3
M12	60.36	0.3
M13	60.82	0.3
M14	61.31	0.3
M15	61.87	0.3

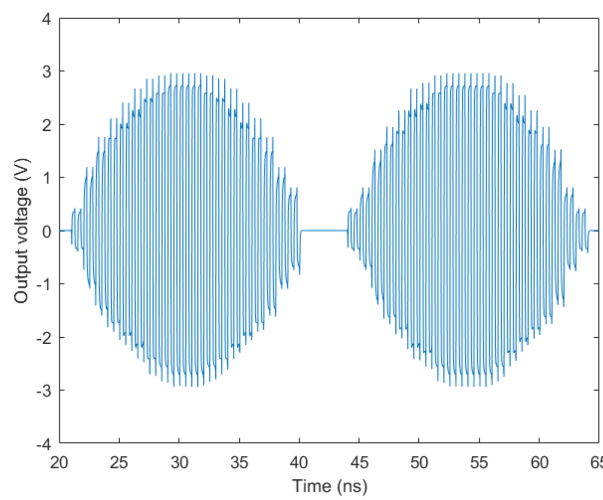

Fig. 29: 42.97MHz single tone output voltage

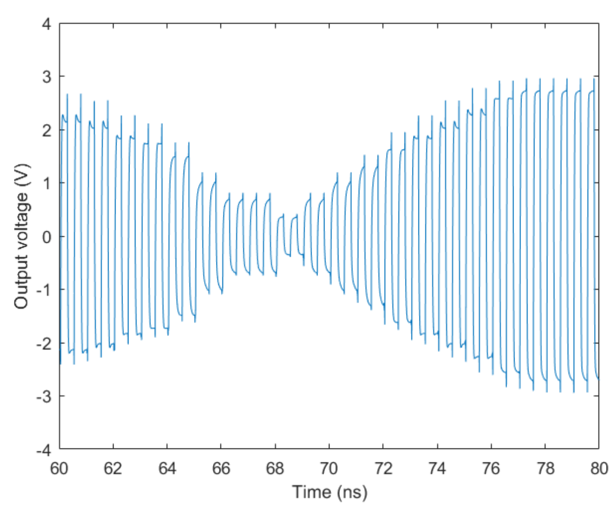

Fig. 30: 42.97MHz and 54.69MHz two tone output voltage