Power Mixing DAC

P. van Anrooij, R. Bonten, M. Hattink, F. Smits
Eindhoven University of Technology, Eindhoven, The Netherlands

***Abstract*—This is the abstract**

I. Introduction

This is the introduction

II. Hardware module

For this design there is chosen to create a system on chip (SoC) of a traditional DAC, mixer and power amplifier (PA), because this leads to several advantages. One thing is that it results in a more compact solution. A compact solution allows the system to be faster, because there are less parasitic capacitances between the structures. Also the need of matching to 50 ohm between these structures becomes superfluous. Using a SoC solution has a disadvantage that it is hard to generate high power, this generates heat which can damage the SoC. Moreover the use of large capacitors or inductors is not possible.

III. System Components

A. Digital front end

The digital front end consist of two parts, D flip flop and NAND/NOR gate. The D flip flop will synchronise the incoming date and the NAND/NOR gate will modulate the signal with the local oscillator.This signal will go to the level shifter. The two parts will be described in this paragraph.

1) D flip flop: A D flip flop will be used to synchronise the incoming thermometer coded data and to ensure that the output pmos and nmos switch at the same time. There are a couple of challenges that are important to take into account when designing a D flip flop, for example the operation speed and the transition time of the output at the rising clock.

A flip flop can be made in different ways. The two main technologies are in CMOS and CML. The CMOS design is relative less complex in compare to CML, but in CML there are more parameters that can be modified to tune the output. In this project the CMOS design is used, because it is less complexity, single-ended and it can be realised in a short time period. The CMOS circuit of previous group is used in this project, [1] - [2], but the size of the pmos is changed to get a better performance. The schematic is shown in Fig. 1. The D flip flop works with a master-slave principal. The master will set the data on the rising clock and it keeps it until the clock is low. The slave will copy the data of the master and hold the data when the clock is low.

To explain this principal in the schematic, the diagram can be divided into three parts, settle time of the data, master latch and slave latch. In the first part the data will be set when the clock is low. The second part, the master latch will set the settled data and when the clock is high it will set the data to the output of the master latch and the first part will be turned off. The third part, the slave latch will follow the master latch when the clock is high, but when the clock is low the master latch output will be turned off and slave latch will be holding the data.

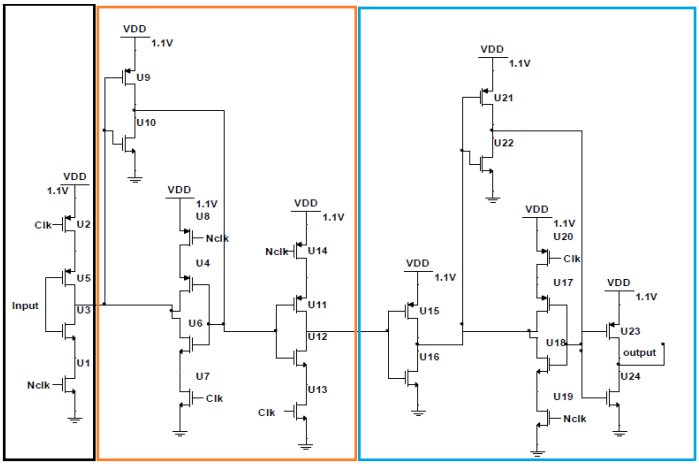

Fig. 1. D flip flop schematic, this schematic will be updated in the next version to define the parts better.

The size of all of the nmos are 50nx90n(length x width). The width of the pmos is determined with the simulation to get smallest delay between the rising clock and the output. The pmos have the following dimensions: 50nx180nm (length x width). The bulk of the pmos is connected to the power supply (1.1V) and the bulk of the nmos is connected to the ground.

The rise time, fall time, critical point graph will be shown in the next version.

2) NAND/NOR gate: The NAND and NOR will modulate the local oscillator signal (LO) with the data from the D flip flop. The LO signal works with a 2Ghz square wave.

The design of the NAND and NOR will be in the next version of the paper.

B. Mixers

These are the mixers

C. Levelshifter

This is the levelshifter

D. Current Sources

These are the currentsources

IV. Results and Analysis

The specified specifications are verified by the use of simulations. While providing a one tone signal, a transient measurement of the output power is simulated. This to verify

a correct functioning DAC, that translates the digitals signals as supposed. This holds that the 15 bit digital unary code is translated to an analogue signal with 16 level resolution.

Next a DFT of the output voltage is simulated to see the spectral content of the one tone model. This to find the power of the harmonic distortion and the spurious-free dynamic range (SFDR). The SFDR describes the power of the fundamental signal to the strongest spurious signal at the output, which is most commonly the second harmonic.

Furthermore a two tone test is simulated, the two tone test is useful test the linearity of the DAC. Non-linear behaviour generates intermodulation products at the output of the DAC. The power of these intermodulation products will examined, especially the third intermodulation product (IM3). Because the IM3 frequencies are very close to the fundamental frequency (at 2f2-f1 and 2f1-f2), it is almost impossible to filter it out of the output signal; therefore, it is better to prevent creating them.

V. Conclusion

This is the conclusion

Acknowlegdements

Dr. G. Radulov

References

[1] G. Radulov, "Course book 5tt50, tu/e," 2014.

[2] H. Li, B.Yin, J. Cao, Y. Zhang, and R. Wang, "Design of a 4-bit power dac achieving the output power of 16.59dbm with imd3<-31dbc up to 5ghz," 2014.