Power Mixing DAC

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***Abstract*—Modern integrated communication devices often require a power mixing Digital-to-Analog Converter (DAC), which is capable of producing a radio signal with enough power to be directly connected to an antenna. This paper presents a 4 bit power mixing DAC. The goals were to be able to mix a signal with a maximum bandwidth of 500 MHz with a 2 GHz carrier wave and deliver a full swing output current of 50 mA to a 50Ω load with an IMD3 > 30 dBc. First the system and its requirements will be discussed. This is followed by a breakdown of the system components. Finally the results will be presented and analyzed.**

I. Introduction

In telecommunication applications there is the need to translate digital stored information to an analogue signal that can be send by an antenna. Now a days there are many architectures to accomplish this, where most are distracted from a more traditional architecture. Fig. 1a. One of these architectures combines the DAC, mixer and power amplifier (PA) in a CMOS structure (Power-Mixing-DAC) Fig. 1b. Such a solution could be useful for several systems. Mainly for systems that require high speed, low power consumption or lack of sufficient available space for a PCB. An example for such a system is the Wi-Fi connection in a mobile phone.

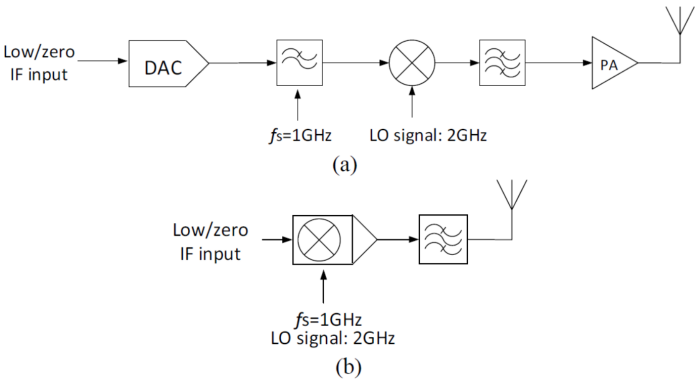


Fig. 1: A traditional transmitter stage (a) and the combined Power-Mixing-DAC

[1]

Because the system is fitted in a CMOS structure, it requires less space, which leads to a more compact solution. This allows the system to be faster, because there are less parasitic capacitances between the structures. Also the need of matching to 50 ohm between these structures becomes superfluous, therefore the system requires components. Using such a combined system solution has as disadvantage that it is hard to generate high power, because power leakage generates heat which can damage the transistors. Moreover the use of large capacitors or inductors is not possible, because these require too much space to create in silicon. Normally these are placed on the PCB.

The paper shows the design and analysis of a Power-Mixing-DAC in 45nm CMOS dummy technology, with as goal a local oscillator (LO) frequency of 2 GHz, a maximum bandwidth of 500MHz, a 20.97dBm output power and a IMD3 >30dBc. The design and analysis is divided in two steps. The first step to create the Power-Mixing-DAC with ideal components, to know where the theoretical boundaries are, this design is used as reference. The second design is composed with transistor components, where the design parameters are chosen to come as close as possible to ideal-component design.

II. Hardware module

When looking deeper in Fig.1b, the architecture of the Power-Mixing-DAC becomes clear. It is differential composed out of several functional blocks: a digital front end structure, a level shifter and an amplifier.

The digital front end synchronizes the data and modulates it with a local oscillator of a 2 GHz square wave. To synchronise the data, D flip flops will be used. The D flip flop has two outputs: Q and $\overline{Q}$. A NAND mixes Q and LO for the PMOS end stage and a NOR mixes $\overline{Q}$ and LO for the NMOS end stage. Before the mixed signals reach the final amplification stage, a level shifter translates the signal from a 1.2V V_DD which are used for the thin-oxide transistors in the digital front end to a 5V V_DD which is used in the final amplification stage. This amplifications stage provides the output power to the 50 ohm matched antenna.

The Power-Mixing-DAC translates a 15 bit unary coded digital signal with a maximum frequency of maximum 500MHz to an analogue signal. Unary coded signals provide higher linearity compared to binary coded signals. One of the reasons is that in the creation process of the transistors, it is more precise to make to transistors of the same size, than to make one with exactly two times the size. Due to the maximum resolution of 16 the signal to noise ratio (SNR) is limited to a theoretical maximum of 25.8dB.

$$SNR = 6.02 + 1.7 25.8dB \quad (1)$$

The specified output current is 50mA, which means that the output power on the 50 ohm matched antenna should be 20.97dBm. The aim is to get an IMD3 of at least 30dBc.

III. System Components

A. Digital front end

The digital front end (DFE) consist of three parts, D flip flop with a NAND and a NOR port. This can been seen in Fig. 2. The D flip flop will synchronise the incoming data and the NAND/NOR gate will up-modulate the signal with the local oscillator in the digital domain. In comparison with the global schematic of the previous group (Appendix: Fig. 18) the DFE consist of one less D flip flop in the diagram. This will

increase the synchronisation of nmos and pmos of the current sources. The DFE works in a high frequency domain and it needs to switch fast. Therefore thin oxide transistors are used. The drawback of this kind of transistors is that they operate at low voltages (max 1.2V), so less power at the output stage. To solve this problem a level shifter is used to increase the power at the output stage. The level shifter is described in paragraph III-B.

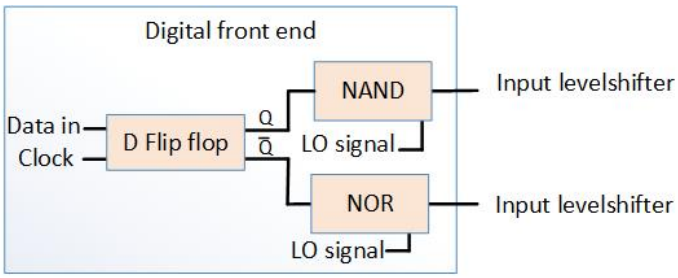


Fig. 2: One side of the diagram of the new digital front end.

1) D flip flop: A D flip flop will be used to synchronise the incoming thermometer coded data to ensure that the transistors of the output stage switch at the same time. There are a couple of challenges that are important to take into account when designing a D flip flop, for example the operation speed and the transition time of the output at the rising clock.

A flip flop can be made in different ways. The two main technologies are in CMOS and CML. The CMOS design is relatively less complex in compare to CML, but in CML there are more parameters that can be modified to tune the output. In this project the CMOS design is used, because it is less complex, single-ended and it can be realised in a short time period.

The CMOS circuit of the previous group is been used as basic circuit. [1] - [2]. The old schematic can been seen in the appendix Fig. 19. The new schematic consist of 32 transistors and is showed in Fig. 3. There are three changes made in compare with the old schematic. The first change is that a second output is been added to flip flop, as mentioned before to reduce one flip flop in the total schematic. The second change is a nmos switch is added to improve the synchronisation between the output and the input. The last change is that the sizes of the nmos and the pmos transistors are changed, to reduce the delay of the output. The size of the nmos and pmos will be further discussed, first the basic principle of a D flip flop is explained.

To explain the principle of a master-slave D flip flop, the schematic can be divided into four parts, settle time of the data, master latch, two switches and slave latch. In the first part the data will be set when the clock is low. The second part, the master will follow the signal of the first part when the clock is low and hold the data when the clock is high. In the third part the switches will be closed when the clock is high. The slave latch(part 4) can set the data and when the clock is high it will hold the data.

The size of the pmos and nmos of part one, two and four are the same. The size of the nmos is set on 50nmx90nm (length x width). The length of the pmos is the same, but the width of the pmos is determined with a parameter sweep to get the smallest delay of transition. In the parameter sweep

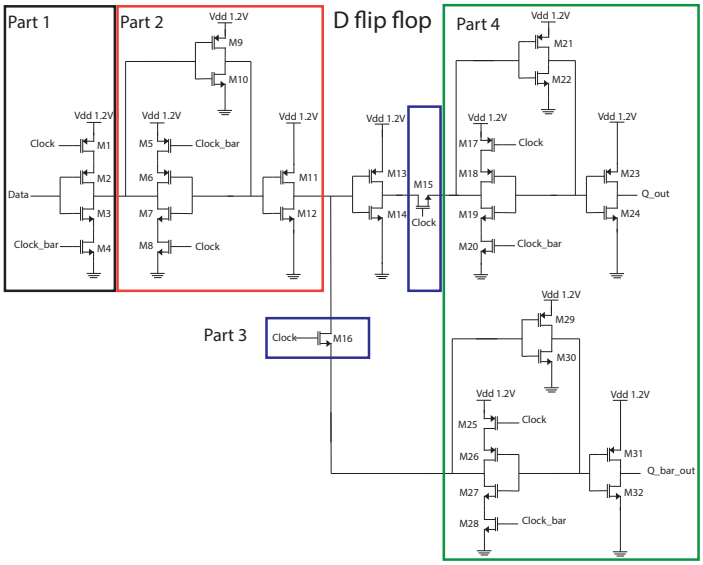


Fig. 3: The improved D flip flop schematic.

the clock frequency is set on 1 GHz and the data frequency is set on 500MHz. The results are showed in the appendix in Fig. 20 and Fig. 21. The optimal width of the pmos is 120nm. It has the smallest delay of transition. The ratio of the width of the pmos and nmos will be 1.33:1.

The size of the switching nmos (part 3) is also determined with a parameter sweep with the same setting. The results are shown in Fig. 22 and Fig. 23 in the appendix. The optimal value of the width is 280nm. The results of this value is compared with the previous schematic and is shown in Fig. 5 and Fig. 4. The overall delay of transition is reduced with 12ps to 13ps of Q and Q bar, but only transition from low to high of Q bar is slightly increased with 2 ps.

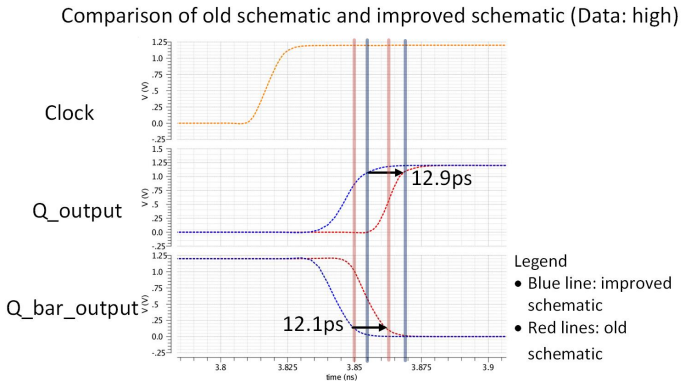


Fig. 4: Comparison of the delay of transition between the old schematic and the new schematic when the data is high

With all the transistors sizes known the critical point can be measured. The minimal time that the data needs to be set is 40ps before the clock is high. The transition delay of Q and Q bar is 29ps when the data is high. When the data is low the delay of Q is 27ps and Q bar is 32ps. This is shown in Fig. 6 and Fig. 7.

In conclusion, in the new schematic the delay of the tran-

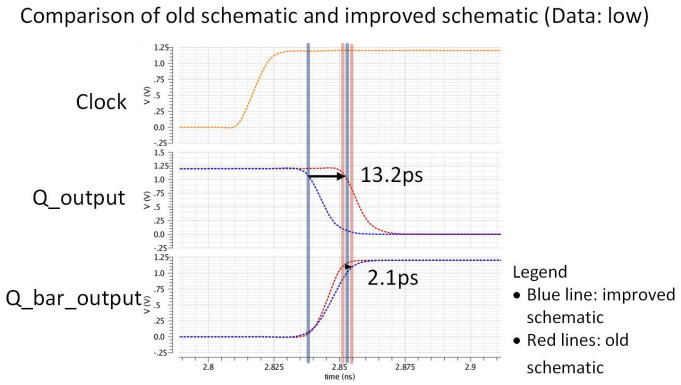


Fig. 5: Comparison of the delay of transition between the old schematic and the new schematic when the data is low.

sition has been reduced and this improves the synchronisation of circuit.

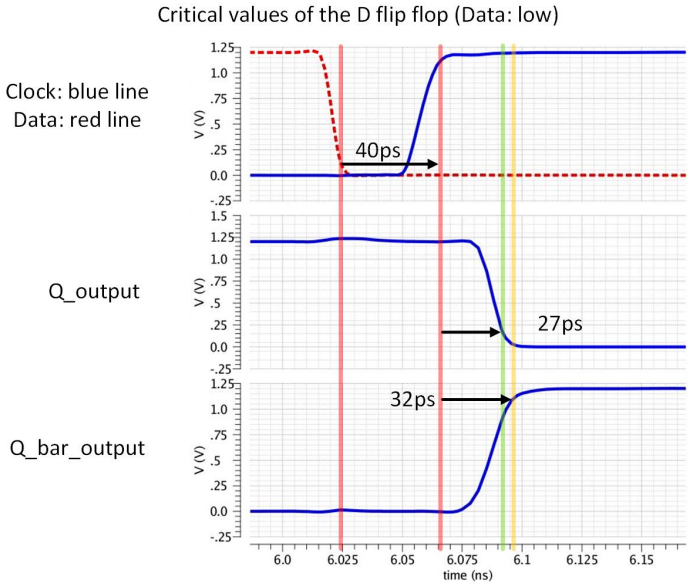


Fig. 6: The critical values when the data goes from high to low

2) NAND/NOR gate: The NAND and NOR will up-modulate the local oscillator signal (LO) with the data from the D flip flop. This will happen in the digital domain with an LO signal of 2Ghz square wave.

The design of a NAND and NOR is shown in Fig. 8 and Fig. 9.

The NAND port has two pmos in parallel and 2 nmos in series. In a normal cmos inverter the width of the pmos is 2 times larger than the nmos. The size of the pmos is 50nmx180nm (length x width). In this situation two nmos transistors are in series. The size of the nmos is been determined with a parameter sweep. The result is shown in the appendix in Fig. 24. The optimal value 180nm is chosen, because it has the same fall and rise time. The size of the nmos and pmos is 50nmx180nm (length x width).

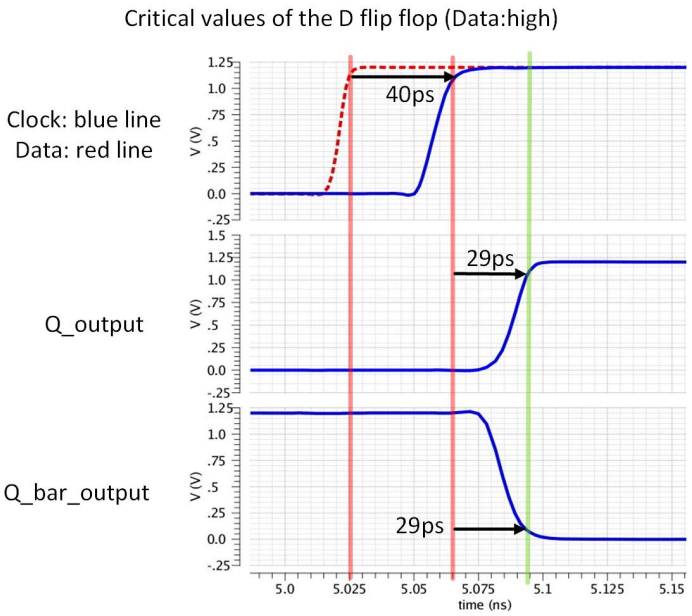


Fig. 7: The critical values when the data goes from low to high.

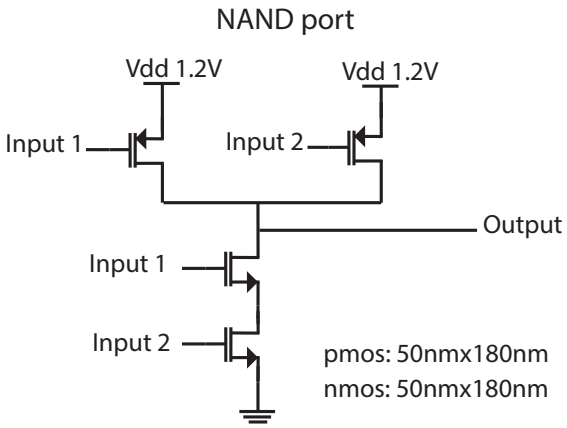


Fig. 8: The schematic of the NAND port.

The NOR port has two pmos in serie and 2 nmos in parallel. The size of the nmos will be the smallest value: 50nmx90nm (length x width). The width of the pmos will be determined with a parameter sweep. The result is shown in the appendix in Fig. 25. The optimal value 280nm is chosen, because it has the same fall and rise time. The size of the pmos is 50nmx280nm (length x width).

B. Levelshifters

To generate sufficient output power thick oxide transitors are used at the output stage. They can generate larger currents compared to thin oxide transistors and support a larger supply voltage. One of the problems with this is that these transistors have a much larger threshold voltage and that the desired gate voltage of the PMOS transistors is entirely out of the range of the thin oxide transistors in the digital front end. Because of this the fast low voltage transitors used in the digital front end cannot generate a large enough V_{ON}. Raising the supply

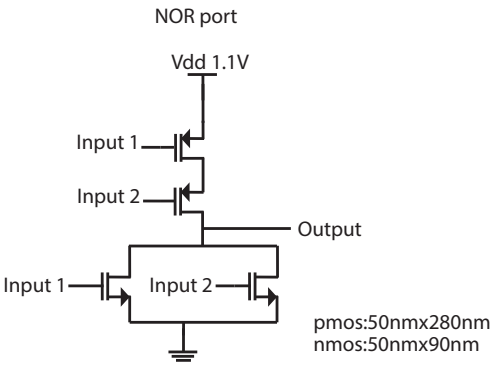


Fig. 9: The schematic of the NAND port.

voltage of the low voltage transistors in order to increase the output voltage of the mixers will break them. So special care has to be taken when a transition from a low voltage circuit to high voltage thick oxide transistors. To this end a level shifter is designed. In this design special care will be taken to ensure that the voltages across any low voltage transistor will not exceed 1.2V, so they will not break. On the output side it has to be able to drive very large transistors. The driven NMOS transistors will have to be supplied with a voltage of 0V(off) to 2V(on) and the driven PMOS transistors with a voltage of 5V(off) to 3V(on).

In [1] a design for the levelshifter was proposed, but they were not able to integrate it with the rest of their design. Some other designs looked at are proposed in [3] and [4]. In this paper the design from [1] is chosen, because the others did not look as promising and are intended for different scenarios compared to the situation in this paper. Designing the levelshifter caused some major problems. First the cadence models originally used have have an unrealistically high threshold voltage of 1.5V, this makes it difficult to drive them with the thin oxide transistors. In order to create a functioning simulation this was changed to a more realistic threshold voltage of 0.7V. This gives a larger V_{ON}, making the transistors conduct more current for a smaller size. This is necessary, because the transistors being driven by the level shifter will be very large. Therefore a large driving current must be supplied by the levelshifter. Another problem that took a lot of time to solve was that the models break down when a 5V V_{DS} is used as a test load transistor. It caused such a large current into the gate that the rest of the levelshifter broke down, without clear indication as to why this happened. Using a V_{DS} of 2.5V for the test loading transistor, which is also more like the final implemenation, solved this.

The design of the levelshifter started with the design of the PMOS driver, which should have an output voltage of 3(off) to 5V(on). As a starting point the design from [1] was used, it is shown on the right in Fig. 10. In this design the thick oxide transistors M3 and M4 serve to protect the thin oxide transistors M5 and M6 from too high voltages. M1 and M2 form a current sensing circuit that charge the output node and each other's gates when switching. Their most important parameter is their width, the larger they are the quicker they charge the output. But a larger M1 and M2 also means that the M3-6 need to be larger to discharges the nodes. Since M2 must drive both M1 and the load it will be bigger than M1. The next most important parameters are the lengths of M3 and M4 and widths of M5 and M6. together they determine the speed at which the output nodes are discharged and the voltage level of the output nodes when M3 and M5 or M4 and M6 are active. The circuit operates as follows. Assume initially VIN is high and $\overline{\text{VIN}}$ is low. Node $\overline{\text{VOUT}}$ will be pulled low by the left branch and the right branch will not conduct any current. Then $\overline{\text{VOUT}}$ is pulled towards 3V and M2 will start conducting and charging node VOUT towards 5V. This will make M1 stop conducting current, causing $\overline{\text{VOUT}}$ to be pulled even closer to 3V. In this way M2 and M1 drive each other's gate and amplify each other, enabling fast switching. When everything is settled VOUT should be near 5V and $\overline{\text{VOUT}}$ near 3V. When the input switches (VIN goes low and $\overline{\text{VIN}}$ goes high) the process is reversed. Node VOUT will be pulled towards 3V and no current will be conducted by the left branch, enabling $\overline{\text{VOUT}}$ to be driven towards 5V. Again, M1 and M2 will amplify this process and switch VOUT from 5V to 3V and vice versa for $\overline{\text{VOUT}}$.

To drive the NMOS transistors of the DAC's output current sources an extra stage is added to the level shifter. Because the threshold voltage is lowered to 0.7V the VIN signal can weakly drive M8 to pull the output to 0V when VIN is high. VOUT is high then, so M7 will not conduct current. When VIN is low, VOUT is near 3V and M7 will conduct current, pulling VOUT_NMOS to 2V. For the NMOS driver important parameters were the length of M7, which largely determines the maximum voltage of the output, and the widths of both M7 and M8, which mostly detemine the speed at which it can switch the load. For both the PMOS and NMOS drivers VBIAS determines the maximum V_{DS} of M5 and M6 and is set to make sure V_{DS} has a maximum value of 1.2V.

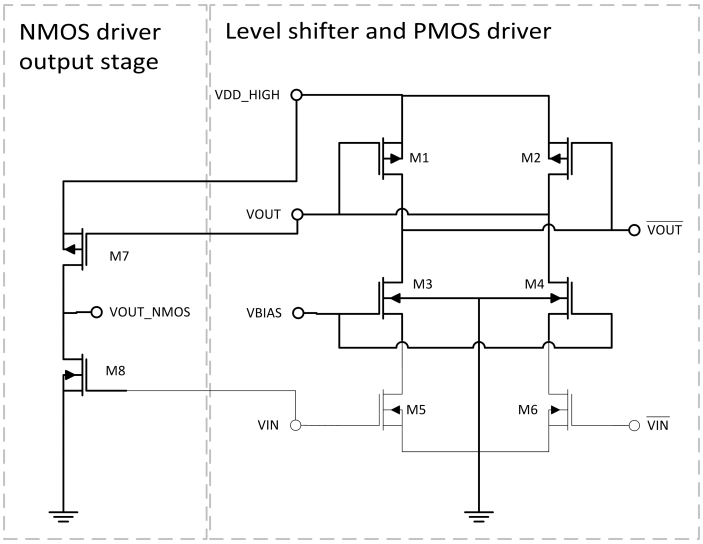


Fig. 10: Schematics of the levelshifter, thick wires indicate a high voltage regime and thin lines the low voltage transistors. On the right the up-shifting PMOS driver is shown. Its output VOUT can drive a PMOS transistor. The NMOS driver's layout is the same with an extra stage added on the left side. The node VOUT_NMOS can drive a NMOS transistor.

The final sizes of transistors in the PMOS and NMOS driving levelshifters are listed in Appendix A in Tables I and II respectively. How these sizes have been determines is discussed next. Both M1 and M2 should have a V_{DS} as low as possible, so their length is set to the minimum of 200n.

Their width determines how fast they can charge the load and each other and is determined using the sweep in Fig. 11. The load of the PMOS driver is a PMOS transistor of size 200nm by 60μm, approximately the size of the current source PMOS transistors. It shows that a larger width is faster, but at some point increasing its size loses effect. Using this sweep it is chosen to be 60μm to allow for a carger loading capacitance. After this the size of M1 was determined in a similar fashion. The output voltage level is most depended on the combination of the lengths of M3 and M4 and widths of M5 and M6, these are determined together by sweeping over both parameters and chosing the value combination that comes closest to 3V. They influence the switching speed, but this variation is small and it is more important that the voltage does not drop below 3V to keep the load PMOS in saturation. Finally the other parameters are fine tuned.

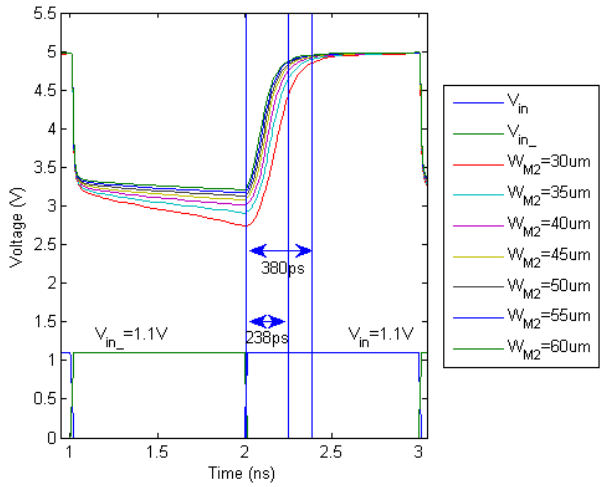


Fig. 11: Parameter sweep of the width of M2, with a thick oxide PMOS transistor of 200nm by 60μm as load.

To determine the sizes of the transistors of the NMOS driver the PMOS driver is used a starting point. This works since it is still only one PMOS transistor being driven by the original circuit, which shows little variation for different load sizes. So initial tuning ofM7 will have little effect on the behaviour of the original circuit. The maximum output voltage level is determined mostly by the dimensions of M7, which are chosen by a combined sweep. The dimensions of M8 determine how fast the output voltage drops. The length is set to the minimum possible value and the width determined using a standard sweep. A too large transistor cannot be driven by the digital front end and too small will not be able to drive the output current sources. The width is chosen such that a larger width does not change the output a lot.

A final aspect of interest is the power consumption of the levelshifter. This is determined mostly by the current necessary for driving the load transistor. The gates of the load are both charged and discharged via the levelshifter, causing most of the powerconsumption. But also the levelshifter's transistors are relatively large and cost significant power to switch. Simulation results are not available yet.

C. Current Sources

The final stage of the power DAC are the current sources. They provide a differential output over a 50Ω resistor. This setup is shown in Fig. 12.

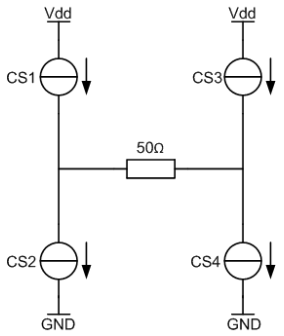


Fig. 12: The final stage of the power DAC: The current sources which will provide the differential output through the resistor.

Due to the local oscillator, the current will alternate between the path through CS1 and CS4 (see Fig. 13a) and the the path through C3 and C2. (see Fig. 13b).

The first design parameters are the voltage supply and the switching devices. Because the DAC should be able to produce 50mA through a 50Ω resistor, the maximum voltage drop will be 2.5V. This already cancels out lower voltage supplies such as 1.2V and 2.5V. The resulting options are 3.3V and 5V. Because the stage consist of two current sources, the voltage headroom will be very limited in the 3.3V voltage supply. Therefore a 5V supply will be used as V_{dd}. This, along with the high switching speeds, limits the switching devices to the thick-oxide CMOS technology.

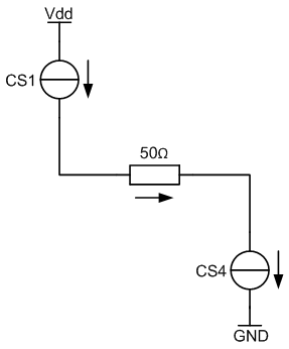
Due to the thick-oxide CMOS technology, the width and length of the CMOS are the only parameters. The most straightforward design method subscribes that the CMOS should always be in saturation so that the current through the CMOS is nearly independent, without channel-length modulation taken into account, of the drain-source voltage of the CMOS. This is directly related to the output impedance of the the switched current source. Therefore Eq. 2 should be valid whatever the drain-source voltage.

$$V_{DS} > V_{TH} + V_{GS} \tag{2}$$

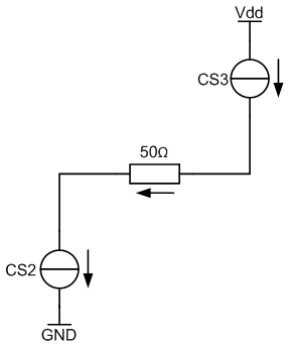
The drain-source voltage of both the NMOS is minimal when the current through the resistor is maximal. This results in a minimum drain-source voltage of 1.25V. Because Eq. 2 should be valid independent of the output, the maximum gate-source provided by the level shifter should be 1.95V, because the threshold voltage of the thick-oxide CMOS is 0.7V. Along with Eq. 3, this would provide a viable current sink.

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \tag{3}$$

So by designing a current sink which operates at a V_{gs} of 1.95V, the switching current sink wil always be in saturation.



(a) One current-steered cycle.



(b) The other current-steered cycle. Vdd is 5V and the maximum current is 50mA.

This provides a high output impedance and thus a high IMD3. Another advantage is the increase in efficiency.

Due to the difference in mobility of electrons and holes, the mobility of a electron is three times higher than the mobility of a hole, the length of the NMOS transistor will be three times higher then the length of the PMOS transistor. Though an larger length has some advantages, decrease in mismatch en less noise, it also means a larger width to maintain the required current through the transistor. A larger width however, means increasing inputcapacitance. To decrease the needed specifications on the level shifter, the length of the PMOS has been chosen to be the minimum possible with the thick-oxide technology, i.e. 300nm. The length of the NMOS is then 900nm.

The width of the NMOS transistors has been determined by a parametric sweep. The width can then be determined so that the current through the transistor is 3.3mA. With the circuit found in Fig. 14 the result is found in Fig. 15.

So the width of the first NMOS should be 30um to guarantee that it will sink 3.3mA when the V_{GS} is 1.95V. Due to the channel-length modulation, it is not sufficient to copy the transistor 15 times. So to determine the width of the second transistor, another transistor will be added to the circuit in Fig. 14 and the V_{out-} will be altered to 2.333V. Then the sweep will take place again until the width has been found for which the circuit sinks 6.667mA. This will be repeated until 15 transistor are switched in parallel and are able to sink 50mA. The list of all widths can be found in table III in the appendix.

The same technique has been used for the PMOS

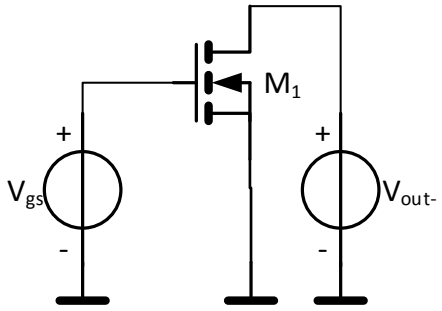


Fig. 14: The circuit used to determine the required width of the transistor to sink 3.3mA. Vout- is 2.4167V ans Vgs is 1.95V.

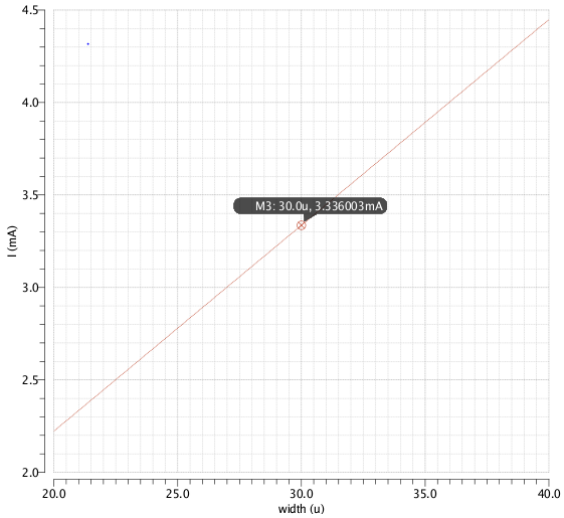


Fig. 15: The current through the transistor versus its width. To make sure that the current through the transistor is 3.3mA, the width should be 30um.

transistors. Due to the dummy technology, which was not able to simulate width over 100um, each bit will be represented by to PMOS in parallel so that the width is maintained within the 100um. This list can also be found in the appendix, table IV.

When all of these transistors are designed in a single set-up, that is a setup as seen in 13a, a sweep can be made through all bits. The results can be found in Fig. 16.

Next paper I will elaborate on the results with the chosen transistors.

IV. Results and Analysis

The specifications are verified by the use of simulations. While providing a one tone signal, a transient measurement of the output power is simulated. This to verify a correct functioning system, that translates the digitals signals as supposed.

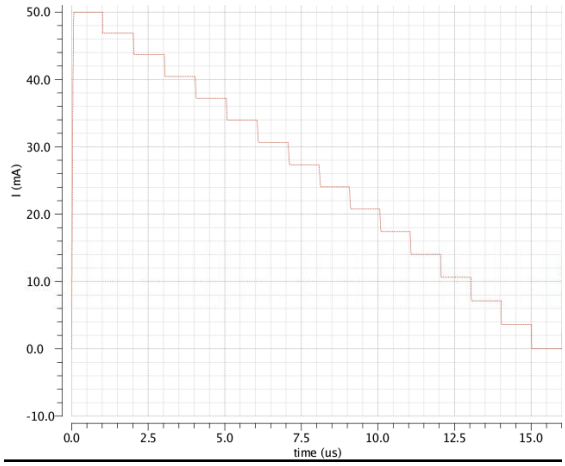


Fig. 16: A sweep through all possible currents, with a maximum of 50mA and a minimum of 0mA.

This holds that the 15 bit digital unary code (Fig. 26) is translated to an analogue signal. Fig. 27

Next a DFT of the output voltage is simulated to see the spectral content of the one tone model. To simulate such a DFT the simulation duration should be chosen wisely, an integer number multiple of the period time, otherwise a single tone will not be shown as a single point in the spectrum. The simulation time is chosen to be 512 LO periods and the first 10 periods are neglected to filter out settling issues. To fit exactly 11 IF periods in this timespan the IF frequency should be 42.97 MHz.

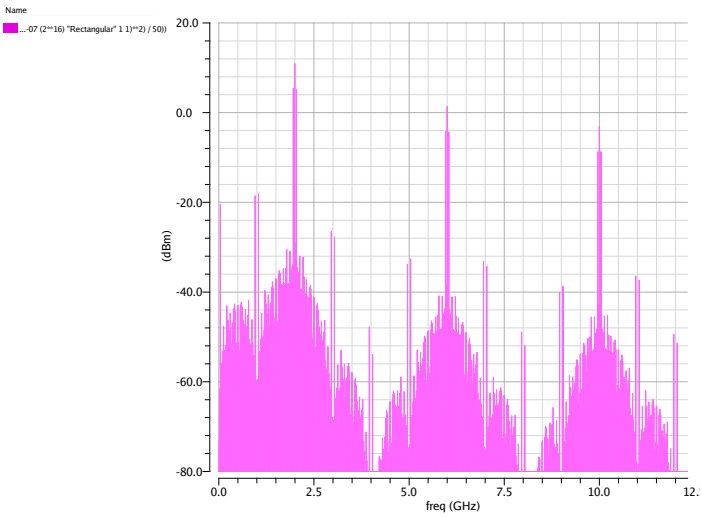


Fig. 17: Single tone spectrical content

Furthermore a two tone test is simulated. The frequency of the second tone is chosen so that 14 cycles fit in the simulation time, which means that the IF frequency of the second tone is equal to 54.69 MHz. Fig. **??** A two tone test is useful test the linearity of the DAC, non-linear behaviour generates intermodulation products at the output of the DAC. The power of these intermodulation products should be low, because they interfere with the modulated IF tones. Especially the third intermodulation product (IM3), because the IM3 frequencies are very close to the fundamental frequency (at 2f2-f1 and 2f1-f2). It is almost impossible to filter IM3 signal out of the output signal; therefore, it is better to prevent creating them. There are more options to express the amount of IM products. For example the spurious-free dynamic range (SFDR) describes power of the fundamental signal to the strongest spurious signal at the output, which is in this case the IM3. Whereas IMD3 describes the difference of the fundamental signal and the IM3.

V. Conclusion

This is the conclusion

Acknowlegdements

Dr. G. Radulov

References

[1] H. Li, B.Yin, J. Cao, Y. Zhang, and R. Wang, "Design of a 4-bit power dac achieving the output power of 16.59dbm with imd3<-31dbc up to 5ghz," 2014.

[2] G. Radulov, "Course book 5tt50, tu/e," 2014.

[3] K.-H. Koo, J.-H. Seo, M.-L. Ko, and J.-W. Kim, "A new level-up shifter for high speed and wide range interface in ultra deep sub-micron," in *Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on*. IEEE, 2005, pp. 1063–1065.

[4] K. J. Hass and D. F. Cox, "Level shifting interfaces for low voltage logic," in *9th NASA Symposium on VLSI Design*. Citeseer, 2000, pp. 3–1.

Appendix A

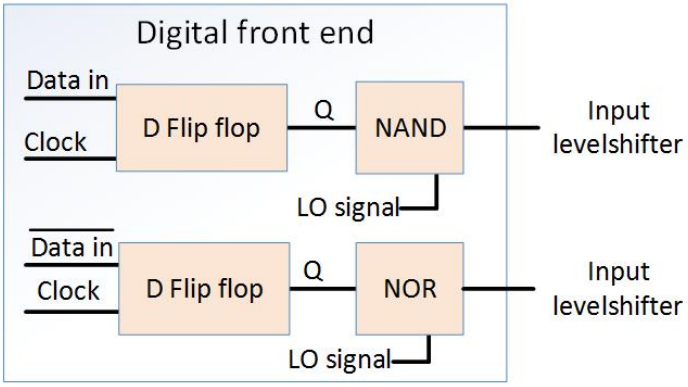


Fig. 18: Global schematic of the previous group.

TABLE I: This table lists the dimensions of the transistors in the levelshifter that drives the PMOS current sources.

Transistor	Width(um)	Length (nm)
M1	20	200
M2	60	200
M3	10	350
M4	10	350
M5	1.2	50
M6	1.2	50

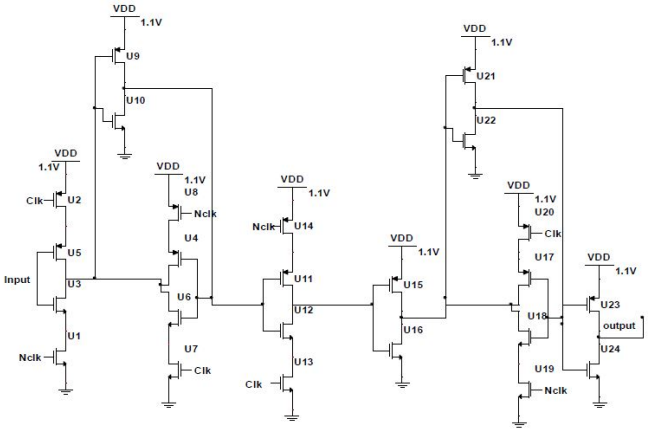


Fig. 19: D flip flop schematic from previous group

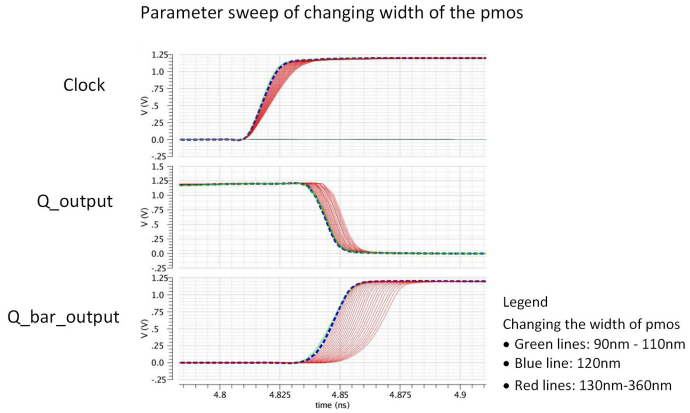


Fig. 20: Parametersweep of changing the width of the pmos when the data is low.

TABLE II: This table lists the dimensions of the transistors in the levelshifter that drives the NMOS current sources.

Transistor	Width(um)	Length (nm)
M1	20	200
M2	60	200
M3	10	350
M4	10	350
M5	1.2	50
M6	1.2	50
M7	50	1700
M8	20	200

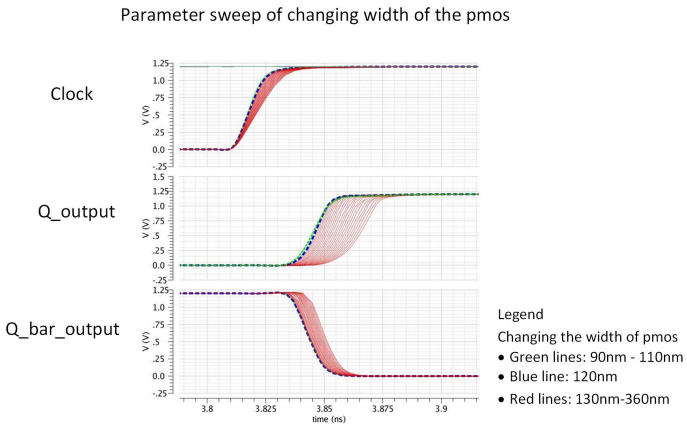


Fig. 21: Parametersweep of changing the width of the pmos when the data is high.

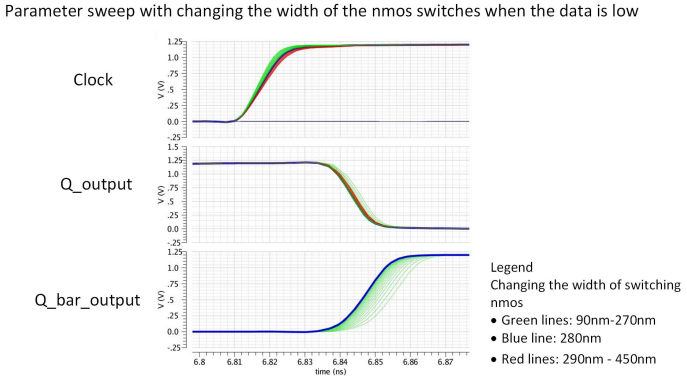


Fig. 22: Parameter sweep of changing the width of the switching nmos when the data is low.

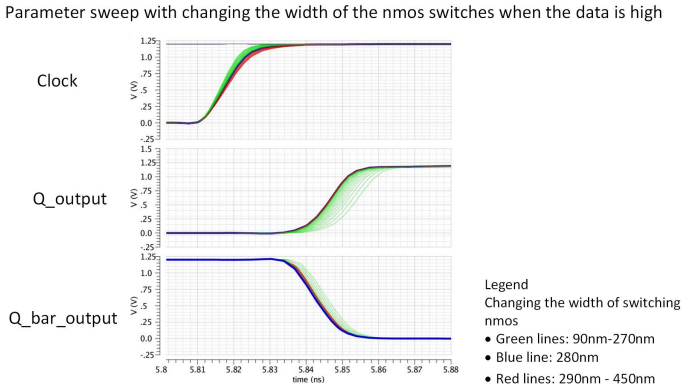


Fig. 23: Parameter sweep of changing the width of the switching nmos when the data is high

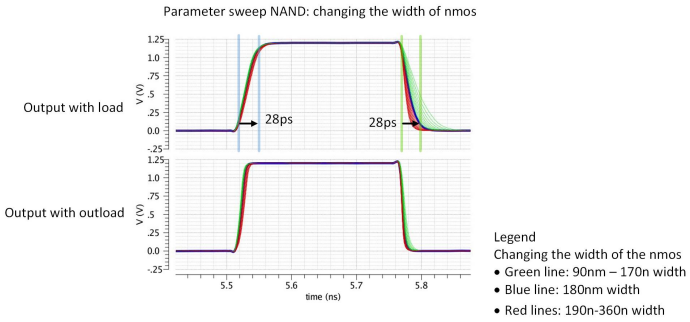


Fig. 24: Parameter sweep of changing the width nmos of the NAND.

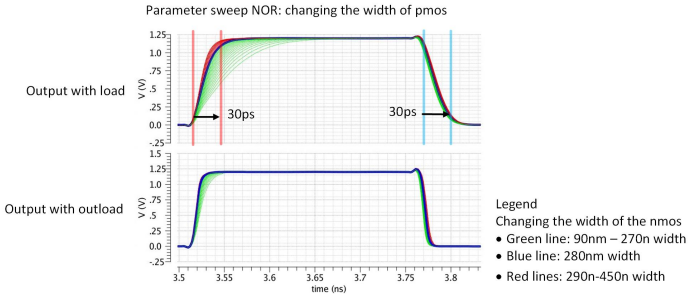


Fig. 25: Parameter sweep of changing the width pmos of the NOR.

TABLE III: This table describes which widths and lengths are used for which NMOS transistors. M1 is the MOSFET which is associated with the lowest current while M15 is associated with the highest current.

NMOS	Width(um)	Length (um)
M1	30.00	0.9
M2	30.17	0.9
M3	30.30	0.9
M4	30.30	0.9
M5	30.36	0.9
M6	30.44	0.9
M7	30.49	0.9
M8	30.57	0.9
M9	30.66	0.9
M10	30.74	0.9
M11	30.83	0.9
M12	30.95	0.9
M13	31.05	0.9
M14	31.18	0.9
M15	31.33	0.9

TABLE IV: This table describes which widths and lengths are used for which PMOS transistors. M1 is the MOSFET which is associated with the lowest current while M15 is associated with the highest current.

PMOS	Width(um)	Length (um)
M1	56.23	0.3
M2	57.25	0.3
M3	57.63	0.3
M4	57.84	0.3
M5	58.04	0.3
M6	58.28	0.3
M7	58.56	0.3
M8	58.87	0.3
M9	59.21	0.3
M10	59.57	0.3
M11	59.95	0.3
M12	60.36	0.3
M13	60.82	0.3
M14	61.31	0.3
M15	61.87	0.3

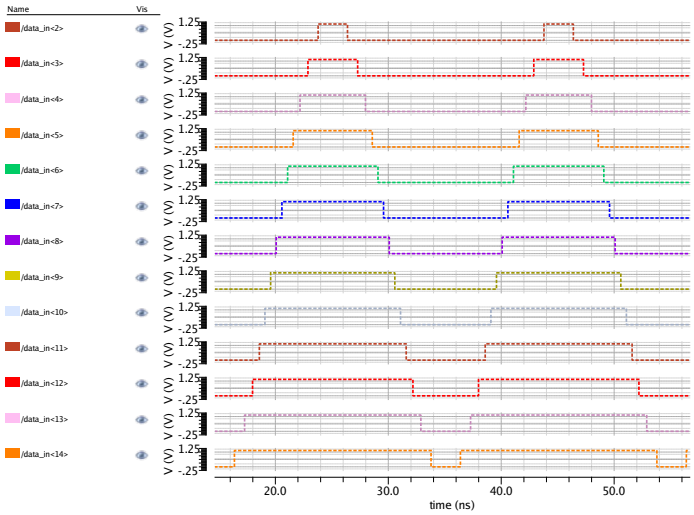


Fig. 26: Thermometer single tone voltage output.

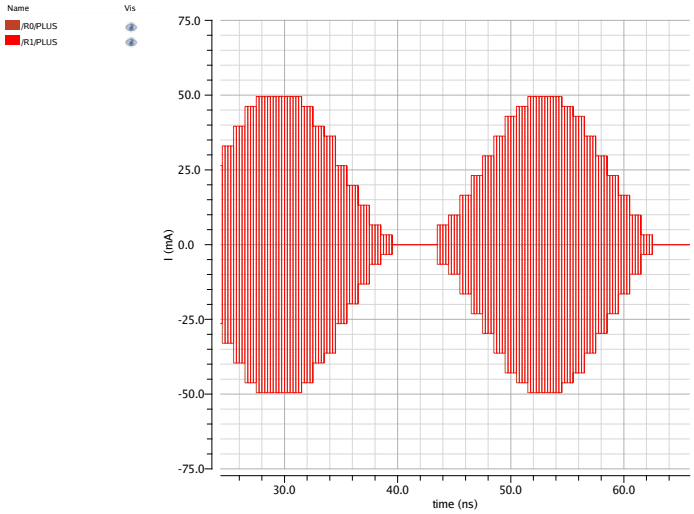


Fig. 27: Output current

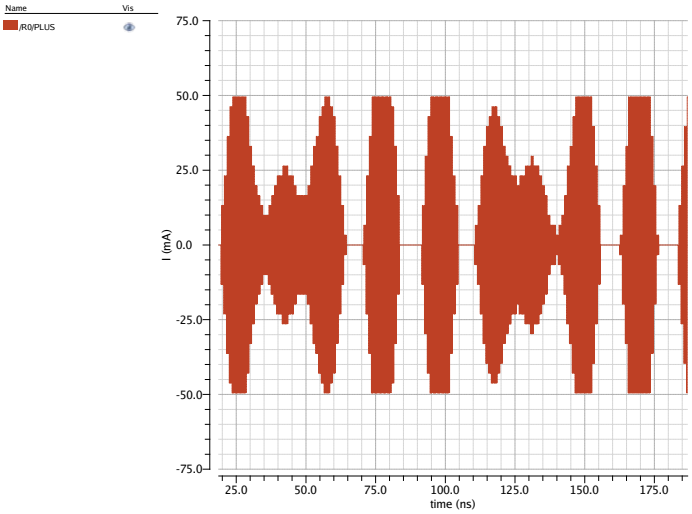


Fig. 28: Two tone output current