Power Mixing DAC

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***Abstract*—This is the abstract**

I. Introduction

In telecommunication applications there is the need to translate digital stored information to an analogue signal that can be send by an antenna. Now a days there are many architectures to accomplish this, where most are distracted from a more traditional architecture. Fig. 1a. One of these architectures combines the DAC, mixer and power amplifier (PA) in a CMOS structure (Power-Mixing-DAC) Fig. 1b. Such a solution could be useful for several systems. Mainly for systems that require high speed, low power consumption or lack of sufficient available space for a PCB. One example for such a system is the Wi-Fi connection in a mobile phone.

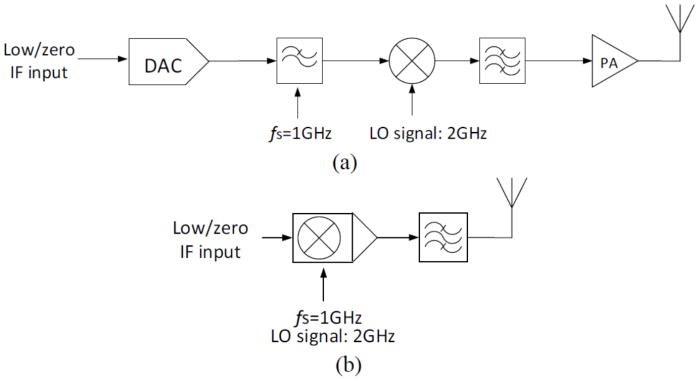

Fig. 1: A traditional transmitter stage (a) and the combined Power-Mixing-DAC.

[1]

Because the system is fitted in a CMOS structure, it requires less space, which leads to a more compact solution. This allows the system to be faster, because there are less parasitic capacitances between the structures. Also the need of matching to 50 ohm between these structures becomes superfluous, therefore the system requires components. Using such a combined system solution has as disadvantage that it is hard to generate high power, because power leakage generates heat which can damage the transistors. Moreover the use of large capacitors or inductors is not possible, because these require too much space to create in silicon. Normally these are placed on the PCB.

The paper shows the design and analysis of a Power-Mixing-DAC in a 45nm CMOS dummy technology, with as goal a local oscillator (LO) frequency of 2 GHz, a maximum bandwidth of 500MHz, a 20.97dBm output power and a IMD3 > 30dBc. The design and analysis is divided in two steps. The first step to create the Power-Mixing-DAC with ideal components, to know where the theoretical boundaries are, this design is used as reference. The second design is composed with transistor components, where the design parameters are chosen to come as close as possible to ideal-component design.

II. Hardware module

When looking deeper in Fig. 1b, the architecture of the Power-Mixing-DAC becomes clear. It is differential composed out of several functional blocks: a digital front end structure, a level shifter and an amplifier.

The digital front end synchronizes the data and modulates it with a local oscillator of a 2 GHz square wave. To synchronise the data, D flip flops will be used. The D flip flop has two outputs: Q and $\overline{Q}$. A NAND mixes Q and LO for the PMOS end stage and a NOR mixes $\overline{Q}$ and LO for the NMOS end stage. Before the mixed signals reach the final amplification stage, a level shifter translates the signal from a 1.2V $V_D D$ which are used for the thin-oxide transistors in the digital front end to a 5V $V_D D$ which is used in the final amplification stage. This amplifications stage provides the output power to the 50 ohm matched antenna.

The Power-Mixing-DAC translates a 15 bit unary coded digital signal with a maximum frequency of maximum 500MHz to an analogue signal. Unary coded signals provide higher linearity compared to binary coded signals. One of the reasons is that in the creation process of the transistors, it is more precise to make to transistors of the same size, than to make one with exactly two times the size. Due to the maximum resolution of 16 the signal to noise ratio (SNR) is limited to a theoretical maximum of 25.8dB.

$$SNR = 6.02 \times n + 1.76 = 25.8dB \tag{1}$$

The specified output current is 50mA, which means that the output power on the 50 ohm matched antenna should be 20.97dBm. The aim is to get an IMD3 of at least 30dBc.

III. System Components

A. Digital front end

The digital front end (DFE) consist of three parts, D flip flop with a NAND and a NOR port. This can been seen in Fig. 2. The D flip flop will synchronise the incoming data and the NAND/NOR gate will up-modulate the signal with the local oscillator in the digital domain. In comparison with the global schematic of the previous group (Appendix: Fig. 19) the DFE consist of one less D flip flop in the diagram. This will increase the synchronisation of nmos and pmos of the current sources. The DFE works in a high frequency domain and it needs to switch fast. Therefore thin oxide transistors are used. The drawback of this kind of transistors is that they operate at low voltages (max 1.2V), so less power at the output stage. To solve this problem a level shifter is used to increase the power at the output stage. The level shifter is described in paragraph III-B.

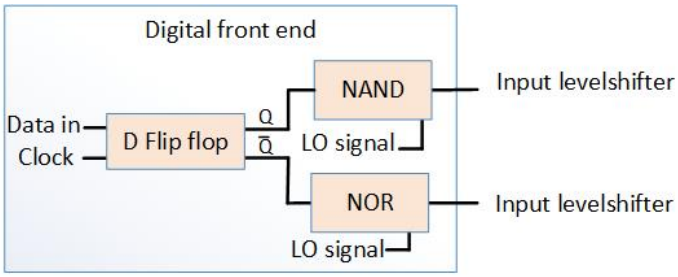

Fig. 2: One side of the diagram of the new digital front end.

1) D flip flop: A D flip flop will be used to synchronise the incoming thermometer coded data to ensure that the transistors of the output stage switch at the same time. There are a couple of challenges that are important to take into account when designing a D flip flop, for example the operation speed and the transition time of the output at the rising clock.

A flip flop can be made in different ways. The two main technologies are in CMOS and CML. The CMOS design is relatively less complex in compare to CML, but in CML there are more parameters that can be modified to tune the output. In this project the CMOS design is used, because it is less complex, single-ended and it can be realised in a short time period.

The CMOS circuit of the previous group is been used as basic circuit. [1] - [2]. The old schematic can been seen in the appendix Fig. 20. The new schematic consist of 32 transistors and is showed in Fig. 3. There are three changes made in compare with the old schematic. The first change is that a second output is been added to flip flop, as mentioned before to reduce one flip flop in the total schematic. The second change is a nmos switch is added to improve the synchronisation between the output and the input. The last change is that the sizes of the nmos and the pmos transistors are changed, to reduce the delay of the output. The size of the nmos and pmos will be further discussed, first the basic principle of a D flip flop is explained.

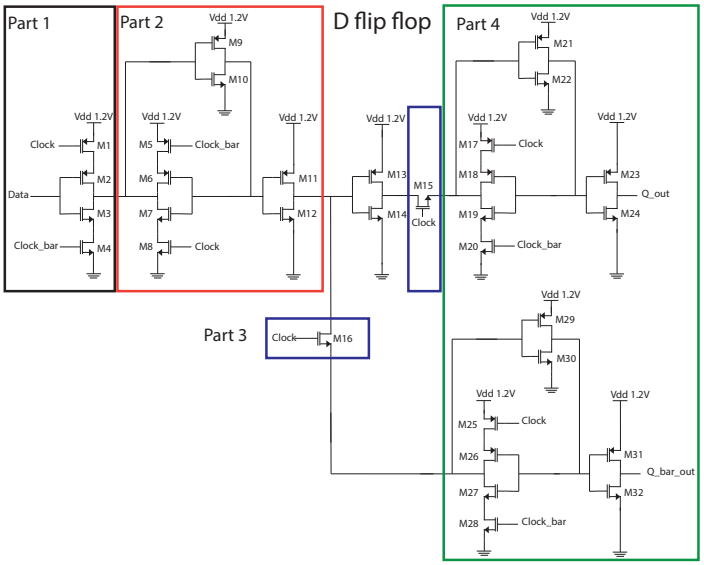

Fig. 3: The improved D flip flop schematic.

To explain the principle of a master-slave D flip flop, the schematic can be divided into four parts, settle time of the data, master latch, two switches and slave latch. In the first part the data will be set when the clock is low. The second part, the master will follow the signal of the first part when the clock is low and hold the data when the clock is high. In the third part the switches will be closed when the clock is high. The slave latch(part 4) can set the data and when the clock is high it will hold the data.

The size of the pmos and nmos of part one, two and four are the same. The size of the nmos is set on 50nmx90nm (length x width). The length of the pmos is the same, but the width of the pmos is determined with a parameter sweep to get the smallest delay of transition. In the parameter sweep the clock frequency is set on 1 GHz and the data frequency is set on 500MHz. The results are showed in the appendix in Fig. 21 and Fig. 22. The optimal width of the pmos is 120nm. It has the smallest delay of transition. The ratio of the width of the pmos and nmos will be 1.33:1.

The size of the switching nmos (part 3) is also determined with a parameter sweep with the same setting. The results are shown in Fig. 23 and Fig. 24 in the appendix. The optimal value of the width is 280nm. The results of this value is compared with the previous schematic and is shown in Fig. 5 and Fig. 4. The overall delay of transition is reduced with 12ps to 13ps of Q and Q bar, but only transition from low to high of Q bar is slightly increased with 2 ps.

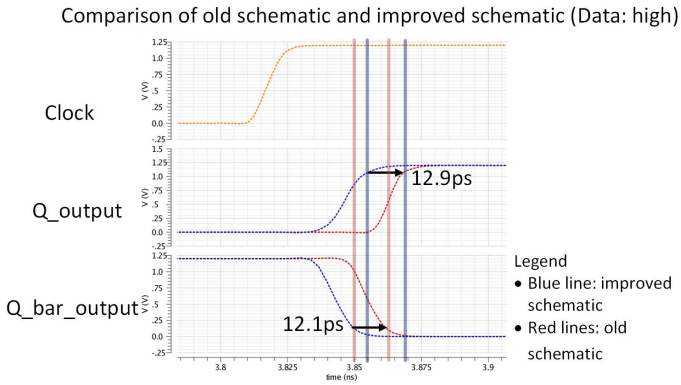

Fig. 4: Comparison of the delay of transition between the old schematic and the new schematic when the data is high

With all the transistors sizes known the critical point can be measured. The minimal time that the data needs to be set is 40ps before the clock is high. The transition delay of Q and Q bar is 29ps when the data is high. When the data is low the delay of Q is 27ps and Q bar is 32ps. This is shown in Fig. 6 and Fig. 7.

In conclusion, in the new schematic the delay of the transition has been reduced and this improves the synchronisation of circuit.

2) NAND/NOR gate: The NAND and NOR will up-modulate the local oscillator signal (LO) with the data from the D flip flop. This will happen in the digital domain with an LO signal of 2Ghz square wave.

The design of a NAND and NOR is shown in Fig. 8 and Fig. 9.

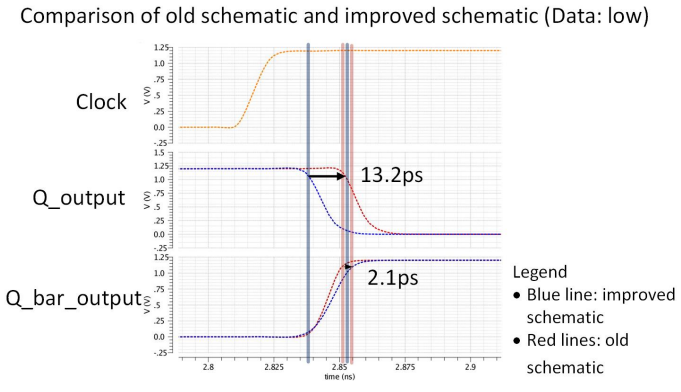

Fig. 5: Comparison of the delay of transition between the old schematic and the new schematic when the data is low.

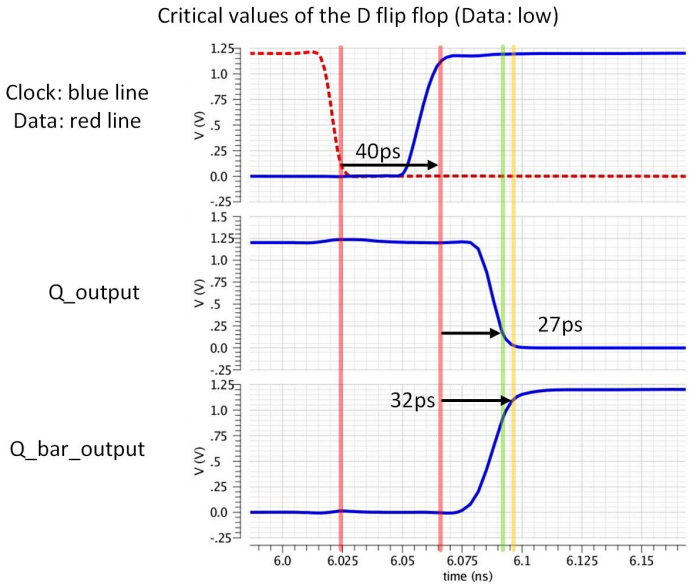

Fig. 6: The critical values when the data goes from high to low

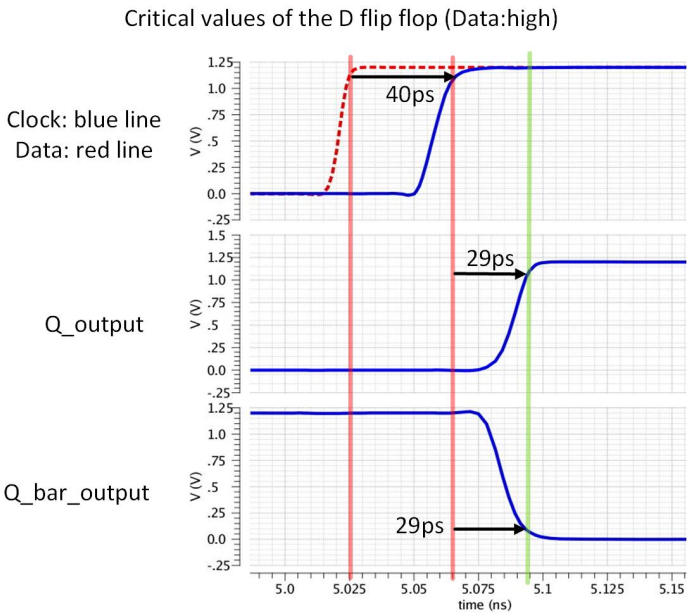

Fig. 7: The critical values when the data goes from low to high.

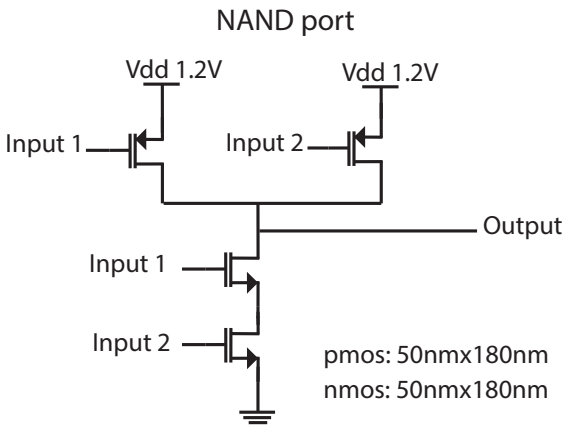

Fig. 8: The schematic of the NAND port.

The NAND port has two pmos in parallel and 2 nmos in series. In a normal cmos inverter the width of the pmos is 2 times larger than the nmos. The size of the pmos is 50nmx180nm (length x width). In this situation two nmos transistors are in series. The size of the nmos is been determined with a parameter sweep. The result is shown in the appendix in Fig. 25. The optimal value 180nm is chosen, because it has the same fall and rise time. The size of the nmos and pmos is 50nmx180nm (length x width).

The NOR port has two pmos in serie and 2 nmos in parallel. The size of the nmos will be the smallest value: 50nmx90nm (length x width). The width of the pmos will be determined with a parameter sweep. The result is shown in the appendix in Fig. 26. The optimal value 280nm is chosen, because it has the same fall and rise time. The size of the pmos is 50nmx280nm (length x width).

B. *Levelshifters*

To generate sufficiënt output power thick oxide transitors are used at the output stage. One of the problems with this is that these transistors have a much larger threshold voltage and that they operate at larger supply voltages than the low voltage transistors. Because of this the fast low voltage transitors used in the digital front end and for mixing cannot generate a large enough V_{ON}. Raising the supply voltage to the low voltage transistors in order to increase the output voltage of the mixers will break them. So special care has to be taken when a transition from a low voltage circuit to high voltage thick oxide transistors. To this end a level shifter is designed. In this design special care will be taken to ensure that the voltages across any low voltage transistor will not exceed 1.1V, so they will not break. On the output side it has to be able to drive very large transistors. The driven NMOS transistors will have to be supplied with a voltage of 0V(off) to 2V(on) and the driven PMOS transistors with a voltage of 5V(off) to 3V(on).

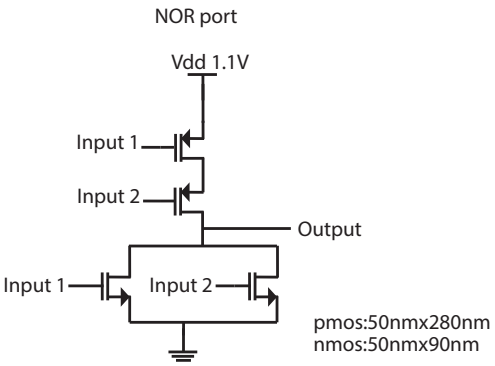

Fig. 9: The schematic of the NAND port.

In [1] a design for the levelshifter was proposed, but they were not able to integrate it with the rest of their design. However, they did show work that it worked in a standalone simulation. The main problem are difficulties with the cadence models of the thick oxide transistors used for simulation. These models show strange behavior and have an unrealistically high threshold voltage of 1.5V. In order to create a functioning simulation this was changed to a more realistic threshold voltage of 0.7V. This gives a larger VON, making the transistors conduct more current for a smaller size. This is necessary, because the transistors being driven by the level shifter will be very large. Therefore a large driving current must be supplied by the levelshifter. Another problem with the models is that they breakdown with too high VON and starts flowing through the base. This also limits the driving capability of the levelshifter. Also a design proposed in [3] was considered. But due to the increased complexity combined with our models and its multiple stages, which are bad for timing performance, this design was not used. That design has an propagation delay of roughly 10 ns, which is not acceptable for this paper's design.

The chosen design is a modified version of the one proposed in [1] and is shown in Fig. 10. The inputs are connected to the gates of the low voltage transistors M5 and M6 and have an input range of 0V(off) to 1.1V(on). For correct operation VIN and $\overline{\text{VIN}}$ must be each other's logical inverse. VBIAS is set to ??V and is connected to the gates of M3 and M4. These transistors protect M5 and M6 from the high supply voltage. M1 and M2 provide an positive feed back loop, which makes the circuit function. Its operation is explained using a low to high transition, so initially VIN is 0V, $\overline{\text{VIN}}$ is 1.1V, VOUT is on its off value and $\overline{\text{VOUT}}$ is 2V. In this situation only the right branch is conducting current, because $\overline{\text{VIN}}$ is high and since there is no current in the left branch $\overline{\text{VOUT}}$ is low. When VIN transitions to a high state, it starts conducting current, forcing VM5 to go a bit higher, as well as $\overline{\text{VOUT}}$. Because $\overline{\text{VOUT}}$ increases, the current through the right branch decreases as well as VOUT. The decreased VOUT makes the left branch conduct more current and $\overline{\text{VOUT}}$ go higher. Due to this postive feedback loop VOUT will go to VDD. To drive the NMOS transistors the levelshifter also needs another output stage, which can consist of a thick oxide PMOS and an NMOS transistor. the PMOS will be driven by VOUT and the NMOS by VIN. To gether the can rase the ON voltage to 2V compared to the output voltage of 1.1V from the low voltage transistors.

A parameter sweep is shown in Fig. 11. It shows that the

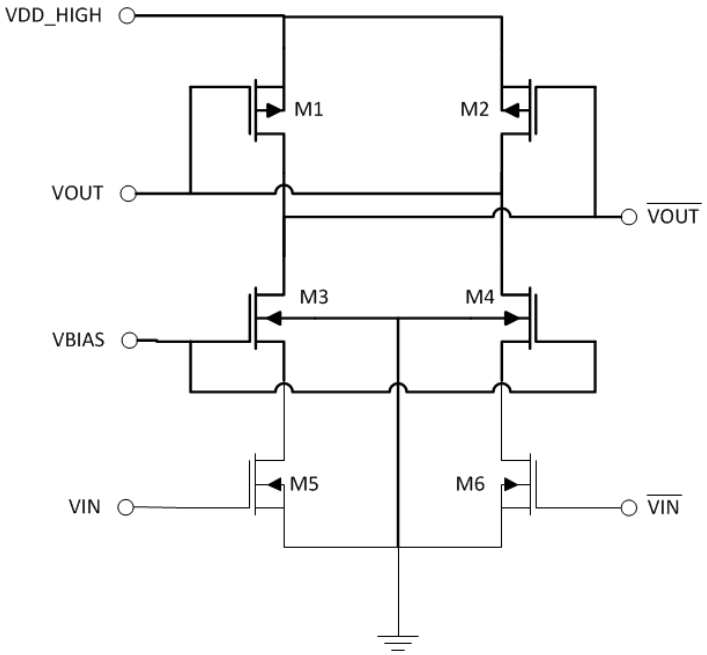

Fig. 10: Schematics of the levelshifter, thick wires indicate a high voltage regime and thing the low voltage transistors

circuit should be able to function. The sweep is simulated while the level shifter is driving the gate of a thick oxide PMOS transistor that is 60 μm wide and 300 nm long. In this sweep the width of transistor M2 is swept from 30 to 60 μm and it shows the impact of this parameter on the rise time. Using this simulation the width of M2 is chosen to be 45 μm, because it sets the on voltage close to the desired 3V and the difference in risetime compared to larger widths is very small. However, to meet the requirments of a 2 GHz LO frequency, the circuit still must become significantly faster.

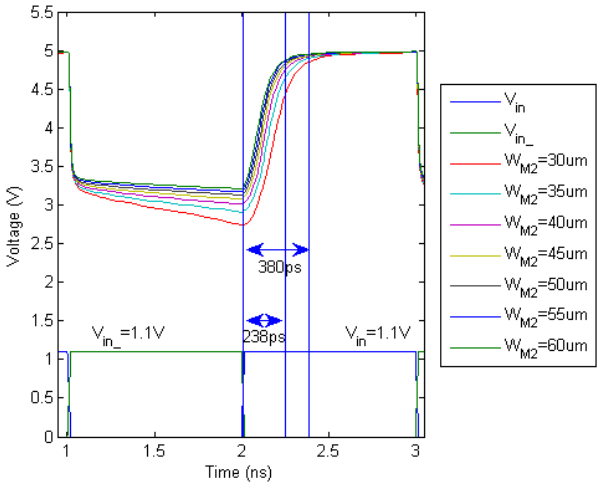

Fig. 11: Early simulation results of the levelshifter

A final aspect of interest is the power consumption of the levelshifter. This is determined mostly by the current necessary for driving the load transistor. The gates of the load are both

charged and discharged via the levelshifter, causing most of the powerconsumption. But also the levelshifter's transistors are relatively large and cost significant power to switch. Simulation results are not available yet.

C. Current Sources

The final stage of the power DAC are the current sources. They provide a differential output over a 50Ω resistor. This setup is shown in Fig. 12.

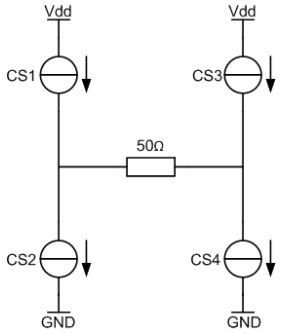

Fig. 12: The final stage of the power DAC: The current sources which will provide the differential output through the resistor.

Due to the local oscillator, the current will alternate between the path through CS1 and CS4 (see Fig. 13) and the the path through C3 and C2. (see Fig. 13).

The first design parameters are the voltage supply and the switching devices. Because the DAC should be able to produce 50mA through a 50Ω resistor, the maximum voltage drop will be 2.5V. This already cancels out lower voltage supplies such as 1.2V and 2.5V. The resulting options are 3.3V and 5V. Because the stage consist of two current sources, the voltage headroom will be very limited in the 3.3V voltage supply. Therefore a 5V supply will be used as V_{dd}. This, along with the high switching speeds, limits the switching devices to the thick-oxide CMOS technology.

Due to the thick-oxide CMOS technology, the width and length of the CMOS are the only parameters. The most

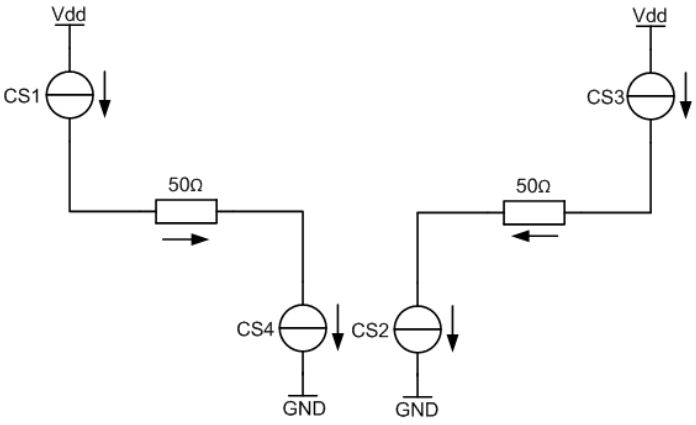

Fig. 13: The two different current transistion modes. Vdd is 5V.

straightforward design method subscribes that the CMOS should always be in saturation so that the current through the CMOS is nearly independent, without channel-length modulation taken into account, of the drain-source voltage of the CMOS. This is directly related to the output impedance of the the switched current source. Therefore Eq. 2 should be valid whatever the drain-source voltage.

$$V_{DS} > V_{TH} + V_{GS} \tag{2}$$

The drain-source voltage of both the NMOS is minimal when the current through the resistor is maximal. This results in a minimum drain-source voltage of 1.25V. Because Eq. 2 should be valid independent of the output, the maximum gate-source provided by the level shifter should be 1.95V, because the threshold voltage of the thick-oxide CMOS is 0.7V. Along with Eq. 3, this would provide a viable current sink.

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \tag{3}$$

So by designing a current sink which operates at a V_{gs} of 1.95V, the switching current sink will always be in saturation. This provides a high output impedance and thus a high IMD3. Another advantage is the increase in efficiency.

The thick-oxide technology however, limits other parameters. The length of the thick-oxide CMOS transistor has as minimum of 200nm when the maximum available voltage headroom is 2.5V. In this configuration however, the maximum available voltage headroom needs to be minimal 2.5V. This limits the length of the transistor to a minimum of 300nm. Though an larger length has some advantages, decrease in mismatch en less noise, it also means a larger width to maintain the required current through the transistor. A larger width however, means increasing inputcapacitance. To decrease the needed specifications on the level shifter, the length of both the PMOS ans the NMOS has been chosen to be optimized within the thick-oxide technology, i.e. 300nm.

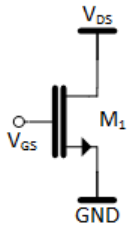

Fig. 14: The circuit used to determine the required width of the transistor to sink 3.3mA. V_{DS} is 2.4167V and V_{GS} is 1.95V.

The primary focus on each transistor is to make sure that it is able to handle the needed amount of current. As has been mentioned before, due to the channel-length modulation, M1 must be able to handle more current when the load is conducting 50mA as M15. Therefore every transistor has to be redesigned. The first transistor has been designed with the circuit found in Fig.14. With this circuit a parametric sweep will be conducted to find the minimum width, to decrease

the input capacitance of the transistor, to be able to conduct the required amount of current. This parametric sweep can be found in 15.

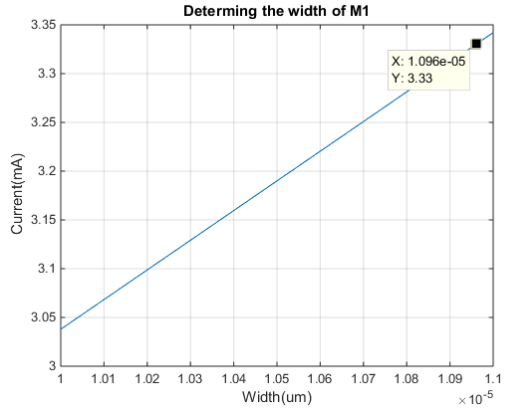

Fig. 15: The current through the transistor versus its width. To make sure that the current through the transistor is 3.3mA, the width should be 10.96um.

So the width of the first NMOS should be 10.96um to guarantee that it will sink 3.3mA when the V_{GS} is 1.95V.

For the second transistor, a similar approach has been taken. Because the drain-source current will decrease, the current through M1 will increase. Therefore the second transistor is placed in parallel with M1, as it will be in the final design, and the width of the second transistor will be swept so that the transistors together will conduct 6.66mA. This technique will be repeated for each transistor. The list of all width and lengths of all NMOS thick-oxide transistors can be found in the appendix, table I.

The same technique has been used for the PMOS transistors. Due to the dummy technology, which was not able to simulate width over 100um, each bit will be represented by to PMOS in parallel so that the width is maintained within the 100um. This list can also be found in the appendix, table II.

When all of these transistors are designed in a single setup, that is a setup as seen in 13, a sweep can be made through all bits. The results can be found in Fig. 16. However, due to the switching and imperfections in both the NMOS and the PMOS, a common-mode error is present in the current. This error is signal dependent, as can be seen in Fig.17.

IV. Results and Analysis

The specifications are verified by the use of simulations. While providing a one tone signal, a transient measurement of the output power is simulated. This to verify a correct functioning system, that translates the digitals signals as supposed. This holds that the 15 bit digital unary code (Fig. 27) is translated to an analogue signal. Fig. 28

Next a DFT of the output voltage is simulated to see the spectral content of the one tone model. To simulate such a DFT the simulation duration should be chosen wisely, an integer number multiple of the period time, otherwise a single tone

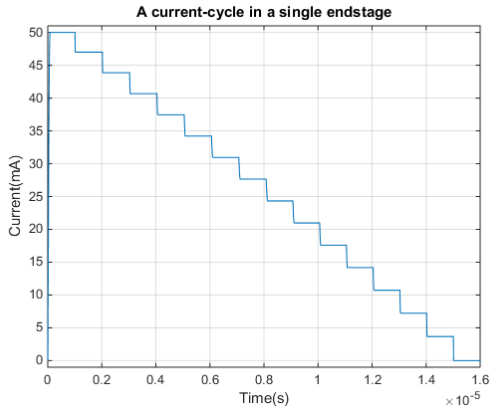

Fig. 16: A sweep through all possible currents, with a maximum of 50mA and a minimum of 0mA.

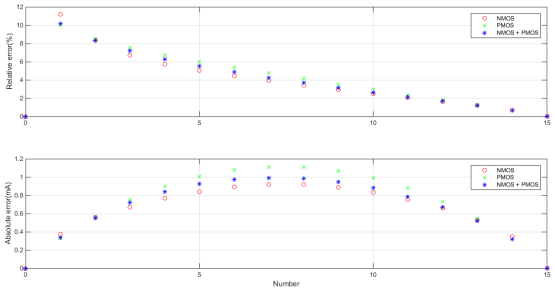

Fig. 17: The absolute and the relative current error in the endstage versus the input number of the DAC.

will not be shown as a single point in the spectrum. The simulation time is chosen to be 512 LO periods and the first 10 periods are neglected to filter out settling issues. To fit exactly 11 IF periods in this timespan the IF frequency should be 42.97 MHz.

Furthermore a two tone test is simulated. The frequency of the second tone is chosen so that 14 cycles fit in the simulation time, which means that the IF frequency of the second tone is equal to 54.69 MHz. Fig. **??** A two tone test is useful test the linearity of the DAC, non-linear behaviour generates intermodulation products at the output of the DAC. The power of these intermodulation products should be low, because they interfere with the modulated IF tones. Especially the third intermodulation product (IM3), because the IM3 frequencies are very close to the fundamental frequency (at 2f2-f1 and 2f1-f2). It is almost impossible to filter IM3 signal out of the output signal; therefore, it is better to prevent creating them. There are more options to express the amount of IM products. For example the spurious-free dynamic range (SFDR) describes power of the fundamental signal to the strongest spurious signal at the output, which is in this case the IM3. Whereas IMD3 describes the difference of the fundamental signal and the IM3.

V. Conclusion

This is the conclusion

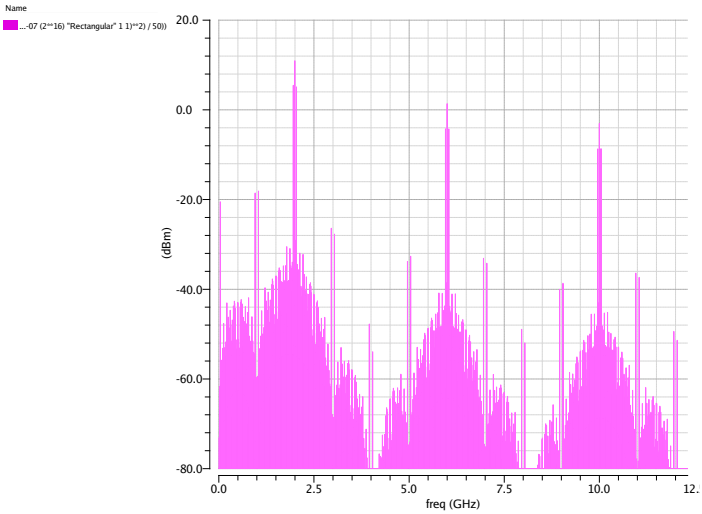

Fig. 18: Single tone spectrical content

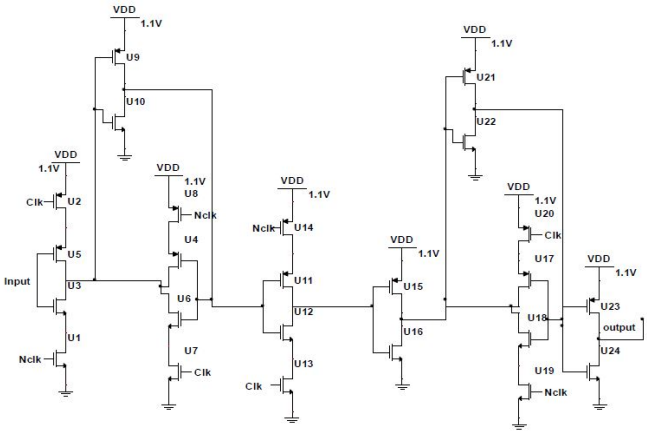

Fig. 20: D flip flop schematic from previous group

ACKNOWLEGDEMENTS

Dr. G. Radulov

REFERENCES

[1] H. Li, B.Yin, J. Cao, Y. Zhang, and R. Wang, "Design of a 4-bit power dac achieving the output power of 16.59dbm with imd3<-31dbc up to 5ghz," 2014.

[2] G. Radulov, "Course book 5tt50, tu/e," 2014.

[3] K. J. Hass and D. F. Cox, "Level shifting interfaces for low voltage logic," in *9th NASA Symposium on VLSI Design*. Citeseer, 2000, pp. 3–1.

VI. APPENDIX

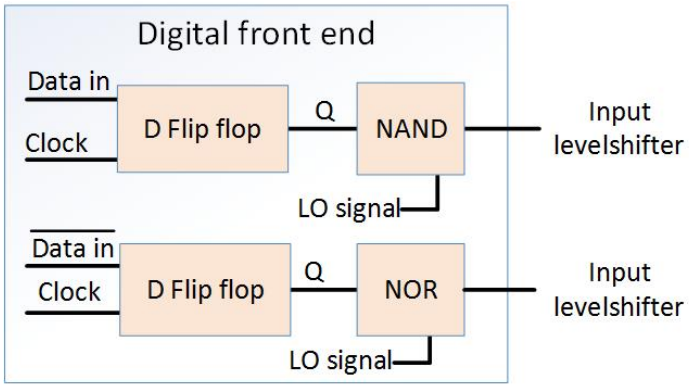

Fig. 19: Global schematic of the previous group.

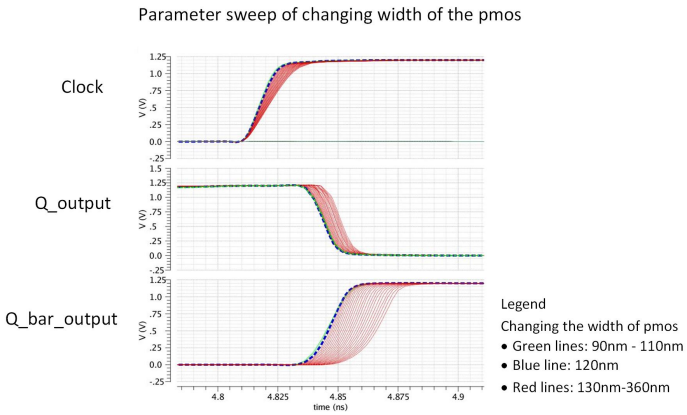

Fig. 21: Parametersweep of changing the width of the pmos when the data is low.

TABLE I: This table describes which widths and lengths are used for which NMOS transistors. M1 is the MOSFET which is associated with the lowest current while M15 is associated with the highest current.

NMOS	Width(um)	Length (um)
M1	10.97	0.3
M2	11.47	0.3
M3	11.60	0.3
M4	11.53	0.3
M5	11.52	0.3
M6	11.63	0.3
M7	11.67	0.3
M8	11.71	0.3
M9	11.76	0.3
M10	11.83	0.3
M11	11.88	0.3
M12	11.96	0.3
M13	12.03	0.3
M14	12.11	0.3
M15	12.20	0.3

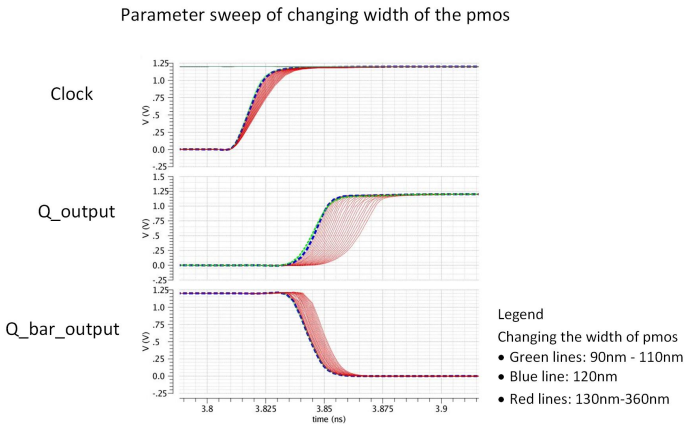

Fig. 22: Parametersweep of changing the width of the pmos when the data is high.

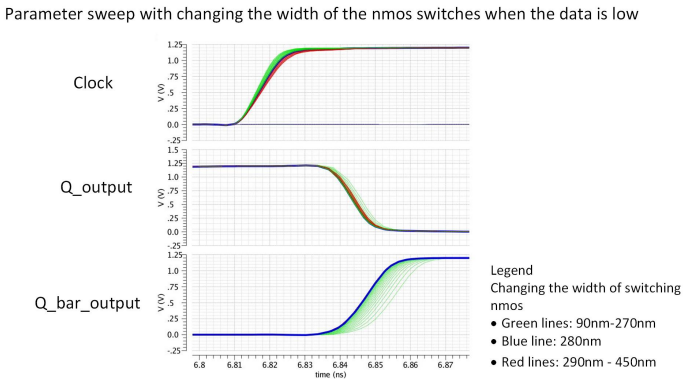

Fig. 23: Parameter sweep of changing the width of the switching nmos when the data is low.

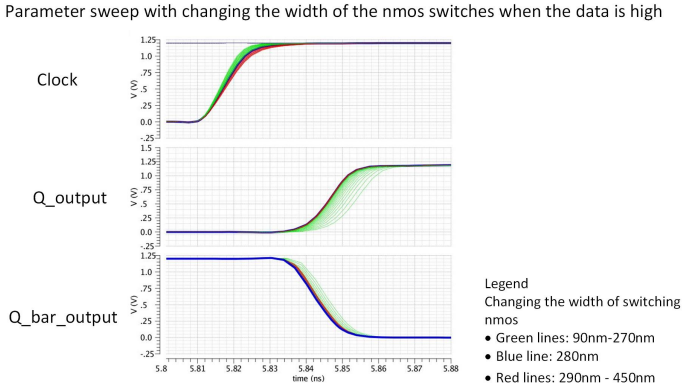

Fig. 24: Parameter sweep of changing the width of the switching nmos when the data is high

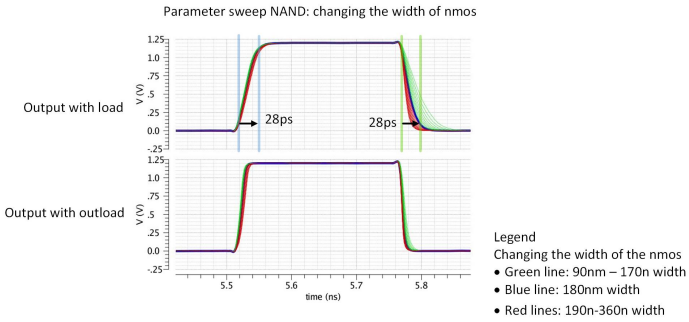

Fig. 25: Parameter sweep of changing the width nmos of the NAND.

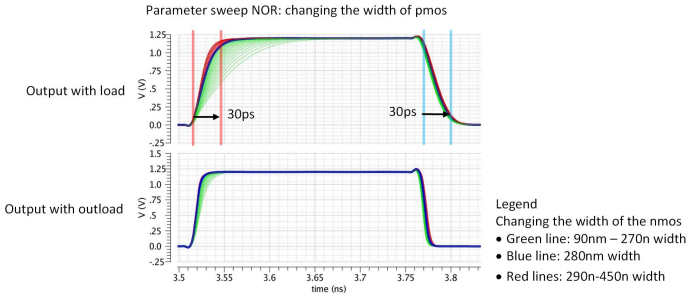

Fig. 26: Parameter sweep of changing the width pmos of the NOR.

TABLE II: This table describes which widths and lengths are used for which PMOS transistors. M1 is the MOSFET which is associated with the lowest current while M15 is associated with the highest current.

PMOS	Width(um)	Length (um)
M1	56.23	0.3
M2	57.25	0.3
M3	57.63	0.3
M4	57.84	0.3
M5	58.04	0.3
M6	58.28	0.3
M7	58.56	0.3
M8	58.87	0.3
M9	59.21	0.3
M10	59.57	0.3
M11	59.95	0.3
M12	60.36	0.3
M13	60.82	0.3
M14	61.31	0.3
M15	61.87	0.3

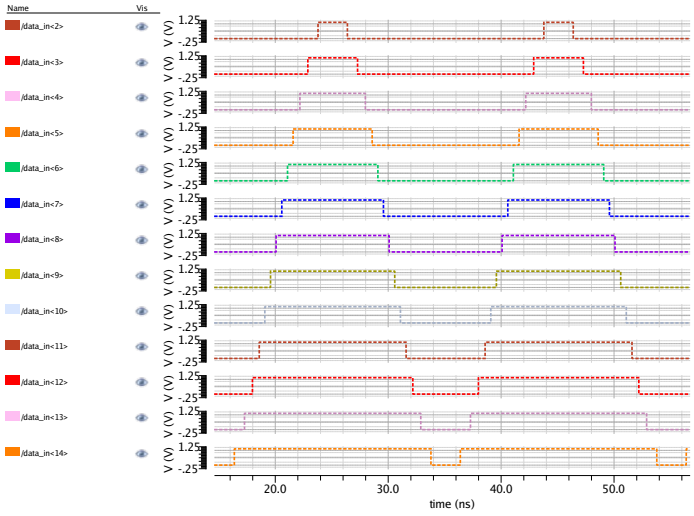

Fig. 27: Thermometer single tone voltage output.

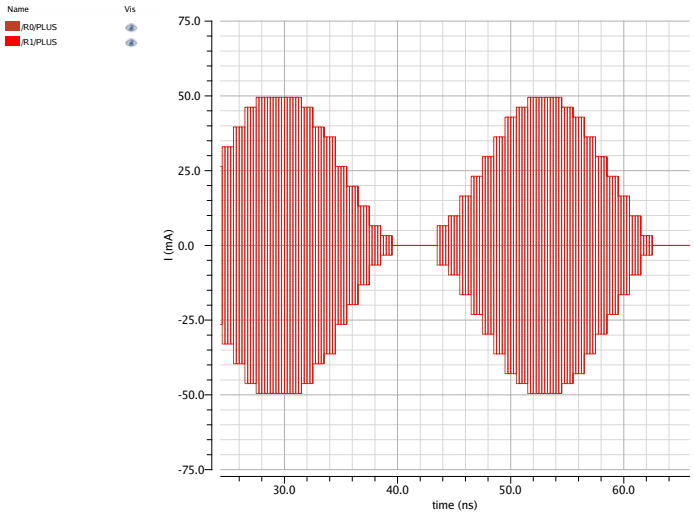

Fig. 28: Output current

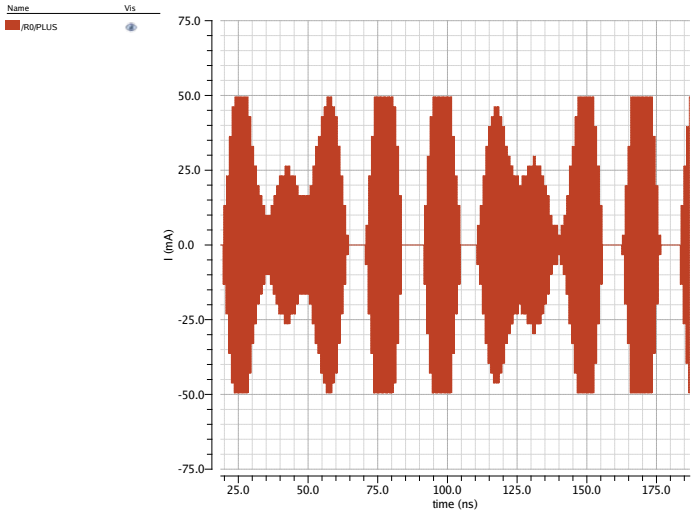

Fig. 29: Two tone output current