Power Mixing DAC

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***Abstract*—This is the abstract**

I. Introduction

For this design there is chosen to create a combined traditional DAC, mixer and power amplifier (PA), because this leads to several advantages. One thing is that it results in a more compact solution. A compact solution allows the system to be faster, because there are less parasitic capacitances between the structures. Also the need of matching to 50 ohm between these structures becomes superfluous. Using such a combined system solution has a disadvantage that it is hard to generate high power, this generates heat which can damage the transistors. Moreover the use of large capacitors or inductors is not possible, because these require too much space to create in silicon. Normally they are placed on the PCB.

Such a solution could be useful for several systems. Mainly for systems that require high speed, low power or lack of sufficient available space for a PCB. One example for such a system is a mobile phone.

II. Hardware module

- System specs

o 2 GHz carrier LO

o IMD3 < 30 dBc

o SFDR ?

o Sensitivity

o Noise floor

o Output power 20.97dBm

o Output current 50mA

o Output voltage swing

o

- Unary coding

o 4 > 16 bit

- 2 directions of dac

o Propotional to input level

- Level shifter

- 2 direction amplifier

III. System Components

A. Digital front end

The digital front end consist of two parts, D flip flop and NAND/NOR gate. The D flip flop will synchronise the incoming date and the NAND/NOR gate will modulate the signal with the local oscillator.This signal will go to the level shifter. The two parts will be described in this paragraph.

1) D flip flop: A D flip flop will be used to synchronise the incoming thermometer coded data and to ensure that the output pmos and nmos switch at the same time. There are a couple of challenges that are important to take into account when designing a D flip flop, for example the operation speed and the transition time of the output at the rising clock.

A flip flop can be made in different ways. The two main technologies are in CMOS and CML. The CMOS design is relative less complex in compare to CML, but in CML there are more parameters that can be modified to tune the output. In this project the CMOS design is used, because it is less complexity, single-ended and it can be realised in a short time period. The CMOS circuit of previous group is used in this project, [1] - [2], but the size of the pmos is changed to get a better performance. The schematic is shown in Fig. 1. The D flip flop works with a master-slave principal. The master will set the data on the rising clock and it keeps it until the clock is low. The slave will copy the data of the master and hold the data when the clock is low.

To explain this principal in the schematic, the diagram can be divided into three parts, settle time of the data, master latch and slave latch. In the first part the data will be set when the clock is low. The second part, the master latch will set the settled data and when the clock is high it will set the data to the output of the master latch and the first part will be turned off. The third part, the slave latch will follow the master latch when the clock is high, but when the clock is low the master latch output will be turned off and slave latch will be holding the data.

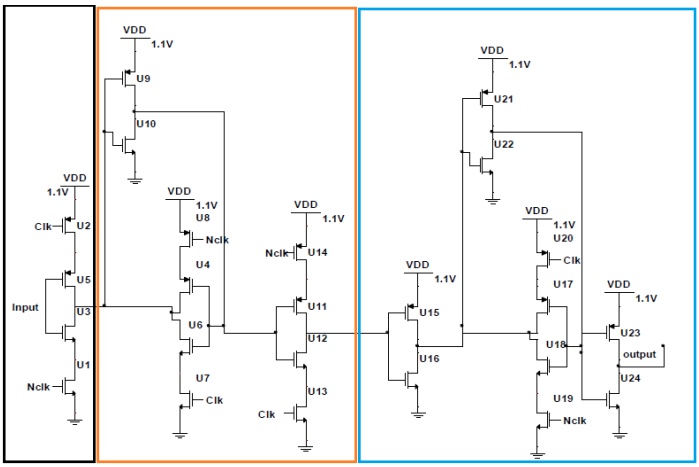


Fig. 1: D flip flop schematic, this schematic will be updated in the next version to define the parts better.

The size of all of the nmos are 50nx90n(length x width). The width of the pmos is determined with the simulation to get smallest delay between the rising clock and the output. The pmos have the following dimensions: 50nx180nm (length

x width). The bulk of the pmos is connected to the power supply (1.1V) and the bulk of the nmos is connected to the ground.

The rise time, fall time, critical point graph will be shown in the next version.

2) NAND/NOR gate: The NAND and NOR will modulate the local oscillator signal (LO) with the data from the D flip flop. The LO signal works with a 2Ghz square wave.

The design of the NAND and NOR will be in the next version of the paper.

B. Levelshifters

To generate sufficië output power thick oxide transitors are used at the output stage. One of the problems with this is that these transistors have a much larger threshold voltage and that they operate at larger supply voltages than the low voltage transistors. Because of this the fast low voltage transitors used in the digital front end and for mixing cannot generate a large enough V_{ON}. Raising the supply voltage to the low voltage transistors in order to increase the output voltage of the mixers will break them. So special care has to be taken when a transition from a low voltage circuit to high voltage thick oxide transistors. To this end a level shifter is designed. In this design special care will be taken to ensure that the voltages accros any low voltage transistor will not exceed 1.1V, so they will not break. On the output side is has to be able to drive relatively large transistors. Also in the on state it must supply a voltage of approximately 2V and in the offstate a voltage smaller than 0.7V.

In [2] a design for the levelshifter was proposed, but they were not able to integrate it with the rest of their design. However, they did show work that it worked in a standalone simulation. The main problem are difficulties with the cadence models of the thick oxide transistors used for simulation. These models show strange behavior and have an unrealistically high threshold voltage of 1.5V. Also a design proposed in [**?**] was considered. But due to the increased complexity combined with our models and its multiple stages, which are bad for timing performance, this design was not used. That design has an propagation delay of roughly 10 ns, which is not acceptable for this paper's design.

The chosen design is a modified version of the one proposed in [2] and is shown in Fig. 2. The inputs are connected to the gates of the low voltage transistors M5 and M6 and have an input range of 0V(off) to 1.1V(on). For correct operation VIN and $\overline{\text{VIN}}$ must be each other's logical inverse. VBIAS is set to ??V and is connected to the gates of M3 and M4. These transistors protect M5 and M6 from the high supply voltage. M1 and M2 provide an positive feed back loop, which makes the circuit function. Its operation is explained using a low to high transition, so initially VIN is 0V, $\overline{\text{VIN}}$ is 1.1V, VOUT is on its off value and $\overline{\text{VOUT}}$ is 2V. In this situation only the right branch is conducting current, because $\overline{\text{VIN}}$ is high and since there is no current in the left branch $\overline{\text{VOUT}}$ is low. When VIN transitions to a high state, it starts conducting current, forcing VM5 to go a bit higher, as well as $\overline{\text{VOUT}}$. Because $\overline{\text{VOUT}}$ increases, the current through the right branch decreases as well as VOUT. The decreased VOUT makes the left branch conduct more current and $\overline{\text{VOUT}}$ go higher. Due to this postive feedback loop VOUT will go to VDD.

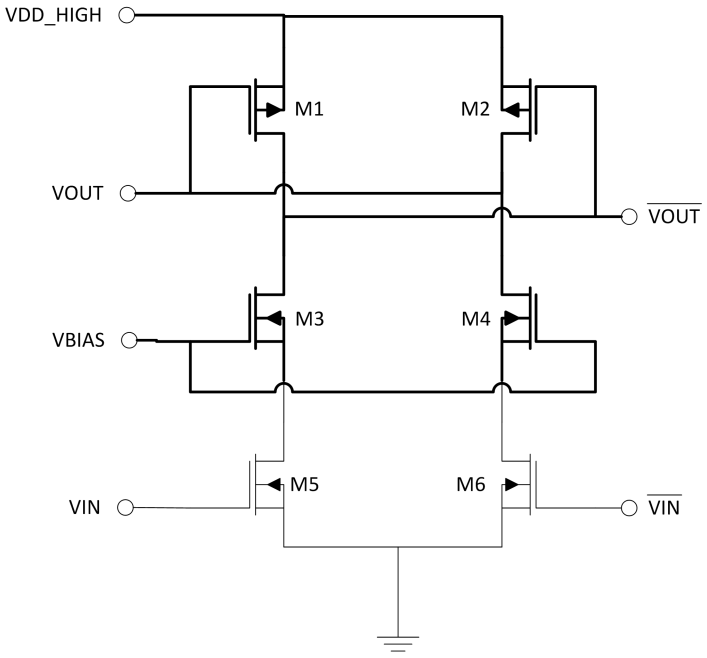


Fig. 2: Schematics of the levelshifter, thick wires indicate a high voltage regime and thing the low voltage transistors

Early simulation results are shown in Fig. 3. It shows that the circuit should be able to function. However in this simulation it is till far to slow with a rise time of about 200 ps, while it is not loaded by the output stage. In the final implementation it should operate at a frequency of 2 GHz, which means that it should be able to transition from low to high and back every 500 ps. This is still being worked on and an issue for further investigation.

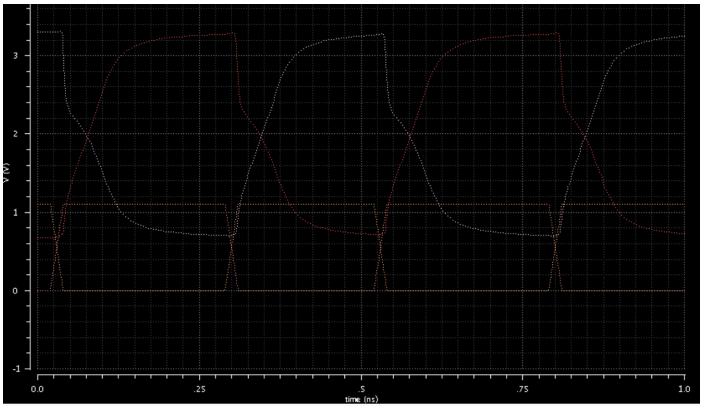


Fig. 3: Early simulation results of the levelshifter

C. Current Sources

The final stage of the power DAC are the current sources. They provide a differential output through a 50Ω resistor. This setup is shown in Fig. 4.

Due to the local oscillator, the current will alternate between $V_{dd} \rightarrow CS1 \rightarrow CS4 \rightarrow GND$ (see Fig.**??**) and $V_{dd} \rightarrow CS3 \rightarrow CS2 \rightarrow GND$ (see Fig.**??**).

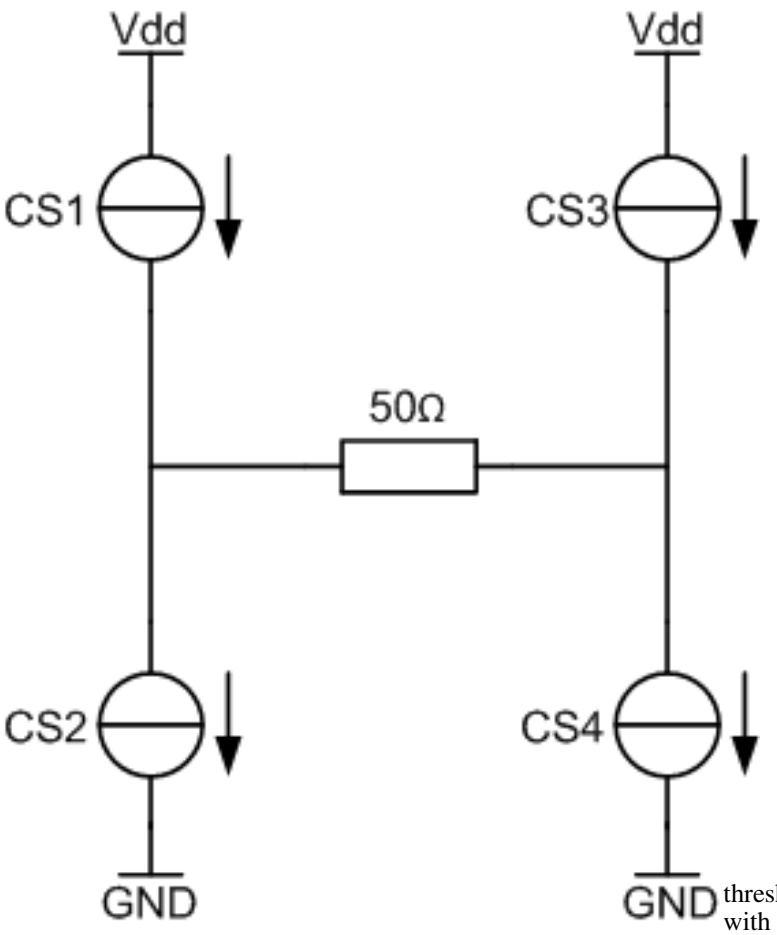
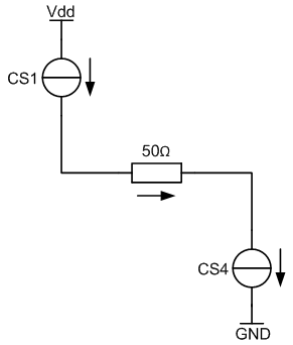
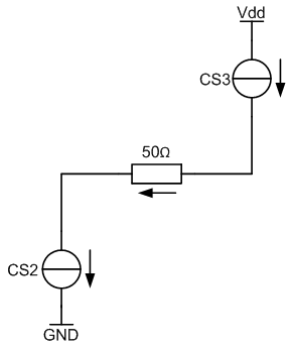


Fig. 4: The final stage of the power DAC: The current sources which will provide the differential output through the resistor.



(a) One current-steered cycle.



(b) The other current-steered cycle.

The first design parameters are the voltage supply and which switching devices are to be used. Because the DAC should be able to produce 50mA through a 50Ω resistor, the maximum voltage drop will be 2.5V. This already cancels out lower voltage supplies such as 1.2V and 2.5V. The resulting options are 3.3V and 5V. Because the stage consist of two current sources, the voltage headroom will be very limited in the 3.3V voltage supply. Therefor a 5V supply will be used as V_{dd}. This, along with the high switching speeds, limits the switching devices to the thick-oxide CMOS technology.

Because thick-oxide CMOS technology has been chosen, the width and length of the CMOS are the only parameters. The most straightforward design method subscribes that the CMOS should always be in saturation so that the current through the CMOS is independent of the drain-source voltage of the CMOS. Therefore Eq.**??** should be valid whatever the drain-source voltage.

$$V_{DS} > V_{TH} + V_{GS}$$

The drain-source voltage of the NMOS is minimal when the current through the resistor is maximal. This results in a minimum drain-source voltage of 1.25V. Because Eq.**??** should be valid independent of the output, the maximum gate-source provided by the level shifter should be 1.95V, because the threshold voltage of the thick-oxide CMOS is 0.7V. Along with Eq.**??**, this would provide the perfect current sources.

$$I_D = \tfrac{1}{2}\mu_n C_{ox}\tfrac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$$

The main disadvantage of this straightforward approach is that this leads to significant speed restrictions. The small overdrive voltage, $V_{DS} - V_{TH}$, will require large width and thus large input capacitances. Due to the large input capacitance the level shifter will not be able to drive the gate-source voltage to the appropriate voltage level. So for the level shifter to work properly, the width of the NMOS should be increased. This will lead to a signal dependent error in the current. This can be seen from the FFT of the total system, the IMD3-level will increase due to this signal-dependence. So the trade-off will be to maximize the width of the NMOS, and therefor also the PMOS, while keeping the level-shifter in its desired working area.

Another aspect which has not been accounted for, is the channel-length modulation. As can be seen from Eq.**??**, the channel length modulation depend on both intrinsic parameters, λ, and extrinsic parameters, V_{DS}. The drain-source voltage is signal dependent. Each active stage of NMOS, will decrease the drain-source voltage. Because the intrinsic parameter λ is inverse proportional to the length of the NMOS, the length of the NMOS can be also be decreased so that the current delivered by the NMOS does not alter for different signals.

The next paper will contain information about the IMD3 - width trade-off and corresponding simulations. It will also contain viable designs.

IV. Results and Analysis

The specified specifications are verified by the use of simulations. While providing a one tone signal, a transient measurement of the output power is simulated. This to verify a correct functioning DAC, that translates the digitals signals as supposed. This holds that the 15 bit digital unary code is translated to an analogue signal with 16 level resolution.

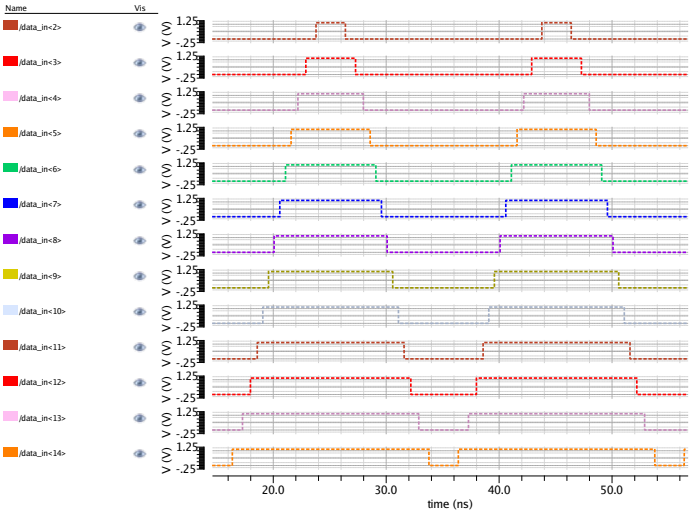


Fig. 6: Thermometer single tone voltage output.

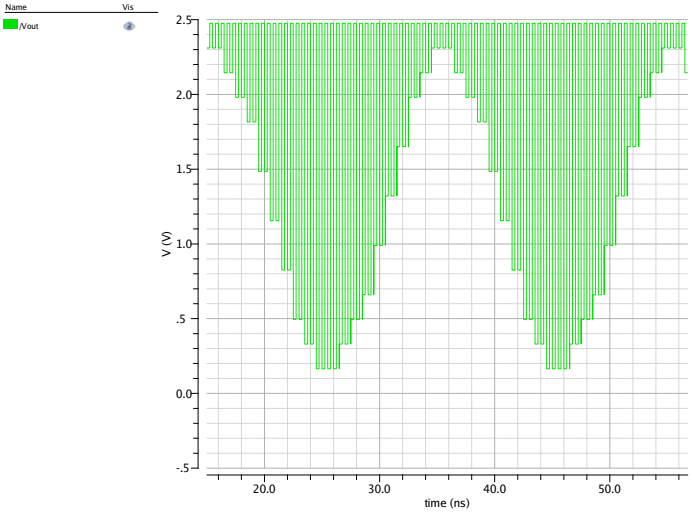


Fig. 7: SoC voltage output.

Next a DFT of the output voltage is simulated to see the spectral content of the one tone model. This to find the power of the harmonic distortion and the spurious-free dynamic range (SFDR). The SFDR describes the power of the fundamental signal to the strongest spurious signal at the output, which is most commonly the second harmonic.

Furthermore a two tone test is simulated, the two tone test is useful test the linearity of the DAC. Non-linear behaviour generates intermodulation products at the output of the DAC. The power of these intermodulation products will examined, especially the third intermodulation product (IM3). Because the IM3 frequencies are very close to the fundamental frequency (at 2f2-f1 and 2f1-f2), it is almost impossible to filter it out of the output signal; therefore, it is better to prevent creating them.

V. Conclusion

This is the conclusion

Acknowlegdements

Dr. G. Radulov

References

[1] G. Radulov, "Course book 5tt50, tu/e," 2014.

[2] H. Li, B.Yin, J. Cao, Y. Zhang, and R. Wang, "Design of a 4-bit power dac achieving the output power of 16.59dbm with imd3<-31dbc up to 5ghz," 2014.