CSCE 692 HW Set 2 - SOLUTIONS

(Chapter 2 and Appendix B)

(100 Points)

Due: NLT 1100 Thursday, 29 January 2019

**Problems :**

**B.1 (a, b, c, d)** [5/5/5/7]

**B.2 (a, b)** [7/7]

**B.5 (a, b, c, d)** [12/12/12/8]

**2.17 (a, b, c)** [5/5/10]

**Instructions:**

* Write your name and a page number on each page
* Please show your work (in some cases, no work = no credit)
* Clearly indicate your answers
* Explain assumptions and provide references (sources) for any additional information you had to research in order to complete any problem.

**Notes:**

1. **Answer all sub questions.**
2. **B.2, To simplify grading, adapt the general format of Fig B.30.**
3. **B.5, Problem Modification: Write buffer eliminates stalls for 97% of writes.**
4. **CACTI,** 
   1. **Use CACTI inputs from handout**
   2. **Let assumed CPU cycle time be random cycle time (ps) for each case.**

B.1 [5/5/5/7] <B.1> You are trying to appreciate how important the principle of locality is in justifying the use of a cache memory, so you experiment with a computer having an L1 data cache and a main memory (you exclusively focus on data accesses). The latencies (in CPU cycles) of the different kinds of accesses are as follows: cache hit, 1 cycle; cache miss, 110 cycles; main memory access with cache disabled, 105 cycles.

1. [5] <B.1> When you run a program with an overall miss rate of 3%, what will the average memory access time (in CPU cycles) be?

1. [5] <B.1> Next, you run a program specifically designed to produce completely random data addresses with no locality. Toward that end, you use an array of size 1 GB (all of which fits in the main memory). Accesses to random elements of this array are continuously made (using a uniform random number generator to generate the elements indices). If your data cache size is 64 KB, what will the average memory access time be?

1. [5] <B.1> If you compare the result obtained in part (b) with the main memory access time when the cache is disabled, what can you conclude about the role of locality in justifying the use of cache memory?

1. [7] <B.1> You observed that a cache hit produces a gain of 104 cycles (1 cycle vs. 105), but it produces a loss of 5 cycles in the case of a miss (110 cycles vs. 105). In the general case, we can express these two quantities as G (gain) and L (loss). Using these two quantities (G and L), create a general formula to identify the highest miss rate after which the cache use would be disadvantageous.

B.2 [7/7] For the purpose of this exercise, we assume that we have 512-byte cache with 64-byte blocks. We will also assume that the main memory is 2 KB large. We can regard the memory as an array of 64-byte blocks: M0, M1, ..., M31. Figure B.30 sketches the memory blocks that can reside in different cache blocks if the cache was direct-mapped.

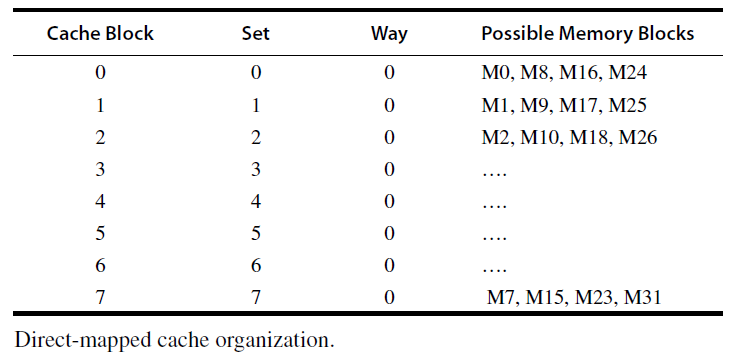


Figure B.30 (from 6th Edition). Memory blocks distributed to direct-mapped cache

1. [7] Show the contents of the table if cache is organized as a fully associative cache.
2. [7] Repeat part (a) with the cache organized as a four-way set associative cache.

B.5 [12/12/12/8] You are building a system around a processor with in-order execution that runs at 1.1 GHz and has a CPI of 1.35 excluding memory accesses. The only instructions that read or write data from memory are loads (20% of all instructions) and stores (10% of all instructions). The memory system for this computer is composed of a split L1 cache that imposes no penalty on hits. Both the I-cache and D-cache are direct mapped and hold 32 KB each. The I-cache has a 2% miss rate and 32-byte blocks, and the D-cache is write-through (no-write allocate) with a 5% read miss rate and 16-byte blocks. There is a write buffer on the D-cache that eliminates stalls for 97% of all writes. The 512 KB write-back (write allocate), unified L2 cache has 64-byte blocks and an access time of 15 ns. It is connected to the L1 cache by a 128-bit data bus that runs at 266 MHz and can transfer one 128-bit word per bus cycle. Of all memory references sent to the L2 cache in this system, 80% are satisfied without going to main memory. Also, 50% of all blocks replaced are dirty. The 128-bit-wide main memory has an access latency of 60 ns, after which any number of bus words may be transferred at the rate of one per cycle on the 128-bit-wide 133 MHz main memory bus.

*A useful tool for solving this type of problem is to extract all of the available information from the problem description. It is possible that not all of the information will be necessary to solve the problem, but having it in summary form makes it easier to think about*

1. [12] What is the average memory access time for instruction accesses?
2. [12] What is the average memory access time for data reads?
3. [12] What is the average memory access time for data writes?
4. [8] What is the overall CPI, including memory accesses?

2.17 [5/5/10] <2.2> The following questions investigate the impact of small and simple caches using CACTI and assume a 32 nm (0.032 μm) technology.

1. [5] <2.2> Compare the access times of 64 KB caches with 64 byte blocks and a single bank. What are the relative access times of two-way and four- way set associative caches in comparison to a direct mapped organization?
2. [5] <2.2> Compare the access times of four-way set associative caches with 64 byte blocks and a single bank. What are the relative access times of 32 KB and 64 KB caches in comparison to a 16 KB cache?
3. [10] <2.2> For a 64 KB cache, find the cache associativity between 1 and 8 with the lowest average memory access time given that misses per instruction for a certain workload suite is 0.00664 for direct mapped, 0.00366 for two- way set associative, 0.000987 for four-way set associative, and 0.000266 for eight-way set associative cache. Overall, there are 0.3 data references per instruction. Assume cache misses take 10 ns in all models. To calculate the hit time in cycles, assume for each associativity, the CPU will be built to have a cycle time equal to the random cycle time found using CACTI, which corresponds to the maximum frequency that cache configuration can operate without any bubbles in the pipeline.