CSCE 692 HW Lab 1 - Cacti Cache Simulator

(100 Points)

Due: NLT 0800 Thursday, 10 January 2019

**Lab Overview:**

Compile CACTI 6.5 on a Linux machine. Use the resulting program, together with the configuration file, to make comparisons of cache performance under various circumstances.

**Assignment tasks:**

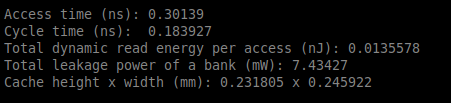
1. [15] Compile CACTI 6.5 (or run provided binary and determine it works on your machine)

**Command to run Cacti:**

./cacti -infile ../Labs/Lab1\_assoc1.cfg

- Note: Lab1\_assoc1.cfg is simply the desired configuration file, and a different configuration was used for each test, changing the specified parameters.

**Sample output:**



1. Compare access times in Lab1\_initial\_configuration\_input.cfg as you change “associativity”
   1. [5] Access time for associativity 1 = 301.39ps, cycle time = 183.927ps
   2. [5] Access time for associativity 4 = 344.226ps, cycle time = 240.763ps
   3. [5] Access time for associativity 8 = 561.563ps, cycle time = 149.119ps
   4. [5] Access time for associativity 16 = 799.303ps, cycle time = 159.446ps

As shown above, the access time increases steadily as associativity increases, while the cycle time fluctuates around roughly the same point.

1. Compare access times across cache sizes (return to associativity = 1)
   1. [5] Access time for 32 KB cache = 387.672ps, cycle time = 183.927ps
   2. [5] Access time for 128 KB cache = 731.590ps, cycle time = 183.927ps
   3. [5] Access time for 1MB KB cache = 1,705.250ps, cycle time = 127.245ps

Access time increased significantly as the cache size increased; while the cycle time was the same for both a 32 KB and 128 KB cache, and smaller for a 1 MB cache.

1. Using associativity = 4, and a cache size of 128KB, choose two different (and interesting) parameters to vary in the cache configuration input fil­e. Observe and record the output changes. Offer an explanation as to why the varying input would cause the varying output.
   1. [5] Parameter one input change:

Increased bus width from 256 to 512 bits.

* 1. [5] Parameter one output change:

Access time: 778.293ps to 742.437ps

Cycle time: 181.293ps to 236.202ps

* 1. [15] Explanation

The access time decreased because the increased bus width allows a higher throughput on the bus. However, the cycle time increased because more work is done per cycle.

* 1. [5] Parameter two input change:

Shifted the block size from 64 bytes to 32 bytes

* 1. [5] Parameter two output change:

Access time: from 778.293ps to 871.888ps

Cycle time: no change: 181.293 ps

* 1. [15] Explanation

By halving the block size on a same-sized cache, with associativity = 1, the number of blocks doubles. However, some of the spatial locality gained from larger blocks is lost. Thus, there might be an increase in the miss rate to the cache, causing the access time to increase.