CSCE 587 Microprocessor Design and Synthesis

Homework 2 – Functional HDL Simulation & Implementation

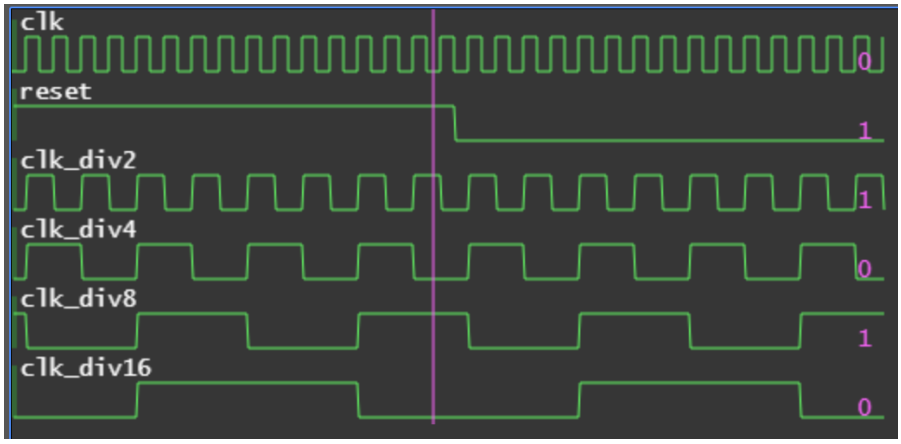
Assignment (200): No written report is required.

Perform the following tasks and submit homework to doug@sidechannel.net. Zip all files into a single file named <lastname>-hw02.zip. Strive to keep final zip file as small as possible.

There are three major parts to this homework, 1) simulating the Verilog-based clock_divider module, 2) simulating the Verilog-based hvsync_generator module used to provide the data and signals needed to drive an old style CRT and 3) redesign the hvsync_generator circuit to output VGA compatible signals given an input clock rate of 25.175MHz (you do not need to implement on the SOCKit boards!).

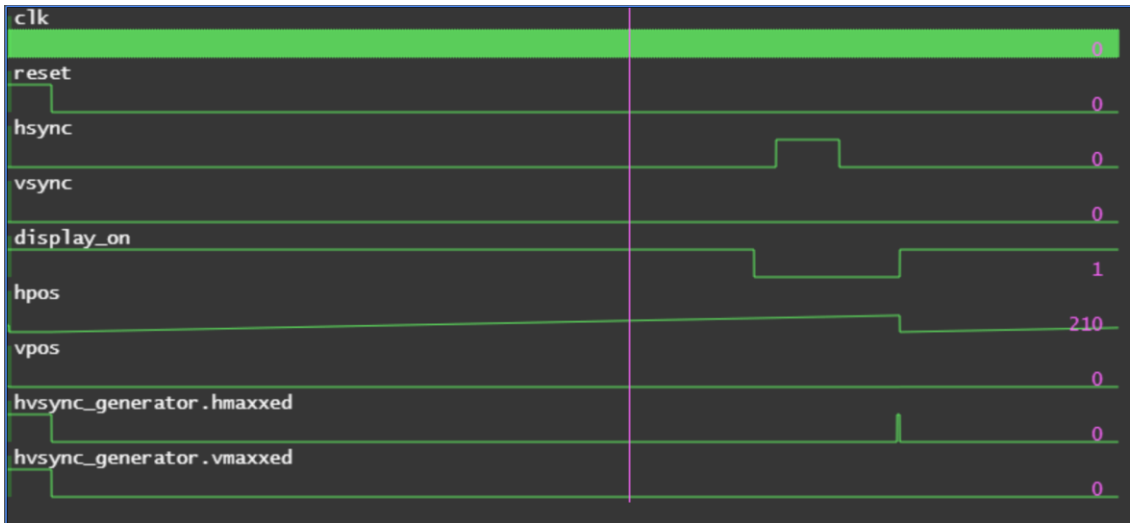
Note: When creating waveforms for simulation, set the "end time" first!

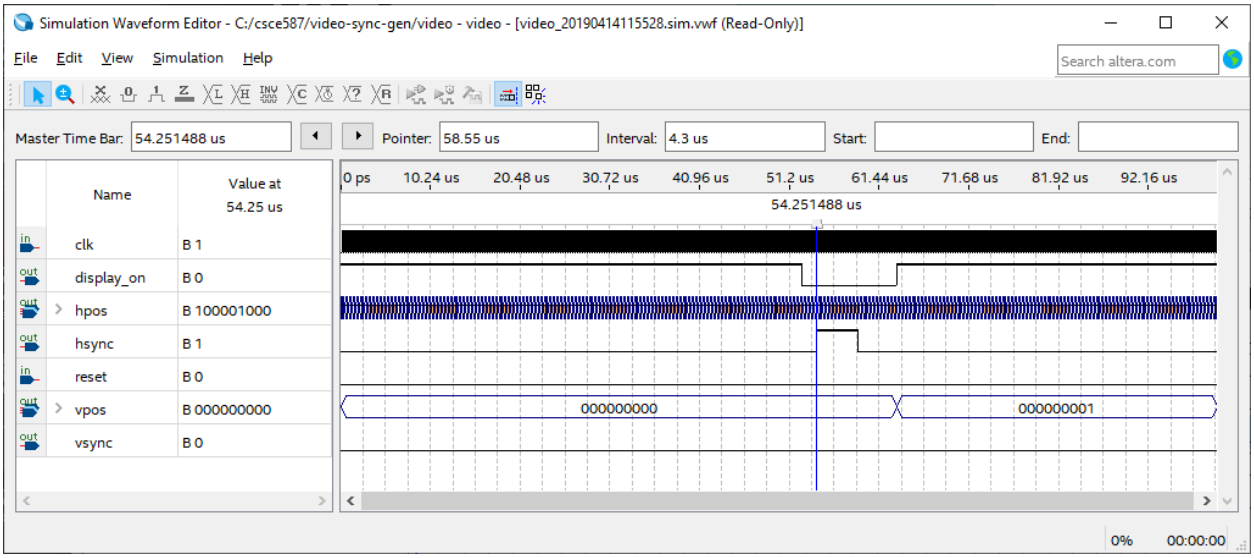
1. Copy/paste the Verilog clock_divider module from the 8-bit workshop website into a Quartus project. Create a functional simulation that stimulates the generator with a clock source (with the same frequency as run by the website emulator) and view the resulting waveform. Document your effort by providing an annotated screenshot(s) of the output waveforms. Provide a written document that describes the frequency of your clock source (and why), and well as a pic of the output signals (i.e., clk_div2, clk_div4, clk_div8, counter, etc.) much like was is shown below.



2. Copy/paste the Verilog hvsync_generator module from the 8-bit workshop website into a Quartus project. Create a functional simulation that stimulates the generator with a clock source (at the appropriate frequency) and view the resulting waveform. Document your effort by providing an annotated screenshot(s) of the output waveforms. Provide a written document that describes the frequency of you clock

source (and why), and well as a pic of a horizontal sync pulse much like what is shown below (akin to Figure 9.3) – don't be concerned with internal module signals such as hmaxxed and vmaxxed. (Make sure to show a vertical sync pulse transition that will be "filled" with lots of horizontal sync pulses!)





3. Given VGA signal specifications (and accompanying VHDL source code that generates those signals, vga_sync.vhd), redesign the hvsync_generator (***with the exact same interface***) circuit to produce those signals given a clock source of 25.175MHz – assume reset is forced to low. Provide a written document that describes the new design as well as a pic of a horizontal sync pulse much like what is shown above (using simulation). (You ***do not*** need to implement this circuit on your FPGA board!)