CSCE 587 Microprocessor Design and Synthesis

Homework 1 – SoCKit, Quartus and HDL Introduction

Assignment (100): No written report is required.

Perform the following tasks and submit homework to doug@sidechannel.net. Zip all files into a single file named <lastname>-hw01.zip. Strive to keep final zip file as small as possible. (Don't send multi-MB pics – shrink/reduce size to something reasonable.)

1. Read SoCKit Getting Started Manual to see how to download and install software.
2. Read/scan SoCKit User's Manual – pay particular attention to pin locations associated with our board!
3. Work through both Quartus tutorials (one is VHDL specific, the other is Verilog). They are nearly identical except for use of either VHDL or Verilog. Skip section 8 (Simulating the Designed Circuit) – we will be using ModelSim for simulation.
4. Implement Quartus design using our board. This means that you will need to correctly assign pin locations mentioned in Table 2 (of Quartus tutorial) with those specified in SoCKit User's Manual (see section 3.6.1 – User Push-buttons, Switches and LED on FPGA).
5. Provide evidence of assignment completion – send me a zip file with project artifacts that include VHDL/Verilog code, SOF file, and a camera picture of it working. Make sure to reduce the size of camera pictures and compress them into jpeg or png, and not include miscellaneous project files. The size of the final zip should be well less than 1MB.