Part 1 - Clock Divider

I simulated the clock divider at a frequency of 4.857 MHz, which was the stated clock frequency in Chapter 9. This equates to the following clock period:

$$\text{Clock Period} = \frac{1}{4.857 \times 10^6} = 205.89ns$$

This produced the below simulation output:

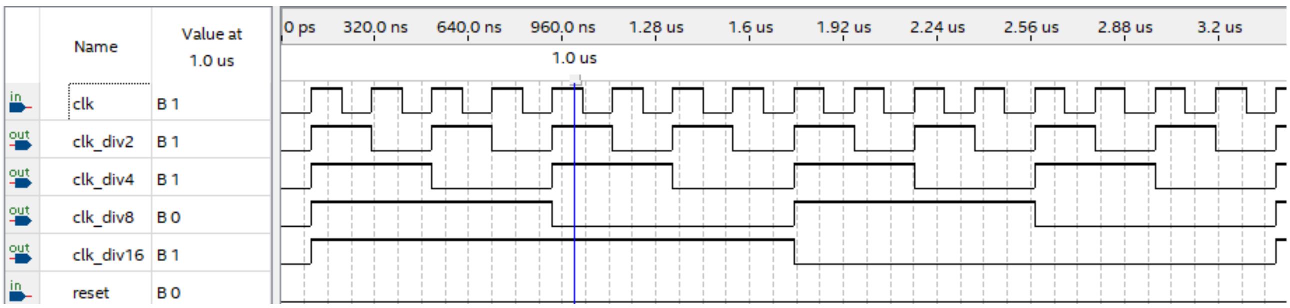

Figure 1: Output waveform of Clock Divider module

Part 2 - HSync Generator

The HSync Generator module was run using the same clock period as the clock divider. There are 309 pixels horizontally, thus, I would expect the simulation to rollover at $t = 309 \cdot 205.89\,ns = 63.620\mu s$.

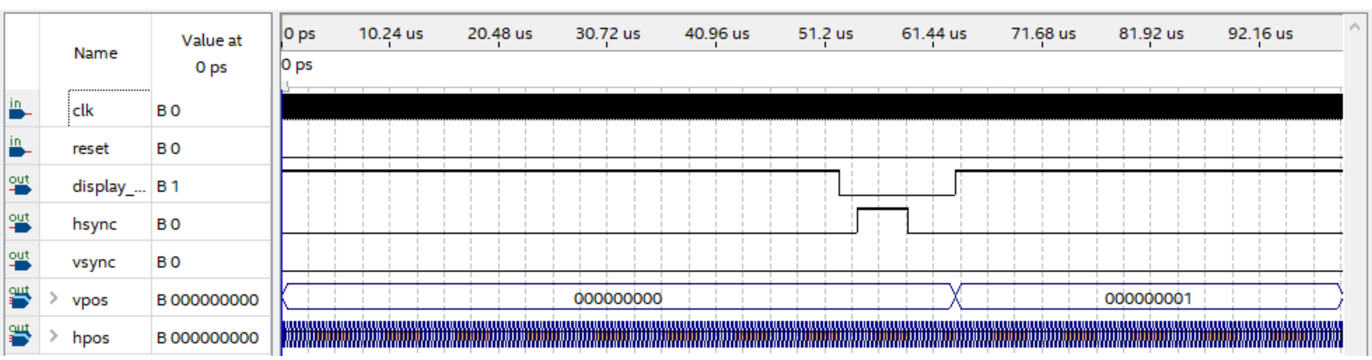

Figure 2: Output waveform of HSync module

As seen above, the second vertical line started at time $t =$

Part 3 - VGA Display

To modify the HSync module to work for a VGA display, I increased the position vectors to 10 bits. I also changed the HSync and VSync timings to match those required for a VGA display, as described in Tables 1 and 2.

Frame	Lines
Visible Area	640
Front Porch	16
Sync Pulse	96
Back Porch	48
Total:	**800**

Table 1: Horizontal Timing

Frame	Lines
Visible Area	480
Front Porch	10
Sync Pulse	2
Back Porch	33
Total:	**525**

Table 2: Vertical Timing

Ths VGA display needs a $25.175MHz$ clock, which gives a clock period of $39.722\,ns$. I would expect a whole line (800 pixels) to take

$$\text{Time per Horizontal Line} = 800 \cdot clock_{period} = 31.778\,\mu s \tag{1}$$

The simulation of the modified module produced the below output waveform:

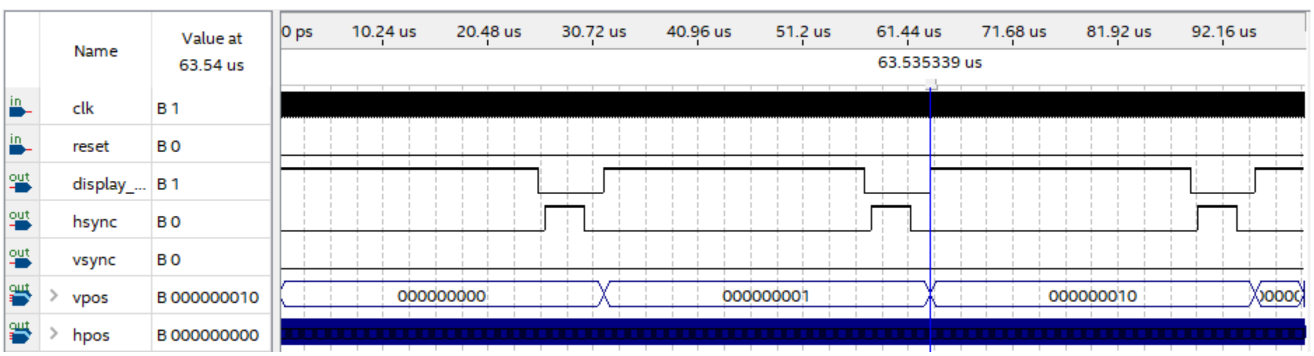

Figure 3: Output waveform of modified HSync module for VGA display

This produced the expected results. The first rollover occurred at $t_1 = 31.757739\mu\,s$, and the second occurred at $t_2 = 63.535339\mu\,s$. This produces a total time per horizontal line of $t = t_2 - t_1 = 31.7776\mu\,s$. This time matches the expected time per horizontal line calculated in Equation 1.