CSCE 587 Microprocessor Design and Synthesis

Homework 2 – Functional HDL Simulation & Implementation

Assignment (200): No written report is required.

Perform the following tasks and submit homework to doug@sidechannel.net. Zip all files into a single file named <lastname>-hw02.zip. Strive to keep final zip file as small as possible.

There are three major parts to this homework, 1) simulating the Verilog-based clock_divider module, 2) simulating the Verilog-based hvsync_generator module used to provide the data and signals needed to drive an old style CRT and 3) implement that same sync circuit on your SOCKit FPGA board with the appropriate clock signal.

1. Copy/paste the Verilog clock_divider module from the 8-bit workshop website into a Quartus project. Create a functional simulation that stimulates the generator with a clock source (with the same frequency as run by the website emulator) and view the resulting waveform. Document your effort by providing an annotated screenshot(s) of the output waveforms. Provide a written document that describes the frequency of you clock source (and why), and well as a pic of the vertical and horizontal sync pulses.
2. Copy/paste the Verilog hvsync_generator module from the 8 bit workshop website into a Quartus project. Create a functional simulation that stimulates the generator with a clock source (at the appropriate frequency) and view the resulting waveform. Document your effort by providing an annotated screenshot(s) of the output waveforms. Provide a written document that describes the frequency of you clock source (and why), and well as a pic of the vertical and horizontal sync pulses.

3. (TDB) This will center creating a clock source for your FPGA logic to use.