



# Open Source ASIC tooling

@matthewvenn

# *chipFlow*

Helping product companies  
make their own chips

<https://www.chipflow.io/>



Learn to design your own  
ASIC and get it fabricated!

<https://zerotoasiccourse.com/>



**YosyshQ**

The home for Yosys and related  
Open Source EDA projects

<https://www.yosyshq.com/>

The background of the slide features a complex, abstract pattern of numerous overlapping rectangles. These rectangles are primarily a vibrant shade of purple, with some darker and lighter variations. They are arranged in a seemingly random, overlapping fashion across the entire slide, creating a sense of depth and texture. The overall effect is modern and dynamic.

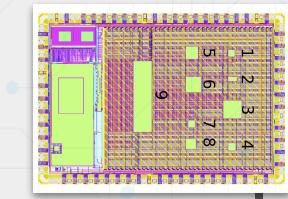
Quick review...

# 2020

June  
Tim Ansell announces Sky130 PDK  
and free shuttle opportunity



November  
Zero to ASIC demo for remoticon



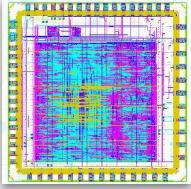
July  
VGA clock GDS with OpenLane

July

December  
MPW1 tapeout with Efabless

# 2021

March  
Strive bringup



**Rapid IC Prototyping Solution**

- Rapid design implementation leveraging a full-carrier chip ASIC (Gated)
- Low-cost MPP shuttle fabrication for the SKY130 open PDK
- No capital equipment requirement
- \$9750 per project
- Includes**
  - Complete design flow based on Specure, Bluebeam, and Cadence
  - Advanced physical implementation for digital designs
  - Support commercial PCB options as well
  - Supports wafer design, tapeout, and evaluation board
  - 200+ user design area
  - 200+ programmable I/O supporting digital and analog
  - >20 package formats, including WLCSP, QFN, QFP, and leadless chip carriers
  - 5 evaluation board assemblies

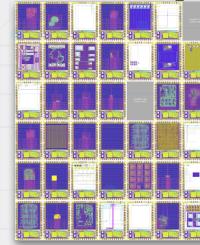
**Schedule based on demand**

- Earliest tapeout: June 15, 2021
- Earliest delivery: July 20, 2021
- Project shuttle capacity:
  - >20 minimum
  - <20 maximum
- \$200 reservation fee (fully refundable if minimum projects not met)

For more information: [jef@efabless.com](mailto:jef@efabless.com)

A diagram illustrating the rapid prototyping solution, showing a central user design area with various sub-blocks and a surrounding infrastructure including tapeout, delivery, and shuttle capacity.

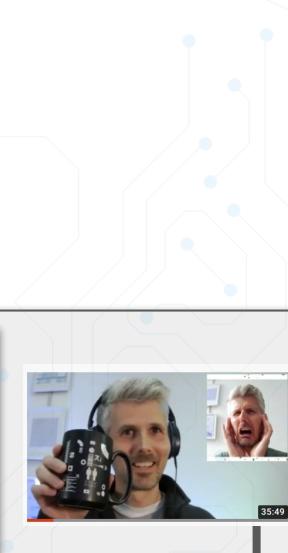
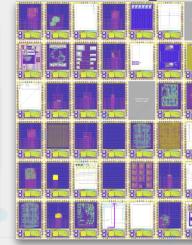
June  
MPW2 tapeout



October  
MPW1 silicon arrived!



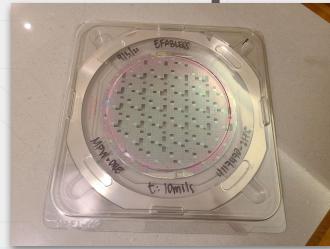
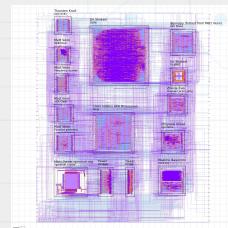
November/December  
MPW3/4 tapeout



May  
Chiplgnite - commercial version

# 2022

Jan/Feb  
MPW1 bringup

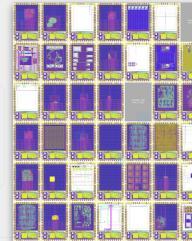


March  
MPW5 tapeout

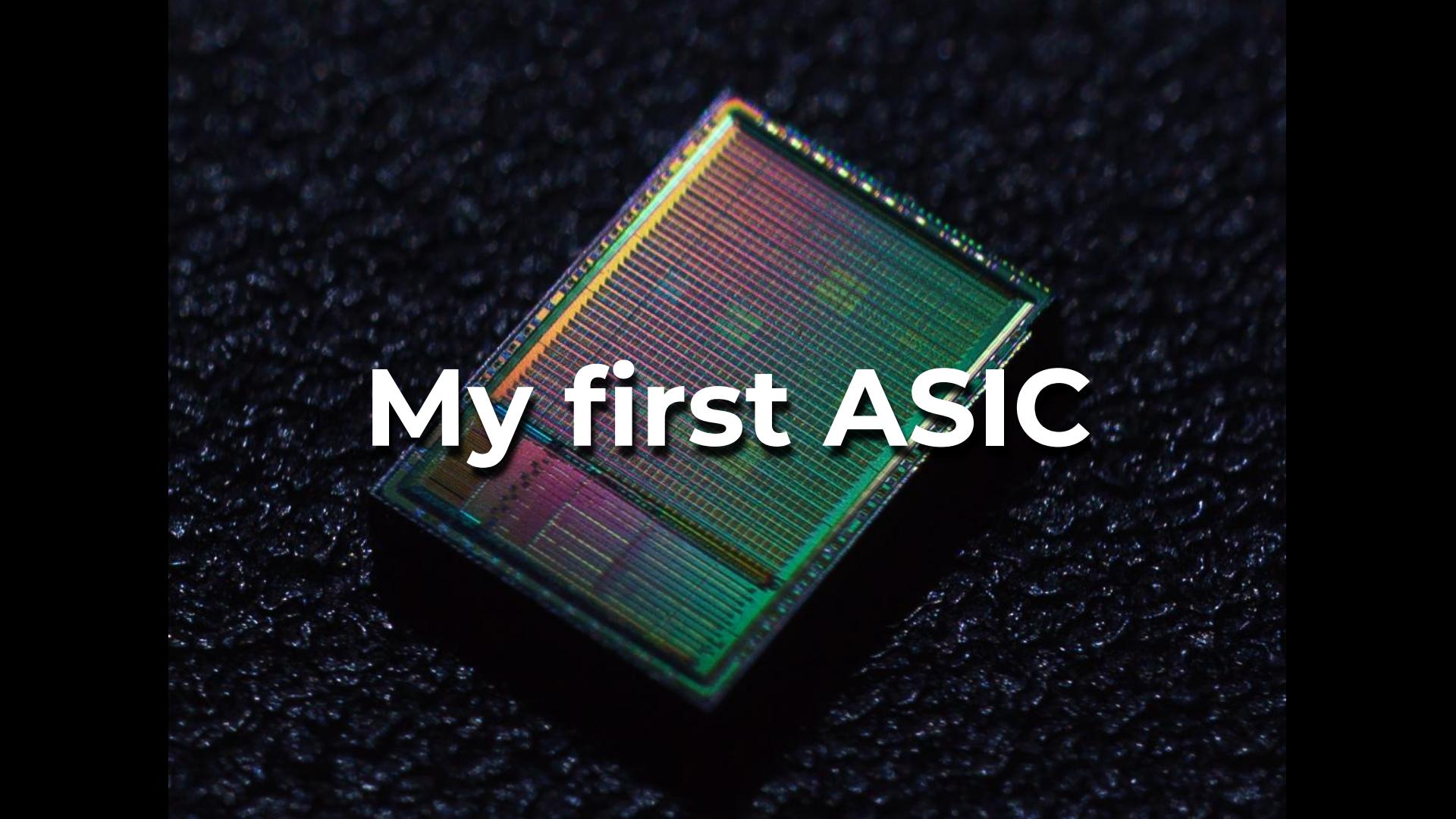
April

MPW2 wafers out of fab

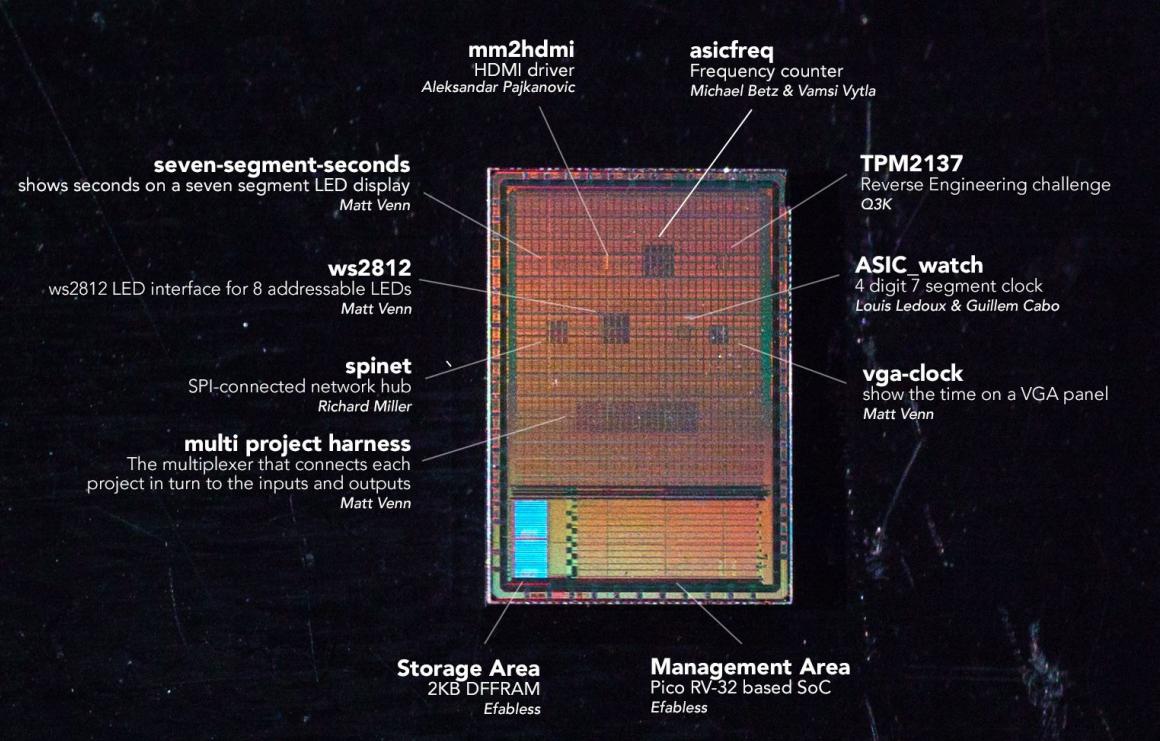
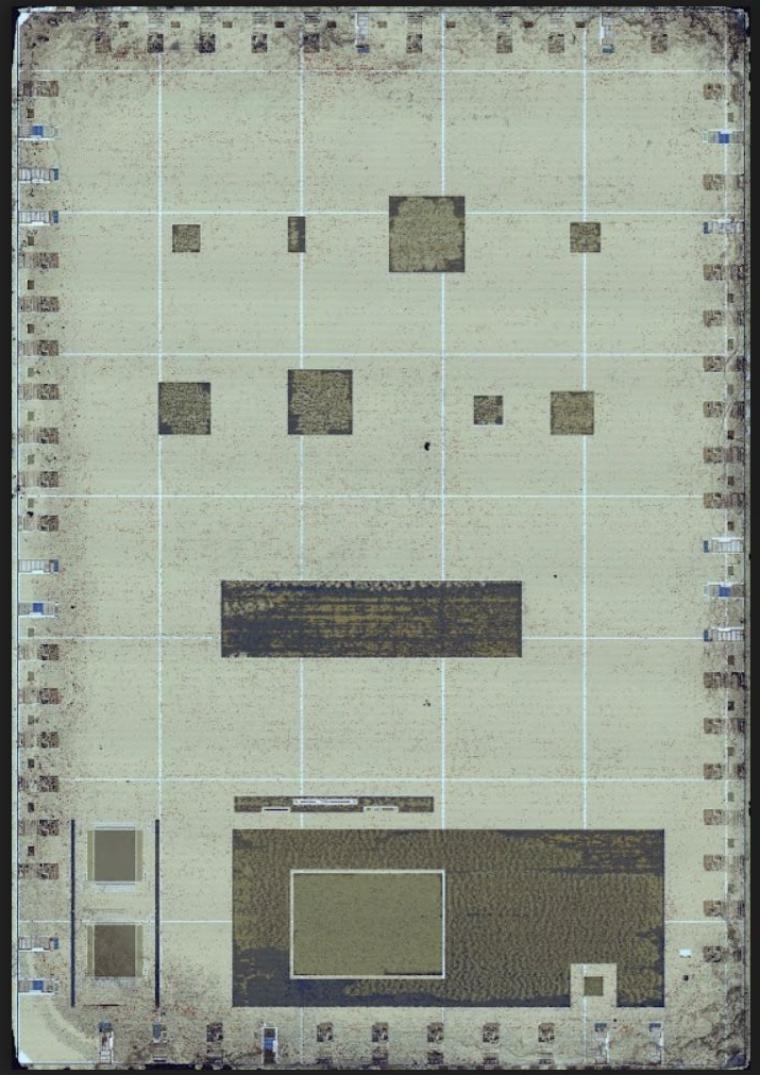
2 more tapeouts, more fabs, PDKs



June  
MPW6 tapeout



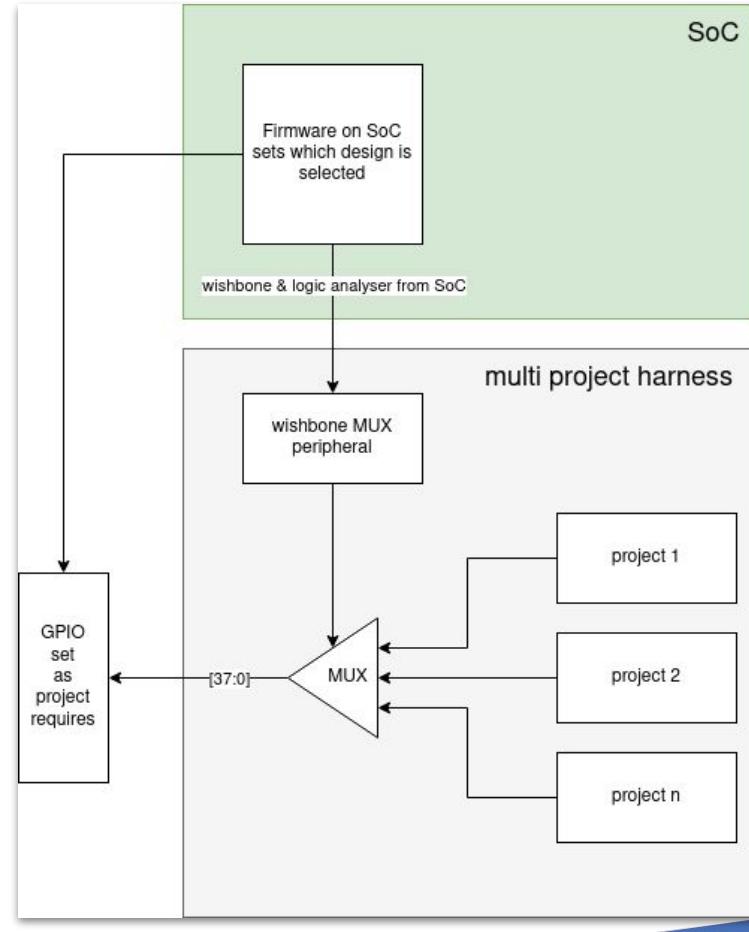
**My first ASIC**

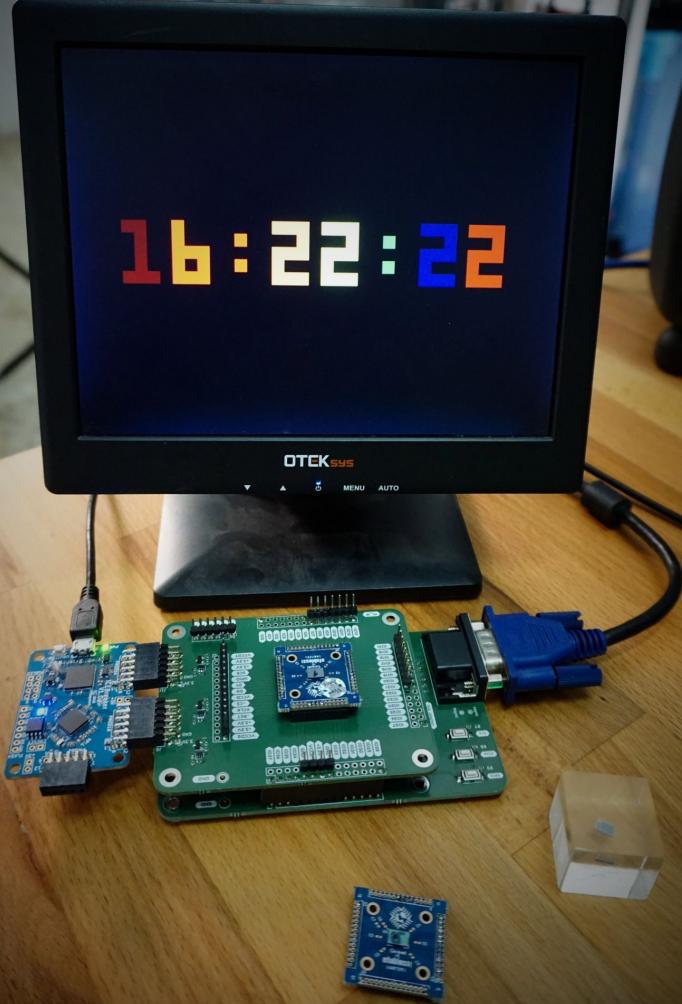


Photos by [Maxiborga](#)  
Die images by <https://www.texplained.com/>  
Lots more info <https://bit.ly/mpw1-samples>

# MPW1

- MUX used
- No build automation 😬
- Ugly implementation
- Used to put 8 designs onto MPW1
- MUX needed to be large to fit all the pins around the edge
- Works!
- More details on harness



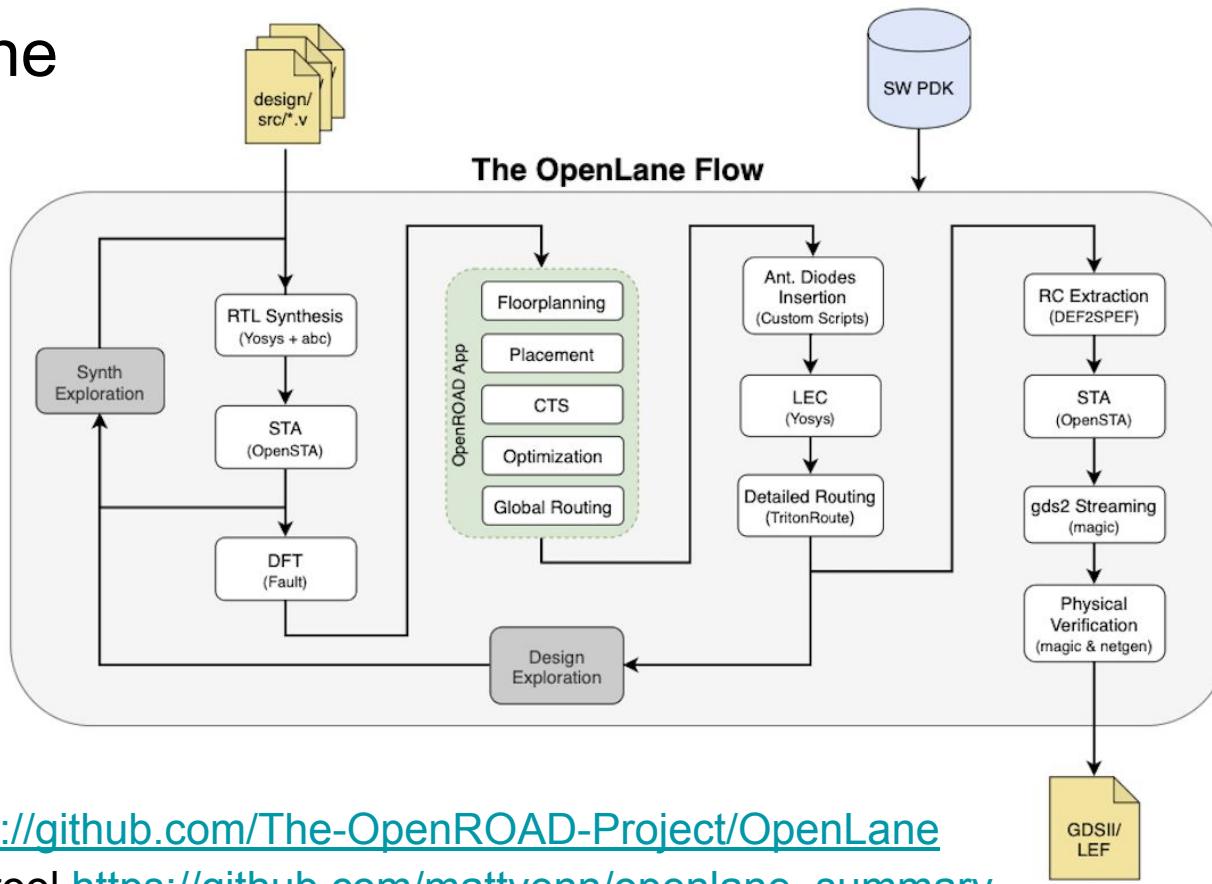


<https://zerotoasiccourse.com/post/mpw1-is-alive/>

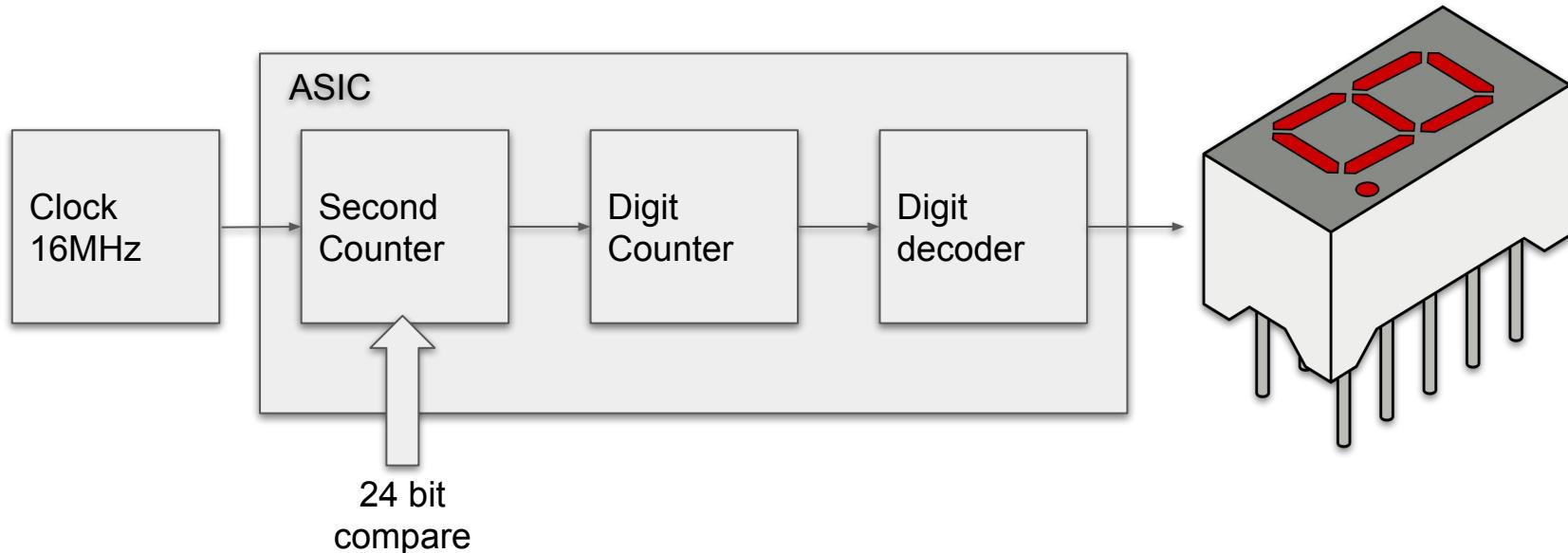


# Demo Time!

# OpenLane

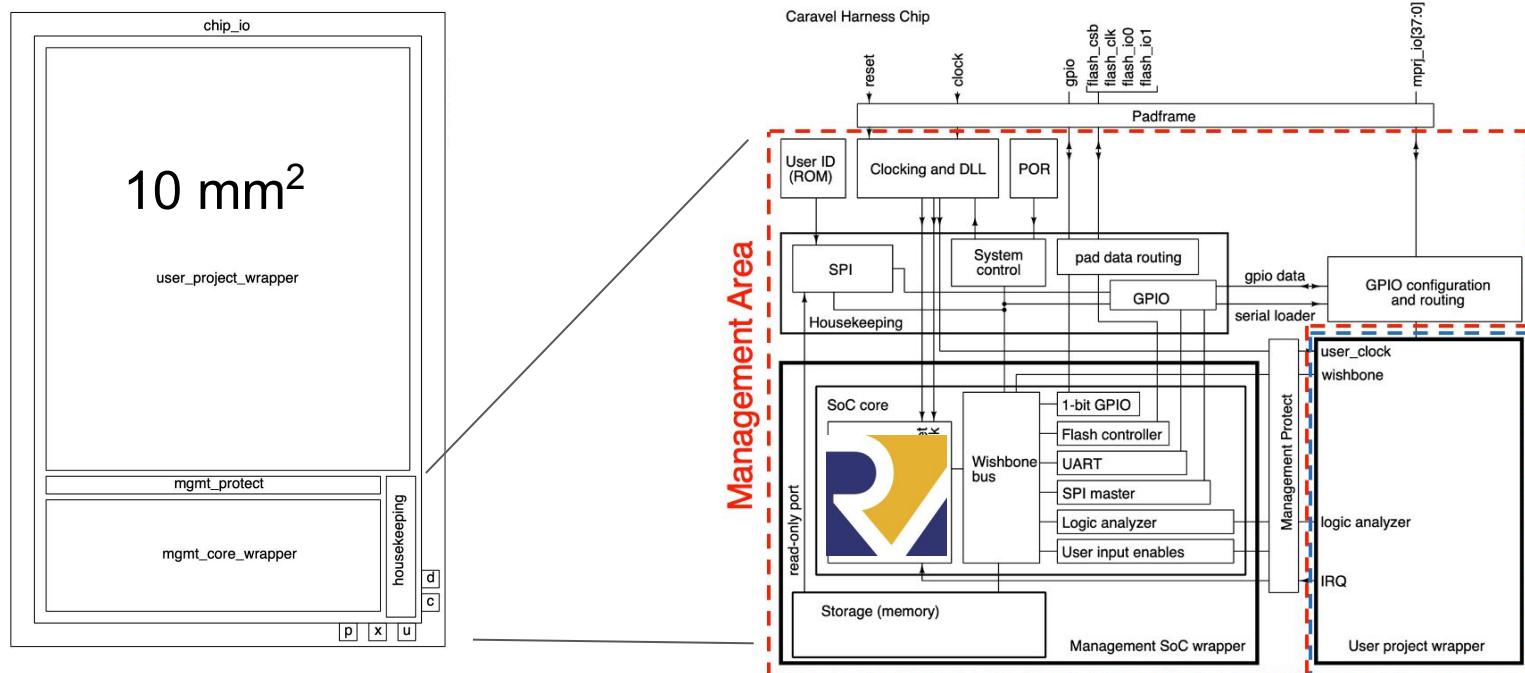


# Demo design - 7 segment seconds



- repo [https://github.com/mattvenn/seven\\_segment\\_seconds](https://github.com/mattvenn/seven_segment_seconds)
- blog post on the working ASIC <https://www.zerotoasiccourse.com/post/mpw1-bringup/>

# Making a submission to Efabless



<https://caravel-harness.readthedocs.io/en/latest/>

# MPW1 silicon problems!

- Issue with clock tree
- Hold time violations not detected
- Fix for MPW2, ChipIgnite
- Fix for tooling for MPW3
- [Blogpost about the problem](#)



**ALL MY  
DESIGNS  
WORKING!**

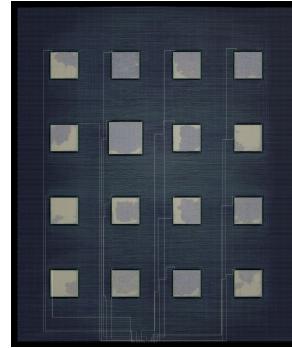


## Zero to ASIC course

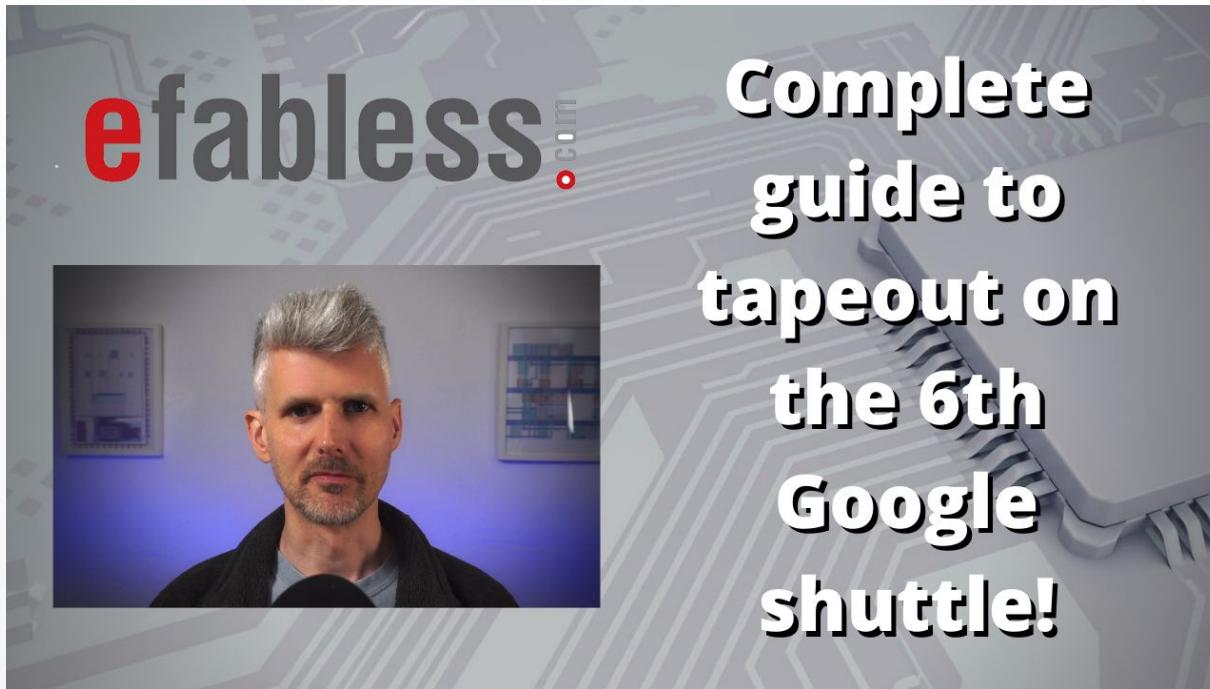
- 200+ people have taken the course
- 40+ designs submitted on all 6 shuttles
- Assumes no prior knowledge

### Feedback

- Matt Venn's Zero To ASIC course is a **real eye-opener** to the possibilities of open source hardware. The course itself is a **tour-de-force overview** of almost all aspects of ASIC development from concept to GDSII. It's also **great fun** and regardless of your background or previous experience, you'll learn a lot and have a great deal of fun doing it. This course has inspired me to take the next step and **submit my own design** to Efabless.



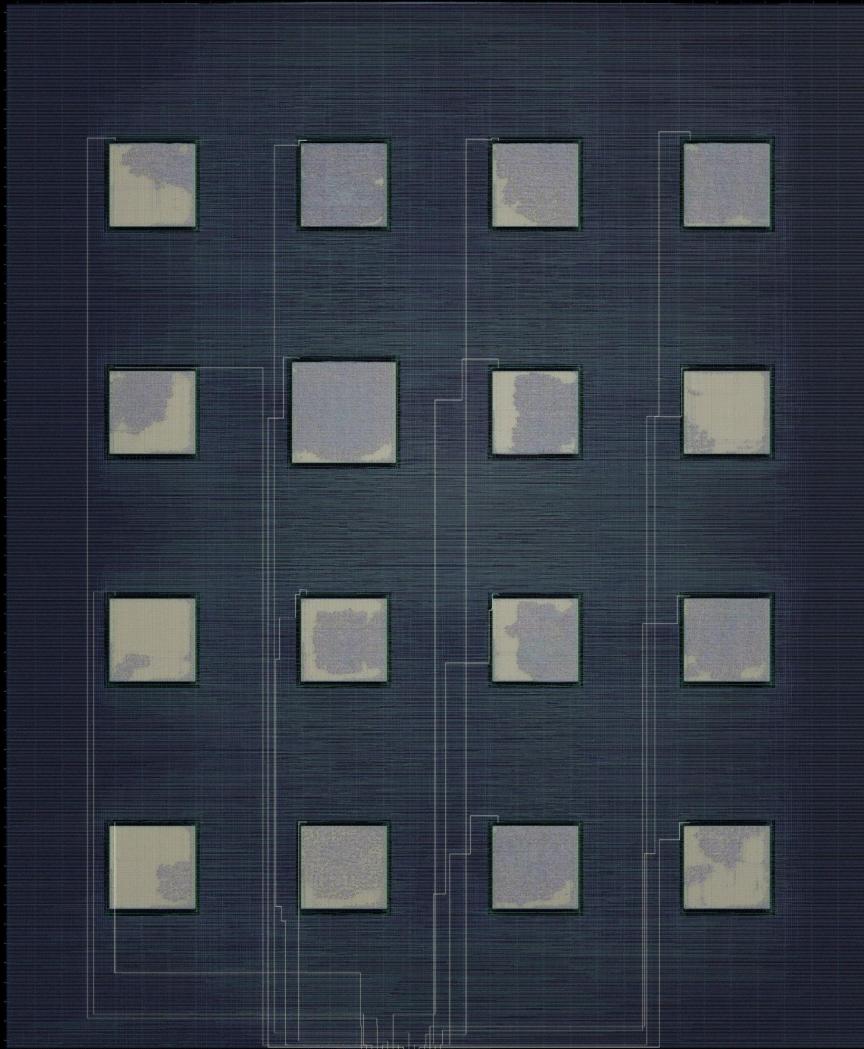
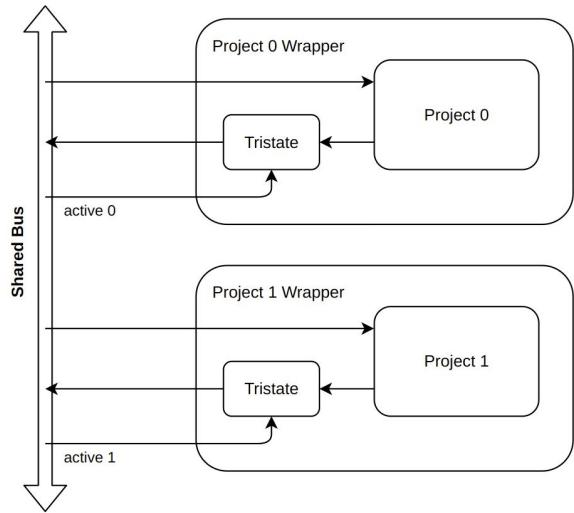
# How to get your CPU onto silicon - demo



[https://www.youtube.com/watch?v=MNuoYz\\_MM-c](https://www.youtube.com/watch?v=MNuoYz_MM-c)

# Multi Project Tools (MPW2-6)

- [https://github.com/mattvenn/multi\\_project\\_tools](https://github.com/mattvenn/multi_project_tools)
- Project outputs isolated with tristate buffers
- Projects are activated by firmware
- Used by my course to submit 75 designs by 40 people across 6 shuttle runs



# Tool overview

# Awesome open source ASIC resources

- [OpenLane](#) - end to end ASIC flow
- [OpenROAD](#) - provides many of the tools in OpenLane
- [Silicon Compiler](#) - end to end ASIC flow
- [Coriolis 2](#) - end to end ASIC flow
- [OSS Cad Suite](#) - lots of open source tools useful for digital design
- [OSFPGA](#) - end to end FPGA flow with open source tools such as Yosys, VTR and VPR
- [VHDL support](#) - with GHDL

## Analog focus

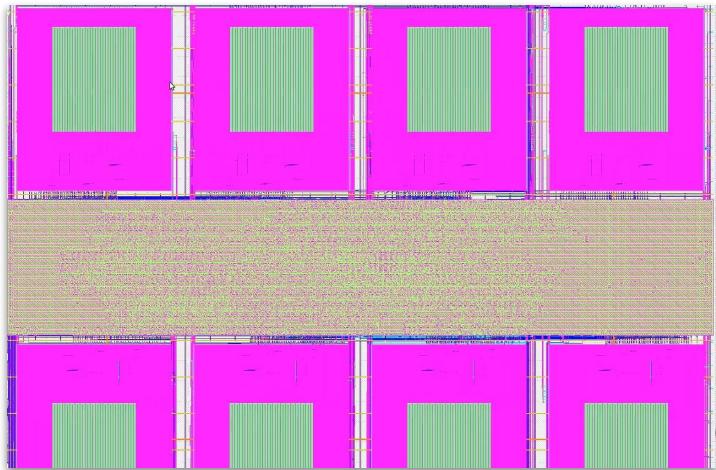
- [Magic](#) - old school, layout drawing tool; [Cheatsheet](#).
- [Klayout](#) - modern style layout drawing tool.
- [Xschem](#) - old school, schematic capture
- [Mosaic](#) - schematic capture (experimental)
- [Ngspice](#) - simulation
- [Xyce](#) - simulation
- [gdsfactory](#) - EDA tool to Layout and simulate circuits

# What's missing?

- RF IC design tools
- Full wave solvers, inductance extraction,
- Other types of analysis - harmonic balance, transient noise, periodic steady state. They exist but we don't know how reliable they are.
- General improvements to physical verification DRC/LVS/PEX, needs to be scalable to new PDKs
- Better mixed-signal co-simulation
- DFT - scan chain insertion
- Power simulation
- Clock distribution & simulation
- Proven Analog IP

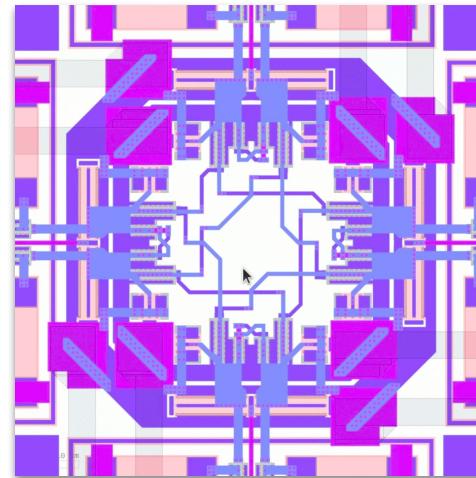
# Example projects

# My picks of MPW1



PyFive USB peripherals

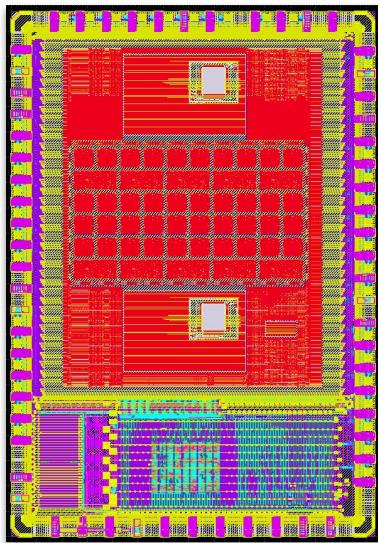
<https://www.zerotoasiccourse.com/post/interview-with-tnt/>



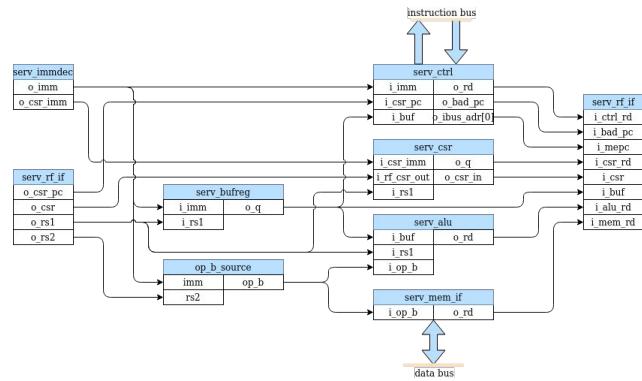
Talking to satellites with silicon

<https://www.zerotoasiccourse.com/post/interview-with-thomas-parry/>

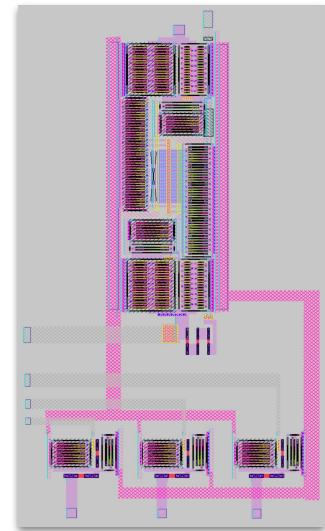
# MPW2



FuseRISC  
<https://platform.efabless.com/projects/134>

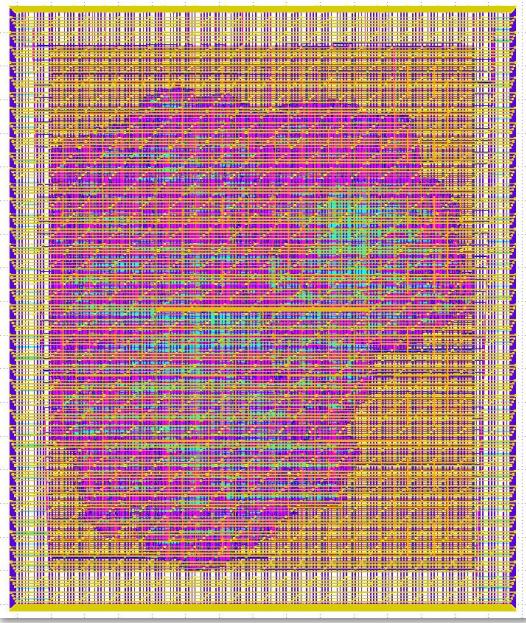


Sub Servient  
<https://platform.efabless.com/projects/104>



Analog Neuron  
<https://platform.efabless.com/projects/204>

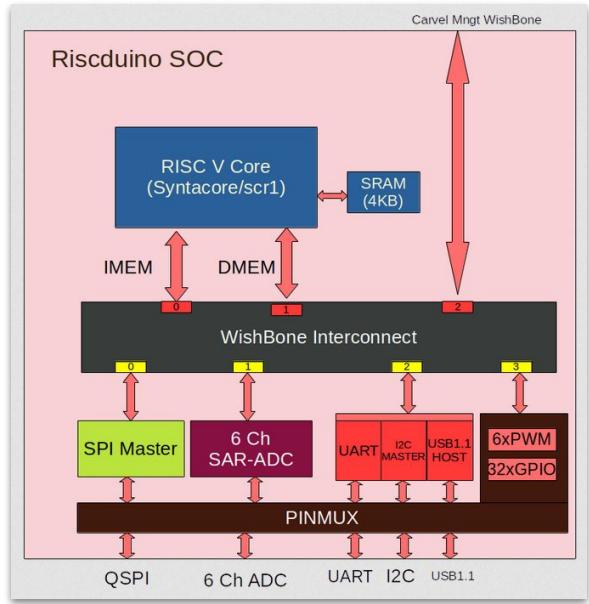
# MPW3



SoC using Coriolis2 for PnR with  
nMigen & Flexcell  
<https://platform.efabless.com/projects/481>

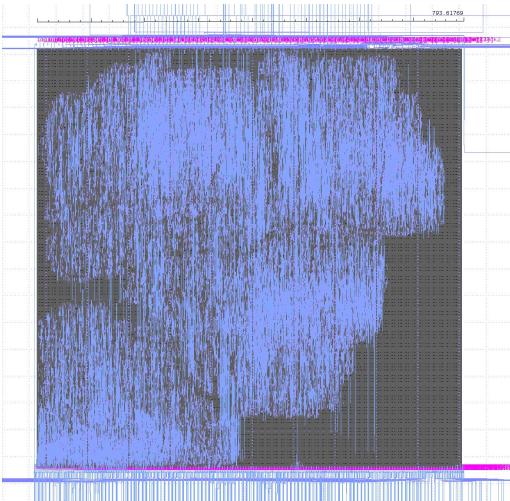


8-bit SAR-ADC  
<https://platform.efabless.com/projects/510>



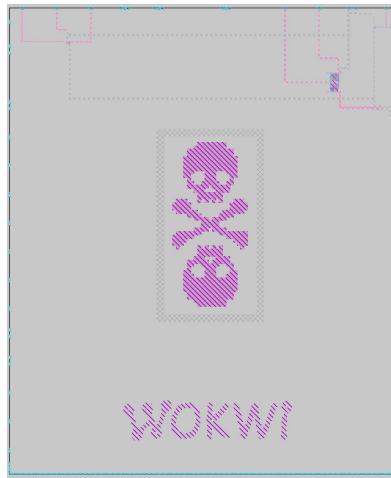
RISC-V Arduino  
<https://platform.efabless.com/projects/385>

# MPW4



Space UART

<https://platform.efabless.com/projects/583>

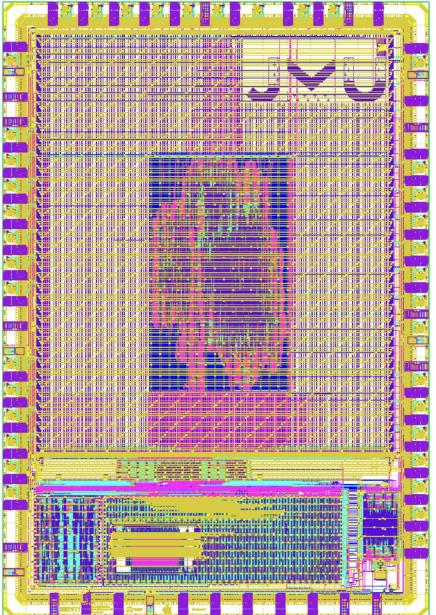


SkullFET  
<https://platform.efabless.com/projects/656>



Sky130 RadTol Test Chip  
<https://platform.efabless.com/projects/637>

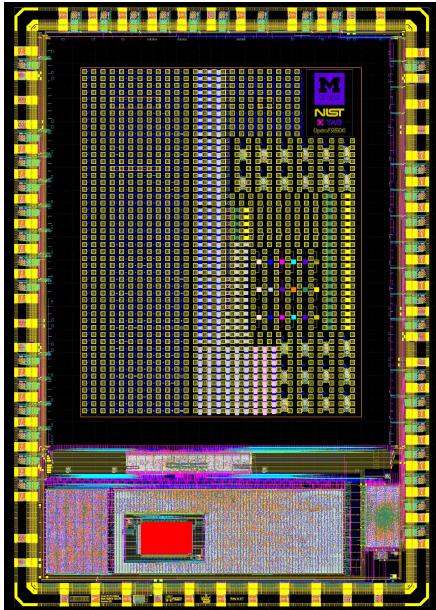
# MPW5



Delta Sigma Audio DAC  
<https://platform.efabless.com/projects/736>

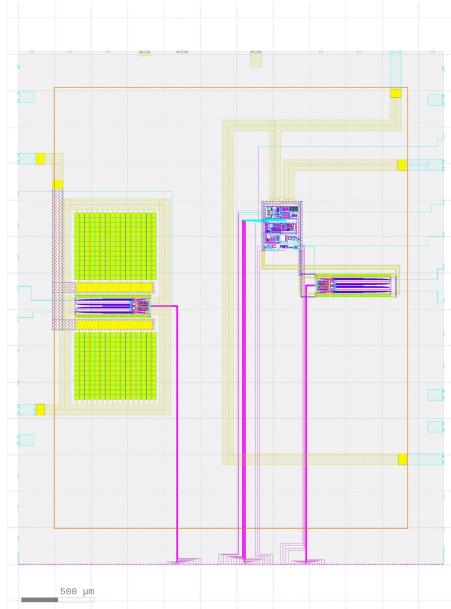


Microwatt  
<https://platform.efabless.com/projects/795>



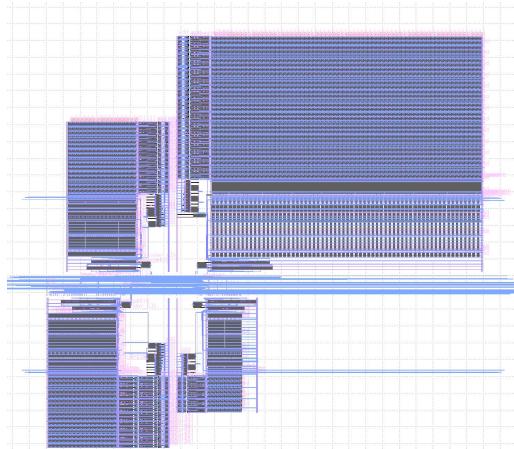
OpenFASOC-cryo-gen  
<https://platform.efabless.com/projects/741>

# MPW6



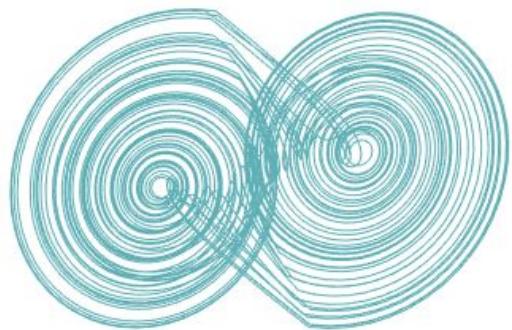
10b SAR-ADC

<https://platform.efabless.com/projects/980>



ReRam array

<https://platform.efabless.com/projects/1089>



RNG MULTI SCROLL CHAOS

<https://platform.efabless.com/projects/973>

# Efabless project browser tool

Screenshot of the Efabless project browser tool interface:

The top navigation bar includes: efabless, Projects, Tools, Marketplace, Community, Company, Login, and Sign Up.

The main search bar shows "Projects" with filters: All Public Projects and Tags.

The search results show 569 results:

- vdp-lite** [public]: VGA sprite generator for the SKY130 Open MPW shuttles. By Dan Rodrigues | <https://github.com/dan-rodrigues>. Tags: MPW-1, SKY130. 2.4k views.
- Softshell** [public]: Multicore processor. By Harrison P. <https://github.com/harrisonp>. Tags: MPW-1, SKY130. 2.4k views.
- Caravel** [public]: Test vehicle for the Sky130 process. By Harrison P. <https://github.com/harrisonp>. Tags: MPW-1, SKY130. 2.4k views.
- Caravel\_sha3\_256...** [public]: SHA-3 256-bit implementation. By Harrison P. <https://github.com/harrisonp>. Tags: MPW-1, SKY130. 2.4k views.

A terminal window at the bottom displays the command: `matt-desktop:2338 [main]: ./efabless_tool.py --list --field summary | grep -i reram`. The output lists several commits related to ReRAM:

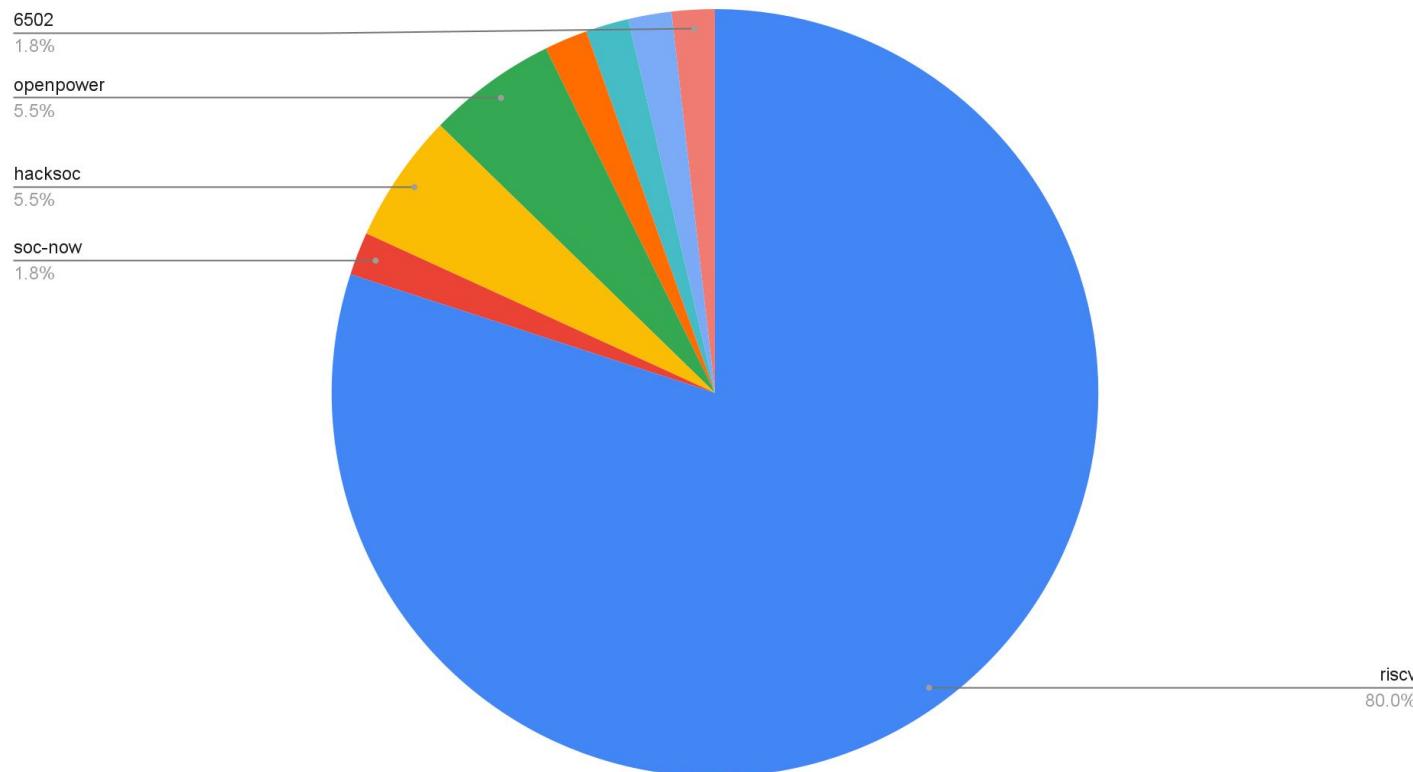
```
669 Copy of of 4tlr reram project
672 Test structure for 1T1R ReRAM
717 Copy of of 4tlr reram project
728 Full ReRAM Memory banks
787 Testing ReRAM structures
836 ReRAM 16x16 array characterisation, incl
997 ReRAM block
```

[https://github.com/mattvenn/efabless\\_project\\_tool](https://github.com/mattvenn/efabless_project_tool)

# RISCV on the shuttles

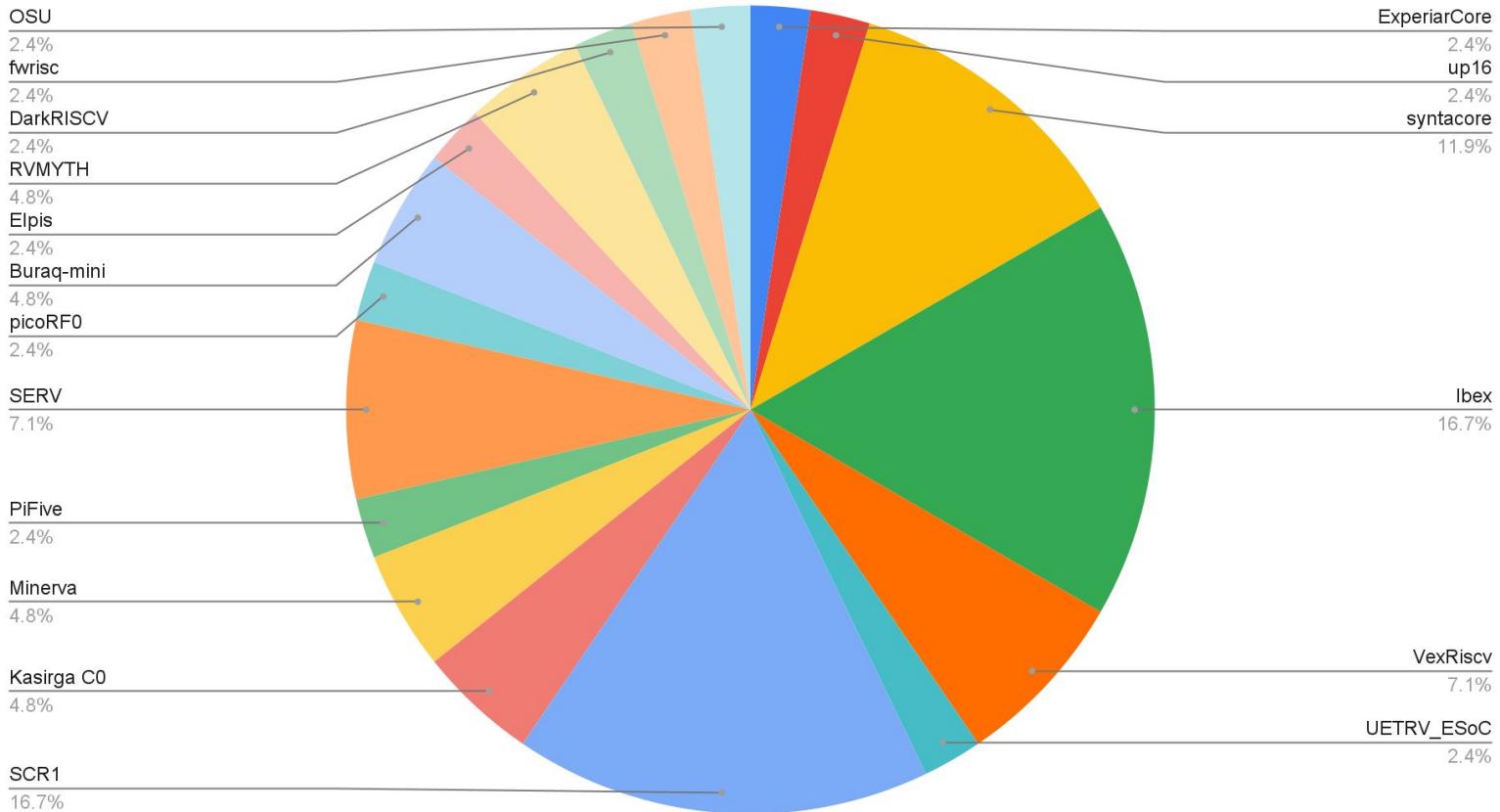
- One ‘free’ RISCV CPU on each chip:  $40 * 6 = 240$ 
  - MPW1 40 PicoRV32
  - MPW2 to 6 200 VexRISC
- Of the 240 applications, 45 were SoC or CPUs
- 37 of which were RISCV variants
- In total **277 RISCV CPUs** across all shuttles so far

45 CPUs were submitted to Google MPW shuttles 1 to 6



[Link to the spreadsheet](#)

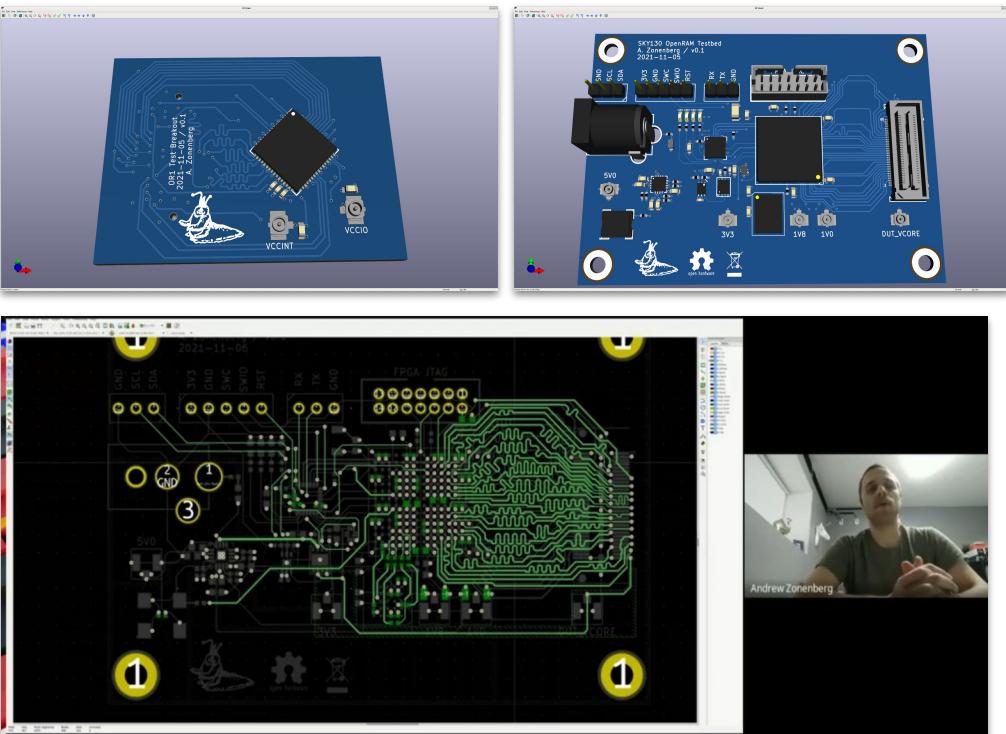
## RISCV by base (excluding PicoRV32)



# Related work

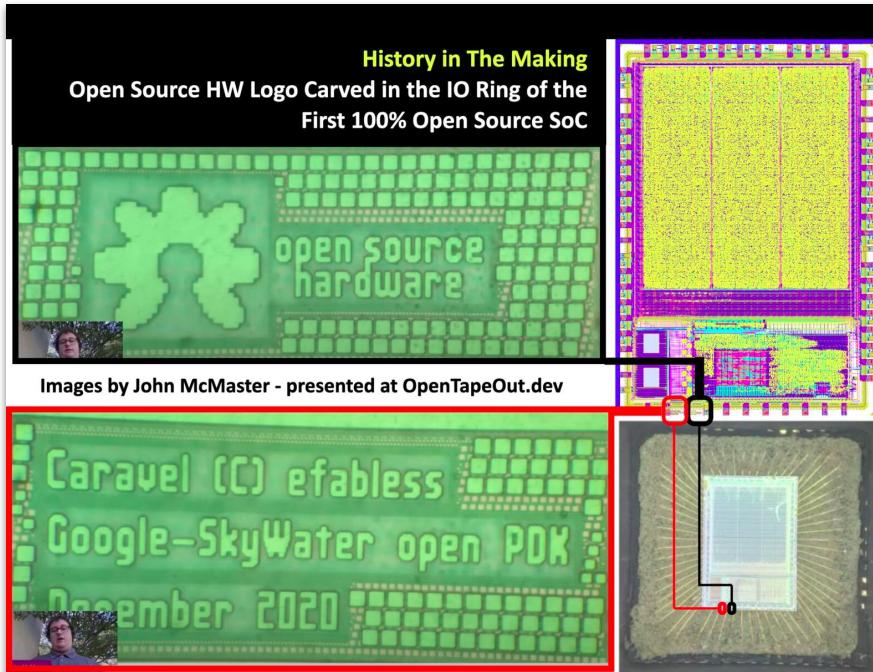
# SRAM characterisation by Andrew Zonenberg

- OpenRAM test
- Efabless provided ICs
- Reusable test board
- Designed in Kicad
- Video diary:
  - [Part 1](#)
  - [Part 2](#)
  - [Part 3](#)



# OpenTapeOut conference

[https://www.youtube.com/playlist?list=PLlynFETmdQDQdLCJu\\_HJBFNY17AAFP5W7](https://www.youtube.com/playlist?list=PLlynFETmdQDQdLCJu_HJBFNY17AAFP5W7)



Day 1 - Saturday 6th November Streaming on youtube		
Time (CET)	Speaker	Title
19:00	Tim 'mithro' Ansell	Keynote
19:40	Tom Spyrou & Matt Liberty	An update on the OpenROAD project
20:20	David Hulton	Fault Injection: Attacks and Defenses
20:30	Lucas Klemmer	Programmable Waveform Analysis using WAL
20:40	Joe FitzPatrick	101 ways to flip your bits and 100 ways to prevent it
Day 2 - Sunday 7th November Streaming on youtube		
Time (CET)	Speaker	Title
19:00	Mohamed Kassem	Making open source chips work
19:20	Thomas Parry	Talking to satellites with open silicon
19:40	Pepijn de Vos	Analog IC design in the 21st century
20:00	Jean-Paul Chaput	Coriolis, a FOSS RTL-to-GDSII Toolchain
20:20	Luke Leighton	Overview of the Libre-SOC Project
20:40	John McMaster	Efabless MPW physical implementation

# Workshop on Open-Source EDA Technology

- A CMOS Programmable Analog Standard Cell Library in Skywater 130nm Open-Source Process
- OpenCache: An Open-Source OpenRAM Based Cache Generator
- Papers and video presentations here:  
<https://woset-workshop.github.io/WOSET2021.html>

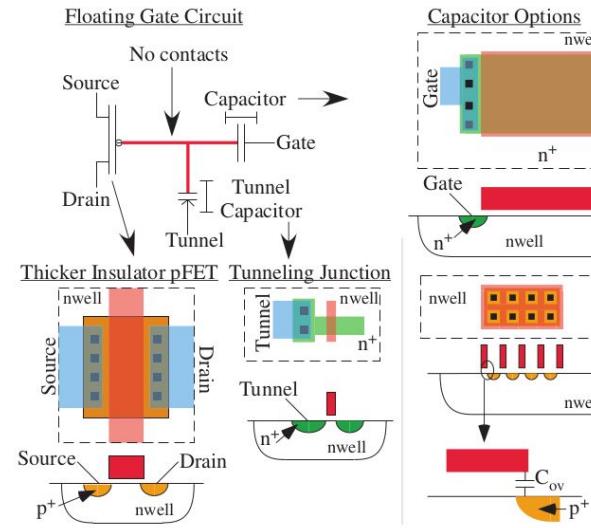
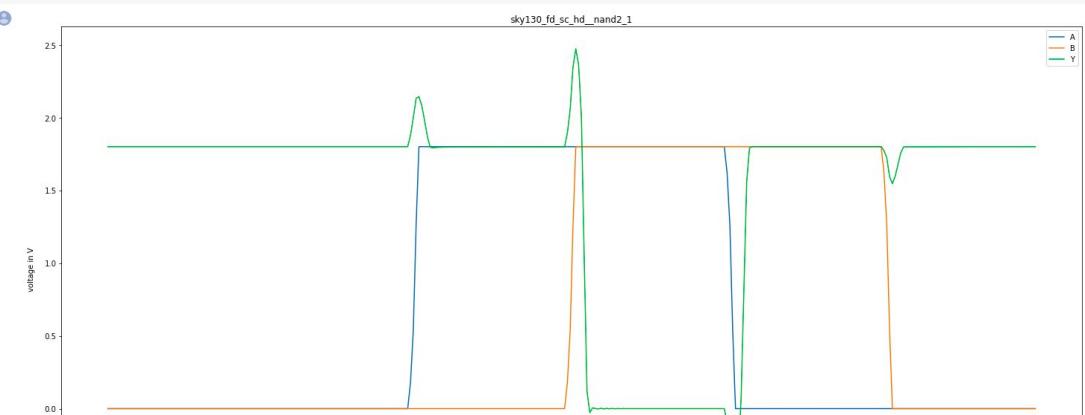


Fig. 2. A Floating-Gate (FG) circuit device requires a thick-insulator pFET for circuit operation and hot-electron injection programming, a single gate conductor with no contacts between elements, at least one input capacitor, and one tunneling capacitor. The capacitors for a typical bulk CMOS process (e.g. 130nm) include varactors (n<sup>+</sup> in nwell) and gate to diffusion overlap capacitors. Tunneling capacitor uses a minimal size capacitor, where the input capacitor(s) are typically a larger size. The total capacitance ( $C_T$ ) sets FG programming timing.

# ASIC tools in the cloud

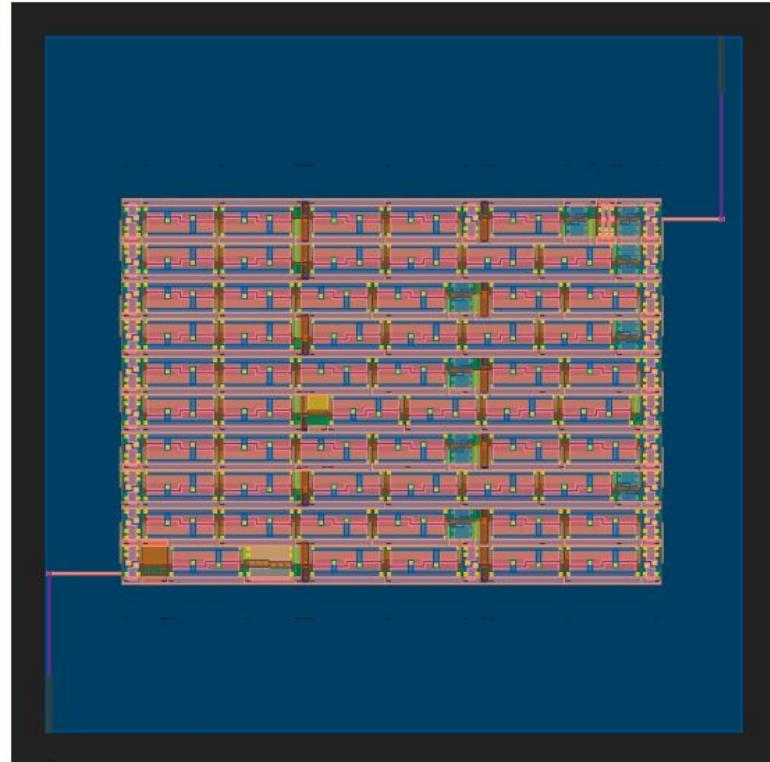
- [CMOS simulation](#)
- [OpenLane](#)
- Follow [Proppy on twitter](#)

```
import matplotlib.pyplot as plt
fig, ax = plt.subplots(figsize=(20, 10))
ax.set_title('sky130_fd_sc_hd_nand2_1')
ax.set_xlabel('time in 1e-14s')
ax.set_ylabel('voltage in V')
ax.plot(analysis.A)
ax.plot(analysis.B)
ax.plot(analysis.Y)
ax.legend(['A', 'B', 'Y'])
plt.tight_layout()
plt.show()
```



```
import pathlib
import gdstk
import IPython.display

gdss = sorted(pathlib.Path('/content/runs').glob('*/results/final/gdss'))
library = gdstk.read_gds(gdss[-1])
top_cells = library.top_level()
top_cells[0].write_svg('inverter.svg')
IPython.display.SVG('inverter.svg')
```



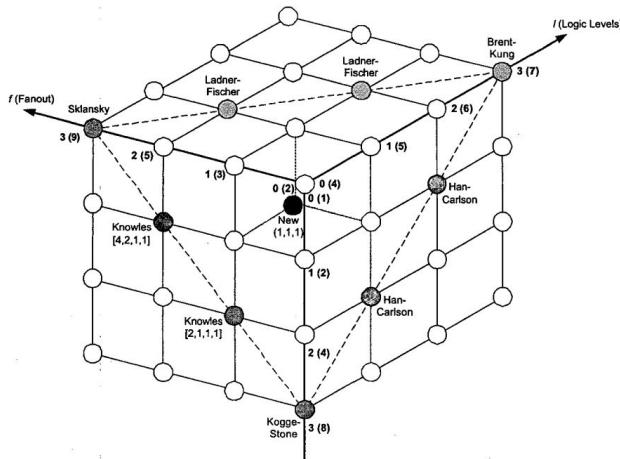
# GitHub Actions

Project	Submission
<ul style="list-style-type: none"><li>● <a href="#">template</a> provided</li><li>● <a href="#">configuration</a> done with YAML</li><li>● runs the tests</li><li>● makes it easier to know if your project is ready</li><li>● <a href="#">workflow file</a></li></ul>	<ul style="list-style-type: none"><li>● collects all the designs</li><li>● builds the submission</li><li>● runs all tests for all projects</li><li>● tristate proof</li><li>● hardens GDS</li><li>● Efabless precheck</li><li>● <a href="#">action used for MPW6</a></li></ul>

Triggered via push 9 days ago  mattvenn pushed -o 0bea000 <a href="#">mpw6</a>	Status <b>Success</b>	Total duration <b>1h 9m 6s</b>	Artifacts <b>2</b>
--	--------------------------	-----------------------------------	-----------------------

# Optimising hardware adders

- When a RISC-V processor boots into Linux, 65% to 72% of instructions use addition
- Teo's work allows us to create specific adders targeting a specific PPA
- We are instrumenting the adders and taping out on MPW6
- Follow [Teo on twitter](#)
- [Blogpost](#)

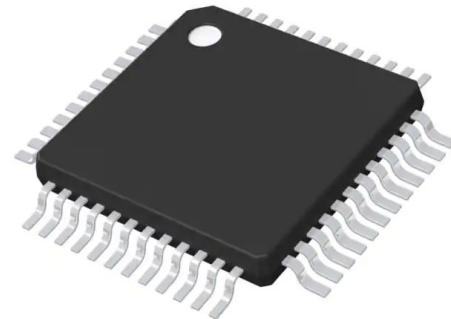


# TinyTapeout

Lowering the barrier to entry for  
ASIC design & manufacture

# Target audience

- Makers
- Schools
- Hackerspaces
- Entry level digital design course at university
- Open Source silicon enthusiasts!



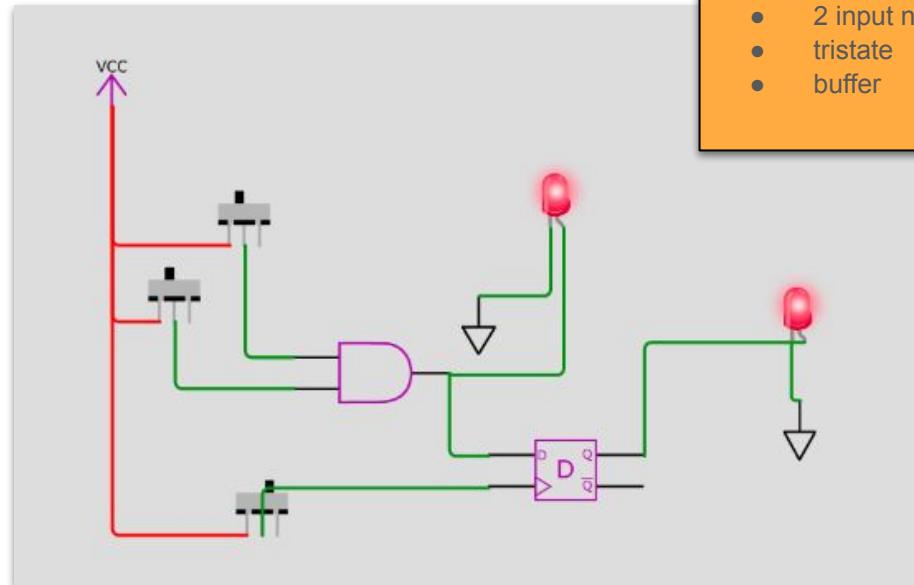
**Create opportunity for all high school tech students to design and receive their own chips.**

# Guided lesson plans / standalone / flipped classroom

- Intro
  - PDK basics,
  - simulation of standard cells
  - relevance of microelectronics / dispel “magic”
- Initial ideas for lesson plans
  - focus on combinational logic to start with
    - set switches to set segments for your initials, puzzles
  - introduce sequential
    - morse code blinker, traffic light, calculator
- Each segment supported by
  - templates for each project
  - video introductions
  - guided walkthrough solutions
  - additional resources

# Build digital designs in the browser

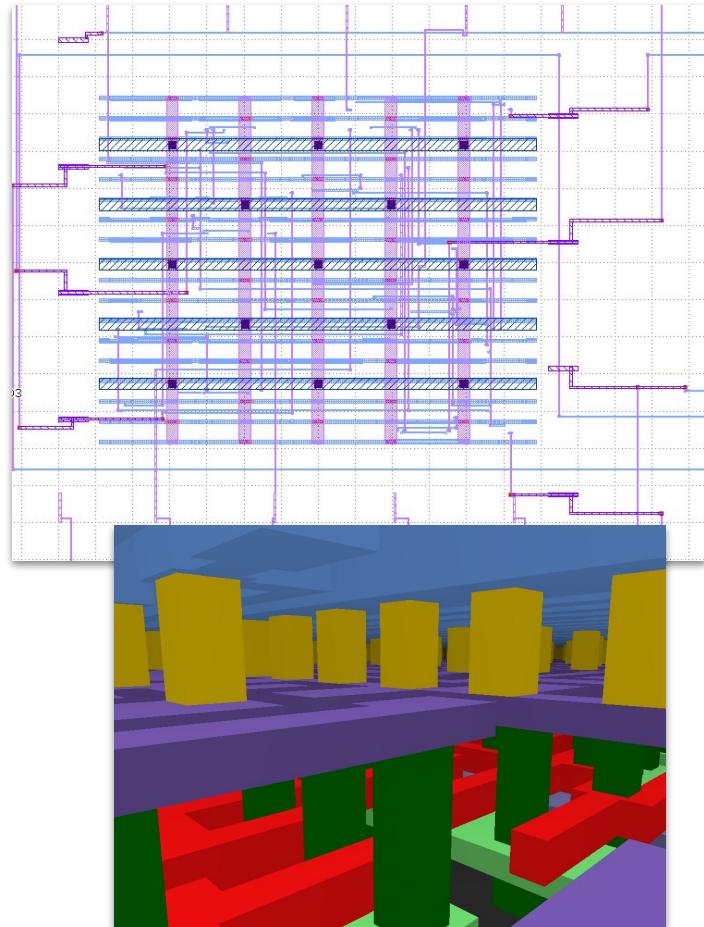
- [Wokwi](#) by Uri Shaked
  - Online simulator
  - no download required
- MVP added:
  - Verilog export
  - API to fetch Verilog file
  - mini cell library
  - clock input
- Open ended
  - build what you want



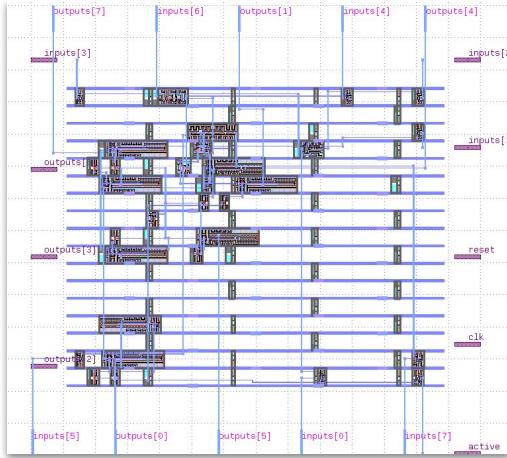
[Standard cell library](#), [Clock divider demo](#), [Animation](#)

# HDL -> GDS

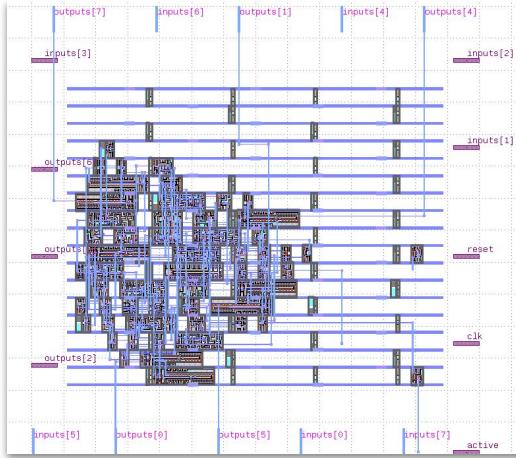
- Create new Github project from template
- Update config to fetch your design from Wokwi
- Github action builds the GDS
- 100um x 100um max size
- enough for about 200 gates
- 8 ins and 8 outs (clock & reset?)
- No tool install or download
- Easy to share image of your design



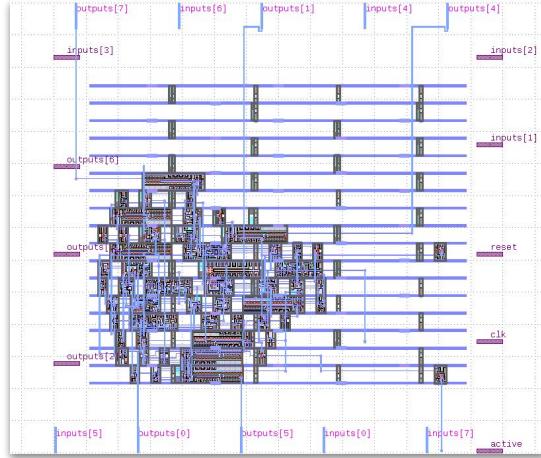
# GDS examples (all 70um x 70um)



binary to decimal  
converter  
25 cells



8 bit counter  
49 cells



4 bit counter & bcd  
50 cells

# Optional - pay for your design to be manufactured!

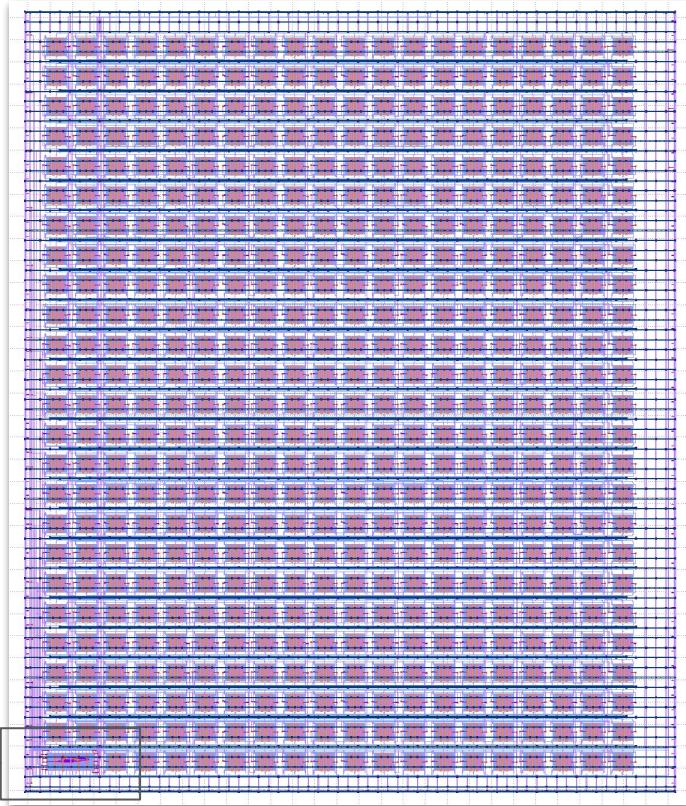
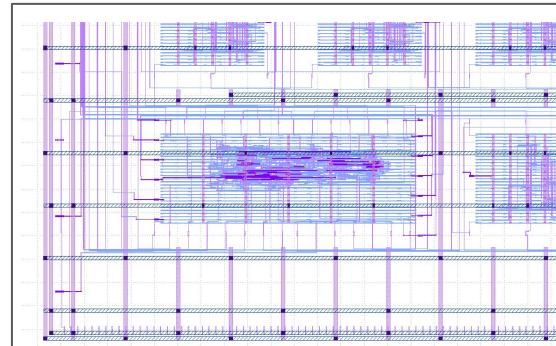
- \$100: IC + PCB + postcard GDS print of your design
- \$25: your design on the IC but no chip or PCB
- Pick a slot for your design on the chip

hackerspace runs workshop for 10 people and orders 1 board:

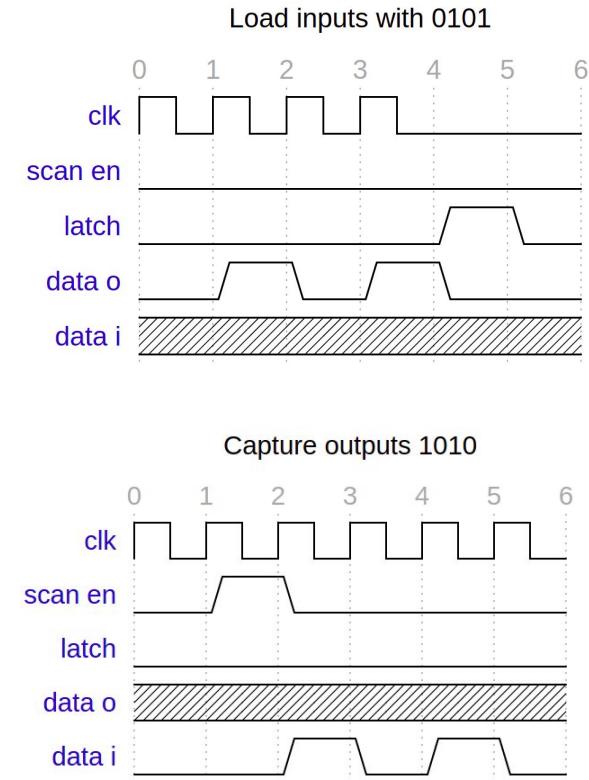
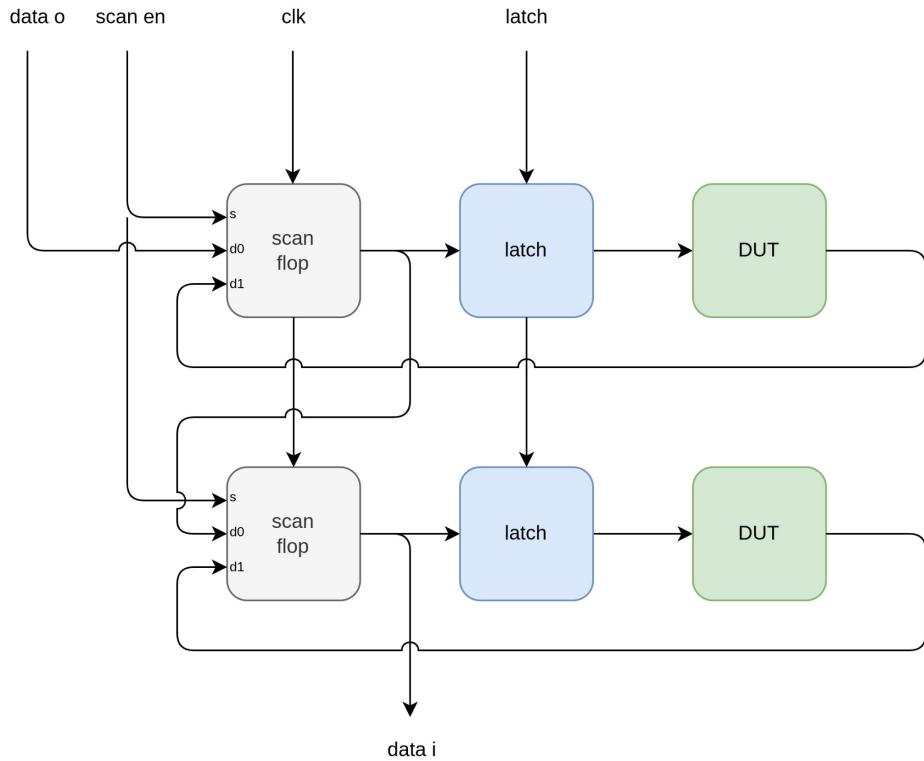
- $9 \times \$25 + 1 \times \$100 = \$325$
- $\$325 / 10 \text{ participants} = \$32.50 \text{ per ticket}$

# Add new design to public shuttle submission

- GDS generation done with a GH action
- Access each design with a JTAG like scan chain
- Low speed ~ 10 - 100kHz
- Currently getting 498 x designs of 100um
- Get 300 chips back on a shuttle, expect yield of 90% after PCBA

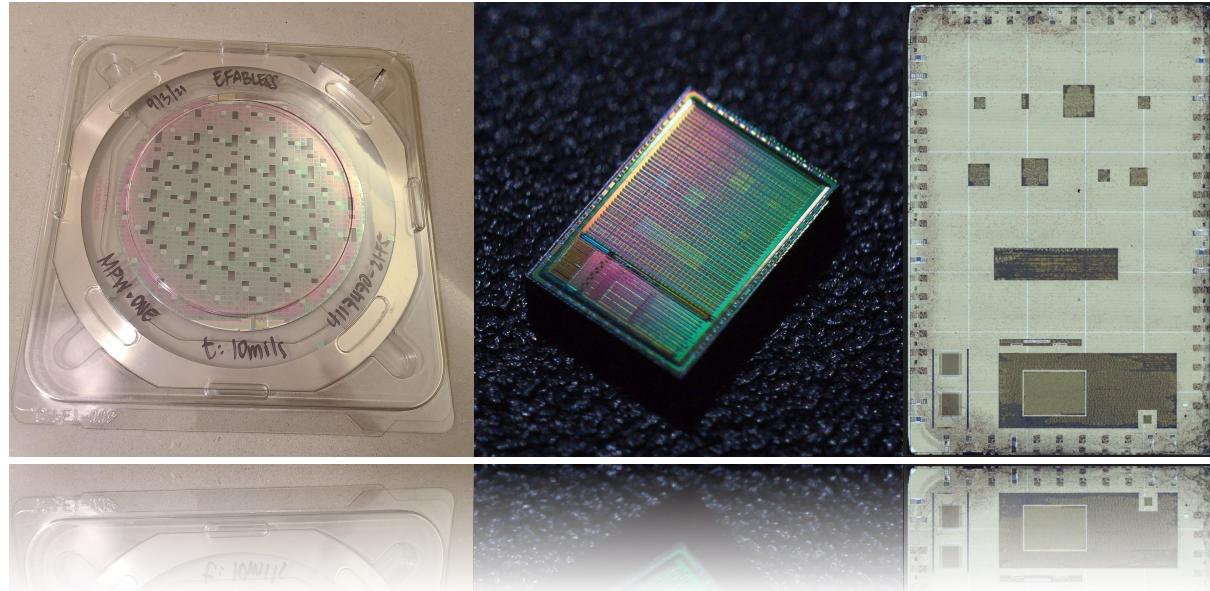


# Scan chain detail



# Receive emails throughout the 6 month wait

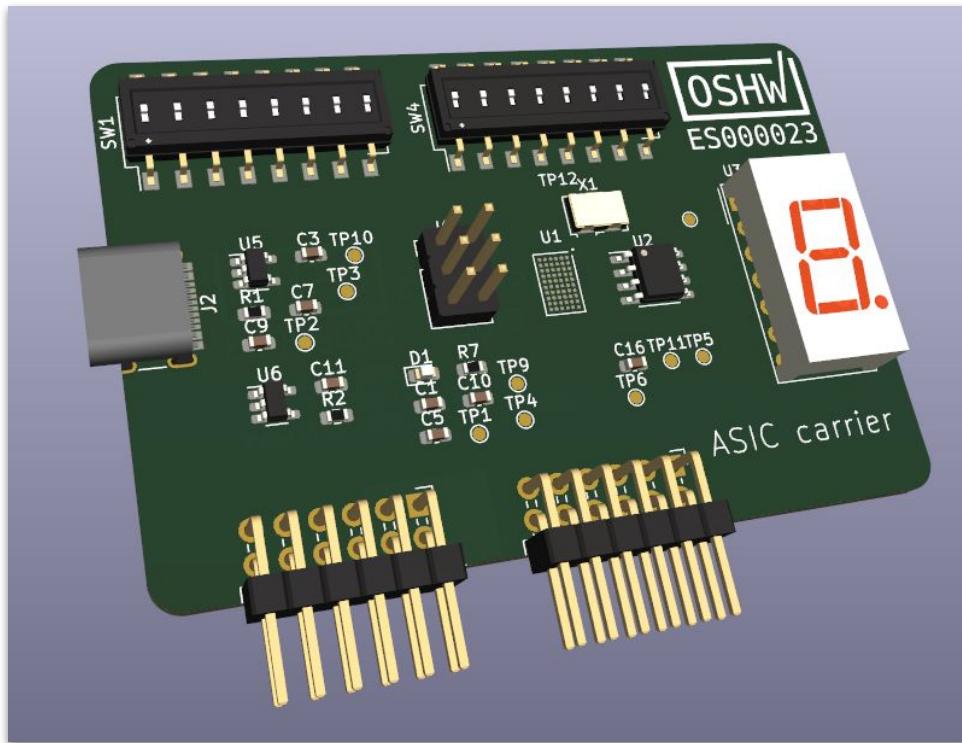
- ASIC basics / tutorials / ideas for designs / this week's coolest design
- When shuttle is full
- Virtual factory tour
- Wafers out
- PCBs out
- PCBs sent



# PCB

- USB C PSU, 3.3v and 1.8v
- Adjustable clock / single step
- 9 dip for design select (or jumpers)
- 8 dip for inputs
- 8 leds for outputs
- Include PMOD headers for IOs

Manufacturing note: ICs go onto breakouts / castellated modules for easier PCBA (board in China, IC in Europe).



A dark, high-contrast photograph featuring two integrated circuit (IC) packages. One chip is oriented vertically on the left, showing a green underside with a grid of gold-colored pins. The other chip is positioned diagonally on the right, showing a purple underside with similar pin connections. The background is a deep black, making the metallic components stand out.

**Watch this space...**

# Open source tools in education: Open-Source FPGA Foundation's 'Tape Out World'

- Program has been launched in several countries, including USA, India, Pakistan, Turkey, Egypt, Australia.
- Partnering with Universities around the world to make their own chips.
- Has completed training of 400 students in Pakistan. They are now working on taping out 12 projects.



# IEEE chip-a-thon



The goal of this chipathon is to bring together IC design newbies, enthusiasts and experienced mentors to benefit from the collaboration opportunities enabled by the rapidly growing open-source IC design movement.

Participants will be selected based on the quality of their submitted chip design proposals. There is no constraint on the complexity or type of design (analog/RF, mixed-signal or digital); you may elect to design your “dream chip” or simply contribute a small, but useful IP block to the community.

The finalists’ designs will be submitted for chip fabrication (130 nm CMOS) via Efabless’ chipIgnite program.

# Funding in the space

- ZeroASIC (silicon compiler) - \$5M
- Efabless - \$5M
- RapidSilicon - \$15M
- US & [EU Chips act](#) - both have educational & training aspects where OSS can be a first win

# EU Chips act

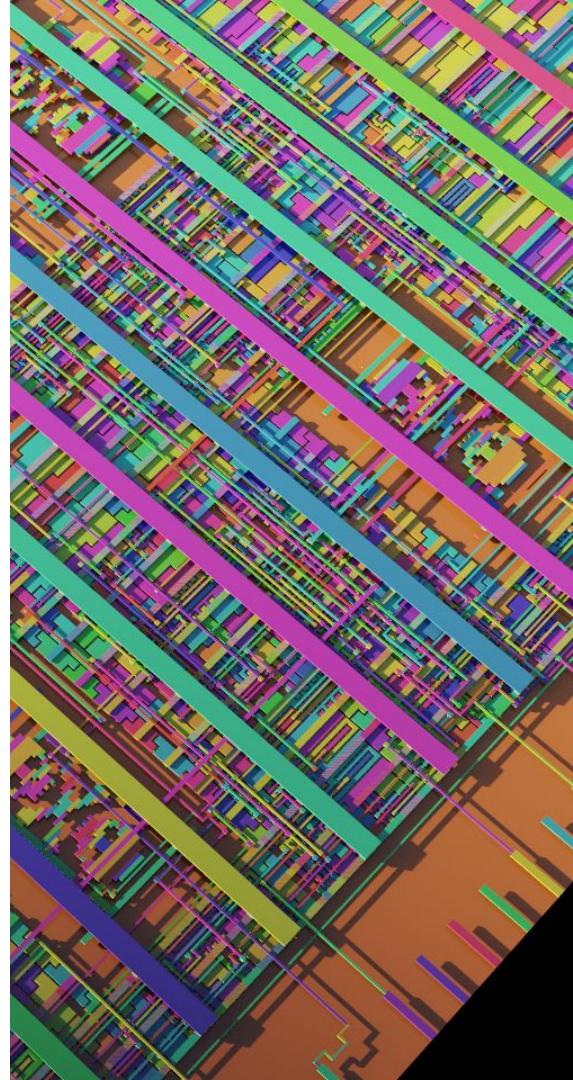
The European Commission has proposed to invest in a European **open source** EDA tooling ecosystem, encouraging open interchange formats and making sure current tools do not introduce restrictions on the utilization of **open source** hardware designs (page 53).

As the commercial vendors mostly provide closed source tools, there a move can be observed towards **open source** tools to support specific parts of the design flow.

**Open source** tools are essential for introducing new companies and more developers into the field, especially developers with a software background who can bring in innovation in hardware-software co-design (page 52).

# Community growth

- 3.5k [slack members](#) on 130 channels
- 650 stars on OpenLane github [repo](#)
- 2k stars on Skywater PDK [repo](#)
- 570 public projects with design/GDS on  
[Efabless website for MPW 1 to 7](#)
- More PDKs coming soon: 90, 130, 180nm
- [90nm just announced!](#)



# Get involved!

- Try the tools, make an issue or a PR
- Next tapeout is MPW7 September 12th.
- Take my [course!](#)
- 5 x \$200 discount code: COSCUP22
- [Awesome resources](#)

# Connect with me!

- Slides <https://bit.ly/coscup22>
- [Newsletter](#)
- Twitter [@matthewvenn](#)
- [Linked.in](#)

