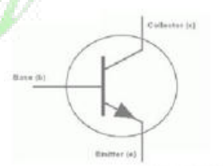
UNIT 3

BIPOLAR JUNCTION TRANSISTOR
&
FIELD EFFECT TRANSISTOR

BJT Introduction



- Concept: **transfer of resistance** [TRANSfer + resISTOR] = **TRANSISTOR**.
- Two types of Transistors: (i) Unipolar Junction Transistor and (ii) Bipolar Junction Transistor
- In unipolar transistor the current conduction is only due to one type of carriers, majority carriers.
- The term Bipolar reflects the fact that both electron and holes participate in the injection process into the oppositely polarized material. Hence this is called Bipolar Junction Transistor.

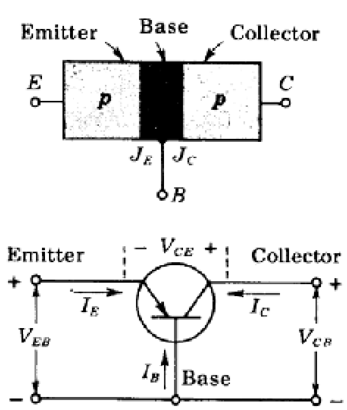
BJT Introduction

- 23 December 1947, S. William Schockley invented first junction transistor along with John Bardeen and Walter H. Brattain at Bell Telephone Laboratories
- Bipolar Junction Transistor (BJT) is an amplifying device that increases the voltage, current or power level. (earlier it was achieved by vacuum tubes)
- It has three terminals (base, emitter, collector) with one controlling the flow between the other two.
- The amplification in the transistor is provided by passing input current signal from a region of low resistance to a region of high resistance.

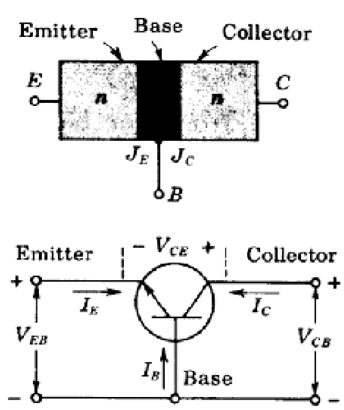
Transistor Construction

There are two types of transistors:
- **pnp**
- **npn**

The terminals are labeled:
- **E - Emitter**
- **B - Base**
- **C - Collector**

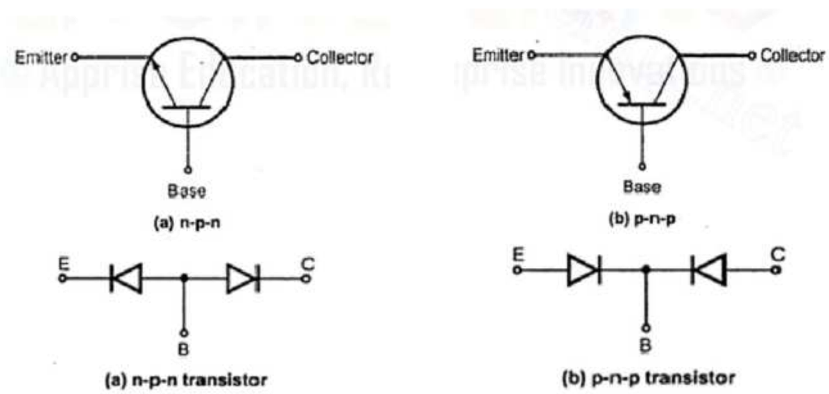


p-n-p type



n-p-n type

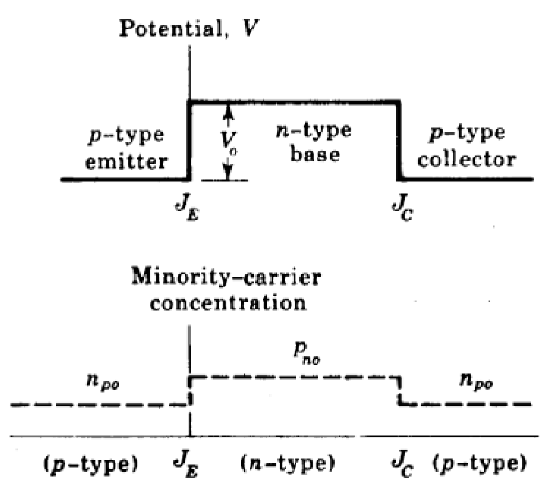
Transistor Symbol

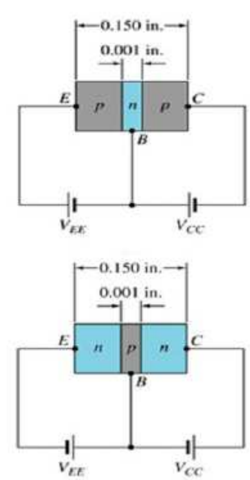


- Relative doping levels in base, emitter and collector must be satisfied to work as a transistor.
- In back to back diodes there are two separate diodes, one forward biased and one reverse biased and diffusion can not take place. Maximum current will be equal to the reverse saturation current of the reverse biased diode.
- Combination of back to back diodes can not work as transistor.

Transistor Working

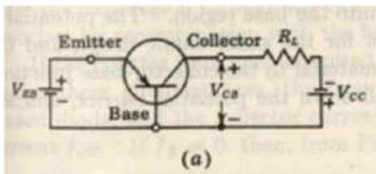
Doping levels: Emitter>Collector>Base

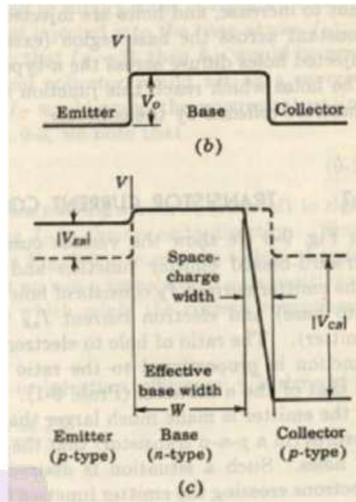




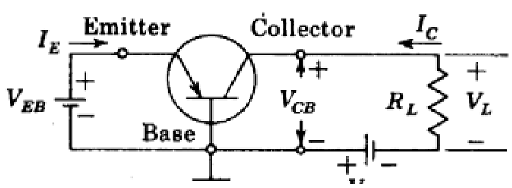
Transistor Working

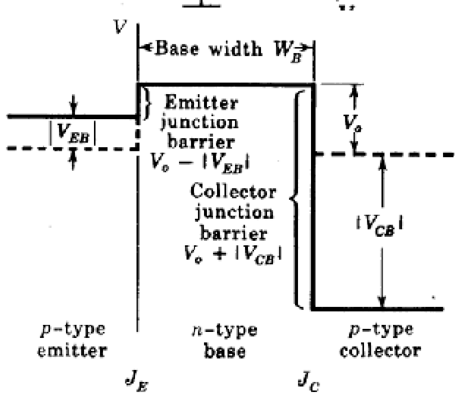
- **The emitter-base junction is forward biased**
- **The base-collector junction is reverse biased**

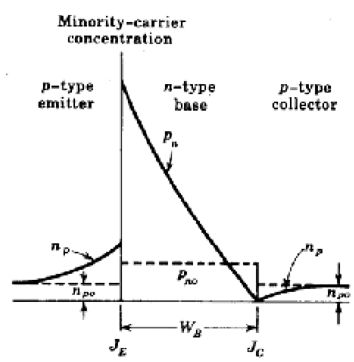




Transistor Working



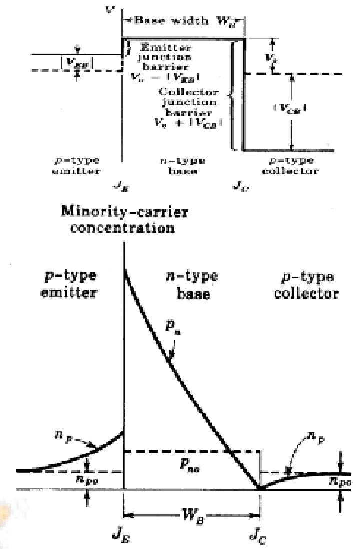




Transistor Working

Doping levels: Emitter>Collector>Base

- Lowering of the emitter base barrier permits minority carrier injection; i.e. holes are injected into the base and electrons are injected into the emitter region.
- Excess holes diffuse across the n-type base, where the electric field intensity is positive and large *(E=-dV/dx>>0)*, holes are accelerated across this junction.
- Holes reaching J_C fall down the potential barrier and therefore collected by collector.
- Since, potential across J_C is negative, from the law of junction, p_n is reduced to zero at collector. Similarly, the reverse collector junction bias reduces the collector electron density n_p to zero at J_C.



Current Components

Ratio of hole to electron currents is proportional to the conductivity of the p material to the n material.

$$I_{pE}/I_{nE} >> 1 \;\Rightarrow I_E \sim I_{pE}$$

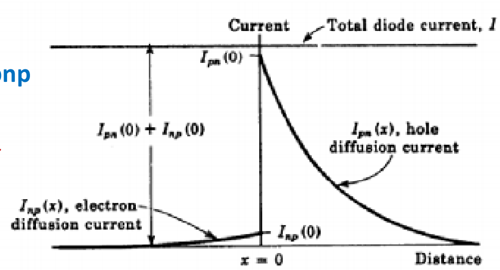
Emitter doping >> Base doping

This is desirable, since , electrons crossing the emitter junction from base to emitter do not contribute carriers which can reach the collector.

$$I_E = I_{pE} + I_{nE}$$

All currents are +ve for pnp transistor.

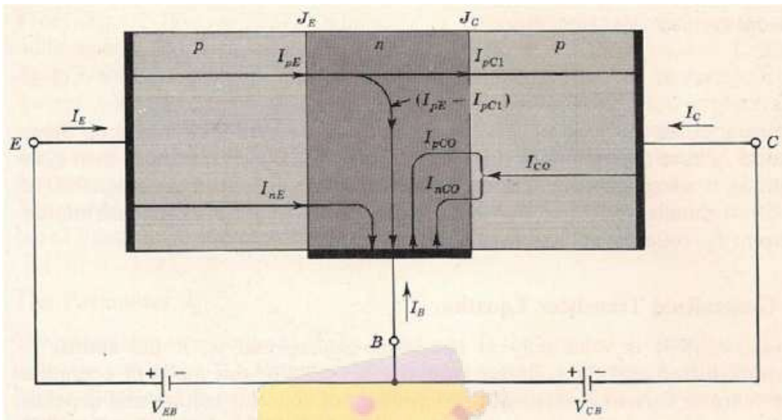
Not all the holes crossing the J_E reach the collector, because some of the holes recombine with electrons in the base.



Let I_{pC1} represent the hole current at J_C due to holes crossing the base from the emitter

Current Components

Hence, there must be a bulk recombination current $I_{pE} - I_{pC1}$ leaving the base. In reality electrons enter the base region from external circuit through base terminal to supply those charges which have been lost by recombination with the holes injected into the based across J_E.



Current Components

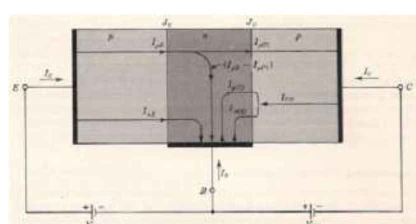
- Consider, for the moment, an open circuited emitter, while the collector junction remains reverse biased.
- The collector current must equal the reverse saturation current of back biased diode at J_C.
- This reverse current consists of two components:

  I_{nCO} consisting of electrons moving from p to n region across J_C and
  I_{pCO} holes crossing from n to p across J_C

  $-I_{CO} = I_{nCO} + I_{pCO}$ Minus sign is chosen so that I_C and I_{CO} have the same sign

  Since $I_E=0$, under open circuit conditions, no holes are injected across emitter junction and hence none can reach collector junction from the emitter.

  I_{pCO} results from the small concentration of holes generated thermally within the base.



Current Components

Now, considering the case in which the emitter is forward biased so that

$$I_C = I_{CO} - I_{pC1} = I_{CO} - \alpha I_E$$

α is defined as fraction of total current which represents holes which have travelled from the emitter across the base to the collector.

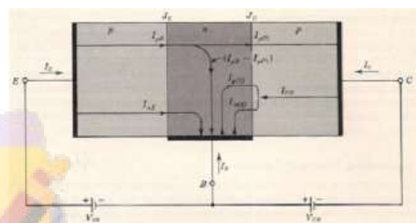
For p-n-p transistor, I_E is positive and both I_C and I_{CO} are negative, which means the current in the collector lead is in the direction opposite to that indicated by the arrow of I_C in the figure.

The electron current crossing J_C is I_{nCO} and represents electrons diffusing from collector into base (+ve current from the base into the collector), its magnitude is proportional to the slope at J_C of the n_p distribution.

Total diffusion hole current crossing J_C from the base is

$$I_{pC} = I_{pC1} + I_{pCO}$$

And its magnitude is proportional to the slope at J_C of the p_n distribution.



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Large signal current gain α

$$\alpha = -\frac{I_C - I_{CO}}{I_E - 0}$$

Collector and emitter currents have opposite signs, and hence it is always a +ve value. It lies between 0.90 to 0.998. It varies with emitter current, collector voltage, and temperature.

Generalized Transistor equation

$$I_C = I_{CO} - I_{pC1} = I_{CO} - \alpha I_E$$

This is valid in active region of operation.

For generalization, use the p-n diode current equation

$$I = I_o\left(e^{V/V_T} - 1\right) \quad I_o \Rightarrow -I_{CO} \quad V \Rightarrow V_C$$

$$I_C = -\alpha I_E + I_{CO}\left(1 - e^{V_C/V_T}\right)$$

If V_C is negative and large compared to V_T, it reduces to the equation same as valid in active region of operation.

p-n junction diode current crossing the collector junction is augmented by the fraction α of the current I_E flowing in the emitter.

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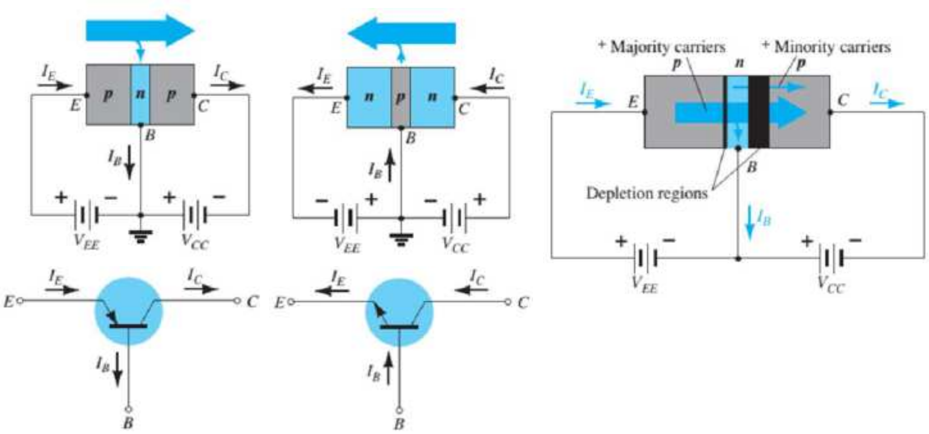
Current Components

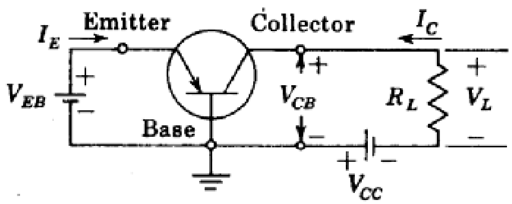
Emitter current is the sum of the collector and base currents:

$$I_E = I_C + I_B$$

The collector current is comprised of two currents: $I_C = I_{C_{\text{majority}}} + I_{CO_{\text{minority}}}$



Transistor as Amplifier



A small voltage change ΔV_i between emitter and base causes a relatively large emitter current change ΔI_E.

Let α' be fraction of ΔI_E collected and passed through R_L. $\Delta I_C = \alpha' \Delta I_E$

Change in output voltage across R_L may be many times the change in input voltage ΔV_i.

$\Delta V_L = -R_L \Delta I_C = -\alpha' R_L \Delta I_E$

Voltage amplification: $|A| = \Delta V_L / \Delta V_i > 1$

If the dynamic resistance of J_E is r_e, then: $\Delta V_i = r_e \Delta I_E$

Amplification factor: $A = -\dfrac{\alpha' R_L \Delta I_E}{r_e \Delta I_E} = -\dfrac{\alpha' R_L}{r_e}$ $\qquad r_e = 26/I_E$

Transistor as Amplifier

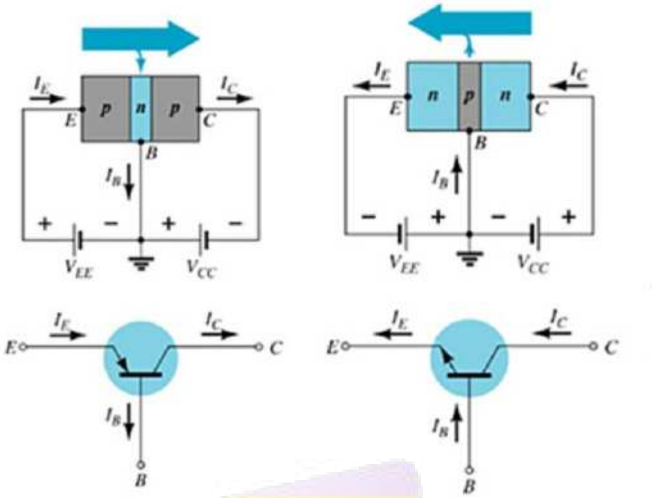
Parameter α' is defined as ratio of the change in the collector current to the change in the emitter current at constant collector-to-base voltage and is called the negative of the small signal short circuit current transfer ratio, or gain.

$$\alpha' = -\left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB}}$$

On the assumption that α is independent of I_E, then from

$$\alpha' = -\alpha \qquad I_C = I_{CO} - I_{pC1} = I_{CO} - \alpha I_E \Rightarrow \alpha = -\frac{I_C - I_{CO}}{I_E - 0}$$

Common-Base Configuration



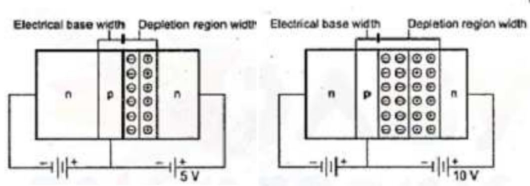
The base is common to both input (emitter–base) and output (collector–base) of the transistor

Common-Base Characteristics

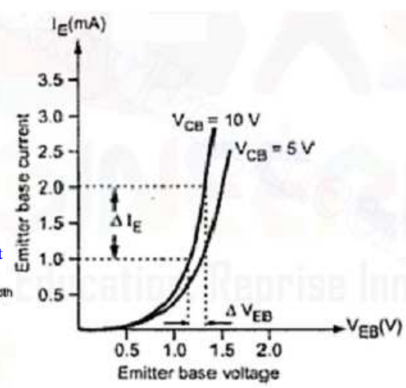
Input Characteristics

This curve shows the relationship between of input current (I_E) to input voltage (V_{BE}) for different output voltage (V_{CB}) levels.

$$V_{EB} = \phi_1\left(V_{CB}, I_E\right) \qquad r_i = r_e = \left.\frac{\Delta V_{EB}}{\Delta I_E}\right|_{V_{CB}=\text{constant}}$$

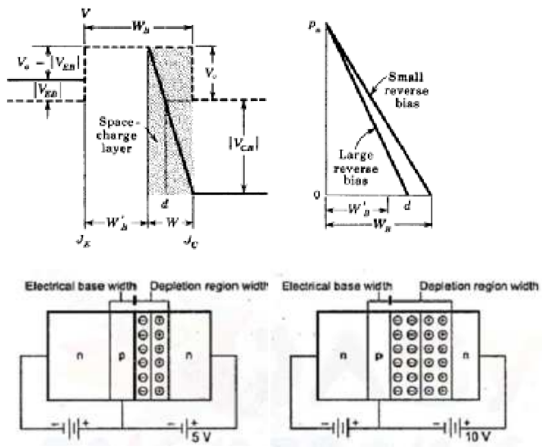


Due to reduction of electrical base width, gradient of charge concentration increases causing more diffusion of carreirs emitted from emitter.



I_E slightly increases with increase in the V_{CB} due to change in width of depletion region in the base under reverse bias condition.

Common-Base Characteristics



$$W_B^{'} = W_B - W$$

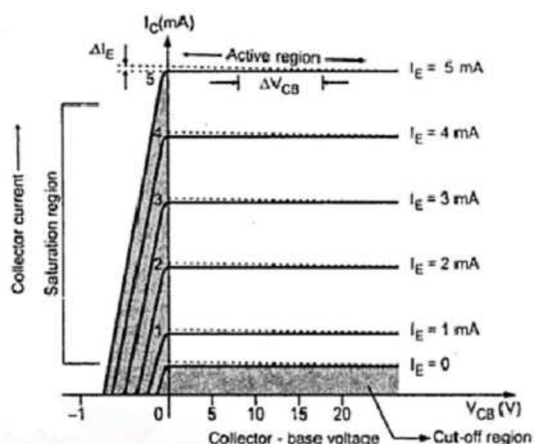
Due to reduction of electrical base width, gradient of charge concentration increases causing more diffusion of carreirs emitted from emitter.

Common-Base Characteristics contd…

Output Characteristics

$$I_C = \phi_2(V_{CB}, I_E)$$

- This graph demonstrates the output current (I_C) to an output voltage (V_{CB}) for various levels of input current (I_E).
- Active region– Operating range of the amplifier.
- Cutoff region– The amplifier is basically off. There is voltage, but little current.
- Saturation region– The amplifier is full on. There is current, but little voltage.

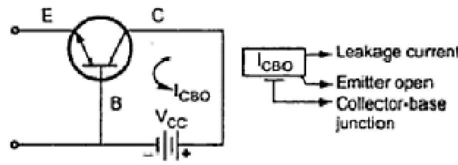


State	Emitter base junction	Collector base junction
Active	Forward biased	Reverse biased
Cut-off	Reverse biased	Reverse biased
Saturation	Forward biased	Forward biased

CB Currents and Current Gain

- Emitter and collector currents: $I_C \approx I_E$
- Base-emitter voltage: $V_{BE} = 0.7$ volts
- Common Base current gain $\alpha = I_C / I_E$
- Ideally : $\alpha = 1$
- Practically : α is between 0.9 and 0.998

$$R_o = \left.\frac{\Delta V_{CB}}{\Delta I_C}\right|_{I_E = \text{constant}}$$



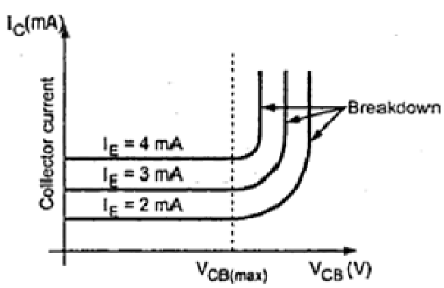
Ideal Currents: $I_E = I_C + I_B$ $\quad I_C = \alpha I_E$

Actual Currents: $I_C = \alpha I_E + I_{CBO}$

where I_{CBO} = minority collector current

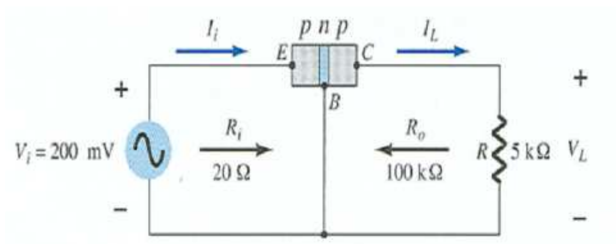
I_{CBO} is usually so small that it can be ignored, except in high power transistors and in high temperature environments.

Punch Through Effect



The curves shown at the right side of dotted line ($V_{CB\ max}$ is exceeded) represent the breakdown condition. When collector to base voltage increases, width of the depletion region at the junction increases. Therefore, when V_{CB} increases above the $V_{CB\ max}$, increase in depletion region is such that it penetrates into the base until it makes contact with emitter-base depletion region. This condition is called 'punch-through' or 'reach through' effect. When this situation occurs, breakdown occurs. i.e. large collector current flows which destroys the transistor. To avoid this punch-through effect V_{CB} should always be kept below the maximum safe limit specified by the manufacturer.

Transistor Amplification



Currents and **Voltages:**

$$I_E = I_i = \frac{V_i}{R_i} = \frac{200\text{mV}}{20\Omega} = 10\text{mA}$$

$$I_C \cong I_E$$

$$I_L \cong I_i = 10 \text{ mA}$$

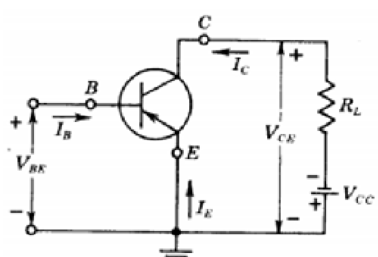
$$V_L = I_L R = (10 \text{ ma})(5 \text{ k}\Omega) = 50 \text{ V}$$

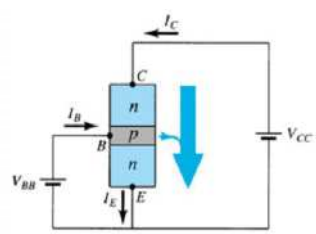
Voltage Gain:

$$A_v = \frac{V_L}{V_i} = \frac{50\text{V}}{200\text{mV}} = 250$$

Common-Emitter Configuration

The emitter is common to both input (base-emitter) and output (collector-emitter). The input is on the base and the output is on the collector.



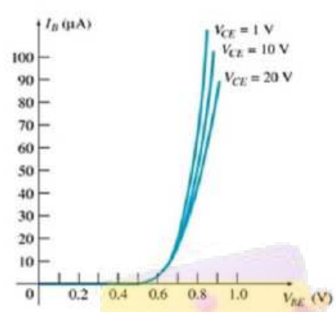


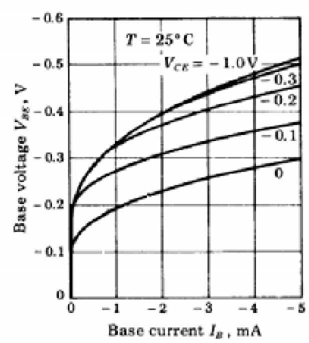
$$V_{BE} = f_1(V_{CE}, I_B) \qquad I_C = f_2(V_{CE}, I_B)$$

CE Input Characteristics

- With collector shorted to emitter, V_{CE}=0, and emitter forward biased, input characteristic is same as that of a forward biased diode.
- If V_{BE}=0, then I_B=0, since under this situation both emitter and collector junctions are short circuited.
- Increasing V_{CE} with constant V_{BE} causes a decrease in base width WB' and results a decreasing base current.

$$V_{BE} = f_1(V_{CE}, I_B)$$

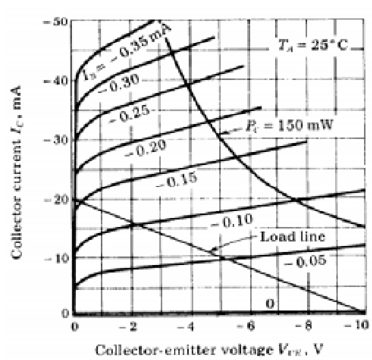


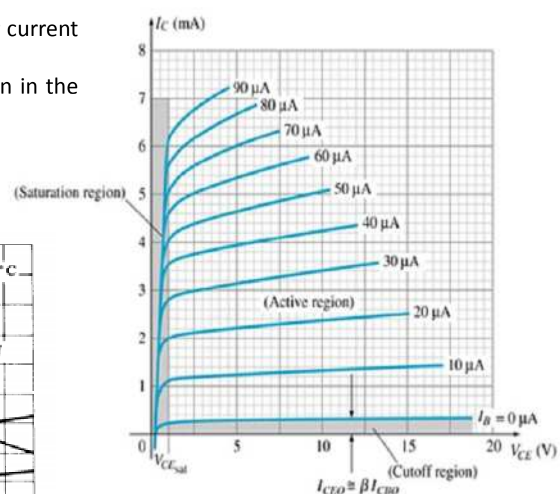


CE Output Characteristics

- For a fixed value of I_B, collector current is not much sensitive to V_{CE}.
- However, slopes are larger than in the CB characteristics.
- I_B is much smaller than I_E.

Regions of operation:
Active, Saturation, Cutoff



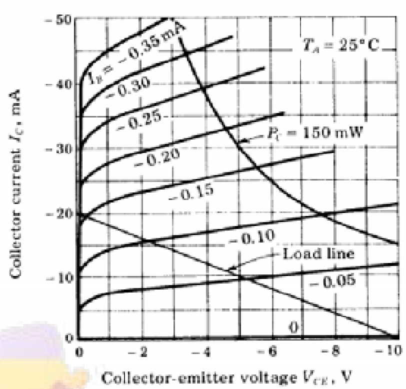


$$I_C = f_2(V_{CE}, I_B)$$

Common-Emitter Amplifier Currents

Active region

- **Right of ordinate V_{CE}= few tenths of a volt and above I_B=0.**
- **O/P current responds most sensitively to an input signal.**
- **For amplifying action, transistor is operated in this region of operation.**



Common-Emitter Amplifier Currents

$$I_C = I_{CO} - \alpha I_E = I_{CO} - \alpha\{-(I_C + I_B)\}$$

KCL: $I_E = -(I_C + I_B)$

$$I_C = I_{CO} + \alpha I_C + \alpha I_B \Rightarrow I_C(1-\alpha) = I_{CO} + \alpha I_B$$

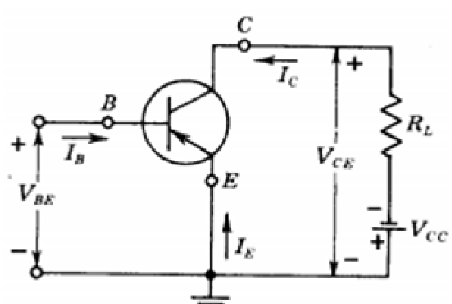
$$I_C = \frac{I_{CO}}{(1-\alpha)} + \frac{\alpha I_B}{(1-\alpha)}$$

If: $\beta = \alpha/(1-\alpha)$, then, $1/(1-\alpha) = (1+\beta)$

$$I_C = (1+\beta) I_{CO} + \beta I_B = I_{CEO} + \beta I_B$$

where I_{CEO} = minority collector current

$I_B >> I_{CO}$; $I_C \cong \beta I_B$

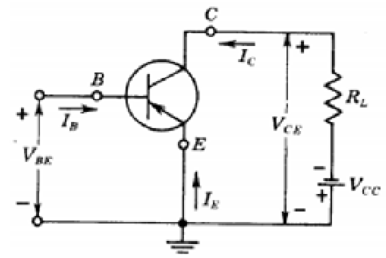


Common-Emitter Amplifier Currents

Cutoff region

When I_B = 0 μA the transistor is in cutoff, but there is some minority current flowing called I_{CEO}.

$$I_{CEO} = \frac{I_{CO}}{1-\alpha}\bigg|_{I_B=0\ \mu A} = (\beta+1)I_{CO}\Big|_{I_B=0\ \mu A}$$



At collector currents of the order of I_{CO}, α is very nearly zero because of recombination in the emitter junction transition region.

$$I_C = I_{CO} = -I_E$$

In silicon, cutoff occurs at $V_{BE} \approx 0$ V corresponding to a base short-circuited to the emitter.

Cutoff means,

$$I_E = 0,\ I_C = I_{CO},\ I_B = -I_C = -I_{CO}$$

And V_{BE} is a reverse voltage whose magnitude is of the order of 0.1 V for Ge and 0 V for a Si transistor.

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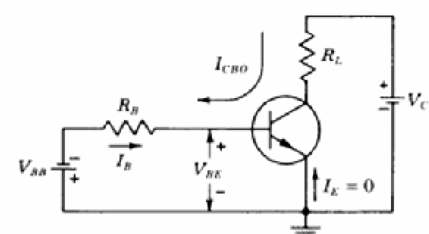
Current gain relations

When I_E = 0, collector current is called I_{CBO}. **$|I_{CBO}|>|I_{CO}|$**

- **A leakage current flows not through the junction but around it and across the surface.**
- **New carriers may be generated by collision in the collector junction transition region, leading to avalanche multiplication of current and eventual breakdown. This current may attain considerable proportions even before breakdown.**



- Beta (β) represents the amplification factor in common emitter

  $\beta = I_C / I_B$
- Alpha (α) represents the amplification factor in common base

  $\alpha = I_C / I_E$
- Relationship between amplification factors β and α

  $\alpha = \beta/(\beta+1)$, $\beta=\alpha/(1-\alpha)$
- Relationship Between Currents

  $I_C = \beta I_B$, $I_E = (\beta+1) I_B$

Large signal current gain (β)

$$I_C = (1+\beta)I_{CO} + \beta I_B = I_{CO} + \beta I_{CO} + \beta I_B$$

$$\beta = \frac{I_C - I_{CO}}{I_B + I_{CO}} = \frac{I_C - I_{CBO}}{I_B - (-I_{CBO})}$$

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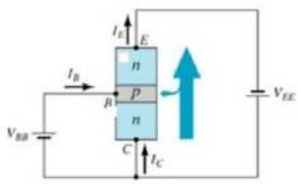
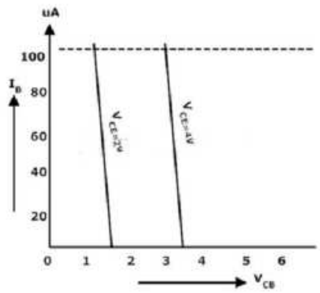
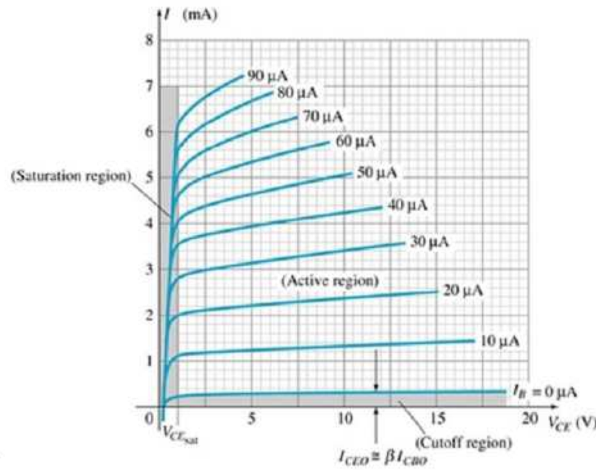
Common-Collector Configuration







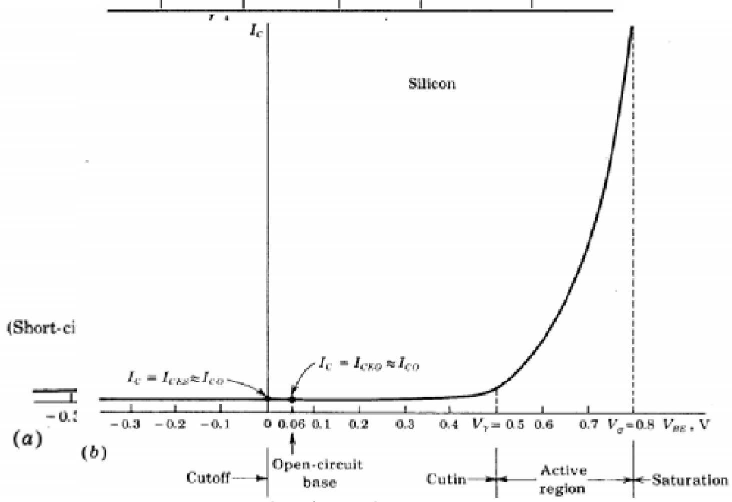
Output characteristics

Input characteristics

Collector current vs. V_{BE}

TABLE 5-1 Typical *n-p-n* transistor-junction voltages at 25°C

	$V_{CE,sat}$	$V_{BE,sat} = V_\sigma$	$V_{BE,active}$	$V_{BE}\ddagger_{,cutin} = V_\gamma$	$V_{BE,cutoff}$
Si	0.2	0.8	0.7	0.5	0.0
Ge	0.1	0.3	0.2	0.1	−0.1



Comparison of Transistor configurations

Sr.No.	Characteristic	Common Base	Common Emitter	Common Collector
1.	Input resistance	Very low (20 Ω)	Low (1 kΩ)	High (500 kΩ)
2.	Output resistance	Very high (1 MΩ)	High (40 kΩ)	Low (50 Ω)
3.	Input current	I_E	I_B	I_B
4.	Output current	I_C	I_C	I_E
5.	Input voltage applied between	Emitter and Base	Base and Emitter	Base and Collector
6.	Output voltage taken between	Collector and Base	Collector and Emitter	Emitter and Collector
7.	Current amplification factor	$\alpha_{dc} = \frac{I_C}{I_E}$	$\beta_{dc} = \frac{I_C}{I_B}$	$\frac{I_E}{I_B}$
8.	Current gain	Less than unity	High (20 to few hundreds)	High (20 to few hundreds)
9.	Voltage gain	Medium	Medium	less than unity
10.	Applications	As a input stage of multistage amplifier	For audio signal amplification	For impedance matching

Recap

- $I_E = I_C + I_B$
- $I_C = \alpha\ I_E$
- $I_C = \beta\ I_B$
- $I_C = \alpha\ I_E + I_{CBO}$
- $\alpha = \beta/(\beta+1)$
- $\beta=\alpha/(1-\alpha)$
- $I_E = (\beta+1)\ I_B$

Quiz

- The current gain of common collector is highest .
  (a) True (b) False
- The voltage gain of common base is highest .
  (a) True (b) False
- The power gain of common emitter is highest .
  (a) True (b) False

Analytical Expression for Transistor Characteristics

Dependence of currents in transistor upon junction voltages:

$$I_C = -\alpha_N I_E + I_{CO}\left(1 - e^{V_C/V_T}\right) = -\alpha_N I_E - I_{CO}\left(e^{V_C/V_T} - 1\right)$$

Subscript N to α indicates transistor in normal mode.

There is no essential reason which constrains us from using transistor in an inverted fashion, i.e., interchanging the roles of the emitter junction and collector junction.

However, from practical point of view, such an arrangement might not be as effective as the normal mode.

For this inverted mode of operation:

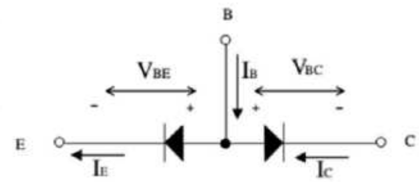
$$I_E = -\alpha_I I_C + I_{EO}\left(1 - e^{V_E/V_T}\right) = -\alpha_I I_C - I_{EO}\left(e^{V_E/V_T} - 1\right)$$

α_I Is the inverted common base current gain, similar to α_N.

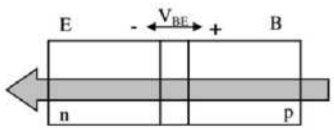
Above equations are derived in a heuristic manner.
Physical analysis of the transistor currents by “Ebers and Moll” verifies these equations.

Analytical Expression for Transistor Characteristics

J. J. Ebers and J. L. Moll from Bell Laboratories in the early 1954 formulated BJT model widely known as "Ebers Moll model" or "Coupled diode model".

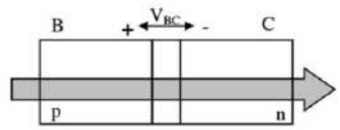


BJT as two back-to-back p-n junctions



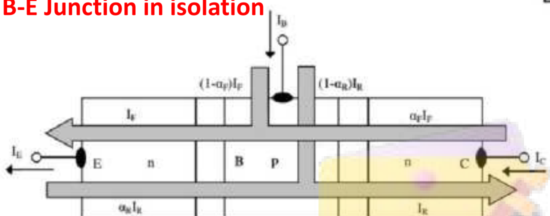
$I_F = I_{ES}(e^{V_{BE}/V_T} - 1)$

B-E Junction in isolation



$I_R = I_{CS}(e^{V_{BC}/V_T} - 1)$

B-C Junction in isolation

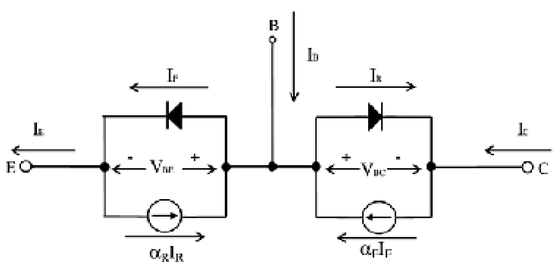


← Combined B-E and B-C junctions

Analytical Expression for Transistor Characteristics

Ebers-Moll model creates electrical model using normal diode laws with an additional transfer ratio to quantify the interdependency of junctions.

interdependency is quantified by forward and reverse transfer ratios, α_N and α_I.

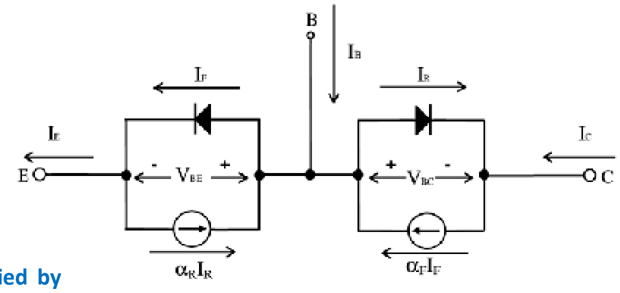


$$I_F = I_{ES}\left(e^{V_{BE}/V_T} - 1\right); \quad I_{ES} = qA\left(\frac{D_e p_{eo}}{L_e} + \frac{D_b n_{bo}}{W_b}\right) = qA\left(\frac{D_e n_i^2}{L_e N_e} + \frac{D_b n_i^2}{W_b N_b}\right)$$

$$I_R = I_{CS}\left(e^{V_{BC}/V_T} - 1\right); \quad I_{CS} = qA\left(\frac{D_c p_{co}}{L_c} + \frac{D_b n_{bo}}{W_b}\right) = qA\left(\frac{D_c n_i^2}{L_c N_c} + \frac{D_b n_i^2}{W_b N_b}\right)$$

Analytical Expression for Transistor Characteristics

Ebers-Moll model creates electrical model using normal diode laws with an additional transfer ratio to quantify the interdependency of junctions.



interdependency is quantified by forward and reverse transfer ratios, α_N and α_I.

$$I_E = I_{ES}\left(e^{V_{BE}/V_T}-1\right)-\alpha_R I_{CS}\left(e^{V_{BC}/V_T}-1\right)$$

$$I_C = \alpha_F I_{ES}\left(e^{V_{BE}/V_T}-1\right)-I_{CS}\left(e^{V_{BC}/V_T}-1\right)$$

$$I_B = \left(1-\alpha_F\right)I_{ES}\left(e^{V_{BE}/V_T}-1\right)+\left(1-\alpha_R\right)I_{CS}\left(e^{V_{BC}/V_T}-1\right)$$

Modes of Operation

Forward Active: B-E Forward biased, V_{BE} => +ve B-C Reverse biased, V_{BC} => -ve

$e^{V_{BE}/V_T} >> 1$ $e^{V_{BC}/V_T} << 1$

$$I_E \approx I_{ES}e^{V_{BE}/V_T}$$

$$I_C \approx \alpha_F I_{ES}e^{V_{BE}/V_T} = \alpha_F I_E$$

$$I_B \approx \left(1-\alpha_F\right)I_{ES}e^{V_{BE}/V_T} = \left(1-\alpha_F\right)I_E$$

Relatively large
Relatively large
small

Reverse Active: B-E Reverse biased, V_{BE} => -ve B-C Forward biased, V_{BC} => +ve

$e^{V_{BE}/V_T} << 1$ $e^{V_{BC}/V_T} >> 1$

$$I_E \approx -\alpha_R I_{CS}e^{V_{BC}/V_T}$$

$$I_C \approx -I_{CS}e^{V_{BC}/V_T} = \alpha_F I_E$$

$$I_B \approx \left(1-\alpha_R\right)I_{CS}e^{V_{BC}/V_T}$$

Moderately high
Moderate
As high as $0.5\left|I_C\right|$

Modes of Operation

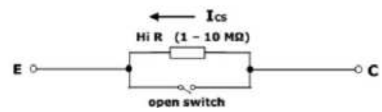
Cut-Off Mode: B-E unbiased, V_{BE} => 0 V B-C Reverse biased, V_{BC} => -ve

$e^{V_{BE}/V_T} = 1$ $e^{V_{BC}/V_T} << 1$

$I_E \approx \alpha_R I_{CS}$ **Leakage current (nA)**

$I_C \approx I_{CS}$ **Leakage current (nA)**

$I_B \approx -(1-\alpha_R) I_{CS}$



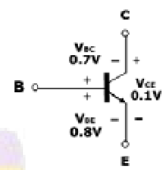
Saturation Mode: B-E Forward biased, V_{BE} => +ve B-C Forward biased, V_{BC} => +ve

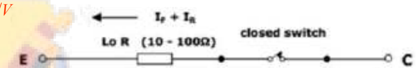
$e^{V_{BE}/V_T} >> 1$ $e^{V_{BC}/V_T} >> 1$

$I_E \approx I_{ES} e^{V_{BE}/V_T} - \alpha_R I_{CS} e^{V_{BC}/V_T}$

$I_C \approx \alpha_F I_{ES} e^{V_{BE}/V_T} - I_{CS} e^{V_{BC}/V_T}$

$I_B \approx (1-\alpha_F) I_{ES} e^{V_{BE}/V_T} + (1-\alpha_R) I_{CS} e^{V_{BC}/V}$





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DC Biasing

- It is applying DC voltages to a transistor in order to turn it on so that it can amplify AC signals.
- There are Three Operating Regions:

a) Active Region Operation

- Base–Emitter junction is forward biased
- Base–Collector junction is reverse biased

b) Cutoff Region Operation

- Both the junctions are reverse biased

c) Saturation Region Operation

- Both the junctions are forward biased

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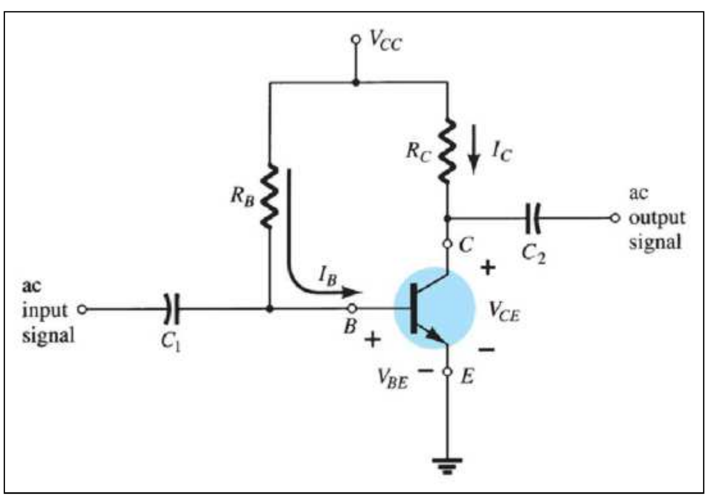
DC Biasing Circuits

1. Fixed-bias circuit
2. Emitter-stabilized bias circuit
3. Voltage divider bias circuit
4. DC bias with voltage feedback

1. Fixed Bias

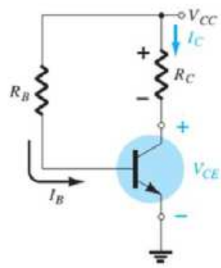


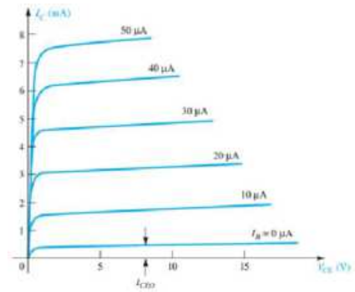
Load line analysis

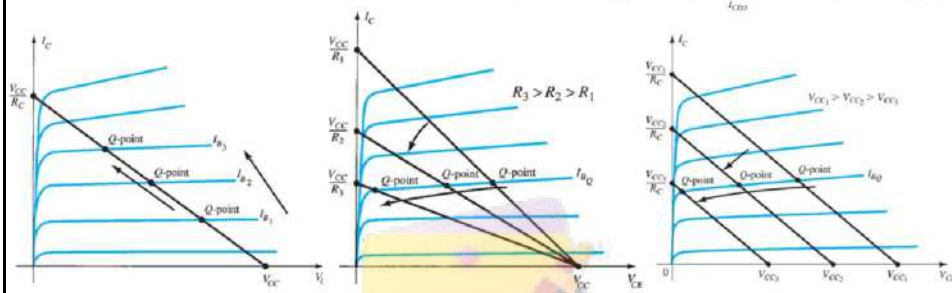
$$V_{CE} = V_{CC} - I_C R_C$$

$$@I_C = 0, \qquad V_{CE} = V_{CC}\big|_{I_C=0}$$

$$@V_{CE} = 0, \qquad I_C = \frac{V_{CC}}{R_C}\bigg|_{V_{CE}=0}$$







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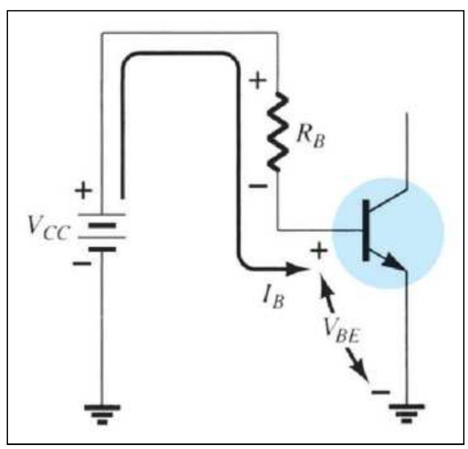
The Base-Emitter Loop

From Kirchhoff's voltage law:

$$\boxed{+V_{CC} - I_B R_B - V_{BE} = 0}$$

Solving for base current:

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B}}$$



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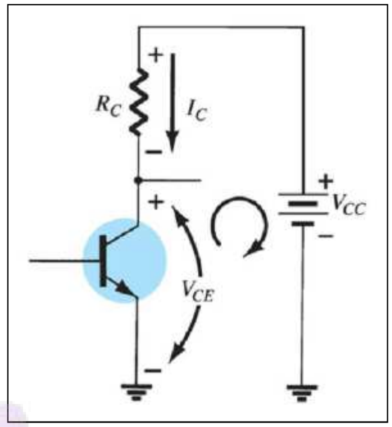
Collector-Emitter Loop

Collector current:

$$I_C = \beta I_B$$

From Kirchhoff's voltage law:

$$V_{CE} = V_{CC} - I_C R_C$$



Saturation

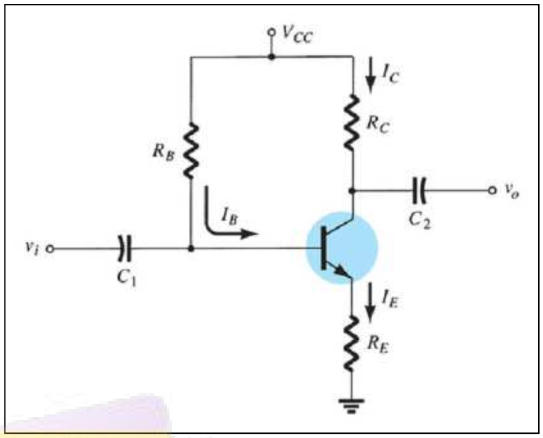
When the transistor is operating in **saturation**, current through the transistor is at its *maximum* possible value.

$$I_{Csat} = \frac{V_{CC}}{R_C}$$

$$V_{CE} \cong 0\ V$$

2. Emitter-Stabilized Bias Circuit

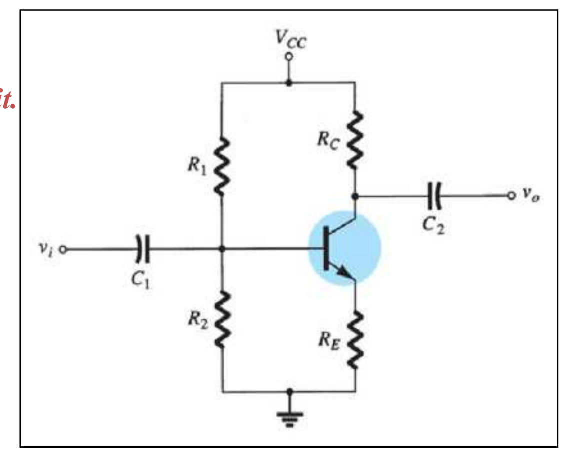
Adding a resistor (R_E) to the emitter circuit stabilizes the bias circuit.



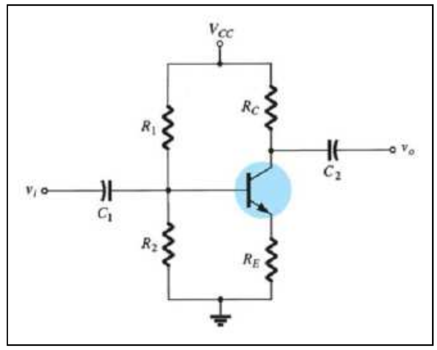
3. Voltage Divider Bias

This is a very stable bias circuit.

The currents and voltages are nearly independent of any variations in β.



Approximate Analysis



Where $I_B << I_1$ and $I_1 \cong I_2$:

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$

Where $\beta R_E > 10R_2$:

$$I_E = \frac{V_E}{R_E}$$

$$V_E = V_B - V_{BE}$$

From Kirchhoff's voltage law:

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$I_E \cong I_C$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

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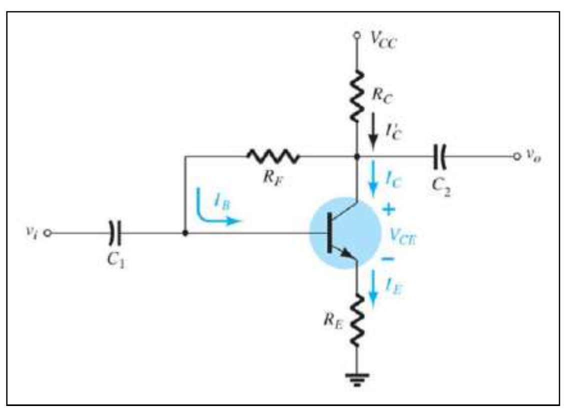
4. DC Bias With Voltage Feedback

Another way to improve the stability of a bias circuit is to add a feedback path from collector to base.



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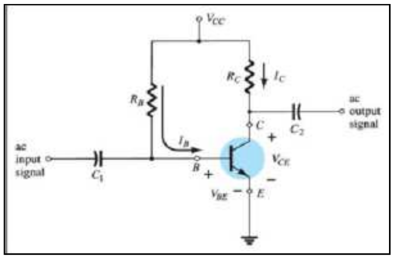
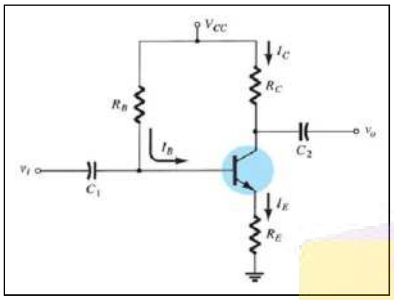
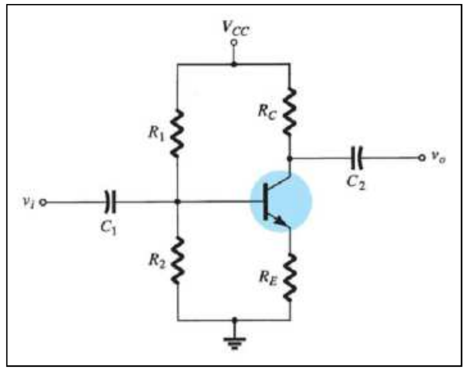
Recap (Fixed, Emitter, Voltage bias)







FETs vs. BJTs

Similarities:

Amplifiers
Switching devices
Impedance matching circuits

Differences:

FETs are voltage controlled devices. BJTs are current controlled devices.

FETs have higher input impedance. BJTs have higher gain.

FETs are less sensitive to temperature variations and are better suited for integrated circuits

FETs are generally more static sensitive than BJTs.

FET Types

JFET: Junction Field Effect Transistor

MOSFET: Metal–Oxide–Semiconductor FET

D-MOSFET: Depletion MOSFET

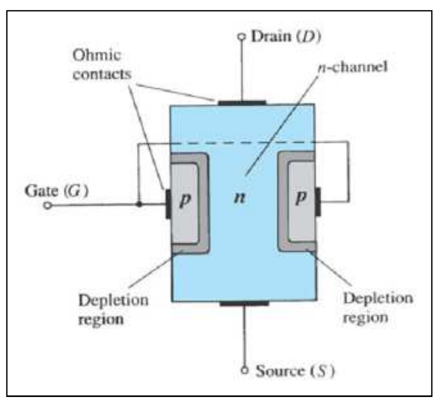
E-MOSFET: Enhancement MOSFET

JFET Construction

There are two types of JFETs:

***n*-channel**
***p*-channel**

The n-channel is the more widely used of the two.



JFETs have three terminals:

The **Drain** (D) and **Source** (S) are connected to the *n*-channel

The **Gate** (G) is connected to the *p*-type material

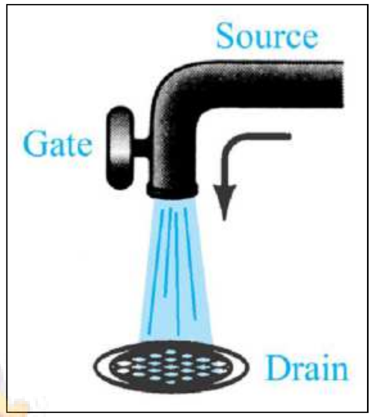
JFET Operation: The Basic Idea

JFET operation can be compared to that of a water spigot.

The **source** is the accumulation of electrons at the negative pole of the drain-source voltage.

The **drain** is the electron deficiency (or holes) at the positive pole of the applied voltage.

The **gate** controls the width of the n-channel and, therefore, the flow of charges from source to drain.



JFET Operating Characteristics

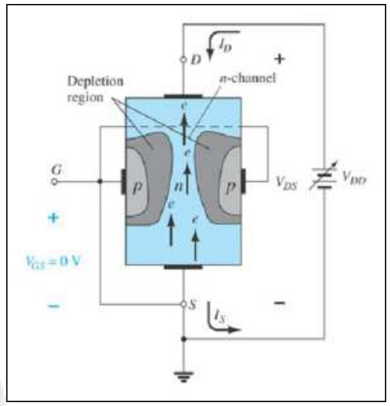
There are three basic operating conditions for a JFET:

- $V_{GS} = 0$ V, V_{DS} increasing to some positive value
- $V_{GS} < 0$ V, V_{DS} at some positive value
- Voltage-controlled resistor

JFET Characteristics: V_{GS}=0V

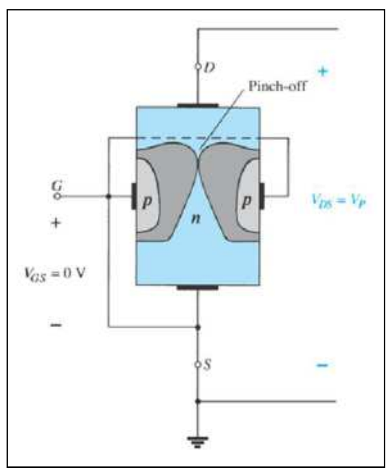
Three things happen when V_{GS} = 0 V and V_{DS} increases from 0 V to a more positive voltage:

- The size of the depletion region between *p*-type gate and *n*-channel increases.
- Increasing the size of the depletion region decreases the width of the *n*-channel, which increases its resistance.
- Even though the *n*-channel resistance is increasing, the current from source to drain (I_D) through the *n*-channel is increasing because V_{DS} is increasing.



JFET Characteristics: Pinch Off

- If V_{GS} = 0 V and V_{DS} continually increases to a more positive voltage, a point is reached where the depletion region gets so large that it pinches off the channel.
- This suggests that the current in channel (I_D) drops to 0 A, but it does not: As V_{DS} increases, so does I_D. However, once pinch off occurs, further increases in V_{DS} do not cause I_D to increase.

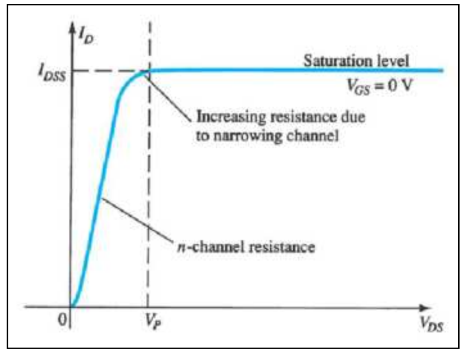


JFET Characteristics: Saturation

At the pinch-off point:

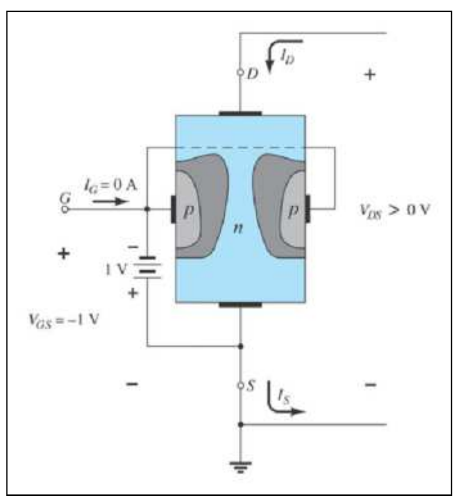
Any further increase in V_{DS} does not produce any increase in I_D. V_{DS} at pinch-off is denoted as $\boldsymbol{V_p}$

I_D is at saturation or maximum, and is referred to as $\boldsymbol{I_{DSS}}$.



JFET Operating Characteristics

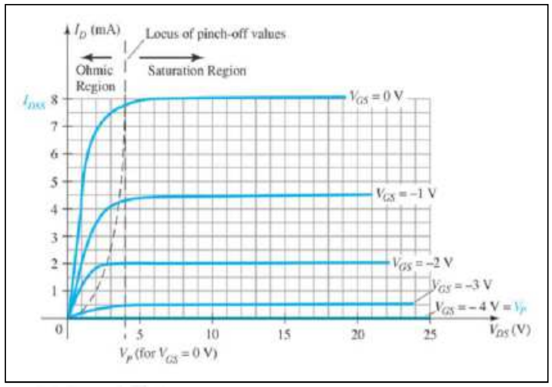
As V_{GS} becomes more negative, the depletion region increases.



JFET Operating Characteristics

As V_{GS} becomes more negative:

- The JFET experiences pinch-off at a lower voltage (V_P).
- I_D decreases ($I_D < I_{DSS}$) even when V_{DS} increases
- I_D eventually drops to 0 A. The value of V_{GS} that causes this to occur is designated $V_{GS(off)}$.



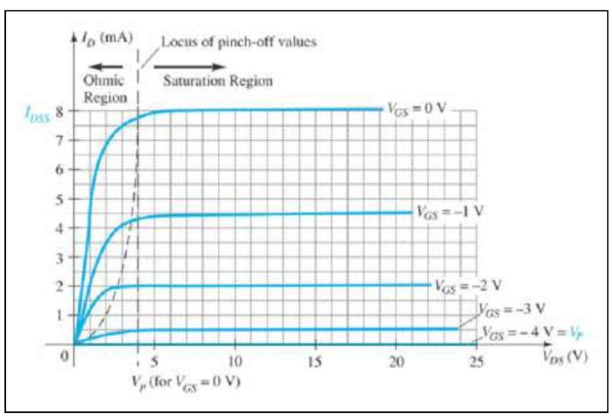
Note that at high levels of V_{DS} the JFET reaches a breakdown situation. I_D increases uncontrollably if $V_{DS} > V_{DSmax}$, and the JFET is likely destroyed.

Voltage-Controlled Resistor

The region to the left of the pinch-off point is called the **ohmic region.**

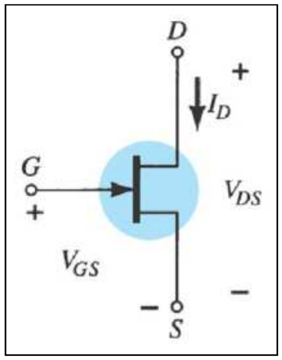
The JFET can be used as a variable resistor, where V_{GS} controls the drain-source resistance (r_d).

$$r_d = \frac{r_o}{\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$



As V_{GS} becomes more negative, the resistance (r_d) increases.

N-Channel JFET Symbol



JFET Transfer Characteristics

JFET input-output transfer characteristics are not as straightforward as they are for a BJT.

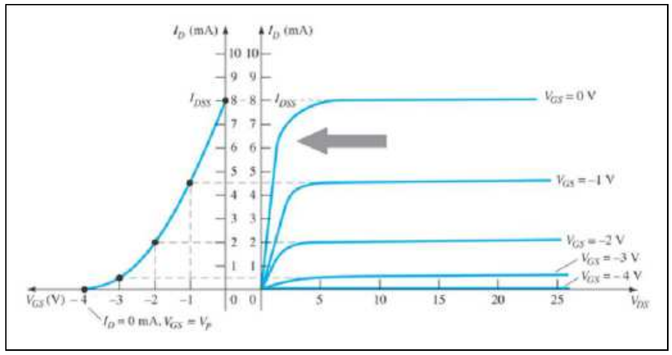
- BJT: β indicates the relationship between I_B (input) and I_C (output).

- JFET: The relationship of V_{GS} (input) and I_D (output) is a little more complicated:

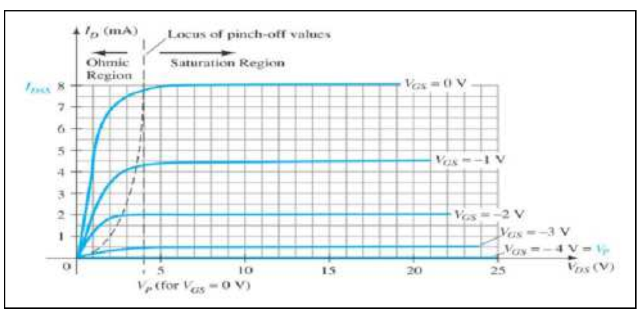
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

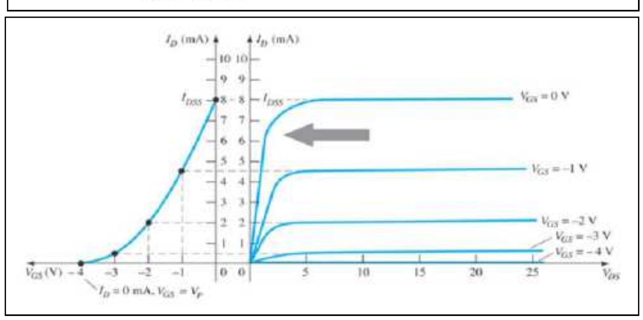
JFET Transfer Curve

This graph shows the value of I_D for a given value of V_{GS}.



Recap of Topic 4 (JFET Drain & Transfer characteristics)





MOSFETs

MOSFETs have characteristics similar to those of JFETs and additional characteristics that make then very useful.

There are two types of MOSFETs:

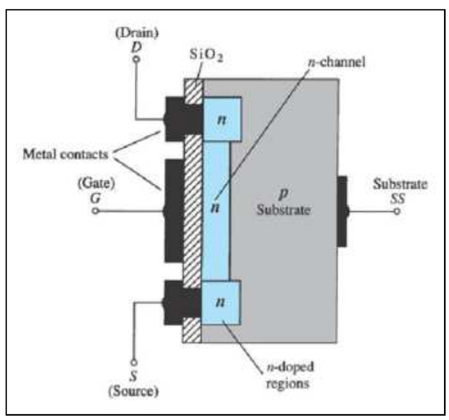
Depletion-Type

Enhancement-Type

Depletion-Type MOSFET Construction

The **Drain (D)** and **Source (S)** connect to the to *n*-type regions. These *n*-typed regions are connected via an *n*-channel. This *n*-channel is connected to the **Gate (G)** via a thin insulating layer of silicon dioxide (SiO_2).

The *n*-type material lies on a *p*-type substrate that may have an additional terminal connection called the **Substrate (SS).**



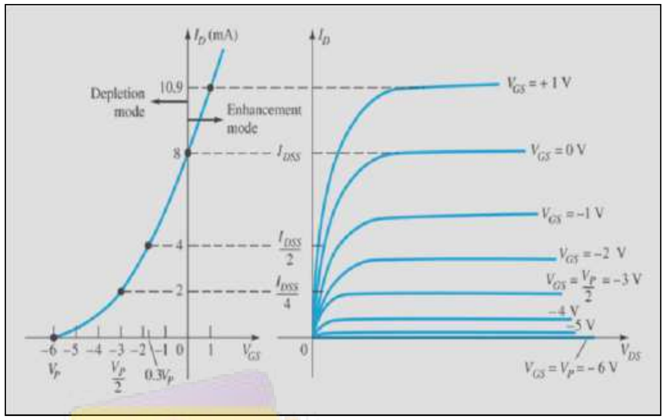
Video

Basic MOSFET Operation

A depletion-type MOSFET can operate in two modes:

Depletion mode

Enhancement mode



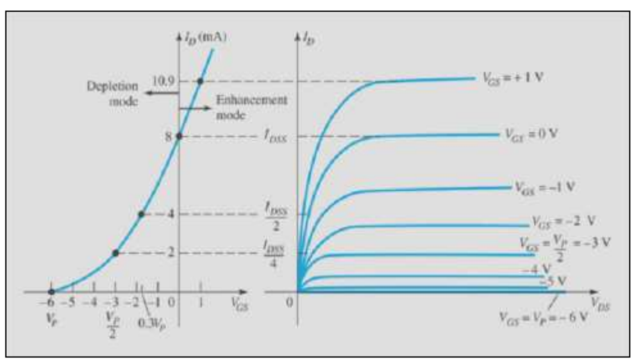
Transfer and Drain characteristics for n-channel

Depletion Mode Operation (D-MOSFET)

The characteristics are similar to a JFET.

When $V_{GS} = 0$ V, $I_D = I_{DSS}$

When $V_{GS} < 0$ V, $I_D < I_{DSS}$



The formula used to plot the transfer curve for a JFET applies to a D-MOSFET as well:

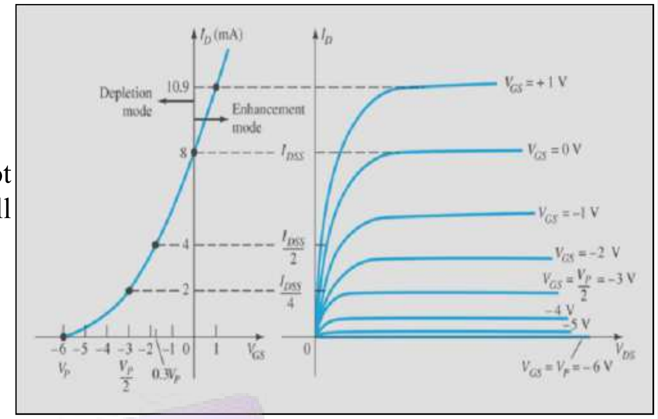
$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

Enhancement Mode Operation (D-MOSFET)

$V_{GS} > 0$ V, I_D increases above I_{DSS} ($I_D > I_{DSS}$)

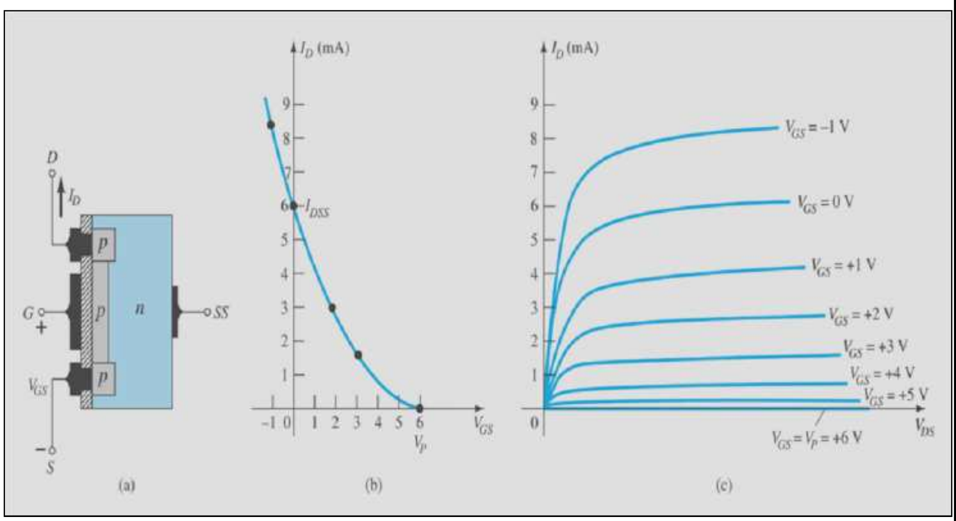
The formula used to plot the transfer curve still applies:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

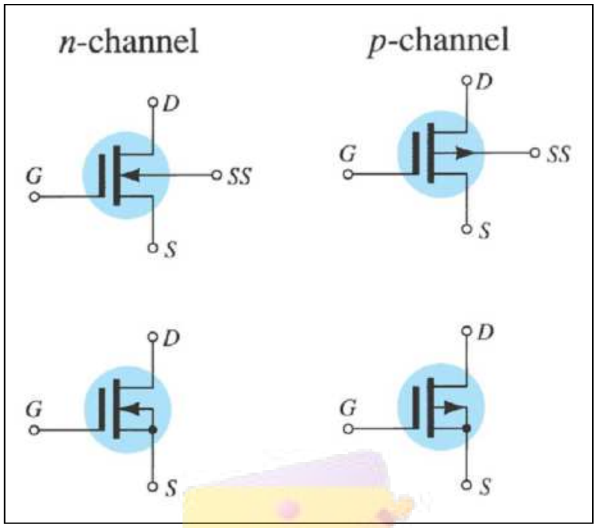


Note that V_{GS} is now positive

p-Channel D-Type MOSFET



D-Type MOSFET Symbols



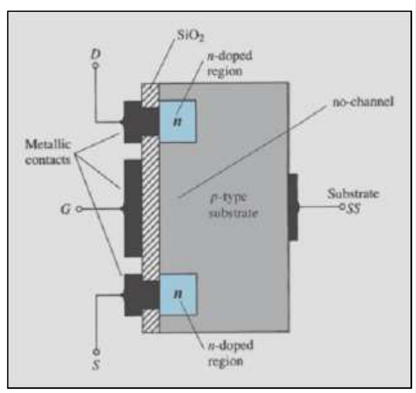
E-Type MOSFET Construction

The **Drain (D)** and **Source (S)** connect to the to *n*-type regions. These *n*-type regions are connected via an induced *n*-channel.

The **Gate (G)** is isolated to the *p*-type substrate via a thin insulating layer of silicon dioxide (SiO_2).

There is no physical channel

p-type substrate has an additional terminal called the **Substrate (SS), always connected to the source terminal.**



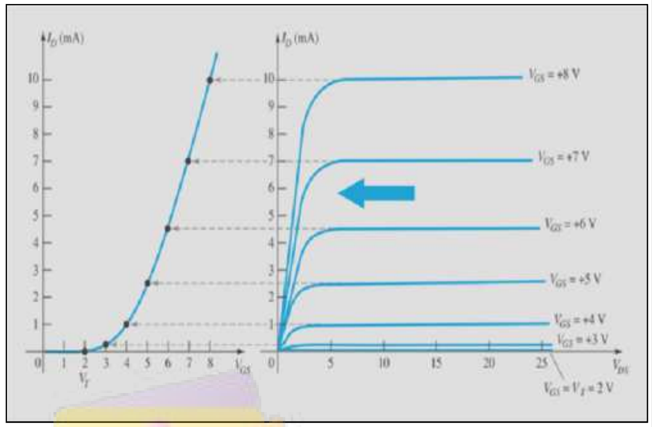
N channel E-MOSFET Operation

The enhancement-type MOSFET (E-MOSFET) operates only in the enhancement mode.

V_{GS} is positive

As V_{GS} increases, I_D increases

As V_{GS} is kept constant and V_{DS} is increased, then I_D saturates (I_{DSS}) and the saturation level (V_{DSsat}) is reached



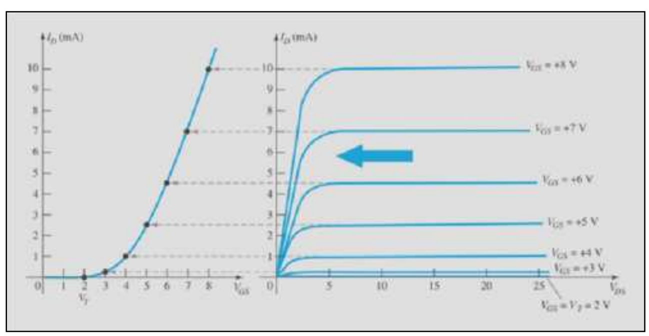
E-Type MOSFET Transfer Curve

To determine I_D given V_{GS}:

$$\boxed{I_D = k(V_{GS} - V_T)^2}$$

For $V_{GS} \geq V_T$

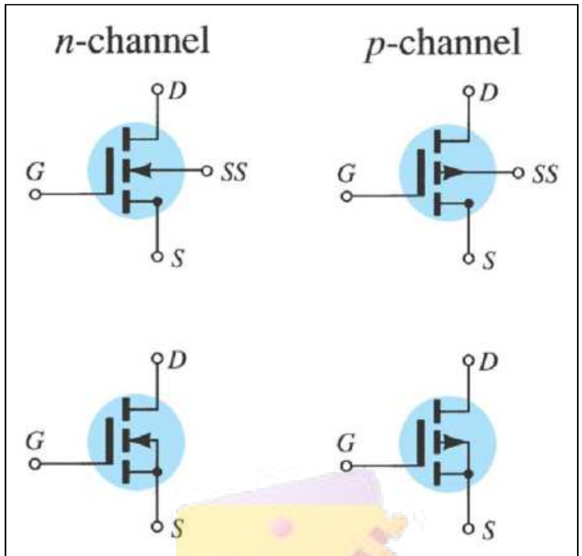
where:
V_T = threshold voltage



V_{DSsat} can be calculated using:

$$\boxed{V_{DSsat} = V_{GS} - V_T}$$

MOSFET Symbols



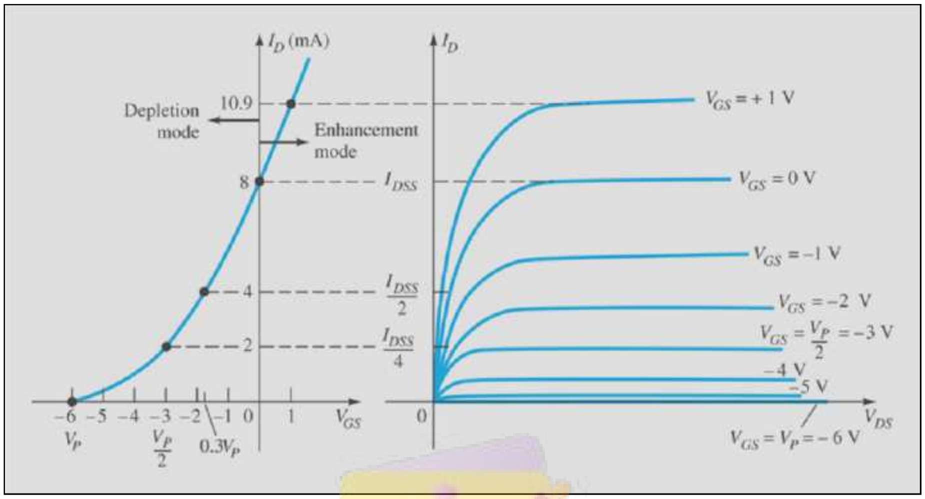
FET Transconductance

Transconductance: The ratio of a change in I_D to the corresponding change in V_{GS} *at constant* V_{DS}

• Transconductance is denoted g_m and given by:

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{\text{Const.}V_{DS}} \qquad g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right]$$

Recap of Topic 5 (MOSFET n channel depletion mode char.)



BJT Transistor Modeling

A model is an equivalent circuit that represents the AC characteristics of the transistor.

A model uses circuit elements that approximate the behavior of the transistor.

There are two models commonly used in small signal AC analysis of a transistor:

r_e model (syllabus)

Hybrid equivalent model

The r_e Transistor Model

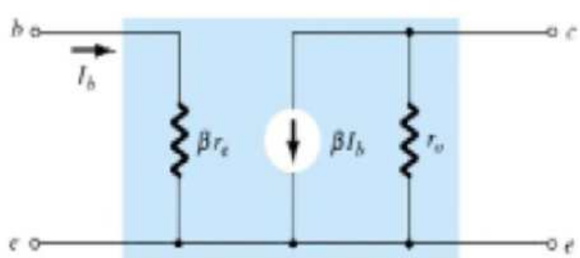
BJTs are basically current-controlled devices; therefore the r_e model uses a diode and a current source to duplicate the behavior of the transistor.

Common-Emitter Configuration

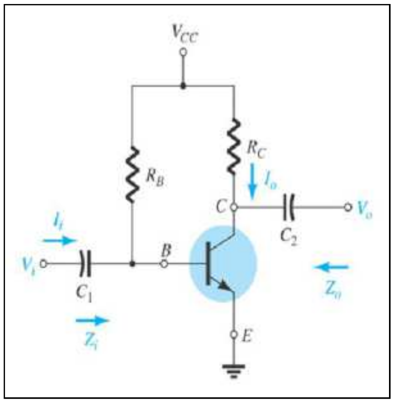
The diode r_e model can be replaced by the resistor r_e.

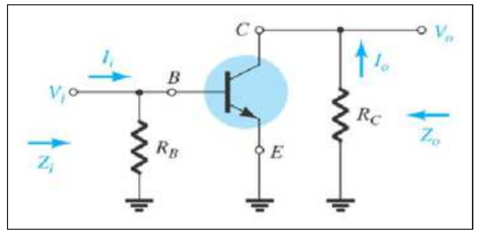
$$I_E = (\beta + 1) I_B \cong \beta I_B$$

$$r_e = \frac{26 \text{ mV}}{I_E}$$

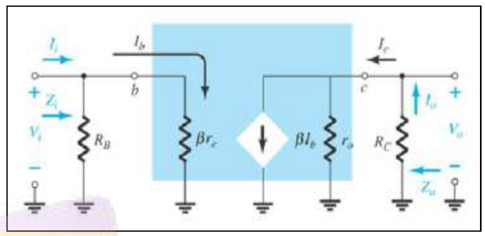


Common-Emitter Fixed-Bias Configuration(Analysis)





AC equivalent



r_e model

Common-Emitter Configuration

Input impedance:

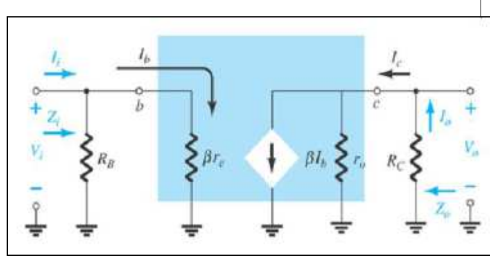
$$\boxed{Z_i = \beta r_e}$$

Output impedance:

$$\boxed{Z_o = r_o \cong \infty \Omega}$$

Voltage gain:

$$\boxed{A_V = -\frac{R_L}{r_e}}$$



r_e model

Common-Emitter Fixed-Bias Calculations

Input impedance:

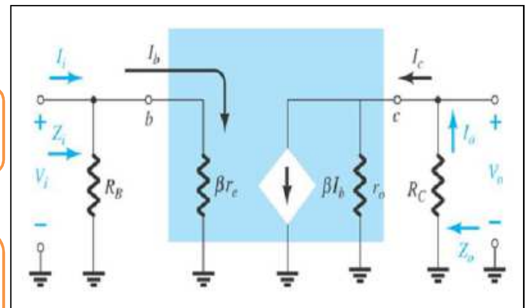
$$Z_i = R_B||\beta|_e$$
$$Z_i \cong \beta r_e \Big|_{R_E \geq 10\beta r_e}$$

Output impedance:

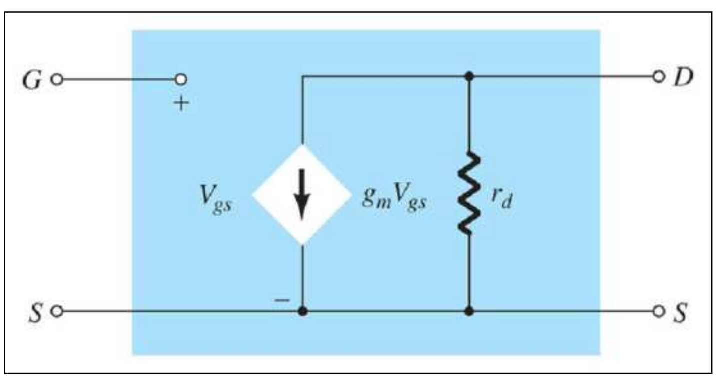
$$Z_o = R_C || r_o$$
$$Z_o \cong R_C \Big|_{r_o \geq 10 R_C}$$

Voltage gain:

$$A_v = \frac{V_o}{V_i} = -\frac{(R_C || r_o)}{r_e}$$
$$A_v = -\frac{R_C}{r_e}\Big|_{r_o \geq 10 R_C}$$



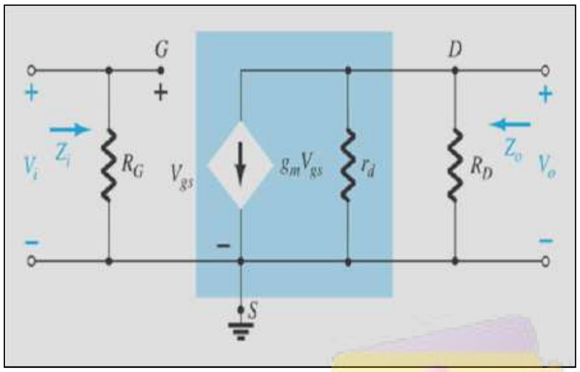
FET AC Equivalent Circuit

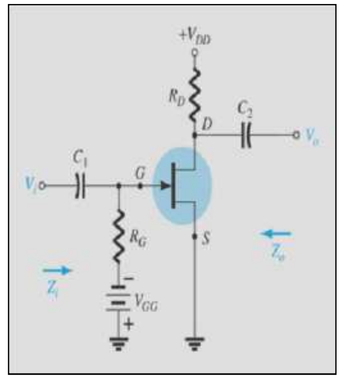


Analysis of Common Source (CS): Fixed-Bias amplifier

The input is applied to the gate and the output is taken from the drain

There is a 180° phase shift between the circuit input and output





Calculations

Input impedance:

$$\boxed{Z_i = R_G}$$

Output impedance:

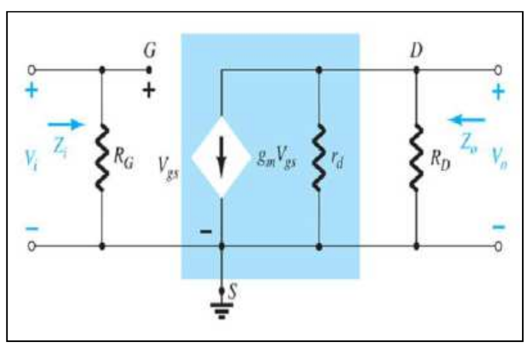
$$Z_o = R_D || r_d$$

$$Z_o \cong R_D \Big|_{r_d \geq 10 R_D}$$

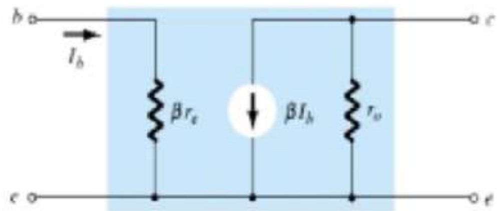
Voltage gain:

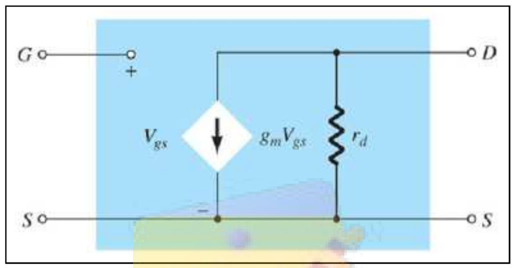
$$A_v = \frac{V_o}{V_i} = -g_m (r_d || R_D)$$

$$A_v = \frac{V_o}{V_i} = -g_m R_D \Big|_{r_d \geq 10 R_D}$$



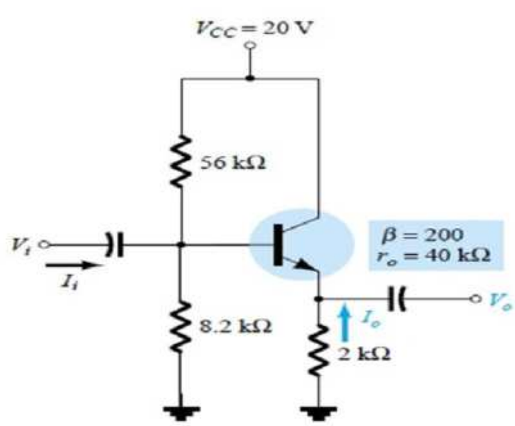
Recap (r_e BJT and FET model)





Problems

- For the voltage divider configuration determine r_e, A_V, Z_{in} and Z_0.



Problems

- Determine Z_i, Z_0 and A_V for the common source configuration if $I_{DSS} = 12$ mA, $V_P = -6V$, and $Y_{os} = 40$ micro Siemens.