Unit-3

4 Nov

FET (field effect Transistor) :- (current is due to majority carriers)
(It is used to amplify weak signals)

Difference b/w BJT & FET :-

1. BJT is bipolar while FET is unipolar
   bipolar indicate that current is due to majority & minority both
   unipolar " " " " majority only
2. BJT is current controlled device while FET is voltage controlled device
3. In case of BJT, $I_C \simeq \beta I_B$ while in the case of FET $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

   (I_{DSS} = saturation current) i.e constant
   (so I_D is controlled by V_{GS})
4. FET has high input impedence generally more than 100 MΩ
   BJT input impedence depend on configuration (generally 1 MΩ)
5. FET is temp stable (parameter doesnot vary with temp)
   and in BJT I_{CO} depend on temp. (10° ↑ in temp double the value of saturation current)
6. FET is smaller in size compared to BJT
7. Low power discipation in FET

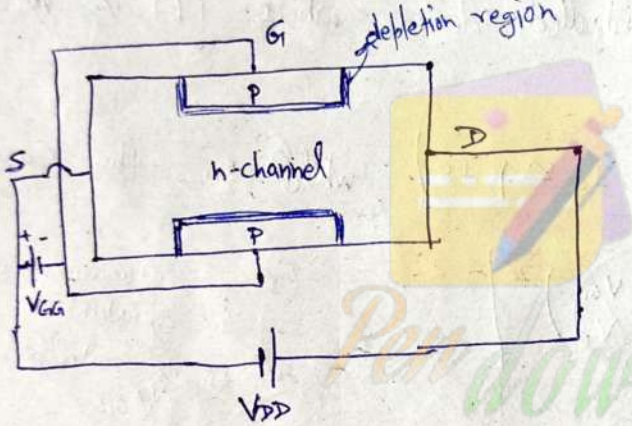
⑦ FET has small gain ~~bound~~ bandwidth product } 2 disadvantages of FET

⑧ slower compared to BJT

⑨ FET are small so can use to make ICs

structure of FET: (2 types ① n-channel ② p-channel)

① n-channel: (majority carriers are e⁻) (value of V_{GS} = -ve)

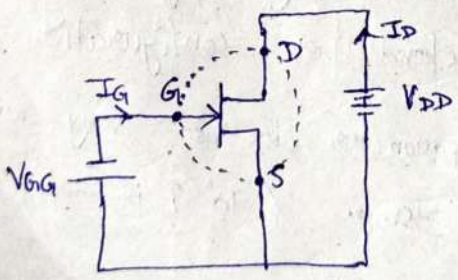


[S = Source
D = drain ~~source~~
G = Gate]

[The channel provide path for e⁻ to flow]

has 3 electrodes

circuit representation -



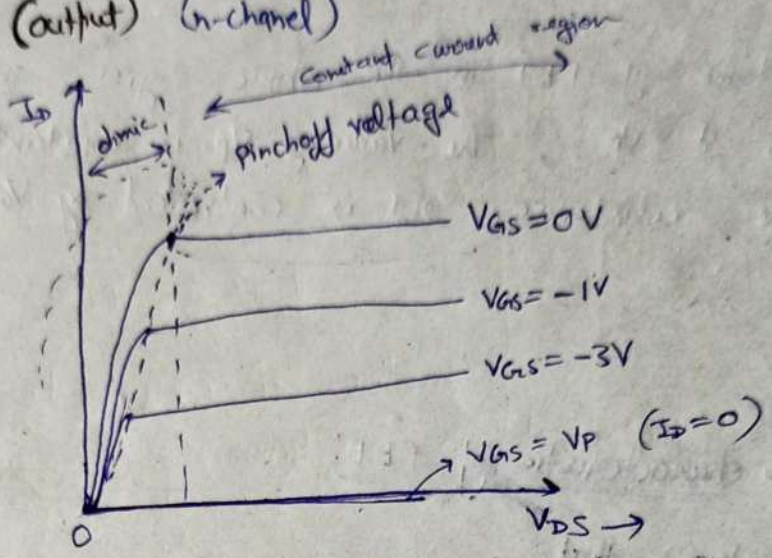
I_D = Drain current
I_S = Source "
I_G = Gate "

at high impedance

$I_G = 0$ (at $Z = \infty$)

(so value of I_G can be ignored)

Characteristics: (output) (n-chanel)



Note:

(1) Area b/w I_D & Pinchoff voltage represent ohmic region

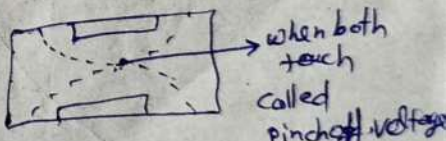
(2) other is constant current region

Conditions to draw Characteristics

(1) $V_{GS}=0$, $V_{GS}=-1V$

(2) vary voltage V_{GG}

on ↑ V_{DS} depletion region (P) ↑ & become very narrow. So current will become constant.



~~Vpos~~

~~Due to property of~~

Properties of FET:

(1) FET can be used as voltage controlled resistor

$$r_d = \frac{r_o}{\left(1-\frac{V_{GS}}{V_P}\right)^2}$$

r_o = value of resistance for $V_{GS}=0$ and r_d is the any point b/w

(2) Resistance of FET in the ohmic region is controlled by V_{GS} & V_p, The value of V_p is constant hence the resistance rd is controlled by V_{GS}.

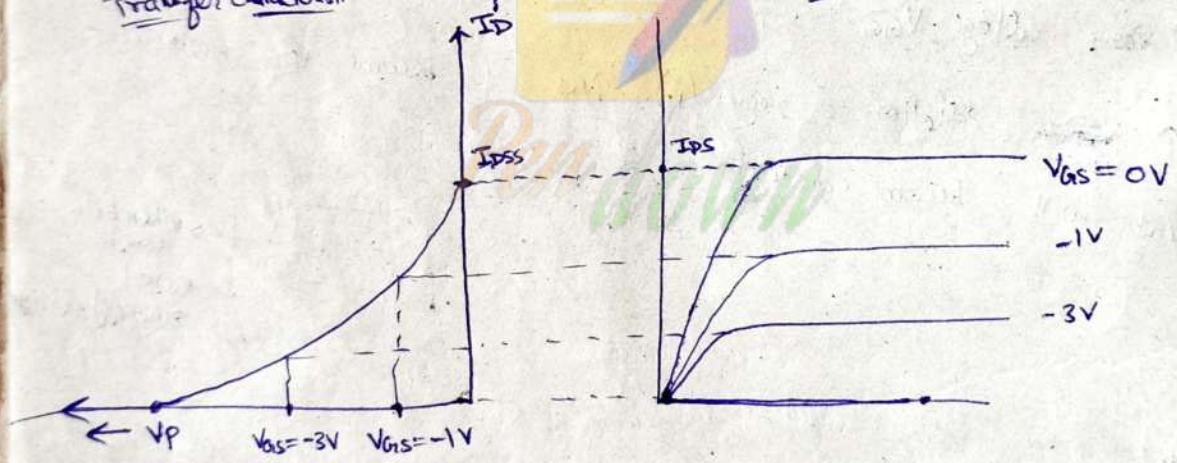
Transfer characteristic of FET:

As we know that

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

when $V_{GS} = 0$, $I_D = I_{DSS}$

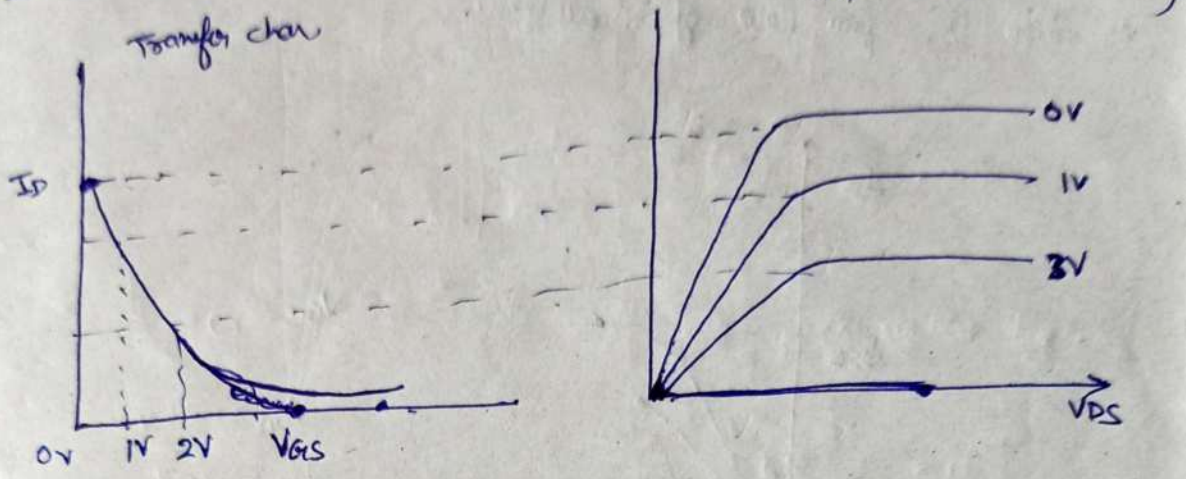
Transfer characteristic



output characteristic

② P-channel : V_{GS} = +ve

(P-channel output characteristic)



Different structures of FET :-

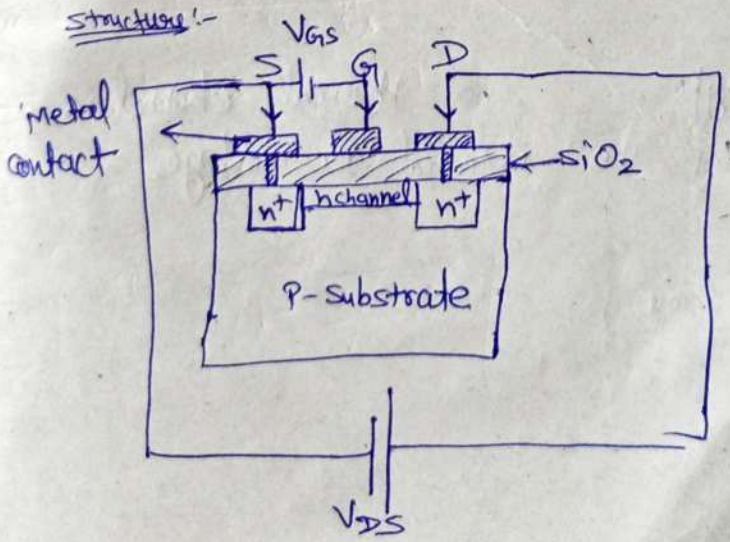
① JFET
② MOSFET
③ MOS, (PMOS, CMOS, NMOS)

15 Nov

② MOSFET :- It is of 2 types → ① Depletion
② Enhancement

① Depletion (n-channel) type MOSFET :-

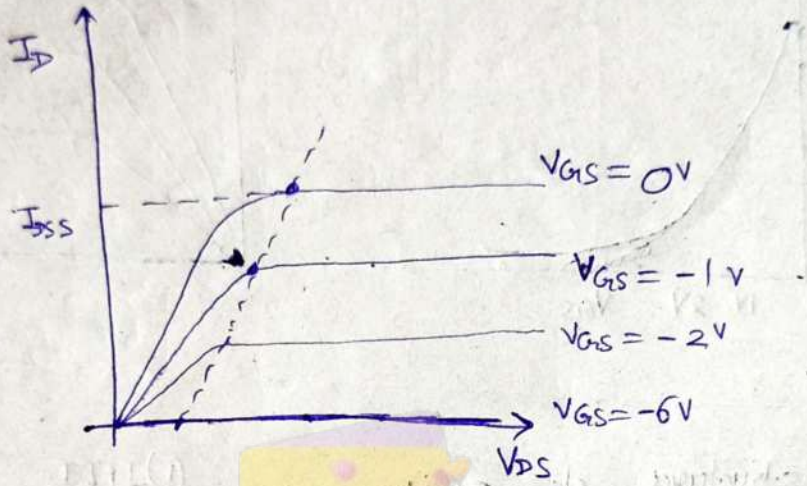
Structure :-



n^+ = doping conc of n is very high

Gate is totally insulated from the channel so gate current = 0

when $V_{GS} = 0$, positive voltage V_{DS} attack the e^- from channel. so there is free flow of electrons.



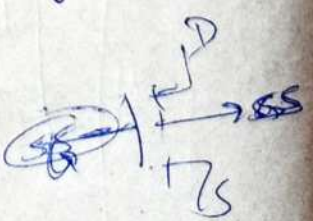
at $V_{GS} = -6V$, current $I_D = 0$

Negative potential on the gate terminal generate the pressure on electron toward the substract and holes from the p-side is attracted towards the n-channel.

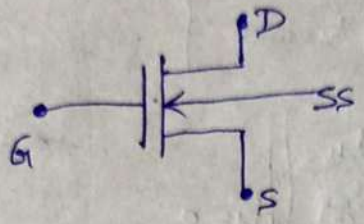
similarly in case of enhancement type, the channel is enhanced (there is no physical n-channel available) by applying external DC voltage.

(2) In case of enhanced type, no physical channel is available it is generated by the external DC voltage.

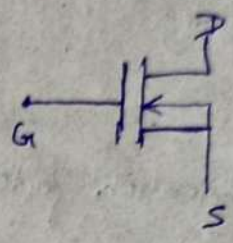
diagram & graph same



Symbolic representation of ~~Hexfet~~ MOSFET:-

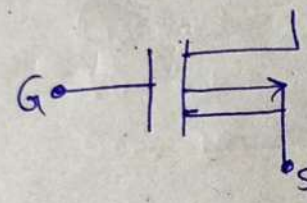


or



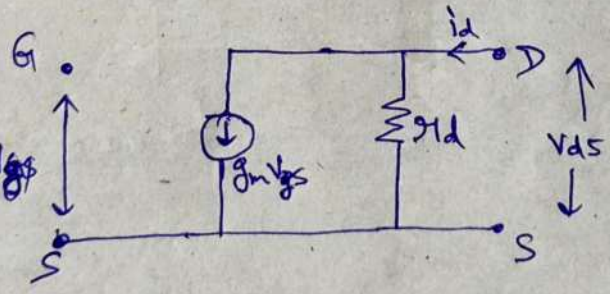
(n-channel)

direction of arrow towards gate in n-channel & outside gate in p-channel;



(p-channel)

FET Small Signal Model: Low signal or Small ~~sign~~ frequency signal Model of FET



$I_G = 0$ because input impedence is ∞ in FET

(low frequency model)

$$i_g = g_m V_{gs} + \frac{V_{ds}}{r_d}$$

$$g_m = \left.\frac{i_d}{V_{gs}}\right|_{V_{ds}=\text{const}}$$ (gm i.e. transconductance)

drain resistance:- $r_d = \left.\frac{V_{ds}}{i_d}\right|_{V_{GS}=\text{const}}$

amplification factor (μ) $= -\left.\frac{V_{ds}}{V_{gs}}\right|_{i_d=0}$ ~~i/p o/p~~

*output voltage is 180° phase shift with the input voltage.

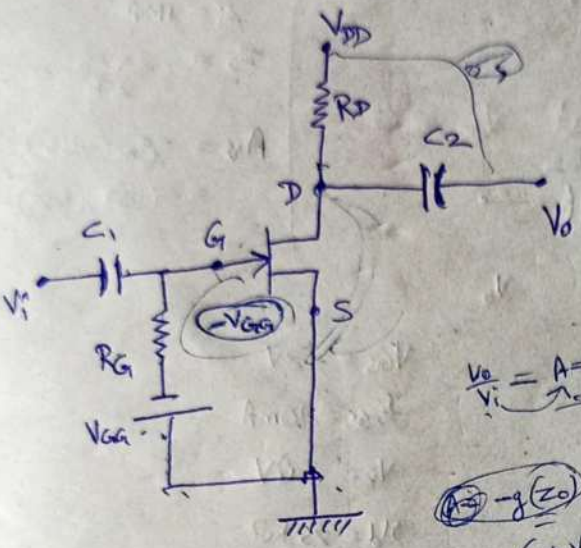
$\mu = g_m r_d$

* FET show the negative temp coefficient of g_m and i_{gs} due to that electron mobility decreases with temperature but in case of BJT it show +ve temp coeff. there is condition of thermal runaway in BJT

There is no condition of thermal runaway in FET.

Q-factor
operating point

FET biasing :-



$\frac{V_o}{V_i} = A = V_c$

$A = -g(z_o)$

$g = g_o\left(1 + \frac{V_{GS}}{V_p}\right)$

for DC analysis capacitors are open and for AC analysis they should be sorted.

for DC analysis, $I_G = 0$ because input impedance of FET = ∞ .

$V_{GS} = -V_{GG}$

$V_{DD} = I_D R_D + V_{DS}$

Q)

Let $V_{GG} = 2V$, $I_{DSS} = 10mA$, $V_e = -8V$

$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_e}\right)^2$

for DC $V_{GS} = -V_{GG}$

$V_{DS} = -V_{GG}$

$I_D = 10mA\left(1 + \frac{2}{-8}\right)^2$

$= 10mA\left(1 - 0.25\right)^2$

$= 10mA\left(0.75\right)^2 = 5.63\,mA$

$V_{DD} = I_D R_D + V_{DS}$ (Let $V_{DD} = 16V$) given

($R_D = 2K\Omega$) given

$V_{DS} = V_{DD} - I_D R_D$

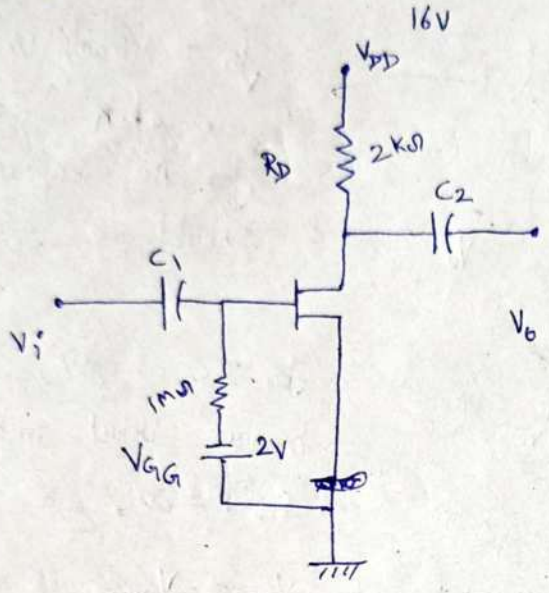
$= 16 - 5.63 \times 2$

$V_{DS} = 4.7V$ Ans

$V_{DS} = V_D - V_S \to 0$

$V_{DS} = V_D = 4.7V$

16 Nov



$Z_i = 1M\Omega$

$Z_o = \frac{2 \times 25}{27} = 1.85k\Omega$

$A_v = -g_m(1.85)$

$= -(1.87)(1.85) = -3.45$

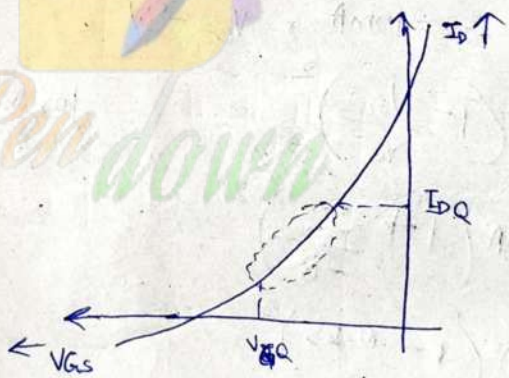
$V_{GS} = -2V$

$I_{DSS} = 10mA$

$V_p = -8V$

$r_d = 25k\Omega$

Transfer characteristics:



V_{GSQ}, I_{DQ}

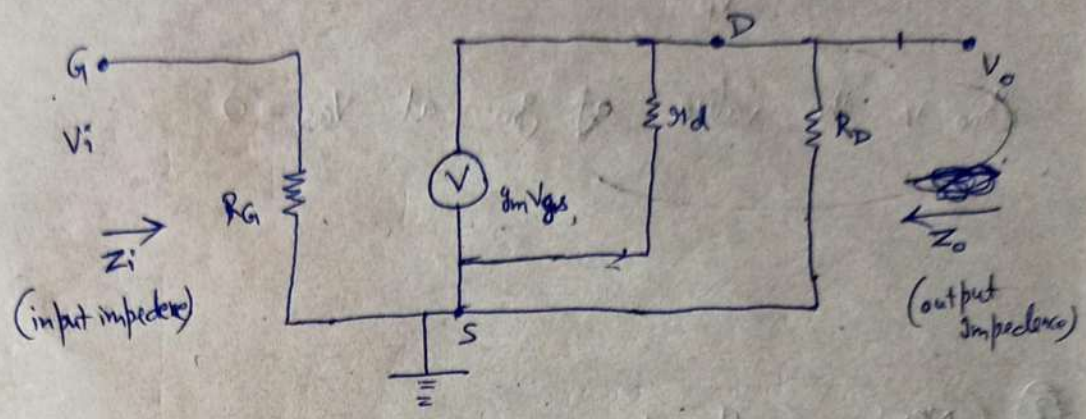
$$g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_p}\right) = g_{mo}\left(1 - \frac{(-2)}{-8}\right)$$

$$= g_{mo}\left(1 - \frac{1}{4}\right)$$

$$g_m = 0.75\, g_{mo}$$

$$g_m = 1.087$$

AC analysis:



$Z_i = ?$
$Z_o = ?$
$A_v = ?$

① Input Impedence $(Z_i) = R_G$

② output Impedence $(Z_o) = r_d \,||\, R_d$

③ $V_o = -g_m V_{gs} \,(r_d \,||\, R_d)$

④ $V_i = V_{gs} = -V_{GG}$

⑤ $V_o = -g_m V_i \,(r_d \,||\, R_d)$

$\frac{V_o}{V_i} = -g_m \,(r_d \,||\, R_d)$ (it is voltage gain A_v)

So $\boxed{A_v = -g_m \,(r_d \,||\, R_d)}$

⑥ if $r_d \geq 10 R_d$

$\boxed{A_v = -g_m R_d}$

$A = -g\,(Z_o)$

$\frac{V_o}{V_i} = -g\,(Z_o)$

$V_o = -g\,(Z_o)\,V_i$

⑦ $\mu = g_m r_d$ (amplification factor)

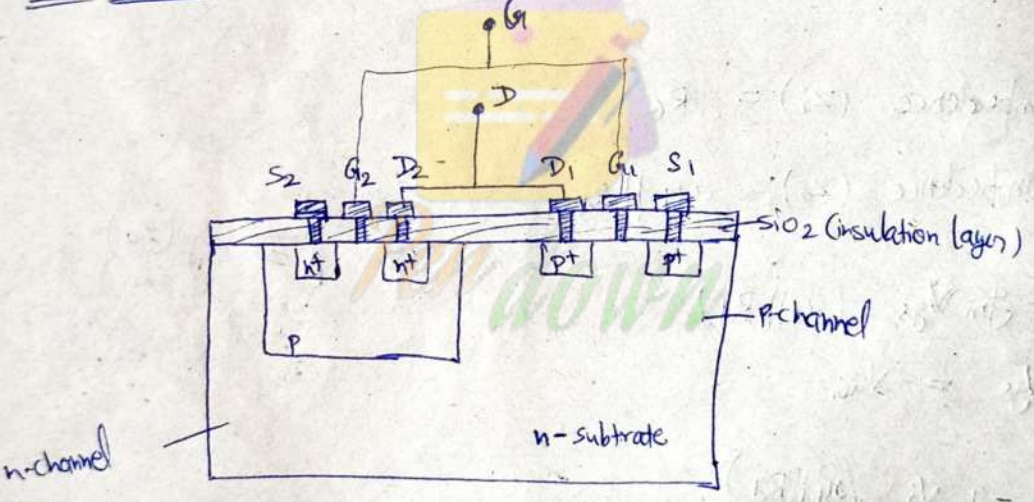
⑧ $g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right) = \frac{2}{|V_P|}\left(I_{DS} \times I_{DSS}\right)^{1/2}$

(2) $g_{mo} = \frac{-2 I_{DSS}}{V_P}$

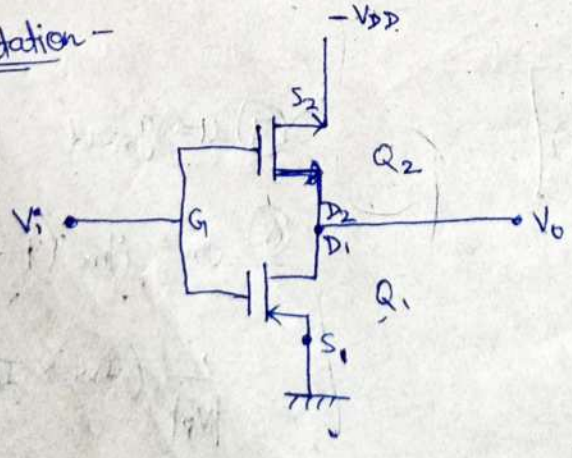
g_{mo} is the value of g_m at $V_{GS} = 0$

(3) CMOS:- (Complementary MOS):

* basic structure:-



* logical representation -

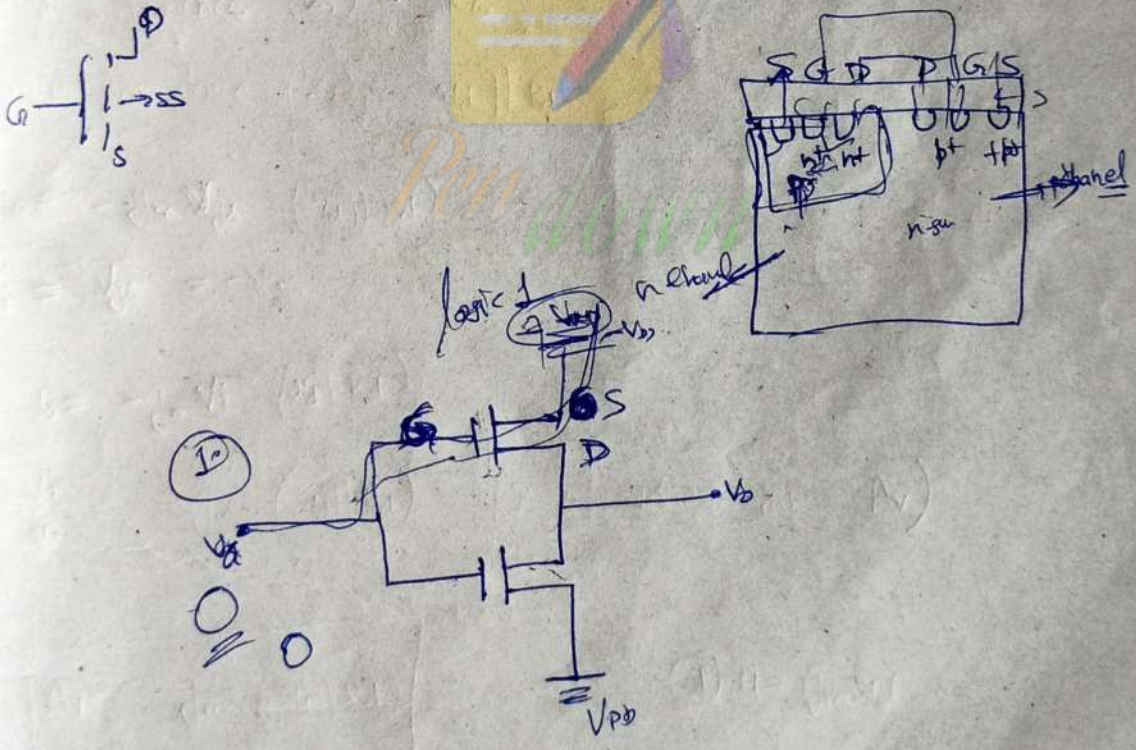


(+ve)
logic=1 = +5V
logic=0 = 0V

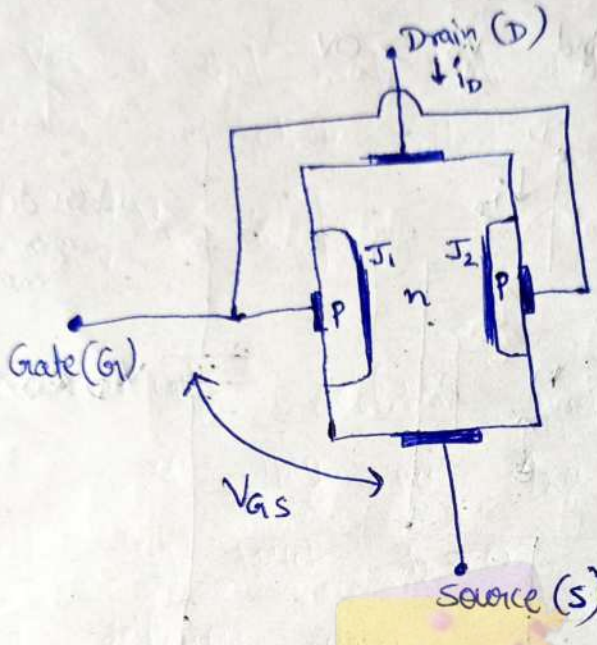
(-ve)
logic=1 = -5V
logic=0 = 0V

① $V_i = -V_{DD}$ (logic = 1) then Q_1 = ON, Q_2 = OFF. $V_o = 0V$ (logic = 0)

② $V_i = 0V$ (logic = 0) then Q_1 = OFF, Q_2 = ON. $V_o = -V_{DD}$ (logic = 1)



JFET



(1) 2 Junction (J_1 & J_2)
so 2 depletion region

(2) on ↑ width of depletion region, Conduction ↓ because width of n-channel will reduced

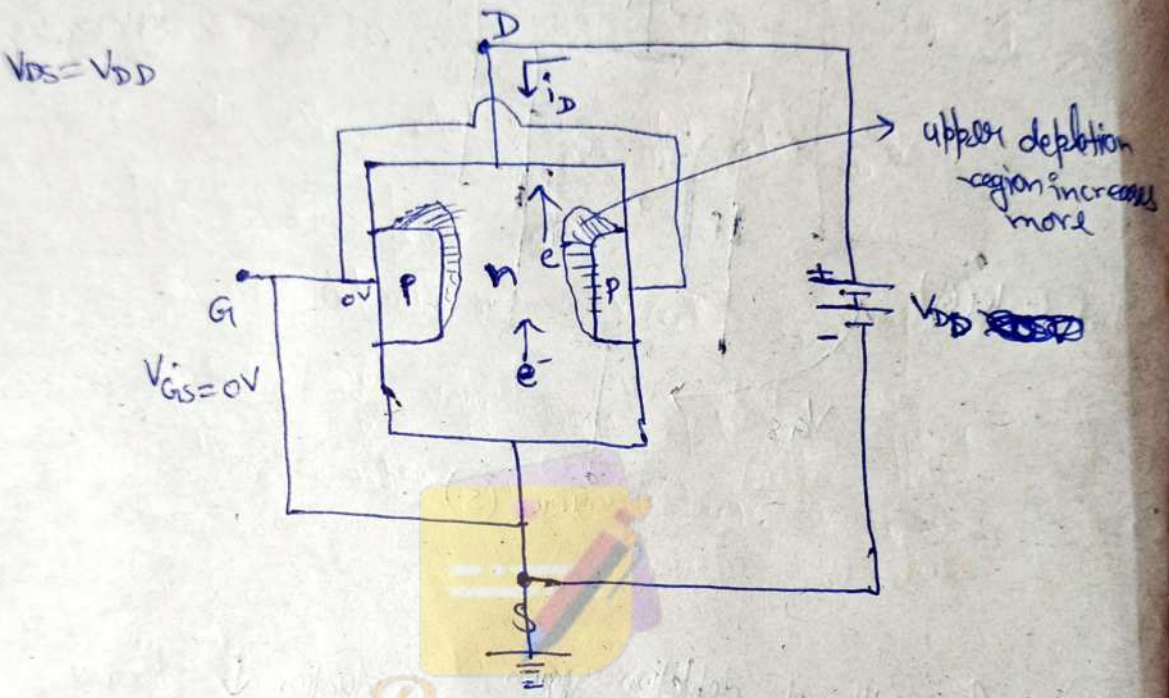
(3) we Can Control the width of depletion region by Gate terminal.

V_{GS} will Control i_D

(4) Cause of e^- flow = V_{DS}

★ Working of JFET:

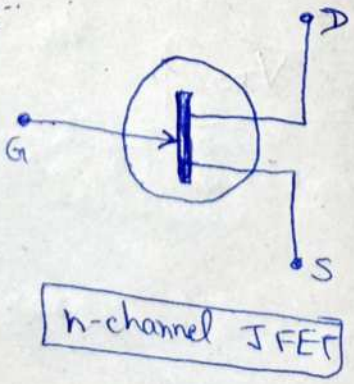
Case 1:- $V_{GS} = 0V$ And $V_{DS} > 0V$



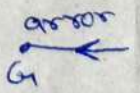
① upper depletion region increases more because potential at V_D = max & decreasing coming to end & $V_S = 0V$

so $V \uparrow \Rightarrow$ dep region $\uparrow$

② Symbol:



n-channel JFET



p-channel JFET

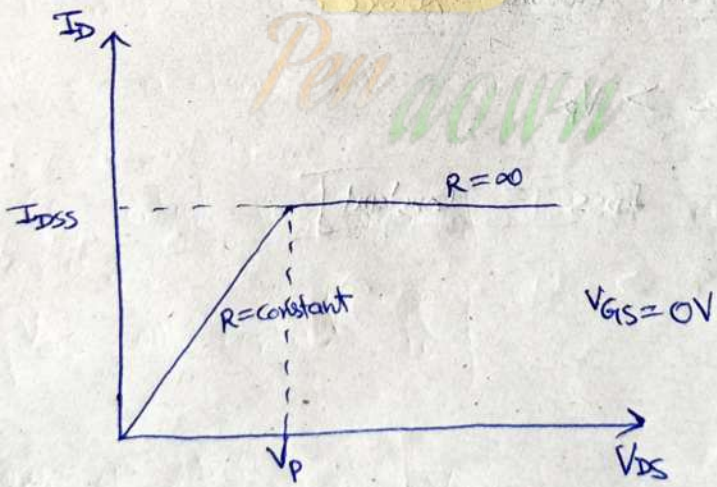
★ Pinch off - Voltage -

when V_{DS} is that much high that 2 depletion regions touches each other called pinch off voltage (V_{DS})

$$\boxed{V_P = V_{DS}}$$

but Practically depletion regions cannot touch each other as they are ↑Res due to I_D and if they touch $I_D = 0$ results in destruction of depletion region

★ $V_{GS} = 0V$



I_{DSS} ↑ = max^m drain Current when $\boxed{V_{GS} = 0V}$ and $\boxed{V_{DS} > |V_P|}$

this the Current from Drain to Source so (IDSS)

Q) When $V_{DS} > V_p$ what is effect of Depletion region?

Ans) Depletion region on top will not ↑ as it cannot touch but at bottom it can ↑.

Q) When $V_{DS} > V_p$ what is effect at I_D?

Ans) as $I_D = I_{DSS}$

& Current will not exceed I_{DSS}

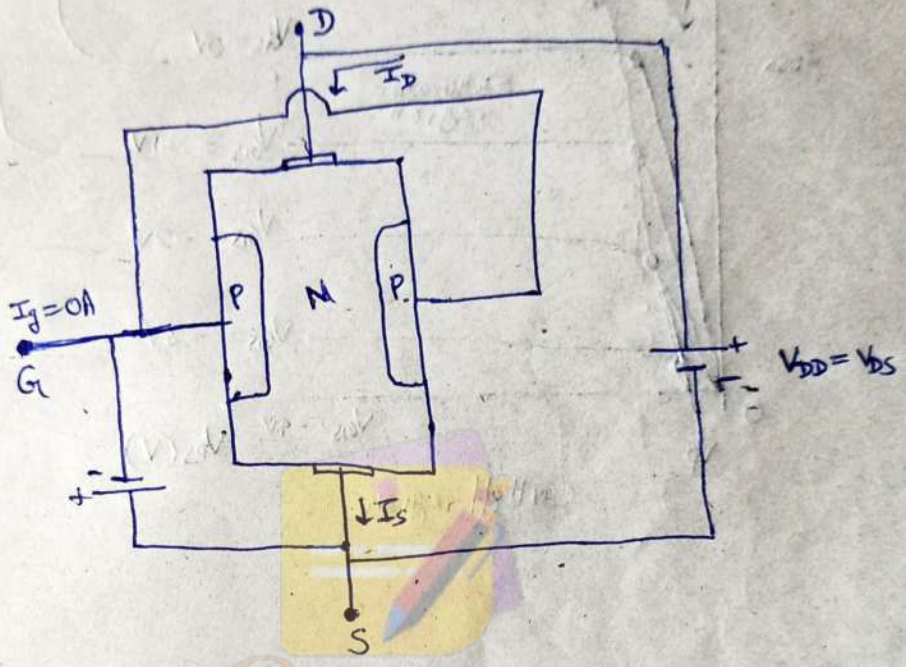
but if very large potential applied, the Junction will breakdown as $I_D >> I_{DSS}$

★ JFET as Constant Current source :-

when $V_{DS} > V_p$

$I_D = I_{DSS} = \text{Constant}$

Case 2:- $V_{GS} < 0V$ and $V_{DS} > 0V$



(1) ☆ To ↑ width of depletion region V_{DS} ↓ & make more -ve

(2) width of depletion region ↑ as reverse biased.

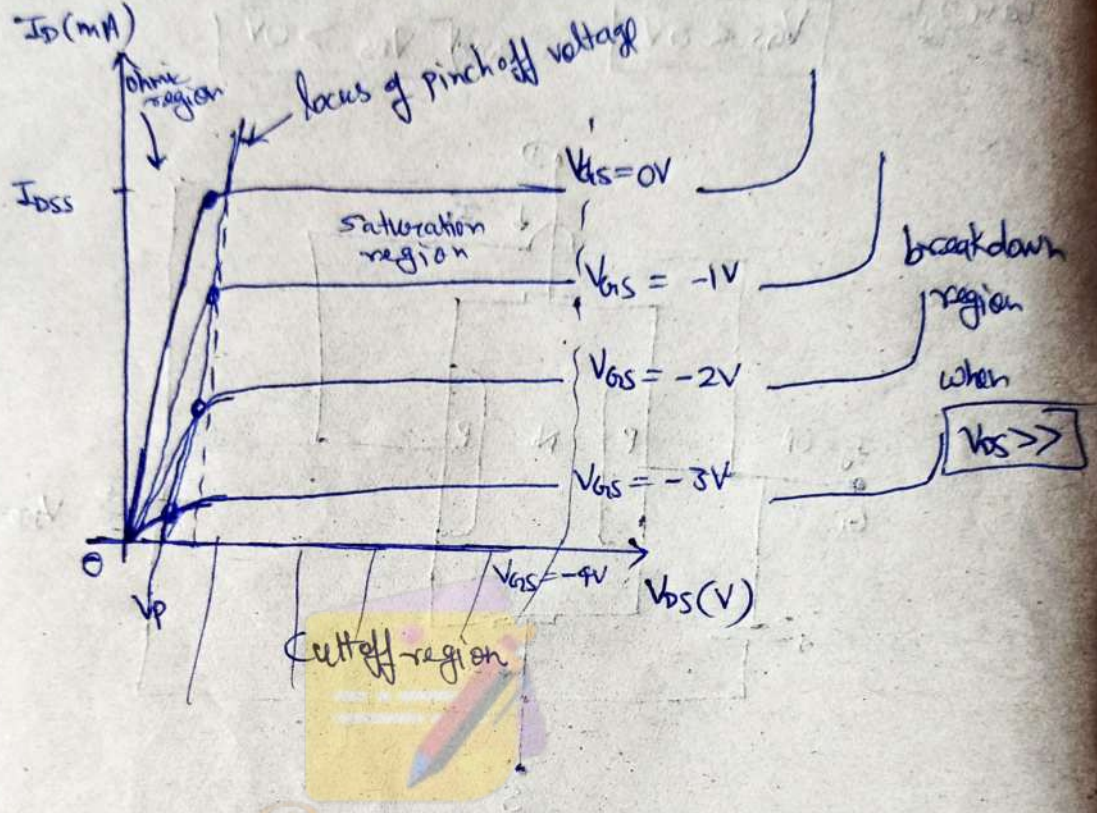
(3)

(4)

Note:- Pinchoff voltage of case (i) > Pinchoff voltage of case (ii)

☆ Saturation Condition- when I_D becomes constant even when on ↑ V_{DS}.

Output / Drain characteristic of JFET:



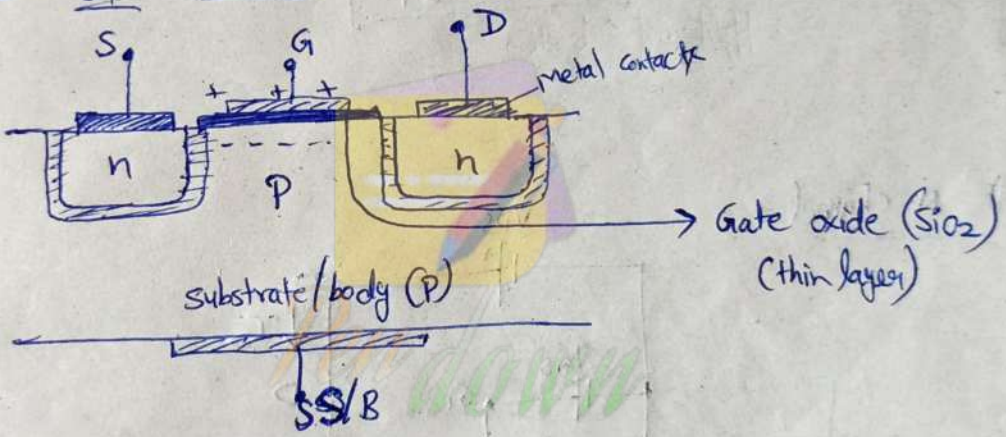
MOSFET

[Metal oxide semi conductor field Effect Transistor]

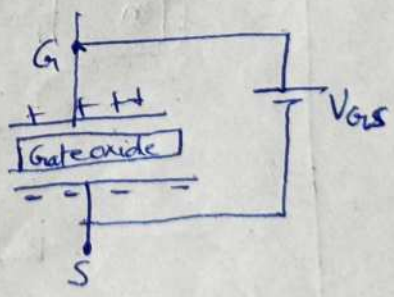
(1) Depletion type MOSFET
[There is a channel b/w drain & source]

(2) Enhancement type MOSFET
[There is no channel b/w Drain & source]

(2) Enhancement type MOSFET :-



n-type



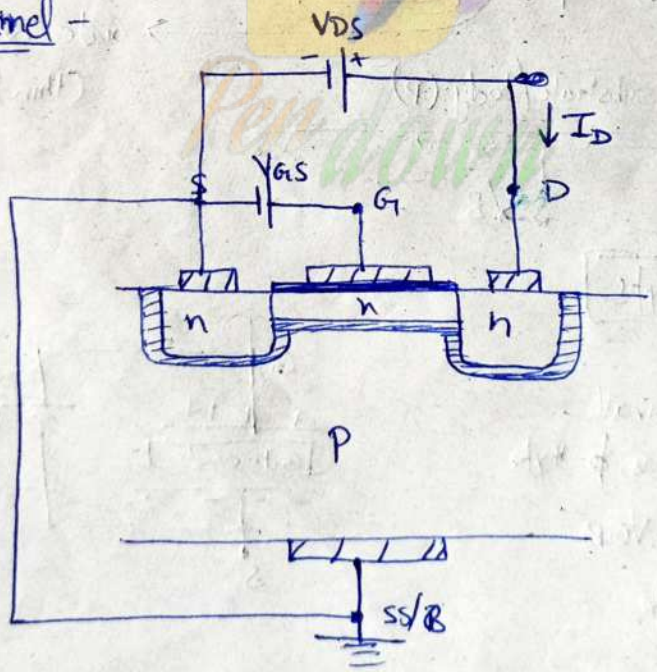
Working when V_{GS} is small
Capacitor act as p-type
but on ↑ V_{GS}
becomes n type
This process is known as inversion
so a channel will form b/w source and drain

☆ Source and substrate are put at same potential internally connected so we get 3 terminals

Threshold voltage : The voltage that results in significant amount of current to flow from source to Drain. is called V_T.
and the current is called drain current I_D.

☆ when $V_{GS} > V_T \Rightarrow I_D \uparrow$

N-channel -



Case (i) $V_{GS} = 0V$

then $V_{GS} = V_{GD}$ width of depletion remains uniform

Case (ii)

Let $V_T = 1V$

$V_{GS} = 2V = V_{GD}$

as $V_{GS} > V_T$

width of depletion region ↑ses

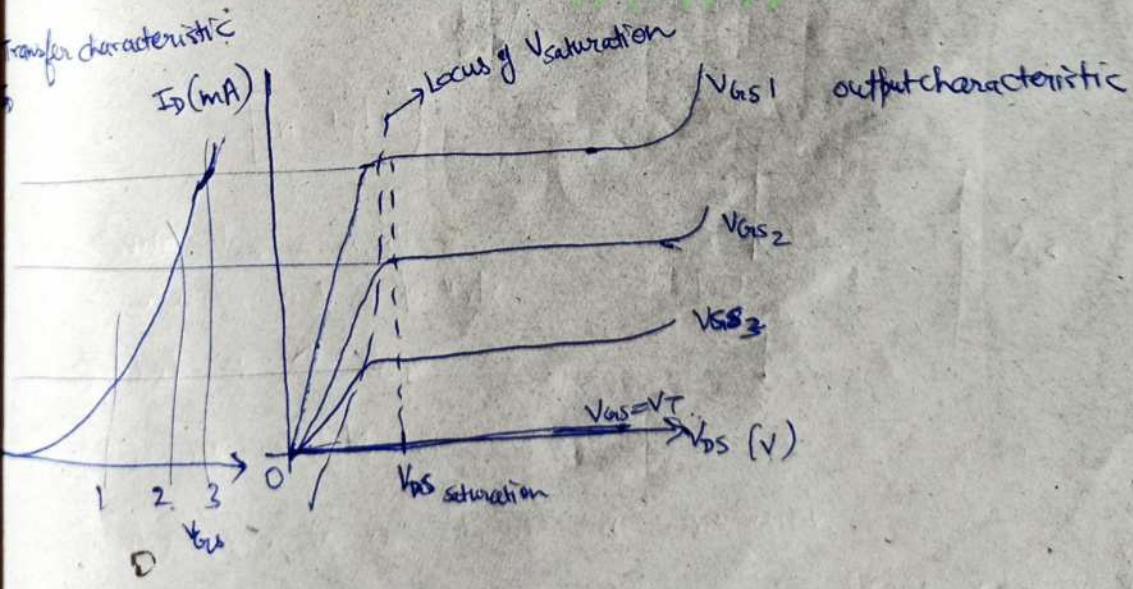
Case (iii)

$V_{DS} = V_{GS} - V_T$

$\boxed{V_{GD} = V_T}$

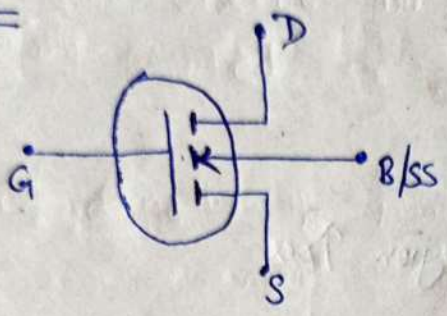
I_D try to become zero but will not zero Called pinchoff.

Drain & Transfer Characteristic of MOSFET -

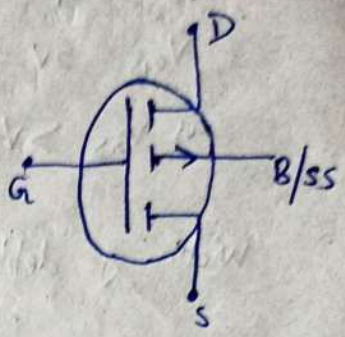


$\boxed{V_{eff} = V_{GS} - V_T}$

Symbol:-

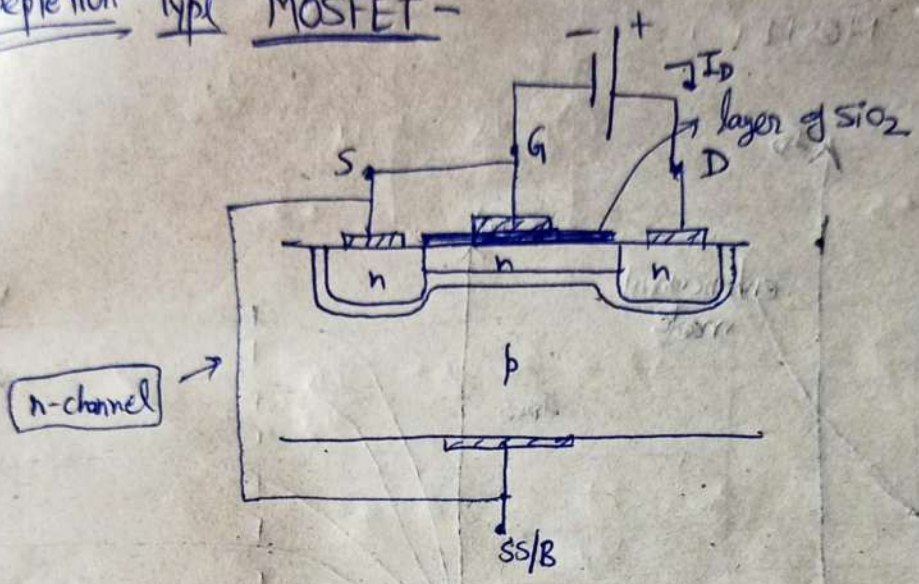


n-channel



p-channel

① Depletion Type MOSFET -



① due to SiO_2, input impedenze of mosfet is v. high

② S and B terminal connected internally

③ As here n-channel is present so $V_{GS} = 0$ possible.

④ As $V_{DS} \uparrow \Rightarrow I_D \uparrow$ but after sometime I_D = Constant because as D terminal becomes more +ve and at junction reverse biasing will ↑ ⇒ width of depletion region will increase. So the channel becomes Narrow so I_D becomes Constant

I_{DSS} = max^m depletion/drain current

Note!: for JFET $V_{GS} \leq 0V$ so $I_{DSS} = I_D$ = max^m current

for MOSFET V_{GS} can be +ve $I_{DSS} = I_D$ & more compossible

Drain & Transfer characteristic of Depletion type MOSFET :-