HIGHEST EFFICIENCY AND SUPER QUALITY AUDIO AMPLIFIER USING MOS POWER FETS IN CLASS G OPERATION

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ABSTRACT

A Class "G" audio power amplifier has achieved a rated continuous output power of 200 watts and peak power of 400 watts. This power amplifier produced no more than 0.01 per cent total harmonic distortion at 20 kHz and 200 watts by using Power MOS FETs in its output stage.

In the worst case the effective efficiency of the amplifier has been measured as approximately 55 per cent at 1/3 the rated power. This paper is concerned with the causes of switching distortion inherent in the Class-G amplifier and several approaches to reducing the switching distortion by using Power MOS FETs.

1. INTRODUCTION

In the past few years there has been growing consumer demand for audio amplifiers with increased power output. This is due in a large part to the advances in recording technique which has provided consumers with records and tapes offering increased dynamic range as well as the growing popularity of bookshelf-type speakers which are not very efficient.

However, as the power rating of audio amplifiers is increased, these components must not only provide the physixal capacity for increased power supply but also larger heat sinks as well.

There have so far been several attempts to reduce heat dissipation from audio and RF tuned power amplifiers by enhancing output stage efficiency. However, those attempts have not necessarily been successful in producing audio power amplifiers which are commercially viable because they had relatively poor signal-to-noise and THD ratios.

As one of the approaches to this generally incompatible requirement for higher efficiency and improved quality in an audio power amplifier, we developed a special power output circuit consisting of stacked 2 Class B system in 1976. This system was referred to as Class "G" operation.4)

The difficulty we encountered in developing this Class-G amplifier was how to reduce switching distortion which occurs when two sets of output transistors are switched from one to another. For the '76 model, the problem was settled by using high-speed epitaxial transistors and Au-doped diodes in its output stage and by making some minor circuit rearrangements.

We introduced a new power element, MOS FET as the output element which guarantees its full power output and high quality performance up to 100 kHz at the power level of several hundred watts, in 1977.⁵⁾

This year we combined power MOS FET with Class-G operation.

In this paper, we analize the origin and causes of switching distortion unique to the Class-G amplifier circuit, and describe the 200 watts Class-G amplifier, using Power MOS FETs in its output stage.

2. BASIC APPROACH TO IMPROVE EFFICIENCY

It is a general requirement for audio power amplifiers to deliver a continuous output 10 to 20 times as large as its mean output power level, because of the increased dynamic range of musical signals. Viewed from the level distribution of musical signals, the effective output power of an amplifier, which has a rated output power of 100 watts, ranges between no more than 5 watts and 10 watts, when the amplifier is carefully set to avoid clipping in reproducing any musical program. And it was found that the portion of the total period during which the output power of the amplifier exceeds 25 watts is only 1 to 2 per cent of the total time in musical reproduction. This seems quite inefficient. The efficiency of a Class-B amplifier decreases as the effective-output/rated-output power ratio decreases, as seen in Figure 1.

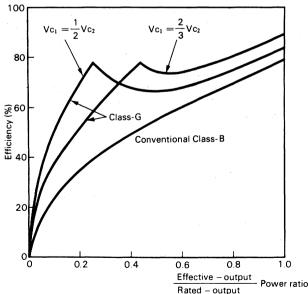


Fig. 1 Power efficiency

According to our calculations the average efficiency is approximately 15 per cent when reproducing an musical program.

Figure 2 illustrates the operating principle of our high-efficiency output circuit. In the Figure, the lower voltage source may be switched in when the output power is small; and when the output power is large, the higher voltage source may be switched in, thus the power loss in the transistors is greatly reduced. The efficiency would be further improved if multiple voltage sources were to be dynamically switched in according to the input signal levels.

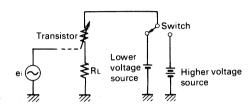


Fig. 2 Principle of operation

One measure to make possible dynamical switching of these voltage sources would be the use of transistor switches supported by the Schmitt trigger circuit which detects the switching threshold levels. However, this approach has the crucial drawback of switching delay and is not suitable for high-quality audio applications. Accordingly we electrically stacked two sets of output transistors one above the other and allowed them to operate as switches for this purpose. Figure 3 shows the basic circuit of the Class-G amplifier. While the amplitude of input voltage ei is smaller than collector voltage Vc1, transistor Q2 is cut off with its base-emitter being reversely biased. When ei exceeds Vc1, Q2 is turned on with its base-emitter diode being forward biased; and the collector current is supplied from the higher voltage source

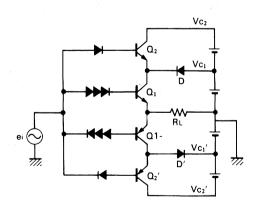


Fig. 3 Basic circuit for the Class-G amplifier

 $V_{\rm C2}$ At the same time, diode D is reversely biased and cuts off the current from the lower voltage source $V_{\rm C1}$. Also, the diodes connected in series in Q's base maintains the voltage across the collector and emitter of Q_1 at the equivalent voltage of the two forward-biased diodes, preventing Q_1 from saturation.

The theoretical efficiency profiles of the Class-G amplifier are also shown in Figure 1. The efficiency curves differ depending on the voltage ratios between the two different voltage sources. As voltage $V_{\rm Cl}$ is lowerd, efficiency in the smaller output region increases, while that in the larger output region decreases. A higher $V_{\rm Cl}$ may be more advantageous when a larger continuous power is required; and a lower $V_{\rm Cl}$ may be more desirable when a smaller mean power is required.

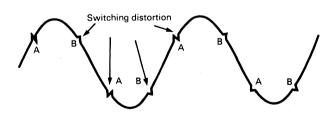
It was found that the optimal supply voltage ratio $(V_{C1}: V_{C2})$, providing the maximum mean efficiency for music reproduction, is 1:3; and the mean efficiency at that ratio is 43 per cent — approximately 3 times as large as that for Class-B amplifiers. Moreover, the use of higher voltage source V_{C2} is not so frequent that the power supply regulation need not be controlled too severely.

When comparing a conventional Class-B amplifier with a Class-G amplifier both rated at 75 watts, the weight of the power transformer is reduced from 4.2 kg for the Class-B amplifier to 3.9 kg for the Class-G amplifier; the weight of the heat sink from 850 g to 300 g; and the peak power output (peak power handling capability for musical signals) is drastically increased from 90 watts to 160 watts and high efficiency is achieved.

3. SWITCHING DISTORTION ANALYSIS

In Class-G operation, large current switching takes place twice for each half cycle, causing switching distortion as shown in Figure 4. The causes of this switching distortion may include the followings:

- 1) Gain fluctuation
- 2) Switching delay of Q_2 and Q_2 due to minority carrier storage



This waveform shows enlarged distortion. This distortion cannot be seen on a CRT even at 20 kHz with negative feedback in Class-G operation.

Fig. 4 Output wave form

- Switching delay of Q₁ and Q₁ due to minority carrier storage
- Reverse recovery current through the diodes due to minority carrier storage

In Figure 4, switching distortion "B" results from above items 1) and 3), and is so low level that it is negligible; Here we discuss switching distortion "A". Figure 5 is an enlargement of the switching distortion "A" shown in Figure 4. The distortion can be broadly divided into two parts: part "a" and part "b" as shown in Figure 5. Part "a" may be attributed to the gain decrease which is derived from the increase in base current required for transistor Q2 to be turned on. Part "b" is the most difficult-to-treat type of distortion, for the frequency component of this has a range of several mega hertz, rejecting negative feedback effect. Assuming that this part "b" distortion (pulse) is caused by the transient responses of transistor Q2 and the diodes, we examined it using a simplified experimental circuit as shown in Figure 6. Current waveforms observed in each part of the experimental circuit are shown in Figure 7.

When the input signal voltage exceeds the lower voltage source of 17 volts, the transistor is turned on and diode D_1 is cut off. At the time, the D_1 's carrier storage causes a large reverse current to pass through D_1 , and the transistor supplies an emitter current to cancel this reverse current.

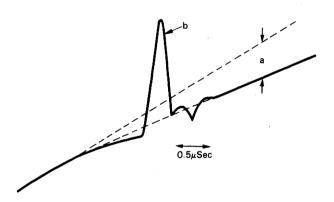


Fig. 5 Enlargement of switching distortion "A" shown in Fig. 4

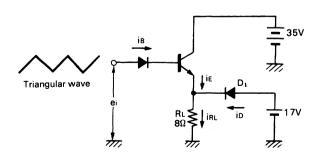


Fig. 6 Experimental circuit (a)

When there is no more carrier storage in D_1 , it rapidly recovers to normal operation. Since the transistor itself has carrier storage, it cannot follow D_1 's rapid change of state, passing excessive current into R_L to cause the pulse on the i_{RL} waveform. It is known from the i_{B} waveform that, in the region between t_2 and t_3 , the emitter current is caused only by transistor's carrier storage with no base current at all.

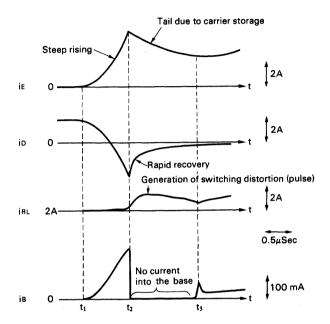


Fig. 7 Current waveforms observed

Figure 8 shows an experimental circuit which is more practical than that shown in Figure 6. The waveform shown in Figure 5 is actually derived from the circuit shown in Figure 8. The reason why the pulse generated at the emitter of Q_2 also appears at the emitter of Q_1 , the output terminal, is that the lowered Q_1 's collector-emitter voltage causes its collector output resistance to drop down to a few ohms.

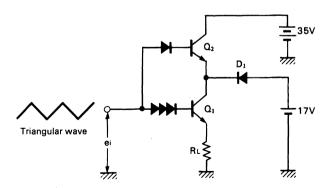


Fig. 8 Experimental circuit (b)

To reduce this switching distortion, the carrier storage in either Q_2 or D_1 must be eliminated or at least reduced. In the '76 model we used a high-speed epitaxial transistor as Q_2 and an Au-doped diode as D_1 to cope with this switching distortion problem. Also in the '76 model we provided a reverse-current prevention inductance in series with D_1 , and a circuit which allows Q_2 to turn on more quietly at a level lower than V_{C1} , thereby achieving at that time less than 0.1 per cent distortion at 20 kHz.

For the present study, a Power MOS FET, a majority carrier device, which has substantially no carrier storage has been used to further reduce switching distortion.

4. FEATURES OF THE POWER MOS FET

In 1977, we developed a complementary Power MOS FET pair (n channel and p channel, with 160V, 7A capacity). In audio power applications, the Power MOS FET, a majority carrier device, is expected to have several advantages over bipolar transistors. It has good frequency response because of fast carrier speed, high-speed switching characteristic due to the absence of minority carrier storage, thermal stability and no secondary breakdown because of its drain current characteristic with negative temperature coefficient, and high power gain because of its high input impedance.

Table 1 lists the specifications of the Power MOS FET. The major advantage of the use of the Power MOS FET in the Class-G amplifier may be due to its fast switching speed. As shown in Figure 9, the Power MOS FET can turn off a current of 2 ampere within 7 nano seconds — more than 20 times as fast as high-speed bipolar switching transistors.

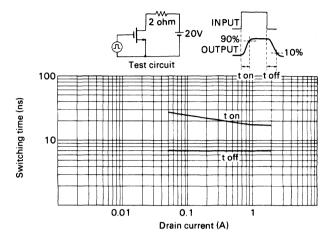


Fig. 9 Switching time vs. drain current of power MOS FET

Table 1 Features of	Power	MOSFET
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Item	Symbol	Conditions	n channel	p channel
Drain to Source Breakdow- voltage	V (BR) DSX	$I_{DS} = 10 \text{ mA}$	160V	-160V
Gate to Source Breakdown voltage	V (BR) GSS	$I_{GS} = +100\mu A$	±14V	±14V
Maximum Drain Current	Iο		7A	-7A
Maximum Power Dissipation	PD		100W	100W
Threshold voltage	V _{GS} (off)	$I_{DS} = 100 \text{mA}$	0.8V	-0.8V
Transconductance	Gm '	$V_{GS} = 3V$	18	1S
On-resistance	Ron	$I_D = 5A$	1Ω	1Ω
Input capacitance	Cgs	$V_{GS} = 5V$	600pF	900pF
Chip size			4.5 × 4.5 mm ²	5 × 5 mm ²

5. PRACTICAL DESIGN OF THE CLASS-G AMPLIFIER

Figure 10 shows the basic output circuit of the Class-G amplifier using the Power MOS FETs. Voltage source V_3 in this Figure is provided to prevent Q_1 from saturation; and diode D_2 protects Q_2 's gate-source from excessive reverse voltage. R_1 in the same Figure discharges the carrier stored between the gate and source of Q_2 . To shorten the turn off time of Q_2 , R_1 must be made as small as possible. But this

makes the input impedance of the output circuit very low despite the very high input impedance of the MOS FET, thus leading to the need for a driving transistor. Although the MOS FET has many advantages over bipolar transistors, it has one and probably only one drawback — namely, a larger turn-on resistance. Therefore, if the output stack is composed only of MOS FETs as shown in Figure 10, the resultant large power loss due to the turn-on resistance would offset the effect of the high-efficiency circuit.

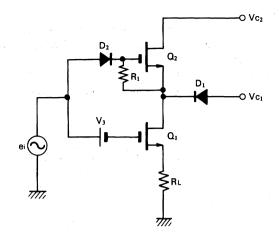


Fig. 10 Basic output circuit for Class-G amplifier using power MOS FETs

Placing primary emphasis on efficiency, we then introduced an output circuit in which Q_1 is replaced with a bipolar transistor as shown in Figure 11. The distortion vs. output power curve for an amplifier using this circuit is shown in Figure 14 as "MOS + Bip. before improvement". The switching-pulse magnitude derived from the circuit in Figure 11 has been reduced to one fourth that of the circuit in Figure 8, and distortion has been reduced to one fifth of that in the conventional Class-G amplifier ("Bip. + Bip.") shown in Figure 14. However the distortion in the high output region is relatively larger than that in the low output region.

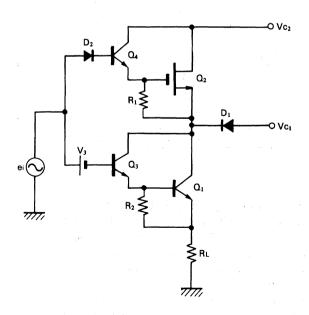


Fig. 11 Actual output circuit for Class-G amplifier

Further improvements have been made to reduce switching distortion. Generally, as signal frequency and switching current get higher, switching distortion becomes larger. Figure 12 shows an improved output circuit and its voltage waveforms.

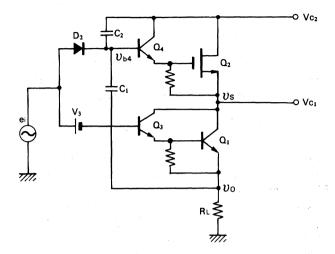


Fig. 12(a) Improved output circuit

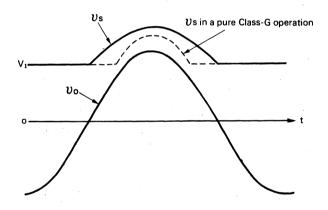


Fig. 12(b) Voltage waveforms Uo and Us

In this circuit, the base current for Q_4 is all fed from the signal source when the circuit operates in the middle to low frequency region where the impedances of C_1 and C_2 are both sufficiently high. And in this frequency region, the amplifier performs pure Class-G operation, and Q_2 's source voltage v_3 moves on the curve shown by the broken line in Figure 12 (b). Meanwhile, in the higher frequency region where the impedances of C_1 and C_2 are small, the base current for Q_4 is fed from the output terminal via C_1 . Q_4 's base voltage is a super-imposition of the DC component v_{b4} and the AC component v_{b4} as follows:

$$V_{b4} + v_{b4} = \frac{C_2}{C_1 + C_2} V_{C2} + \frac{C_1}{C_1 + C_2} v_{O}$$

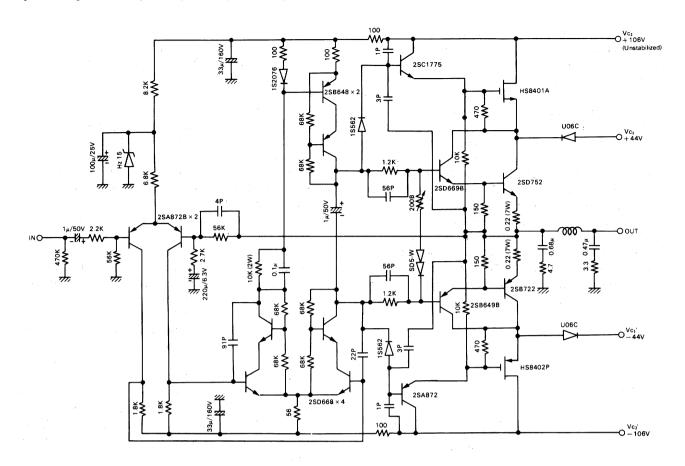


Fig. 13 The total Class-G amplifier circuit

When Q_4 's base voltage exceeds V_1 , Q_2 and Q_4 are turned on, and Q_2 's source voltage v_s moves on the solid line shown in Figure 12 (b). To operate Q_2 in the Class-B region for high frequencies without power-source switching at large currents, the ratio of C_1 to C_2 may be selected to satisfy the following relationship:

$$\frac{C_2}{C_1 + C_2} = \frac{V_{C1}}{V_{C2}}$$

The total Class-G amplifier circuit derived from the discussions made up to here is shown in Figure 13; its distortion vs. output power characteristic is shown in Figure 14 as "MOS + Bip. after improvement". The amplifier shown in Figure 13 has achieved 0.01 per cent total harmonic distortion at 20 kHz and 200 watts. Figure 14 also shows the distortion curve for the "MOS + MOS" amplifier. The low distortion of this "MOS + MOS" amplifier is due to the increased negative feedback resulting from widened open-gain bandwidth. However, this "MOS + MOS" circuit is not acceptable, because of its larger loss and hence lower maximum output.

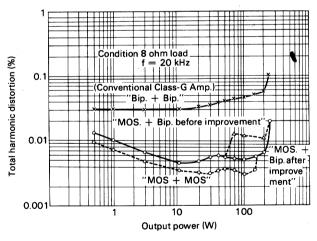


Fig. 14 Total harmonic distortion vs. output power

The higher power-supply voltage in the amplifier shown in Figure 13 is selected at the very high value of 106 volts. This voltage gives the amplifier the potential to deliver a peak

power output of 400 watts into 8 ohms. The use of this high voltage supply is, of course, not frequent in most music programs so that the transformer capacity employed is relatively small resulting in lower cost. According to our experimental results, the period of maximum amplitude in most music programs is no more than 20 ms. For such a brief period, the electrolytic capacitors will able to supply enough current to deliver the peak power. The lower power supply voltage in Figure 13 is selected not at 1/3 the higher supply voltage (106V) but at approx. 2/5 of 44 volts, so that the maximum efficiency is obtained at 1/3 the rated output power when heat dissipation, etc. are considered.

Efficiency comparison between this Class-G amplifier and a conventional Class-B amplifier using a continuous sine wave — not a very original method — is shown in Figure 15. Approximately twice the efficiency is achived with the Class-G amplifier for an output below 50 watts compared with that of the Class-B amplifier.

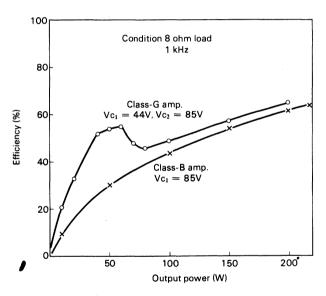


Fig. 15 Power efficiency

6. CONCLUSION

A high-quality Class-G power amplifier has been developed using Power MOS FETs as a switching device to improve switching distortion ratio without degrading power efficiency.

It was first revealed that switching distortion is mainly caused by carrier storage in switching diodes and transistors. Then, the Power MOS FET which has substantially no minority carrier storage was introduced to improve this switching distortion performance However, this still seemed not to be sufficient, and further attempts were made. The approach introduced is that the amplifier is allowed to operate in pure Class-G in the middle to low frequency region, whereas above 10 kHz, the amplifier is allowed to operate in near Class-B. These efforts achieved a total harmonic distortion of less than 0.01 per cent at 20 kHz and 200 watts. This distortion ratio is approximately one tenth that available with conventional Class-G amplifiers. The effective efficiency of the amplifier is approximately 55 per cent at approx. 1/3 the maximum output power. This efficiency is about twice that with conventional Class-B amplifiers.

7. ACKNOWLEDGEMENT

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8. REFERENCES

- H.R. Camenzind, "Modulated pulse audio power amplifiers for integrated circuits", IEEE Audio and Electroacoustics, AU-14(3) p.136-140, September
- (2) Y. Yamasaki and T. Itoh, "PCM-PWM power amplifier", The Acoustical Society of Japan, Reports of the 1975 spring meeting p.357.
- (3) F.H. Raab, "High-efficiency amplification techniques", IEEE Circuit and Systems, Vol. 7 (10) p.3-11, December 1975.
- (4) T. Sampei, S. Ohashi, "A new high efficiency circuit" NIKKEI ELECTRONICS p.74-87, 12 July 1976.
- (5) T. Sampei, S. Ohashi and S. Ochi, "100 watt super audio amplifier using new MOS devices" IEEE Consumer Electronics CE-23(3) p.409-417, August 1977.

BIOGRAPHY



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