[86.46 / 66.61] Microelectrónica -
Tecnología de circuitos Integrados

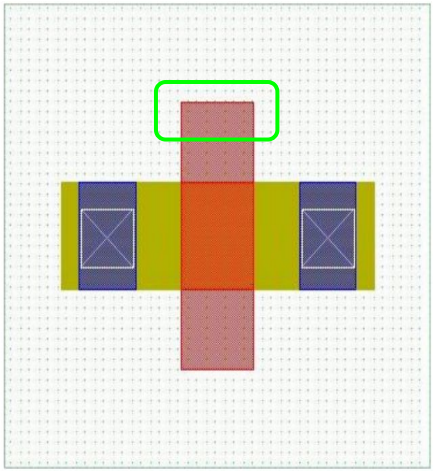
SAED90nm - nmos4t

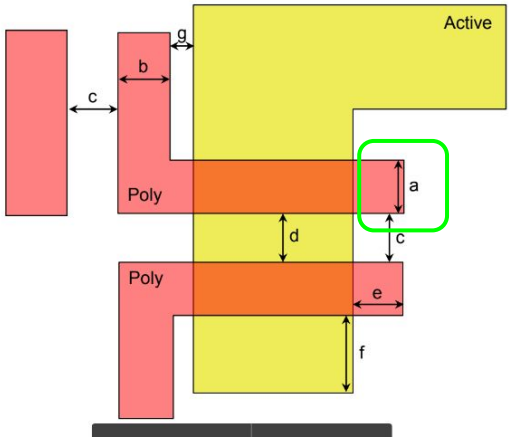
Introducción a la interpretación de las reglas de diseño.

Interpretación de las reglas de proceso - POLY

Table 3. PO Rules

Rule #	Rule description	µm	Mark
PO.W.1	Minimum width	0.1	a
PO.W.2	Minimum poly width in a thick oxide gate	0.3	b

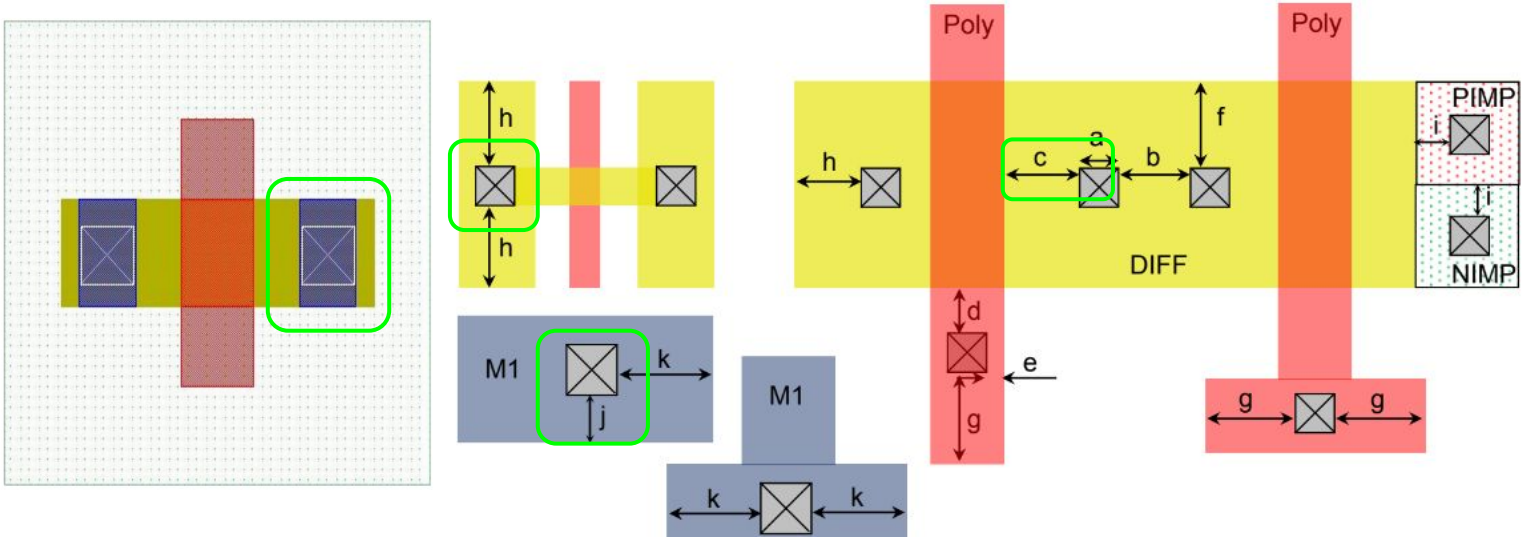




Interpretación de las reglas de proceso - CO

Table 4. CO Rules

Rule #	Rule description	µm	Mark
CO.W.1	Exact contact size	0.13	a
CO.S.1	Minimum contact spacing	0.13	b
CO.S.2	(Contact inside DIFF) space to gate	0.12	c
CO.S.3	(Contact inside Poly) space to Active	0.12	d
CO.E.1	Minimum enclosure by poly	0.04	e
CO.E.2	Minimum enclosure by DIFF	0.04	f
CO.E.3	Minimum enclosure by poly at least two apposite sides	0.05	g
CO.E.4	Minimum enclosure by DIFF at least two apposite sides	0.05	h
CO.E.5	Minimum butted diffusion IMP enclosure of S/D contact	0.06	i
CO.E.6	Minimum enclosure of any contact (CO outside M1 is not allowed)	0.005	j
CO.E.7	Minimum enclosure of contact at end of line	0.05	k



Interpretación de las reglas de proceso - M1

Table 11. M1 Rules

Rule #	Rule description	µm	Mark
M1.W.1	Minimum width	0.14	a
M1.S.1	Minimum spacing	0.14	b
M1.S.2	Minimum spacing when either metal line is wider than 5 µm	0.25	c
M1.A.1	Minimum area	0.07^2	d