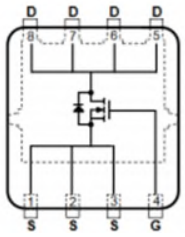
100V N-Channel Enhancement Mode MOSFET

Voltage	100 V	R_{DSON}	9.2 mΩ
Current	62 A	$Q_{G\ (TYP)}$	37.8 nC

DFN5060-8L



Top side view

Feature

- $R_{DS(ON)}$, V_{GS}@10V, I_D@15A<9.2mΩ
- $R_{DS(ON)}$, V_{GS}@4.5V, I_D@8A<14mΩ
- High switching speed
- Low reverse transfer capacitance
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case: DFN5060-8L Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.0028 ounces, 0.08 grams

Application

- SR solutions of PD Charger, BMS, BLDC motor driver switch

Absolute Maximum Ratings (T_A = 25 °C unless otherwise specified)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	+20 / -12	
Continuous Drain Current (Note 3)	T_C=25°C	I_D	62	A
	T_C=100°C		39.2	
Pulsed Drain Current	T_C=25°C	I_{DM}	248	A
Single Pulse Avalanche Current (Note 5)		I_{AS}	43	A
Single Pulse Avalanche Energy (Note 5)		E_{AS}	92	mJ
Power Dissipation	T_C=25°C	P_D	125	W
	T_C=100°C		1	
Operating Junction and Storage Temperature Range		T_J,T_{STG}	-55~150	°C

Thermal Characteristics

PARAMETER		SYMBOL	MAXIMUM	UNITS
Thermal Resistance	Junction-to-Case (Bottom)	$R_{\theta JC}$	1.9	°C/W
	Junction-to-Case (Top)	$R_{\theta JT}$	-	°C/W
	Junction-to-Ambient (Note.4)	$R_{\theta JA}$	39	°C/W

Electrical Characteristics (T_A = 25 °C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250uA	100	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250uA	1.2	1.6	2.5	
Drain-Source On-State Resistance (Note 1)	$R_{DS(on)}$	V_{GS}=10V, I_D=15A	-	8.1	9.2	mΩ
		V_{GS}=4.5V, I_D=8A	-	11.7	14	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V, V_{GS}=0V	-	-	1	uA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=+20V, V_{DS}=0V	-	-	9.5	nA
Transfer characteristics (Note 1)	gfs	V_{DS}=10V, I_D=3A	-	11	-	S
Dynamic (Note 6)						
Total Gate Charge	Q_g	V_{DS}=50V, I_D=8.5A, V_{GS}=10V	-	37.8	-	nC
Gate-Source Charge	Q_{gs}		-	7.8	-	
Gate-Drain Charge	Q_{gd}		-	8.4	-	
Plateau Voltage	V_{GP}		-	-	-	V
Input Capacitance	Ciss	V_{DS}=50V, V_{GS}=0V, f=1.0MHZ	-	2250	-	pF
Output Capacitance	Coss		-	410	-	
Reverse Transfer Capacitance	Crss		-	25	-	
Turn-On Delay Time	$td_{(on)}$	V_{DD}=50V, I_D=1A, V_{GS}=10V, R_G=6Ω (Note 2)	-	14.6	-	ns
Turn-On Rise Time	t_r		-	21.5	-	
Turn-Off Delay Time	$td_{(off)}$		-	54	-	
Turn-Off Fall Time	t_f		-	84.3	-	
Gate Resistance	Rg	f =1.0MHz	-	1.43	-	Ω
Drain-Source Diode						
Diode Forward Voltage	V_{SD}	I_S=1A, V_{GS}=0V	-	-	1	V
Reverse Recovery Charge	Q_{rr}	I_{SD} = 10A di/dt = 100A/μs	-	75.1	-	nC
Reverse Recovery Time	T_{rr}		-	49.2	-	ns

NOTES :

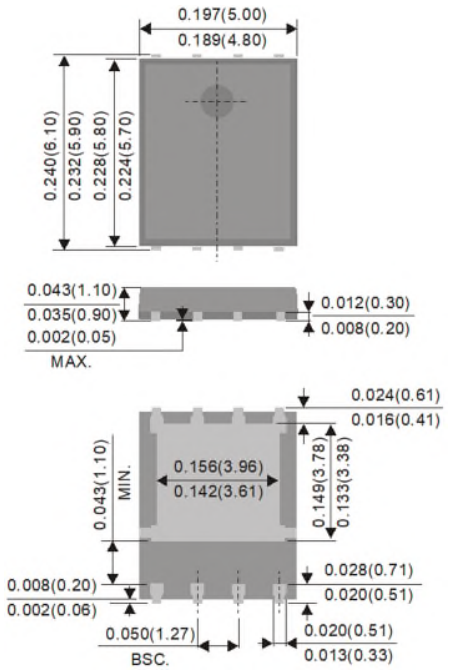
1. Pulse width≤300us, Duty cycle≤2%
2. Essentially independent of operating temperature typical characteristics.
3. The maximum current rating is package limited.
4. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch^2 with 2oz.square pad of copper.
5. The test condition is L=0.1mH, I_{AS}=65A, V_{DD}=50V, V_{GS}=10V, R_G=25ohm, Starting T_J=25°C
6. Guaranteed by design, not subject to production testing.

Product and Packing Information

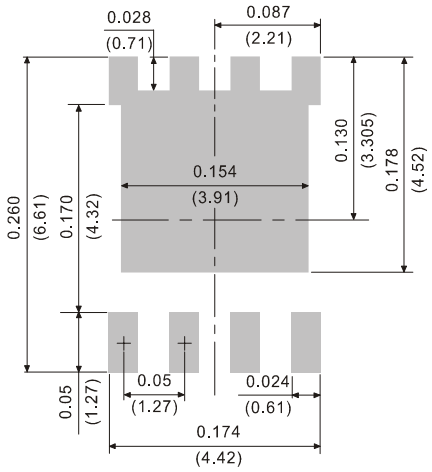
Part No.	Package Type	Packing Type	Marking
PSMQC092N10LS1	DFN5060-8L	3000pcs / 13” reel	092N10LS

Packaging Information & Mounting Pad Layout

DFN5060-8L Dimension Unit: inch(mm)



DFN5060-8L Pad Layout Unit: inch(mm)



Marking Diagram

PJ
092N10LS
YWLL x

Y = Year Code
W = Week Code (A~Z)
LL = Lot Code (00~99)
x = Production Line Code

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