4. Logic Gates.

(Marks:-17)

Q.1 Logic Gates:-

Ans.

Gate is an electronic circuit in which only one input & two or more than output.

- There are three basic types of logic gates:-
  1. **AND Gate.**
  2. **OR Gate.**
  3. **NOT Gate. [Bubble/ Inverter Gate]**

Logic Decision:-

Inter connection of gate to perform variety of logic decision operation is called logic decision.

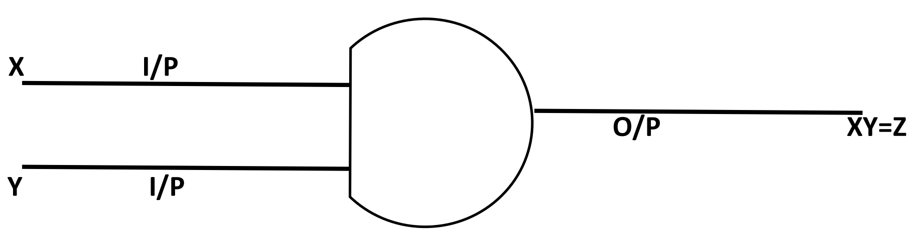
Truth Table:-

A table which list all the possible communication of Input variable & corresponding output is called truth table.

1. AND Gate :-

AND Gate is logical gate in which two or more input & only one output.

Block Diagram of AND Gate:-



Truth table of AND Gate:-

Input		Output
X	Y	Z=XY
0	0	0(low)
0	1	0
1	0	0
1	1	1(High)

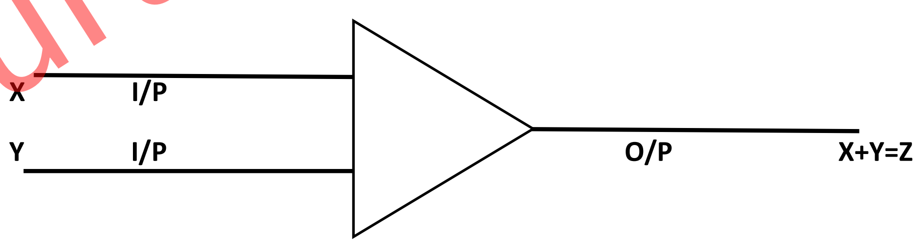
Explain:-

If both input are low than output low, if both input are high than output high otherwise output is low.

2. OR Gate:-

OR Gate is two or more than input & only one output.

Block Diagram of OR Gate:-



Truth table of OR Gate:-

Input		Output
X	**Y**	**Z=X+Y**
0	0	0(Low)
0	1	1
1	0	1
1	1	1(High)

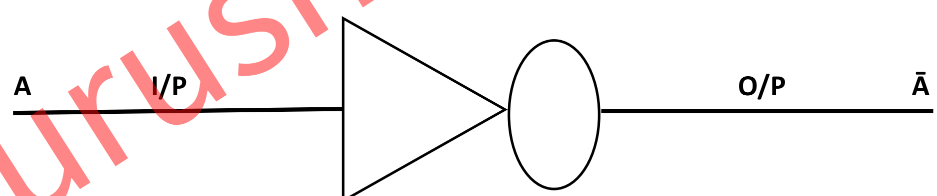
Explain:-

If both input are low than output will be low otherwise output will be high. If any input high than output will be high.

3. **NOT Gate [Bubble/ Inverter Gate]:-**

Not Gate is inverter gate. It has only one input & only one output. It contain bubble to inverter.

Block diagram of NOT Gate:-



Truth table of NOT Gate:-

Input	Output
A	**Ā**
0	1
1	0

Explain:-

If input is low than output is high & if input is high than output is low.

Q.2 Universal Gate:-

Ans.

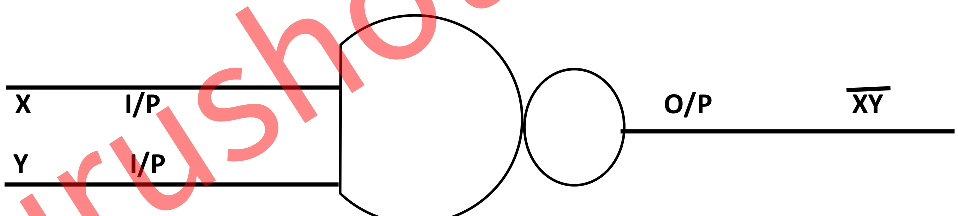
- There are two types of universal gate.
  1. **NAND [AND + NOT]**
  2. **NOR [OR + NOT]**

NAND & NOR perform all three basic logic [AND, OR, NOT] that's way is called universal gate.

1. **NAND [AND + NOT]:-**

   NAND Gate is universal gate in which two or more than two input & only one output.

Block diagram of NAND Gate:-



Truth table of NAND Gate:-

Input		**Output**	
X	**Y**	**XY**	**$\overline{XY}$**
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

Explain:-

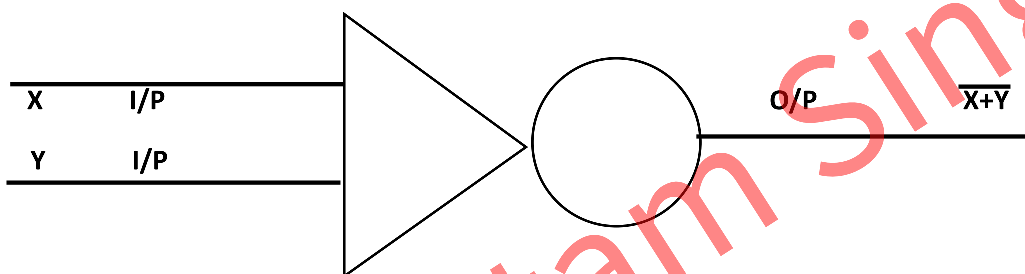
If both input are high then output will be low. Otherwise output will be high.

NAND Gate is communication is AND & NOT gate.

2. **NOR[OR+NOT] :-**

NOR is universal gate in which two or more than two input & only one output.

Block diagram of NOR Gate:-



Truth table of NOR Gate:-

Input		Output	
X	**Y**	**X+Y**	$\overline{\mathbf{X+Y}}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

Explain:-

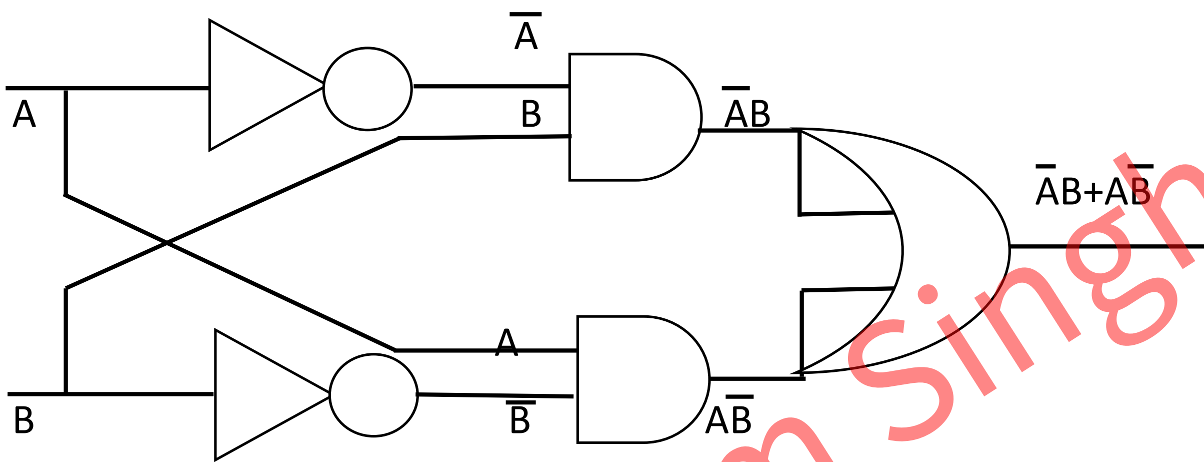
If both input are low than output is high, otherwise input is high than output will be low.

NOR Gate is communication of OR+NOT Gate.

Q.3 Exclusive- OR-Gate [ex-OR]... [$\overline{A}B+A\overline{B}$] or [A (+) B].

Ans.

<u>**Block Diagram of Exclusive OR Gate**</u>**:-**



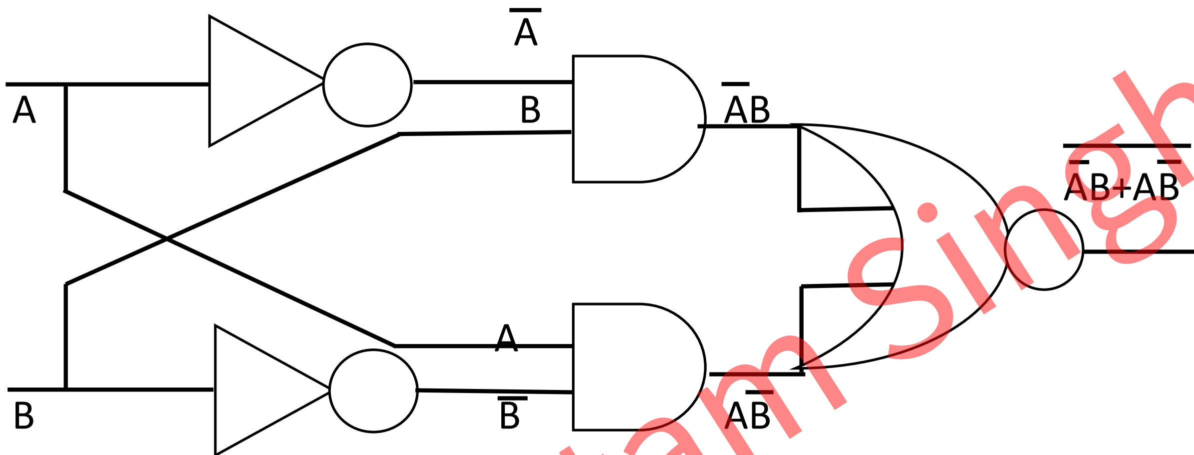
<u>**Truth table of Exclusive OR Gate**</u>**:-**

Input				**Output**		
A	**B**	**$\overline{A}$**	**$\overline{B}$**	**$\overline{A}B$**	**$A\overline{B}$**	**$\overline{A}B+A\overline{B}$**
0	0	1	1	0	0	0
0	1	1	0	1	0	1
1	0	0	1	0	1	1
1	1	0	0	0	0	0

Q.4 Exclusive- NOR-Gate [ex-NOR]... [$\overline{\bar{A}B + A\bar{B}}$].

Ans.

<u>Block Diagram of Exclusive NOR Gate</u>:-



<u>Truth table of Exclusive NOR Gate</u>:-

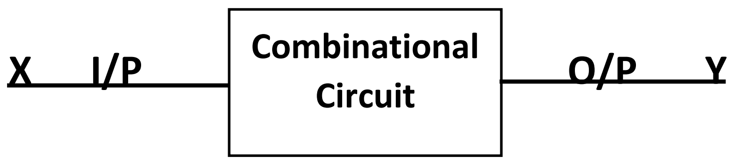
Input				**Output**			
A	**B**	**$\bar{A}$**	**$\bar{B}$**	**$\bar{A}B$**	**$A\bar{B}$**	**$\bar{A}B+A\bar{B}$**	**$\overline{\bar{A}B+A\bar{B}}$**
0	0	1	1	0	0	0	1
0	1	1	0	1	0	1	0
1	0	0	1	0	1	1	0
1	1	0	0	0	0	0	1

Q.5 Combinational Circuit

Ans.

In combinational circuit output is depend on only present input.

Block diagram of combinational:-



- There are two types of combinational circuit.
  1. **Adder**
     I. **Half adder (0+0)**
     II. **Full adder(0+0+0)**
  2. **Subtraction**
     I. **Half subtraction(0-0)**
     II. **Full subtraction (0-0-0)**

1. **Adder:-**

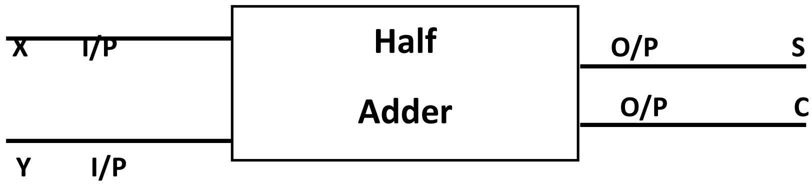
In combinational circuit perform addition of bit is called adder.

- There are two types of adder:-
  I. **Half adder (0+0)**
  II. **Full adder(0+0+0)**

I. Half adder (0+0) :-

In communicational circuit which can perform the addition of two bit is called half adder.

Block diagram of Half adder:-



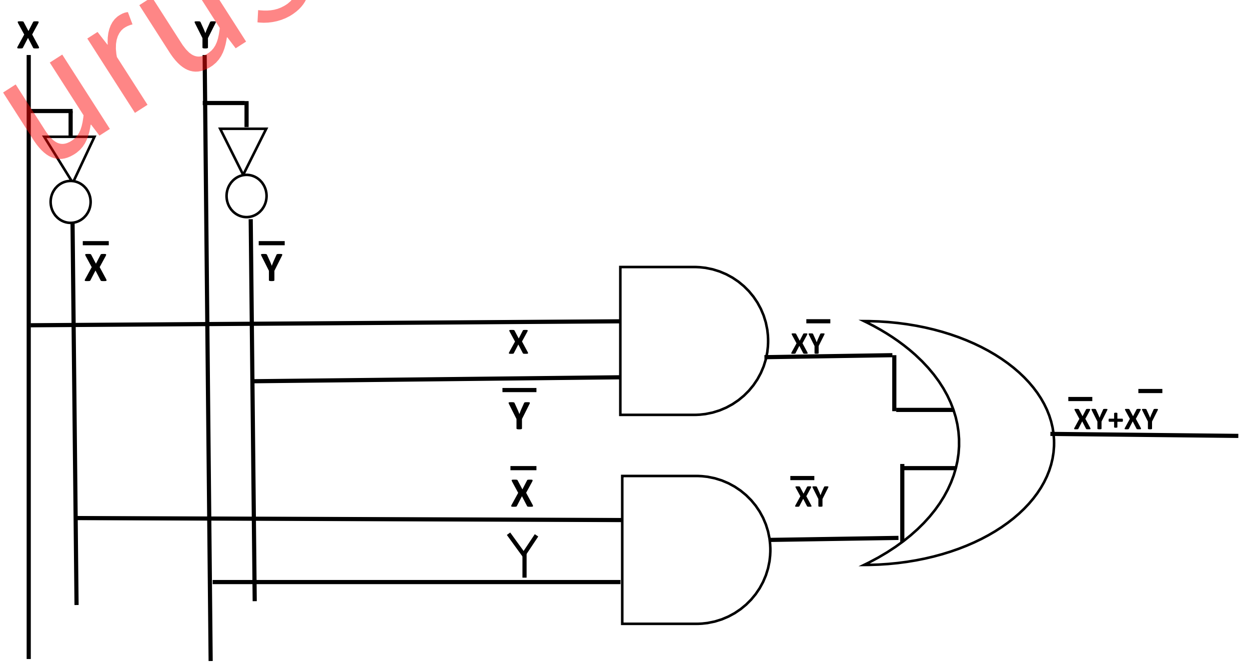
Truth table of Half adder:-

Input		Output	
X	Y	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

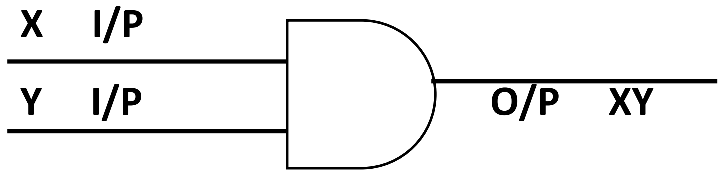
Logic of Half adder of Sum:-

$$[\bar{X}Y + X\bar{Y}]$$

Circuit of Half adder of Sum: -



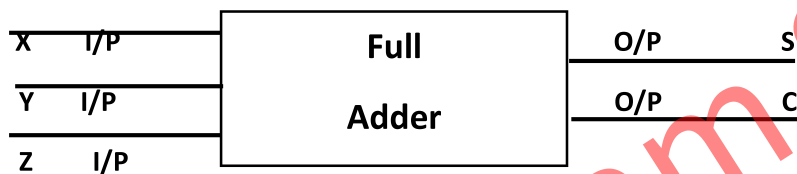
Circuit of Half adder of carry: - [logic: - XY]



II. **Full adder(0+0+0) :-**

In communicational can which three bit addition is called full adder.

Block diagram of Full adder:-



Truth table of Full adder:-

Input			Output	
X	Y	Z	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Logic of Full adder of sum:-

$= \bar{X}\,\bar{Y}\,Z + \bar{X}\,Y\,\bar{Z} + X\,\bar{Y}\,\bar{Z} + X\,Y\,Z$

$= \overline{X}\,(\overline{Y}\,Z + Y\,\overline{Z}) + X\,(\overline{Y}\,\overline{Z} + Y\,Z)$

$= \overline{X}\,(Y \oplus Z) + X\,\overline{(Y \oplus Z)}$

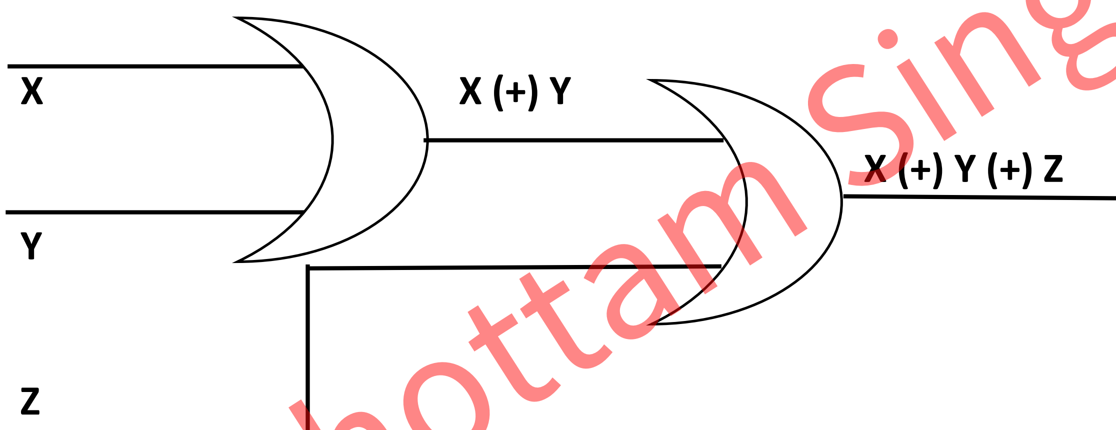
$= (\overline{Y} \oplus \overline{Z})$ == K ધારતાં

= XK + XK

= X (+) K

= X (+) Y (+) Z

Circuit of Full adder of sum:-



Logic of Full adder of carry:-

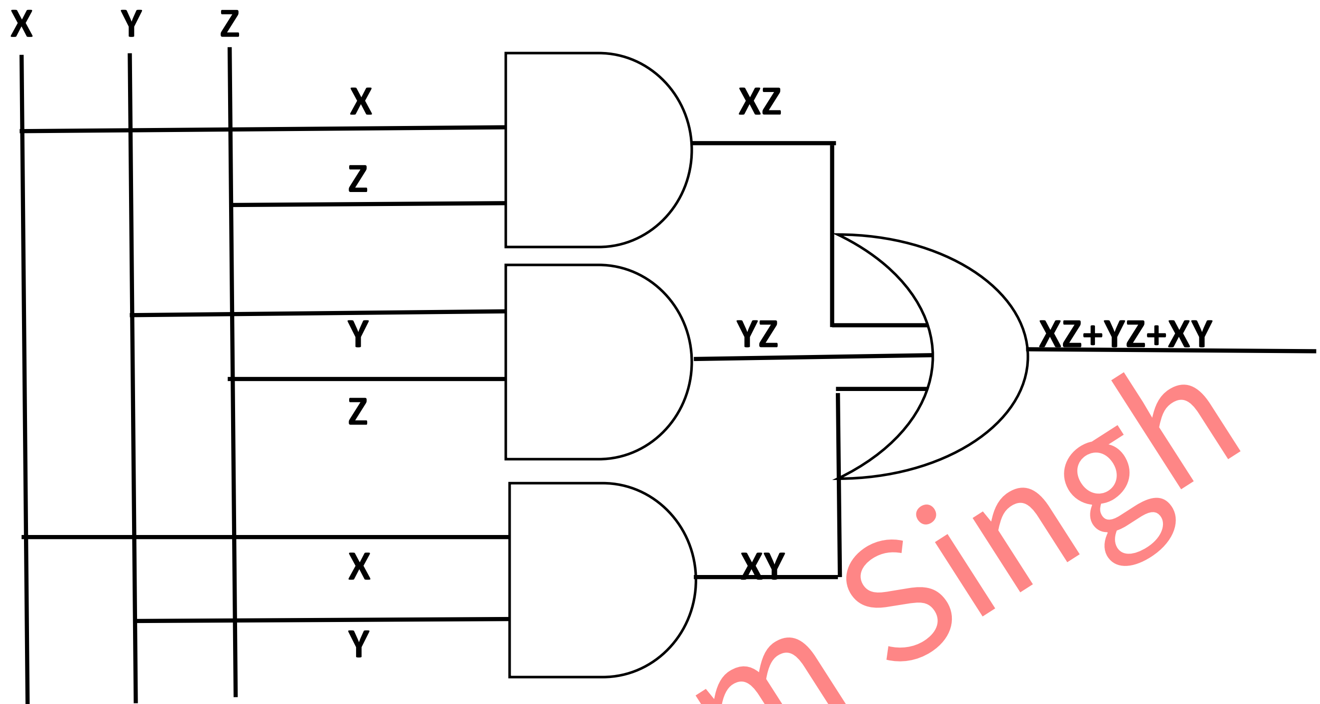
$= \overline{X}YZ + X\overline{Y}Z + XY\overline{Z} + XYZ$

$= Z\,(\overline{X}Y + X\overline{Y}) + XY(\overline{Z} + Z)$

= Z(X(+)Y)+ XY(1)

= ZX+ZY+XY

Circuit of Full adder of carry:-



2. **Subtraction:-**

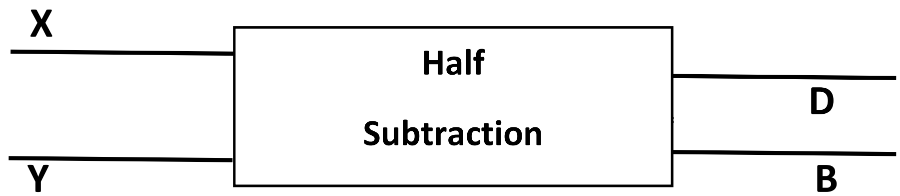
There are two types of subtraction:-

I. **Half subtraction (0-0)**
II. **Full subtraction (0-0-0)**

I. Half subtraction(0-0):-

In communicational circuit which can perform difference between two bit.

Block diagram of half subtraction:-



Truth table of half subtraction:-

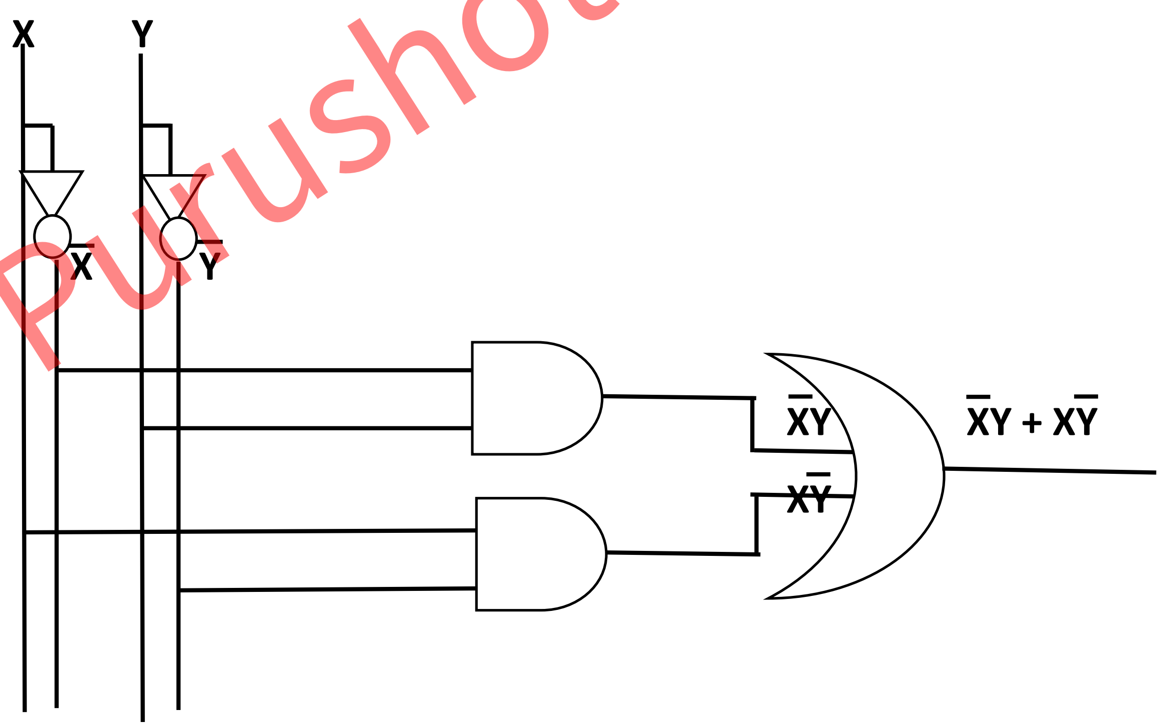
Input		Output	
X	Y	D	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Logic of half subtraction of Difference:-

$= \bar{X}Y+X\bar{Y}$

$= X\ (+)\ Y$

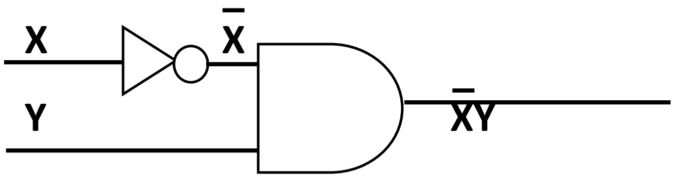
Circuit of half subtraction of difference:-



Logic of half subtraction of borrow:-

$=\overline{X}Y$

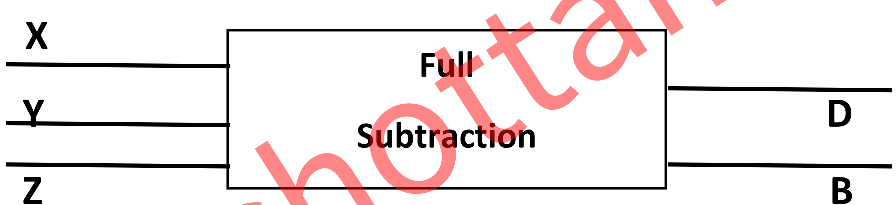
Circuit of half subtraction of borrow:-



II. **Full subtraction (0-0-0):-**

In communicational circuit which can perform different between 3 bits is called full subtraction.

Block diagram of full subtraction:-



<u>Truth table of full subtraction</u>:-

Input			**Output**	
X	**Y**	**Z**	**D**	**B**
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

<u>Logic of full subtraction of different</u>:-

$=\overline{X}\,\overline{Y}Z+\overline{X}Y\overline{Z}+X\overline{Y}\,\overline{Z}+XYZ$

$=\overline{X}\,(\,Y\,(+)\,Z\,)+X\,(\,\overline{Y\,(+)\,Z}\,)$

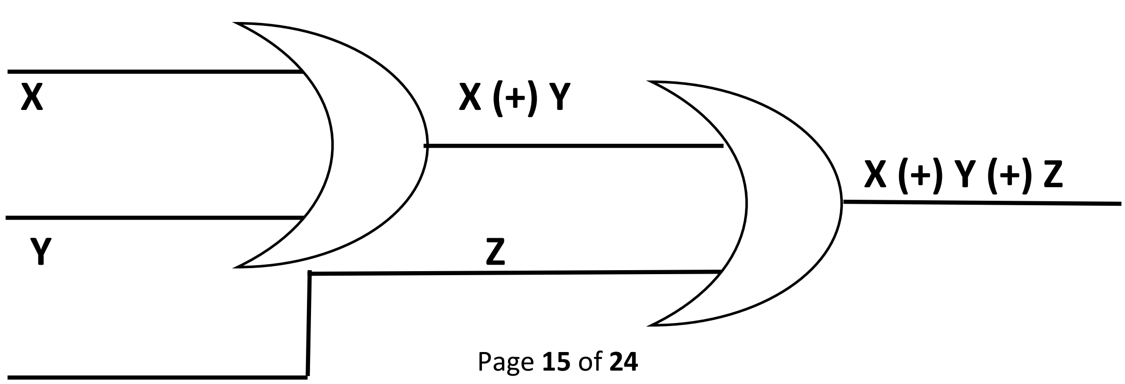
$= Y\,(+)\,Z = K$ ધારતાં

$= \overline{X}\,(K) + X\,(\overline{K})$

$= X\,(+)\,K$

$= X\,(+)\,Y\,(+)\,Z$ K= Y (+) Z મૂકતાં.

<u>Circuit of subtraction of difference</u>:-



<u>Logic of full subtraction of borrow</u>:-

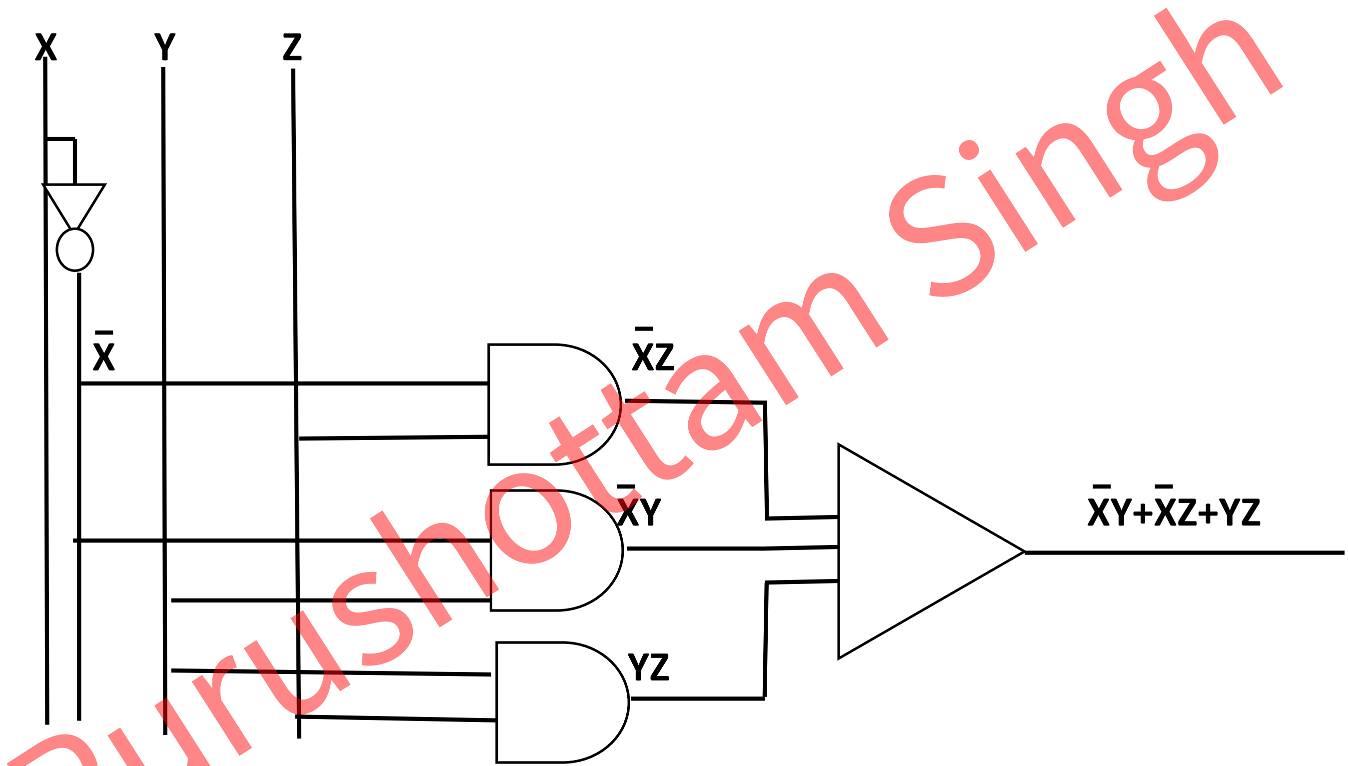
$= \overline{X}\,\overline{Y}Z + \overline{X}Y\overline{Z} + \overline{X}YZ + XYZ$

$= \overline{X}\,(\overline{Y}Z+YZ) + YZ\,(\overline{X}+X)$

$= \overline{X}\,(Y\,(+)\,Z) + YZ\,(1)$

$= \overline{X}Y + \overline{X}Z + YZ$

<u>Circuit of full subtraction of borrow</u>:-

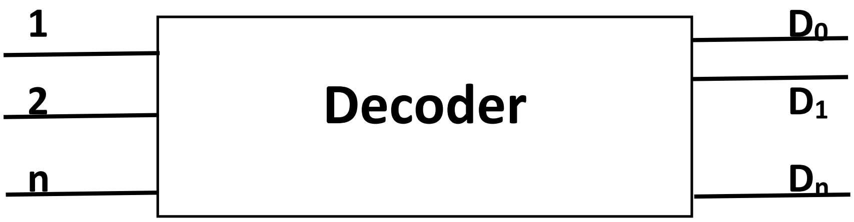


Q.6 Decoder:-

Ans.

Decoder is combinational that convert binary Information from n input line 2^n output line.

Block diagram of Decoder:-



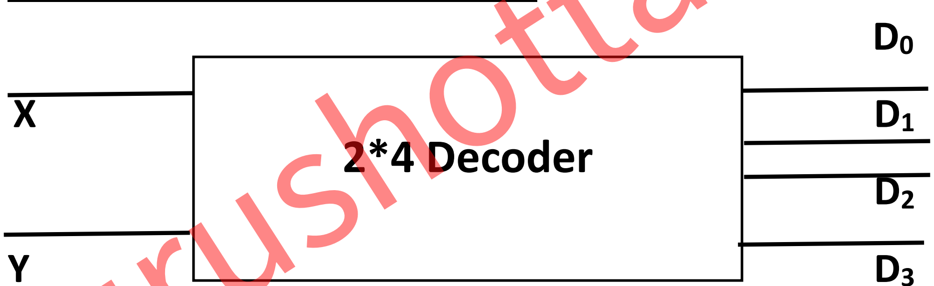
➢ There are two types of decoder:-

1. **(2*4) Decoder or 2*4 line Decoder.**
2. **(3*8) Decoder or 3*8 line Decoder.**

1. (2*4) Decoder or 2*4 line Decoder:-

A Decoder is having two input line & $2^n = 2^2 = 2*2 = 4$ decoder is called 2*4 decoder.

Block diagram of 2*4 Decoder:-



Truth table of 2*4 Decoder:-

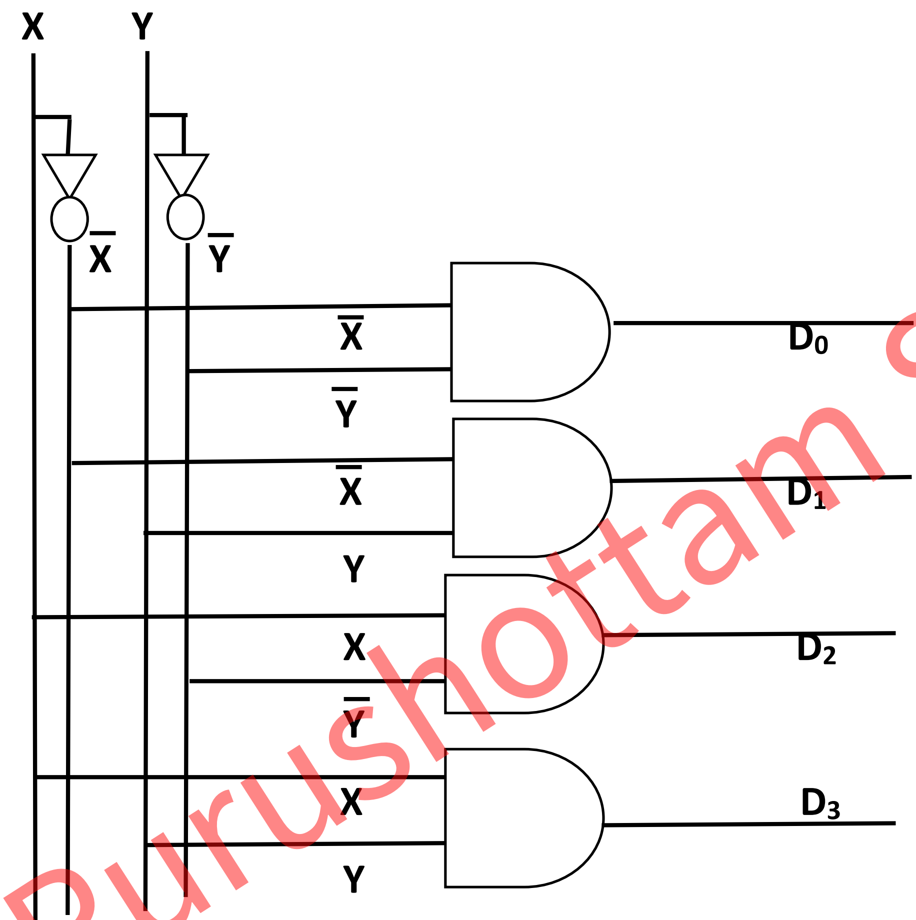
Input		Output			
X	Y	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Logic of 2*4 Decoder:-

$D_0 = \overline{X}\,\overline{Y}$ $\quad$ $D_2 = X\overline{Y}$

$D_1 = \overline{X}Y$ $\quad$ $D_3 = XY$

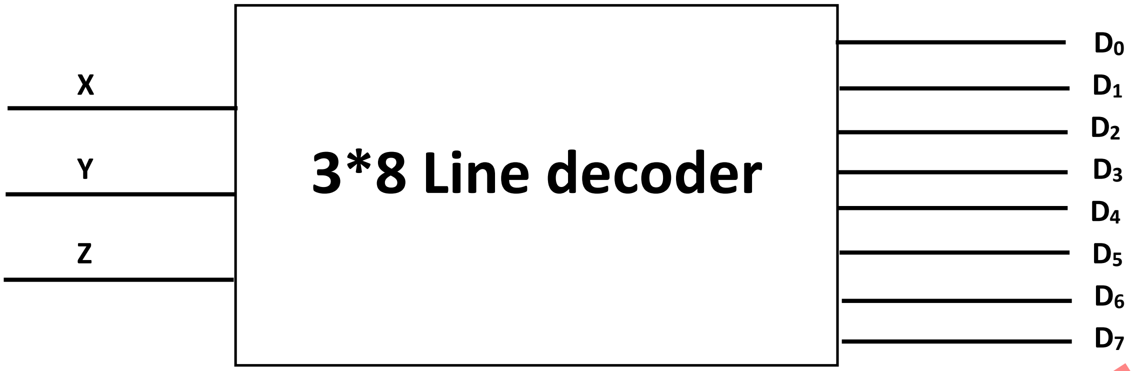
Circuit of 2*4 Decoder:-



2. 3*8 Decoder or 3*8 line Decoder:-

A decoder having three input line $2^n = 2^3 = 2*2*2 = 8$ output line is called 3*8 decoder.

Block diagram of 3*8 line Decoder:-



Truth table of 3*8 line Decoder:-

Input			Output (Octal)							
X	Y	Z	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

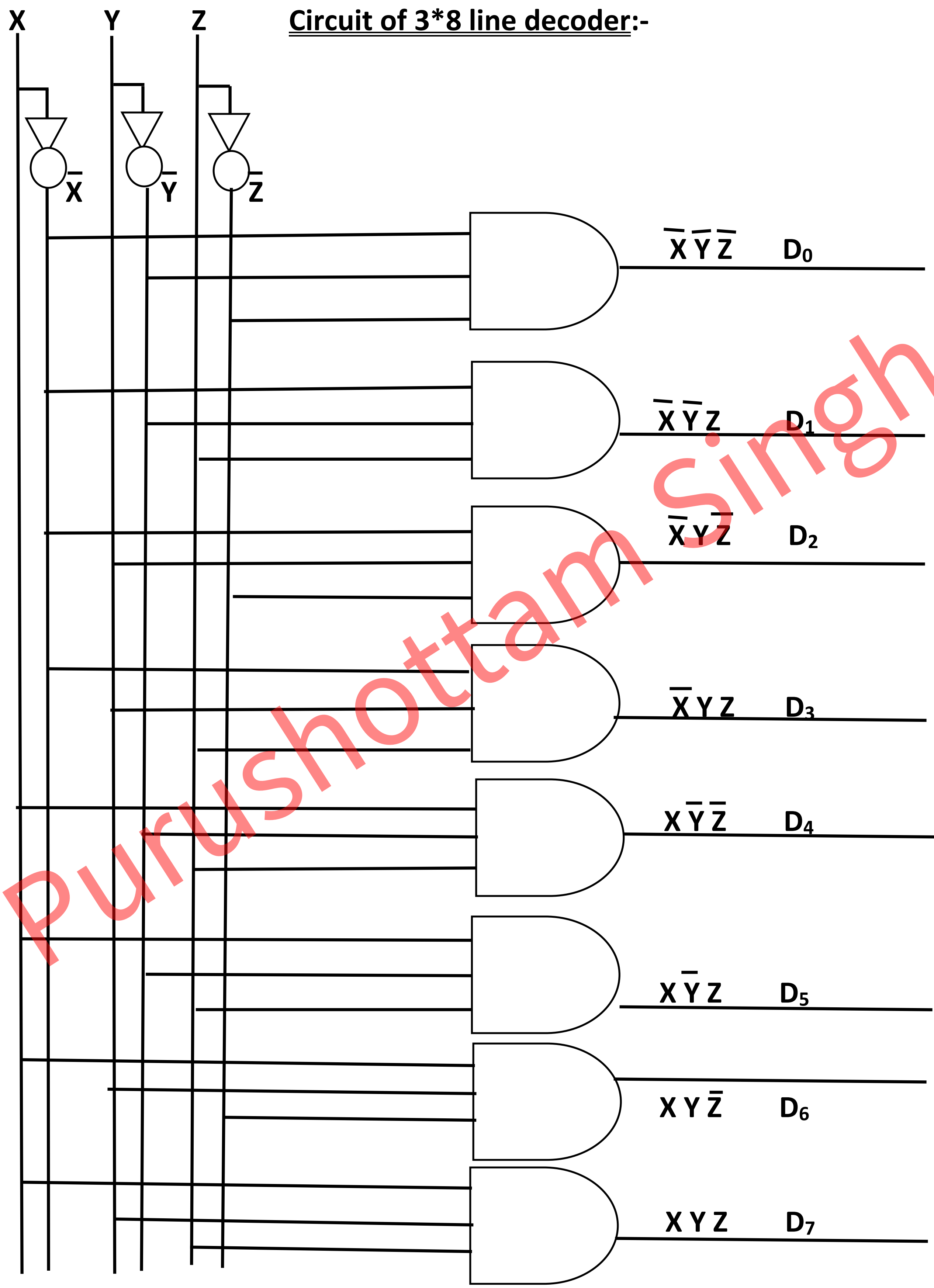
Logic of 3*8 line Decoder:-

$D_0 = \bar{X}\ \bar{Y}\ \bar{Z}$ $D_3 = \bar{X}\ Y\ Z$ $D_6 = X\ Y\ \bar{Z}$

$D_1 = \bar{X}\ \bar{Y}\ Z$ $D_4 = X\ \bar{Y}\ \bar{Z}$ $D_7 = X\ Y\ Z$

$D_2 = \bar{X}\ Y\ \bar{Z}$ $D_5 = X\ \bar{Y}\ Z$

Circuit of 3*8 line decoder:-

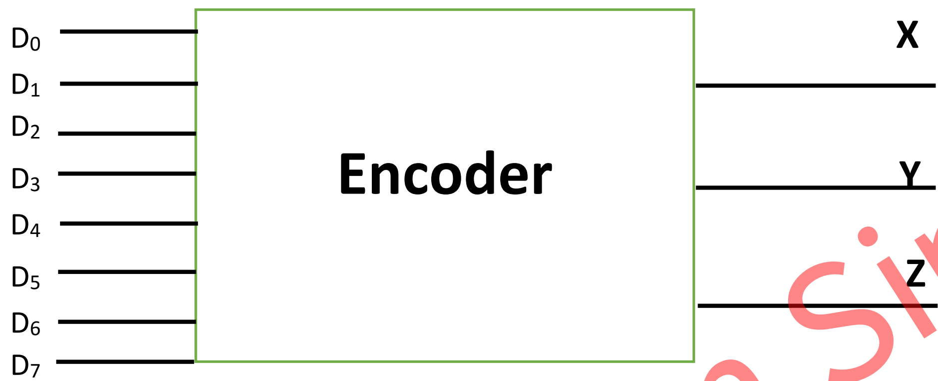


Q.7 Encoder:-

Ans.

Encoder is digital circuit that product operation from decoder. Encoder has 2^n input & n output line.

<u>Block diagram of encoder</u>:-



<u>Explain</u>:-

Octal to binary encoder consist of 8 input & 3 output which generate binary run.

<u>Truth table of encoder</u>:-

Input	Output		
Octal	**X**	**Y**	**Z**
D_0	0	0	0
D_1	0	0	1
D_2	0	1	0
D_3	0	1	1
D_4	1	0	0
D_5	1	0	1
D_6	1	1	0
D_7	1	1	1

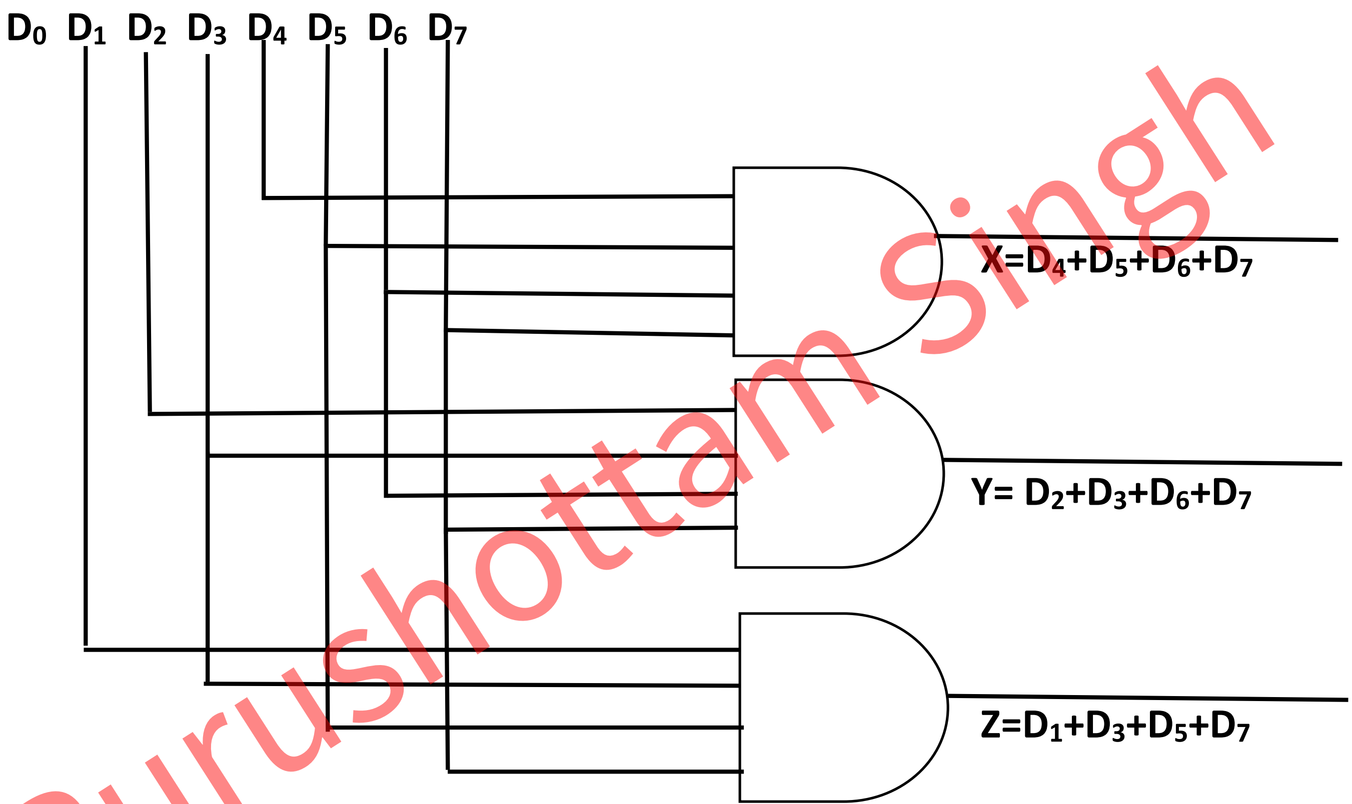
Logic of encoder:-

$X=D_4+D_5+D_6+D_7$

$Y=D_2+D_3+D_6+D_7$

$Z=D_1+D_3+D_5+D_7$

Circuit of encoder:-



Q.8 write short note on 8 4 2 1 BCD code [BCD: - Binary Code Decimal].

Ans.

The 8 4 2 1 BCD code is a weighted code is also sequence is called so it is useful for mathematical operation.

In this code each decimal digits 0 to 9 is coded by 4 bit binary number.

It is called natural binary because of the 8 4 2 1 wait attached to it.

There are six invalid communicational 1010, 1011, 1100, 1101, 1110 & 1111 they are not a part of 8 4 2 1 BCD code.

Advantages of BCD code:-

- It is easy to convert from decimal. Ex. 31 0011 0001

Disadvantages of BCD code:-

- It required more bit to represent of number.

<u>BCD Arithmetic:</u>-

(1) <u>Additions</u> :-

BCD addition is perform by adding the corresponding digits of for bit binary.

If there is query out a group to the next group or if the result is eagle them 0110 (6) is called to the group.

(2) <u>Subtraction</u>:-

BCD subtraction is borrow from next row them 0110 (6) is subtracted from the group.

Q.9 Excess three code (XS-3)

Ans.

- Excess-3 also called (XS-3) code.
- Excess-3 also called non-weighted.

XS-3 code derived from each binary code corresponding 8 4 2 1 plus 0011 (3).

It can be used arithmetic operation.

Table of XS-3

Decimal	8	4	2	1	XS-3 code
0	0	0	0	0	0011 (0+3)=3
1	0	0	0	1	0100(1+3)=4
2	0	0	1	0	0101(2+3)=5
3	0	0	1	1	0110(3+3)=6
4	0	1	0	0	0111(4+3)=7
5	0	1	0	1	1000(5+3)=8
6	0	1	1	0	1001(6+3)=9
7	0	1	1	1	1010(7+3)=10
8	1	0	0	0	1011(8+3)=11
9	1	0	0	1	1100(8+4)=12

XS-3 code has six invalid state like 0000, 0001, 0010, 1101, 1110, 1111.