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MOHSIN IBNA HOSSAIN
AIUB, DLAC NOTE'S.

#FINAL TERM:-

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#SEQUENTIAL CIRCUIT DESIGN

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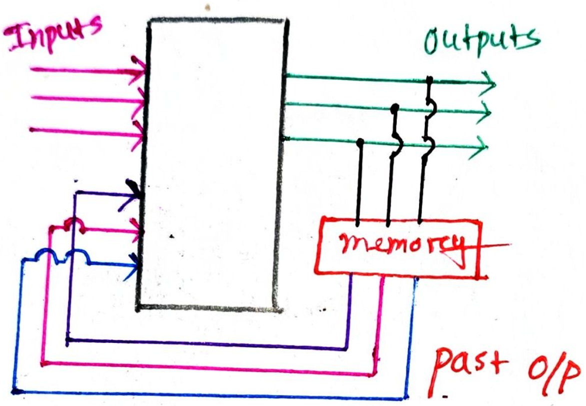
#LATCHES

Sequential Circuits:-

⇒ In Sequential Circuits, the present output depends on the present input as well as past output/Outputs



SR Latch:-

⇒ The basic storage element is called "LATCH".

There are two types:-

1. NOR SR Latch.
2. NAND SR Latch

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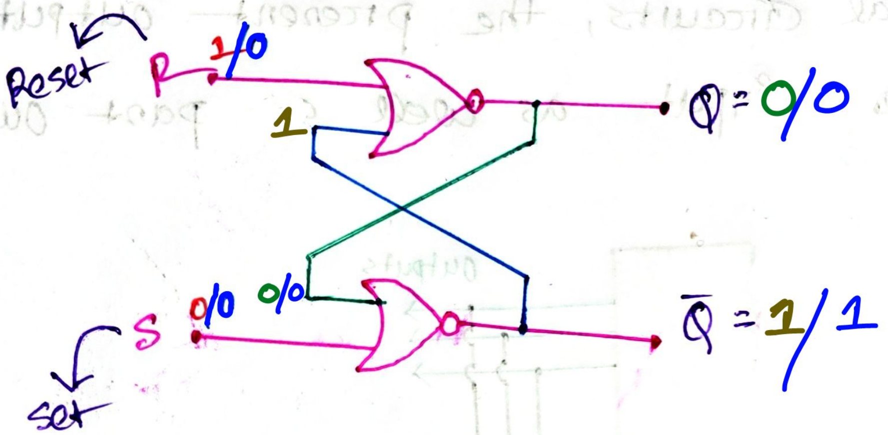
SR NOR Latch:-



Note:-

Reset $Q = 0$

Set $Q = 1$

TRUTH TABLE: FOR NOR Gate:-

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Analyse the SR Latch:-

Case 1:-

if $S = 0,\ R = 1$; then:- $Q = 0$ & $\bar{Q} = 1$

Ex:- if $\boxed{S = 0,\ R = 0 \ \text{then:-}\ Q = 0 \ \&\ \bar{Q} = 1}$ → memory

Case : 2:-

if $S = 1,\ R = 0$; then:- $Q = 1$ & $\bar{Q} = 0$

∴ Ex:- $\boxed{\text{if}\ S = 0,\ R = 0;\ \text{then}\ Q = 1 \ \&\ \bar{Q} = 0}$ → memory

Case: 3:-

if $S=1, R=1$ then:- $Q=0$ & $\bar{Q}=0$

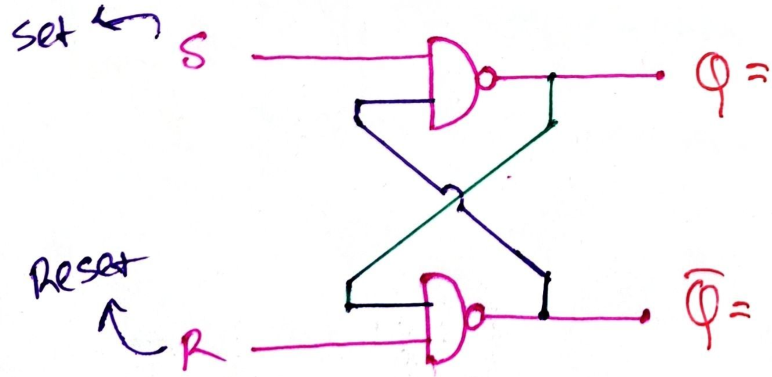
Ex: if:- $S=0, R=0$; then $Q=0$ & $\bar{Q}=1$
$Q=1$ & $\bar{Q}=0$

"Not used" cz its Break the rules.

Truth Table for SR Latch:- (NOR)

S	R	Q	$\bar{Q}$
0	0	Memory	Memory
0	1	0	1
1	0	1	0
1	1	Not used	Not used

SR NAND Latch:-



Truth table for NAND Gate:-

A	B	Y
$\boxed{0}$	0	$\boxed{1}$
$\boxed{0}$	1	$\boxed{1}$
1	0	1
1	1	0

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Analyse the Latch:-

Case 1:-

if $S=0, R=1$ then, $Q=1$ & $\bar{Q}=0$

For:- if $\boxed{S=1, R=1 \quad \text{then, } Q=1 \ \& \ \bar{Q}=0}$ → memory

Case: 2:-

if $S=1, R=0$ then:- $Q=0$ & $\bar{Q}=1$

For:- if $\boxed{S=1, R=1 \quad \text{then:- } Q=0 \ \& \ \bar{Q}=1}$ → memory

Case 3:-

if $S=0, R=0$, then:- $Q=1$ & $\bar{Q}=1$ → Not used

Truth table for SR latch (NAND):-

S	R	Q	$\bar{Q}$
0	0	Not used	
0	1	1	0
1	0	0	1
1	1	memory	

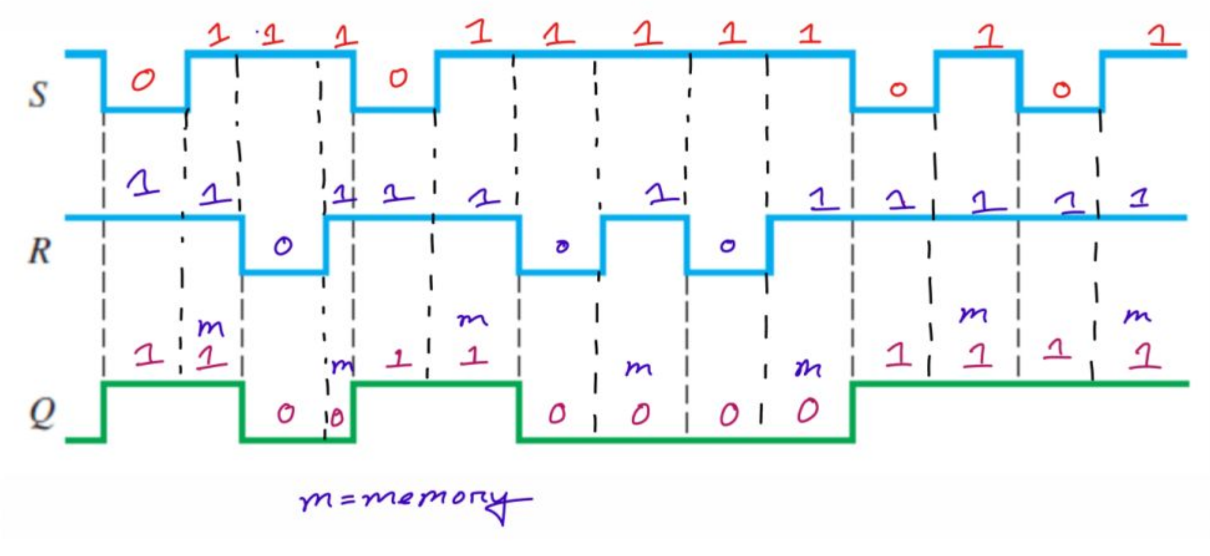
Exercise 1:

Determine the **Output(Q) Waveform** for **NAND** ***SR Latches*** that are initially **LOW**.

➔ **We Know,**

Truth table for SR Latch (NAND):-

S	R	Q	$\bar{Q}$
0	0	Not used	
0	1	1	0
1	0	0	1
1	1	memory	



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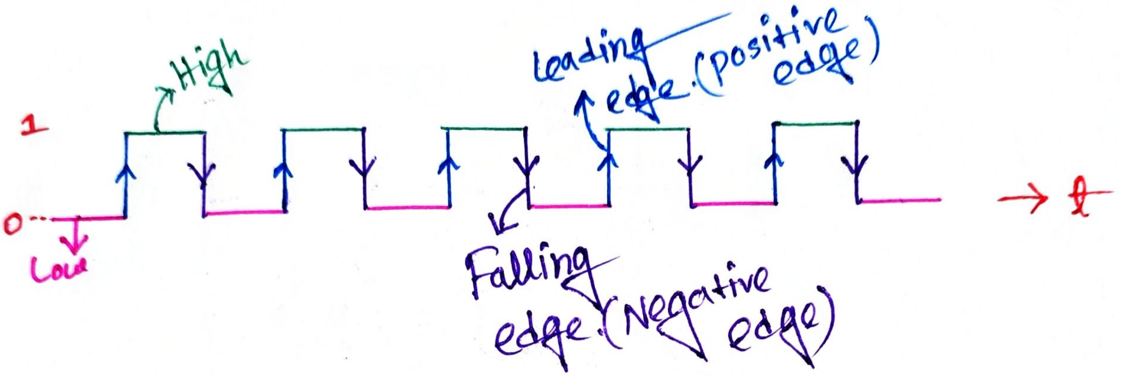
#Clock

Clock:-

⇒ It's a signal that goes from Low to High then again Low and repeats.



Triggering Methods:-

⇒ It's usually refer to how flip-flops and other Sequential elements change their states.

There are two types:-

1. Level-triggered.
2. Edge-triggered.

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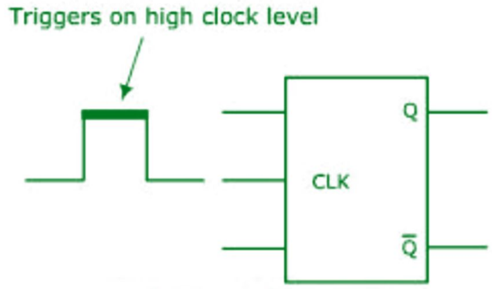
Level - triggered :-

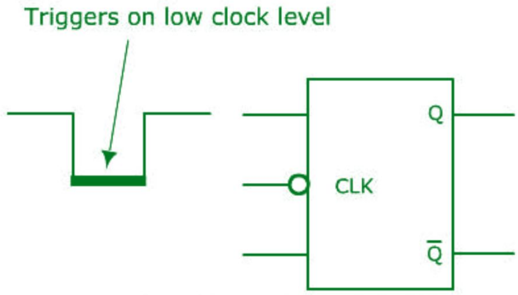
⇒ This flip-flops respond to the level of the clock signal, either high (1) or Low (0).

Block Diagram for high Level :-



High Level Triggering

Block Diagram for Low Level :-

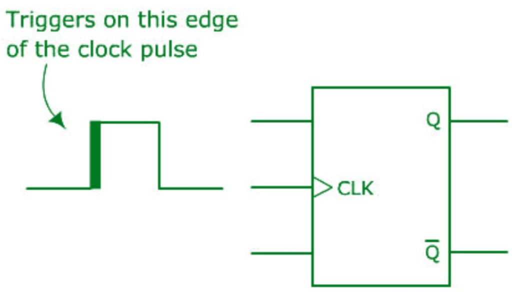


Low Level Triggering

Edge - Triggered :-

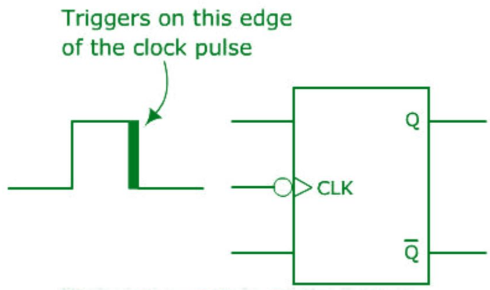
⇒ these flip-flops change state on a specific edge of the clock signal, either the rising edge (positive edge) or the falling edge (Negative edge)

Block Diagram For (+ve edge)



Positive Edge Triggering

Block Diagram for (-Ve edge)



Negative Edge Triggering

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FLIP FLOP

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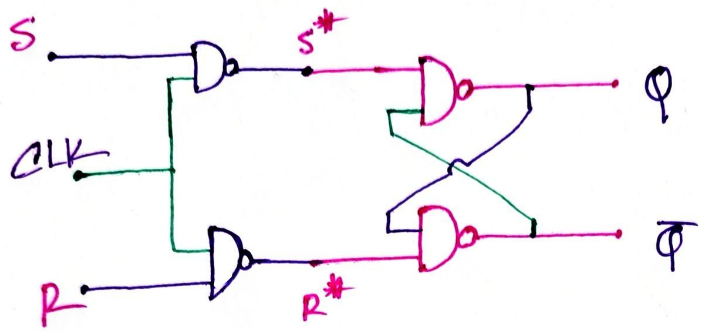
SR FLIP FLOP

SR FLIP FLOP



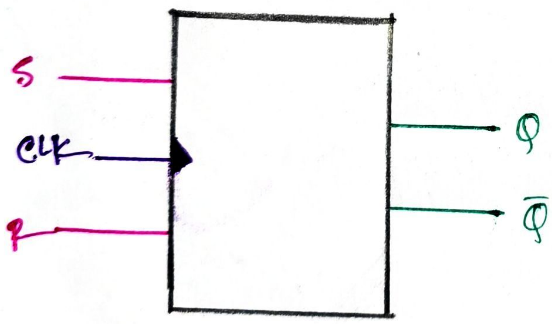
Truth table of SR Latch (NAND)

S^*	R^*	Q	$\bar{Q}$
0	0	Not used	
0	1	1	0
1	0	0	1
1	1	memory	

$\therefore S^* = (\overline{S \cdot CLK}) = \bar{S} + \overline{CLK}$

$\therefore R^* = (\overline{R \cdot CLK}) = \bar{R} + \overline{CLK}$

Block Diagram of SR Flip-Flop:-



Truth table for SR Flip-Flop:-

CLK	S	R	Q	$\bar{Q}$
0	X	X	memory	
1	0	0	memory	
1	0	1	0	1
1	1	0	1	0
1	1	1	Not used	

Analyse the truth table:-

Case: 1:-

CLK = 0;

$S^* = \bar{S} + 1 = X + 1 = 1$

$R^* = \bar{R} + 1 = X + 1 = 1$

$\therefore Q$ & $\bar{Q}$ = memory

Case: 2:-

CLK = 1;

$S^* = \bar{S}$

$R^* = \bar{R}$

Let, $S = 0, R = 0$ —(1)

$\therefore S^* = 1$

$R^* = 1$

$\therefore Q$ & $\bar{Q}$ = memory

Case: 3:-

From eq (1):-

Let, $S = 0, R = 1$

$\therefore S^* = 1$

$R^* = 0$

$\therefore Q = 0$ & $\bar{Q} = 1$

Case 4:-

From eq (1):-

Let, $S = 1, R = 0$

$\therefore S^* = 0$

$R^* = 1$

$\therefore Q = 1$ & $\bar{Q} = 0$

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Characteristic Truth Table for SR Flip-Flop:-

Q_n	S	R	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	Invalid (x)
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	Invalid (x)

Truth table for SR-Flip-flop

clk	S	R	Q_{n+1} → next state
0	X	X	Q_n → p. state
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	Invalid

Excitation table:-

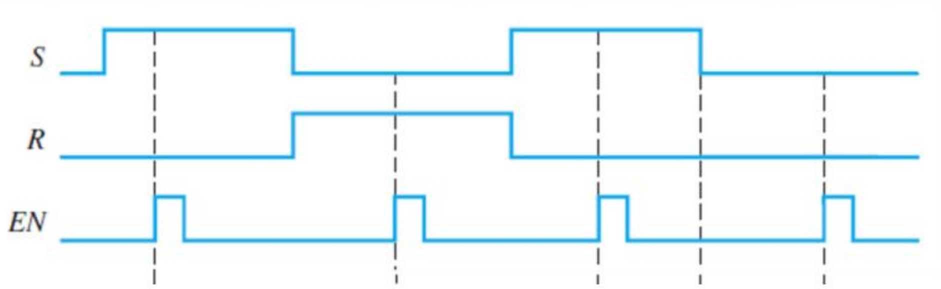
Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

K-map for Q_{n+1}:-

Q_n \ SR	00	01	11	10
0	0	0	X	1
1	1	0	X	1

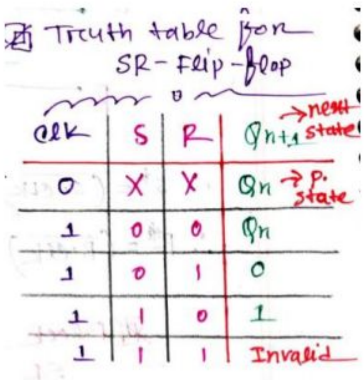
$\therefore Q_{n+1} = Q_n\bar{R} + S$

Exercise 2:



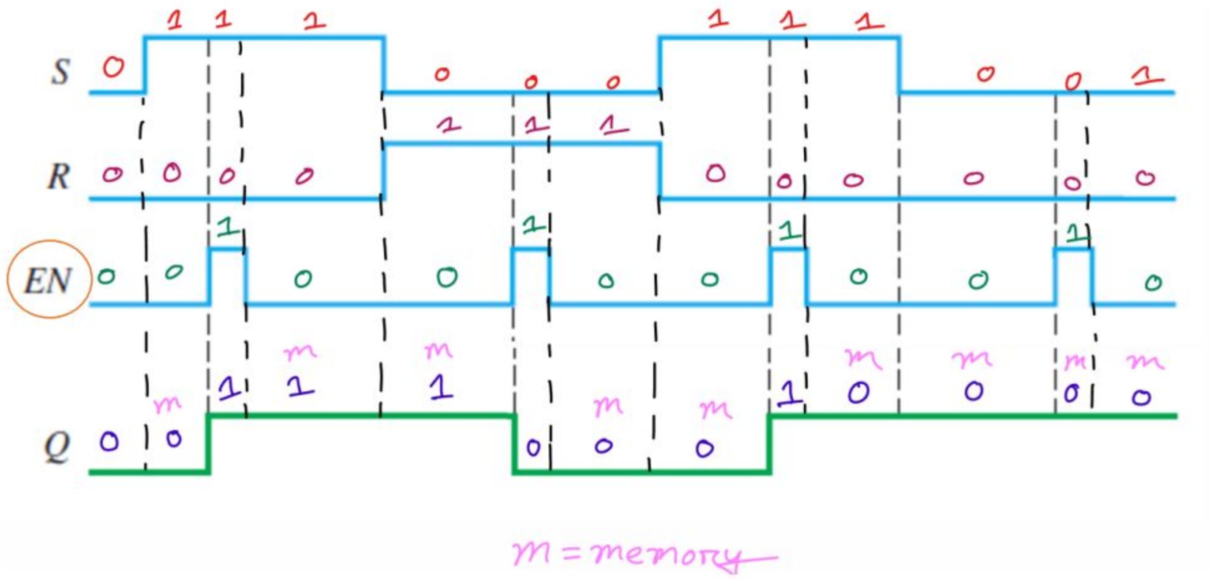
Determine the **Output(Q) Waveform** for ***SR FLIP FLOPS*** that are initially **Reset**

➔ **We Know,**



Truth table for SR-Flip-flop

Clk	S	R	Q_{n+1} → next state
0	X	X	Q_n → p. state
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	Invalid



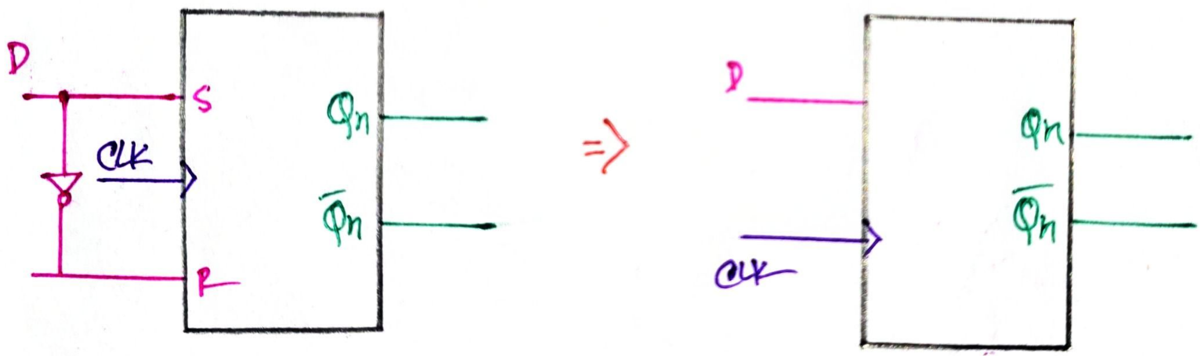
D-Flip Flop

D FLIP FLOP:-

⇒ In "NAND" SR Latch the invalid input condition of S=0, R=0. It is the drawback of the SR Latch.

To avoid the drawback we need an inverter to connect ~~the~~ between the set and Reset inputs. It ensure that at the same time S and R never equal to 1.

Logic Circuit with Block Diagram



T.T for D.F.F:-

CLK	D	Q_{n+1}
0	X	Q_n
1	0	0
1	1	1

Truth table for SR FLIP-FLOP:-

CLK	S	R	Q	$\bar{Q}$
0	X	X	memory	
1	0	0	memory	
1	0	1	0	1
1	1	0	1	0
1	1	1	Not used	

Characteristic Table for D-flip-flop:-

Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

$\boxed{\therefore Q_{n+1} = D}$

We know:-

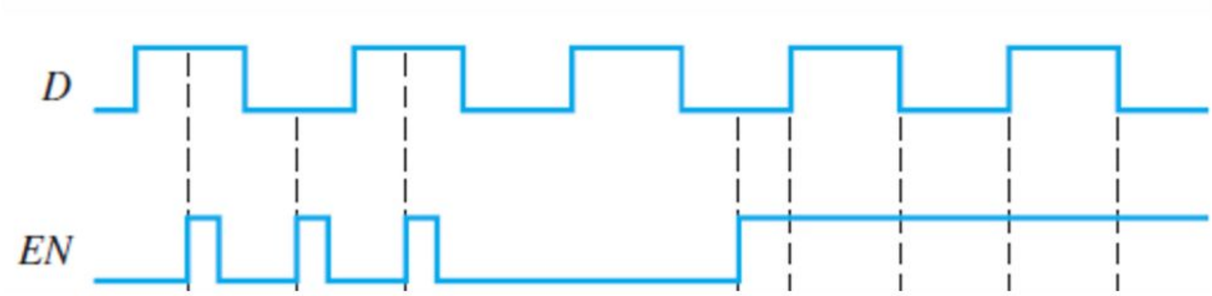
T.T for D.f.f

CLK	D	Q_{n+1}
0	X	Q_n
1	0	0
1	1	1

Excitation Table for D-flip-flop:-

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Exercise 3:

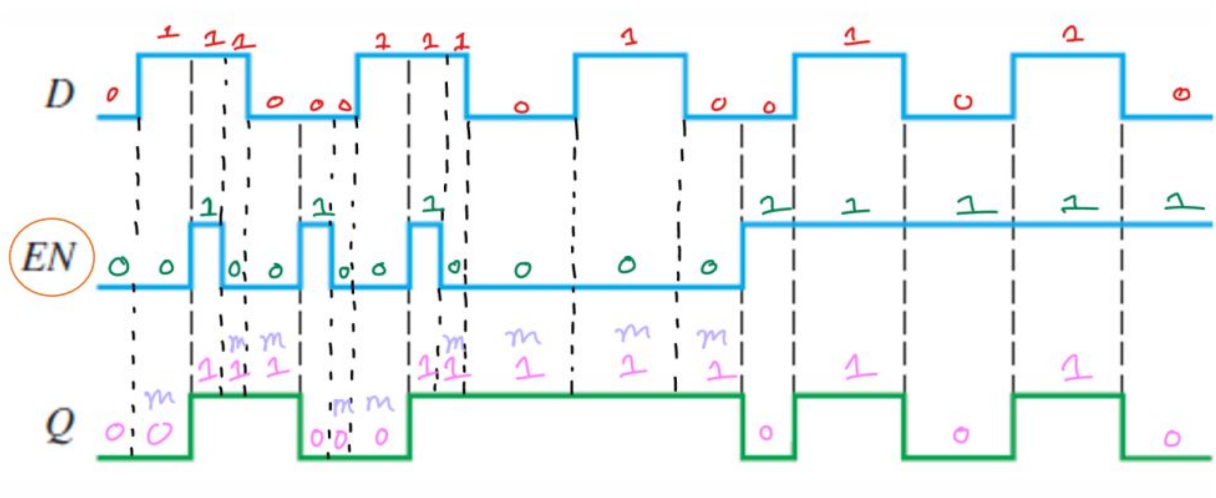


Determine the **Output(Q) Waveform** for ***D FLIP FLOPS*** that are initially **Reset**

➔ **We Know,**

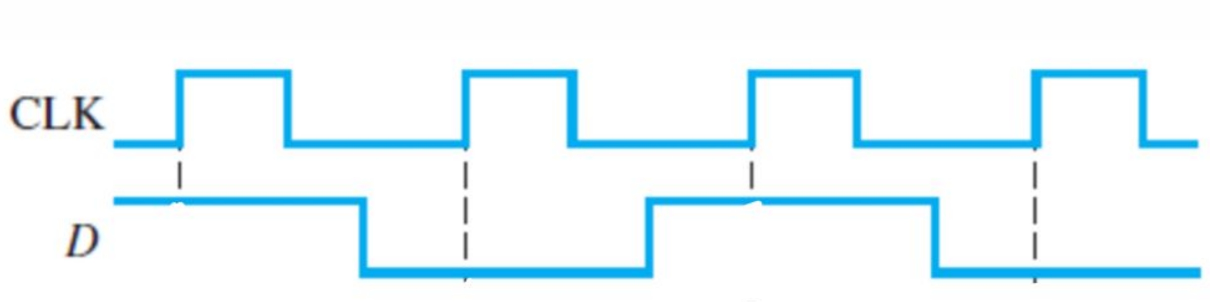
T.T for D.F.F

CLK	D	Q_{n+1}
0	X	Q_n
1	0	0
1	1	1



m = memory

Exercise 4:

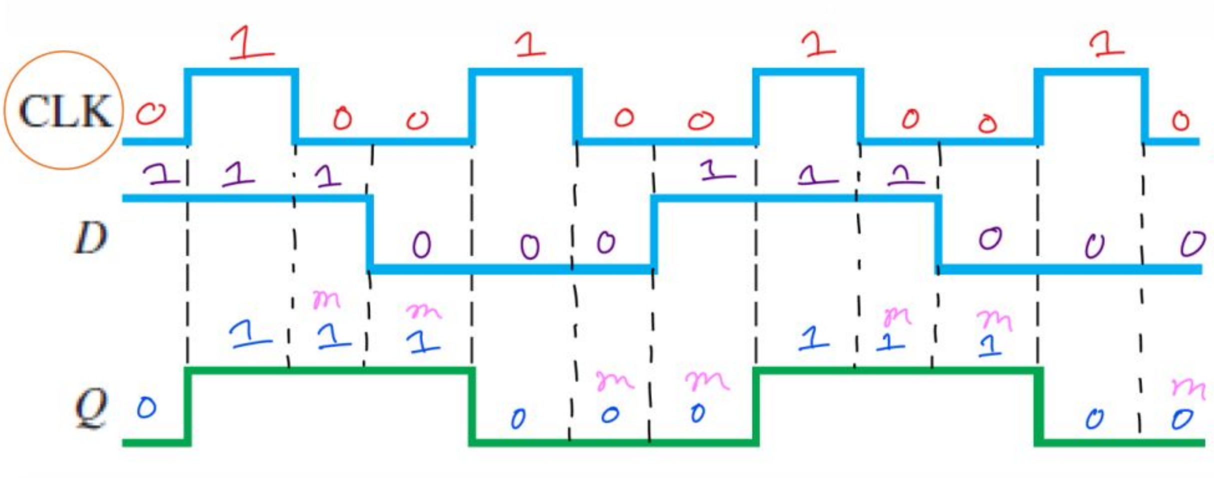


Determine the **Output(Q) Waveform** for ***D FLIP FLOPS*** that are initially **Reset**

➔ **We Know,**

T.T for D.F.F.

CLK	D	Q_{n+1}
0	X	Q_n
1	0	0
1	1	1



m = memory

Sub :

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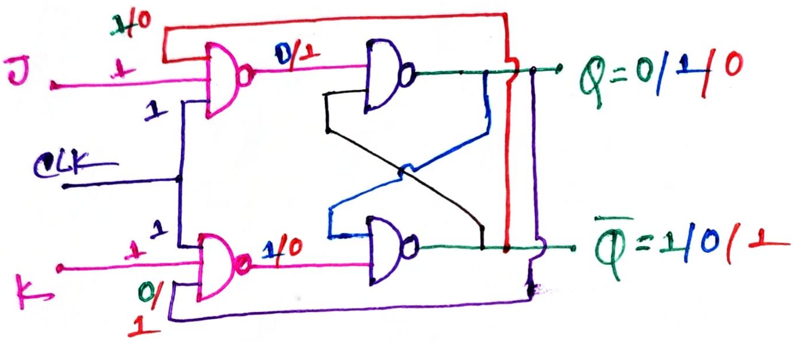
JK FLIP FLOP

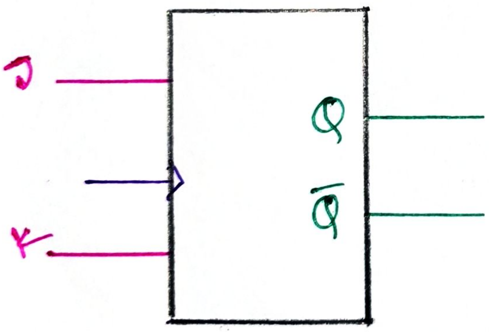
JK Flip-Flop:-

⇒ The JK flip flop is similar to the SR flipflop but there is no change in state when J=0 & K=0.

Logic Circuit



Block Diagram:-



T.T for J.K f.f

CLK	J	K	Q_{n+1}
0	x	x	Q_n (memory)
1	0	0	Q_n (memory)
1	0	1	0
1	1	0	1
1	1	1	$\overline{Q_n}$ (toggle)

similar to SR f.f

Analyse the T.T.

Case 5:-

CLK = 1

Let $Q=0, \overline{Q}=1$

Now $J=1, K=1$

$\therefore Q = 0, 1, 0, 1, \ldots$ &

$\overline{Q} = 1, 0, 1, 0, \ldots$

$\therefore Q_{n+1} = 0$
1
0
1
....
$\overline{Q_n}$

Sub : Time : Date : / /

Characteristic Table:-

Q_n	J	K	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

We know,
T.T. for JK.ff

CLK	J	K	Q_{n+1}
0	X	X	Q_n
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	$\overline{Q_n}$

K-map for Q_{n+1}:-

Q_n \ JK	00	01	11	10
0	0	0	1	1
1	1	0	0	1

$\therefore Q_{n+1} = Q_n\overline{K} + \overline{Q_n}J$

Excitation Table:-

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

K-map for J

Q_n \ Q_{n+1}	0	1
0	0	1
1	X	X

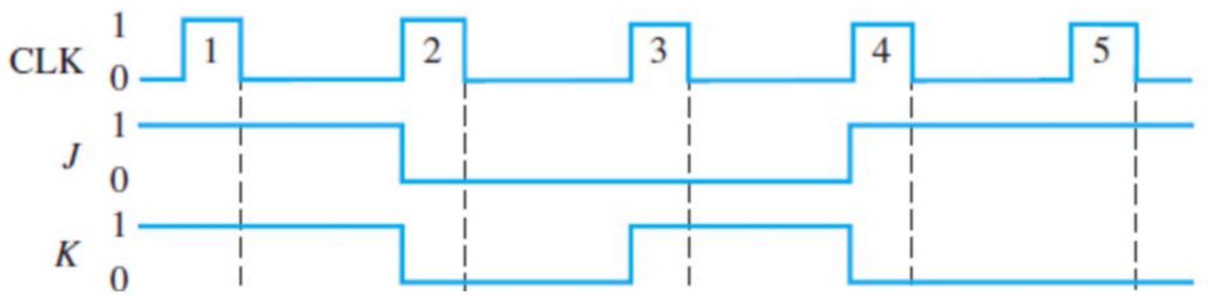
$J = Q_{n+1}$

K-map for K

Q_n \ Q_{n+1}	0	1
0	X	X
1	1	0

$K = \overline{Q_{n+1}}$

Exercise 5:

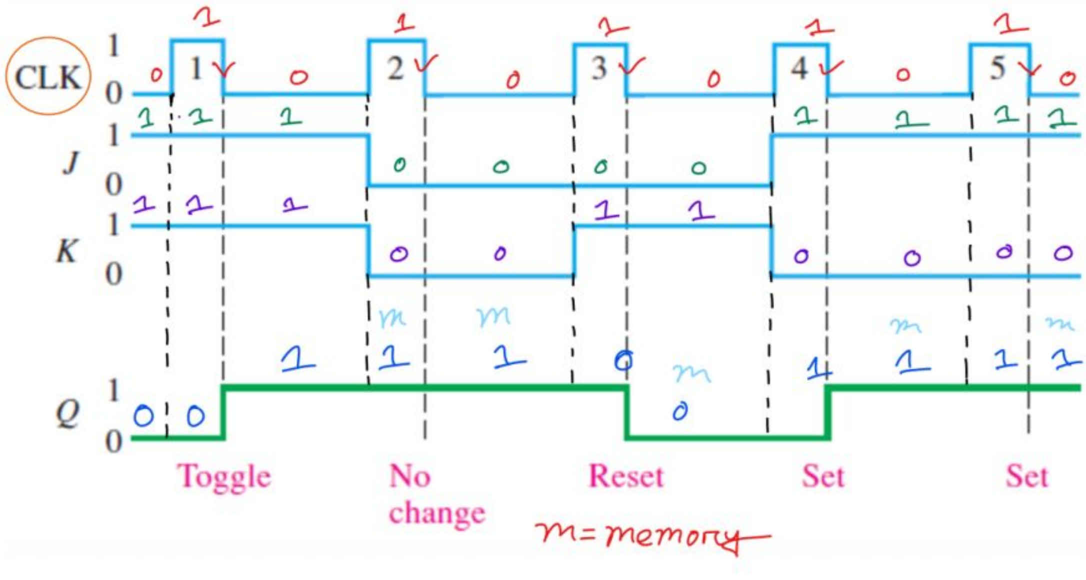


Determine the **Output(Q) Waveform** for ***JK FLIP FLOPS*** that are initially **Reset** and the flip flop is **negative edge triggered.**

➔ **We Know,**

T.T for J.K f.f

CLK	J	K	Q_{n+1}
0	x	x	Q_n (memory)
1	0	0	Q_n (memory)
1	0	1	0
1	1	0	1
1	1	1	$\overline{Q_n}$ (toggle)



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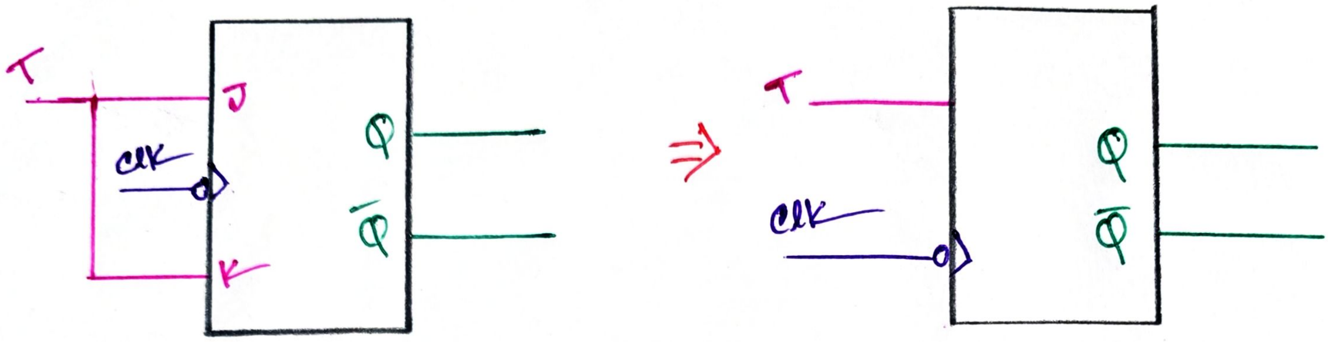
T- Flip Flop

T-flip-flop:-

Logic Circuit & Block Diagram:-



T.T for T.FF:-

clk	T	Q_{n+1}
0	X	Q_n (memory)
1	0	Q_n (memory)
1	1	$\bar{Q}_n$ (Toggling)

Characteristic Table:-

Q_n	T	Q_{n+1}
$\boxed{0}$	0	$\boxed{0}$
$\boxed{0}$	1	$\boxed{1}$
$\boxed{1}$	0	$\boxed{1}$
$\boxed{1}$	1	$\boxed{0}$

$\therefore Q_{n+1} = Q_n \oplus T$

Excitation Table:-

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

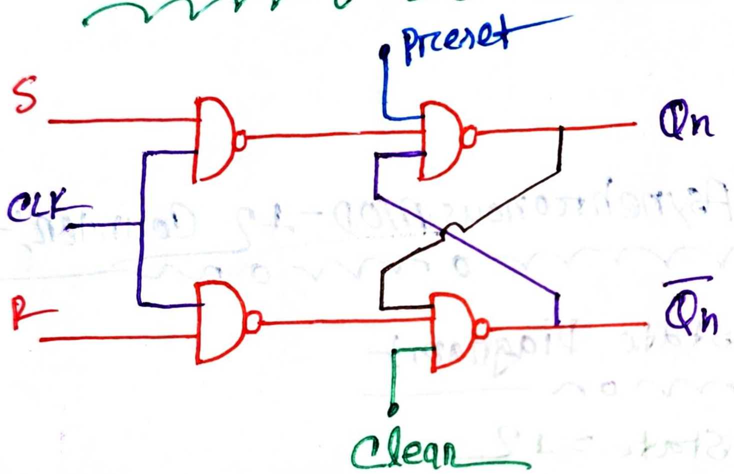
$T = Q_n \oplus Q_{n+1}$

Preset & Clear Inputs

1. They are the direct inputs or overriding inputs or asynchronous inputs.

2. The synchronous inputs are S, R, J, K, D, & T

Logic Circuit:



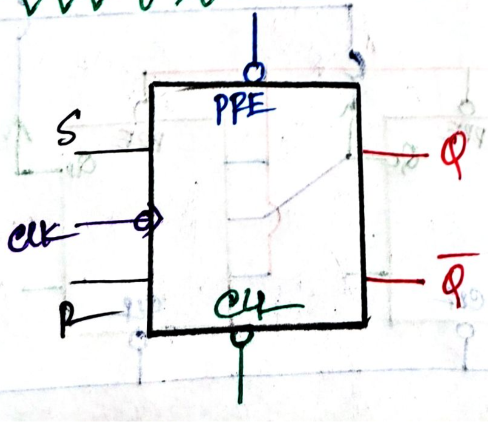
if, preset = 0, Then $Q_n = 1$ & $\overline{Q_n} = 0$

if, Clear = 0, Then $Q_n = 0$ & $\overline{Q_n} = 1$

What ever be the value of clock & synchronous inputs.

Block Diagram:

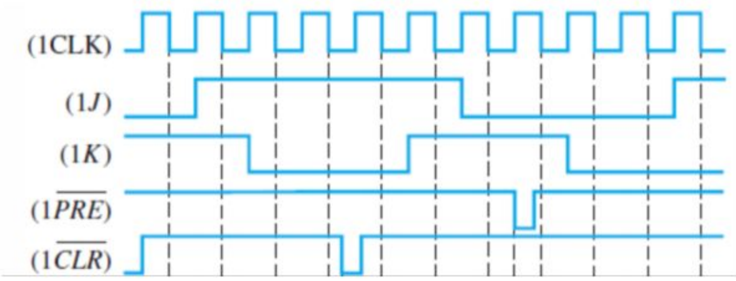
For Active Low:



Truth Table

PR	CLR	Qn
0	0	Not used
0	1	1
1	0	0
1	1	F.F will Perform Normally.

Exercise 6:



Determine the **Output(Q) Waveform** for ***JK FLIP FLOPS*** that are initially **Reset** and the flip flop is **negative edge triggered.**

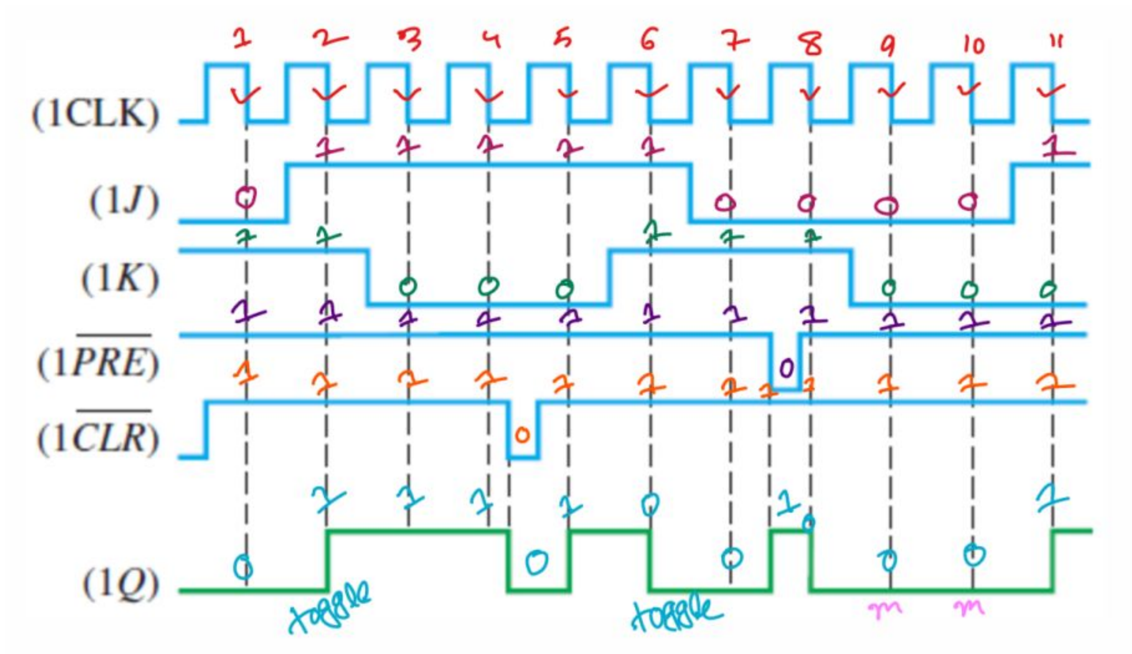
➔ **We Know,**

T.T for J.K F.F

CLK	J	K	Q_{n+1}
0	x	x	Q_n (memory)
1	0	0	Q_n (memory)
1	0	1	0
1	1	0	1
1	1	1	$\overline{Q_n}$ (toggle)

Truth Table

PR	CLR	Q_n
0	0	Not used
0	1	1
1	0	0
1	1	F.F will Perform Normally



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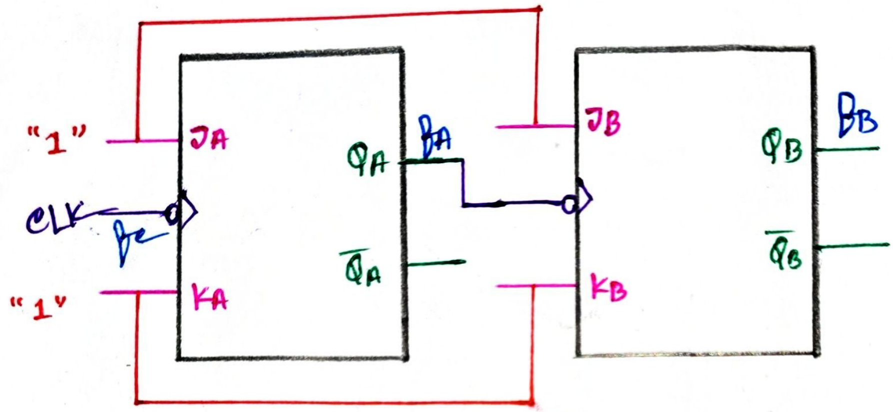
Counters

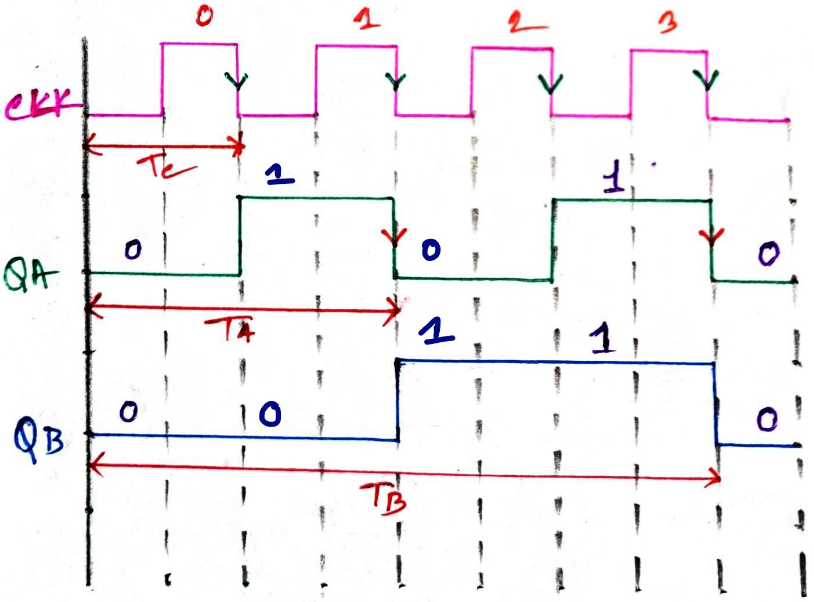
Counter :-

⇒ It's a Sequential circuit and it just simply counts.

Example :



Analyse the Input & output clock frequency



Truth Table :-

CLK	Q_B	Q_A
0	0	0
1	0	1
2	1	0
3	1	1

Types of Counters:-

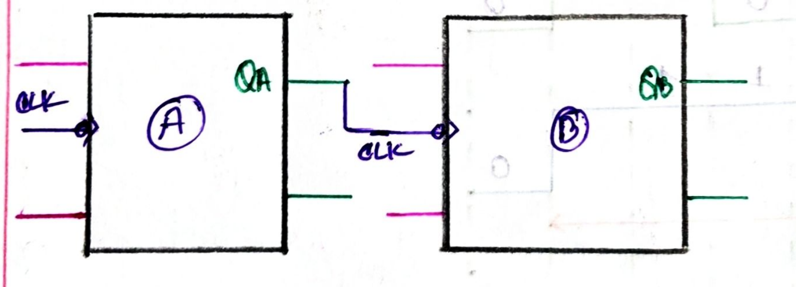
⇒ There are two types:-

1. Asynchronous Counters (Ripple Counters)
2. Synchronous Counters.

Asynchronous Vs Synchronous:-

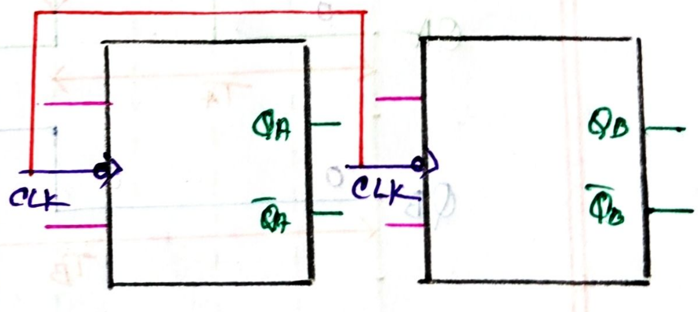
Asynchronous

⇒ Flip Flop are Connected in such a way that the O/P of 1st flip flop drives the clock of next flip flop



Synchronous:-

⇒ There is no Connection between O/P of 1st flip flop and clock of next flip flop. F.F are clocked Simultaneously



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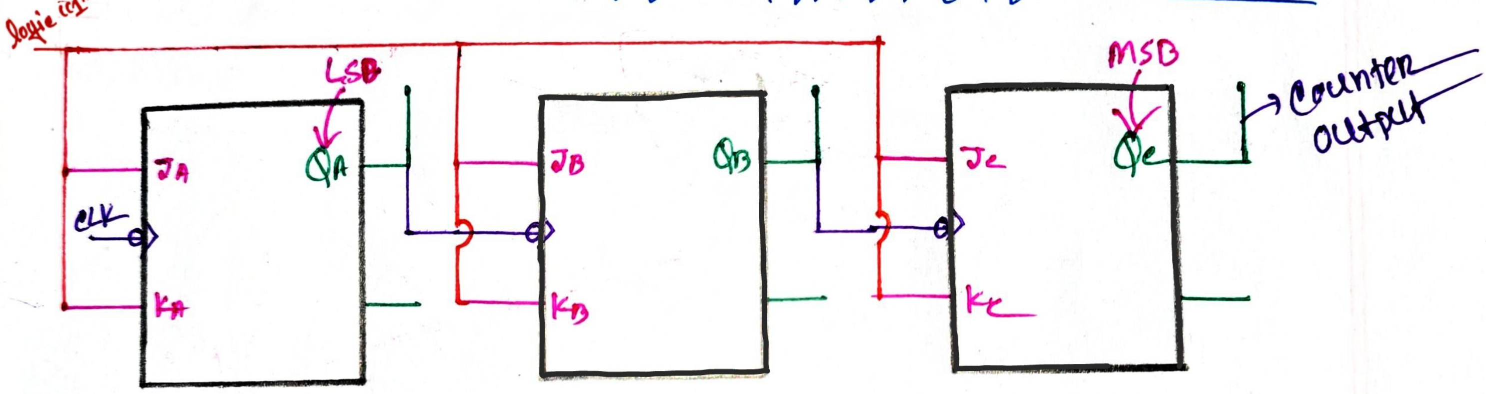
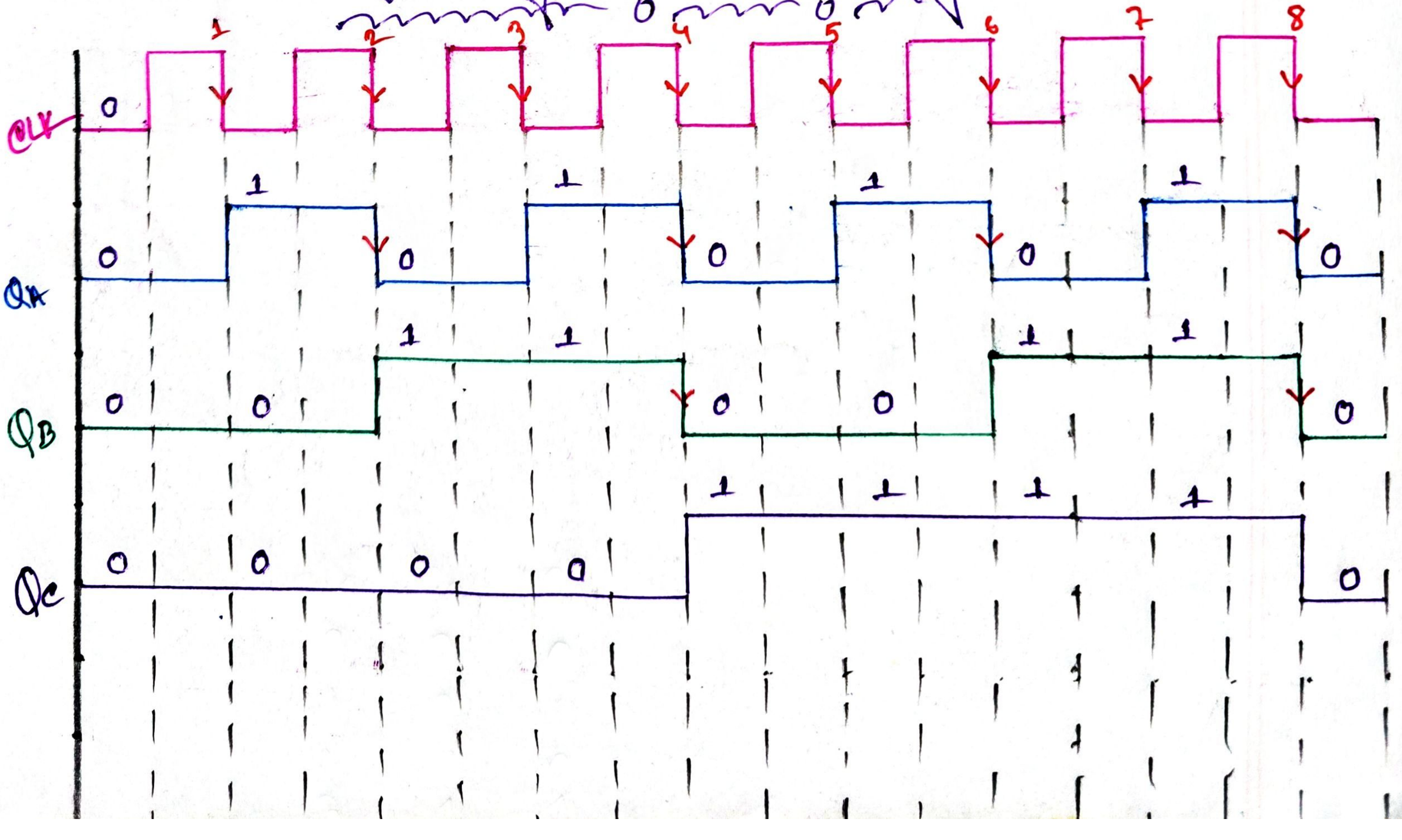
Classification of Counters:-

1. Up Counter
2. Down Counter
3. Up/Down Counter.

3 Bit Asynchronous Up Counter:-



Analyse the Clock Diagram:-

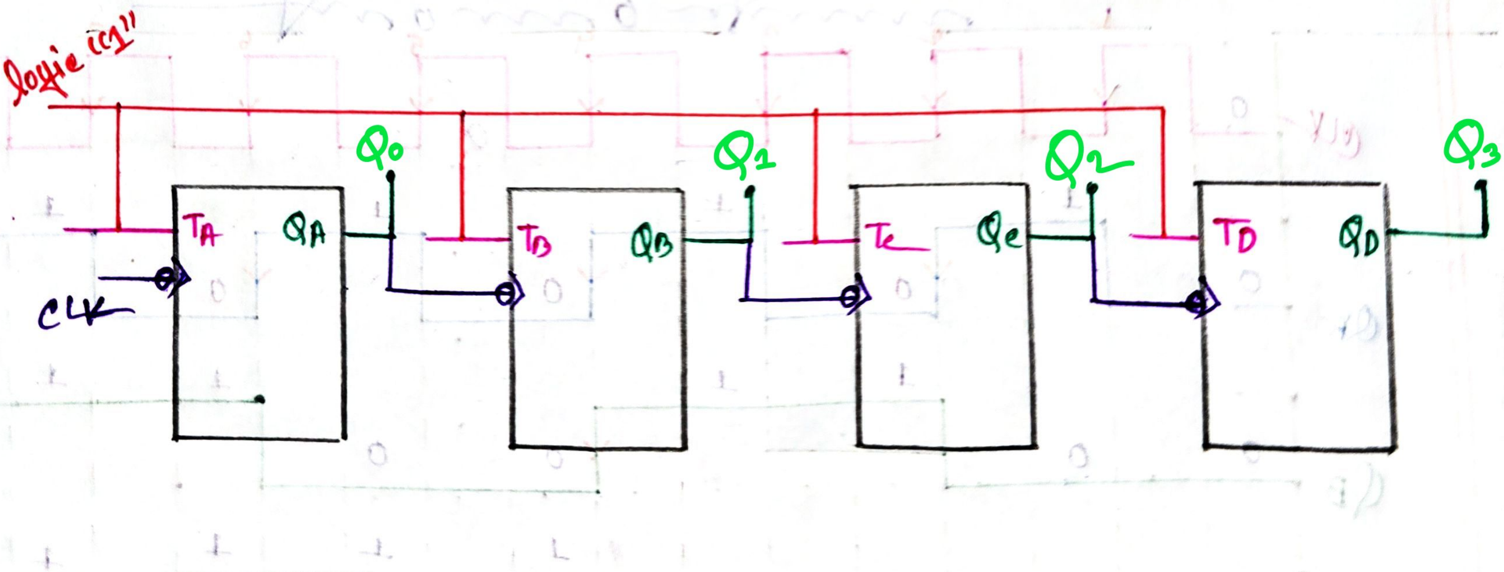


Sub : Time : Date : / /

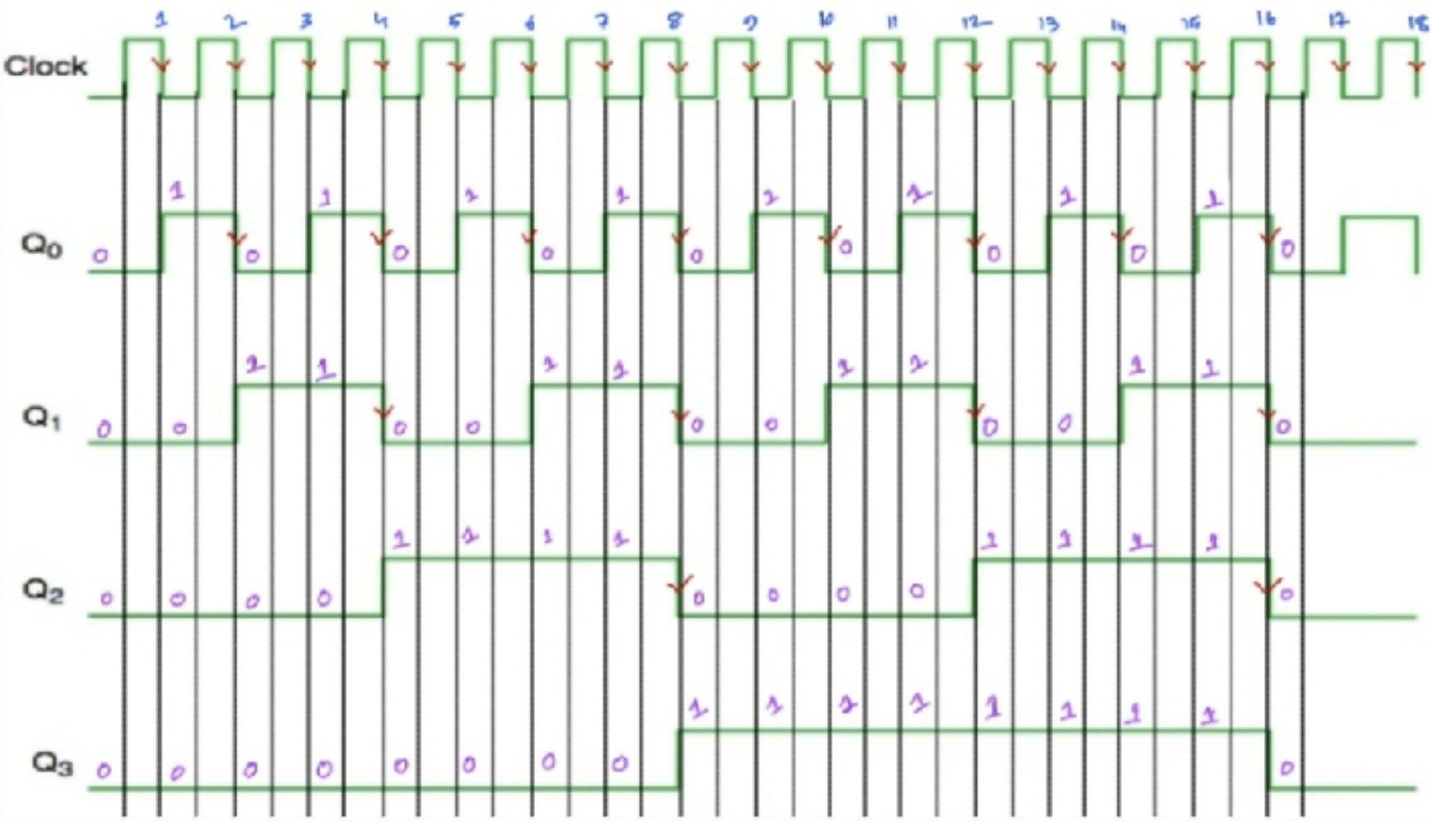
Table for 3 bit Asys. Up Counter:-

Clock	Q_C	Q_B	Q_A	Decimal eq
Initally	0	0	0	0
1st (↓)	0	0	1	1
2nd (↓)	0	1	0	2
3rd (↓)	0	1	1	3
4th (↓)	1	0	0	4
5th (↓)	1	0	1	5
6th (↓)	1	1	0	6
7th (↓)	1	1	1	7

4-Bit Asynchornous Up Counter:-



Analyse the Clock Diagram

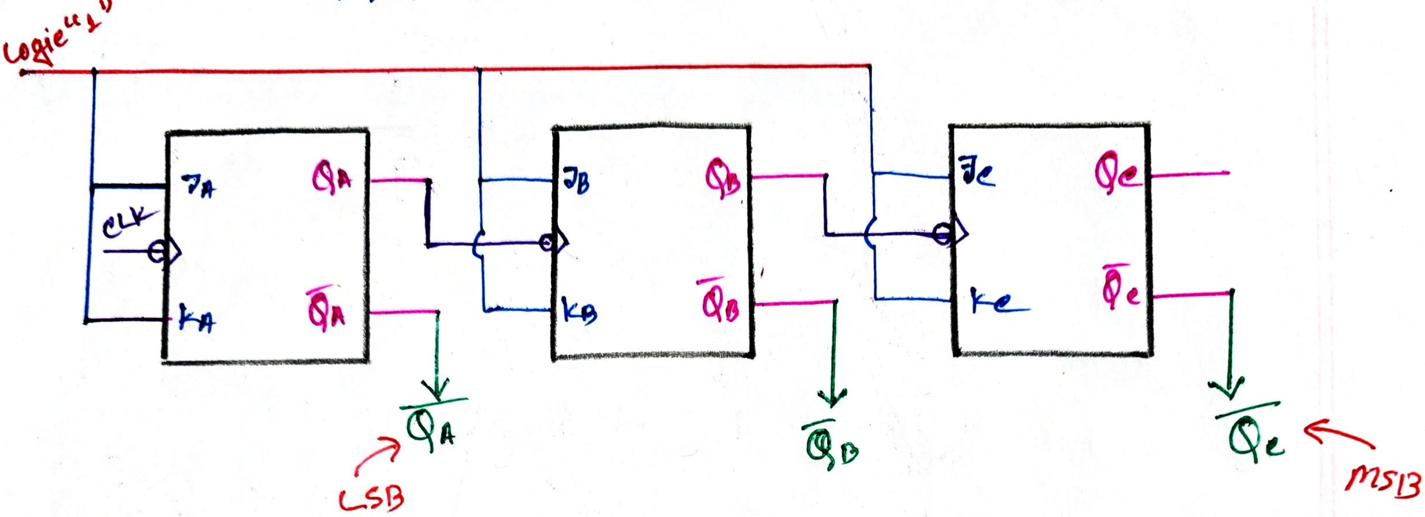


Truth table for 4 bit asynchronous Up Counter

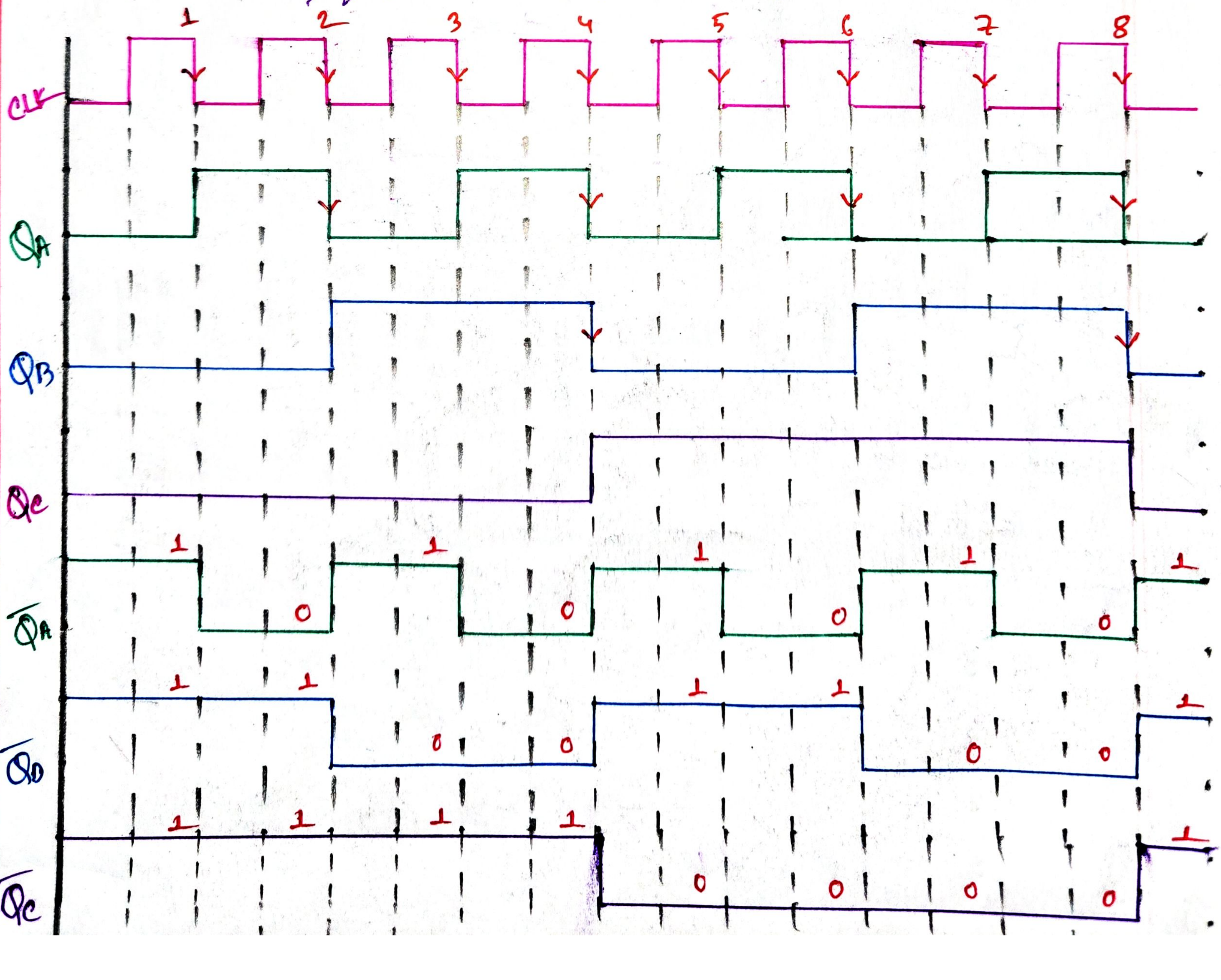
Clock Cycles	Output Bits				Decimal Value
	QA	QB	QC	QD	
1	0	0	0	0	0
2	0	0	0	1	1
3	0	0	1	0	2
4	0	0	1	1	3
5	0	1	0	0	4
6	0	1	0	1	5
7	0	1	1	0	6
8	0	1	1	1	7
9	1	0	0	0	8
10	1	0	0	1	9
11	1	0	1	0	10
12	1	0	1	1	11
13	1	1	0	0	12
14	1	1	0	1	13
15	1	1	1	0	14
16	1	1	1	1	15

Sub :

3 Bit Down Counters: (Asynchronous)



Analyse the clock Diagram:-



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State Diagram of a Counter:-

⇒ 2-Bit Up Counter:-

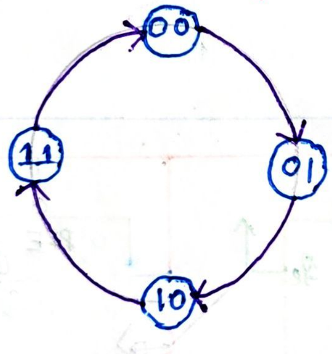
→ Total state for 2 bits = 4

→ MAX Count = 4 − 1 = 3

The combinitions are:-

Q_B	Q_A	Count
0	0	0
0	1	1
1	0	2
1	1	3

State Diagram:-



⇒ 2-Bit Down Counter:-

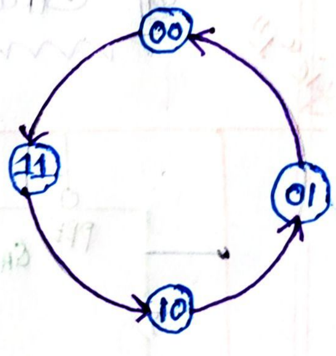
→ Total State for 2bit = 4

→ max Count = 4 − 1 = 3

The combinations are:-

Q_B	Q_A	Count
1	1	3
1	0	2
0	1	1
0	0	0

State Diagram:-



3-bit Up-down Counter:-

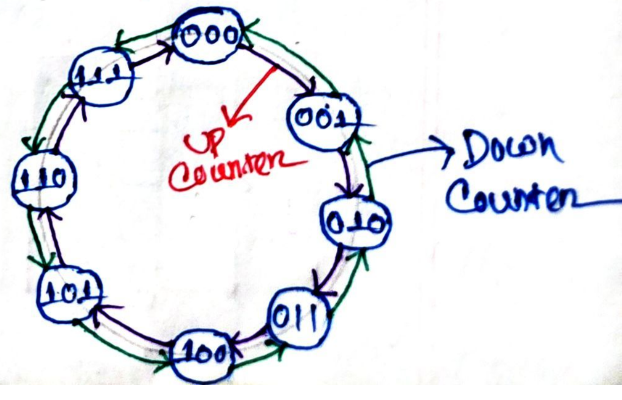
⇒ Total state for 3 bits = 8

⇒ MAX Count = 8 − 1 = 7

The Combinations are:-

Q_C	Q_B	Q_A	Count
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

State Diagram:-



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MOD Counters:-

⇒ MOD Counters are cascaded counter circuits which count to a set modulus value before resetting.

Some of them are:-

1. Asynchronous Counter for 2 bit (known as MOD-4)
2. Asynchronous Counter for 3 bit (known as MOD-8)
3. Asynchronous Counter for Decade (known as MOD-10)
4. MOD-12 ripple counter
5. MOD-6 ripple counter

MOD-6 Ripple Counter using MOD-8 Counter:-

T.T for MOD-8

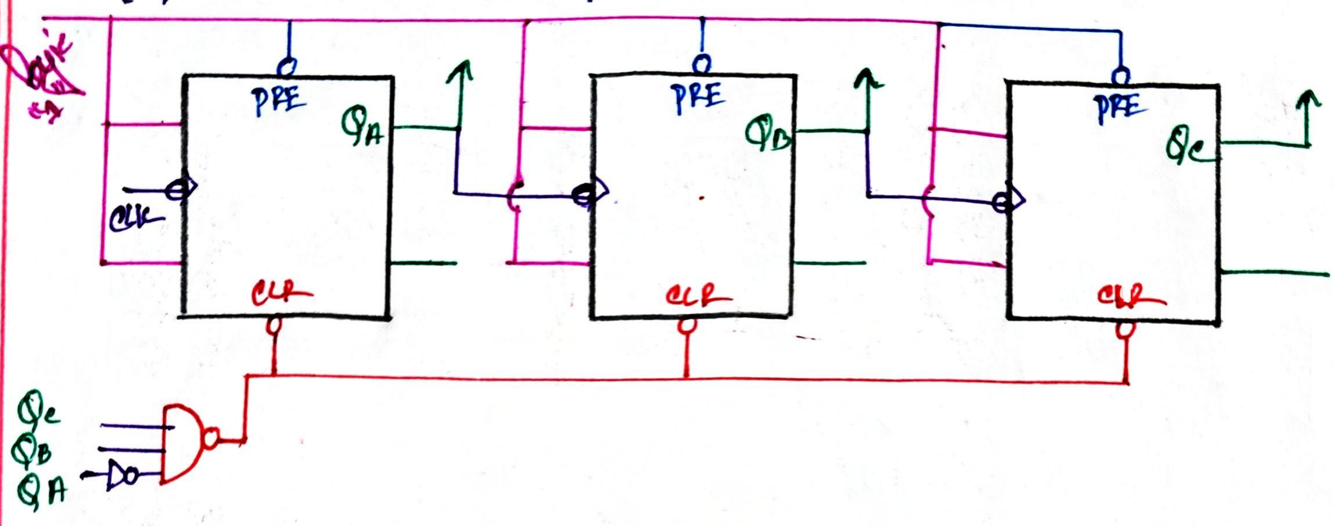
C	B	A	Decimal Value
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Max Count = 6 − 1
= 5

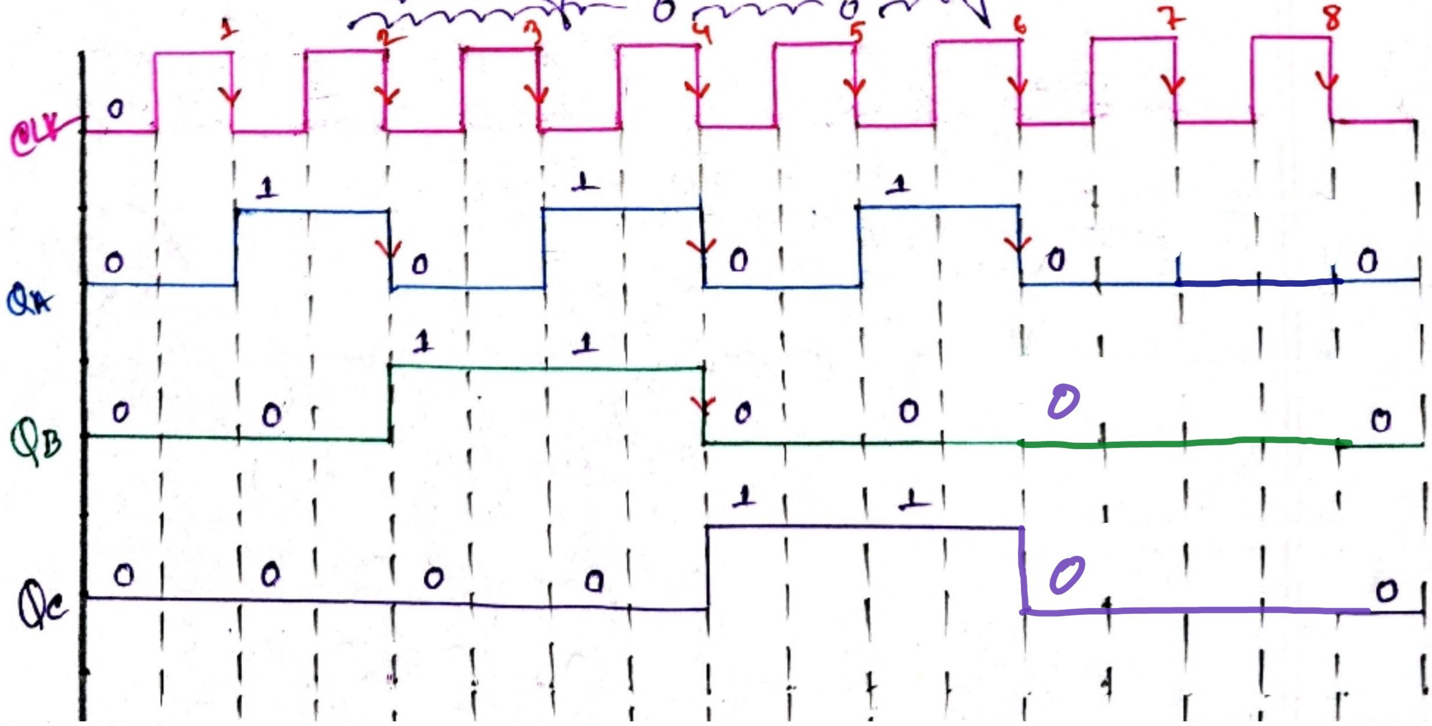
Sub :

Time : Date : / /

Logic circuit



Analyse the Clock Diagram:-



Important point's:-

1. Negative edge triggered → Q is clock → Up Counter
2. Positive edge triggered → $\overline{Q}$ in clock → Up Counter
3. Negative edge triggered → $\overline{Q}$ is clock → Down Counter
4. positive edge triggered → Q is clock → Down Counter

Day

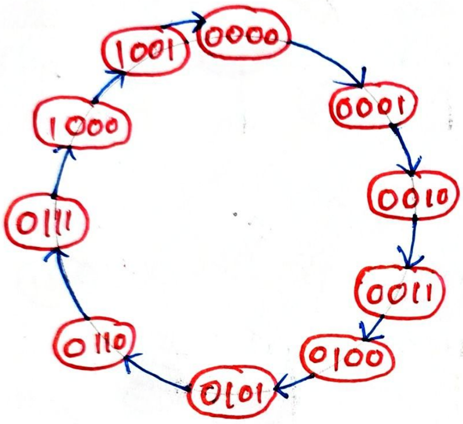
Sub : Time : Date : / /

#Decade (BCD) Ripple Counters:—

(MOD 10)

⇒ Draw the State Diagrams:—

here, No. of State = 10

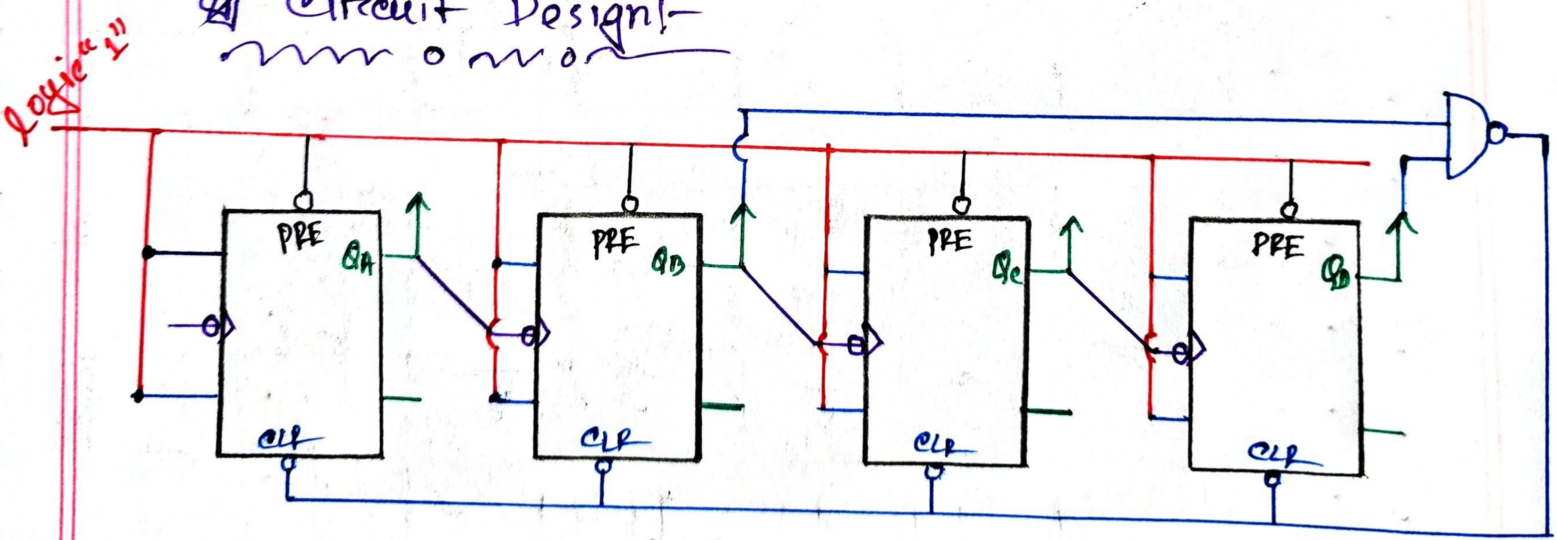


Max Count = 10 − 1
= 9

Truth Table for MOD16

CLK	Q_D	Q_C	Q_B	Q_A	BCD
1	0	0	0	0	0
2	0	0	0	1	1
3	0	0	1	0	2
4	0	0	1	1	3
5	0	1	0	0	4
6	0	1	0	1	5
7	0	1	1	0	6
8	0	1	1	1	7
9	1	0	0	0	8
10	1	0	0	1	9
11	$\boxed{1}$	0	$\boxed{1}$	0	10
12	1	0	1	1	
13	1	1	0	0	
14	1	1	0	1	
15	1	1	1	0	

☒ Circuit Design:—



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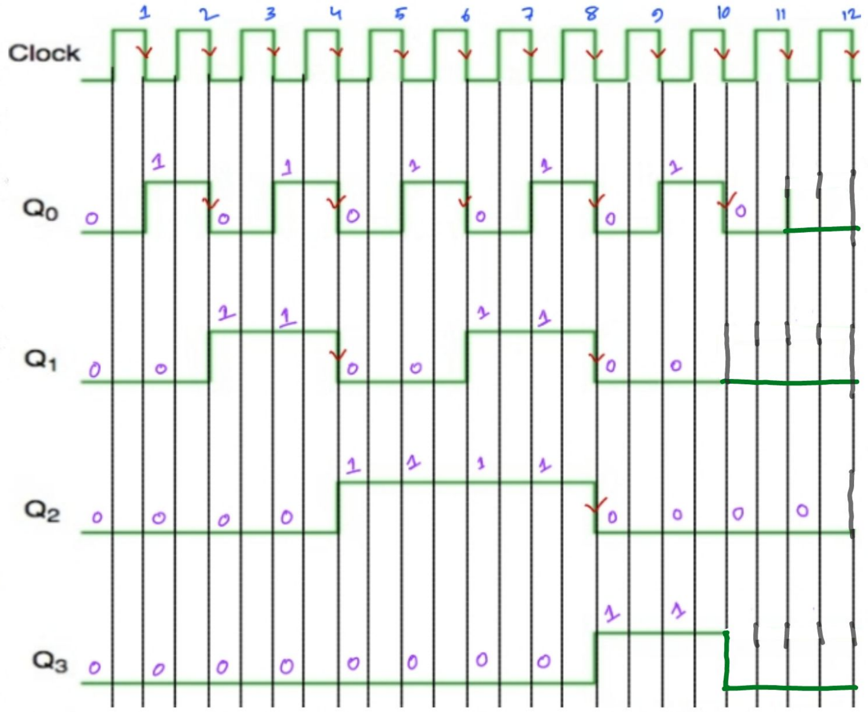


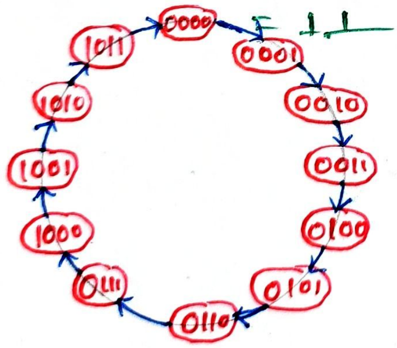
Asynchronous MOD-12 Counter:-

⇒ Draw the state Diagram:-

here, No. of State = 12

Max count = 12 − 1

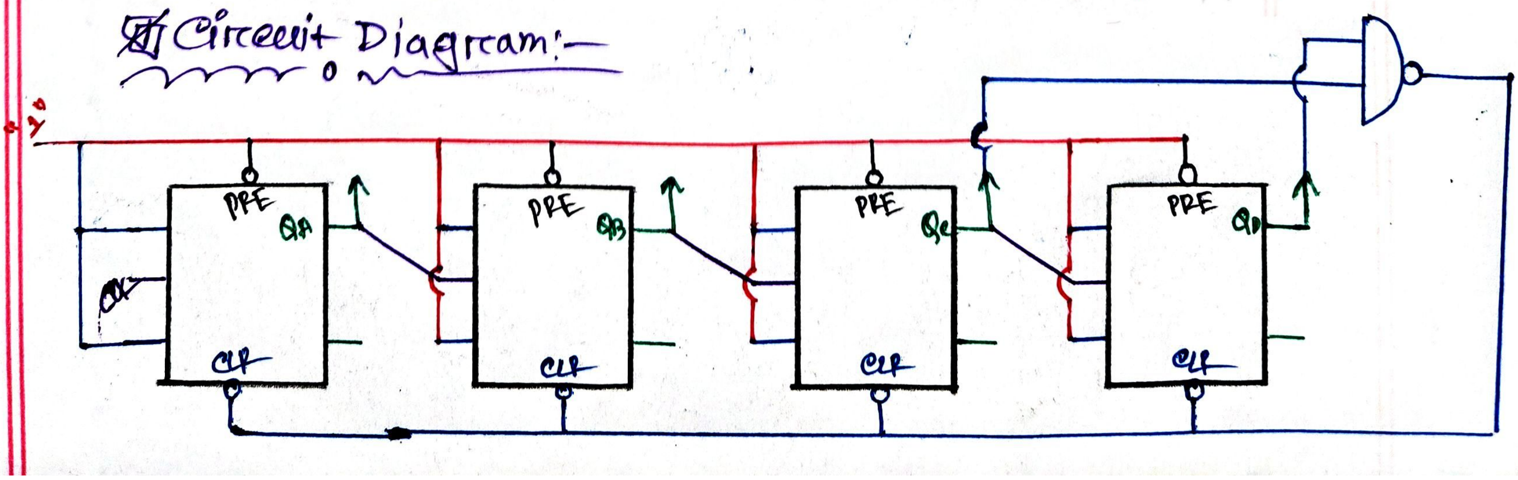
= 11



Truth Table for MOD16

Clk	Q_D	Q_C	Q_B	Q_A	BCD
1	0	0	0	0	0
2	0	0	0	1	1
3	0	0	1	0	2
4	0	0	1	1	3
5	0	1	0	0	4
6	0	1	0	1	5
7	0	1	1	0	6
8	0	1	1	1	7
9	1	0	0	0	8
10	1	0	0	1	9
11	1	0	1	0	10
12	1	0	1	1	11
13	$\boxed{1}$	$\boxed{1}$	0	0	12
14	1	1	0	1	
15	1	1	1	0	

☒ Circuit Diagram:-



Synchronous Counter:-

Sub : Day Time : Date : / /

How to Design Synchronous Counter:-

⇒ Step 1:- Decide the number of flip-flops & which one ?

⇒ Step 2:- Excitation table for the flip-flops.

⇒ Step 3:- Draw state diagram & circuit excitation Table

⇒ Step 4: Obtain simplified equations using "K" map.

⇒ Step 5:- Draw the Logic diagram.

2-bit synchronous up Counter:-

Step: 1:-

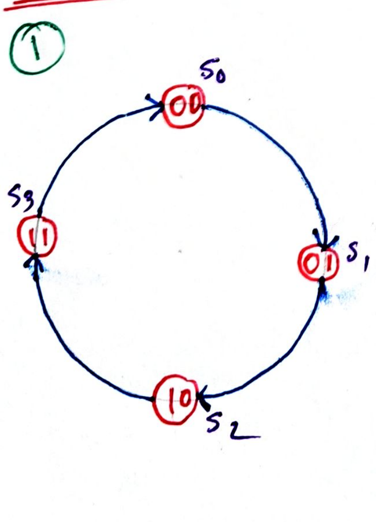
⇒ For 2bit we need two Flip Flop (JK F.F) →

Step: 2:-

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Step: 3:-

(i)



(ii) Ckt excitation Table:-

Q_1	Q_2	Q_1^*	Q_2^*	J_1	K_1	J_2	K_2
0	0	0	1	0	X	1	X
0	1	1	0	1	X	X	1
1	0	1	1	X	0	1	X
1	1	0	0	X	1	X	1

Step: 4:-

For J_1:-

$Q_1 \backslash Q_2$	0	1
0	0	1
1	X	X

$J_1 = Q_2$

For K_1:-

$Q_1 \backslash Q_2$	0	1
0	X	X
1	0	1

$K_1 = Q_2$

For J_2:-

$Q_1 \backslash Q_2$	0	1
0	1	X
1	1	X

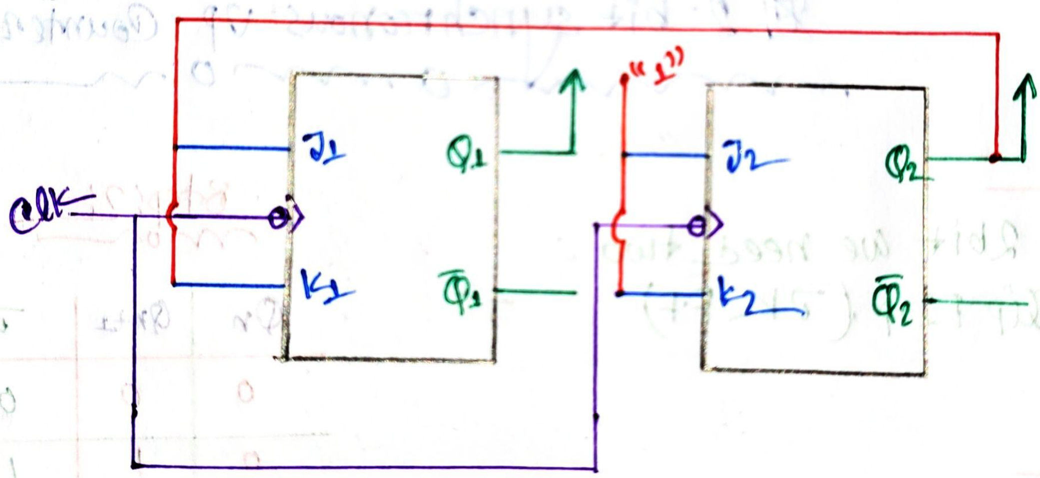
$J_2 = 1$

For K_2:-

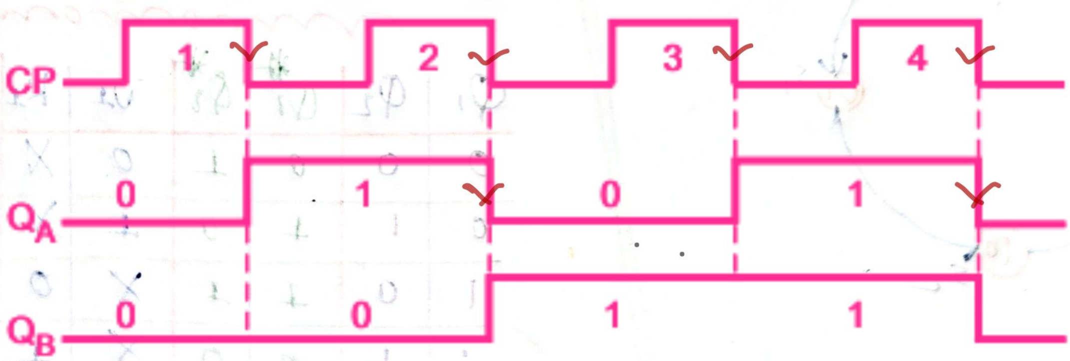
$Q_1 \backslash Q_2$	0	1
0	X	1
1	X	1

$K_2 = 1$

Step: 5:-



Alalyse the output wave:-



3-Bit Synchronous Up Counter using JK flip flop:-

⇒ Step 1:-

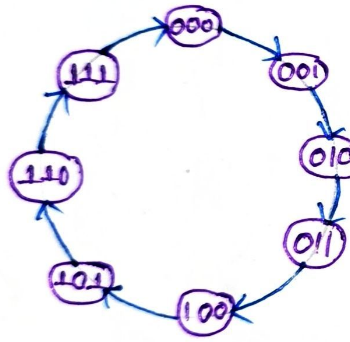
for 3 bit we need 3 JK flip flop

⇒ Step 2:-

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

⇒ Step: 3:-

(i) State diagram:-



(ii) ckt excitation table:-

Q_C	Q_B	Q_A	Q_C^*	Q_B^*	Q_A^*	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	1	1	1	X	0	X	0	1	X
1	1	1	0	0	0	X	1	X	1	X	1

⇒ Step: 4:-

K-map for J_C

$Q_C \backslash Q_BQ_A$	00	01	11	10
0	0	0	1	0
1	X	X	X	X

$\therefore J_C = Q_BQ_A$

K-map for K_C

$Q_C \backslash Q_BQ_A$	00	01	11	10
0	X	X	X	X
1	0	0	1	0

$\therefore K_C = Q_BQ_A$

K-map for J_B

$Q_C \backslash Q_BQ_A$	00	01	11	10
0	0	1	X	X
1	0	1	X	X

$\therefore J_B = Q_A$

K-map for K_B

$Q_C \backslash Q_BQ_A$	00	01	11	10
0	X	X	1	0
1	X	X	1	0

$\therefore K_B = Q_A$

∴ K-map for J_A

Q_C \ Q_BQ_A	00	01	11	10
0	1	X	X	1
1	1	X	X	1

∴ $J_A = 1$

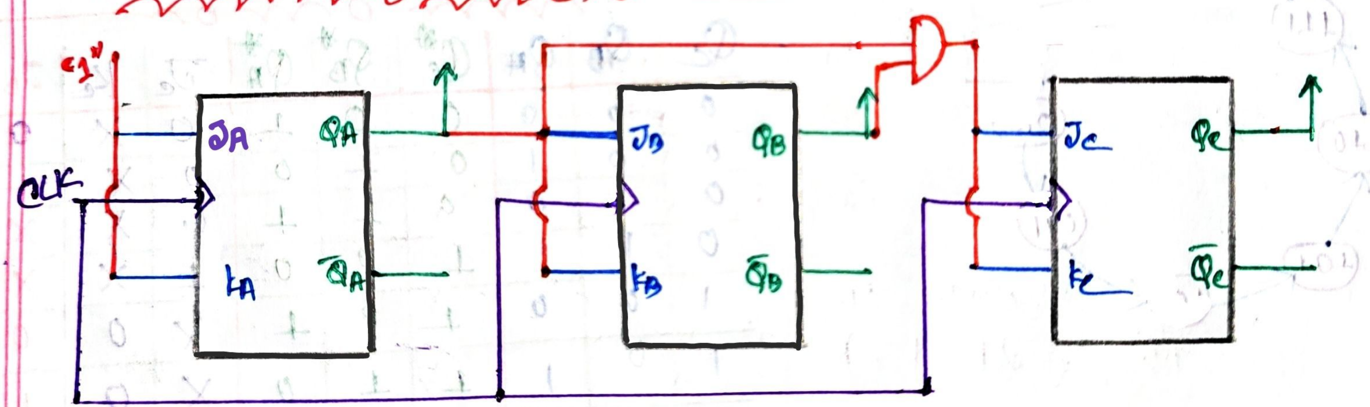
∴ K-map for K_A

Q_C \ Q_BQ_A	00	01	11	10
0	X	1	1	X
1	X	1	1	X

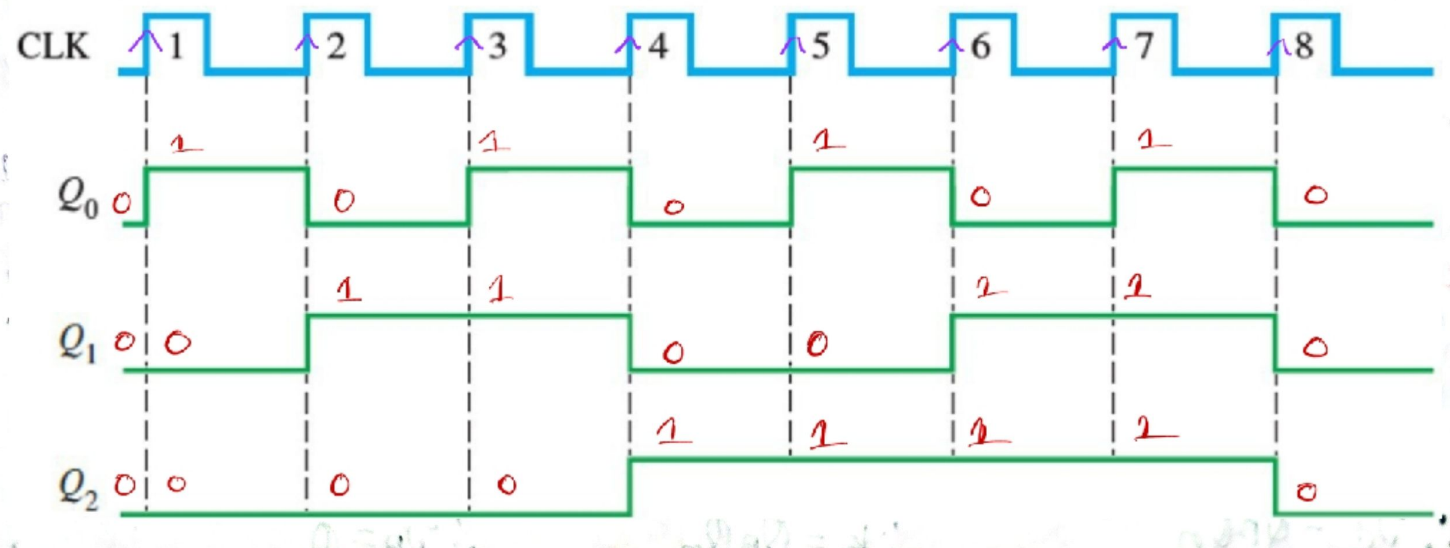
∴ $K_A = 1$

∴ Step: 5:–

⇒ Draw the logic circuit:–



Clock Diagram:–



4-Bit Synchronous Up Counter Using JK flip flop

Step 1:

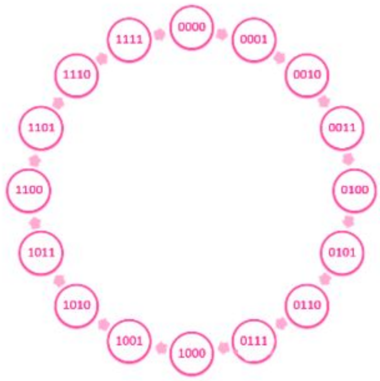
➔ For 4 bit we need 4 JK flip flop

Step 2:

➔ Draw the JK Excitation Table:

Qn	Qn+1	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Step 3.1:



Step 3.2:

CKT Excitation Table

Q_D	Q_C	Q_B	Q_A	Q_D^*	Q_C^*	Q_B^*	Q_A^*	J_D	K_D	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	0	0	0	1	0	X	0	X	0	X	1	X
0	0	0	1	0	0	1	0	0	X	0	X	1	X	X	1
0	0	1	0	0	0	1	1	0	X	0	X	X	0	1	X
0	0	1	1	0	1	0	0	0	X	1	X	X	1	X	1
0	1	0	0	0	1	0	1	0	X	X	0	0	X	1	X
0	1	0	1	0	1	1	0	0	X	X	0	1	X	X	1
0	1	1	0	0	1	1	1	0	X	X	0	X	0	1	X
0	1	1	1	1	0	0	0	1	X	X	1	X	1	X	1
1	0	0	0	1	0	0	1	X	0	0	X	0	X	1	X
1	0	0	1	1	0	1	0	X	0	0	X	1	X	X	1
1	0	1	0	1	0	1	1	X	0	0	X	X	0	1	X
1	0	1	1	1	1	0	0	X	0	1	X	X	1	X	1
1	1	0	0	1	1	0	1	X	0	X	0	0	X	1	X
1	1	0	1	1	1	1	0	X	0	X	0	1	X	X	1
1	1	1	0	1	1	1	1	X	0	X	0	X	0	1	X
1	1	1	1	0	0	0	0	X	1	X	1	X	1	X	1

Step 4:

➔K-Map for J_D:

$Q_DQ_C \backslash Q_BQ_A$	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	X	X	X	X
10	X	X	X	X

$\therefore J_D = Q_C Q_B Q_A$

➔K-Map for K_D:

$Q_DQ_C \backslash Q_BQ_A$	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	0	0	1	0
10	0	0	0	0

$\therefore K_D = Q_C Q_B Q_A$

➔K-Map for J_C:

$Q_DQ_C \backslash Q_BQ_A$	00	01	11	10
00	0	0	1	0
01	X	X	X	X
11	X	X	X	X
10	0	0	1	0

$\therefore J_C = Q_B Q_A$

➔K-Map for K_C:

$Q_DQ_C \backslash Q_BQ_A$	00	01	11	10
00	X	X	X	X
01	0	0	1	0
11	0	0	1	0
10	X	X	X	X

$\therefore K_C = Q_B Q_A$

➔K-Map for J_B:

$Q_DQ_C \backslash Q_BQ_A$	00	01	11	10
00	0	1	X	X
01	0	1	X	X
11	0	1	X	X
10	0	1	X	X

$\therefore J_B = Q_A$

➔K-Map for K_B:

$Q_DQ_C \backslash Q_BQ_A$	00	01	11	10
00	X	X	1	0
01	X	X	1	0
11	X	X	1	0
10	X	X	1	0

$\therefore K_B = Q_A$

➔K-Map for J_A:

$Q_DQ_C \backslash Q_BQ_A$	00	01	11	10
00	1	X	X	1
01	1	X	X	1
11	1	X	X	1
10	1	X	X	1

$\therefore J_A = 1$

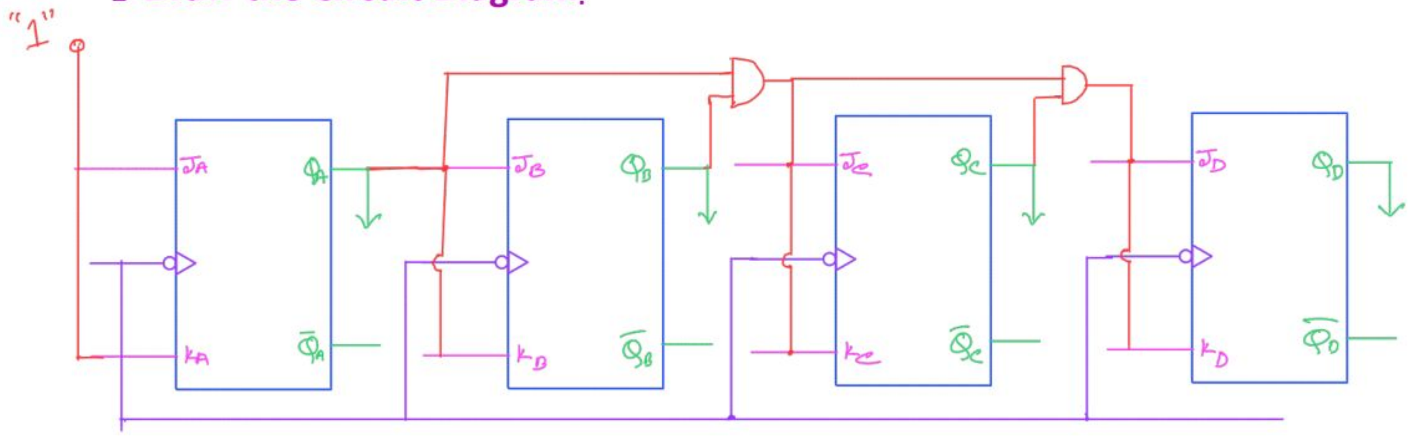
➔K-Map for K_A:

$Q_DQ_C \backslash Q_BQ_A$	00	01	11	10
00	X	1	1	X
01	X	1	1	X
11	X	1	1	X
10	X	1	1	X

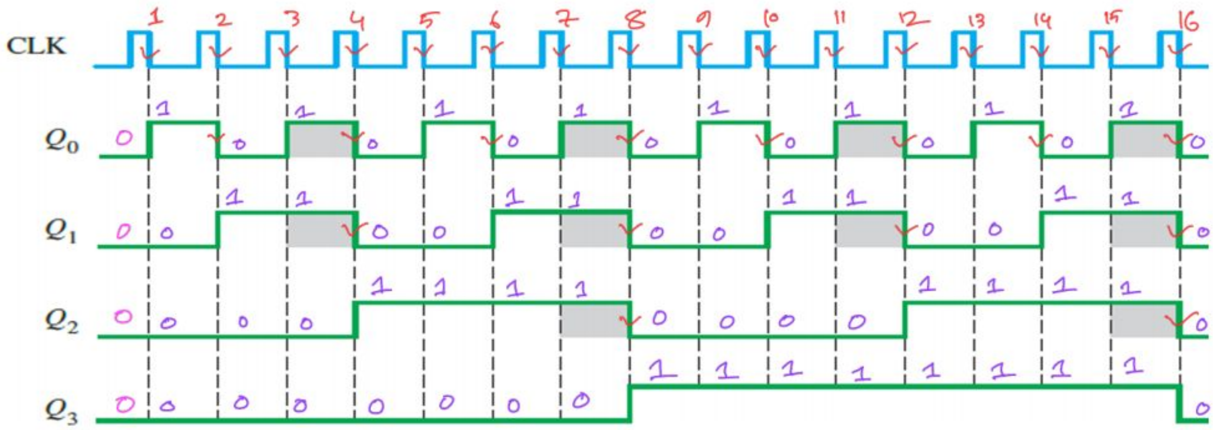
$\therefore K_A = 1$

Step 5:

➔Draw the Circuit Diagram:



Timing diagram of 4-Bit Synchronous Up Counter:



4-Bit Synchronous Decade BCD Counter Using JK flip flop

Step 1:

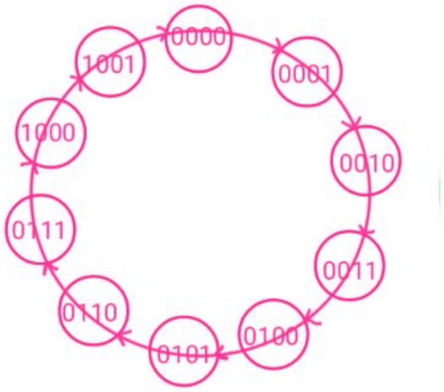
➔ For 4 bit we need 4 JK flip flop

Step 2:

➔ Draw the JK Excitation Table:

Qn	Qn+1	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Step 3.1:



Step 3.2:

CKT Excitation Table

Q_D	Q_C	Q_B	Q_A	Q_D^*	Q_C^*	Q_B^*	Q_A^*	J_D	K_D	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	0	0	0	1	0	X	0	X	0	X	1	X
0	0	0	1	0	0	1	0	0	X	0	X	1	X	X	1
0	0	1	0	0	0	1	1	0	X	0	X	X	0	1	X
0	0	1	1	0	1	0	0	0	X	1	X	X	1	X	1
0	1	0	0	0	1	0	1	0	X	X	0	0	X	1	X
0	1	0	1	0	1	1	0	0	X	X	0	1	X	X	1
0	1	1	0	0	1	1	1	0	X	X	0	X	0	1	X
0	1	1	1	1	0	0	0	1	X	X	1	X	1	X	1
1	0	0	0	1	0	0	1	X	0	0	X	0	X	1	X
1	0	0	1	0	0	0	0	X	1	0	X	0	X	X	1

Step 4:

➔K-Map for J_D:

$Q_DQ_C \backslash Q_BQ_A$	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	X	X	X	X
10	X	X	X	X

$\therefore J_D = Q_C Q_B Q_A$

➔K-Map for K_D:

$Q_DQ_C \backslash Q_BQ_A$	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	X	X	X	X
10	0	1	X	X

$\therefore K_D = Q_A$

➔K-Map for J_C:

$Q_DQ_C \backslash Q_BQ_A$	00	01	11	10
00	0	0	1	0
01	X	X	X	X
11	X	X	X	X
10	0	0	X	X

$\therefore J_C = Q_B Q_A$

➔K-Map for K_C:

$Q_DQ_C \backslash Q_BQ_A$	00	01	11	10
00	X	X	X	X
01	0	0	1	0
11	X	X	X	X
10	X	X	X	X

$\therefore K_C = Q_B Q_A$

➔K-Map for J_B:

$Q_DQ_C \backslash Q_BQ_A$	00	01	11	10
00	0	1	X	X
01	0	1	X	X
11	X	X	X	X
10	0	0	X	X

$\therefore J_B = \overline{Q_D} Q_A$

➔K-Map for K_B:

$Q_DQ_C \backslash Q_BQ_A$	00	01	11	10
00	X	X	1	0
01	X	X	1	0
11	X	X	X	X
10	X	X	X	X

$\therefore K_B = Q_A$

➔K-Map for J_A:

Q_DQ_C \ Q_BQ_A	00	01	11	10
00	1	X	X	1
01	1	X	X	1
11	X	X	X	X
10	1	X	X	X

$\therefore J_A = 1$

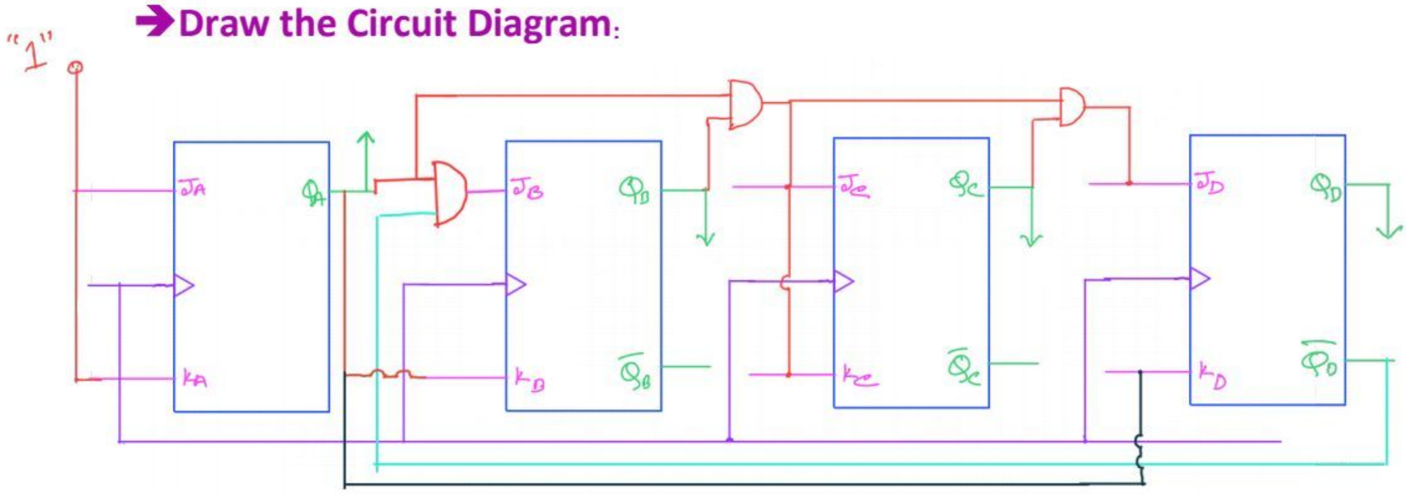
➔K-Map for K_A:

Q_DQ_C \ Q_BQ_A	00	01	11	10
00	X	1	1	X
01	X	1	1	X
11	X	X	X	X
10	X	1	X	X

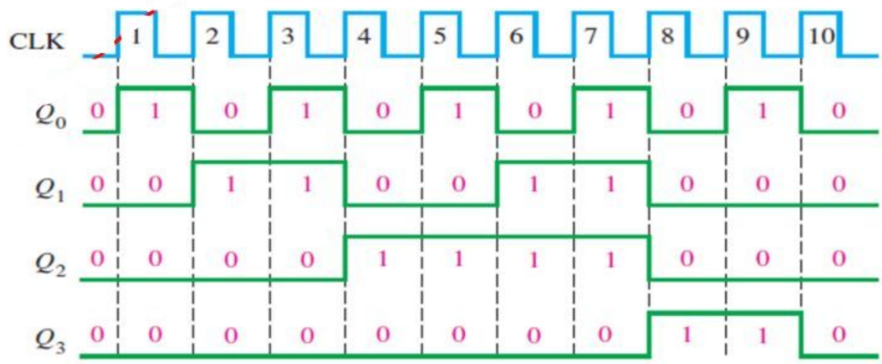
$\therefore K_A = 1$

Step 5:

➔Draw the Circuit Diagram:



Timing diagram of 4-Bit Synchronous Up Counter



Sub :

Time : Date : / /

UP/DOWN Counters: