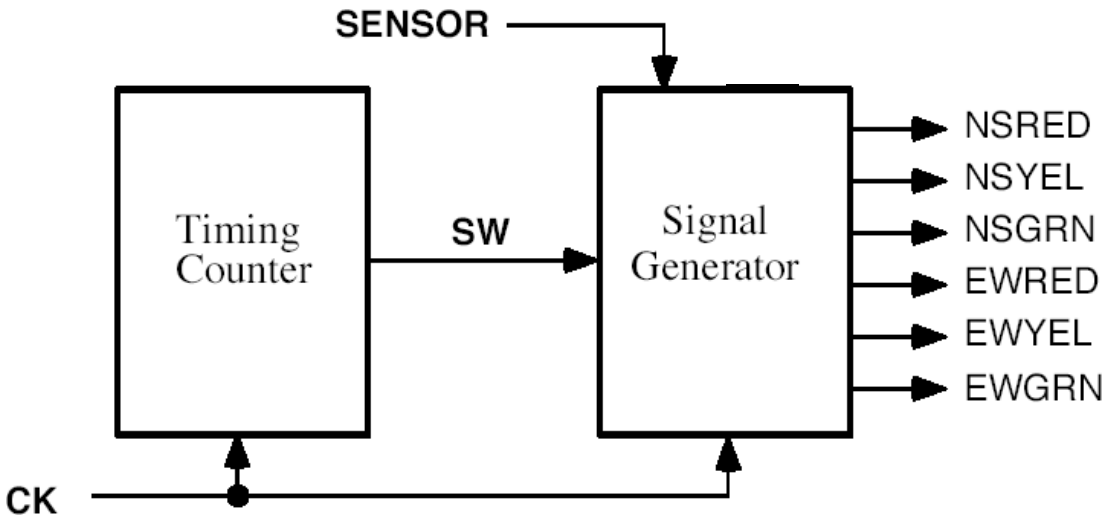
EECE 320 – Digital Systems Design

Project #2

Design and Simulation of a Simple Traffic Light Controller

Specifications

The controller consists of two sequential circuits, a timing counter and a signal generator. The counter is used to define a fundamental timing signal SW that drives the signal generator. The signal generator generates the signals that control the traffic lights. The controller has the following block diagram:



The input and internal signals have the following functions:

CK:	A clock with a one second cycle time (i.e., period = 1 second)
SENSOR:	Indicates that a car is waiting at a red light in the **East-West** direction.
SW:	An internal timing signal used to switch the state of the lights as explained below.

The following six output signals control the individual traffic lights:

NSRED	The red light for the north-south lane.
NSYEL	The yellow light for the north-south lane
NSGRN	The green light for the north-south lane
EWRED	The red light for the east-west lane.
EWYEL	The yellow light for the east-west lane
EWGRN	The green light for the east-west lane

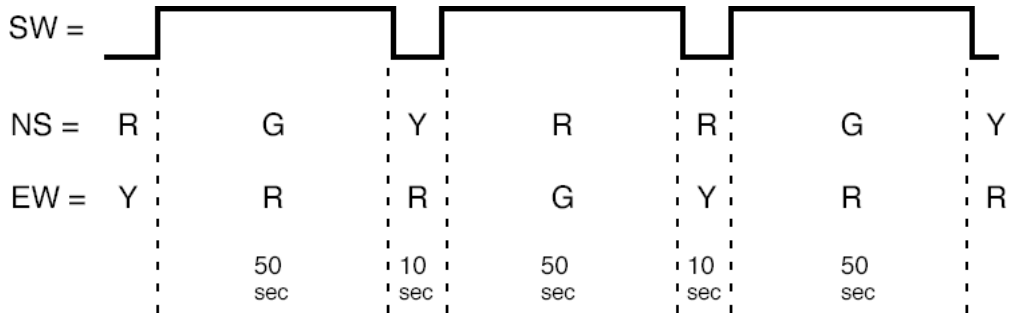
Mode of Operation:

The lights are to switch between north-south and east-west in the normal Green-Yellow-Red sequence

with the green light on for 50 seconds, the yellow light on for 10 seconds, and the red light on for 60 seconds, as long as there are cars in the east-west direction. If there are no cars in the east-west direction, then the north-south direction is favored by keeping its green light on until a car arrives in the east-west direction. The controller determines the presence of a car on the east-west lane by the input SENSOR, which is asserted whenever a car is detected as waiting at the light.

Timing Signals:

The signal SW is used to define the timing of the normal Green-Yellow-Red sequence. It should have the following waveform:



Implementation:

- Do not use SW as a clock for any of the flip-flops in the signal generator. All the flip-flops in the project must have their clock inputs connected directly to the clock signal CK.

- If you were to actually build this circuit you would need a clock with a one second period to drive both the signal generator and the timing counter. In simulating the project, however, do not worry about the rate of the clock, since the functionality of the circuits is independent of the clock rate. You may use any clock rate for testing, as long as it takes 120 clock cycles to go through a full Green-Yellow-Red sequence.

- The timing counter should be implemented using one or more counters. The signal generator should be designed as a simple sequential circuit based on regular FSM design.

- You may assume that once a car arrives at the light it will wait there until its light turns green. That is, the car will not back up and leave the intersection or run a red light.

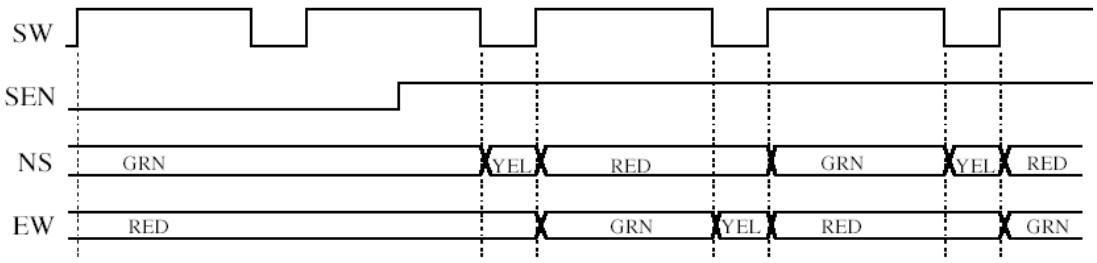
- You may also assume that the SENSOR signal is synchronized with CK so there will be no problem with meta-stability. However, it can change value on any rising clock edge. Your design must deal with the possibility that the SENSOR signal may change in the middle of any of the periods identified by the timing diagram above. You must design the state diagram of the Signal Generator so that none of the Red, Green, or Yellow periods are shortened by the SENSOR changing in the middle of one of these periods.

- When there has been no cars in the east west direction for long enough to cause the controller to be stalled with north/south green and east/west red, and then a car arrives, the controller should go through a full yellow period for the north/south direction. Pay special attention to the case where the car arrives while SW is 0, as this can give rise to a shortened yellow period if you are not careful.

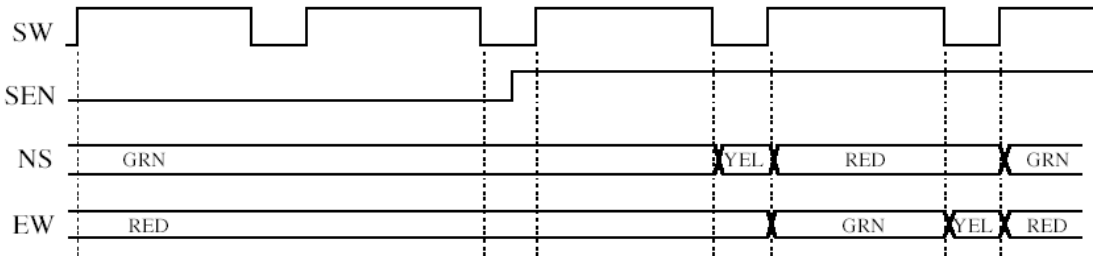
- The following timing diagrams are intended to clarify these requirements by giving a precise statement of how the circuit should behave when the sensor input SEN changes value. In order to verify that your circuit meets this requirement you should observe the behavior in these timing diagrams when you apply the indicated waveforms on the SW and SEN inputs.

- Test your design with these two tests using the simulator and include in your outputs two fields as shown below (NS and EW) representing the colors of the lights in each ***state***.

Test 1



Test 2



Deliverables

- You should submit the Verilog files (*.sv) for all the modules of the circuit and the testbench of the complete circuit on Moodle. Do not submit testbenches for individual modules. Additionally, include a PDF file containing the code for all modules, including the testbench, and screenshots of the EPwave viewer showing the results of the different test cases.