

1. Description

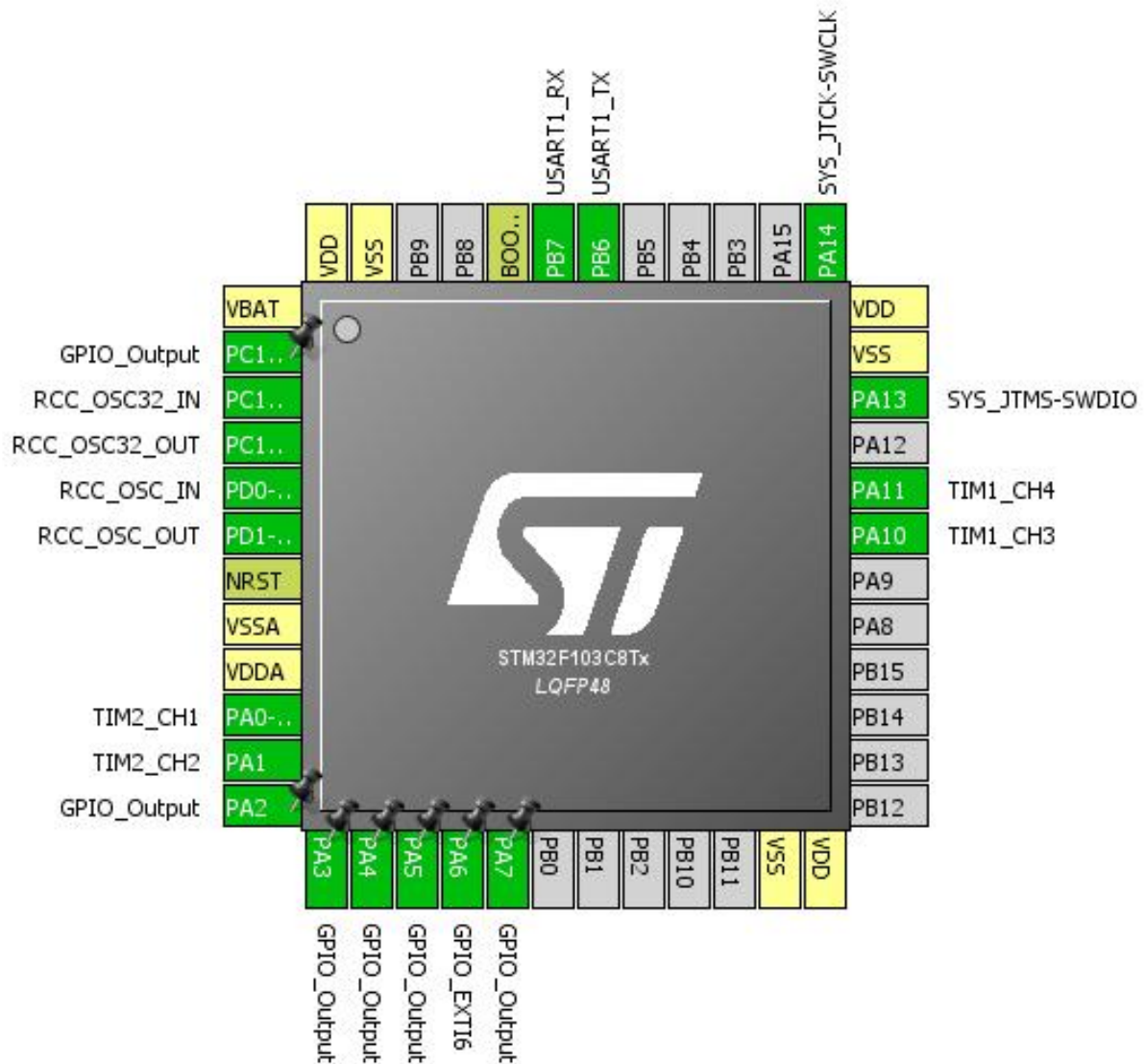
1.1. Project

Project Name	STM32F103C8T6_AlphaCarControl
Board Name	STM32F103C8T6_AlphaCarControl
Generated with:	STM32CubeMX 4.20.1
Date	11/21/2019

1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F103
MCU name	STM32F103C8Tx
MCU Package	LQFP48
MCU Pin number	48

2. Pinout Configuration

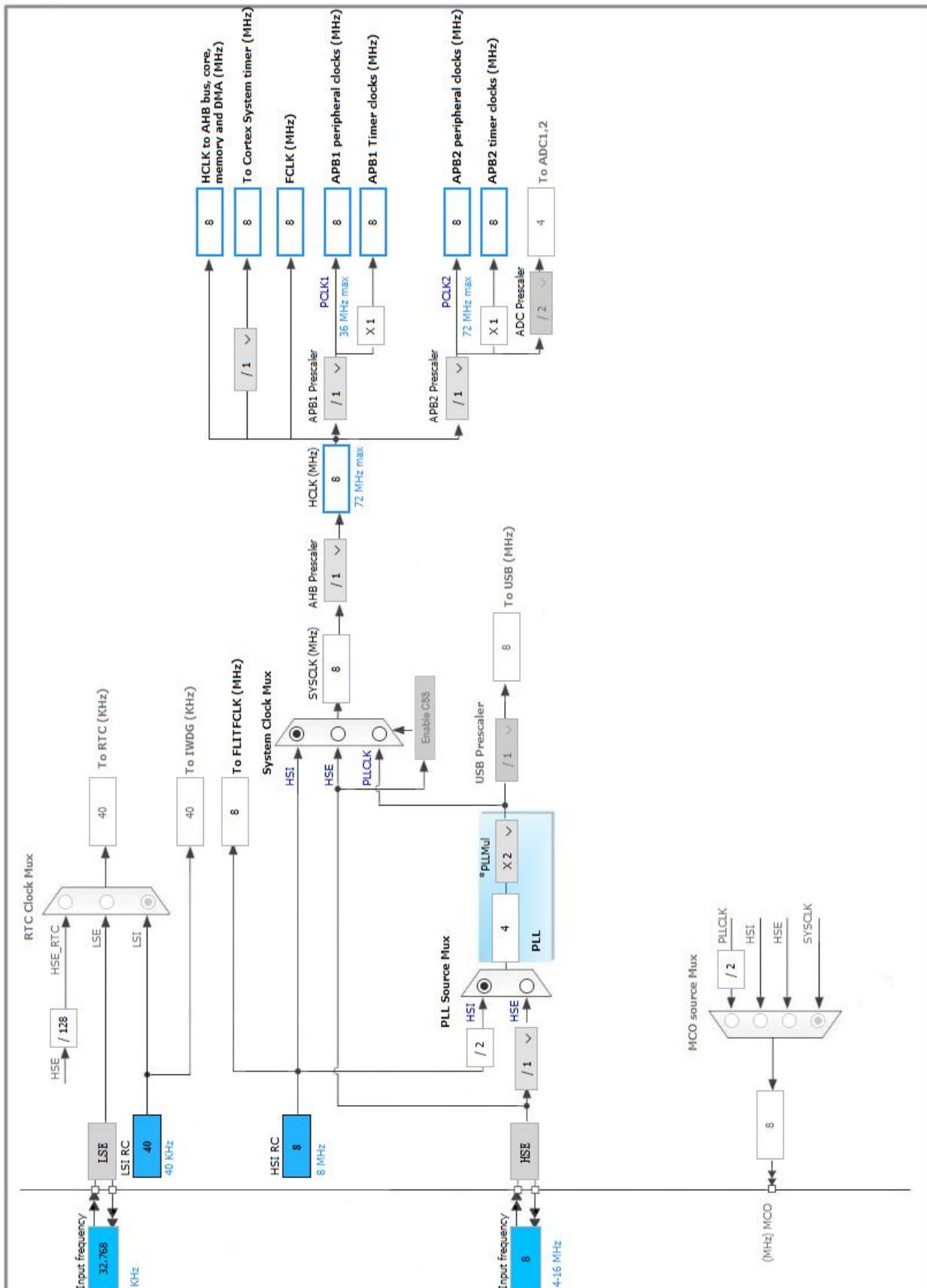


3. Pins Configuration

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13-TAMPER-RTC *	I/O	GPIO_Output	
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
5	PD0-OSC_IN	I/O	RCC_OSC_IN	
6	PD1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	VSSA	Power		
9	VDDA	Power		
10	PA0-WKUP	I/O	TIM2_CH1	
11	PA1	I/O	TIM2_CH2	
12	PA2 *	I/O	GPIO_Output	
13	PA3 *	I/O	GPIO_Output	
14	PA4 *	I/O	GPIO_Output	
15	PA5 *	I/O	GPIO_Output	
16	PA6	I/O	GPIO_EXTI6	
17	PA7 *	I/O	GPIO_Output	
23	VSS	Power		
24	VDD	Power		
31	PA10	I/O	TIM1_CH3	
32	PA11	I/O	TIM1_CH4	
34	PA13	I/O	SYS_JTMS-SWDIO	
35	VSS	Power		
36	VDD	Power		
37	PA14	I/O	SYS_JTCK-SWCLK	
42	PB6	I/O	USART1_TX	
43	PB7	I/O	USART1_RX	
44	BOOT0	Boot		
47	VSS	Power		
48	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

5.1.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	0 WS (1 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

5.2. SYS

Debug: Serial Wire

Timebase Source: SysTick

5.3. TIM1

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

5.3.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	800 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	999 *
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves)
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Trigger Event Selection Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State Disable
BRK Polarity High

Break And Dead Time management - Output Configuration:

Automatic Output State Disable
Off State Selection for Run Mode (OSSR) Disable
Off State Selection for Idle Mode (OSSI) Disable
Lock Configuration Off

PWM Generation Channel 3:

Mode PWM mode 1
Pulse (16 bits value) **999 ***
Fast Mode Disable
CH Polarity High
CH Idle State Reset

PWM Generation Channel 4:

Mode PWM mode 1
Pulse (16 bits value) **999 ***
Fast Mode Disable
CH Polarity High
CH Idle State Reset

5.4. TIM2

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

5.4.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) **88 ***
Counter Mode Up
Counter Period (AutoReload Register - 16 bits value) **1799 ***
Internal Clock Division (CKD) No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode Disable (no sync between this TIM (Master) and its Slaves)
Trigger Event Selection Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode PWM mode 1

Pulse (16 bits value)	45 *
Fast Mode	Disable
CH Polarity	High
PWM Generation Channel 2:	
Mode	PWM mode 1
Pulse (16 bits value)	123 *
Fast Mode	Disable
CH Polarity	High

5.5. TIM3

mode: Clock Source

5.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	799 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	9999 *
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.6. TIM4

mode: Clock Source

5.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	160 *
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.7. USART1

Mode: Asynchronous

5.7.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

* User modified value

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PD0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PD1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PA10	TIM1_CH3	Alternate Function Push Pull	n/a	Low	
	PA11	TIM1_CH4	Alternate Function Push Pull	n/a	Low	
TIM2	PA0-WKUP	TIM2_CH1	Alternate Function Push Pull	n/a	Low	
	PA1	TIM2_CH2	Alternate Function Push Pull	n/a	Low	
USART1	PB6	USART1_TX	Alternate Function Push Pull	n/a	High *	
	PB7	USART1_RX	Input mode	No pull-up and no pull-down	n/a	
GPIO	PC13-TAMPER-RTC	GPIO_Output	Output Push Pull	n/a	Low	
	PA2	GPIO_Output	Output Push Pull	n/a	Low	
	PA3	GPIO_Output	Output Push Pull	n/a	Low	
	PA4	GPIO_Output	Output Push Pull	n/a	Low	
	PA5	GPIO_Output	Output Push Pull	n/a	Low	
	PA6	GPIO_EXTI6	External Interrupt Mode with Rising/Falling edge	No pull-up and no pull-down	n/a	
	PA7	GPIO_Output	Output Push Pull	n/a	Low	

6.2. DMA configuration

DMA request	Stream	Direction	Priority
USART1_RX	DMA1_Channel5	Peripheral To Memory	Low

USART1_RX: DMA1_Channel5 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Byte
Memory Data Width: Byte

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel5 global interrupt	true	0	0
TIM3 global interrupt	true	0	0
TIM4 global interrupt	true	0	0
USART1 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
EXTI line[9:5] interrupts	unused		
TIM1 break interrupt	unused		
TIM1 update interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		

* User modified value

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F1
Line	STM32F103
MCU	STM32F103C8Tx
Datasheet	13587_Rev17

7.2. Parameter Selection

Temperature	25
Vdd	3.3

8. Software Project

8.1. Project Settings

Name	Value
Project Name	STM32F103C8T6_AlphaCarControl
Project Folder	D:\wifi\CarControlCode\STM32F103C8T6_AlphaCarControl
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F1 V1.4.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No