Design I/O circuits for a 2RW 8T SRAM array

Group Number: 13

Group Members :
Mintu Kumar(2022296)
Aman Kumar(2022060)
Dhruv Sharma(2022371)
Noorain Ansari(2022339)

INDRAPRASTHA INSTITUTE *of*
INFORMATION TECHNOLOGY
DELHI

Problem Statement

Design I/O circuits for an **8T 2RW SRAM Array** with **512 rows**, each contributing **0.5 fF parasitic capacitance** per row.

Design Goals:

- **Precharge Circuit**: Charge bitlines to full **VDD** within **250 ps** under worst-case PVT (SS, 1.08 V, 125°C).
- **Write Driver**: Discharge BL or BLB within **100 ps** under the same PVT conditions.
- **16:1 Multiplexer**: Efficiently select 1 out of 16 words per row with **minimal delay**, **low parasitics**, **reduced area**, and **limited stack effect**.

Challenges

1. Precharge Circuit:

- Ensuring both bitlines are fully charged to VDD and maintain equal voltage levels to prevent read delays.
- Determining optimal PMOS sizing to meet the 250 ps timing requirement under worst-case PVT conditions (SS, 1.08 V, 125°C) without excessive area increase.

2. Write Driver:

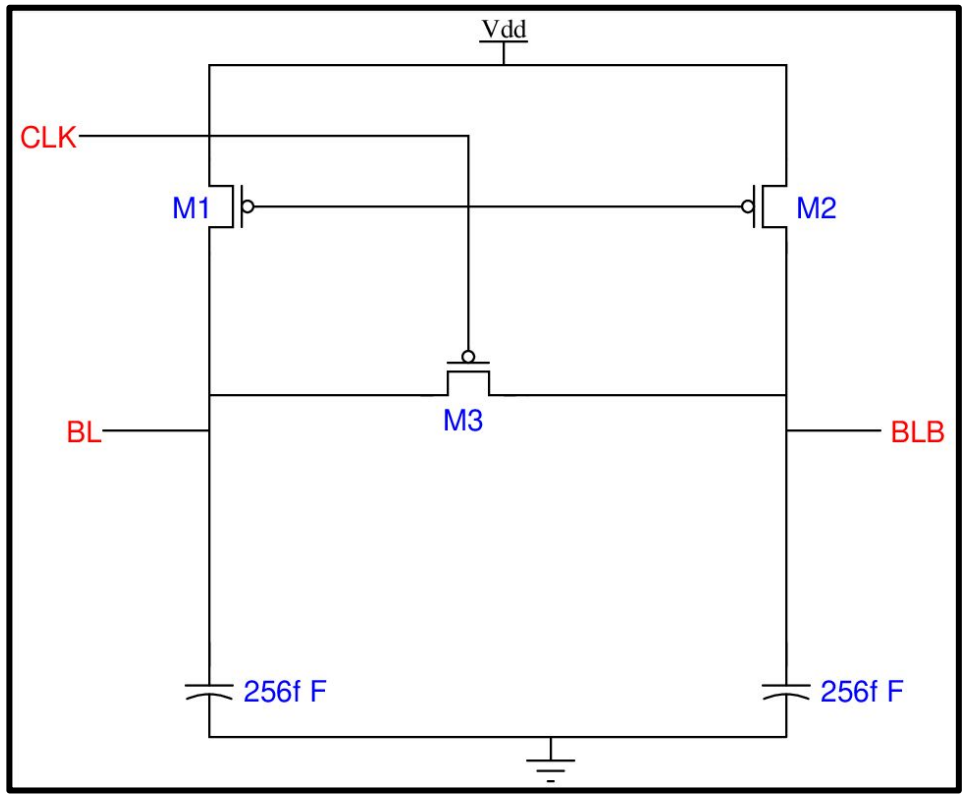
- Achieving bitline discharge within 100 ps proved challenging; increasing NMOS size met timing but led to area concerns.
- Implemented fingering technique by dividing transistors into multiple fingers to balance drive strength and area.
- Utilized cross-coupled PMOS transistors to assist in charging the complementary bitline, ensuring proper write functionality.

3. 16:1 Multiplexer:

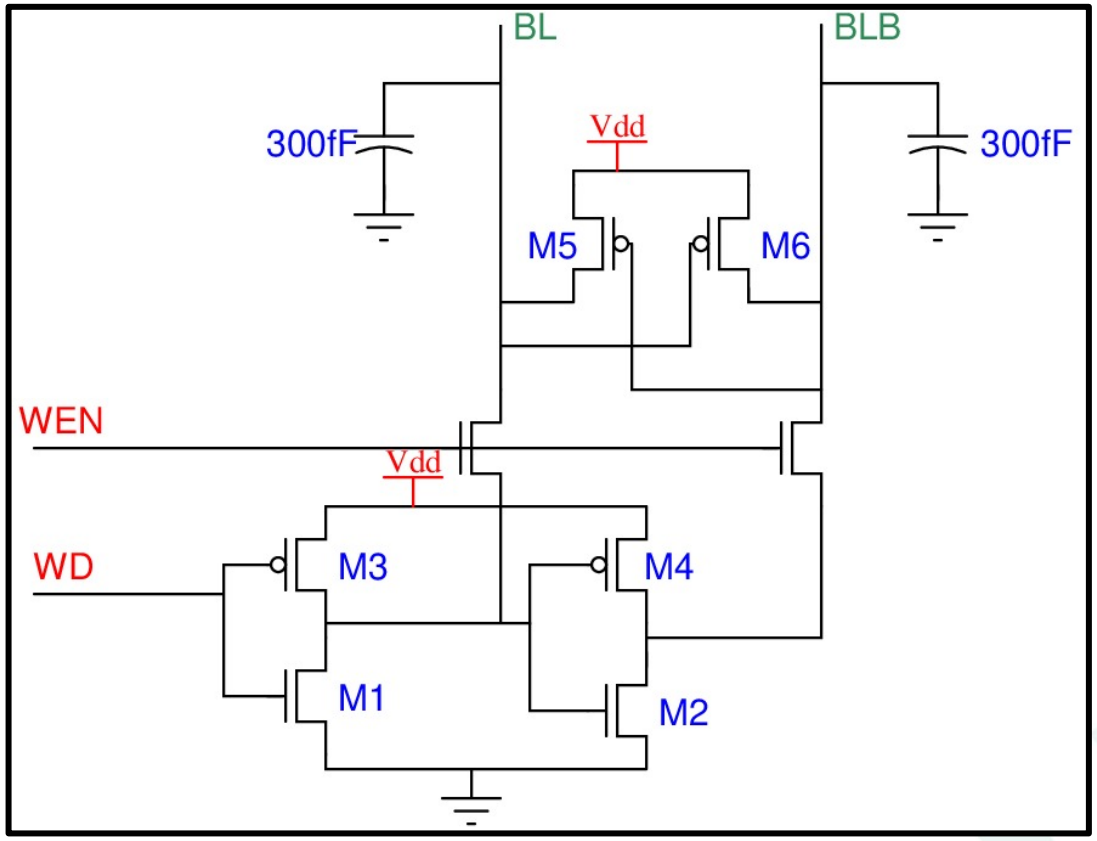
- Designing a multiplexer with minimal parasitic capacitance, reduced stack effect, compact area, and low delay was complex.
- Adopted a two-stage approach: first stage as a 4:1 tree-structured multiplexer to reduce area, followed by a conventional multiplexer for efficient signal transfer.

Schematic + Sizing

Precharge Circuit



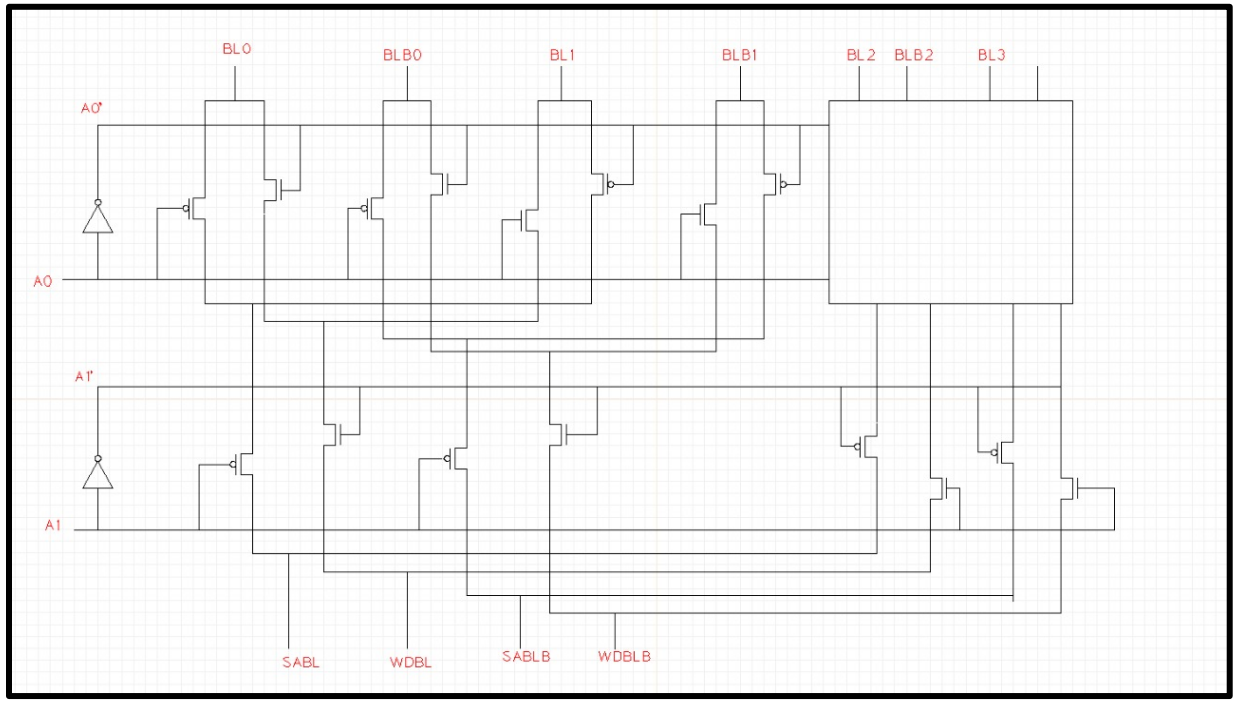
Write Driver Circuits



Precharge Sizing: PMOS – 6.2 µm
Write Driver Sizing: Inverter **PMOS/NMOS** – 12 µm / 8 µm; Output **NMOS** – 15 µm, **PMOS** – 8 µm

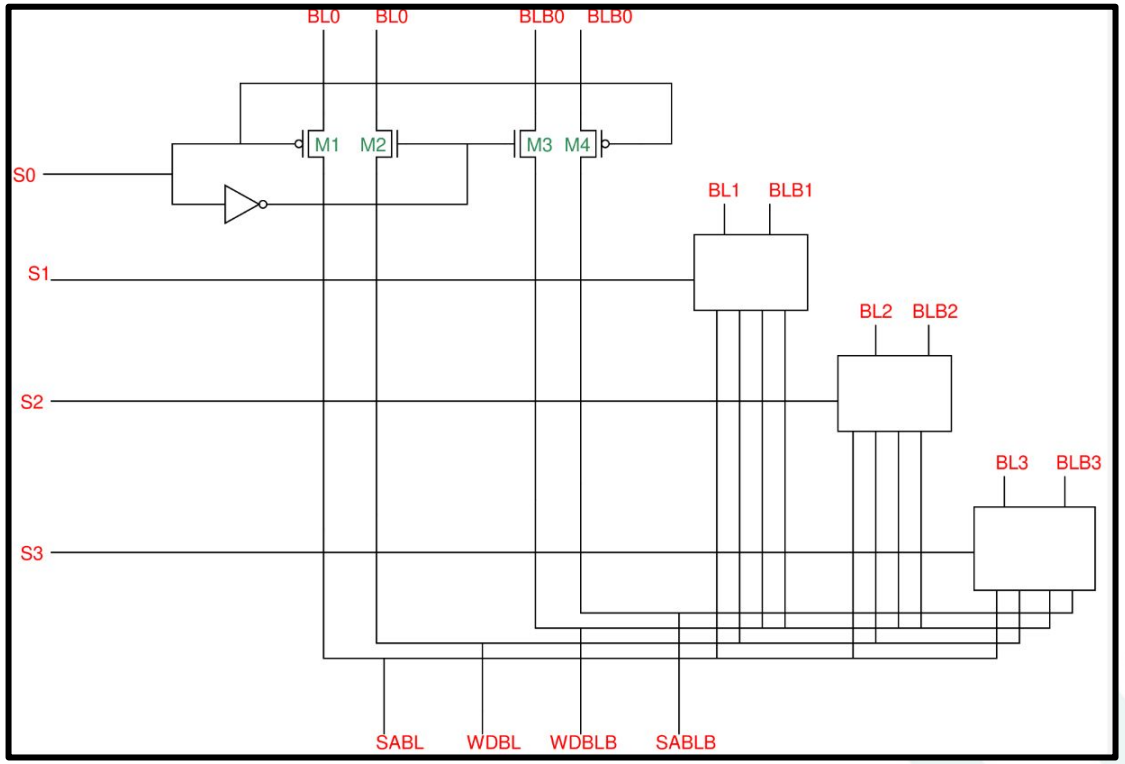
Schematic + Sizing

Mux 4:1 (Stage-1)



WDBLB

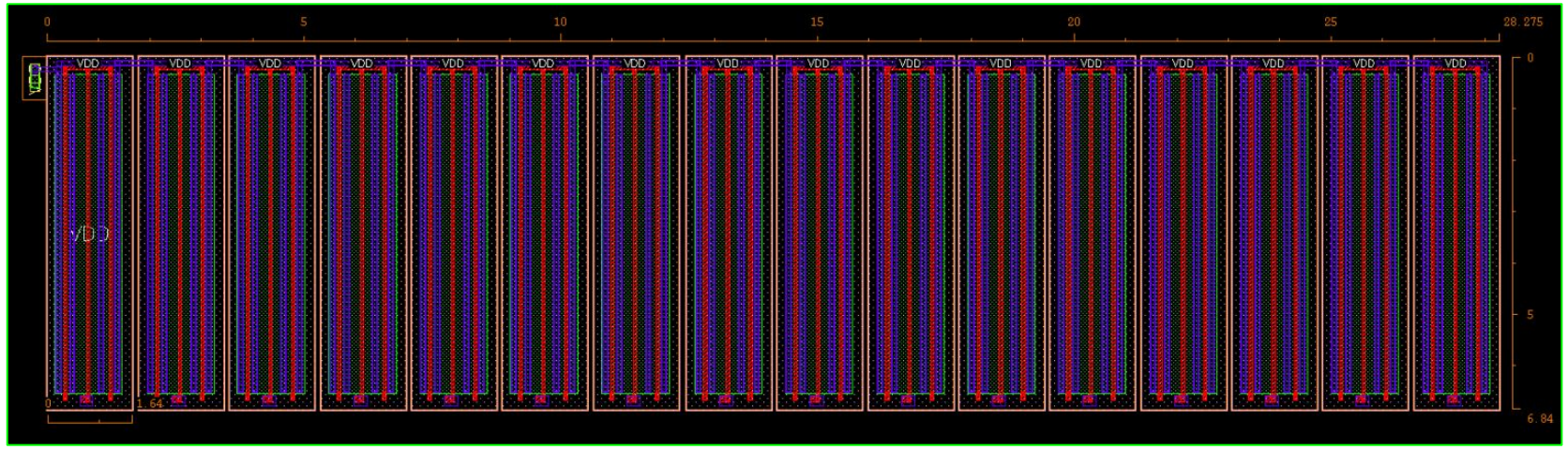
Mux 4:1 (Stage-2)

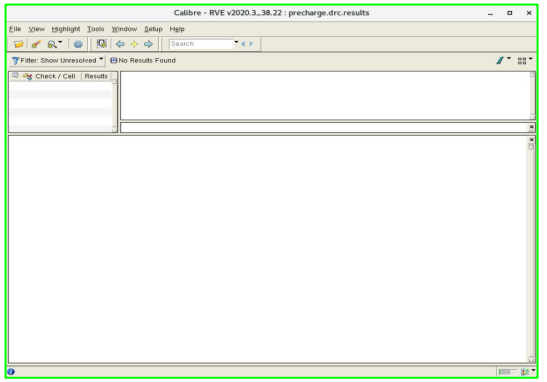


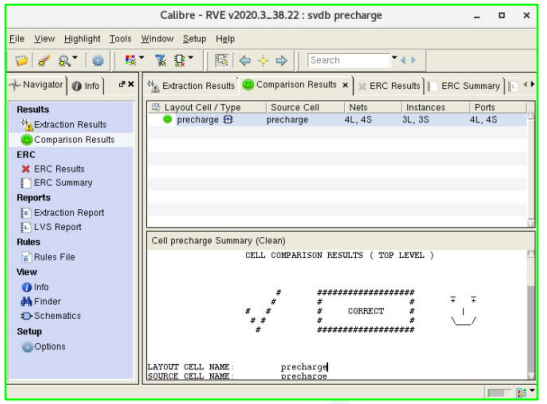
Mux Stage 1 Sizing: PMOS/NMOS – 3 µm; Inverter **PMOS/NMOS** – 1.4 µm / 0.7 µm
Mux Stage 2 Sizing: Inverter **PMOS/NMOS** – 1.4 µm / 0.7 µm; **PMOS/NMOS** – 5 µm / 5 µm

Layout Finalization, LVS Clean & DRC Clean

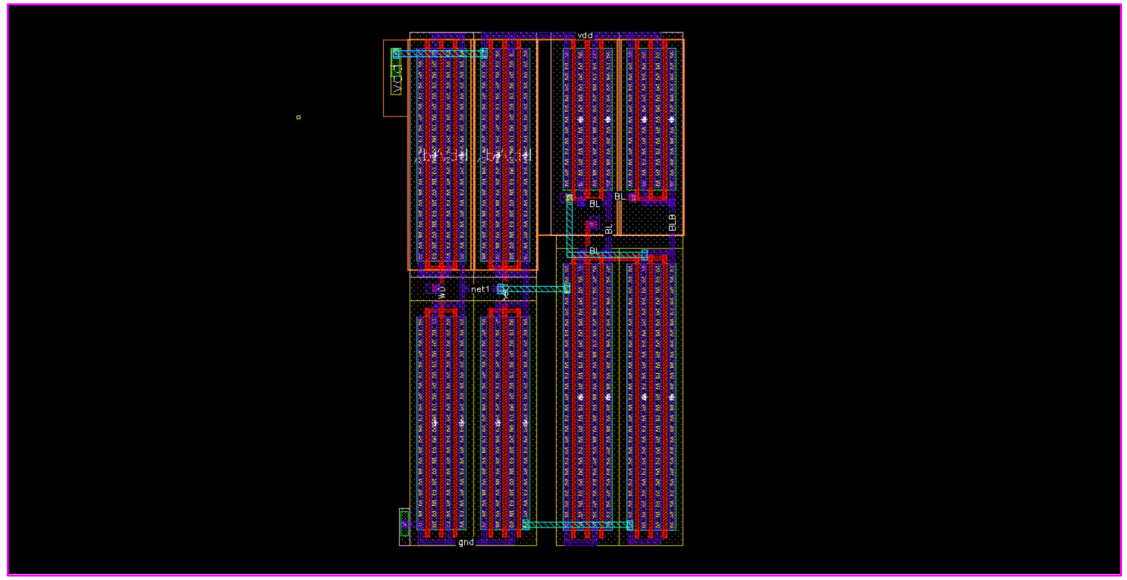
Pre-Charge Circuit

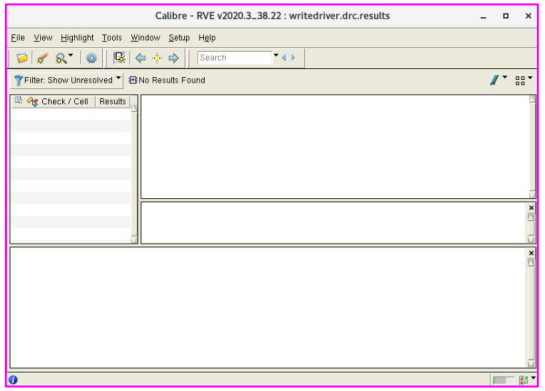


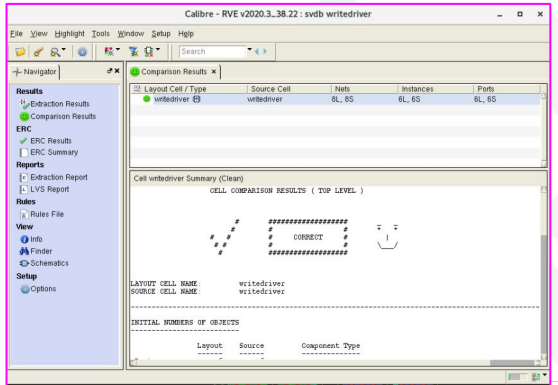




Write Driver

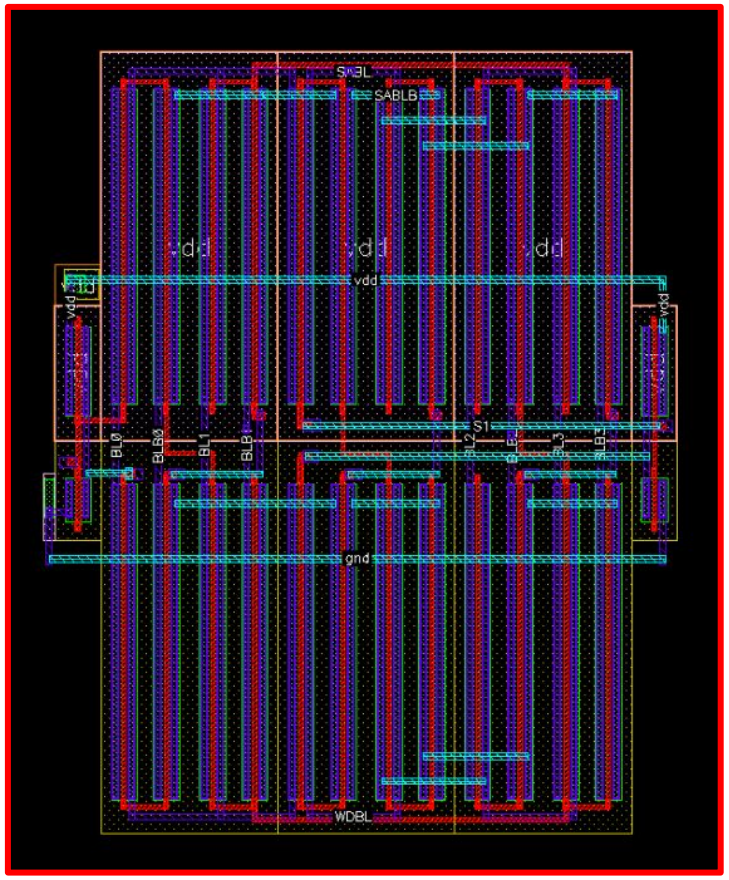


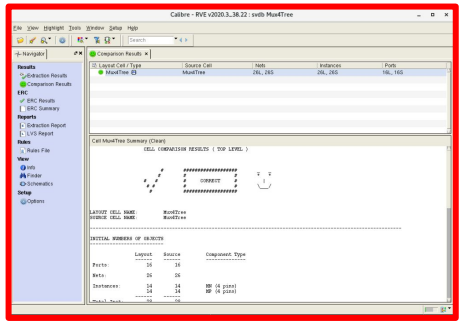


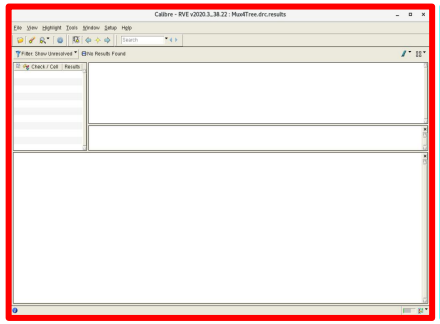


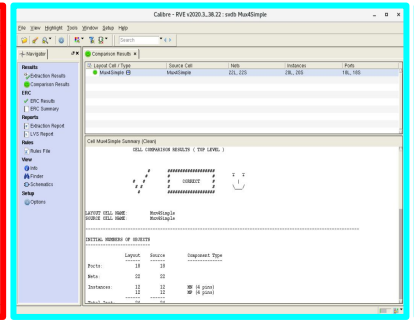
Layout Finalization, LVS Clean & DRC Clean

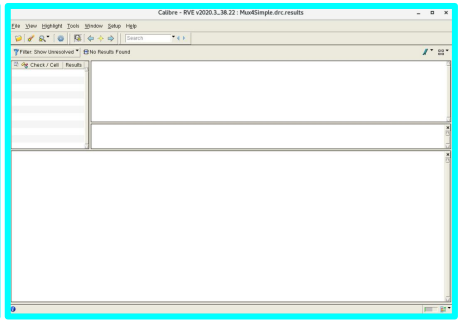
Mux Stage-1



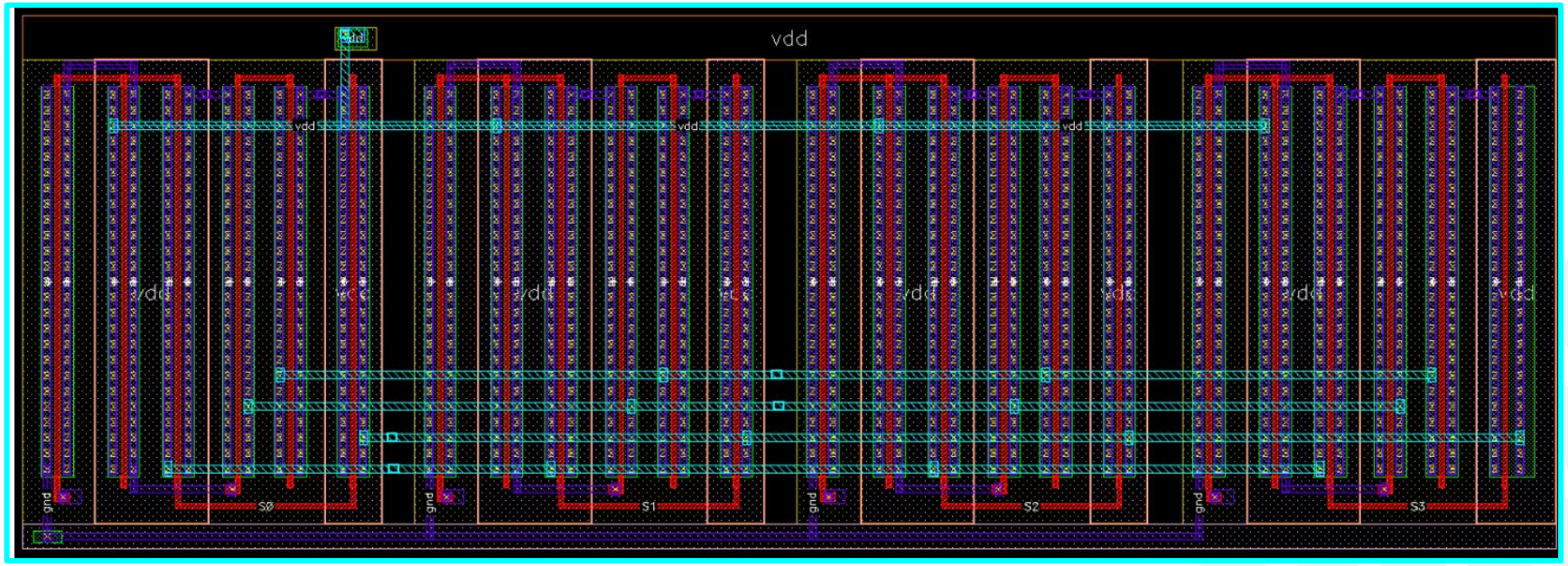








Mux Stage-2



Verification Plan (& Justification)

1. Precharge Circuit:

- **Setup:** Both BL and BLB were initially discharged to 0 V.
- **Simulation:** Transient analysis conducted over 100 ns.
- **Observation:** Both bitlines successfully charged to VDD, confirming correct precharge functionality.

2. Write Driver:

- **Setup:** BL and BLB precharged to VDD.
- **Simulation:** Transient analysis over 40 ns with a 0–1.08 V data pulse (20 ns duration, 50% duty cycle) and a 10 ns write enable (WE) pulse.
- **Observation:** BL or BLB discharged appropriately based on data input and WE signal, validating write operation.

Verification Plan (& Justification)

3. 16:1 Multiplexer:

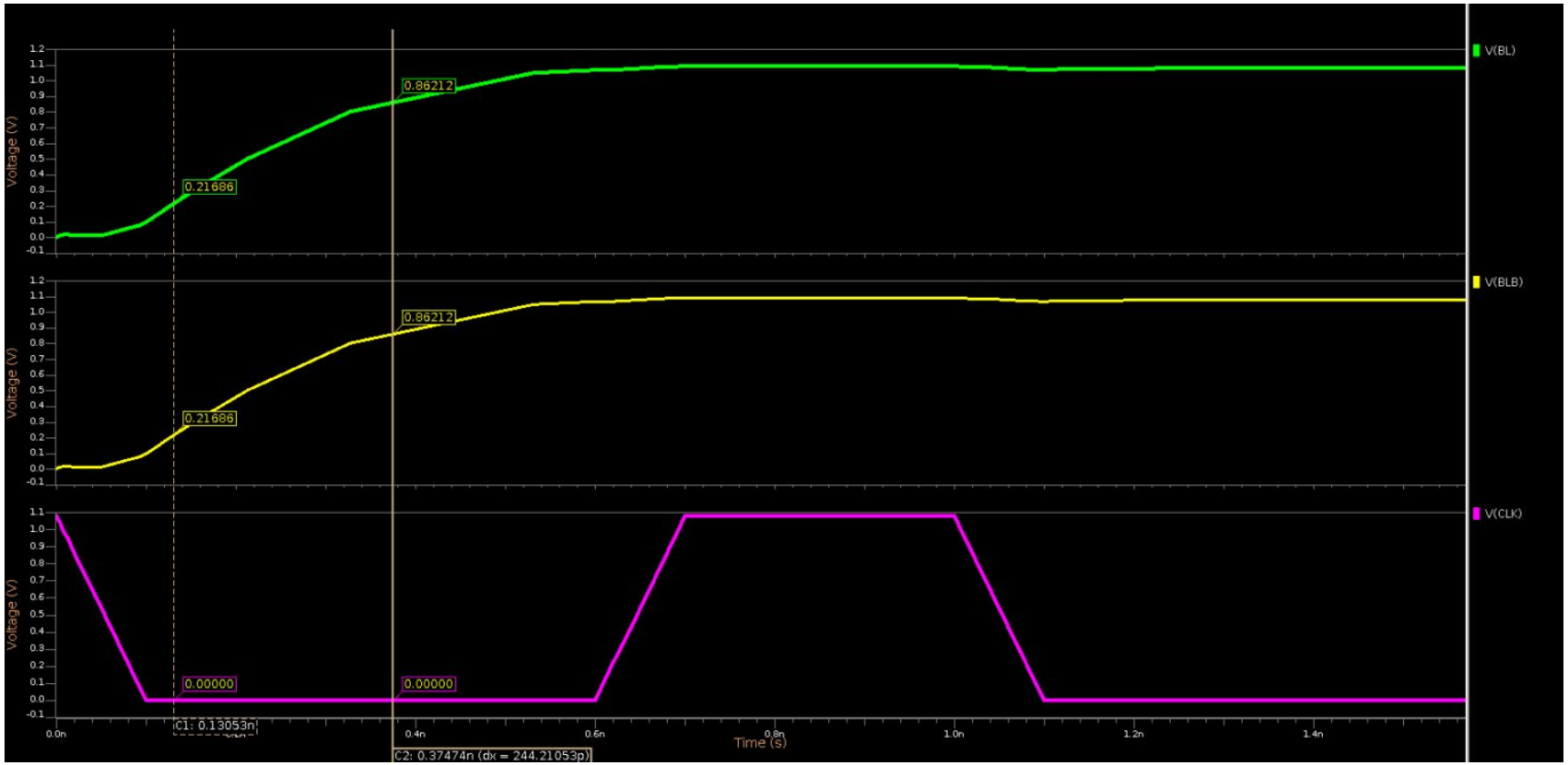
- **Setup:** BL0 configured with '00', BL1/BLB1 with '01', etc.
- **Simulation:** Address lines A0 and A1 pulsed to select different inputs.
- **Observation:** Correct voltage levels observed at SABL and SABLB outputs corresponding to selected inputs. Noted slight voltage drop on WDBL and WDBLB due to NMOS threshold voltage, which is typical in such configurations.

Justification:

- Simulation waveforms confirm that each component meets the specified timing and functional requirements under worst-case PVT conditions (SS, 1.08 V, 125°C). Design optimizations, such as transistor sizing and fingering techniques, effectively balance performance with area constraints.

Results

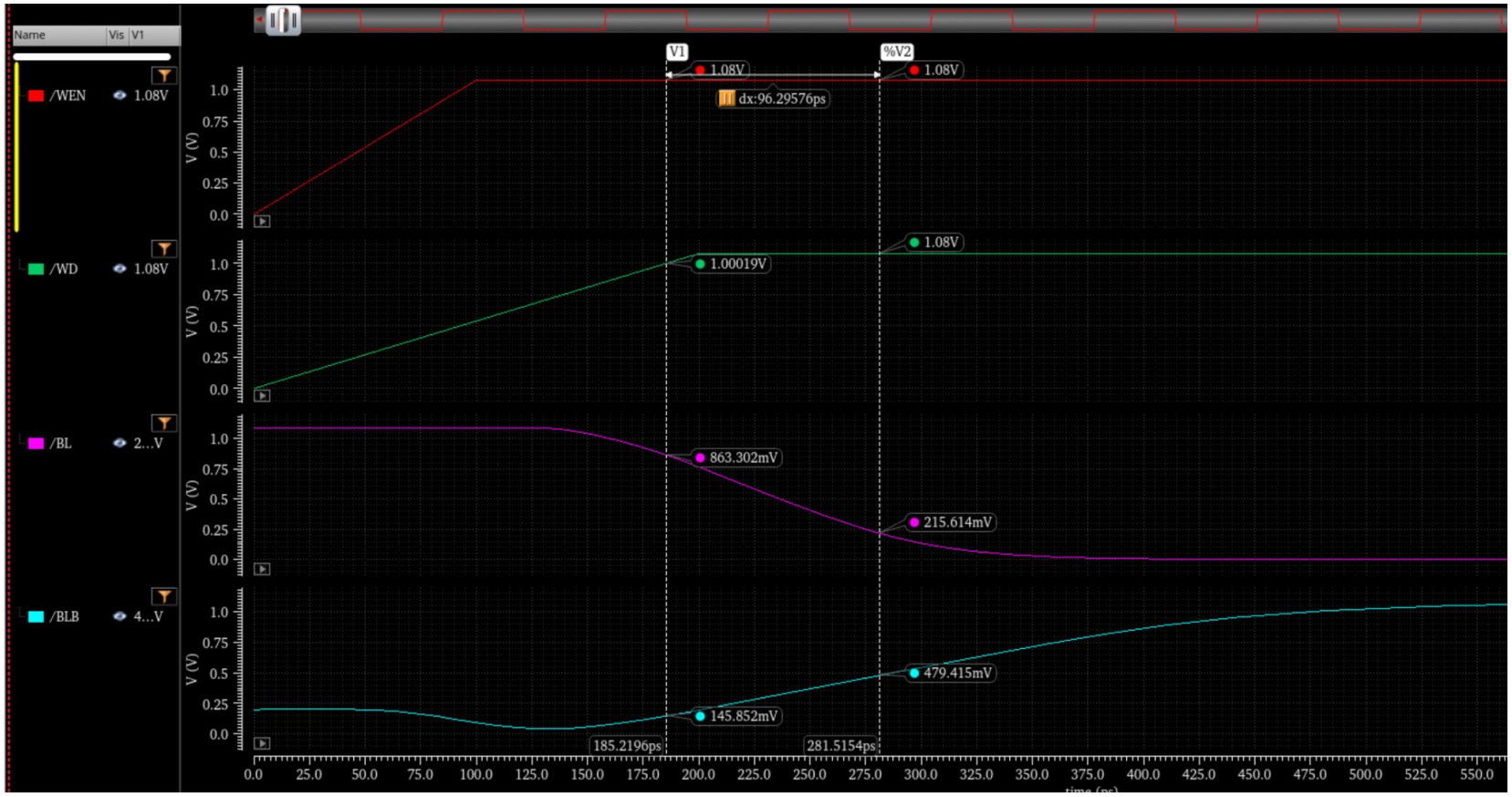
Precharge Charging Time Simulation



Precharge time for BL and BLB: 244 ps at SS, 1.08 V, 125 °C

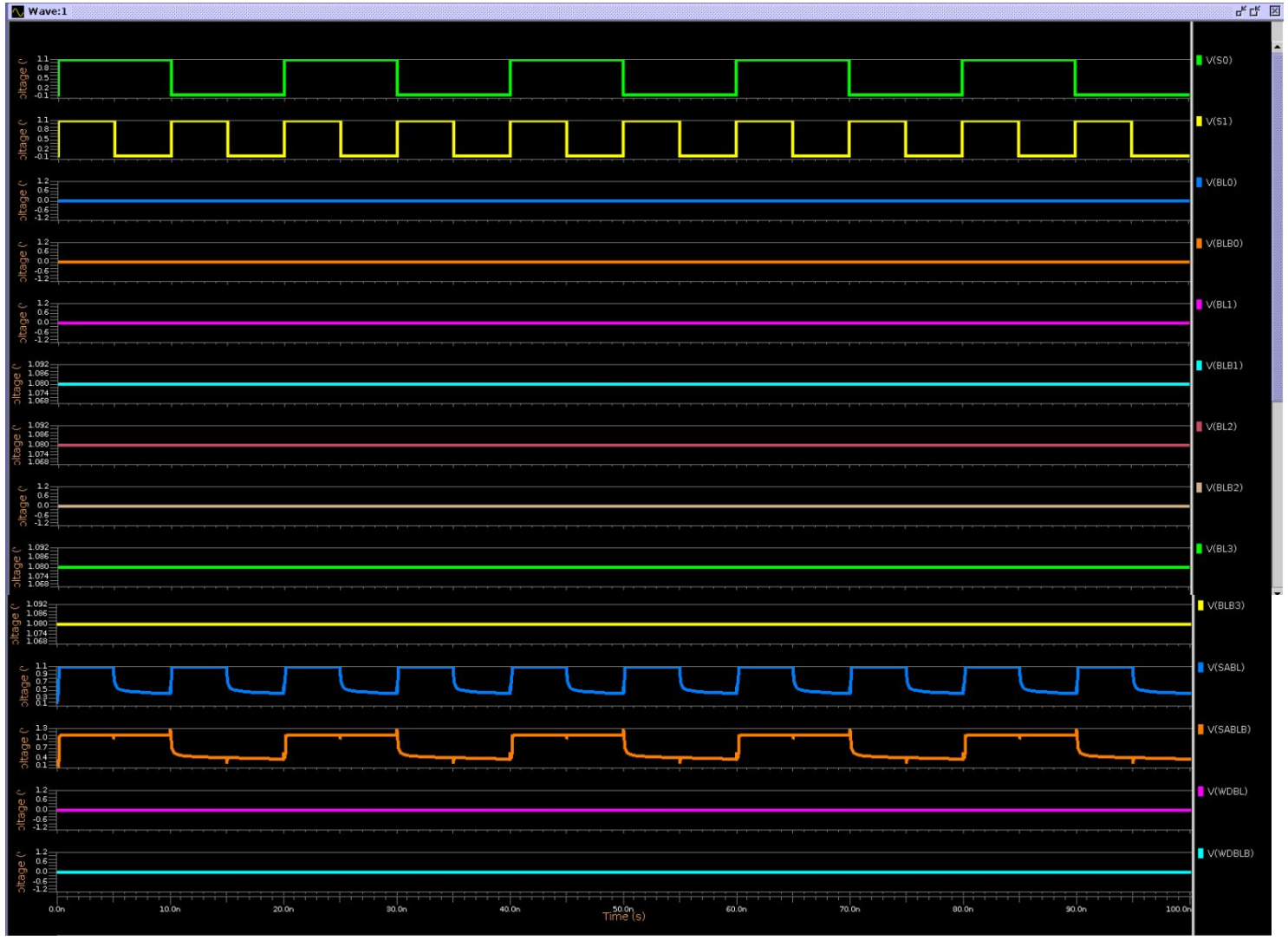
Results

Write Driver Discharge Time Simulation



Discharge time for BL and BLB: 96 ps at SS, 1.08 V, 125 °C

WaveForm of Mux Stage-1



Propagation delay at SS, 1.08 V, 125 °C is 14 ps.

Write Driver - Layout Simulation

Pre Layout Simulation -

	DISCHARGE_TIME	LEAKAGE_CURRENT	STATIC_POWER_VAL
FF 1.32 -40	102ps	-4.3255uA	-0.0057mW
FF 1.32 125	118ps	-1.4403uA	-1.9012mW
TT 1.20 25	142ps	-5.1432uA	-0.0061mW
SS 1.08 125	227ps	-62.438uA	-0.0674mW
SS 1.08 25	196ps	-0.81328uA	-0.0008mW
SS 1.08 -40	104ps	-0.052673uA	-0.00005mW

Post Layout Simulation

	DISCHARGE_TIME	LEAKAGE_CURRENT	STATIC_POWER_VAL
FF 1.32 -40	107.91 ps	−0.00026148 µA	-0.3451uW
FF 1.32 125	151.60 ps	−0.29819 µA	-3.93uW
TT 1.20 25	151.71 ps	−0.0051432 µA	-6.171uW
SS 1.08 125	234.84 ps	−0.062438 µA	-67.433uW
SS 1.08 25	200.15 ps	−0.00081336 µA	-0.8784uW
SS 1.08 -40	177.38 ps	−0.000052965 µA	-0.0572uW

Precharge - Layout Simulation

Pre Layout Simulation -

	PRECHARGE_TIME	*LEAKAGE_CURRENT*	*STATIC_POWER_VAL*
FF 1.32 -40	110.23 ps	−0.92530 µA	-1.221uW
FF 1.32 125	133.70 ps	−0.70145 µA	-0.92592uW
TT 1.20 25	162.62 ps	−0.41171 µA	-0.4940uW
SS 1.08 125	246.02 ps	−0.52095 µA	-0.5626uW
SS 1.08 25	225.10 ps	−0.52931 µA	-0.57166uW
SS 1.08 -40	205.59 ps	−0.52404 µA	-0.56596uW

Post Layout Simulation -

	PRECHARGE_TIME	*LEAKAGE_CURRENT*	*STATIC_POWER_VAL*
FF 1.32 -40	142.03 ps	−0.88815 µA	-1.1724uW
FF 1.32 125	179.74 ps	−0.69280 µA	-0.9145uW
TT 1.20 25	163.08 ps	−0.38044 µA	-0.4565uW
SS 1.08 125	250.39 ps	−0.52227 µA	-0.56406uW
SS 1.08 25	229.63 ps	−0.53029 µA	-0.5727uW
SS 1.08 -40	197.99 ps	−0.52539 µA	-0.5674uW

CONCLUSION

- Significant effort was made to **reduce write delay** in the Write Driver circuit.
- **Fingering technique** was applied by dividing the poly into three fingers, resulting in improved timing performance.
- Learned valuable concepts while implementing the **16:1 Mux Tree**, which involved a complex PMOS/NMOS arrangement.
- Understood how to optimize for:
  - **Smaller area**
  - **Better speed**
  - **Reduced stack effect**
  - **Lower parasitic capacitance**
- The project strengthened our understanding of **layout design**, **timing optimization**, and **circuit performance** under real-world constraints.

Future Work

1. Minimizing Delay, Stack Effect & Parasitic Capacitance

- Use **shorter interconnects** to reduce parasitic delay.
- Optimize **transistor sizing** to balance speed and area.
- Implement **low-capacitance routing layers** for faster transitions.
- Choose **minimum stack height** in transistor stacks to lower resistance and delay.

2. Area-Efficient & High-Speed Performance

- Prefer **compact layout styles** like folding or fingering.
- Use **multi-finger transistors** for better area utilization and faster switching.
- Apply **device sharing** strategies to reuse transistors where possible.

3. Write Driver Placement Between Mux1 and Mux2

- Test placing the **write driver between MUX1 and MUX2** to check if:
  - Discharge time is reduced.
  - Signal travel distance is minimized.
  - Load on the driver is better balanced.

Future Work

4. Advanced Fingering Techniques

- Use **dynamic finger segmentation** based on switching activity.
- Optimize finger width and spacing to **minimize discharge time**.
- Aim for **lower silicon area** with equal or better performance.

5. Improved Multiplexer Designs

- Explore **alternative MUX architectures** (like tree or lattice structures).
- Reduce number of stages in two-stage MUX if possible.
- Test **reconfigurable MUX logic** to reduce overall capacitance.
- Focus on **better signal integrity** and **lower delay paths**.

Work Distribution

- **Aman Kumar:** Schematic design (Virtuoso) – Column MUX and ADEL simulation for functional verification, Layout verification and pre- and post-simulation .
- **Mintu Kumar:** Schematic design (Virtuoso) – Write driver and precharge circuit, and layout design.
- **Dhruv Sharma:** Schematic design (Virtuoso) – Write driver and X-circuit, and pre- and post-simulation.
- **Noorain Ansari:** PPT.