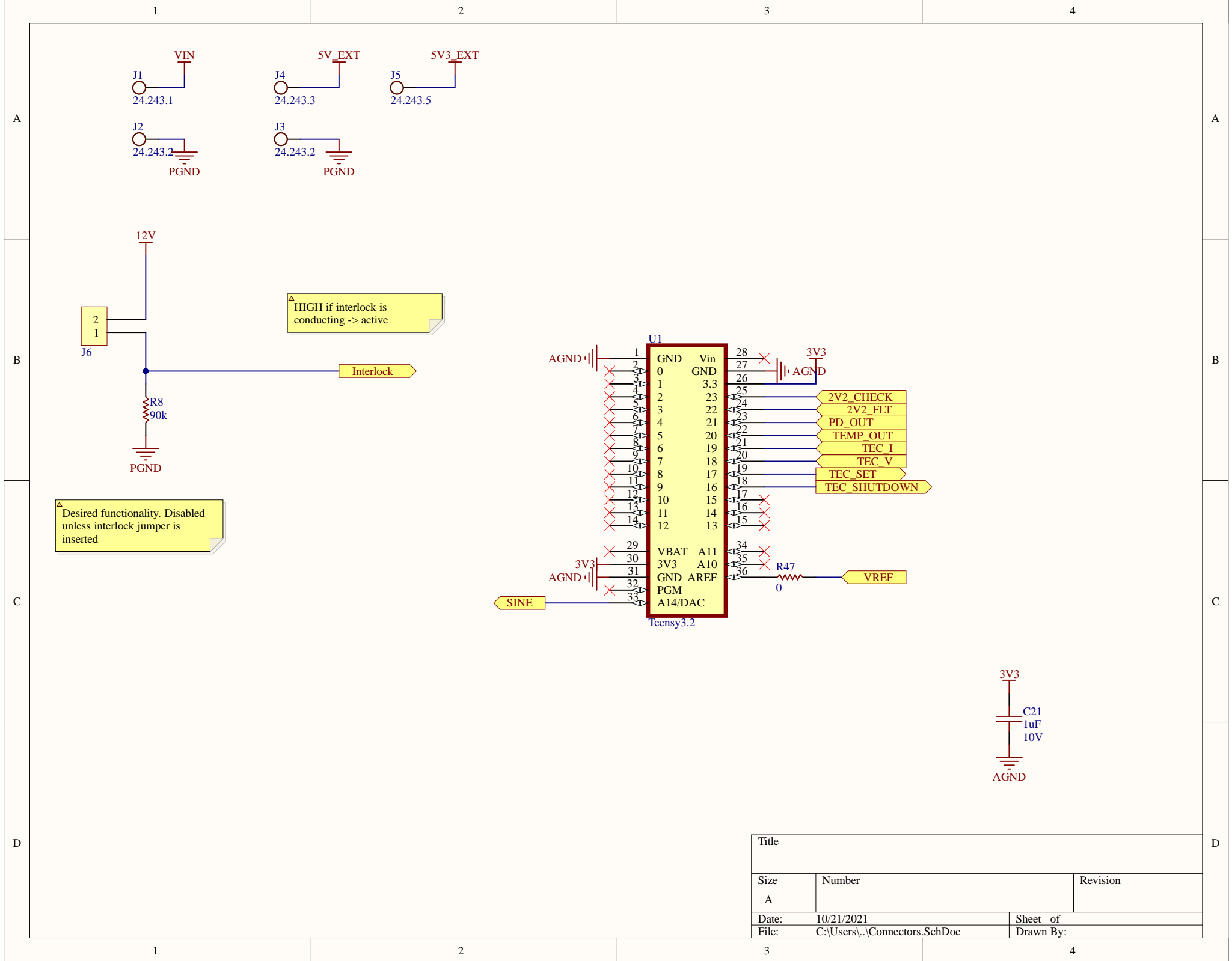
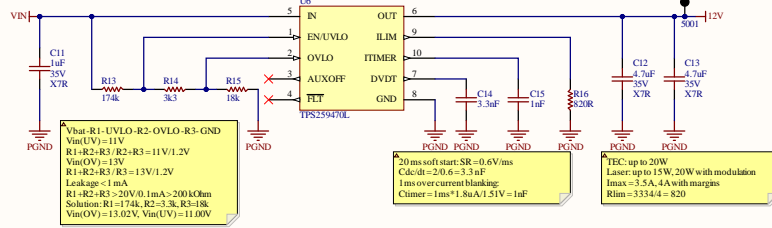


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Date:	10/21/2021	Sheet of
File:	C:\Users\...\Top.SchDoc	Drawn By:

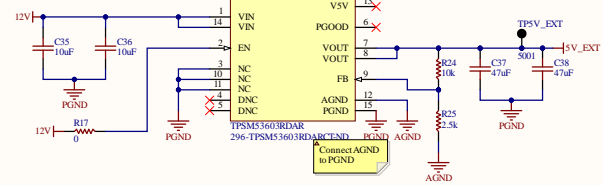


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Power Input Protection

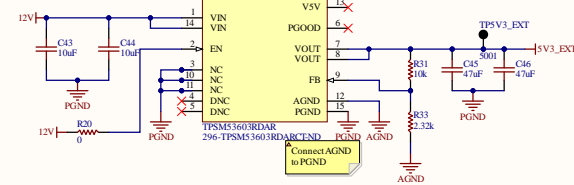


External 5V

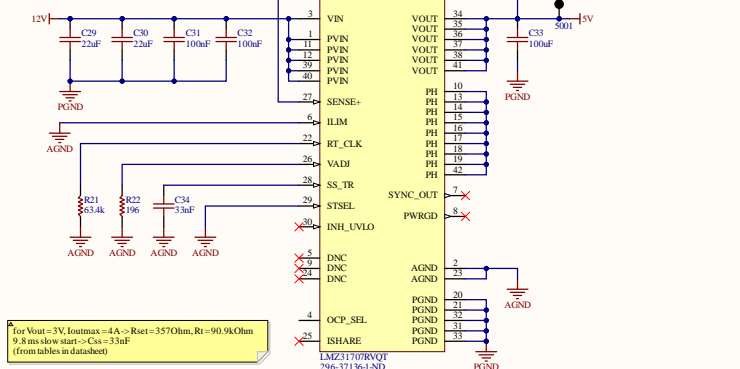


FB Voltage Divider for R_FBT, 10kOhm is recommended
R_FBB = 10(V_out - 1)kOhm
V_out = 5V -> 2.5kOhm
V_out = 5.3V -> 2.32kOhm
V_out = 3.3V -> 4.35kOhm

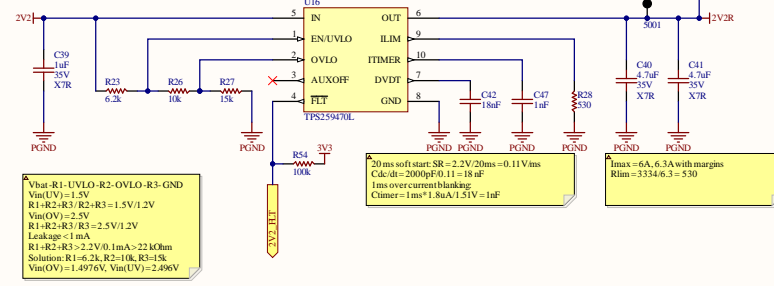
External 5V3



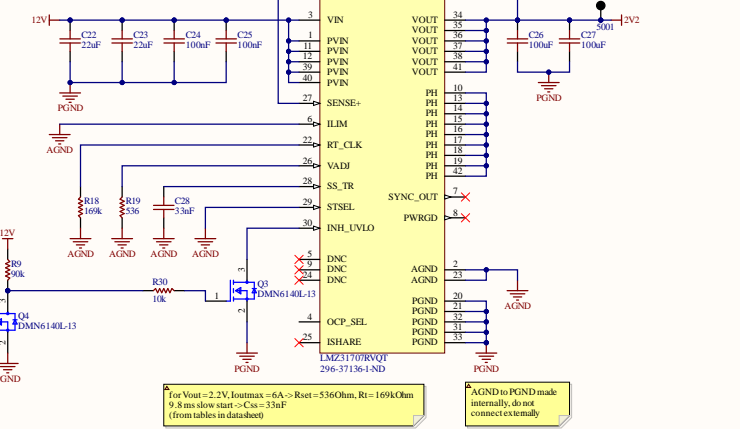
5V (TEC) Power



Laser Diode OVC



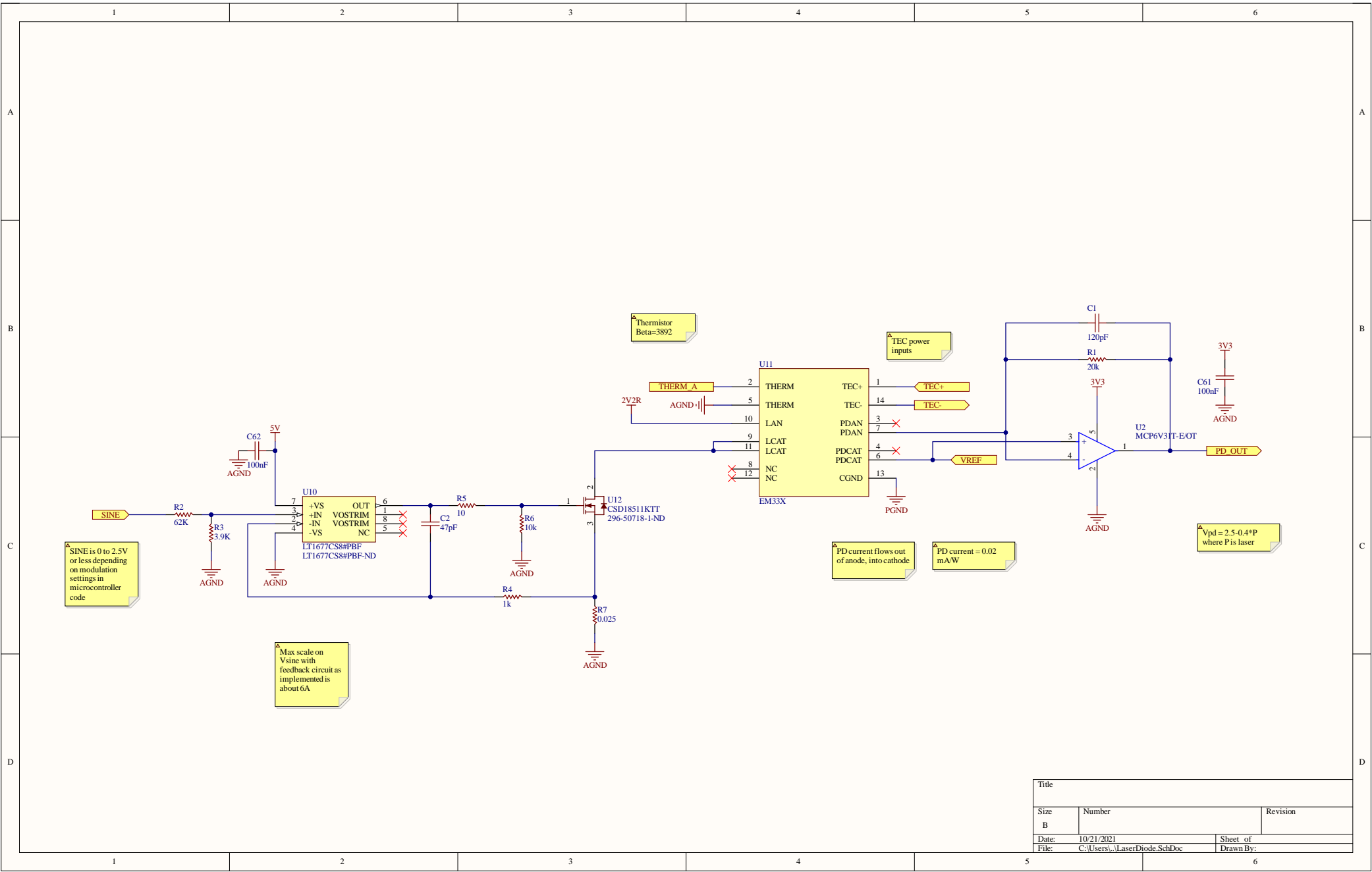
Laser Diode Power



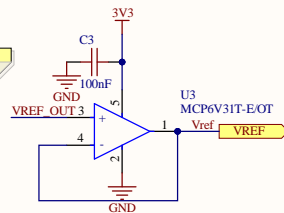
HIGH if interlock is inserted. This causes NFET to be ON. This causes the INH pin to be pulled low. This disables the power supply. Inserted -> OFF
Conversely removed -> ON

GNDs are connected internal to the power modules. Where noted they will be short circuited deliberately in layout. These are indicated with notes. The design rules allow short from AGND to PGND

Title		
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File	C:\Users\j.Power\SchDoc	Drawn By:

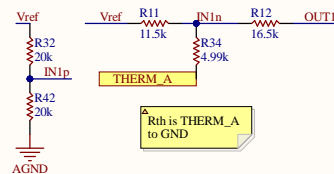
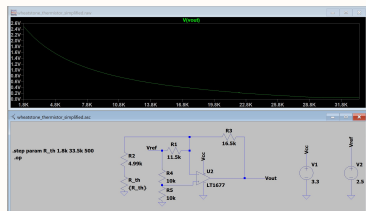
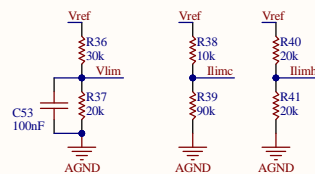


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Date: 10/21/2021	Sheet of	
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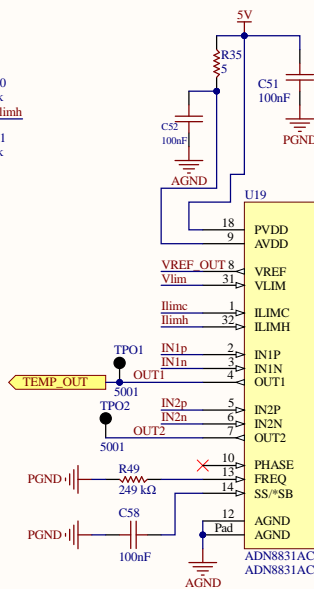


$I(V_{refout})$ must be < 2 mA

Parameters:
 $V_{ref} = 2.5$ V, $I_{TC_max} = 4$ A, $I_{TH_max} = 0$ A,
 $R_{sense} = 0.01$ ohms, $V_{T_max} = 5$ V
 $V_{ILIMC} = (V_{ref}/2) + (25 \cdot I_{TC_max} \cdot R_s)$
 $\rightarrow V_{ILIMC} = 2.25$ V
 $V_{ILIMH} = (V_{ref}/2) - (25 \cdot I_{TC_max} \cdot R_s)$
 $\rightarrow V_{ILIMH} = 1.25$ V
 $V_{VLIM} = V_{T_max}/5$
 $\rightarrow V_{VLIM} = 1$ V

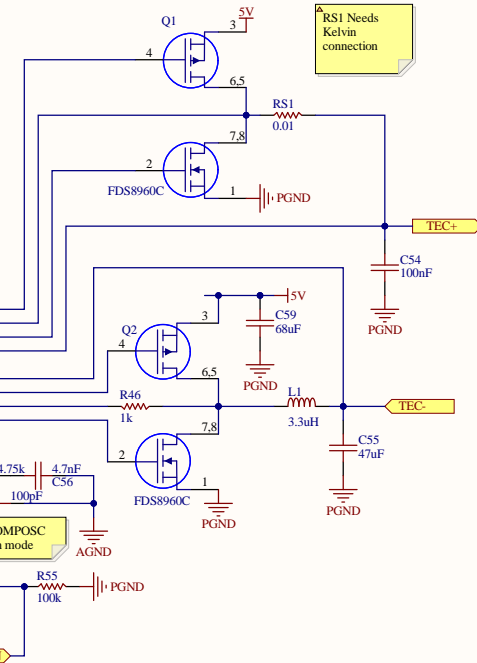


R_{th} is THERM_A to GND

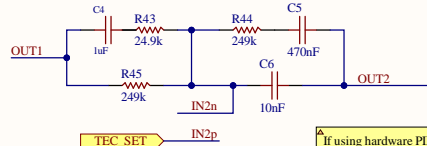
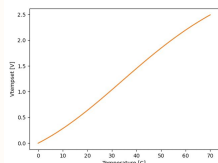


TEC_I and TEC_V
 Range from 0 to 5V
 theoretically
 0V to 2.25 V
 expected

RS1 Needs Kelvin connection

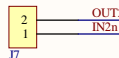


COMP SW and COMPOS not used in free run mode



TEC_SET

This jumper bypasses hardware PID



If using hardware PID, TEC_SET voltage corresponds to requested temp. Otherwise TEC_SET is modified based on software PID

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Date:	10/21/2021	Sheet of
File:	C:\Users\TEC\Documents\TECController.SchDoc	Drawn By: