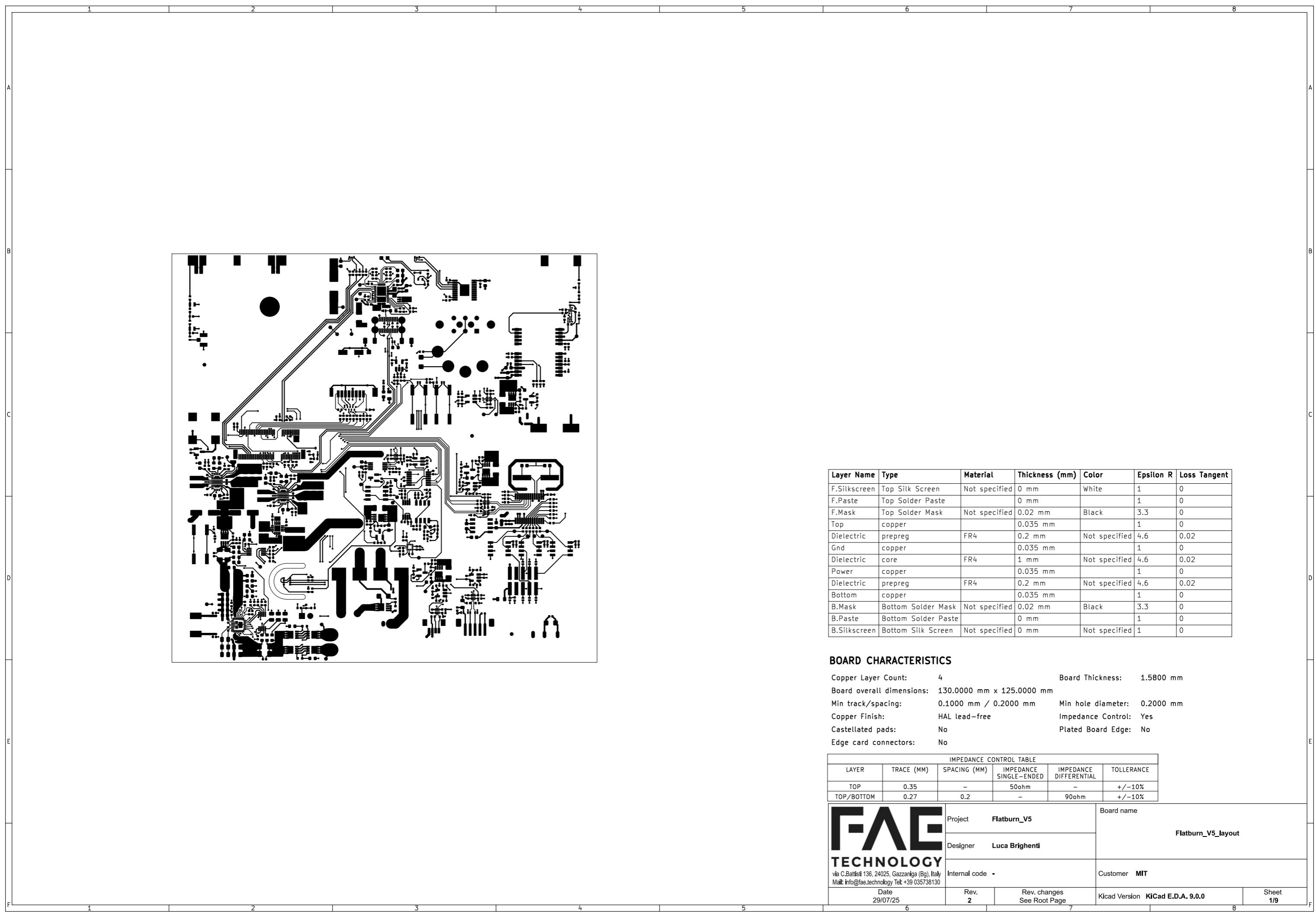


1 2 3 4 5 6 7 8



A A

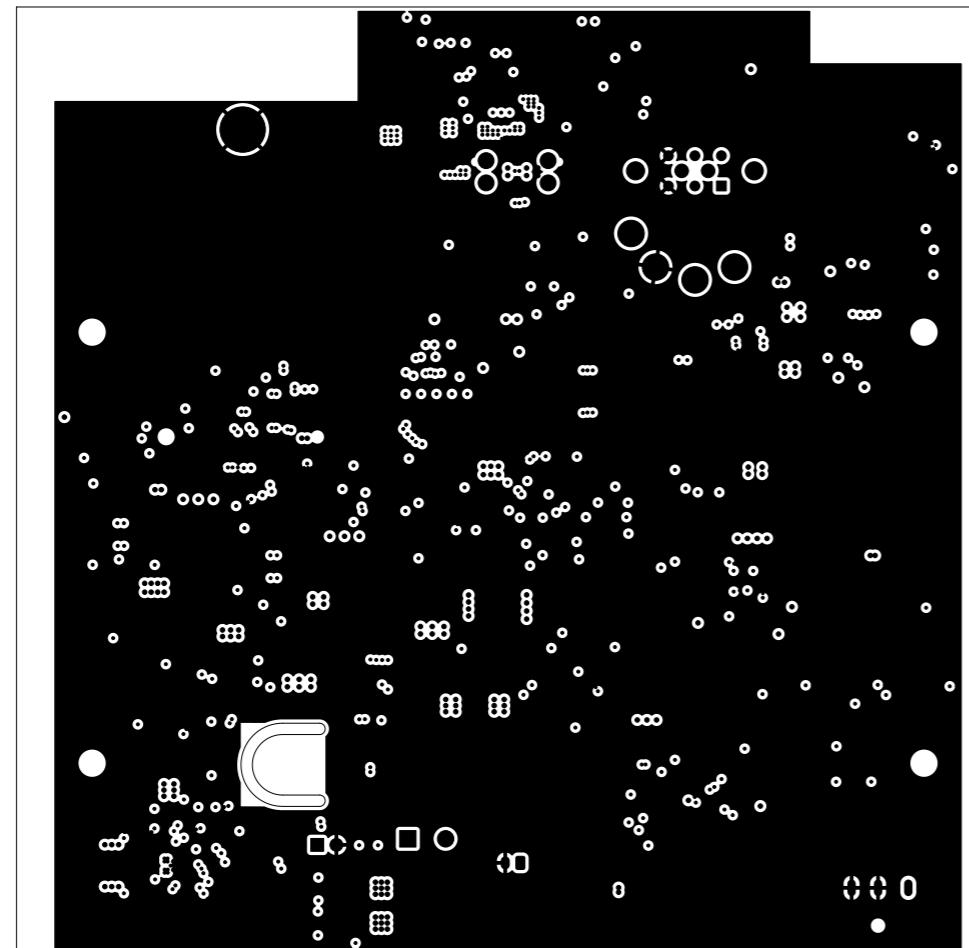
B B

C C

D D

E E

F F



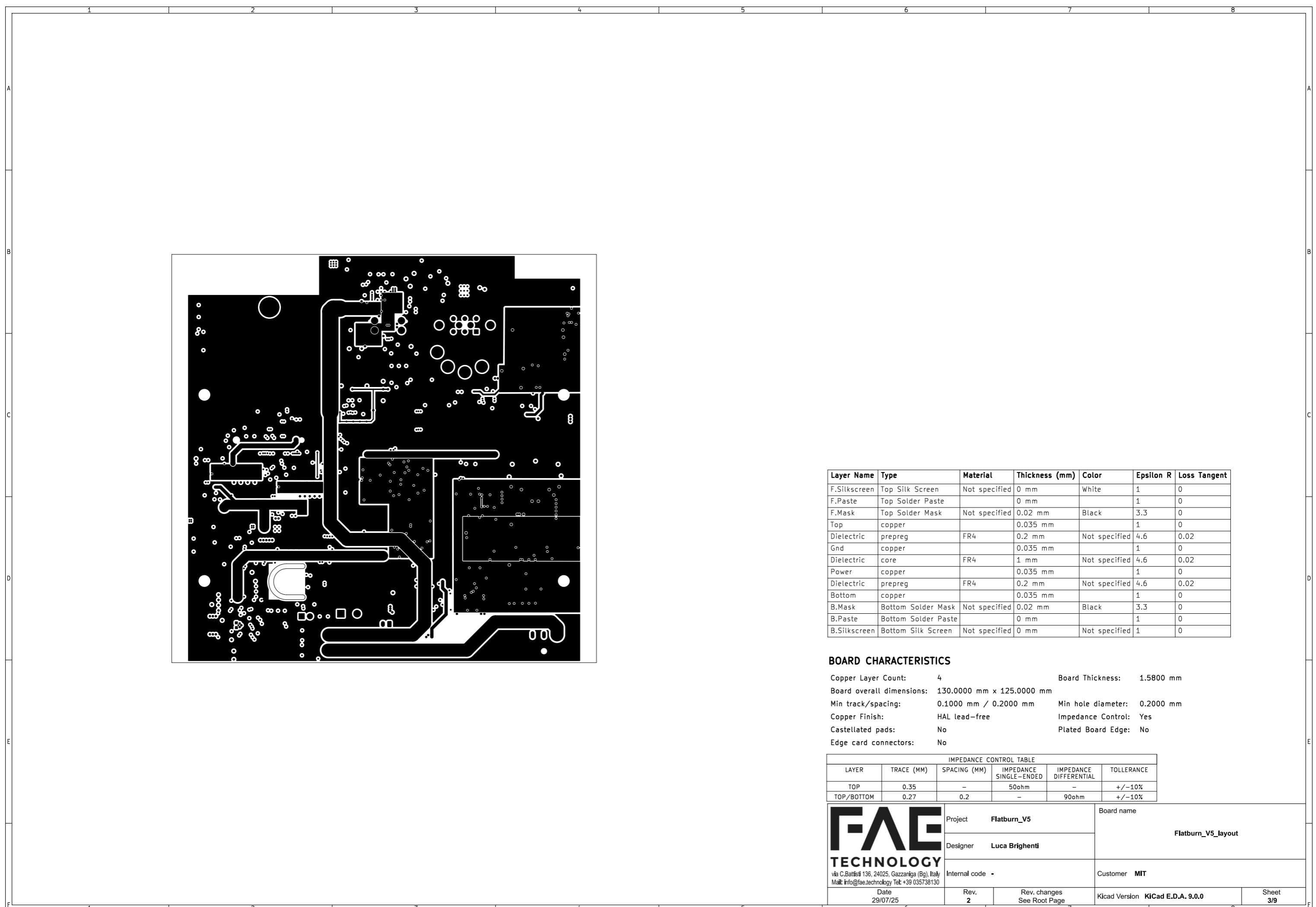
Layer Name	Type	Material	Thickness (mm)	Color	Epsilon R	Loss Tangent
F.Silkscreen	Top Silk Screen	Not specified	0 mm	White	1	0
F.Paste	Top Solder Paste		0 mm		1	0
F.Mask	Top Solder Mask	Not specified	0.02 mm	Black	3.3	0
Top	copper		0.035 mm		1	0
Dielectric	prepreg	FR4	0.2 mm	Not specified	4.6	0.02
Gnd	copper		0.035 mm		1	0
Dielectric	core	FR4	1 mm	Not specified	4.6	0.02
Power	copper		0.035 mm		1	0
Dielectric	prepreg	FR4	0.2 mm	Not specified	4.6	0.02
Bottom	copper		0.035 mm		1	0
B.Mask	Bottom Solder Mask	Not specified	0.02 mm	Black	3.3	0
B.Paste	Bottom Solder Paste		0 mm		1	0
B.Silkscreen	Bottom Silk Screen	Not specified	0 mm	Not specified	1	0

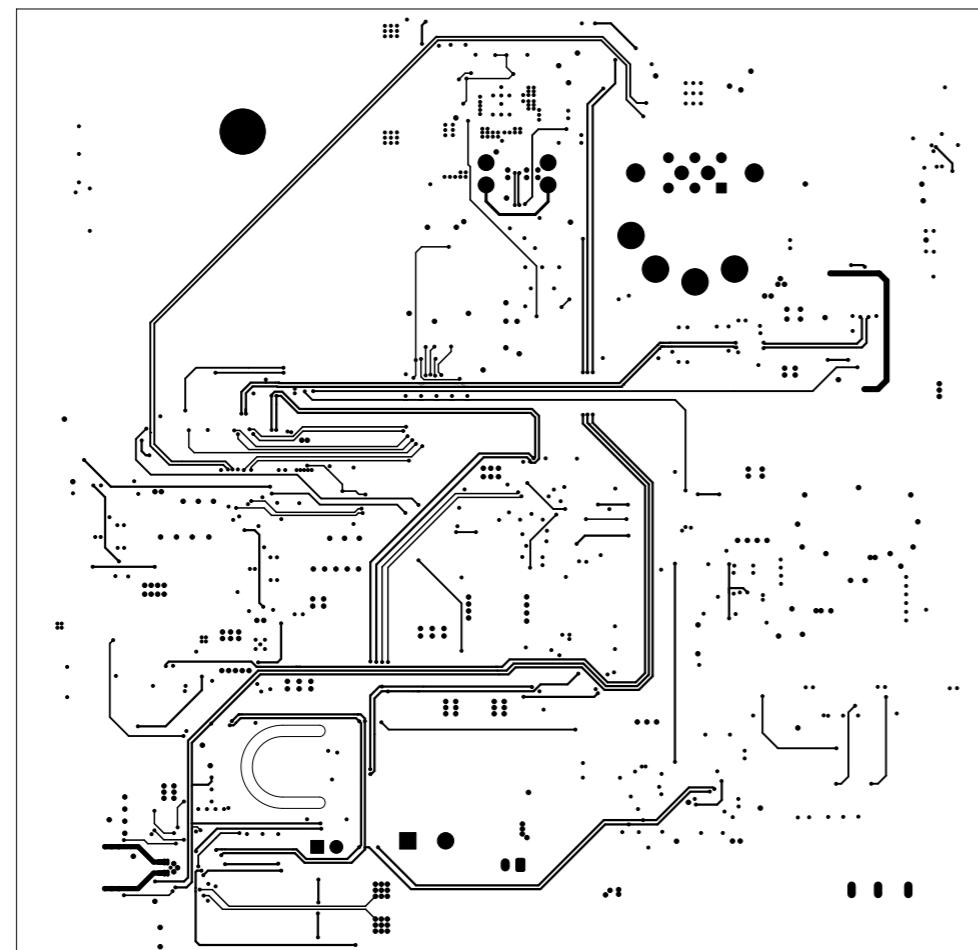
BOARD CHARACTERISTICS

Copper Layer Count: 4 Board Thickness: 1.5800 mm
 Board overall dimensions: 130.0000 mm x 125.0000 mm
 Min track/spacing: 0.1000 mm / 0.2000 mm Min hole diameter: 0.2000 mm
 Copper Finish: HAL lead-free Impedance Control: Yes
 Castellated pads: No Plated Board Edge: No
 Edge card connectors: No

IMPEDANCE CONTROL TABLE					
LAYER	TRACE (MM)	SPACING (MM)	IMPEDANCE SINGLE-ENDED	IMPEDANCE DIFFERENTIAL	TOLERANCE
TOP	0.35	-	50ohm	-	+/-10%
TOP/BOTTOM	0.27	0.2	-	90ohm	+/-10%

 Project Flatburn_V5	Board name Flatburn_V5_layout	
	Designer Luca Brighenti	
	Internal code -	Customer MIT
Date 29/07/25	Rev. 2	Rev. changes See Root Page
Kicad Version	Kicad E.D.A. 9.0.0	Sheet 2/9





Layer Name	Type	Material	Thickness (mm)	Color	Epsilon R	Loss Tangent
F.Silkscreen	Top Silk Screen	Not specified	0 mm	White	1	0
F.Paste	Top Solder Paste		0 mm		1	0
F.Mask	Top Solder Mask	Not specified	0.02 mm	Black	3.3	0
Top	copper		0.035 mm		1	0
Dielectric	prepreg	FR4	0.2 mm	Not specified	4.6	0.02
Gnd	copper		0.035 mm		1	0
Dielectric	core	FR4	1 mm	Not specified	4.6	0.02
Power	copper		0.035 mm		1	0
Dielectric	prepreg	FR4	0.2 mm	Not specified	4.6	0.02
Bottom	copper		0.035 mm		1	0
B.Mask	Bottom Solder Mask	Not specified	0.02 mm	Black	3.3	0
B.Paste	Bottom Solder Paste		0 mm		1	0
B.Silkscreen	Bottom Silk Screen	Not specified	0 mm	Not specified	1	0

BOARD CHARACTERISTICS

Copper Layer Count: 4 Board Thickness: 1.5800 mm
 Board overall dimensions: 130.0000 mm x 125.0000 mm
 Min track/spacing: 0.1000 mm / 0.2000 mm Min hole diameter: 0.2000 mm
 Copper Finish: HAL lead-free Impedance Control: Yes
 Castellated pads: No Plated Board Edge: No
 Edge card connectors: No

IMPEDANCE CONTROL TABLE					
LAYER	TRACE (MM)	SPACING (MM)	IMPEDANCE SINGLE-ENDED	IMPEDANCE DIFFERENTIAL	TOLERANCE
TOP	0.35	-	50ohm	-	+/-10%
TOP/BOTTOM	0.27	0.2	-	90ohm	+/-10%

 via C.Battisti 136, 24025, Gazzaniga (Bg), Italy Mail: info@fae.technology Tel: +39 035738130	Project	Flatburn_V5	Board name Flatburn_V5_layout
	Designer	Luca Brighenti	
	Internal code	-	
Date	29/07/25	Rev.	Customer MIT
		2	See Root Page
Rev. changes			Kicad Version KiCad E.D.A. 9.0.0
			Sheet 4/9

A A

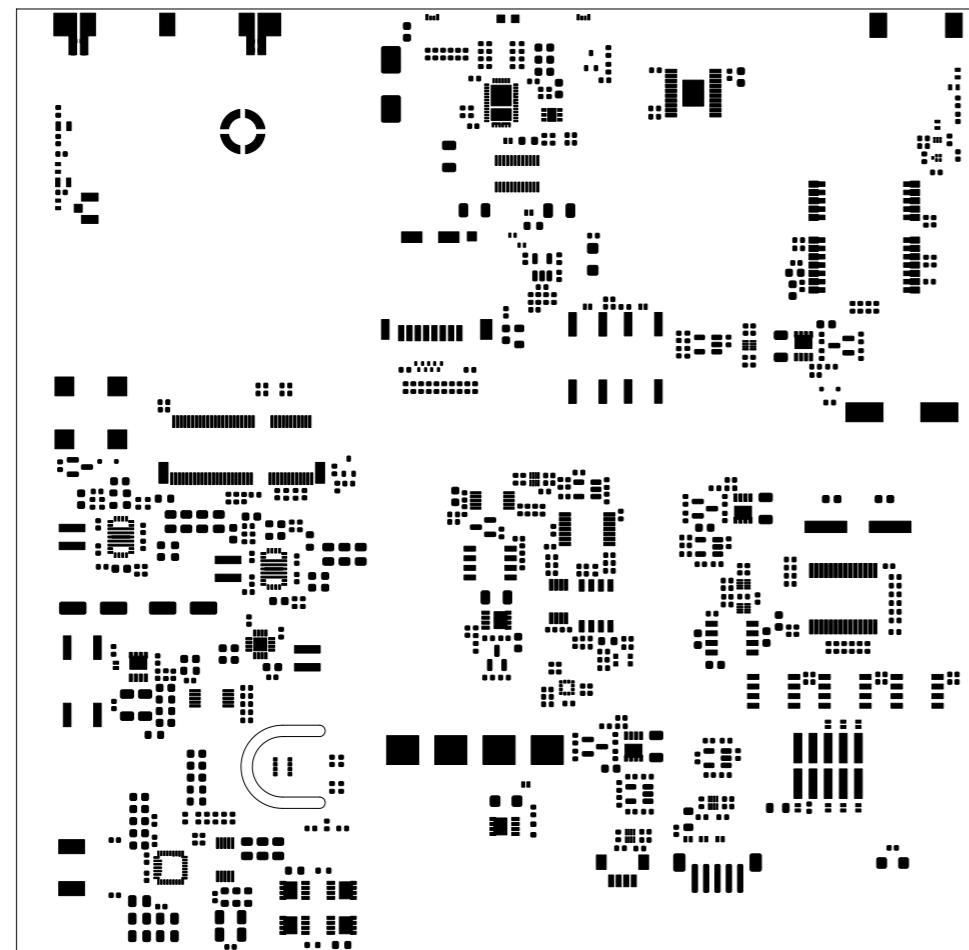
B B

C C

D D

E E

F F



Layer Name	Type	Material	Thickness (mm)	Color	Epsilon R	Loss Tangent
F.Silkscreen	Top Silk Screen	Not specified	0 mm	White	1	0
F.Paste	Top Solder Paste		0 mm		1	0
F.Mask	Top Solder Mask	Not specified	0.02 mm	Black	3.3	0
Top	copper		0.035 mm		1	0
Dielectric	prepreg	FR4	0.2 mm	Not specified	4.6	0.02
Gnd	copper		0.035 mm		1	0
Dielectric	core	FR4	1 mm	Not specified	4.6	0.02
Power	copper		0.035 mm		1	0
Dielectric	prepreg	FR4	0.2 mm	Not specified	4.6	0.02
Bottom	copper		0.035 mm		1	0
B.Mask	Bottom Solder Mask	Not specified	0.02 mm	Black	3.3	0
B.Paste	Bottom Solder Paste		0 mm		1	0
B.Silkscreen	Bottom Silk Screen	Not specified	0 mm	Not specified	1	0

BOARD CHARACTERISTICS

Copper Layer Count: 4 Board Thickness: 1.5800 mm
 Board overall dimensions: 130.0000 mm x 125.0000 mm
 Min track/spacing: 0.1000 mm / 0.2000 mm Min hole diameter: 0.2000 mm
 Copper Finish: HAL lead-free Impedance Control: Yes
 Castellated pads: No Plated Board Edge: No
 Edge card connectors: No

IMPEDANCE CONTROL TABLE					
LAYER	TRACE (MM)	SPACING (MM)	IMPEDANCE SINGLE-ENDED	IMPEDANCE DIFFERENTIAL	TOLLERANCE
TOP	0.35	-	50ohm	-	+/-10%
TOP/BOTTOM	0.27	0.2	-	90ohm	+/-10%

 via C.Battisti 136, 24025, Gazzaniga (Bg), Italy Mail: info@fae.technology Tel: +39 035738130	Project	Flatburn_V5	Board name Flatburn_V5_layout
	Designer	Luca Brighenti	
	Internal code	-	
	Date	Rev. 2	Customer MIT
	29/07/25	Rev. changes See Root Page	Kicad Version KiCad E.D.A. 9.0.0
			Sheet 5/9

A

B

C

D

E

F

A

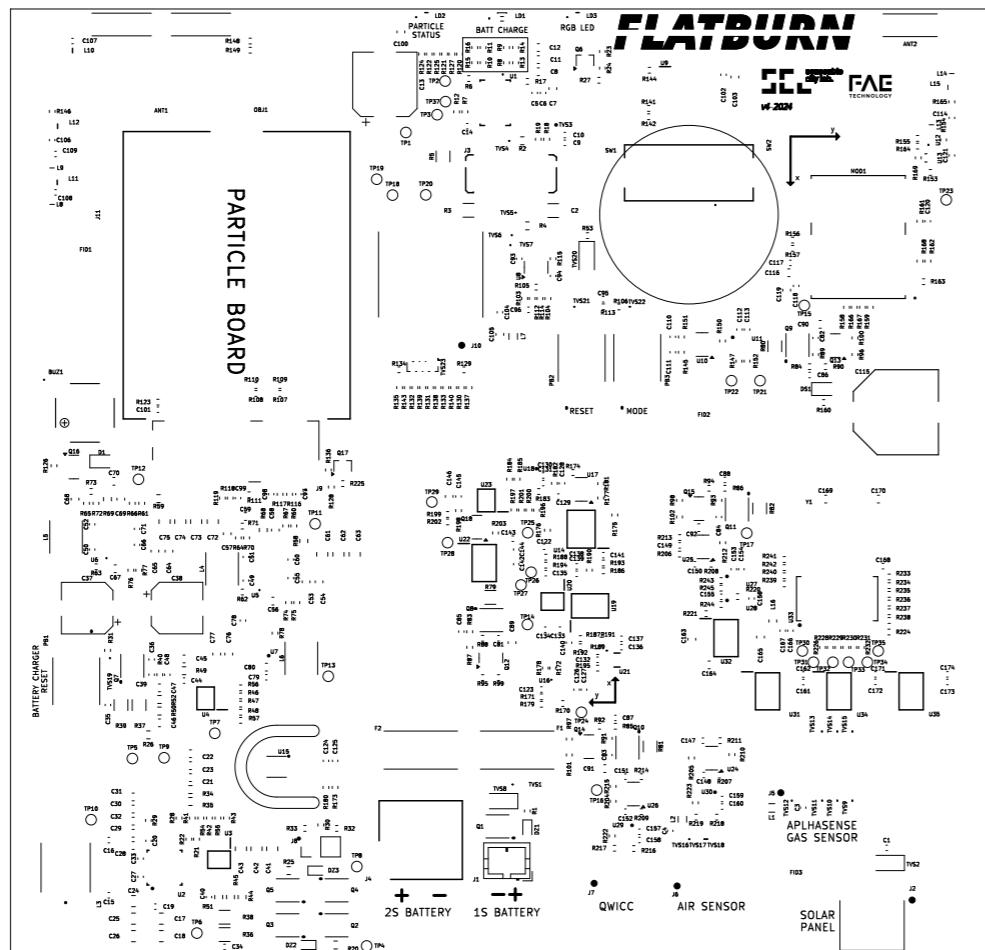
B

C

D

E

F



Layer Name	Type	Material	Thickness (mm)	Color	Epsilon R	Loss Tangent
F.Silkscreen	Top Silk Screen	Not specified	0 mm	White	1	0
F.Paste	Top Solder Paste		0 mm		1	0
F.Mask	Top Solder Mask	Not specified	0.02 mm	Black	3.3	0
Top	copper		0.035 mm		1	0
Dielectric	prepreg	FR4	0.2 mm	Not specified	4.6	0.02
Gnd	copper		0.035 mm		1	0
Dielectric	core	FR4	1 mm	Not specified	4.6	0.02
Power	copper		0.035 mm		1	0
Dielectric	prepreg	FR4	0.2 mm	Not specified	4.6	0.02
Bottom	copper		0.035 mm		1	0
B.Mask	Bottom Solder Mask	Not specified	0.02 mm	Black	3.3	0
B.Paste	Bottom Solder Paste		0 mm		1	0
B.Silkscreen	Bottom Silk Screen	Not specified	0 mm	Not specified	1	0

BOARD CHARACTERISTICS

Copper Layer Count: 4 Board Thickness: 1.5800 mm
 Board overall dimensions: 130.0000 mm x 125.0000 mm
 Min track/spacing: 0.1000 mm / 0.2000 mm Min hole diameter: 0.2000 mm
 Copper Finish: HAL lead-free Impedance Control: Yes
 Castellated pads: No Plated Board Edge: No
 Edge card connectors: No

IMPEDANCE CONTROL TABLE					
LAYER	TRACE (MM)	SPACING (MM)	IMPEDANCE SINGLE-ENDED	IMPEDANCE DIFFERENTIAL	TOLLERANCE
TOP	0.35	—	50ohm	—	+/-10%
TOP/BOTTOM	0.27	0.2	—	90ohm	+/-10%

 <p>via C.Battisti 136, 24025, Gazzaniga (Bg), Italy Mail: info@fae.technology Tel: +39 035738130</p>	Project	Flatburn_V5	Board name Flatburn_V5_layout
	Designer	Luca Brighenti	
	Internal code	-	
	Date	Rev. 2 See Root Page	Customer MIT
	29/07/25		Kicad Version KiCad E.D.A. 9.0.0
			Sheet 6/9

A A

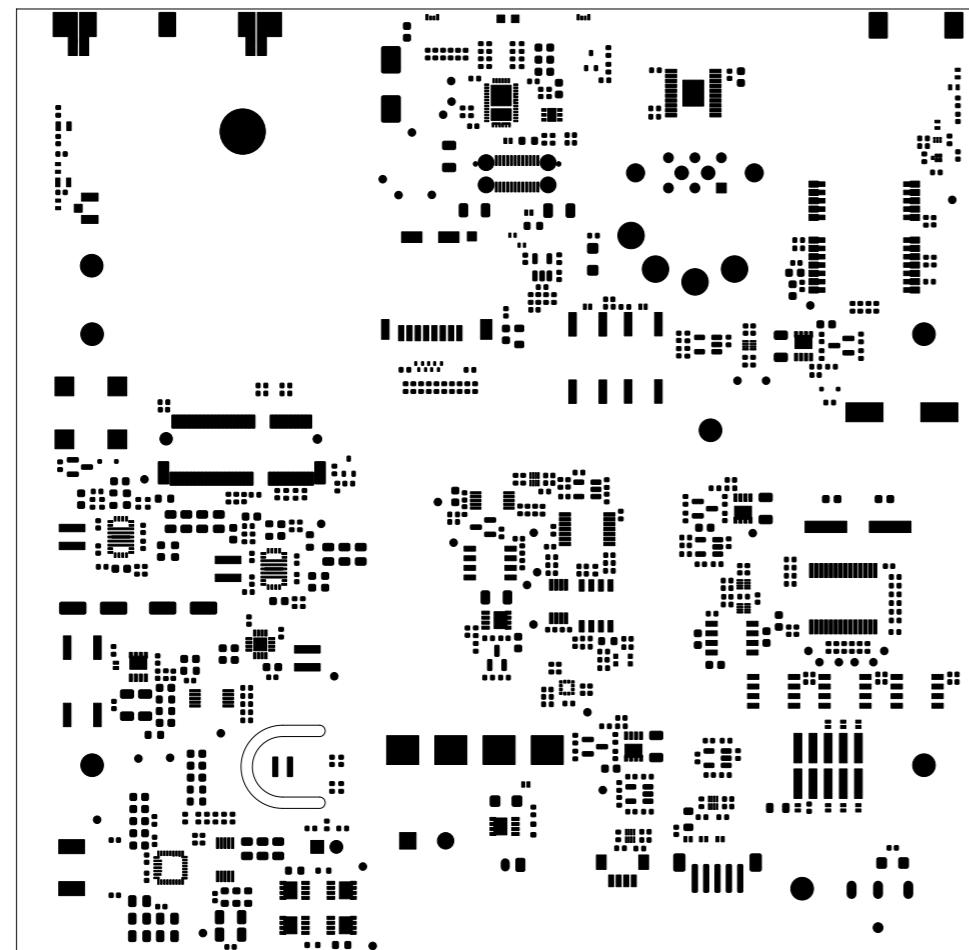
B B

C C

D D

E E

F F



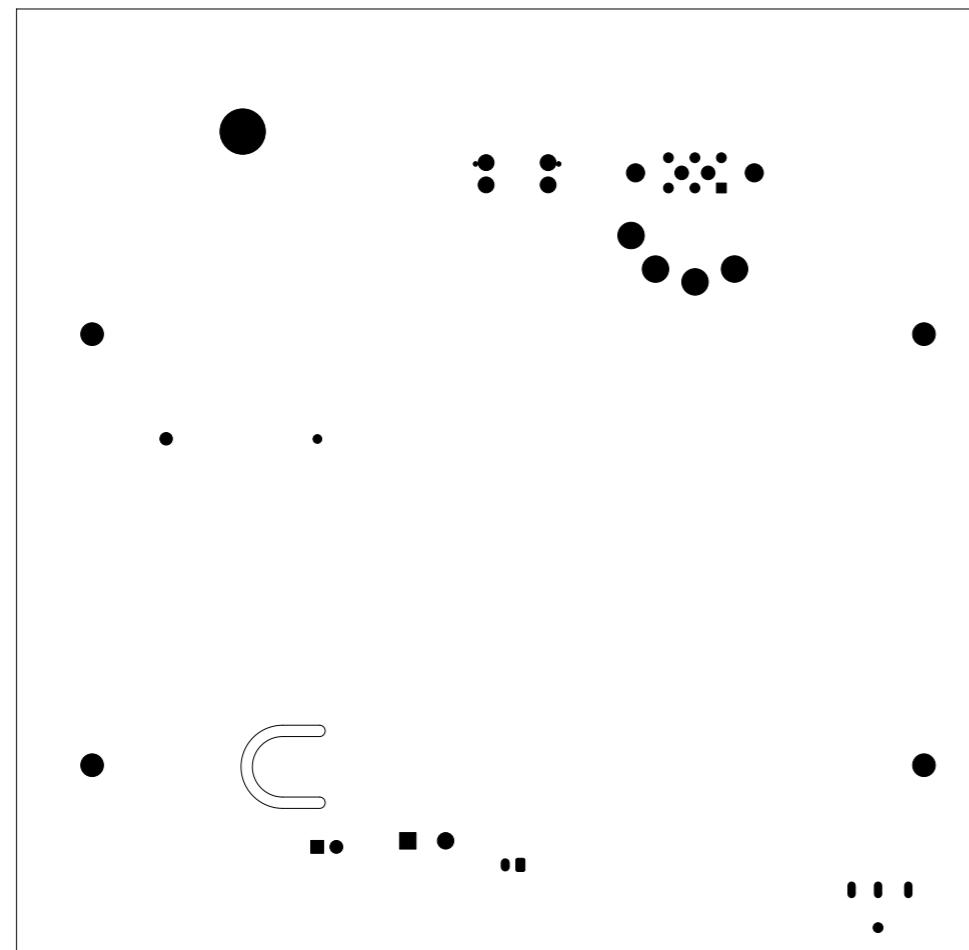
Layer Name	Type	Material	Thickness (mm)	Color	Epsilon R	Loss Tangent
F.Silkscreen	Top Silk Screen	Not specified	0 mm	White	1	0
F.Paste	Top Solder Paste		0 mm		1	0
F.Mask	Top Solder Mask	Not specified	0.02 mm	Black	3.3	0
Top	copper		0.035 mm		1	0
Dielectric	prepreg	FR4	0.2 mm	Not specified	4.6	0.02
Gnd	copper		0.035 mm		1	0
Dielectric	core	FR4	1 mm	Not specified	4.6	0.02
Power	copper		0.035 mm		1	0
Dielectric	prepreg	FR4	0.2 mm	Not specified	4.6	0.02
Bottom	copper		0.035 mm		1	0
B.Mask	Bottom Solder Mask	Not specified	0.02 mm	Black	3.3	0
B.Paste	Bottom Solder Paste		0 mm		1	0
B.Silkscreen	Bottom Silk Screen	Not specified	0 mm	Not specified	1	0

BOARD CHARACTERISTICS

Copper Layer Count: 4 Board Thickness: 1.5800 mm
 Board overall dimensions: 130.0000 mm x 125.0000 mm
 Min track/spacing: 0.1000 mm / 0.2000 mm Min hole diameter: 0.2000 mm
 Copper Finish: HAL lead-free Impedance Control: Yes
 Castellated pads: No Plated Board Edge: No
 Edge card connectors: No

IMPEDANCE CONTROL TABLE					
LAYER	TRACE (MM)	SPACING (MM)	IMPEDANCE SINGLE-ENDED	IMPEDANCE DIFFERENTIAL	TOLERANCE
TOP	0.35	-	50ohm	-	+/-10%
TOP/BOTTOM	0.27	0.2	-	90ohm	+/-10%

 via C.Battisti 136, 24025, Gazzaniga (Bg), Italy Mail: info@fae.technology Tel: +39 035738130	Project	Flatburn_V5	Board name Flatburn_V5_layout
	Designer	Luca Brighenti	
	Internal code	-	
Date	29/07/25	Rev.	Customer MIT
Rev. changes	See Root Page	Kicad Version	Kicad E.D.A. 9.0.0
		Sheet	7/9



Layer Name	Type	Material	Thickness (mm)	Color	Epsilon R	Loss Tangent
F.Silkscreen	Top Silk Screen	Not specified	0 mm	White	1	0
F.Paste	Top Solder Paste		0 mm		1	0
F.Mask	Top Solder Mask	Not specified	0.02 mm	Black	3.3	0
Top	copper		0.035 mm		1	0
Dielectric	prepreg	FR4	0.2 mm	Not specified	4.6	0.02
Gnd	copper		0.035 mm		1	0
Dielectric	core	FR4	1 mm	Not specified	4.6	0.02
Power	copper		0.035 mm		1	0
Dielectric	prepreg	FR4	0.2 mm	Not specified	4.6	0.02
Bottom	copper		0.035 mm		1	0
B.Mask	Bottom Solder Mask	Not specified	0.02 mm	Black	3.3	0
B.Paste	Bottom Solder Paste		0 mm		1	0
B.Silkscreen	Bottom Silk Screen	Not specified	0 mm	Not specified	1	0

BOARD CHARACTERISTICS

Copper Layer Count: 4 Board Thickness: 1.5800 mm
 Board overall dimensions: 130.0000 mm x 125.0000 mm
 Min track/spacing: 0.1000 mm / 0.2000 mm Min hole diameter: 0.2000 mm
 Copper Finish: HAL lead-free Impedance Control: Yes
 Castellated pads: No Plated Board Edge: No
 Edge card connectors: No

IMPEDANCE CONTROL TABLE					
LAYER	TRACE (MM)	SPACING (MM)	IMPEDANCE SINGLE-ENDED	IMPEDANCE DIFFERENTIAL	TOLERANCE
TOP	0.35	-	50ohm	-	+/-10%
TOP/BOTTOM	0.27	0.2	-	90ohm	+/-10%

 via C.Battisti 136, 24025, Gazzaniga (Bg), Italy Mail: info@fae.technology Tel: +39 035738130	Project	Flatburn_V5	Board name Flatburn_V5_layout
	Designer	Luca Brighenti	
	Internal code	-	
Date	Rev.	Rev. changes See Root Page	Customer MIT
29/07/25	2		Kicad Version KiCad E.D.A. 9.0.0
			Sheet 8/9

A

B

C

D

E

F

A

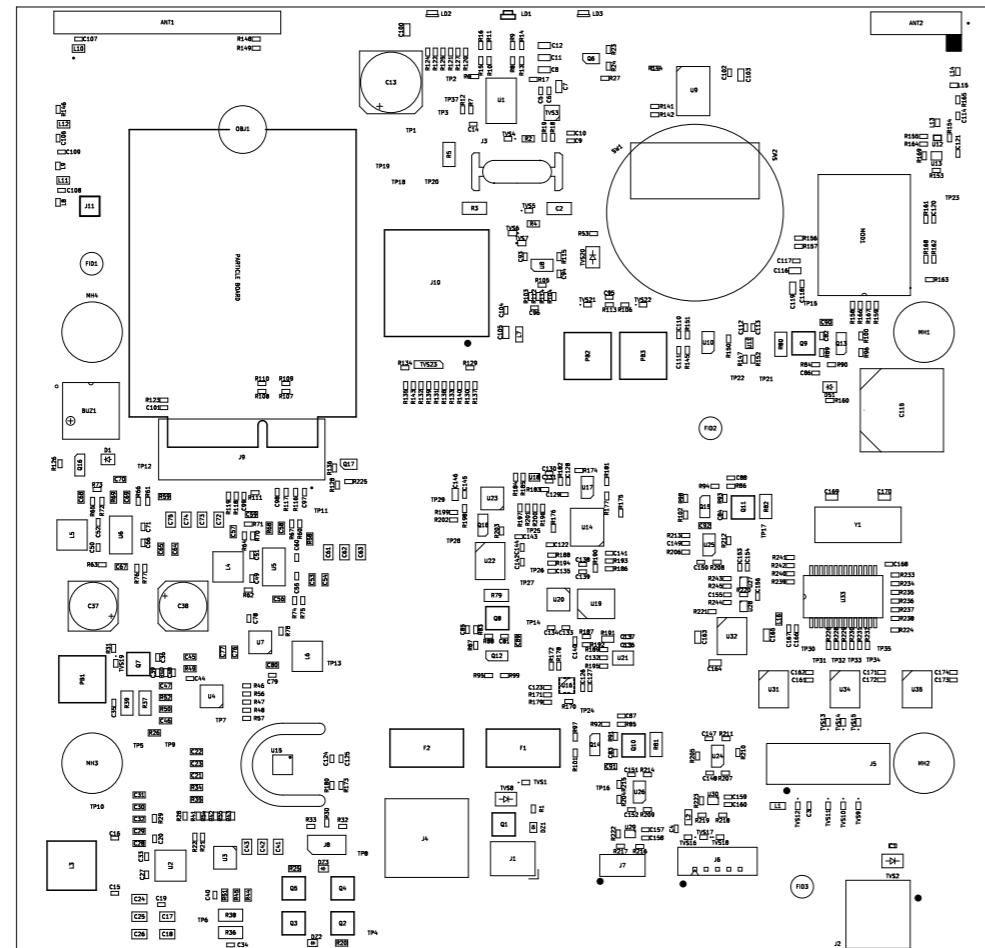
B

C

D

E

F



Layer Name	Type	Material	Thickness (mm)	Color	Epsilon R	Loss Tangent
F.Silkscreen	Top Silk Screen	Not specified	0 mm	White	1	0
F.Paste	Top Solder Paste		0 mm		1	0
F.Mask	Top Solder Mask	Not specified	0.02 mm	Black	3.3	0
Top	copper		0.035 mm		1	0
Dielectric	prepreg	FR4	0.2 mm	Not specified	4.6	0.02
Gnd	copper		0.035 mm		1	0
Dielectric	core	FR4	1 mm	Not specified	4.6	0.02
Power	copper		0.035 mm		1	0
Dielectric	prepreg	FR4	0.2 mm	Not specified	4.6	0.02
Bottom	copper		0.035 mm		1	0
B.Mask	Bottom Solder Mask	Not specified	0.02 mm	Black	3.3	0
B.Paste	Bottom Solder Paste		0 mm		1	0
B.Silkscreen	Bottom Silk Screen	Not specified	0 mm	Not specified	1	0

BOARD CHARACTERISTICS

Copper Layer Count: 4 Board Thickness: 1.5800 mm

Board overall dimensions: 130.0000 mm x 125.0000 mm

Min track/spacing: 0.1000 mm / 0.2000 mm Min hole diameter: 0.2000 mm

Copper Finish: HAL lead-free Impedance Control: Yes

Castellated pads: No Plated Board Edge: No

Edge card connectors: No

IMPEDANCE CONTROL TABLE					
LAYER	TRACE (MM)	SPACING (MM)	IMPEDANCE SINGLE-ENDED	IMPEDANCE DIFFERENTIAL	TOLERANCE
TOP	0.35	—	50ohm	—	+/-10%
TOP/BOTTOM	0.27	0.2	—	90ohm	+/-10%



Project Flatburn_V5
Designer Luca Brighenti
Internal code -
Customer MIT

Date 29/07/25	Rev. 2	Rev. changes See Root Page	Kicad Version KiCad E.D.A. 9.0.0	Sheet 9/9
---------------	--------	----------------------------	----------------------------------	-----------