LPC11CXX User Manual

Chapter 18: Timer

- Page 333:
  - MAT0: match output
- Page 74:
  - SCK0 is the clock pin used in SSP0 peripheral (#1 of 2 SPI peripherals). DSR, DCD, and RI are related to UART.
  - The manual says “some input functions (SCK0, DSR, DCD, and RI) are multiplexed to several physical pins”
    - Means they’ve given you the option of using a few different external pins for these signals
  - IOCON_LOC registers are used to select the physical pin of the functions SCKO, DSR, DCD, and RI
  - The IOCON registers control the pins function and electrical characteristics
  - The SYSAHBCLKCTRL register enables the clocks to individual system and peripheral blocks
    - Pins 7 and 8 enable the clock for counter/timer 0 and 1 respectively
- Page 225:
  - The manual says “Use the IOCON_LOC register (see Section 7.4) to select a physical location for the SCK0 function in addition to selecting the function in the IOCON registers.”
    - There are IOCON registers for every pin on the IC. They control which peripheral is internally routed, and given control of, that pin. There are also IOCON_LOC registers for selecting where certain specific signals get routed to, like the CLK of SPI0
- Page 334
  - Match registers store a value
    - When the match register equals the timer counter, we can toggle a pin, set it to a logic low, set it to a logic high, or do nothing

Chapter 3: System Configuration

- The system configuration block controls oscillators, start logic, and clock generators
- Clock generation
  - There are 3 independent oscillators (system oscillator, internal RC oscillator, watchdog oscillator)
- The SYSAHBCLKCTRL register gates the system clock to peripherals and memories
- System AHB Clock Control Register
  - The AHBCLKCTRL enables the clocks to individual system and peripheral blocks

Chapter 7: I/O Configuration

- The IOCON registers control the function (GPIO or peripheral), the input mode, and the hysteresis of all PIOn_m pins. If a pin is used as an input for the ADC, an analog input mode can be selected
- Pin function:
  - The FUNC bits in the IOCON register can be set to GPIO (FUNC=000) or a peripheral function
  - The GPIOnDIR registers determine whether the pin is configured as an input or an output

        - The GPIOnDIR registers have no effect for peripheral functions (only GPIO)
- Pin mode:
    - The MODE bits in the IOCON register allow the selection of internal pull-up, internal pull-down, or repeater mode for each pin
    - Repeater mode:
        - Internal pull-up resistor is enabled if input is a logic HIGH. Internal pull-down resistor is enabled if input is a logic LOW
        - Pin retains the last known state if it is not driven by an external source (allows power savings from external source)
- Hysteresis
    - The input buffer of digital functions can be configured with hysteresis or as a plain buffer
- A/D mode
    - A/D mode can be selected in IOCON registers that control a pin with an analog function
- Open-drain mode
    - Pins configured as GPIO outputs can be configures to open-drain mode (disables the high-drive transistor)

Chapter 18:

- Configure the CT16B0/1 pins in the IOCONFIG register block
- Set bit 7 and 8 in the SYSAHBCLKCTRL register
    - Bit 7 enables the clock for 16-bit counter/timer 0
    - Bit 8 enables the clock for 16-bit counter/timer 1
- The capture signal may be useful for measuring wheel speed
    - A transition in the capture pin can load the capture register with the value in the counter/timer
- Configuring registers:
    - Set interrupt register (TMR16B0IR)
        - A bit must be set to a logic high to enable match interrupts
    - Set timer control register: TCR (TMR16B0TCR)
        - 1 bit enables the counter, the other bit resets the counter
        - CT[0]: enable
        - CT[1]: reset
    - Timer counter value is stored in Timer Counter (TMR16B0TC)
        - Timer counter is incremented when the prescale timer reaches its terminal count
    - Set prescale register (TMR16B0PR)
        - Specifies the maximum value of the prescale counter
    - Prescale counter register (TMR16B0PC)
        - Contains the prescale counter value
    - Set match control registers (TMR16B0MCR)
        - You can interrupt, reset, or stop on match
    - Set match registers (TMR16B0MR0)
        - Sets match value
    - Set capture control register (for wheel speed sensors)
        - Can capture value of timer on rising edge or falling edge.
        - Also have the option of triggering interrupt upon capture event
    - Capture register (CT16B0CR0) (for wheel speed sensors)
        - Register loaded with counter/timer value on capture event

    - Count Control Register (TMR16B0CTCR)
        - You can configure the processor to increase a counter when transitions occur on the capture pin
        - Used to select between timer and counter mode
        - If counter mode is selected, other registers specify the type of capture event (rising edge falling edge, either rising or falling) that increases the counter.

Chapter 25:

- Basic Configuration:
    - To use the ADC, you must set the function of one of the PIOn_m pins to AD
    - You must enable the clock for the ADC by setting bit 13 in the SYSAHBCLKCTRL register block
    - You must power the ADC through the PDRUNCFG register block
- A/D Control Registers:
    - SEL: selects which of the AD7:0 pins are to be sample and converted
    - CLKDIV: the APB clock (PCLK) is divided by CLKDIV + 1 to obtain the ADC clock, which should be less than or equal to 4.5MHz
    - You can select normal mode or burst mode
    - In burst mode, you can scan through several pins and measure the analog values
    - A/D conversion can be started by the program, or by an edge on one of the pins (including a match output)
    - Match outputs are controlled by a timer. If a counter reaches the value of the match register, the match output pin changes its voltage output.
- A/D Global Data Register
    - The value of the most recent A/D is stored in the A/D Global Data Register
    - The V_VREF register contains a binary fraction representing the voltage on the A/D pin divided by VDD
    - VDD: power (also known as VREF)
        - The maximum analog input must not exceed VDD
    - VSS: ground
    - Zero in the V_VREF field indicates that the voltage on the ADn pin was less than , equal to, or close to VSS
    - 0x3FF indicates that the voltage on the ADn pin was greater than, equal to, or close to VREF
- A/D Interrupt enable register
    - The A/D channels can generate an interrupt when conversion is complete
- A/D Data Registers
    - The result of A/D conversions are stored in A/D Data registers (there is one A/D data register for each analog input)
- A/D status register
    - Allows the checking of all A/D channels simultaneously

Questions:

- Page 410 says: “the CLKS field selects the number of bits of accuracy of the result in the LS bits of ADDR”
    - If you choose less bits of accuracy, do you only get the least significant bits?
    - Why would this be useful, aren’t the higher order bits more important

- Page 411 says: “The DONE bit is cleared when the register is read and the ADCR (AD control) is written”
    - What do they mean by: “when the ADCR is written”? Is it when the SEL, CLKDIV, BURST, etc. registers are written?
    - Aren’t these registers always written?
- Page 413 says: “The result register for an A/D channel that is generating an interrupt must be read in order to clean the corresponding DONE flag”
    - What result register are they talking about? Is it V_VREF in the Data Registers?
    - What does reading the register in order mean?

Chapter 28:

- Parts on the LPC1100C series do not support NMI (non-maskable interrupt)
- Processor Modes:
    - Thread mode: used to execute application software
    - Handler mode: used to handle exceptions. Processor returns to thread mode when it has finished all exception processing.
- Cortex Microcontroller Software Interface Standard (CMSIS)
    - CMSIS defines:
        - A common way to access peripheral registers
        - A common way to define exception vectors
        - The names of the registers of core peripherals
        - The core exception vectors

<u>Software Implementation:</u>

- Memory mapping is defined in chip.h
- To change values stored in registers, call functions in library
- Interrupt numbers (e.g CAN_IRQn) are defined in cmsis_11cxx.h
- Use (void) in C to indicate that a function takes no arguments
    - Source: http://stackoverflow.com/questions/42125/function-declaration-isnt-a-prototype

<u>Acronyms:</u>

- MATO: match output
- SCKO: serial clock (used to synchronize the transfer of data. It is driven by the master and received by the slave)
- DSR: data set ready
- PIO: programmed input/output (Method of transferring data between the CPU and a peripheral. Programmed I/O happens when software running on the CPU uses instructions that access I/O address space to perform data transfers to or from a peripheral.)
- AHB: AMBA high performance bus
    - Advanced Microcontroller Bus Architecture (AMBA) is an interconnect specification for the connection and management of functional blocks.
    - AHB is a bus for AMBA
- APB: advanced peripheral bus
- NVIC: nested vectored interrupt controller
- NMI: non-maskable interrupt
- ISR: interrupt service routine
- PDN: power distribution network