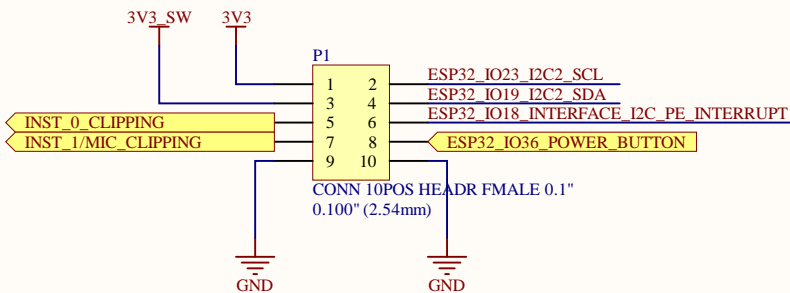
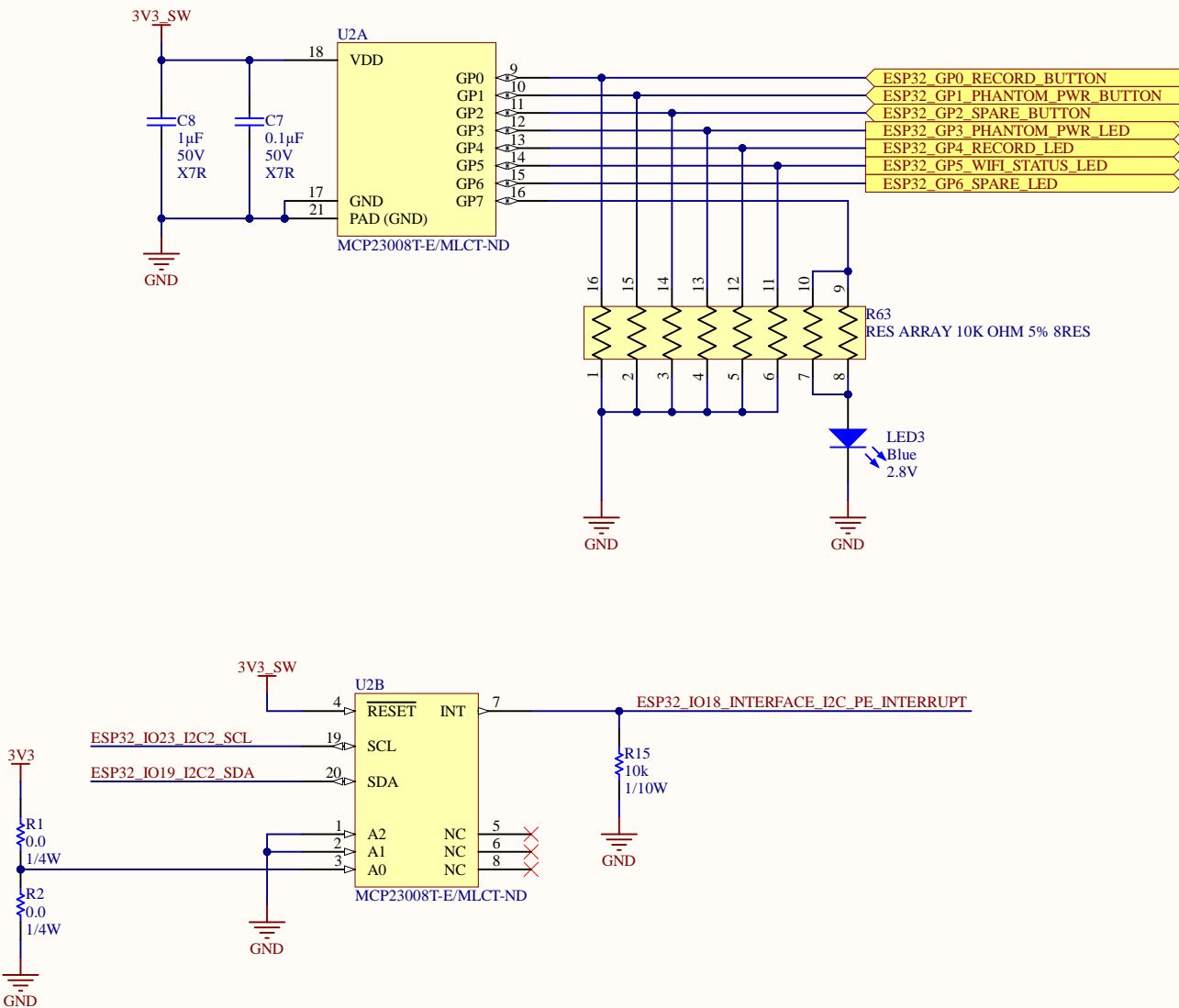


Connector



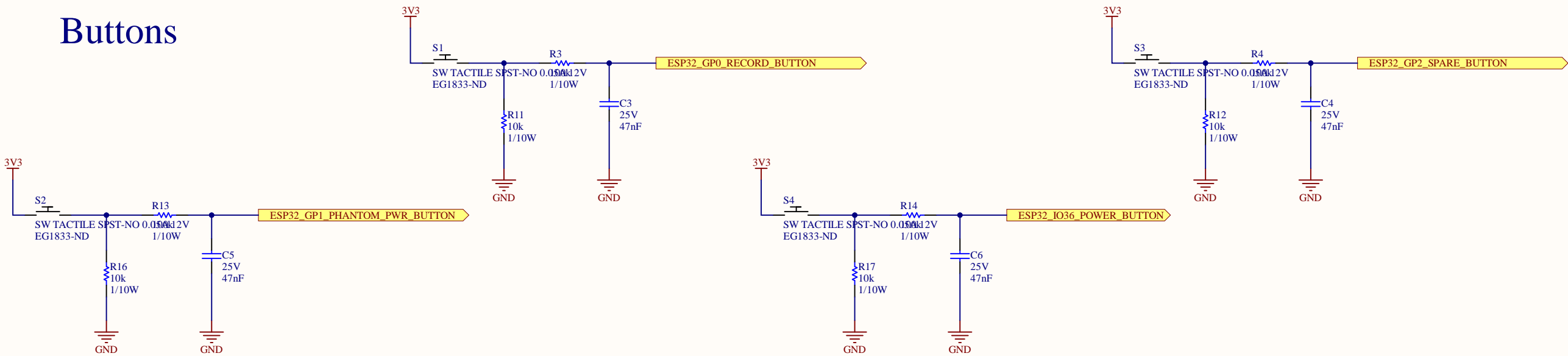
GPIO Expander



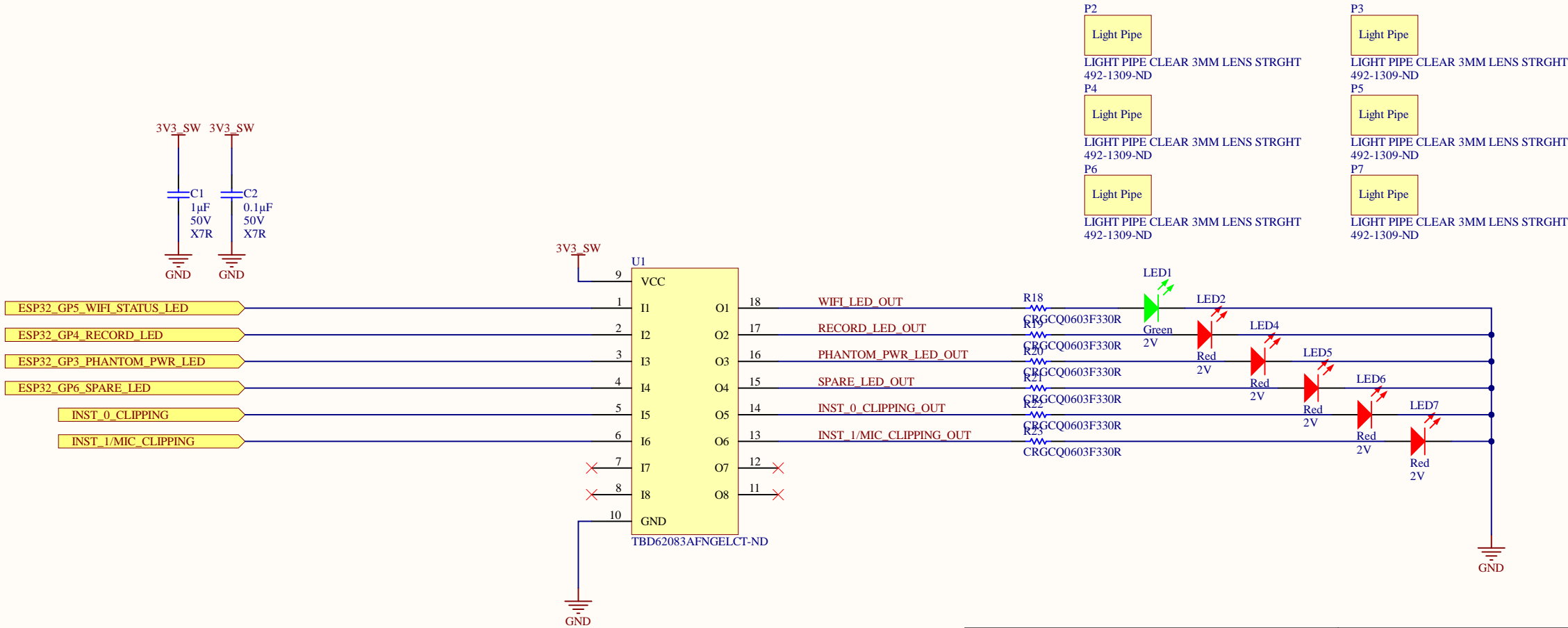
PROJECT	MIXR User Interface.PrjPcb		
DOCUMENT	Title		
PART NUMBER	VARIANT	[No Variations]	
DRAWN BY	Taiping Li	REVISION	1.0
LAST MODIFIED	2020-02-09	SHEET	14 OF 14



Buttons



LED Driver



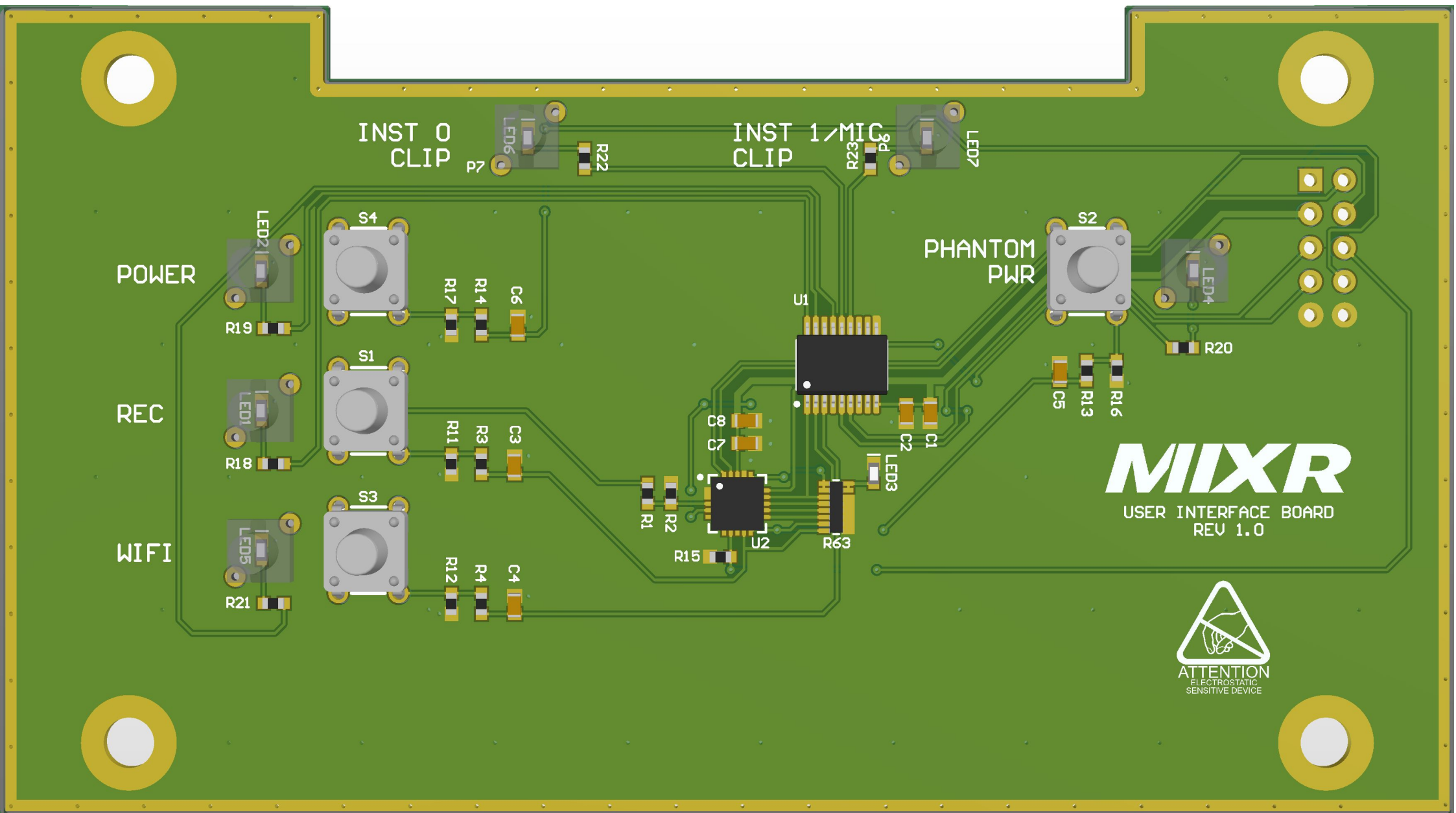
PROJECT		MIXR User Interface.PrjPcb	
DOCUMENT		*	
PART NUMBER		VARIANT	[No Variations]
DRAWN BY		REVISION	1.0
LAST MODIFIED		SHEET	* OF *



Bill of Materials	
Project:	MIXR User Interface.PrjPcb
Revision:	1.0
Project Lead:	Taiping Li
Generated On:	2020-02-09 9:09 PM
Production Quantity:	1
Currency	CAD
Total Parts Count:	46

# MIXR

[illegible]



INST 0  
CLIP

INST 1/MIC  
CLIP

POWER

REC

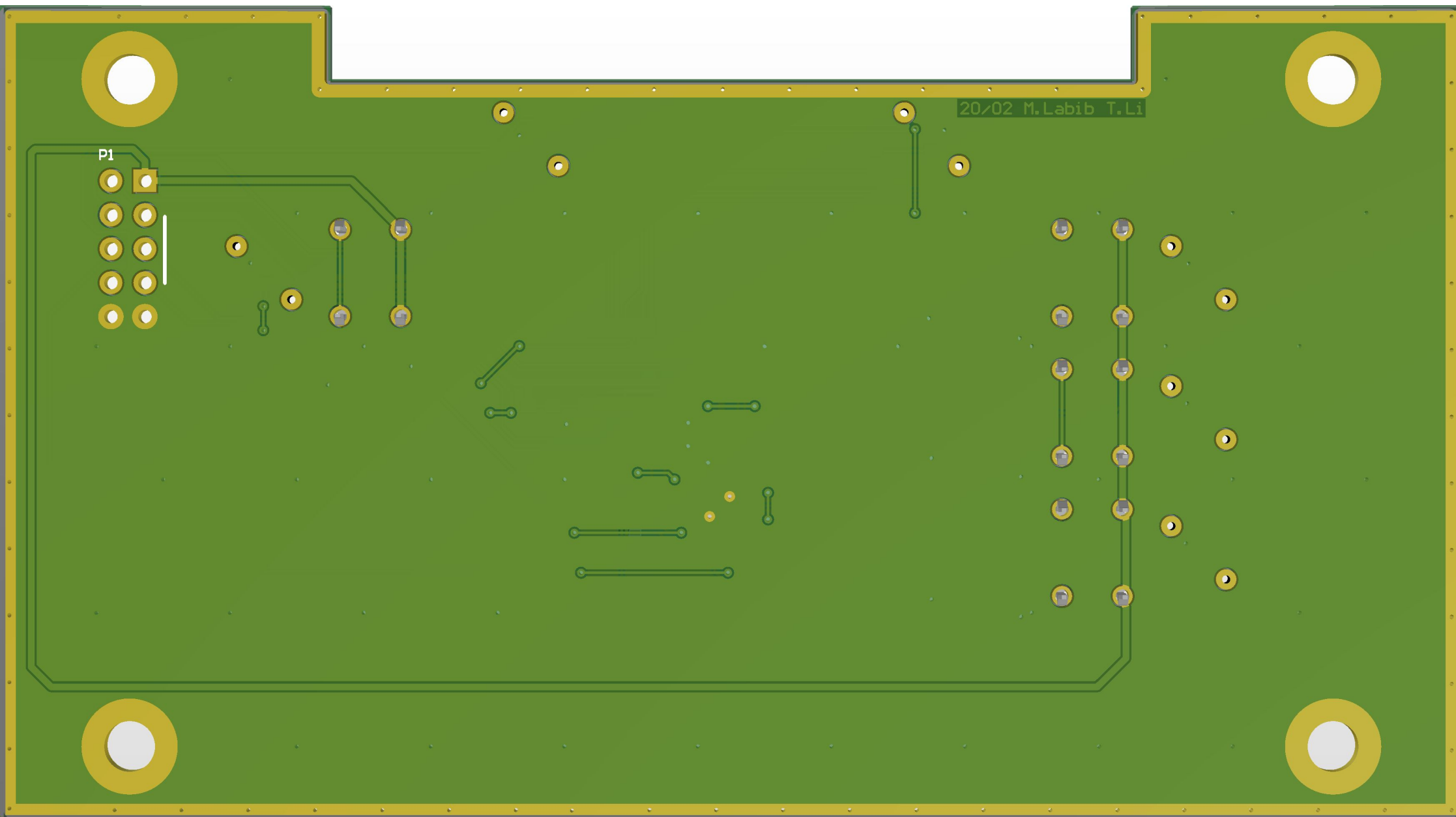
WIFI

PHANTOM  
PWR

**MIXR**

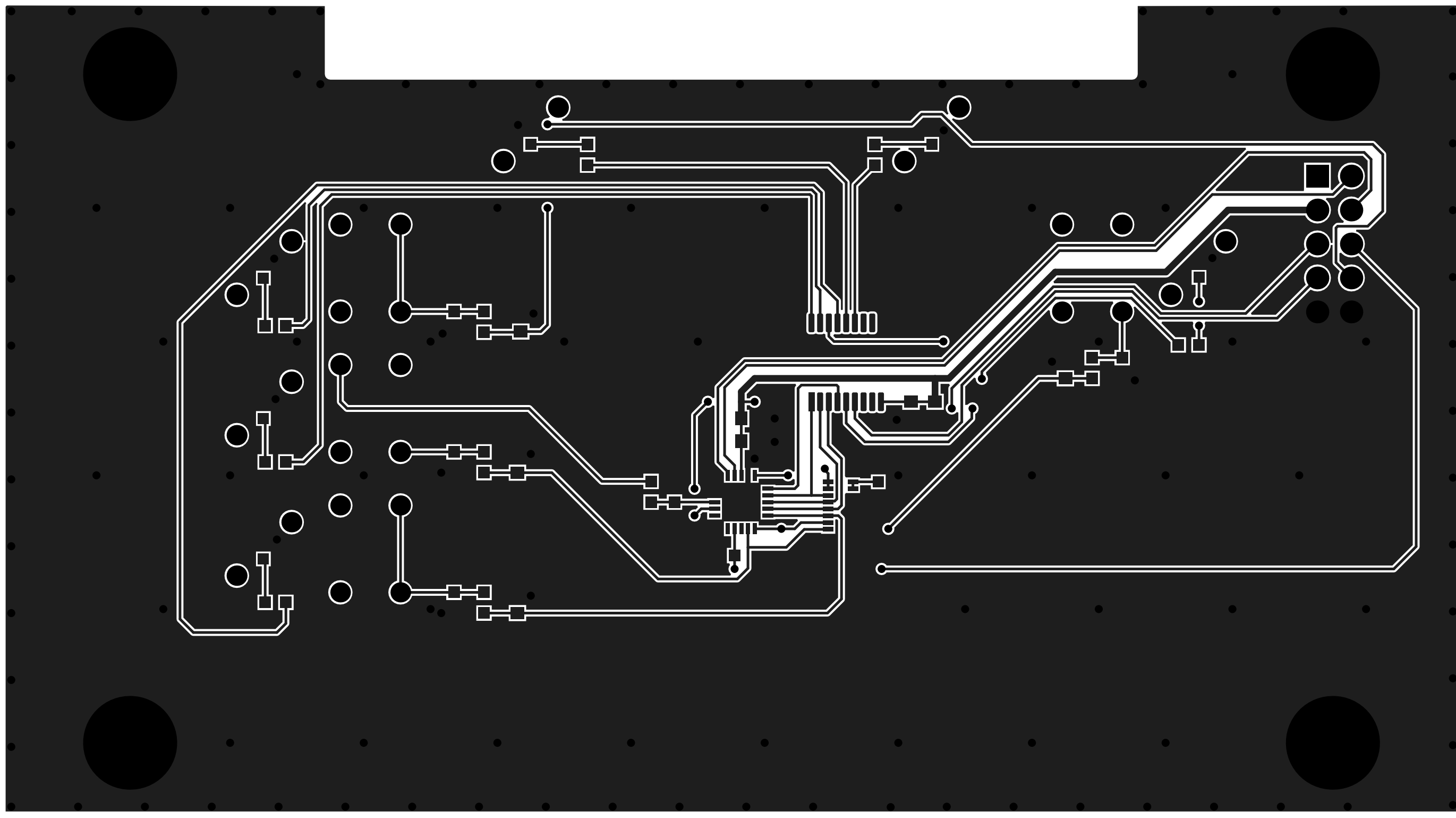
USER INTERFACE BOARD  
REV 1.0

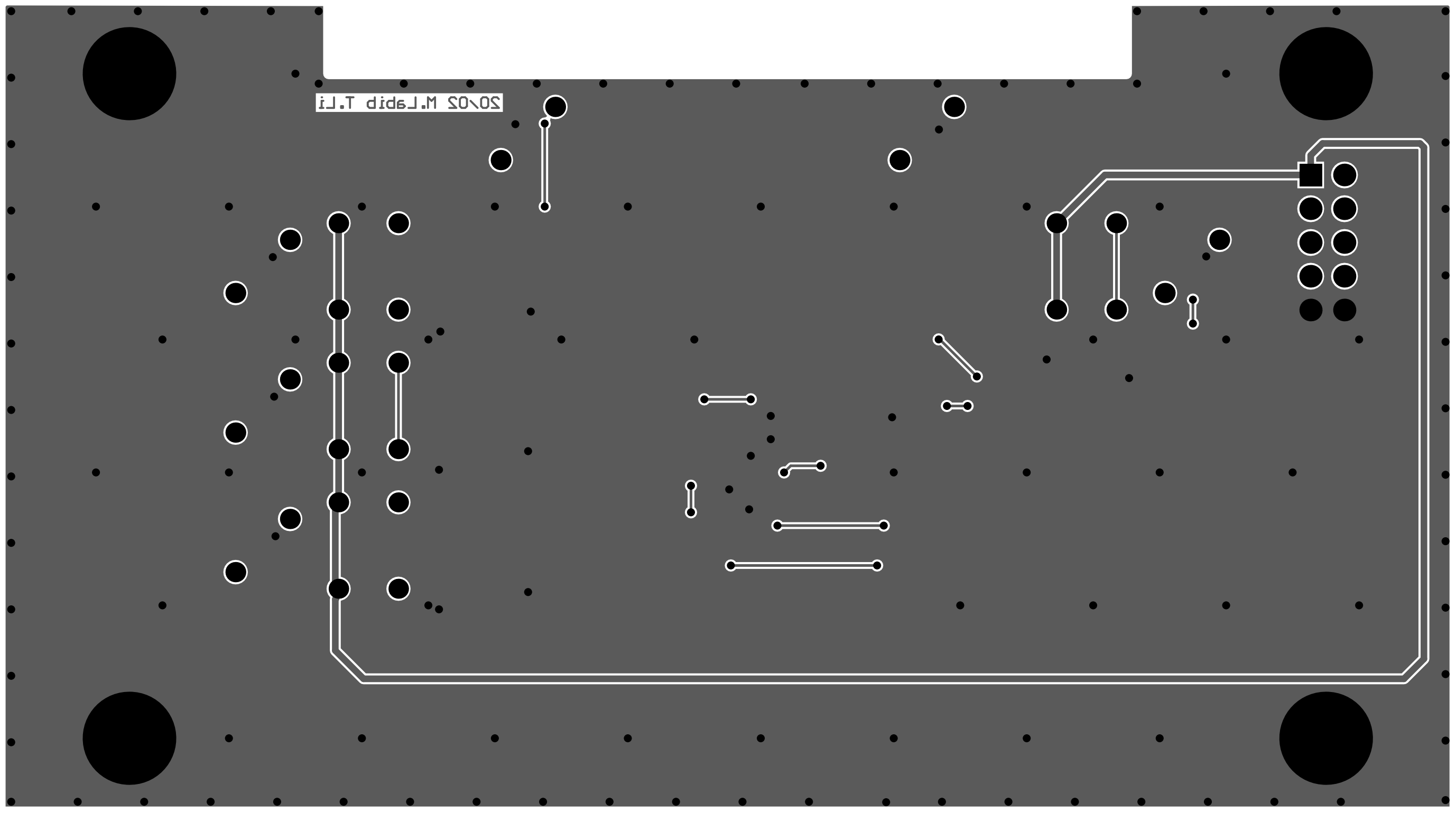




20/02 M.Labib T.Li

P1





iJ.T didsJ.M SO\OS

## Design Rules Verification Report

Filename : C:\Users\Taiping\Documents\FYDP\mixr-hardware\MIXR User Interface\MIXR Us

Warnings 0  
Rule Violations 40

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.152mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ( All )	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.154mm) (Max=2.54mm) (Preferred=0.2mm) (All)	0
Power Plane Connect Rule(Relief Connect )(Expansion=0.5mm) (Conductor Width=0.2mm) (Air Gap=0.2mm)	0
Power Plane Connect Rule(Relief Connect )(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Minimum Annular Ring (Minimum=0.12mm) (All)	0
Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.1mm) (Disabled)(All),(All)	0
Silk To Solder Mask (Clearance=0.178mm) (IsPad),(All)	34
Silk to Silk (Clearance=0.254mm) (All),(All)	6
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (All)	0
Height Constraint (Min=0mm) (Max=30mm) (Preferred=12.7mm) (All)	0
Total	40

Silk To Solder Mask (Clearance=0.178mm) (IsPad),(All)	
Silk To Solder Mask Clearance Constraint: (0.093mm < 0.178mm) Between Pad R23-2(64.625mm,49.527mm) on Top Layer And Text "INST 1/MIC	

CLIP" (54.25mm,48.025mm) on Top Overlay [Top Overlay] to [Top Solder] clearance [0.093mm]	



**Silk To Solder Mask (Clearance=0.178mm) (IsPad), (All)**

Silk To Solder Mask Clearance Constraint: (0.177mm < 0.178mm) Between Pad S1-1(24.625mm,26.527mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.157mm < 0.178mm) Between Pad S1-1(24.625mm,26.527mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad S1-1(24.625mm,33.027mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.157mm < 0.178mm) Between Pad S1-1(24.625mm,33.027mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.131mm < 0.178mm) Between Pad S1-2(29.125mm,26.527mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad S1-2(29.125mm,26.527mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.178mm) Between Pad S1-2(29.125mm,33.027mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad S1-2(29.125mm,33.027mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.177mm < 0.178mm) Between Pad S2-1(78.625mm,37.027mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.157mm < 0.178mm) Between Pad S2-1(78.625mm,37.027mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad S2-1(78.625mm,43.527mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.157mm < 0.178mm) Between Pad S2-1(78.625mm,43.527mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.131mm < 0.178mm) Between Pad S2-2(83.125mm,37.027mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad S2-2(83.125mm,37.027mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.178mm) Between Pad S2-2(83.125mm,43.527mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad S2-2(83.125mm,43.527mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.177mm < 0.178mm) Between Pad S3-1(24.625mm,16.027mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.157mm < 0.178mm) Between Pad S3-1(24.625mm,16.027mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad S3-1(24.625mm,22.527mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.157mm < 0.178mm) Between Pad S3-1(24.625mm,22.527mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.131mm < 0.178mm) Between Pad S3-2(29.125mm,16.027mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad S3-2(29.125mm,16.027mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.178mm) Between Pad S3-2(29.125mm,22.527mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad S3-2(29.125mm,22.527mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.177mm < 0.178mm) Between Pad S4-1(24.625mm,37.027mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.157mm < 0.178mm) Between Pad S4-1(24.625mm,37.027mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad S4-1(24.625mm,43.527mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.157mm < 0.178mm) Between Pad S4-1(24.625mm,43.527mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.131mm < 0.178mm) Between Pad S4-2(29.125mm,37.027mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad S4-2(29.125mm,37.027mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.178mm) Between Pad S4-2(29.125mm,43.527mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad S4-2(29.125mm,43.527mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U2-10(55.625mm,20.777mm) on Top Layer And Text "U2"

**Silk to Silk (Clearance=0.254mm) (All),(All)**

Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "INST 1/MIC
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**CLIP" (54.25mm,48.025mm) on Top Overlay And Text "P6" (66.025mm,49.377mm) on Top Overlay Silk Text to Silk Clearan****Silk to Silk (Clearance=0.254mm) (All),(All)**

Silk To Silk Clearance Constraint: (0.068mm < 0.254mm) Between Text "INST 1/MIC
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**CLIP" (54.25mm,48.025mm) on Top Overlay And Text "R23" (63.625mm,48.052mm) on Top Overlay Silk Text to Silk Cleara****Silk to Silk (Clearance=0.254mm) (All),(All)**

Silk To Silk Clearance Constraint: (0.162mm < 0.254mm) Between Text "R63" (61.175mm,19.477mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.248mm < 0.254mm) Between Text "S2" (80.375mm,43.977mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.248mm < 0.254mm) Between Text "S3" (26.275mm,22.977mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.248mm < 0.254mm) Between Text "S4" (26.275mm,43.977mm) on Top Overlay And Track