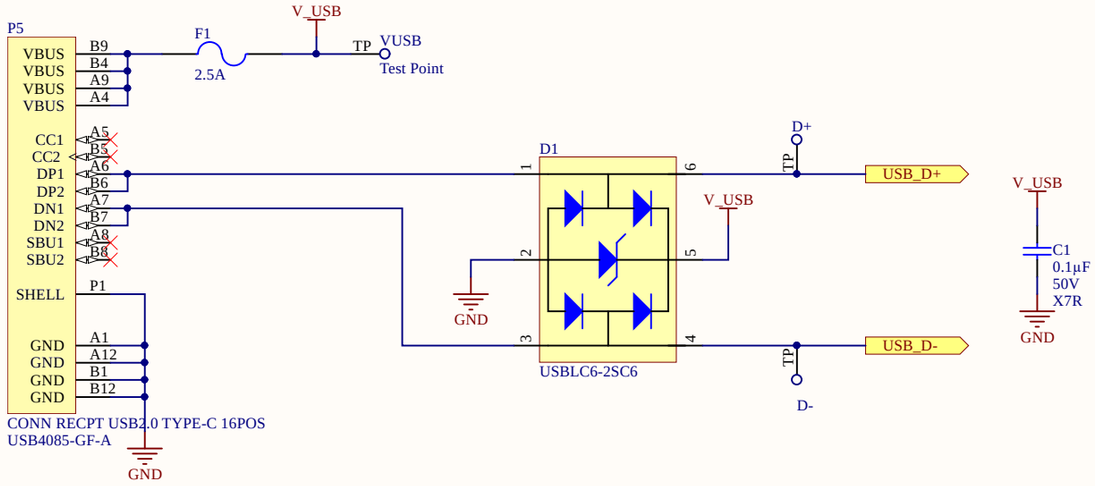
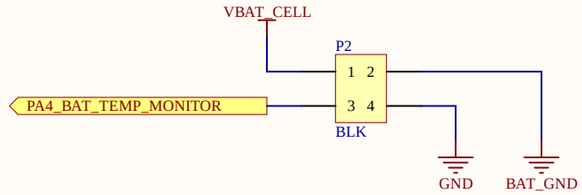
PROJECT	MIXR Power.PrjPcb				
DOCUMENT	Title				
PART NUMBER		VARIANT	[No Variations]		
DRAWN BY	Taiping Li	REVISION	1.0		
LAST MODIFIED	2019-07-12	SHEET	1 OF 5		

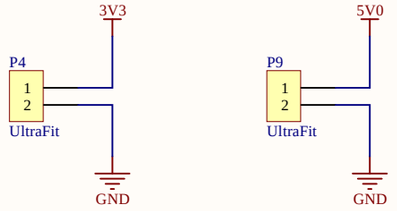
USB-C Connector



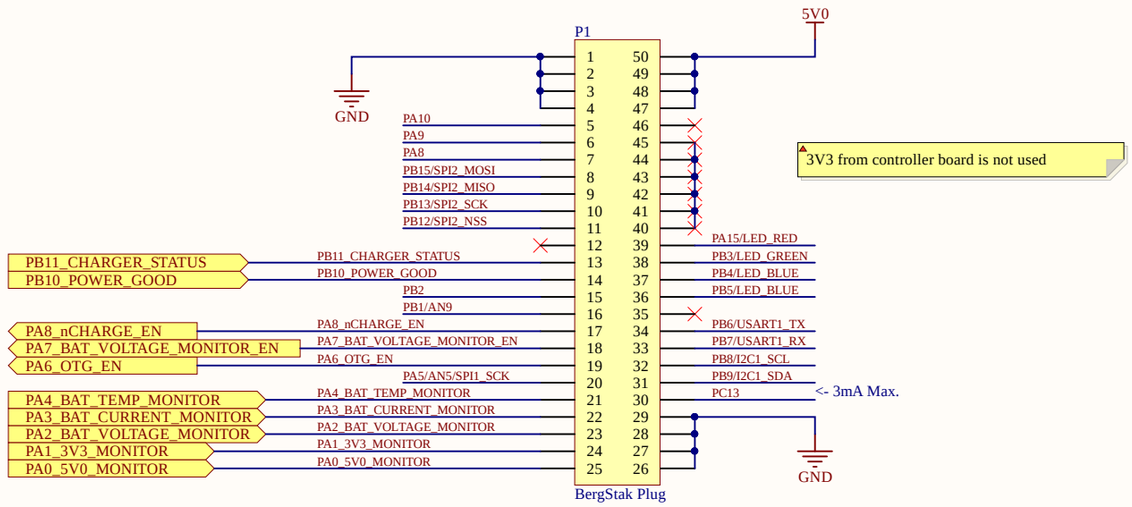
1s Li-Ion Input



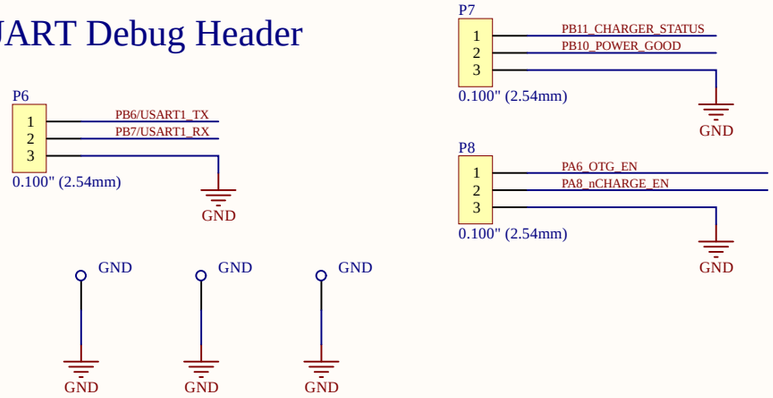
Regulator Outputs



Controller Board

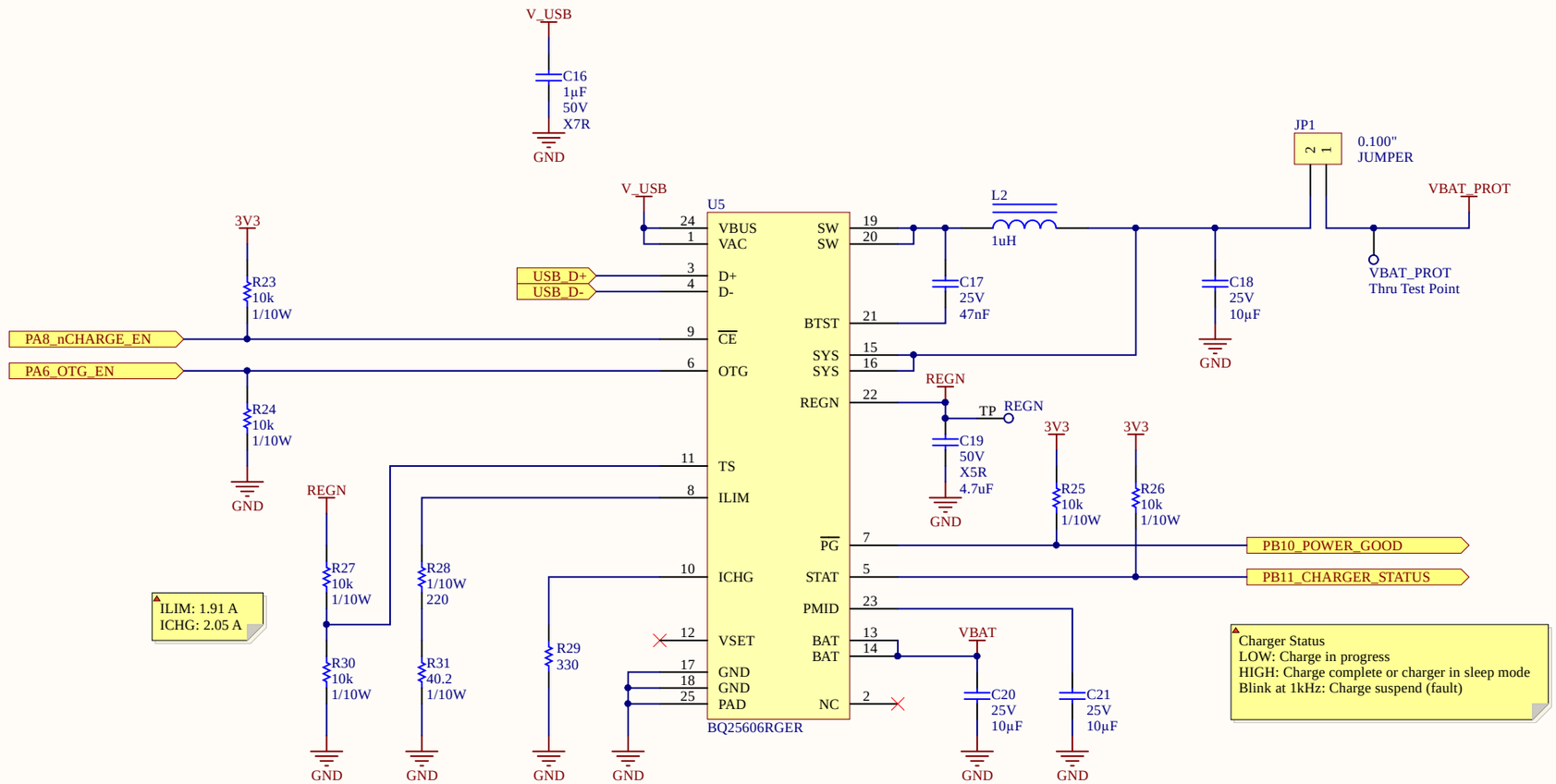


UART Debug Header



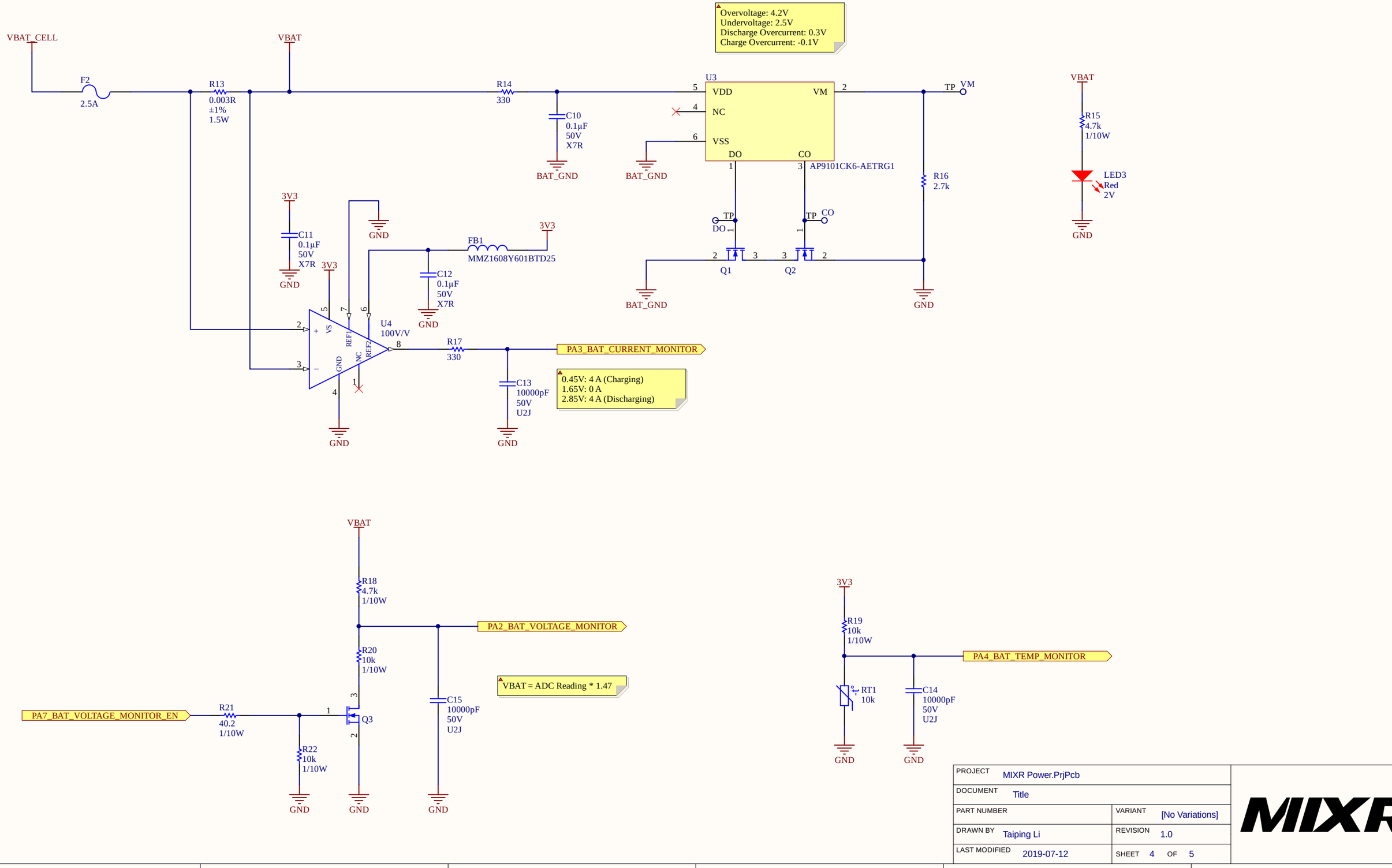
PROJECT	MIXR Power.PrjPcb		
DOCUMENT	Title		
PART NUMBER		VARIANT	[No Variations]
DRAWN BY	Taiping Li	REVISION	1.0
LAST MODIFIED	2019-07-12	SHEET	2 OF 5

MIXR



PROJECT	MIXR Power.PrjPcb
DOCUMENT	Title
PART NUMBER	VARIANT [No Variations]
DRAWN BY Taiping Li	REVISION 1.0
LAST MODIFIED 2019-07-12	SHEET 3 OF 5

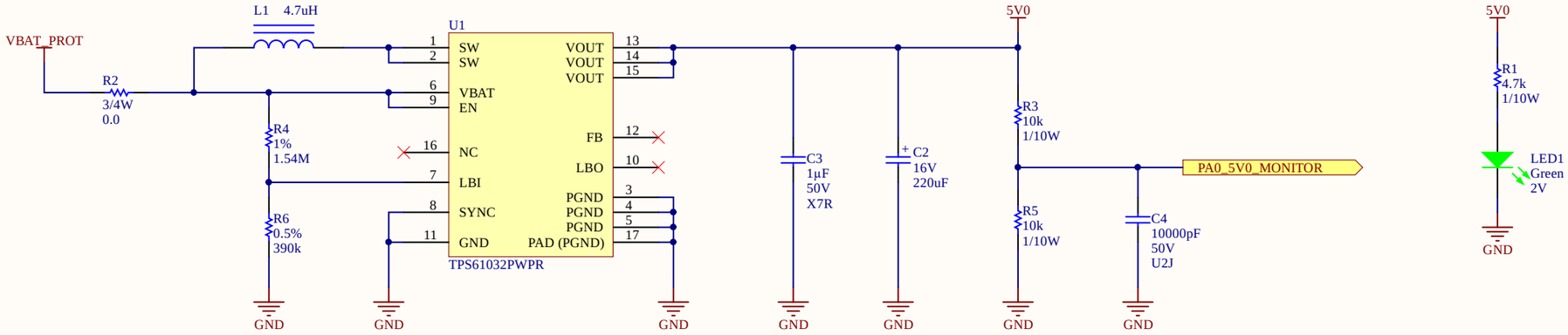
MIXR



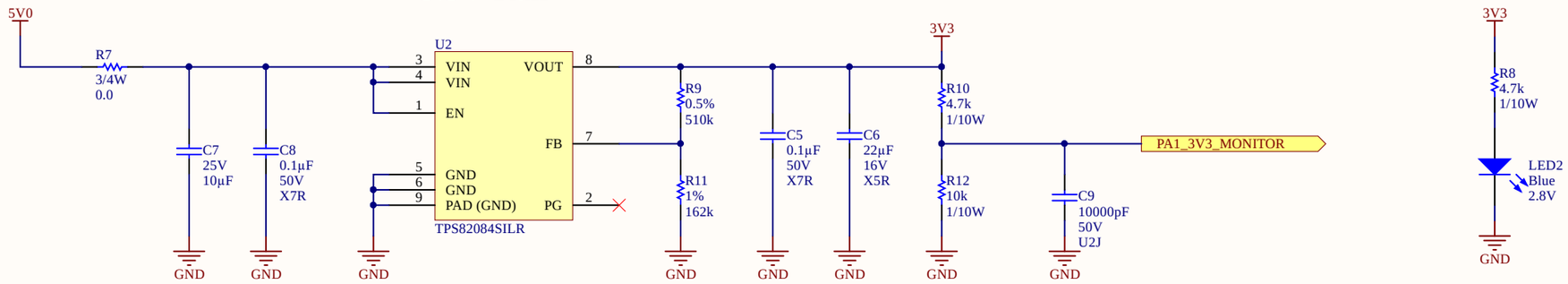
PROJECT	MIXR Power.PrjPcb
DOCUMENT	Title
PART NUMBER	VARIANT [No Variations]
DRAWN BY	Taiping Li
REVISION	1.0
LAST MODIFIED	2019-07-12
SHEET	4 OF 5

MIXR

5V Rail



3.3V Rail



PROJECT	MIXR Power.PrjPcb
DOCUMENT	Title
PART NUMBER	VARIANT [No Variations]
DRAWN BY Taiping Li	REVISION 1.0
LAST MODIFIED 2019-07-12	SHEET 5 OF 5

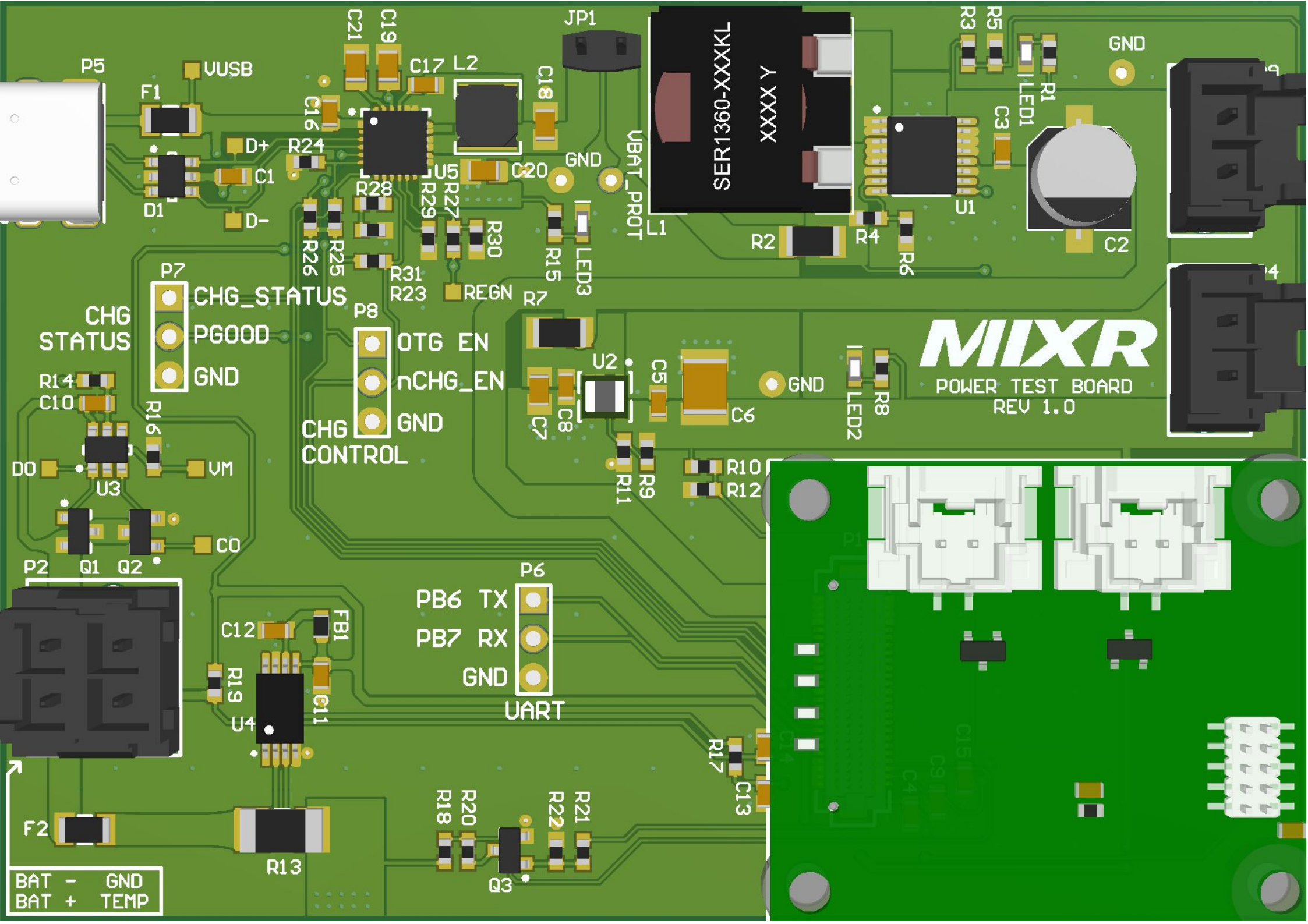
MIXR

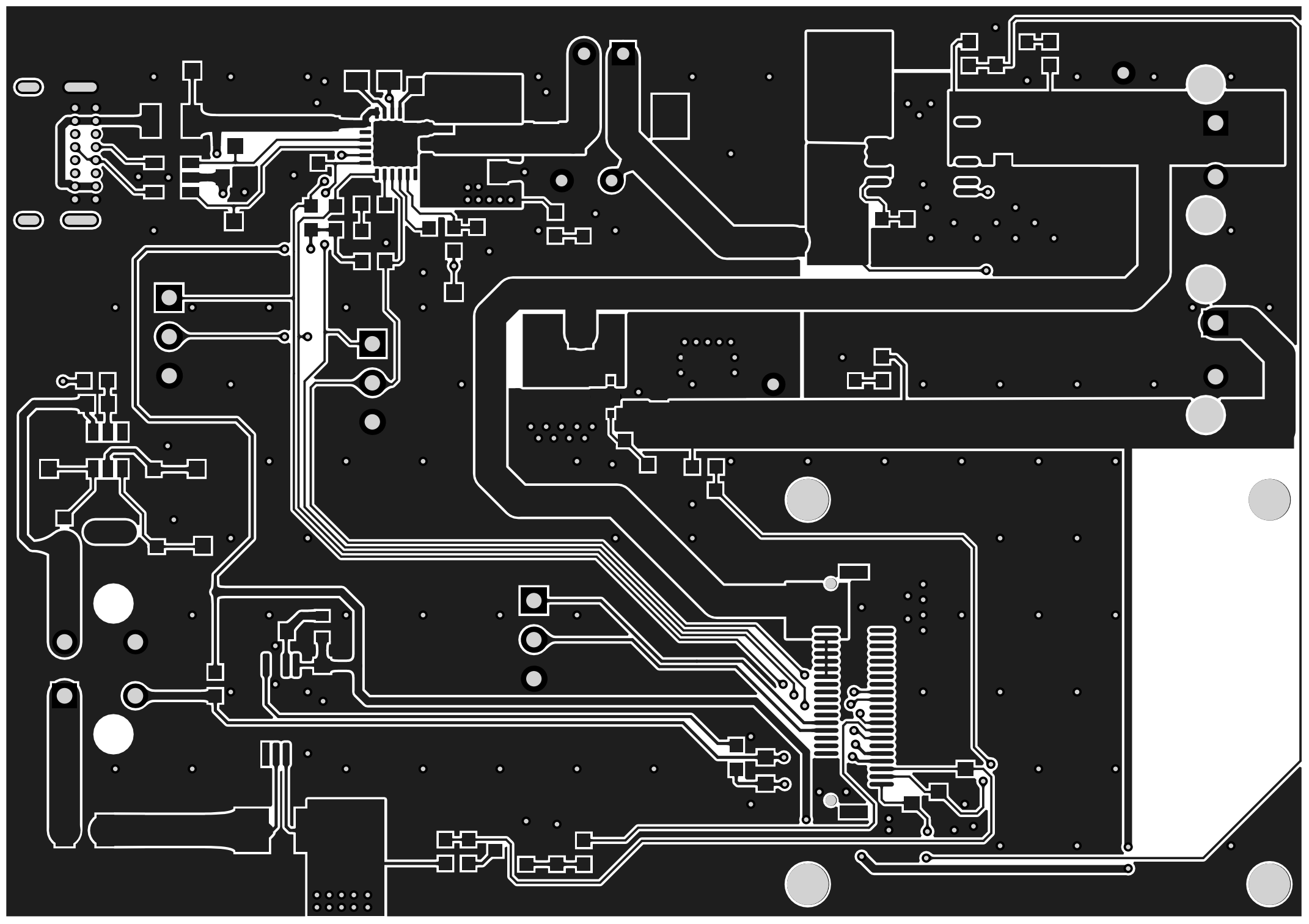
Bill of Materials

Project:	MIXR Power.PrjPcb
Revision:	1
Project Lead:	Taiping Li
Generated On:	2019-07-12 20:15
Production Quantity:	1
Currency	CAD
Total Parts Count:	83

MIXR

LibRef	Designator	Manufacturer 1	Manufacturer Part Number 1	Supplier 1	Supplier Part Number 1	Supplier Unit Price 1	Quantity	Supplier Subtotal 1
CAP CER 0.1UF 50V 10% X7R 0603	C1, C5, C8, C10, C11, C12	Kyocera AVX	06035C-104KAT2A	Digi-Key	478-5052-1-ND	0.20857	6	$ 1.25
CAP ALUM 220UF 20% 16V SMD	C2	Panasonic	EEE-1CA221XAP	Digi-Key	PCE4583CT-ND	0.59964	1	$ 0.60
CAP CER 1UF 50V 10% X7R 0603	C3, C16	Taiyo Yuden	UMK107AB7105KA-T	Digi-Key	587-3247-1-ND	0.365	2	$ 0.73
CAP CER 10nF 50V 5% X7R 0603	C4, C9, C13, C14, C15	KEMET	C0603C103J5JACTU	Digi-Key	399-13384-1-ND	0.46929	5	$ 2.35
CAP CER 22UF 16V ±20% X5R 1210	C6	Murata	GRM32ER61C226ME20L	Digi-Key	490-1881-1-ND	2.31	1	$ 2.31
CAP CER 10uF 25V 10% X5R 0805	C7, C18, C20, C21	Murata	GRM21BR61E106KA73L	Digi-Key	490-5523-1-ND	0.56054	4	$ 2.24
CAP CER 0.047UF 10% 25V X7R 0603	C17	KEMET	C0603C473K3RACTU	Digi-Key	399-7931-1-ND	0.14339	1	$ 0.14
CAP CER 4.7UF 50V 10% X5R 0805	C19	Murata	GRT21BR61H475ME13L	Digi-Key	490-12395-1-ND	0.62571	1	$ 0.63
DIODE TVS 5.25V 17V SOT23-6	D1	STMicroelectronics	USBLC6-2SC6	Digi-Key	497-5235-1-ND	0.61268	1	$ 0.61
FUSE 2.5A 32VDC 1206	F1, F2	Littelfuse	046602.5NRHF	Digi-Key	F6143CT-ND	1.09	2	$ 2.19
FB 600 OHM 1LN 0603	FB1	TDK	MMZ1608Y601BTD25	Digi-Key	445-172850-1-ND	0.13036	1	$ 0.13
Thru Test Point	GND, VBAT_PROT						4	
CONN 2POS JUMPER 0.1"	JP1	Omron	XG8T-0231	Digi-Key	XG8T-0231-ND	0.24768	1	$ 0.25
IND 4.7uH 9.4A 10% SMD	L1	Coilcraft	SER1360-472KLB	Mouser	994-SER1360-472KLB	2.7	1	$ 2.70
IND 1uH 3.8A 25 MOHM SMD	L2	Vishay Dale	IFSC1515AHER1R0M01	Digi-Key	541-1403-1-ND	0.83428	1	$ 0.83
LED GREEN CLEAR 2V 0603	LED1	Wurth Electronics	150060VS75000	Digi-Key	732-4980-1-ND	0.1825	1	$ 0.18
LED BLUE CLEAR 2.8V 0603	LED2	Vishay Lite-On	LTST-C193TBKT-5A	Digi-Key	160-1827-1-ND	0.61268	1	$ 0.61
LED RED CLEAR 2V 0603	LED3	Wurth Electronics	150060RS75000	Digi-Key	732-4978-1-ND	0.1825	1	$ 0.18
CONN 50POS Bergstak Plug 0.02"	P1	Amphenol FCI	10132797-055100LF	Digi-Key	609-5226-1-ND	1.82	1	$ 1.82
CONN 4POS 2 ROW ULTRA-FIT 0.138"	P2	Molex	1722991104	Digi-Key	WM11777-ND	1.17	1	$ 1.17
CONN 2POS ULTRA-FIT 0.138"	P4, P9	Molex	1722871102	Digi-Key	WM11701-ND	1.02	2	$ 2.03
CONN RECPT USB2.0 TYPE-C 16POS	P5	Global Connector Technology	USB4085-GF-A	Digi-Key	073-USB4085-GF-ACT-ND		1	
CONN 3POS HEADR MALE 0.1"	P6, P7, P8	Wurth Electronics	61300311121	Digi-Key	732-5316-ND	0.16946	3	$ 0.51
MOSFET N-CH 30V 6.2A 0.9W SOT-23	Q1, Q2, Q3	Diodes	DMN3023L-7	Digi-Key	DMN3023L-7DICT-ND	0.46929	3	$ 1.41
RES 4.7K OHM 1% 1/10W 0603	R1, R8, R10, R15, R18	Yageo Phycomp	RC0603FR-074K7L	Digi-Key	311-4.70KHRCT-ND	0.13036	5	$ 0.65
RES 0.0 OHM 3/4W 1206	R2, R7	Stackpole Electronics	HCJ1206ZT0R00	Digi-Key	HCJ1206ZT0R00CT-ND	0.71696	2	$ 1.43
RES 10K OHM 1% 1/10W 0603	, R12, R19, R20, R22, R23, R24, R25, R26, R2	Yageo Phycomp	RC0603FR-0710KL	Digi-Key	311-10.0KHRCT-ND	0.03129	12	$ 0.38
RES 1.54M OHM 1% 1/10W 0603	R4	Vishay	CRCW06031M54FKEA	Digi-Key	541-1.54MHCT-ND	0.13036	1	$ 0.13
RES 390K OHM 1% 1/10W 0603	R6	Yageo	RT0603DRE07390KL	Digi-Key	311-2555-1-ND	0.16946	1	$ 0.17
RES 510K OHM 0.5% 1/10W 0603	R9	Yageo	RT0603DRE07510KL	Digi-Key	311-2610-1-ND	0.16946	1	$ 0.17
RES 162K OHM 1% 1/10W 0603	R11	Yageo	RC0603FR-07162KL	Digi-Key	311-162KHRCT-ND	0.13036	1	$ 0.13
RES 0.003 OHM 1% 1.5W 2010	R13	Stackpole Electronics	CSNL2010FT3L00	Digi-Key	CSNL2010FT3L00CT-ND	0.88643	1	$ 0.89
RES 330 OHM 1% 1/10W 0603	R14, R17, R29	TE Connectivity	CRGCQ0603F330R	Digi-Key	A129682CT-ND	0.13036	3	$ 0.39
RES 2.7K OHM 1% 1/10W 0603	R16	TE Connectivity	CRGCQ0603F2K7	Digi-Key	A129693CT-ND	0.13036	1	$ 0.13
RES 40.2 OHM 0.5% 1/10W 0603	R21, R31	Yageo	RT0603DRE0740R2L	Digi-Key	311-2576-1-ND	0.15643	2	$ 0.31
RES 220 OHM 1% 1/10W 0603	R28	Yageo Phycomp	RC0603FR-07220RL	Digi-Key	311-220HRCT-ND	0.13036	1	$ 0.13
NTC THERMISTORS 10K 0603 SMD	RT1	Murata	NCU18XH103F60RB	Digi-Key	490-16279-2-ND		1	
IC REG BOOST 5V 3.6A 16-TSSOP	U1	Texas Instruments	TPS61032PWPR	Digi-Key	296-14418-1-ND	3.6	1	$ 3.60
IC DCDC 0.8-6V 2A 8-uSIP	U2	Texas Instruments	TPS82084SILR	Digi-Key	296-46279-1-ND	4.07	1	$ 4.07
IC BATT PROT LI-ION 1-CELL SOT26	U3	Diodes	AP9101CK6-AETRG1	Digi-Key	9101CK6-AETRG1DICT-	0.58661	1	$ 0.59
IC CURRENT AMPLIFIER INA240 8-TSSOP	U4	Texas Instruments	INA240A3PWR	Digi-Key	296-45090-1-ND	3.45	1	$ 3.45
IC BATT CHG LI-ION 1 CELL 24-VQFN	U5	Texas Instruments	BQ25606RGER	Digi-Key	296-47743-1-ND	3.6	1	$ 3.60
							Total:	$ 45.09


P5
VUSB
F1
D+
D-
D1
C1
R24
C21
C19
C17
L2
C16
C18
U5
R28
R29
R27
R30
R26
R25
R31
R23
REGN
C20
GND
JP1
VBAT_PROT
L1
SER1360-XXXKL
XXXX Y
R3
R5
LED1
R1
GND
C3
U1
R2
R4
R6
C2
P7
CHG_STATUS
PGOOD
GND
CHG
STATUS
P8
OTG EN
nCHG_EN
GND
CHG
CONTROL
R15
LED3
R7
U2
C7
C8
C5
C6
GND
LED2
R8
MIXR
POWER TEST BOARD
REV 1.0
R14
C10
R16
DO
VM
U3
CO
P2
Q1
Q2
R11
R9
R10
R12
P6
PB6 TX
PB7 RX
GND
UART
C12
FB1
R19
C11
U4
R17
C13
F2
R13
R18
R20
R22
R21
Q3
BAT - GND
BAT + TEMP



T.LI 19\07

Design Rules Verification Report

Filename : C:\Users\Taiping\Documents\FYDP\mixr-hardware\MIXR Regulators\MIXR Pow

Warnings 0
Rule Violations 181

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.152mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.15mm) (Max=3mm) (Preferred=0.15mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Minimum Annular Ring (Minimum=0.05mm) (All)	0
Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.3mm) (All),(All)	93
Silk To Solder Mask (Clearance=0.178mm) (IsPad),(All)	56
Silk to Silk (Clearance=0.254mm) (All),(All)	16
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (All)	16
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	181

Minimum Solder Mask Sliver (Gap=0.3mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C10-1(7.005mm,33.729mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C1-1(14.5mm,48.45mm) on Top Layer And Pad C1-2(15.85mm,48.45mm) on
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C11-1(20.95mm,16.7mm) on Top Layer And Pad C11-2(20.95mm,15.35mm) on
Minimum Solder Mask Sliver Constraint: (0.022mm < 0.3mm) Between Pad C11-2(20.95mm,15.35mm) on Top Layer And Via (21mm,14.4mm) from Top
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C12-1(18.65mm,18.95mm) on Top Layer And Pad C12-2(17.3mm,18.95mm) on
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C13-1(49.75mm,9.05mm) on Top Layer And Pad C13-2(49.75mm,7.7mm) on
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C14-1(49.75mm,10.75mm) on Top Layer And Pad C14-2(49.75mm,12.1mm) on
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C15-1(62.75mm,10mm) on Top Layer And Pad C15-2(62.75mm,8.65mm) on
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C16-1(21.5mm,51.9mm) on Top Layer And Pad C16-2(21.5mm,53.25mm) on
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C17-1(28.35mm,54.4mm) on Top Layer And Pad C17-2(27mm,54.4mm) on Top
Minimum Solder Mask Sliver Constraint: (0.272mm < 0.3mm) Between Pad C18-2(35.5mm,52.65mm) on Top Layer And Via (35.5mm,54mm) from Top
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C3-1(65.2mm,50.8mm) on Top Layer And Pad C3-2(65.2mm,49.45mm) on Top
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C4-1(59.25mm,7.75mm) on Top Layer And Pad C4-2(59.25mm,6.4mm) on Top
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C5-1(42.85mm,33.075mm) on Top Layer And Pad C5-2(42.85mm,34.425mm)
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C8-1(36.85mm,35.5mm) on Top Layer And Pad C8-2(36.85mm,34.15mm) on
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C9-1(61mm,8.5mm) on Top Layer And Pad C9-2(61mm,7.15mm) on Top Layer
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad D1-1(10mm,49.4mm) on Top Layer And Pad D1-2(10mm,48.45mm) on Top
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad D1-2(10mm,48.45mm) on Top Layer And Pad D1-3(10mm,47.5mm) on Top
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad D1-4(12.4mm,47.5mm) on Top Layer And Pad D1-5(12.4mm,48.45mm) on Top
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad D1-5(12.4mm,48.45mm) on Top Layer And Pad D1-6(12.4mm,49.4mm) on Top
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.3mm) Between Pad P1-(54mm,22.05mm) on Multi-Layer And Pad P1-(55.5mm,22.8mm) on Top
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.3mm) Between Pad P1-(54mm,7.95mm) on Multi-Layer And Pad P1-(55.5mm,7.2mm) on Top Layer
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad Q2-2(10.2mm,26.25mm) on Top Layer And Via (11.3mm,26.2mm) from Top
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad Q3-2(34.2mm,5.6mm) on Top Layer And Via (34.2mm,6.6mm) from Top Layer
Minimum Solder Mask Sliver Constraint: (0.172mm < 0.3mm) Between Pad R2-2(54.2mm,44.25mm) on Top Layer And Pad R4-1(55.75mm,45.75mm) on
Minimum Solder Mask Sliver Constraint: (0.122mm < 0.3mm) Between Pad R22-2(36.2mm,5.35mm) on Top Layer And Via (36.2mm,6.4mm) from Top
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad U2-1(40.35mm,35.275mm) on Top Layer And Pad U2-2(39.7mm,35.275mm) on
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad U2-1(40.35mm,35.275mm) on Top Layer And Pad U2-9(39.375mm,34.175mm)
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad U2-2(39.7mm,35.275mm) on Top Layer And Pad U2-3(39.05mm,35.275mm) on
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad U2-2(39.7mm,35.275mm) on Top Layer And Pad U2-9(39.375mm,34.175mm)
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad U2-3(39.05mm,35.275mm) on Top Layer And Pad U2-4(38.4mm,35.275mm) on
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad U2-3(39.05mm,35.275mm) on Top Layer And Pad U2-9(39.375mm,34.175mm)
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad U2-4(38.4mm,35.275mm) on Top Layer And Pad U2-9(39.375mm,34.175mm)
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad U2-5(38.4mm,33.075mm) on Top Layer And Pad U2-6(39.05mm,33.075mm) on
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad U2-5(38.4mm,33.075mm) on Top Layer And Pad U2-9(39.375mm,34.175mm)
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad U2-6(39.05mm,33.075mm) on Top Layer And Pad U2-7(39.7mm,33.075mm) on
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad U2-6(39.05mm,33.075mm) on Top Layer And Pad U2-9(39.375mm,34.175mm)
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad U2-7(39.7mm,33.075mm) on Top Layer And Pad U2-8(40.35mm,33.075mm) on
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad U2-7(39.7mm,33.075mm) on Top Layer And Pad U2-9(39.375mm,34.175mm)
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad U2-8(40.35mm,33.075mm) on Top Layer And Pad U2-9(39.375mm,34.175mm)
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad U3-1(6.05mm,29.5mm) on Top Layer And Pad U3-2(7mm,29.5mm) on Top
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad U3-2(7mm,29.5mm) on Top Layer And Pad U3-3(7.95mm,29.5mm) on Top
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad U3-4(7.95mm,31.9mm) on Top Layer And Pad U3-5(7mm,31.9mm) on Top
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad U3-5(7mm,31.9mm) on Top Layer And Pad U3-6(6.05mm,31.9mm) on Top
Minimum Solder Mask Sliver Constraint: (0.115mm < 0.3mm) Between Pad U4-4(19.25mm,10.95mm) on Top Layer And Via (20mm,11mm) from Top Layer
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad U5-1(23.75mm,51.9mm) on Top Layer And Pad U5-2(23.75mm,51.4mm) on
Minimum Solder Mask Sliver Constraint: (0.134mm < 0.3mm) Between Pad U5-1(23.75mm,51.9mm) on Top Layer And Pad U5-24(24.5mm,52.65mm) on
Minimum Solder Mask Sliver Constraint: (0.072mm < 0.3mm) Between Pad U5-1(23.75mm,51.9mm) on Top Layer And Pad U5-25(25.75mm,50.65mm) on
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad U5-10(26mm,48.65mm) on Top Layer And Pad U5-11(26.5mm,48.65mm) on
Minimum Solder Mask Sliver Constraint: (0.072mm < 0.3mm) Between Pad U5-10(26mm,48.65mm) on Top Layer And Pad U5-25(25.75mm,50.65mm) on
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad U5-10(26mm,48.65mm) on Top Layer And Pad U5-9(25.5mm,48.65mm) on Top
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad U5-11(26.5mm,48.65mm) on Top Layer And Pad U5-12(27mm,48.65mm) on

Minimum Solder Mask Sliver (Gap=0.3mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.072mm < 0.3mm) Between Pad U5-11(26.5mm,48.65mm) on Top Layer And Pad U5-25(25.75mm,50.65mm) on
Minimum Solder Mask Sliver Constraint: (0.202mm < 0.3mm) Between Pad U5-12(27mm,48.65mm) on Top Layer And Pad U5-13(27.75mm,49.4mm) on
Minimum Solder Mask Sliver Constraint: (0.072mm < 0.3mm) Between Pad U5-12(27mm,48.65mm) on Top Layer And Pad U5-25(25.75mm,50.65mm) on
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad U5-13(27.75mm,49.4mm) on Top Layer And Pad U5-14(27.75mm,49.9mm) on
Minimum Solder Mask Sliver Constraint: (0.072mm < 0.3mm) Between Pad U5-13(27.75mm,49.4mm) on Top Layer And Pad U5-25(25.75mm,50.65mm) on
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad U5-14(27.75mm,49.9mm) on Top Layer And Pad U5-15(27.75mm,50.4mm) on
Minimum Solder Mask Sliver Constraint: (0.072mm < 0.3mm) Between Pad U5-14(27.75mm,49.9mm) on Top Layer And Pad U5-25(25.75mm,50.65mm) on
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad U5-15(27.75mm,50.4mm) on Top Layer And Pad U5-16(27.75mm,50.9mm) on
Minimum Solder Mask Sliver Constraint: (0.072mm < 0.3mm) Between Pad U5-15(27.75mm,50.4mm) on Top Layer And Pad U5-25(25.75mm,50.65mm) on
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad U5-16(27.75mm,50.9mm) on Top Layer And Pad U5-17(27.75mm,51.4mm) on
Minimum Solder Mask Sliver Constraint: (0.072mm < 0.3mm) Between Pad U5-16(27.75mm,50.9mm) on Top Layer And Pad U5-25(25.75mm,50.65mm) on
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad U5-17(27.75mm,51.4mm) on Top Layer And Pad U5-18(27.75mm,51.9mm) on
Minimum Solder Mask Sliver Constraint: (0.072mm < 0.3mm) Between Pad U5-17(27.75mm,51.4mm) on Top Layer And Pad U5-25(25.75mm,50.65mm) on
Minimum Solder Mask Sliver Constraint: (0.202mm < 0.3mm) Between Pad U5-18(27.75mm,51.9mm) on Top Layer And Pad U5-19(27mm,52.65mm) on
Minimum Solder Mask Sliver Constraint: (0.072mm < 0.3mm) Between Pad U5-18(27.75mm,51.9mm) on Top Layer And Pad U5-25(25.75mm,50.65mm) on
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad U5-19(27mm,52.65mm) on Top Layer And Pad U5-20(26.5mm,52.65mm) on
Minimum Solder Mask Sliver Constraint: (0.072mm < 0.3mm) Between Pad U5-19(27mm,52.65mm) on Top Layer And Pad U5-25(25.75mm,50.65mm) on
Minimum Solder Mask Sliver Constraint: (0.072mm < 0.3mm) Between Pad U5-2(23.75mm,51.4mm) on Top Layer And Pad U5-25(25.75mm,50.65mm) on
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad U5-2(23.75mm,51.4mm) on Top Layer And Pad U5-3(23.75mm,50.9mm) on
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad U5-20(26.5mm,52.65mm) on Top Layer And Pad U5-21(26mm,52.65mm) on
Minimum Solder Mask Sliver Constraint: (0.072mm < 0.3mm) Between Pad U5-20(26.5mm,52.65mm) on Top Layer And Pad U5-25(25.75mm,50.65mm) on
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad U5-21(26mm,52.65mm) on Top Layer And Pad U5-22(25.5mm,52.65mm) on
Minimum Solder Mask Sliver Constraint: (0.072mm < 0.3mm) Between Pad U5-21(26mm,52.65mm) on Top Layer And Pad U5-25(25.75mm,50.65mm) on
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad U5-22(25.5mm,52.65mm) on Top Layer And Pad U5-23(25mm,52.65mm) on
Minimum Solder Mask Sliver Constraint: (0.072mm < 0.3mm) Between Pad U5-22(25.5mm,52.65mm) on Top Layer And Pad U5-25(25.75mm,50.65mm) on
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad U5-23(25mm,52.65mm) on Top Layer And Pad U5-24(24.5mm,52.65mm) on
Minimum Solder Mask Sliver Constraint: (0.072mm < 0.3mm) Between Pad U5-23(25mm,52.65mm) on Top Layer And Pad U5-25(25.75mm,50.65mm) on
Minimum Solder Mask Sliver Constraint: (0.072mm < 0.3mm) Between Pad U5-24(24.5mm,52.65mm) on Top Layer And Pad U5-25(25.75mm,50.65mm) on
Minimum Solder Mask Sliver Constraint: (0.072mm < 0.3mm) Between Pad U5-25(25.75mm,50.65mm) on Top Layer And Pad U5-3(23.75mm,50.9mm) on
Minimum Solder Mask Sliver Constraint: (0.072mm < 0.3mm) Between Pad U5-25(25.75mm,50.65mm) on Top Layer And Pad U5-4(23.75mm,50.4mm) on
Minimum Solder Mask Sliver Constraint: (0.072mm < 0.3mm) Between Pad U5-25(25.75mm,50.65mm) on Top Layer And Pad U5-5(23.75mm,49.9mm) on
Minimum Solder Mask Sliver Constraint: (0.072mm < 0.3mm) Between Pad U5-25(25.75mm,50.65mm) on Top Layer And Pad U5-6(23.75mm,49.4mm) on
Minimum Solder Mask Sliver Constraint: (0.072mm < 0.3mm) Between Pad U5-25(25.75mm,50.65mm) on Top Layer And Pad U5-7(24.5mm,48.65mm) on
Minimum Solder Mask Sliver Constraint: (0.072mm < 0.3mm) Between Pad U5-25(25.75mm,50.65mm) on Top Layer And Pad U5-8(25mm,48.65mm) on
Minimum Solder Mask Sliver Constraint: (0.072mm < 0.3mm) Between Pad U5-25(25.75mm,50.65mm) on Top Layer And Pad U5-9(25.5mm,48.65mm) on
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad U5-3(23.75mm,50.9mm) on Top Layer And Pad U5-4(23.75mm,50.4mm) on
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad U5-4(23.75mm,50.4mm) on Top Layer And Pad U5-5(23.75mm,49.9mm) on
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad U5-5(23.75mm,49.9mm) on Top Layer And Pad U5-6(23.75mm,49.4mm) on
Minimum Solder Mask Sliver Constraint: (0.202mm < 0.3mm) Between Pad U5-6(23.75mm,49.4mm) on Top Layer And Pad U5-7(24.5mm,48.65mm) on
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad U5-7(24.5mm,48.65mm) on Top Layer And Pad U5-8(25mm,48.65mm) on Top
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad U5-8(25mm,48.65mm) on Top Layer And Pad U5-9(25.5mm,48.65mm) on Top

Silk To Solder Mask (Clearance=0.178mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad C11-2(20.95mm,15.35mm) on Top Layer And Text "C11"
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad C13-1(49.75mm,9.05mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad C13-2(49.75mm,7.7mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad C14-1(49.75mm,10.75mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad C14-2(49.75mm,12.1mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.176mm < 0.178mm) Between Pad C19-2(25.3mm,56.475mm) on Top Layer And Text "C19"
Silk To Solder Mask Clearance Constraint: (0.127mm < 0.178mm) Between Pad L1-1(54.2mm,48.825mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.127mm < 0.178mm) Between Pad L1-2(54.2mm,56.039mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.127mm < 0.178mm) Between Pad L1-3(43.557mm,52.432mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.164mm < 0.178mm) Between Pad P5-A1(6.225mm,52.975mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.164mm < 0.178mm) Between Pad P5-A12(6.225mm,47.025mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.164mm < 0.178mm) Between Pad P5-A4(6.225mm,52.125mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.164mm < 0.178mm) Between Pad P5-A5(6.225mm,51.275mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.164mm < 0.178mm) Between Pad P5-A6(6.225mm,50.425mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.164mm < 0.178mm) Between Pad P5-A7(6.225mm,49.575mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.164mm < 0.178mm) Between Pad P5-A8(6.225mm,48.725mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.164mm < 0.178mm) Between Pad P5-A9(6.225mm,47.875mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.082mm < 0.178mm) Between Pad P6-1(34.7mm,20.94mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad P6-1(34.7mm,20.94mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.144mm < 0.178mm) Between Pad P6-1(34.7mm,20.94mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.088mm < 0.178mm) Between Pad P6-2(34.7mm,18.4mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad P6-2(34.7mm,18.4mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.088mm < 0.178mm) Between Pad P6-3(34.7mm,15.86mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.169mm < 0.178mm) Between Pad P6-3(34.7mm,15.86mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad P6-3(34.7mm,15.86mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.144mm < 0.178mm) Between Pad P7-1(11mm,40.64mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.082mm < 0.178mm) Between Pad P7-1(11mm,40.64mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad P7-1(11mm,40.64mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad P7-2(11mm,38.1mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.088mm < 0.178mm) Between Pad P7-2(11mm,38.1mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad P7-3(11mm,35.56mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.169mm < 0.178mm) Between Pad P7-3(11mm,35.56mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.088mm < 0.178mm) Between Pad P7-3(11mm,35.56mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.082mm < 0.178mm) Between Pad P8-1(24.2mm,37.64mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad P8-1(24.2mm,37.64mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.144mm < 0.178mm) Between Pad P8-1(24.2mm,37.64mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.088mm < 0.178mm) Between Pad P8-2(24.2mm,35.1mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad P8-2(24.2mm,35.1mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.088mm < 0.178mm) Between Pad P8-3(24.2mm,32.56mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.169mm < 0.178mm) Between Pad P8-3(24.2mm,32.56mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad P8-3(24.2mm,32.56mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.058mm < 0.178mm) Between Pad Q1-1(4.2mm,26.3mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.058mm < 0.178mm) Between Pad Q1-2(4.2mm,24.5mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.058mm < 0.178mm) Between Pad Q2-1(10.2mm,24.45mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.058mm < 0.178mm) Between Pad Q2-2(10.2mm,26.25mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.058mm < 0.178mm) Between Pad Q3-1(34.2mm,3.8mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.058mm < 0.178mm) Between Pad Q3-2(34.2mm,5.6mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad R23-2(25.075mm,43mm) on Top Layer And Text "R31" (25.5mm,41.8mm)
Silk To Solder Mask Clearance Constraint: (0.167mm < 0.178mm) Between Pad R27-2(29.5mm,45.2mm) on Top Layer And Text "R27" (29mm,48mm) on
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.178mm) Between Pad R28-1(25.05mm,46.7mm) on Top Layer And Text "R28" (23.3mm,47.3mm)
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.178mm) Between Pad R28-2(23.5mm,46.7mm) on Top Layer And Text "R28" (23.3mm,47.3mm) on
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad R4-1(55.75mm,45.75mm) on Top Layer And Track

Silk To Solder Mask (Clearance=0.178mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad R4-1(55.75mm,45.75mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.106mm < 0.178mm) Between Pad U5-7(24.5mm,48.65mm) on Top Layer And Text "R28" (23.3mm,47.3mm)
Silk To Solder Mask Clearance Constraint: (0.144mm < 0.178mm) Between Pad U5-8(25mm,48.65mm) on Top Layer And Text "R28" (23.3mm,47.3mm) on
Silk To Solder Mask Clearance Constraint: (0.137mm < 0.178mm) Between Pad U5-9(25.5mm,48.65mm) on Top Layer And Text "R28" (23.3mm,47.3mm)

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.248mm < 0.254mm) Between Text "BAT -

BAT +" (0.5mm,0.8mm) on Top Overlay And Track (0.5mm,0.5mm)(10.5mm,0.5mm) on Top Overlay Silk Text to Silk Clearan

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.249mm < 0.254mm) Between Text "BAT -

BAT +" (0.5mm,0.8mm) on Top Overlay And Track (0.5mm,3.5mm)(1mm,3.5mm) on Top Overlay Silk Text to Silk Clearance

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.229mm < 0.254mm) Between Text "BAT -

BAT +" (0.5mm,0.8mm) on Top Overlay And Track (1mm,3.5mm)(10.5mm,3.5mm) on Top Overlay Silk Text to Silk Clearanc

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.248mm < 0.254mm) Between Text "GND

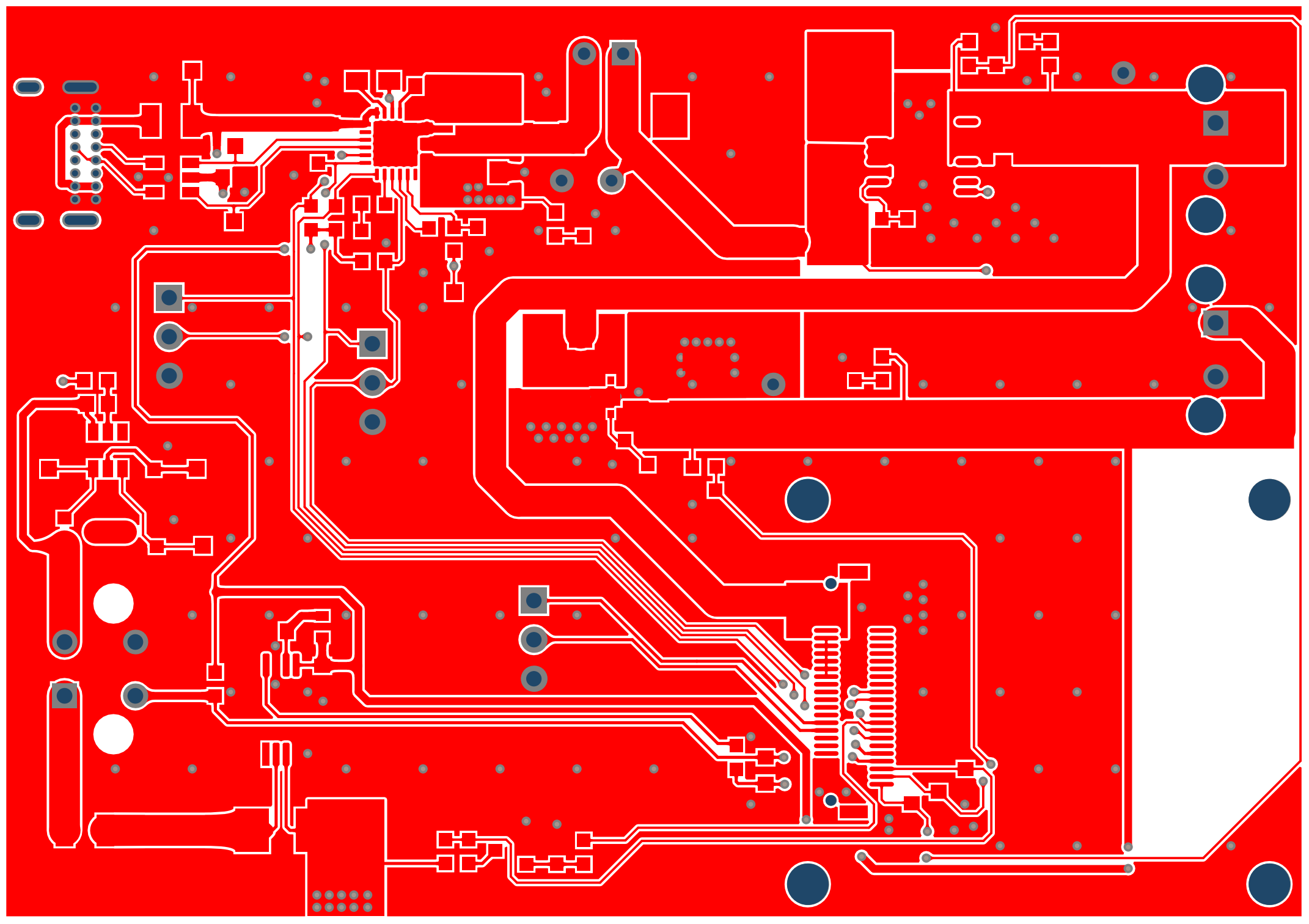
TEMP" (5.6mm,0.8mm) on Top Overlay And Track (0.5mm,0.5mm)(10.5mm,0.5mm) on Top Overlay Silk Text to Silk Clearan

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.229mm < 0.254mm) Between Text "GND

TEMP" (5.6mm,0.8mm) on Top Overlay And Track (1mm,3.5mm)(10.5mm,3.5mm) on Top Overlay Silk Text to Silk Clearanc

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.248mm < 0.254mm) Between Text "P2" (1.7mm,22.7mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.23mm < 0.254mm) Between Text "P4" (81.8mm,41.9mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.228mm < 0.254mm) Between Text "P4" (81.8mm,41.9mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.203mm < 0.254mm) Between Text "P7" (10.6mm,42mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.23mm < 0.254mm) Between Text "P9" (81.8mm,54.9mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.228mm < 0.254mm) Between Text "P9" (81.8mm,54.9mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.248mm < 0.254mm) Between Text "Q1" (5.3mm,22.7mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.248mm < 0.254mm) Between Text "Q2" (7.8mm,22.7mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.25mm < 0.254mm) Between Text "R27" (29mm,48mm) on Top Overlay And Text "U5" (28.4mm,48.4mm) on Top
Silk To Silk Clearance Constraint: (0.175mm < 0.254mm) Between Text "R28" (23.3mm,47.3mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.175mm < 0.254mm) Between Text "R28" (23.3mm,47.3mm) on Top Overlay And Track

Board Clearance Constraint (Gap=0mm) (All)
Board Outline Clearance(Outline Edge): (0.35mm < 0.406mm) Between Board Edge And Text "R3" (62.6mm,59.5mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.35mm < 0.406mm) Between Board Edge And Text "R5" (64.3mm,59.5mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.025mm < 0.406mm) Between Board Edge And Track (0.125mm,45.525mm)(0.125mm,54.475mm) on Top
Board Outline Clearance(Outline Edge): (0.025mm < 0.406mm) Between Board Edge And Track (0.125mm,45.525mm)(0.475mm,45.525mm) on Top
Board Outline Clearance(Outline Edge): (0.025mm < 0.406mm) Between Board Edge And Track (0.125mm,54.475mm)(0.475mm,54.475mm) on Top
Board Outline Clearance(Outline Edge): (0.373mm < 0.406mm) Between Board Edge And Track (0.5mm,0.5mm)(0.5mm,3.5mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.373mm < 0.406mm) Between Board Edge And Track (0.5mm,0.5mm)(10.5mm,0.5mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.373mm < 0.406mm) Between Board Edge And Track (0.5mm,3.5mm)(0.5mm,9.5mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.373mm < 0.406mm) Between Board Edge And Track (0.5mm,3.5mm)(1mm,3.5mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.373mm < 0.406mm) Between Board Edge And Track (0.5mm,9.5mm)(0.5mm,9.6mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.373mm < 0.406mm) Between Board Edge And Track (0.5mm,9.6mm)(1.3mm,10.4mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.373mm < 0.406mm) Between Board Edge And Track (10.5mm,0.5mm)(10.5mm,3.5mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (50mm,0mm)(50mm,30mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (50mm,0mm)(85mm,0mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (50mm,30mm)(85mm,30mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (85mm,0mm)(85mm,30mm) on Top Overlay



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