

A

B

C

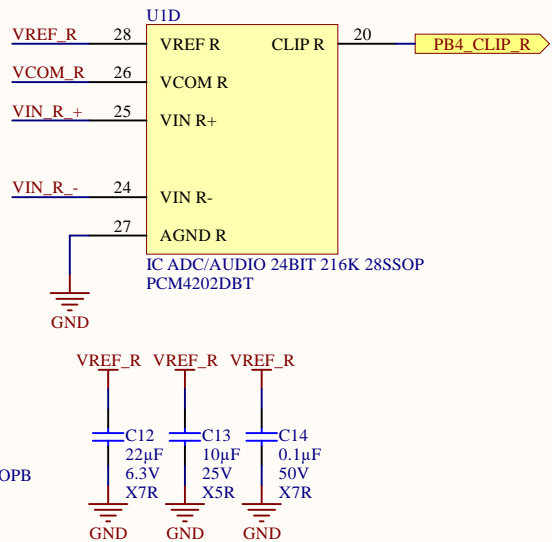
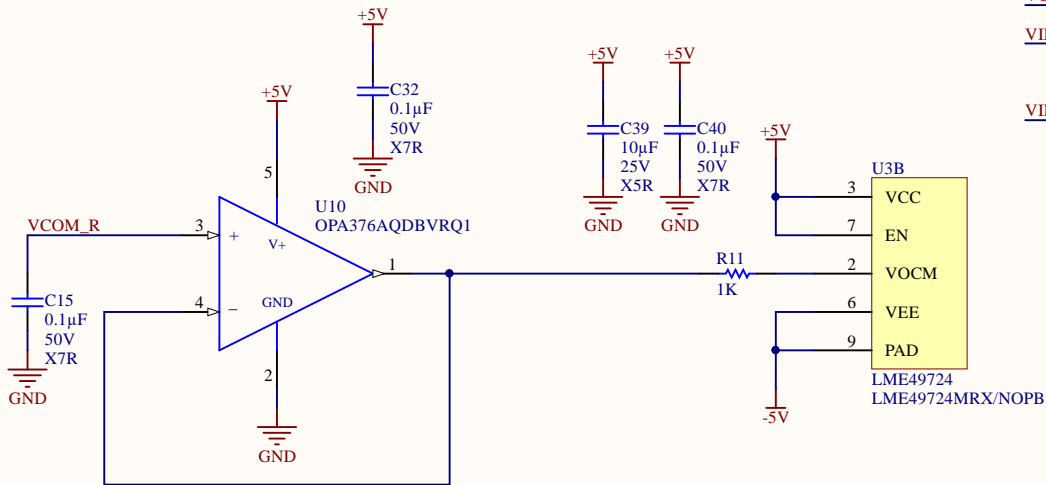
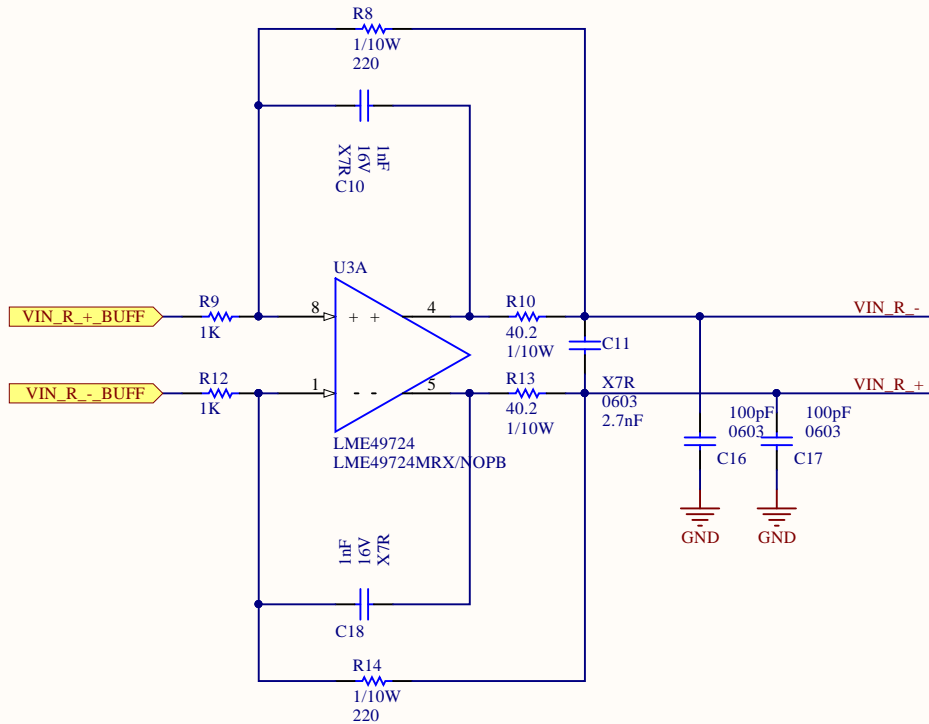
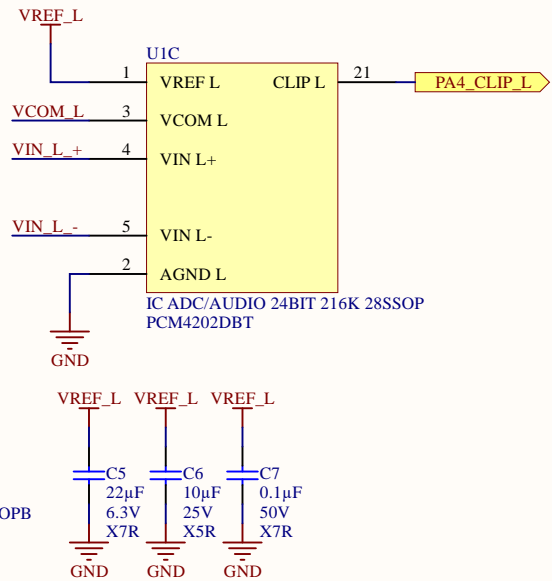
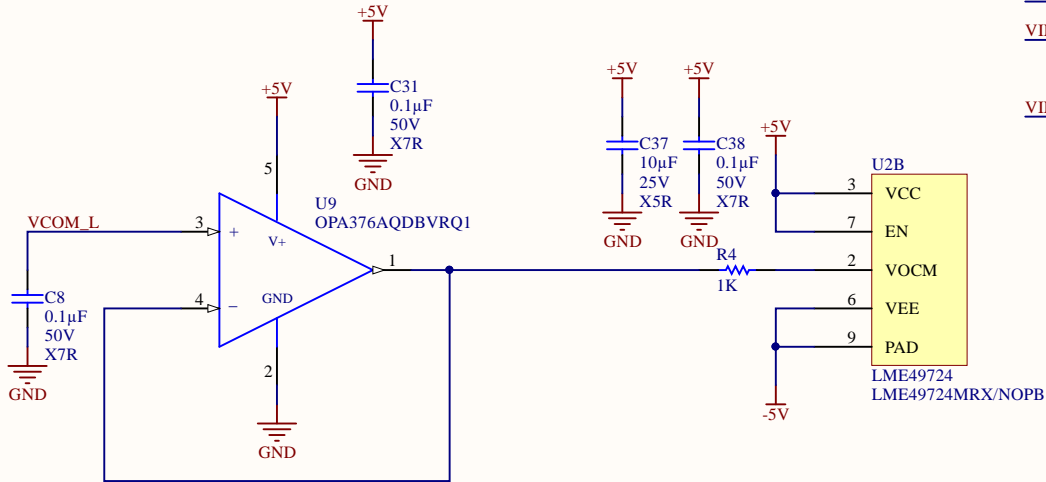
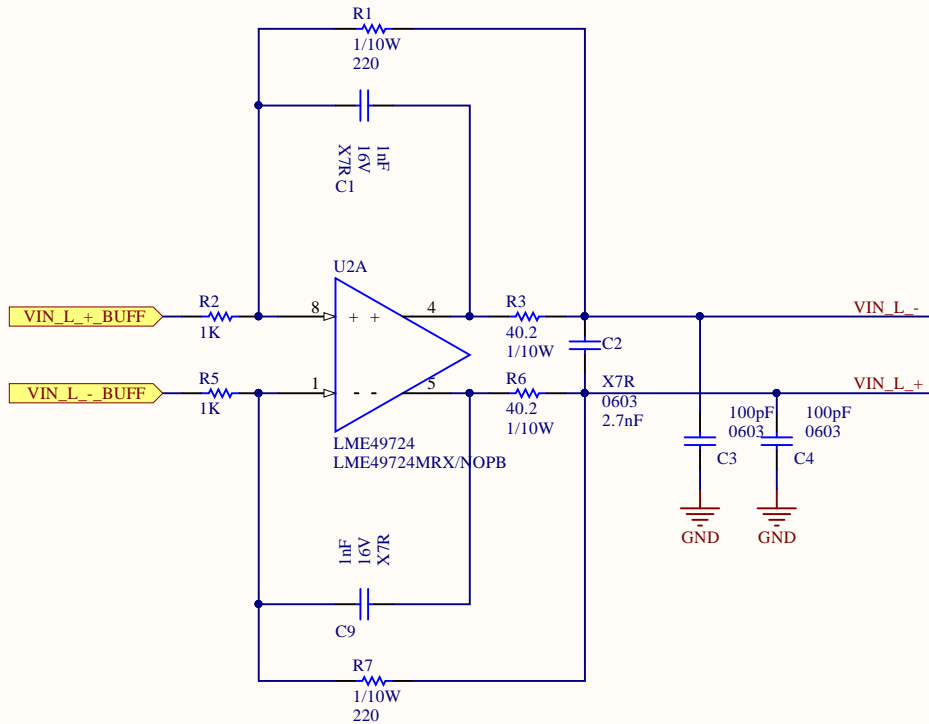
D

A

B

C

D



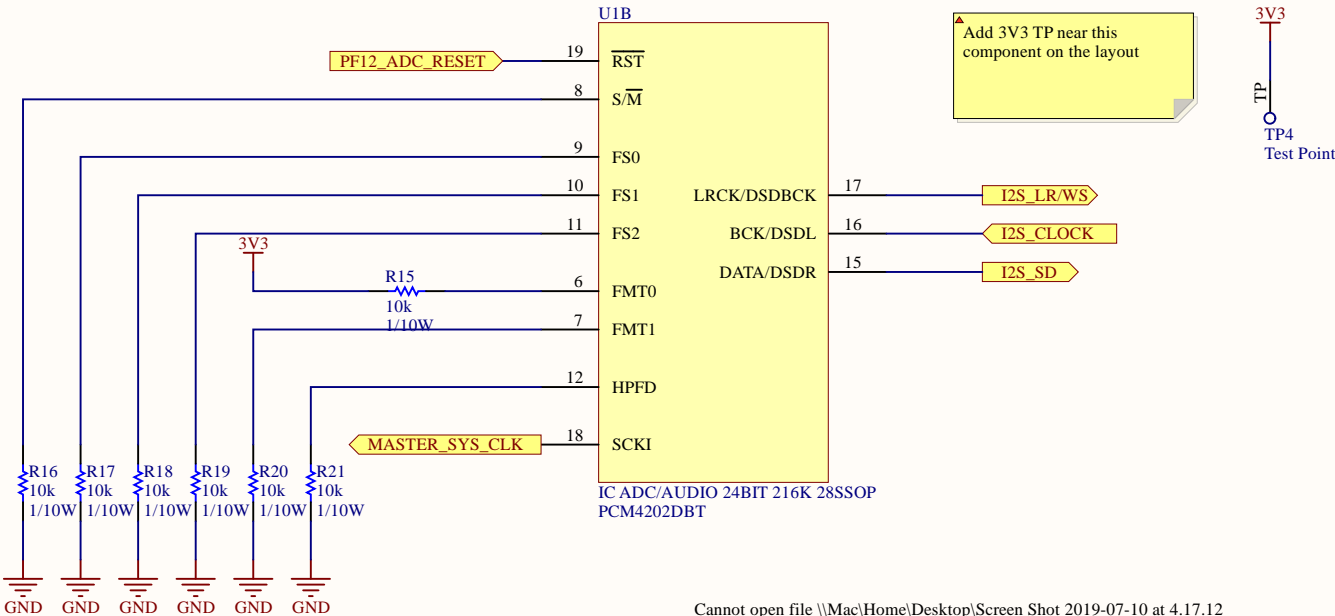
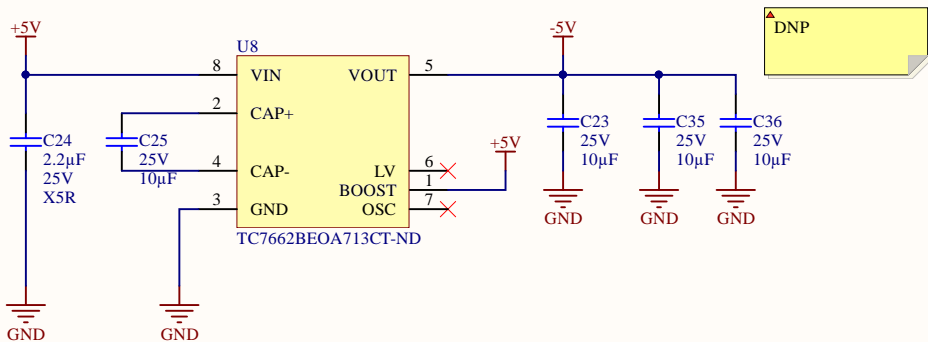
PROJECT MIXR Input System.PrjPcb	
DOCUMENT *	
PART NUMBER	VARIANT [No Variations]
DRAWN BY	REVISION
LAST MODIFIED 2019-07-12	SHEET * OF *

**MIXR**



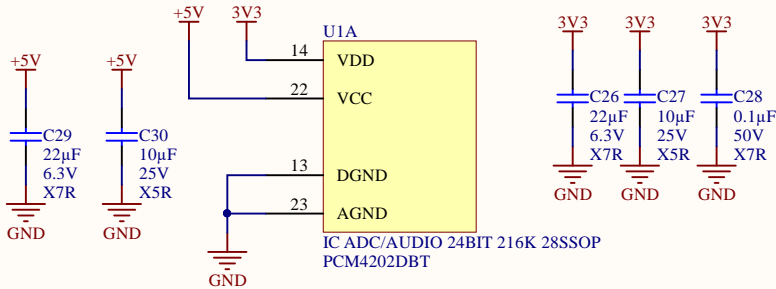
Table 5. Audio Data Format Selection

FMT1	FMT0	AUDIO DATA FORMAT
0	0	24-bit Left Justified
0	1	24-bit I2S
1	0	24-bit Right Justified
1	1	1-bit DSD (Master Mode Only)



Add 3V3 TP near this component on the layout




3V3  
TP  
TP4  
Test Point



Cannot open file \\Mac\Home\Desktop\Screen Shot 2019-07-10 at 4.17.12 PM.png

PROJECT	MIXR Input System.PrjPcb
DOCUMENT	*
PART NUMBER	VARIANT [No Variations]
DRAWN BY	REVISION
LAST MODIFIED	2019-07-12
SHEET	* OF *



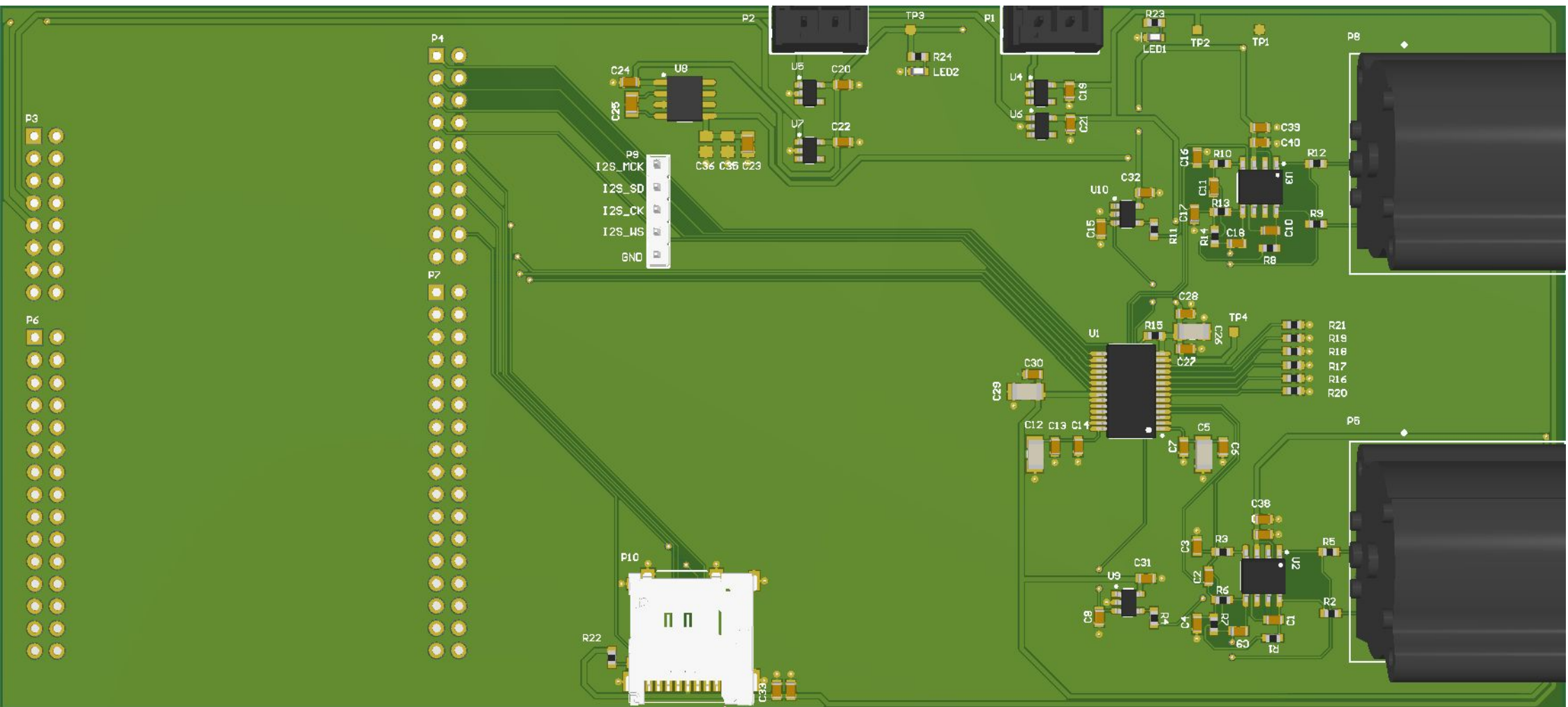
1	2	3	4	5	6																											
A					A																											
B					B																											
C					C																											
D	<table><tr><td colspan="2">PROJECT</td><td colspan="2">MIXR Input System.PrjPcb</td><td rowspan="5"></td></tr><tr><td colspan="2">DOCUMENT</td><td colspan="2">*</td></tr><tr><td colspan="2">PART NUMBER</td><td>VARIANT</td><td>[No Variations]</td></tr><tr><td colspan="2">DRAWN BY</td><td colspan="2">REVISION</td></tr><tr><td colspan="2">LAST MODIFIED</td><td colspan="2">2019-07-12</td></tr><tr><td colspan="2"></td><td>SHEET</td><td>*</td><td>OF</td><td>*</td></tr></table>				PROJECT		MIXR Input System.PrjPcb			DOCUMENT		*		PART NUMBER		VARIANT	[No Variations]	DRAWN BY		REVISION		LAST MODIFIED		2019-07-12				SHEET	*	OF	*	D
PROJECT		MIXR Input System.PrjPcb																														
DOCUMENT		*																														
PART NUMBER		VARIANT	[No Variations]																													
DRAWN BY		REVISION																														
LAST MODIFIED		2019-07-12																														
		SHEET	*	OF	*																											
1	2	3	4	5	6																											

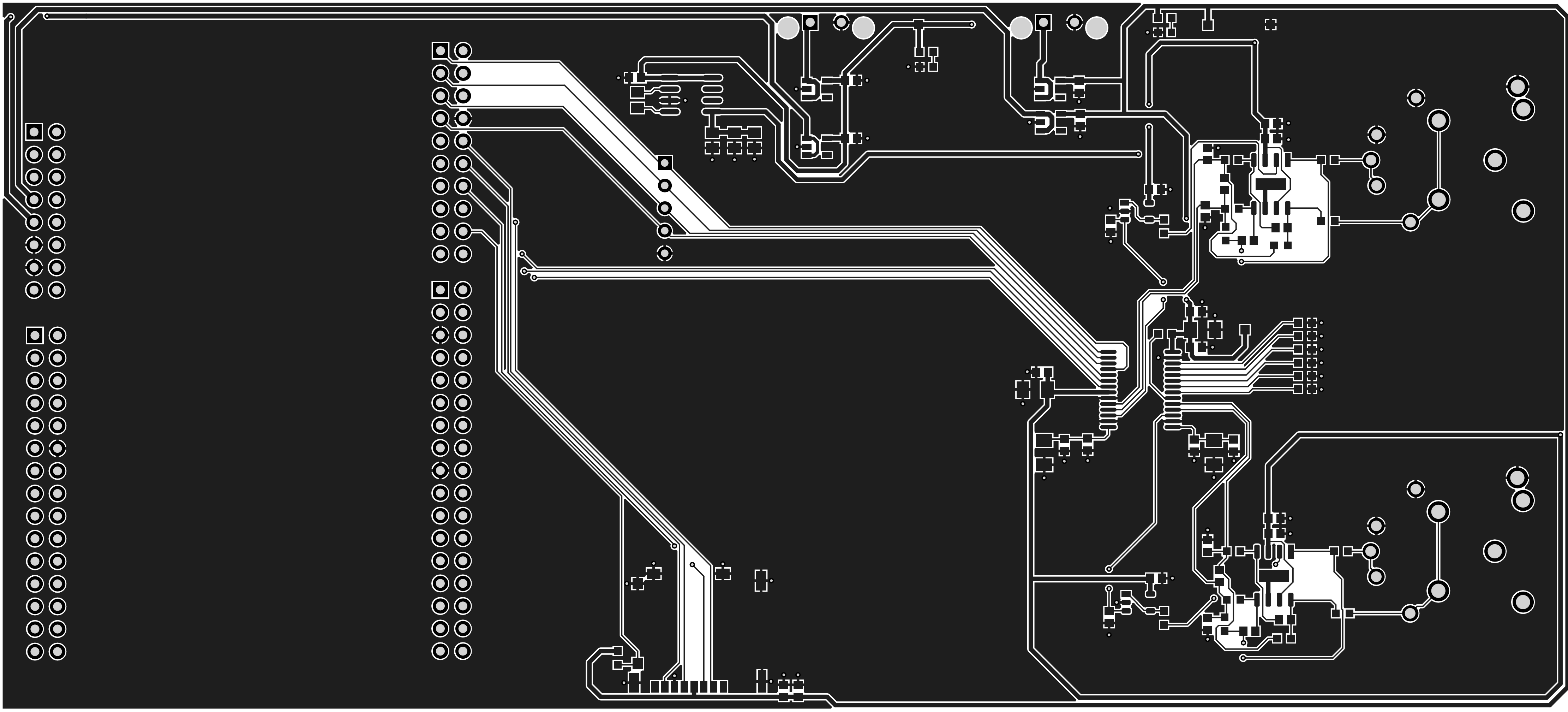
# Bill of Materials

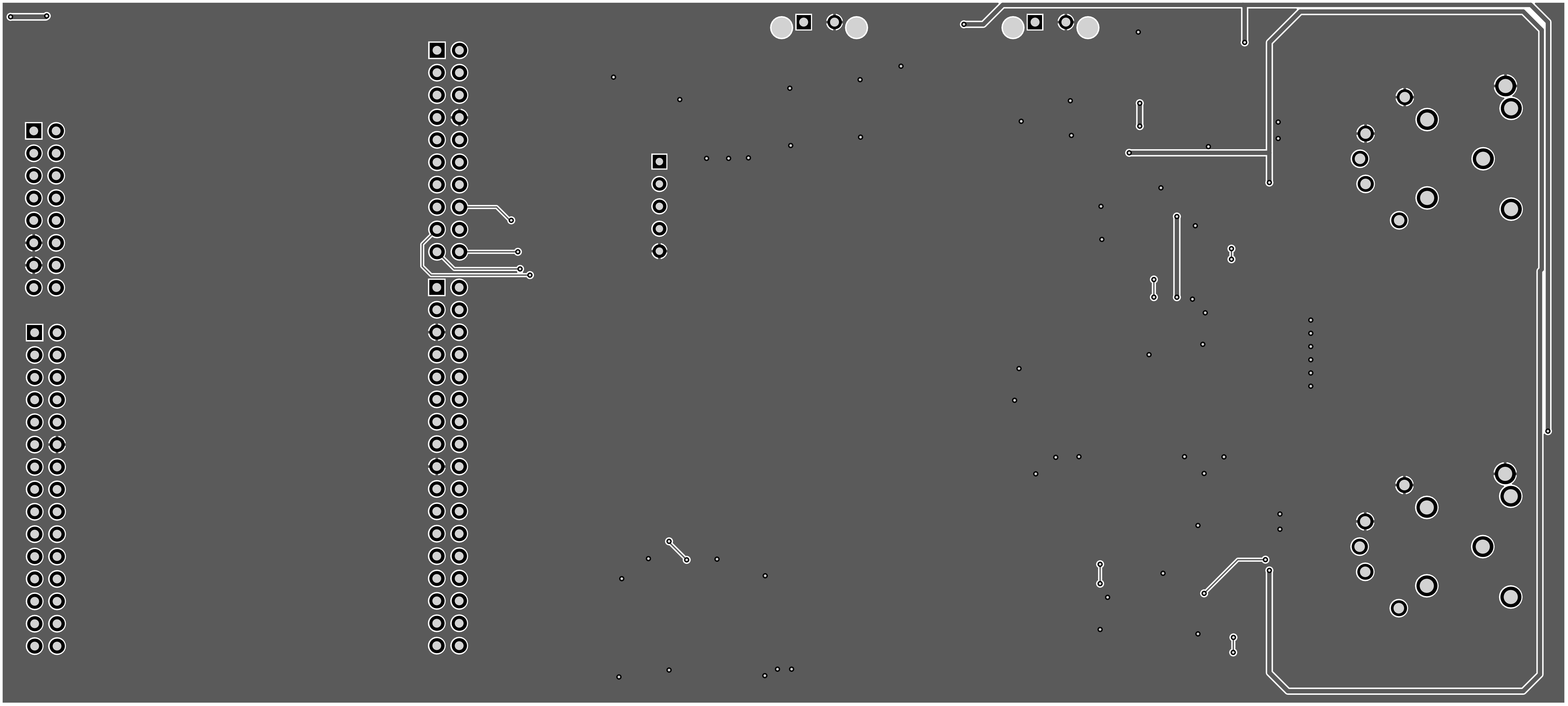
Project:	MIXR Input System.PrfPcb
Revision:	<Parameter ProjectRevision not found>
Project Lead:	<Parameter ProjectAuthor not found>
Generated On:	2019-07-12 20:30
Production Quantity:	1
Currency	CAD
Total Parts Count:	84

# MIXR

LibRef	Designator	Manufacturer 1	Manufacturer Part Number 1	Supplier 1	Supplier Part Number 1	Supplier Unit Price 1	Quantity	Supplier Subtotal 1
CAP CER 1NF 16V 10% X7R 0603	C1, C9, C10, C18	KEMET	C0603C102K4RECAUTO	Digi-Key	399-17878-1-ND	0.24768	4	\$ 0.99
CAP CER 2700PF 50V X7R 0603	C2, C11	KEMET	C0603C272K5RACTU	Digi-Key	399-7890-1-ND	0.14339	2	\$ 0.29
CAP CER 100PF 50V C0G/NP0 0603	C3, C4, C16, C17	Kyocera AVX	06035A101FAT2A	Digi-Key	478-6202-1-ND	0.24768	4	\$ 0.99
CAP CER 22UF 6.3V ±10% X7R 1206	C5, C12, C26, C29	Murata	GRM31CR70J226KE19L	Digi-Key	490-6515-1-ND	1.39	4	\$ 5.58
CAP CER 10uF 25V 20% X5R 0603	C6, C13, C27, C30, C37, C39	Murata	GRM188R61E106MA73D	Digi-Key	490-7202-1-ND	0.5475	6	\$ 3.28
CAP CER 0.1UF 50V 10% X7R 0603	C7, C8, C14, C15, C28, C31, C32, C34, C38, C4	Kyocera AVX	06035C-104KAT2A	Digi-Key	478-5052-1-ND	0.14991	10	\$ 1.50
CAP CER 4.7UF 25V 10% X5R 0603	C19, C20, C21, C22, C33	Murata	GRM188R61E475KE11D	Digi-Key	490-7203-1-ND	0.48232	5	\$ 2.41
CAP CER 10uF 25V 10% X5R 0805	C23, C25	Murata	GRM21BR61E106KA73L	Digi-Key	490-5523-1-ND	0.56054	2	\$ 1.12
CAP CER 2.2UF 25V 10% X5R 0603	C24	Murata	GRM188R61E225KA12D	Digi-Key	490-10731-1-ND	0.22161	1	\$ 0.22
LED GREEN CLEAR 2V 0603	LED1	Wurth Electronics	150060VS75000	Digi-Key	732-4980-1-ND	0.1825	1	\$ 0.18
LED BLUE CLEAR 2.8V 0603	LED2	Vishay Lite-On	LTST-C193TBKT-5A	Digi-Key	160-1827-1-ND	0.61268	1	\$ 0.61
CONN 2POS ULTRA-FIT 0.138"	P1, P2	Molex	1722871102	Digi-Key	WM11701-ND	1.02	2	\$ 2.03
CONN 16POS HEADER FEMALE 0.1"	P3	Sullins	PPTC082LFBN-RC	Digi-Key	S7076-ND	1.29	1	\$ 1.29
CONN 20POS HEADER FEMALE 0.1"	P4	Sullins	PPTC102LFBN-RC	Digi-Key	S7078-ND	1.69	1	\$ 1.69
CONN XLR-TRS COMBO 3 POLE	P5, P8	Neutrik	NCJ6FA-H	Mouser	568-NCJ6FA-H	2.69	2	\$ 5.37
CONN 30POS HEADER FEMALE 0.1"	P6	Sullins	PPTC152LFBN-RC	Digi-Key	S7083-ND	2.37	1	\$ 2.37
CONN 34POS HEADER FEMALE 0.1"	P7	Sullins	PPTC172LFBN-RC	Digi-Key	S7085-ND	2.53	1	\$ 2.53
CONN 5POS HEADR MALE 0.1in	P9	Molex	22-28-4050	Digi-Key	WM50014-05-ND	0.31286	1	\$ 0.31
CONN MICRO-SD ULTRA-LOW 8CKT	P10	Molex	503182-1852	Digi-Key	WM12834CT-ND	3.19	1	\$ 3.19
RES 220 OHM 1% 1/10W 0603	R1, R7, R8, R14	Yageo Phycomp	RC0603FR-07220RL	Digi-Key	311-220HRCT-ND	0.13036	4	\$ 0.52
RES 1K OHM 5% 1/10W 0603	R2, R4, R5, R9, R11, R12	Yageo	RC0603JR-071KL	Digi-Key	311-1.0KGRCT-ND	0.13036	6	\$ 0.78
RES 40.2 OHM 0.5% 1/10W 0603	R3, R6, R10, R13	Yageo	RT0603DRE0740R2L	Digi-Key	311-2576-1-ND	0.15643	4	\$ 0.63
RES 10K OHM 1% 1/10W 0603	R5, R16, R17, R18, R19, R20, R21, R22, R23, R	Yageo Phycomp	RC0603FR-0710KL	Digi-Key	311-10.0KHRCT-ND	0.03129	10	\$ 0.31
IC ADC 24 BIT AUDIO 216KHZ SSOP-28	U1	Texas Instruments	PCM4202DBT	Digi-Key	296-17438-1-ND	12.84	1	\$ 12.84
IC OP AMP AUDIO LME49724 8-SOIC	U2, U3	TI National Semiconductor	LME49724MRX/NOPB	Digi-Key	296-37390-1-ND	3.48	2	\$ 6.96
IC IDEAL DIODE CURRENT SWITCH SOT23-5	U4, U5, U6, U7	Maxim	MAX40200AUK+T	Digi-Key	MAX40200AUK+TCT-ND	1.16	4	\$ 4.64
IC REG SWTCHD CAP INV 20MA 8SOIC	U8	Microchip	TC7662BEOA713	Digi-Key	TC7662BEOA713CT-ND	2.99	1	\$ 2.99
IC OP AMP GEN PURPOSE RR 5.5MHZ SOT-23-5	U9, U10	Texas Instruments	OPA376AQDBVRQ1	Digi-Key	296-36701-1-ND	2.79	2	\$ 5.58
							Total:	\$ 71.21









## Design Rules Verification Report

Filename : C:\Users\Taiping\Documents\FYDP\mixr-hardware\MIXR Input System\MIXR In

Warnings 0  
Rule Violations 152

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.152mm) (All),(All)	0
Clearance Constraint (Gap=0.6mm) (Disabled)(InNetClass('HV_IN')), (InNet('*+6V'))	0
Clearance Constraint (Gap=0.6mm) (Disabled)(InNetClass('HV_IN')), (InNet('*+5V'))	0
Clearance Constraint (Gap=0.6mm) (Disabled)(InNetClass('HV_IN')), (InNet('GND'))	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ( (All) )	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.15mm) (Max=2.54mm) (Preferred=0.15mm) (All)	0
Power Plane Connect Rule(Relief Connect )(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.152mm)	0
Hole Size Constraint (Min=0.025mm) (Max=100mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.3mm) (All),(All)	108
Silk To Solder Mask (Clearance=0.178mm) (IsPad),(All)	29
Silk to Silk (Clearance=0mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (All)	15
Height Constraint (Min=0mm) (Max=254mm) (Preferred=12.7mm) (All)	0
Total	152

Minimum Solder Mask Sliver (Gap=0.3mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C 10-1(143.555mm,54.4mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C 1-1(143.925mm,10.3mm) on Top Layer And Pad C 1-2(145.275mm,10.3mm)
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C 11-1(137.8mm,59.95mm) on Top Layer And Pad C 11-2(137.8mm,58.6mm) on
Minimum Solder Mask Sliver Constraint: (0.267mm < 0.3mm) Between Pad C 12-2(117.5mm,27.725mm) on Top Layer And Via (117.5mm,26.255mm) from
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C 13-1(119.77mm,30.625mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.217mm < 0.3mm) Between Pad C 13-2(119.77mm,29.275mm) on Top Layer And Via (119.77mm,28.13mm) from
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C 14-1(122.4mm,30.675mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.3mm) Between Pad C 14-2(122.4mm,29.325mm) on Top Layer And Via (122.4mm,28.2mm) from
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C 15-1(125mm,55.275mm) on Top Layer And Pad C 15-2(125mm,53.925mm) on
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad C 15-2(125mm,53.925mm) on Top Layer And Via (125mm,52.85mm) from Top
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C 16-1(135.9mm,62.025mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.207mm < 0.3mm) Between Pad C 16-2(135.9mm,63.375mm) on Top Layer And Via (137.085mm,63.375mm)
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C 17-1(135.6mm,56.925mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.3mm) Between Pad C 17-2(135.6mm,55.575mm) on Top Layer And Via (135.6mm,54.4mm) from
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C 18-1(139.725mm,52.95mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.172mm < 0.3mm) Between Pad C 18-1(139.725mm,52.95mm) on Top Layer And Via (139.7mm,51.8mm) from
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C 19-1(121.42mm,70.93mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.072mm < 0.3mm) Between Pad C 19-2(121.42mm,69.58mm) on Top Layer And Via (121.42mm,68.58mm) from
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C 20-1(95.075mm,70.97mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.217mm < 0.3mm) Between Pad C 20-2(96.425mm,70.97mm) on Top Layer And Via (97.57mm,70.97mm) from
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C 2-1(137.2mm,15.875mm) on Top Layer And Pad C 2-2(137.2mm,14.525mm)
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C 21-1(121.545mm,67.175mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.252mm < 0.3mm) Between Pad C 21-2(121.545mm,65.825mm) on Top Layer And Via (121.545mm,64.645mm)
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C 22-1(95.075mm,64.45mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.27mm < 0.3mm) Between Pad C 22-2(96.425mm,64.45mm) on Top Layer And Via (97.623mm,64.45mm) from
Minimum Solder Mask Sliver Constraint: (0.182mm < 0.3mm) Between Pad C 23-2(84.906mm,63.36mm) on Top Layer And Via (84.906mm,62.1mm) from
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C 24-1(70.825mm,71.257mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.297mm < 0.3mm) Between Pad C 24-1(70.825mm,71.257mm) on Top Layer And Via (69.6mm,71.257mm) from
Minimum Solder Mask Sliver Constraint: (0.205mm < 0.3mm) Between Pad C 26-2(136.725mm,42.917mm) on Top Layer And Via (136.725mm,44.525mm)
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C 27-1(133.925mm,40.95mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.3mm) Between Pad C 27-2(135.275mm,40.95mm) on Top Layer And Via (136.45mm,40.95mm) from
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C 28-1(133.925mm,44.95mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad C 28-2(135.275mm,44.95mm) on Top Layer And Via (135.275mm,46.075mm)
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.3mm) Between Pad C 29-2(115.1mm,36.2mm) on Top Layer And Via (115.1mm,34.6mm) from Top
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C 30-1(117.947mm,38.15mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C 3-1(135.9mm,17.95mm) on Top Layer And Pad C 3-2(135.9mm,19.3mm) on
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C 31-1(129.425mm,14.975mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.234mm < 0.3mm) Between Pad C 31-2(130.775mm,14.975mm) on Top Layer And Via (131.937mm,14.975mm)
Minimum Solder Mask Sliver Constraint: (0.172mm < 0.3mm) Between Pad C 3-2(135.9mm,19.3mm) on Top Layer And Via (135.9mm,20.4mm) from Top
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C 32-1(129.325mm,58.7mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad C 32-2(130.675mm,58.7mm) on Top Layer And Via (131.7mm,58.7mm) from
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C 33-1(89.8mm,1.625mm) on Top Layer And Pad C 33-2(89.8mm,2.975mm) on
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.3mm) Between Pad C 33-2(89.8mm,2.975mm) on Top Layer And Via (89.8mm,4.1mm) from Top
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C 34-1(88.2mm,2.975mm) on Top Layer And Pad C 34-2(88.2mm,1.625mm) on
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.3mm) Between Pad C 34-1(88.2mm,2.975mm) on Top Layer And Via (88.2mm,4.1mm) from Top
Minimum Solder Mask Sliver Constraint: (0.238mm < 0.3mm) Between Pad C 35-2(82.656mm,63.36mm) on Top Layer And Via (82.656mm,62.044mm) from
Minimum Solder Mask Sliver Constraint: (0.238mm < 0.3mm) Between Pad C 36-2(80.156mm,63.36mm) on Top Layer And Via (80.156mm,62.044mm) from
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C 37-1(142.725mm,19.975mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.3mm) Between Pad C 37-2(144.075mm,19.975mm) on Top Layer And Via (145.2mm,19.975mm)
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C 38-1(142.725mm,21.7mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.3mm) Between Pad C 38-2(144.075mm,21.7mm) on Top Layer And Via (145.2mm,21.7mm) from
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C 39-1(142.4mm,66.1mm) on Top Layer And Pad C 39-2(143.75mm,66.1mm) on

Minimum Solder Mask Sliver (Gap=0.3mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C40-1(142.365mm,64.4mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C4-1(135.9mm,10.5mm) on Top Layer And Pad C4-2(135.9mm,9.15mm) on
Minimum Solder Mask Sliver Constraint: (0.122mm < 0.3mm) Between Pad C4-2(135.9mm,9.15mm) on Top Layer And Via (135.9mm,8.1mm) from Top
Minimum Solder Mask Sliver Constraint: (0.222mm < 0.3mm) Between Pad C5-2(136.6mm,27.725mm) on Top Layer And Via (136.6mm,26.3mm) from Top
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C6-1(138.85mm,30.55mm) on Top Layer And Pad C6-2(138.85mm,29.2mm) on
Minimum Solder Mask Sliver Constraint: (0.092mm < 0.3mm) Between Pad C6-2(138.85mm,29.2mm) on Top Layer And Via (138.85mm,28.18mm) from
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C7-1(134.375mm,30.575mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.092mm < 0.3mm) Between Pad C7-2(134.375mm,29.225mm) on Top Layer And Via (134.375mm,28.205mm)
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C8-1(124.8mm,11.275mm) on Top Layer And Pad C8-2(124.8mm,9.925mm) on
Minimum Solder Mask Sliver Constraint: (0.124mm < 0.3mm) Between Pad C8-1(124.8mm,11.275mm) on Top Layer And Via (125.65mm,12.25mm) from
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C9-1(139.925mm,9mm) on Top Layer And Pad C9-2(141.275mm,9mm) on Top
Minimum Solder Mask Sliver Constraint: (0.267mm < 0.3mm) Between Pad LED1-2(130.3mm,76.371mm) on Top Layer And Via (129.129mm,76.371mm)
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad P10-1(81.4mm,2.735mm) on Top Layer And Pad P10-2(80.3mm,2.735mm) on
Minimum Solder Mask Sliver Constraint: (0.267mm < 0.3mm) Between Pad P10-10(71.76mm,14.365mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.142mm < 0.3mm) Between Pad P10-10(71.76mm,14.365mm) on Top Layer And Via (70.535mm,14.365mm)
Minimum Solder Mask Sliver Constraint: (0.222mm < 0.3mm) Between Pad P10-11(71.355mm,3.215mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.062mm < 0.3mm) Between Pad P10-11(71.355mm,3.215mm) on Top Layer And Via (70.215mm,3.215mm) from
Minimum Solder Mask Sliver Constraint: (0.072mm < 0.3mm) Between Pad P10-11(73.56mm,15.49mm) on Top Layer And Via (73.56mm,16.64mm) from
Minimum Solder Mask Sliver Constraint: (0.012mm < 0.3mm) Between Pad P10-11(81.34mm,15.49mm) on Top Layer And Via (81.34mm,16.58mm) from
Minimum Solder Mask Sliver Constraint: (0.082mm < 0.3mm) Between Pad P10-11(85.645mm,14.695mm) on Top Layer And Via (86.805mm,14.695mm)
Minimum Solder Mask Sliver Constraint: (0.042mm < 0.3mm) Between Pad P10-11(85.745mm,3.365mm) on Top Layer And Via (86.765mm,3.365mm) from
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad P10-2(80.3mm,2.735mm) on Top Layer And Pad P10-3(79.2mm,2.735mm) on
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad P10-3(79.2mm,2.735mm) on Top Layer And Pad P10-4(78.1mm,2.735mm) on
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad P10-4(78.1mm,2.735mm) on Top Layer And Pad P10-5(77mm,2.735mm) on
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad P10-5(77mm,2.735mm) on Top Layer And Pad P10-6(75.9mm,2.735mm) on
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad P10-6(75.9mm,2.735mm) on Top Layer And Pad P10-7(74.8mm,2.735mm) on
Minimum Solder Mask Sliver Constraint: (0.142mm < 0.3mm) Between Pad P10-6(75.9mm,2.735mm) on Top Layer And Via (75.9mm,4mm) from Top Layer
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad P10-7(74.8mm,2.735mm) on Top Layer And Pad P10-8(73.7mm,2.735mm) on
Minimum Solder Mask Sliver Constraint: (0.065mm < 0.3mm) Between Pad P5-8(170.75mm,26.255mm) on Multi-Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.065mm < 0.3mm) Between Pad P8-8(170.79mm,70.255mm) on Multi-Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.142mm < 0.3mm) Between Pad R16-2(147.63mm,37.7mm) on Top Layer And Via (148.7mm,37.7mm) from Top
Minimum Solder Mask Sliver Constraint: (0.142mm < 0.3mm) Between Pad R17-2(147.63mm,39.2mm) on Top Layer And Via (148.7mm,39.2mm) from Top
Minimum Solder Mask Sliver Constraint: (0.142mm < 0.3mm) Between Pad R18-2(147.63mm,40.7mm) on Top Layer And Via (148.7mm,40.7mm) from Top
Minimum Solder Mask Sliver Constraint: (0.142mm < 0.3mm) Between Pad R19-2(147.63mm,42.2mm) on Top Layer And Via (148.7mm,42.2mm) from Top
Minimum Solder Mask Sliver Constraint: (0.142mm < 0.3mm) Between Pad R20-2(147.63mm,36.275mm) on Top Layer And Via (148.7mm,36.2mm) from
Minimum Solder Mask Sliver Constraint: (0.142mm < 0.3mm) Between Pad R21-2(147.63mm,43.7mm) on Top Layer And Via (148.7mm,43.7mm) from Top
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad U10-1(126.575mm,57.2mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad U10-2(126.575mm,56.25mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.3mm) Between Pad U1-13(131.975mm,39.775mm) on Top Layer And Via (130.35mm,39.775mm)
Minimum Solder Mask Sliver Constraint: (0.201mm < 0.3mm) Between Pad U2-2(143.99mm,17.95mm) on Top Layer And Via (143.555mm,16.52mm) from
Minimum Solder Mask Sliver Constraint: (0.117mm < 0.3mm) Between Pad U2-9(143.355mm,15.25mm) on Top Layer And Via (143.555mm,16.52mm) from
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad U4-1(117.02mm,70.95mm) on Top Layer And Pad U4-2(117.02mm,70mm) on
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad U4-2(117.02mm,70mm) on Top Layer And Pad U4-3(117.02mm,69.05mm) on
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad U5-1(90.77mm,70.95mm) on Top Layer And Pad U5-2(90.77mm,70mm) on Top
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad U5-2(90.77mm,70mm) on Top Layer And Pad U5-3(90.77mm,69.05mm) on Top
Minimum Solder Mask Sliver Constraint: (0.142mm < 0.3mm) Between Pad U5-2(90.77mm,70mm) on Top Layer And Via (89.6mm,70mm) from Top Layer
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad U6-1(117.1mm,67.2mm) on Top Layer And Pad U6-2(117.1mm,66.25mm) on
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad U6-2(117.1mm,66.25mm) on Top Layer And Pad U6-3(117.1mm,65.3mm) on
Minimum Solder Mask Sliver Constraint: (0.222mm < 0.3mm) Between Pad U6-2(117.1mm,66.25mm) on Top Layer And Via (115.85mm,66.25mm) from
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad U7-1(90.77mm,64.45mm) on Top Layer And Pad U7-2(90.77mm,63.5mm) on
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad U7-2(90.77mm,63.5mm) on Top Layer And Pad U7-3(90.77mm,62.55mm) on
Minimum Solder Mask Sliver Constraint: (0.042mm < 0.3mm) Between Pad U7-2(90.77mm,63.5mm) on Top Layer And Via (89.7mm,63.5mm) from Top

**Minimum Solder Mask Sliver (Gap=0.3mm) (All),(All)**

Minimum Solder Mask Sliver Constraint: (0.158mm < 0.3mm) Between Pad U8-3(75.356mm,68.717mm) on Top Layer And Via (77.117mm,68.717mm) from
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad U9-1(126.725mm,13.2mm) on Top Layer And Pad U9-2(126.725mm,12.25mm)
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad U9-2(126.725mm,12.25mm) on Top Layer And Pad U9-3(126.725mm,11.3mm)
Minimum Solder Mask Sliver Constraint: (0.072mm < 0.3mm) Between Pad U9-2(126.725mm,12.25mm) on Top Layer And Via (125.65mm,12.25mm) from

**Silk To Solder Mask (Clearance=0.178mm) (IsPad),(All)**

Silk To Solder Mask Clearance Constraint: (0.149mm < 0.178mm) Between Pad C11-2(137.8mm,58.6mm) on Top Layer And Text "R13"
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad C38-1(142.725mm,21.7mm) on Top Layer And Text "C37"
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad C38-2(144.075mm,21.7mm) on Top Layer And Text "C37"
Silk To Solder Mask Clearance Constraint: (0.123mm < 0.178mm) Between Pad C9-1(139.925mm,9mm) on Top Layer And Text "R7" (138.7mm,10.9mm)
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad P10-11(85.745mm,3.365mm) on Top Layer And Text "C33"
Silk To Solder Mask Clearance Constraint: (0.084mm < 0.178mm) Between Pad P5-3(154.24mm,18mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.084mm < 0.178mm) Between Pad P8-3(154.28mm,62mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.173mm < 0.178mm) Between Pad R13-1(139.375mm,56.525mm) on Top Layer And Text "R13"
Silk To Solder Mask Clearance Constraint: (0.173mm < 0.178mm) Between Pad R13-2(137.825mm,56.525mm) on Top Layer And Text "R13"
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U4-1(117.02mm,70.95mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U4-2(117.02mm,70mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U4-3(117.02mm,69.05mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U4-4(119.32mm,69.05mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U4-5(119.32mm,70.95mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U5-1(90.77mm,70.95mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U5-2(90.77mm,70mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U5-3(90.77mm,69.05mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U5-4(93.07mm,69.05mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U5-5(93.07mm,70.95mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U6-1(117.1mm,67.2mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U6-2(117.1mm,66.25mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U6-3(117.1mm,65.3mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U6-4(119.4mm,65.3mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U6-5(119.4mm,67.2mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U7-1(90.77mm,64.45mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U7-2(90.77mm,63.5mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U7-3(90.77mm,62.55mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U7-4(93.07mm,62.55mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U7-5(93.07mm,64.45mm) on Top Layer And Track

**Board Clearance Constraint (Gap=0mm) (All)**

Board Outline Clearance(Outline Edge): (Collision < 0.295mm) Between Arc (82.31mm,0.2mm) on Top Overlay And Board Edge
Board Outline Clearance(Outline Edge): (Collision < 0.295mm) Between Board Edge And Track (113.675mm,74.57mm)(113.675mm,79.87mm) on Top
Board Outline Clearance(Outline Edge): (Collision < 0.295mm) Between Board Edge And Track (113.675mm,79.87mm)(121.92mm,79.87mm) on Top
Board Outline Clearance(Outline Edge): (Collision < 0.295mm) Between Board Edge And Track (120.92mm,79.87mm)(124.75mm,79.87mm) on Top
Board Outline Clearance(Outline Edge): (Collision < 0.295mm) Between Board Edge And Track (124.75mm,74.57mm)(124.75mm,79.87mm) on Top
Board Outline Clearance(Outline Edge): (Collision < 0.295mm) Between Board Edge And Track (153.235mm,30.5mm)(177.735mm,30.5mm) on Top
Board Outline Clearance(Outline Edge): (Collision < 0.295mm) Between Board Edge And Track (153.235mm,5.5mm)(177.735mm,5.5mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.295mm) Between Board Edge And Track (153.275mm,49.5mm)(177.775mm,49.5mm) on Top
Board Outline Clearance(Outline Edge): (Collision < 0.295mm) Between Board Edge And Track (153.275mm,74.5mm)(177.775mm,74.5mm) on Top
Board Outline Clearance(Outline Edge): (Collision < 0.295mm) Between Board Edge And Track (177.735mm,5.5mm)(177.735mm,30.5mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.295mm) Between Board Edge And Track (177.775mm,49.5mm)(177.775mm,74.5mm) on Top
Board Outline Clearance(Outline Edge): (Collision < 0.295mm) Between Board Edge And Track (87.425mm,74.57mm)(87.425mm,79.87mm) on Top
Board Outline Clearance(Outline Edge): (Collision < 0.295mm) Between Board Edge And Track (87.425mm,79.87mm)(95.67mm,79.87mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.295mm) Between Board Edge And Track (94.67mm,79.87mm)(98.5mm,79.87mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.295mm) Between Board Edge And Track (98.5mm,74.57mm)(98.5mm,79.87mm) on Top Overlay

