Assignment 3

Logical Effort

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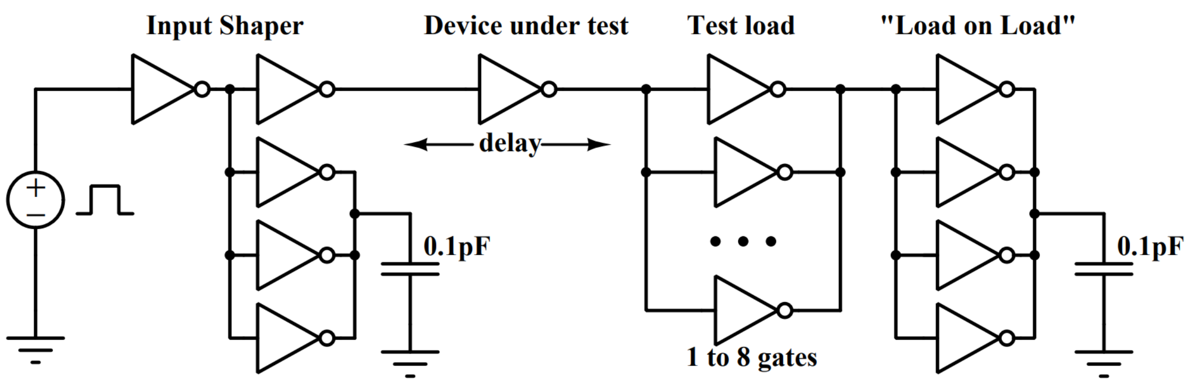
Question 1 :

a) The circuit is shown in the below figure:



Delay: d
Parasitic Delay: Pinv
Logical Effort: g = 1
Branching Effort: b = number of inverters in test load
ELectrical Effort: h = 1
d = g*b*h + Pinv
⇒ d = b + Pinv
⇒ Tau*d = Tau* b + Tau*Pinv
Above is a straight line which we will find from the simulation.

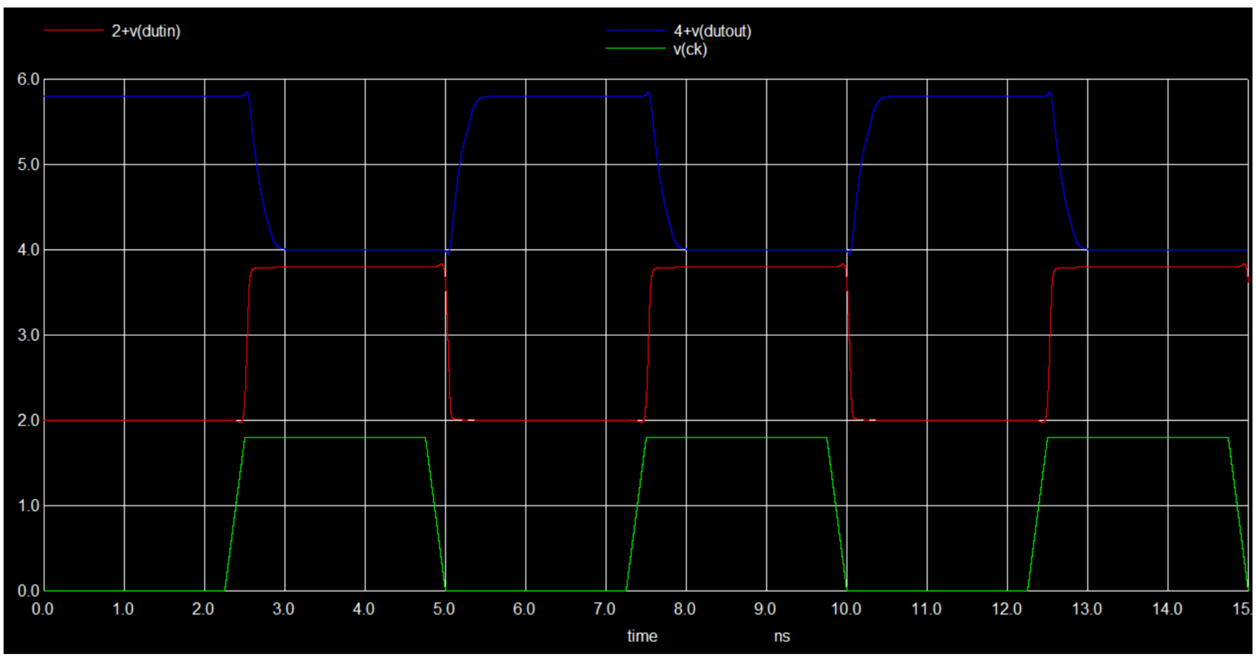
The code used for the above circuit is given below :

```
* Logic Effort Measurement

.include models-180nm

* Unit Inverter
.subckt inv supply Inp Output
```

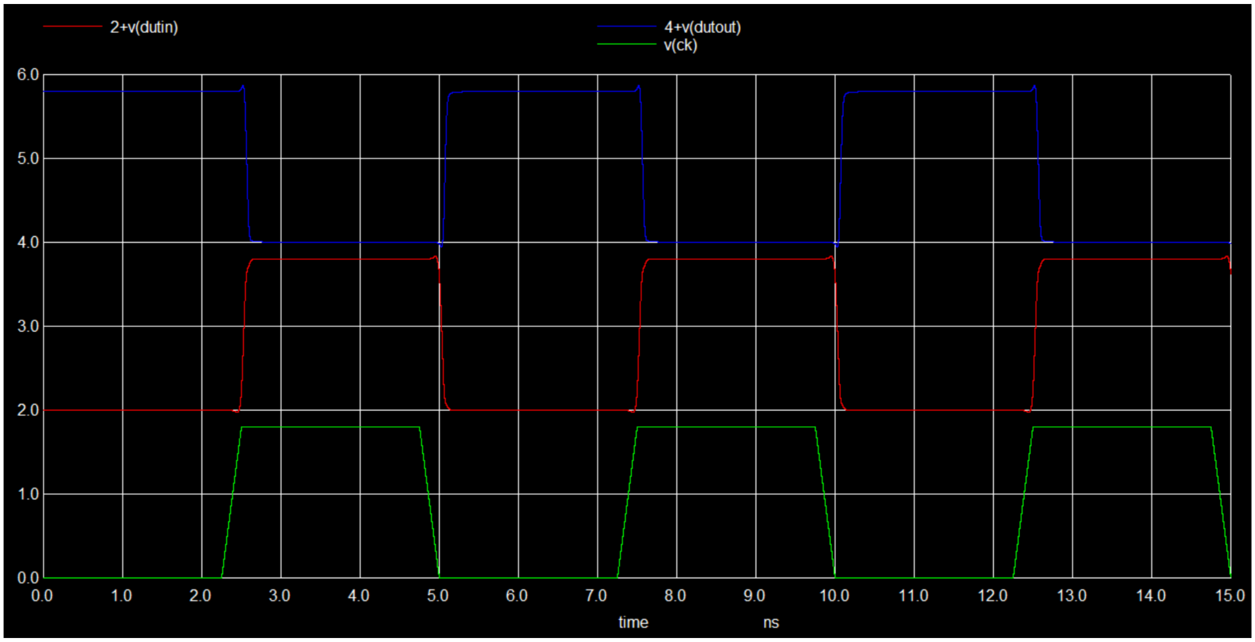
```
.param w_p =1.2961392U                a_p=0.36U*w_p                    p_p=0.72U+2*w_p
.param w_n =0.4162298U        a_n=0.36U*w_n                 p_n=0.72U+2*w_n
MP1 Output Inp Supply Supply cmosp
+ L=0.18U W=w_p AD = a_p AS = a_p PD = p_p PS = p_p
MN1 Output Inp 0 0 cmosn
+ L=0.18U W=w_n AD = a_n AS = a_n PD = p_n PS = p_n
.ends

vdd supply 0 dc 1.8

x0 supply Ck mid inv

x1 supply mid dutin inv
x2 supply mid out inv
x3 supply mid out inv
x4 supply mid out inv

C1 out 0 0.1pF
* DUT
xdut supply dutin dutout inv

* Add inverters one by one to see the change in delay
xtl1 supply dutout out inv
xtl2 supply dutout out inv
xtl3 supply dutout out inv
xtl4 supply dutout out inv
xtl5 supply dutout out inv
xtl6 supply dutout out inv
xtl7 supply dutout out inv
xtl8 supply dutout out inv
xtl9 supply dutout out inv
xtl10 supply dutout out inv
xtl11 supply dutout out inv
xtl12 supply dutout out inv

xll1 supply out llout inv
xll2 supply out llout inv
xll3 supply out llout inv
xll4 supply out llout inv

C2 llout 0 0.1pF

.param Trep= 5n
.param Trf = {Trep/20.0}
```

```
.param Tw = {Trep/2.0 - Trf}
.param hival=1.8
.param loval=0.0
Vpulse Ck 0 DC 0 PULSE({loval} {hival} {Tw} {Trf} {Trf} {Tw} {Trep})
.tran 0.1pS {3*Trep} 0nS

.control
run
plot V(Ck) 2+V(dutin) 4+V(dutout)
meas tran delay1 TRIG v(dutin) VAL=0.9 RISE=2 TARG v(dutout) VAL=0.9 FALL=2
meas tran delay2 TRIG v(dutin) VAL=0.9 FALL=2 TARG v(dutout) VAL=0.9 RISE=2
let avg_delay = (delay1 + delay2)/2
print avg_delay
.endc
.end
```

For b=8



For b=1



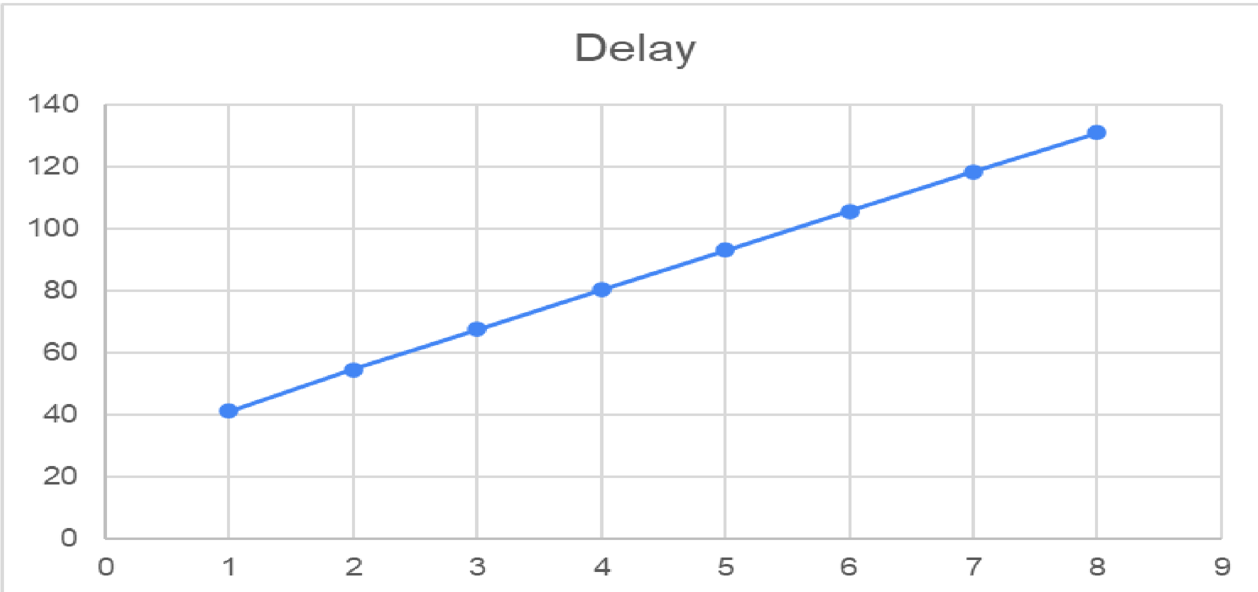
Here in this code by changing the number of inverters we are basically changing the value of b and because of that we can observe the change in the value of delay as given below:

Measured delay against b

b	Delay (in ps)
1	41.1
2	54.5
3	67.45
4	80.22
5	92.9
6	105.55
7	118.177
8	130.82

The graph for delay vs branching is given below and it can be observed that the graph is a perfect straight line:

Absolute Delay vs Branching Effort



Now we need to find the slope and intercept of this straight line which after passing through excel gives :

Slope m = 12.77863095
Intercept c = 28.83578571

Therefore the equation of this line can be written as :
Y = mx + c , here Y - delay and x - b

Y = 12.77863095x + 28.83578571

Tau = Slope of the line = m
= **12.77863095**

Pinv = Intercept/slope = c/m
= 28.83578571/12.77863095
= **2.25656299355**

The widths of the transistors used for same rise and fall times is given below:
w_p =1.2961392U
w_n =0.4162298U

Therefore Gamma = W_P/W_N = **3.11399904572**