Question 1 :

a)

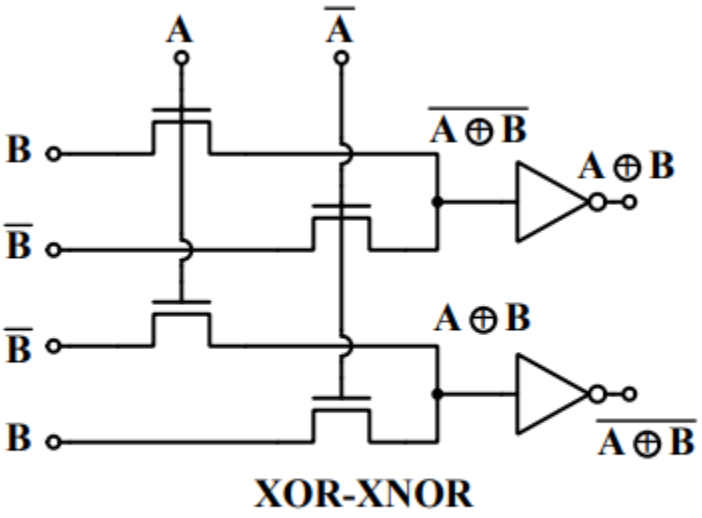
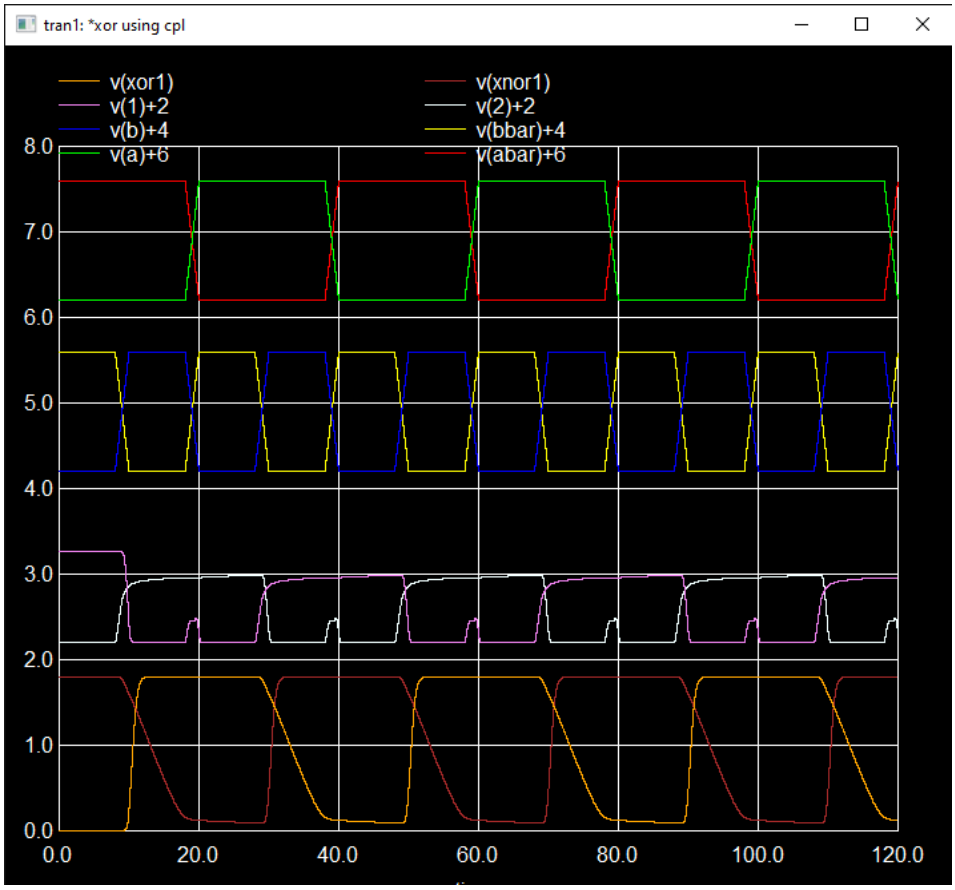
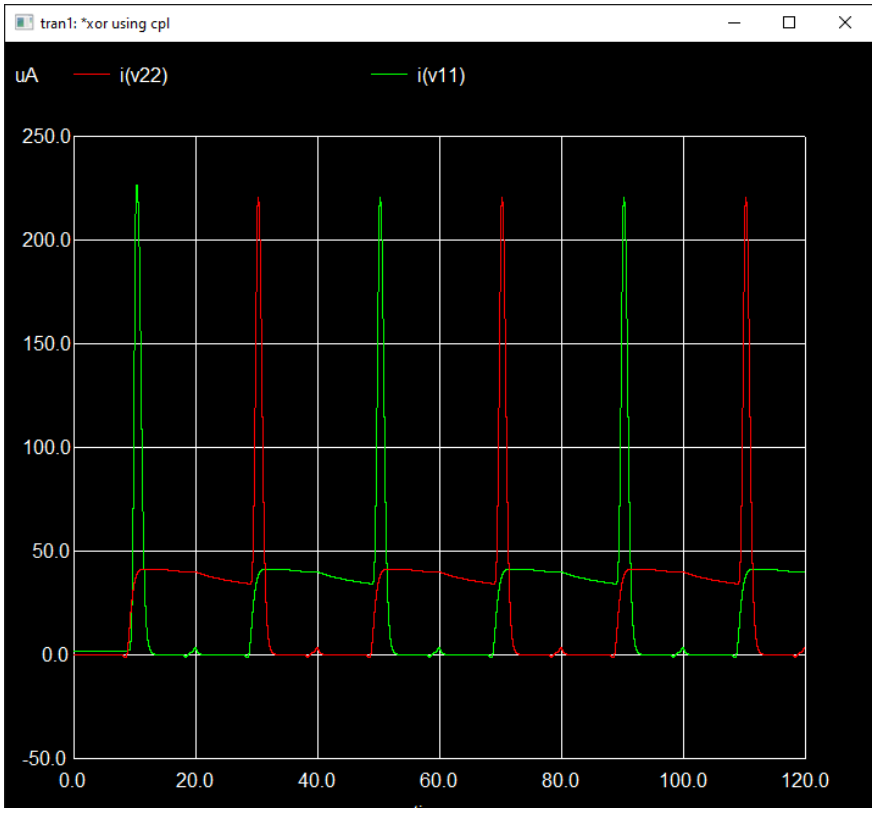


Figure 4.2: Implementation of XOR and XNOR by CPL logic.



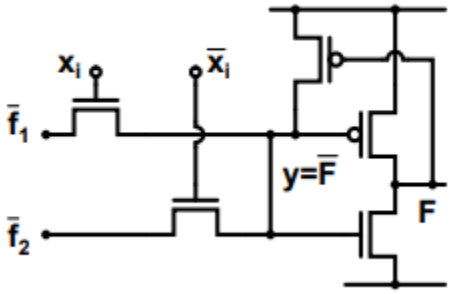


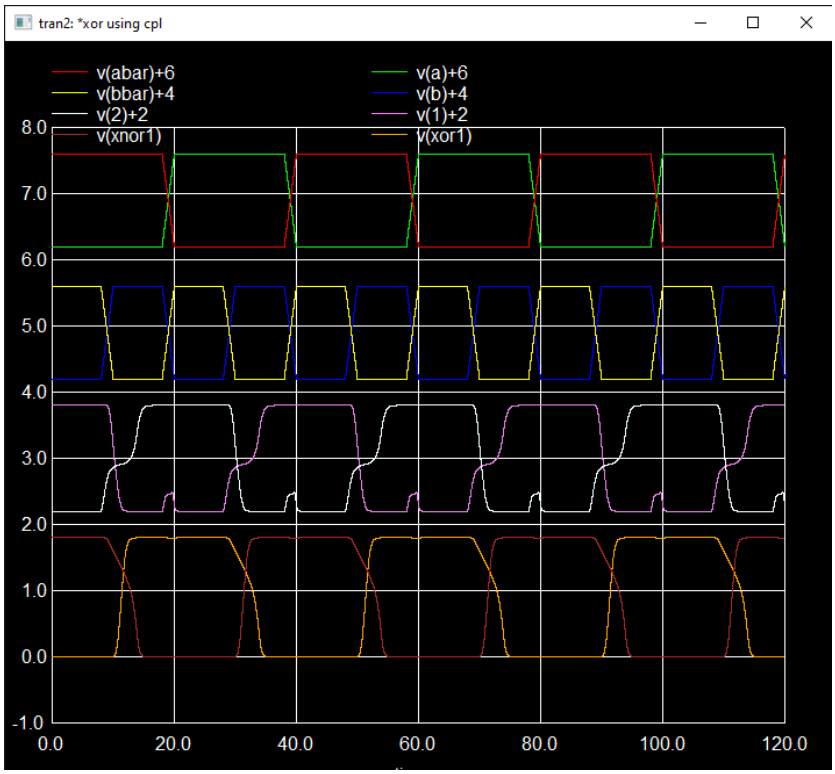

```
ngspice 36
v3#branch                               4.9389e-12
v2#branch                                        0
v1#branch                                        0


No. of Data Rows : 120077
idd_avg_xor          =  2.416183e-05 from=  0.000000e+00 to=  1.200000e-07
idd_avg_xnor         =  2.673651e-05 from=  0.000000e+00 to=  1.200000e-07
ngspice 3 ->
x0 = 8e-09, y0 = 2.21875

x0 = 6.85714e-09, y0 = 2.5    x1 = 1.10476e-08, y1 = 1.95313
dx = 4.19048e-09, dy = -0.546875
dy/dx = -1.30504e+08    dx/dy = -7.66259e-09

x0 = 9.52381e-09, y0 = 0

x0 = 9.52381e-09, y0 = 0.015625
```

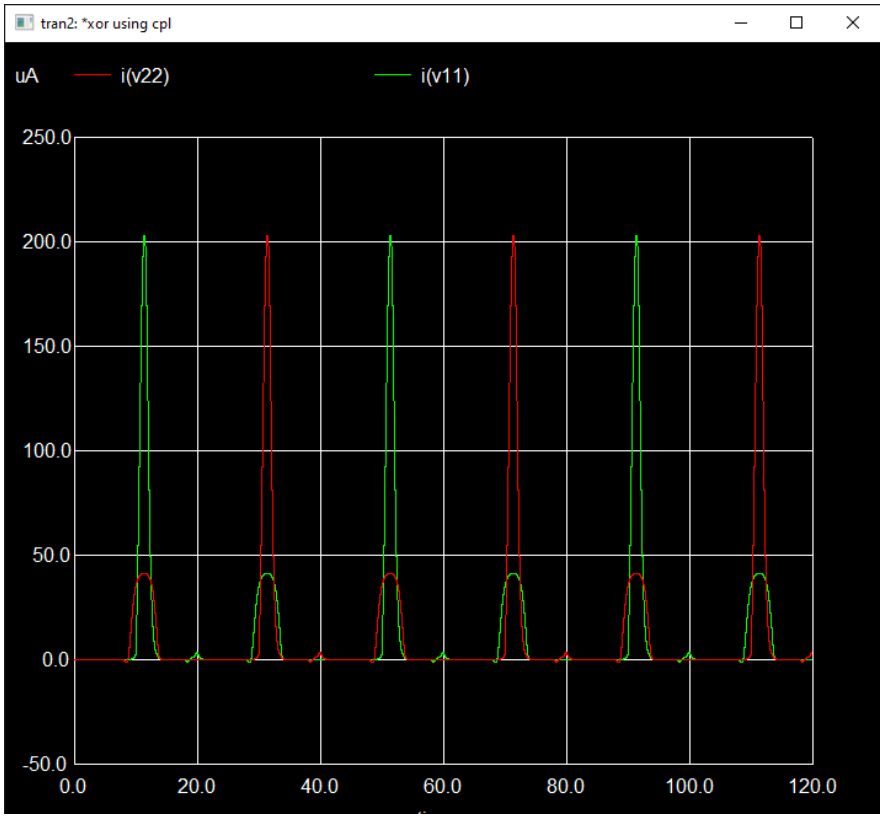
There is a small peak at the output based on the output of the switch matrix due to the transition and switching of the select line which determine the value of the output lines.Also the output of the matrix is not reaching Vdd.

There is a leakage current at the output which otherwise would be 0.

b)


x_i
$\bar{x}_i$
$\bar{f}_1$
$\bar{f}_2$
$y=\bar{F}$
F

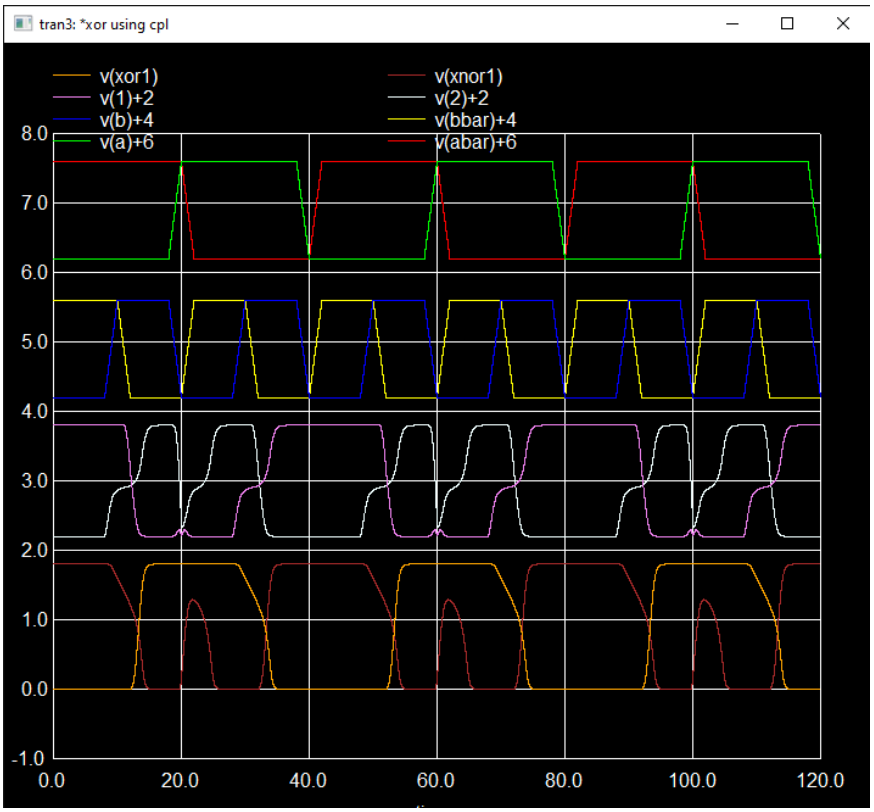

tran2: *xor using cpl
v(abar)+6
v(bbar)+4
v(2)+2
v(xnor1)
v(a)+6
v(b)+4
v(1)+2
v(xor1)
8.0
7.0
6.0
5.0
4.0
3.0
2.0
1.0
0.0
-1.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0



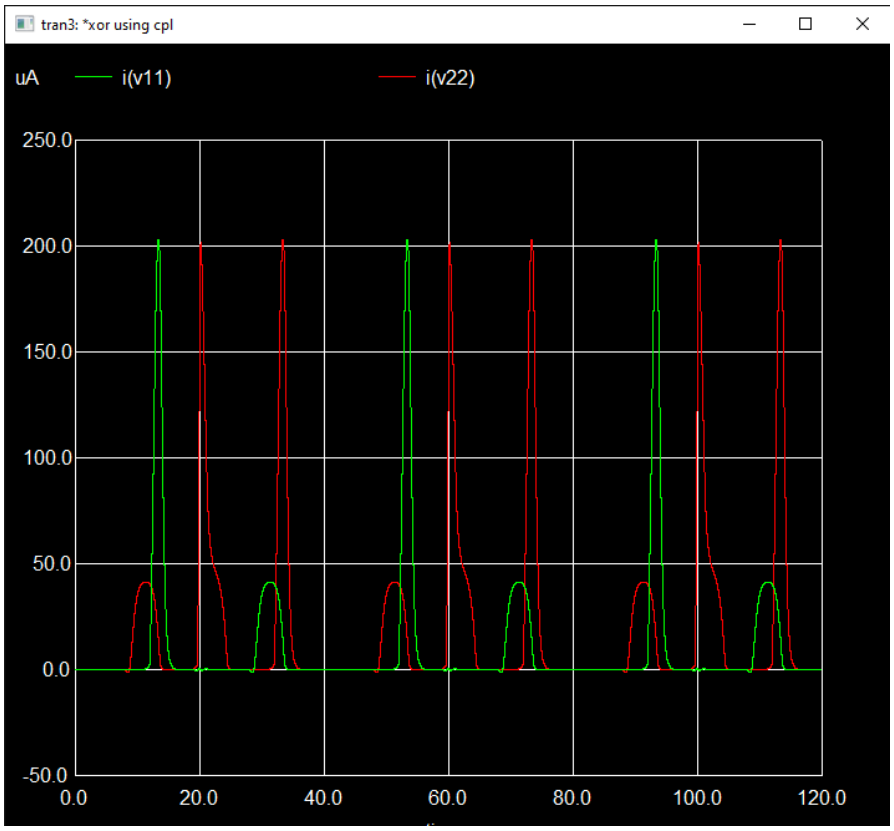
ngspice 36

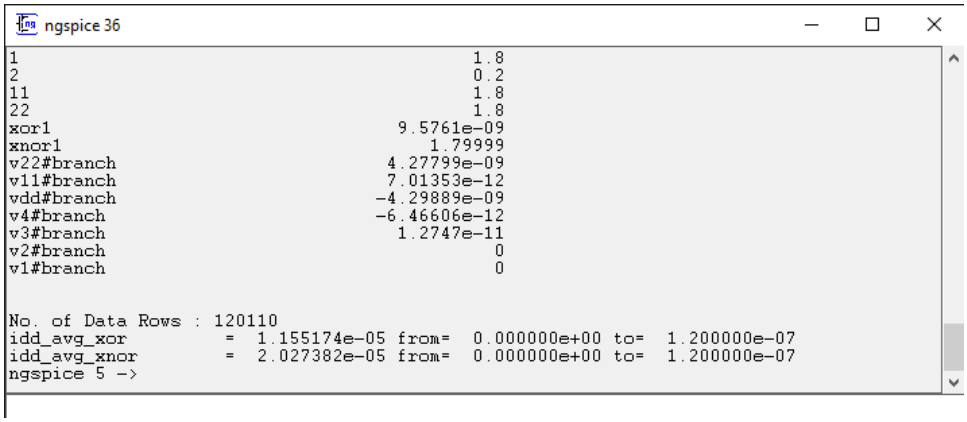
```
1                                   1.8
2                                   0.2
11                                  1.8
22                                  1.8
xor1                          9.5761e-09
xnor1                           1.79999
v22#branch                    4.27799e-09
v11#branch                    7.01353e-12
vdd#branch                   -4.29889e-09
v4#branch                    -6.46606e-12
v3#branch                     1.2747e-11
v2#branch                             0
v1#branch                             0


No. of Data Rows : 120077
idd_avg_xor          =  1.162138e-05 from=  0.000000e+00 to=  1.200000e-07
idd_avg_xnor         =  1.161179e-05 from=  0.000000e+00 to=  1.200000e-07
ngspice 4 ->
```

The output of the matrix is reaching Vdd and the delay is reduced.
The current now reaches 0 as the pmos of the inverter is getting turned off completely.


tran3: *xor using cpl
v(xor1)
v(1)+2
v(b)+4
v(a)+6
v(xnor1)
v(2)+2
v(bbar)+4
v(abar)+6
8.0
7.0
6.0
5.0
4.0
3.0
2.0
1.0
0.0
-1.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0

c)

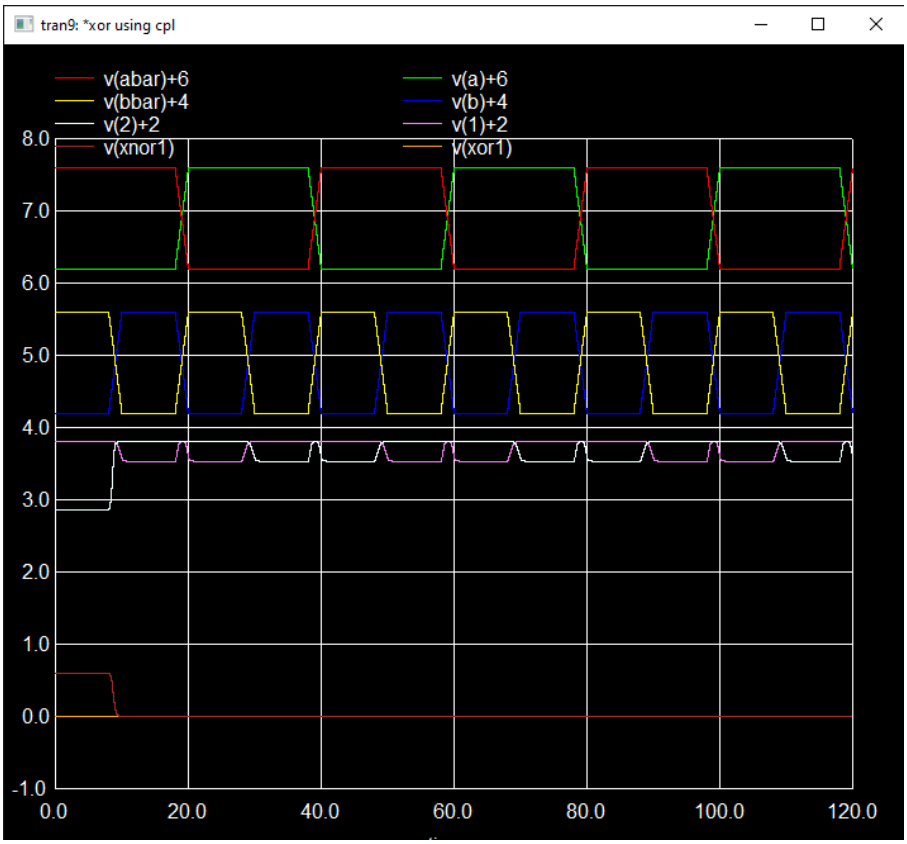

tran3: *xor using cpl
uA
i(v11)
i(v22)
250.0
200.0
150.0
100.0
50.0
0.0
-50.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0

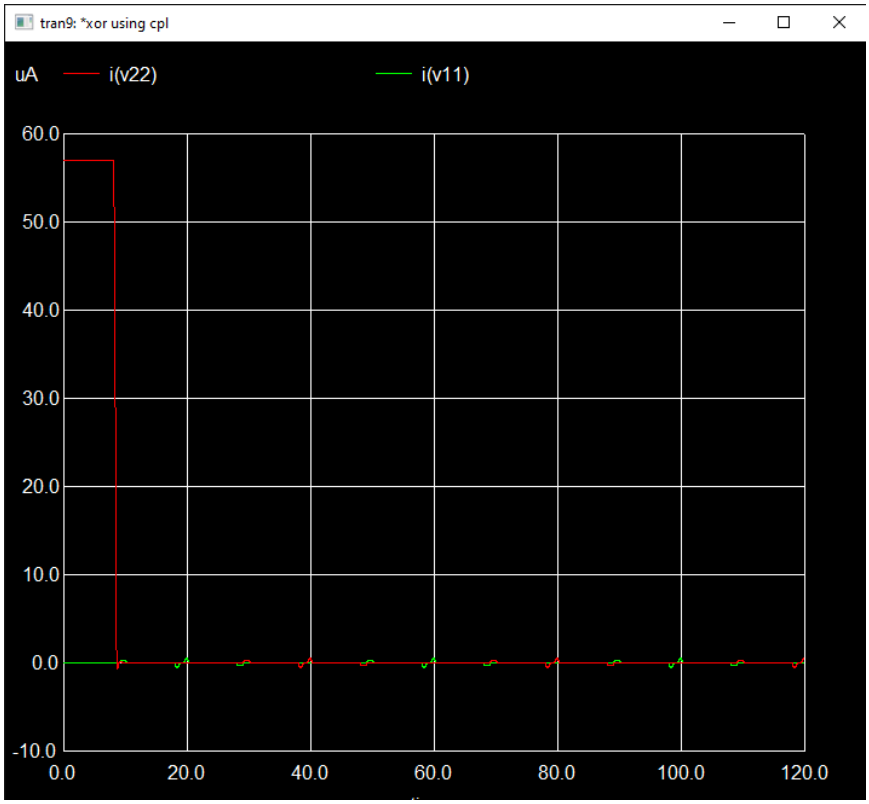


Due to the delay, the outputs are not complementary and one more state in the xnor region and there is a small peak whenever A:0->1 and B:1->0.

There are 2 peaks in the current waveform due to the small peak which results in a higher avergae current in xnor region.

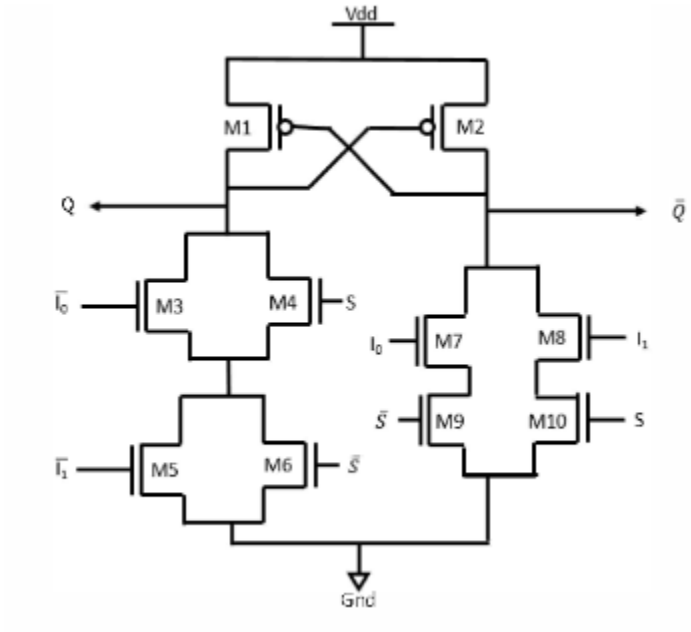
d)

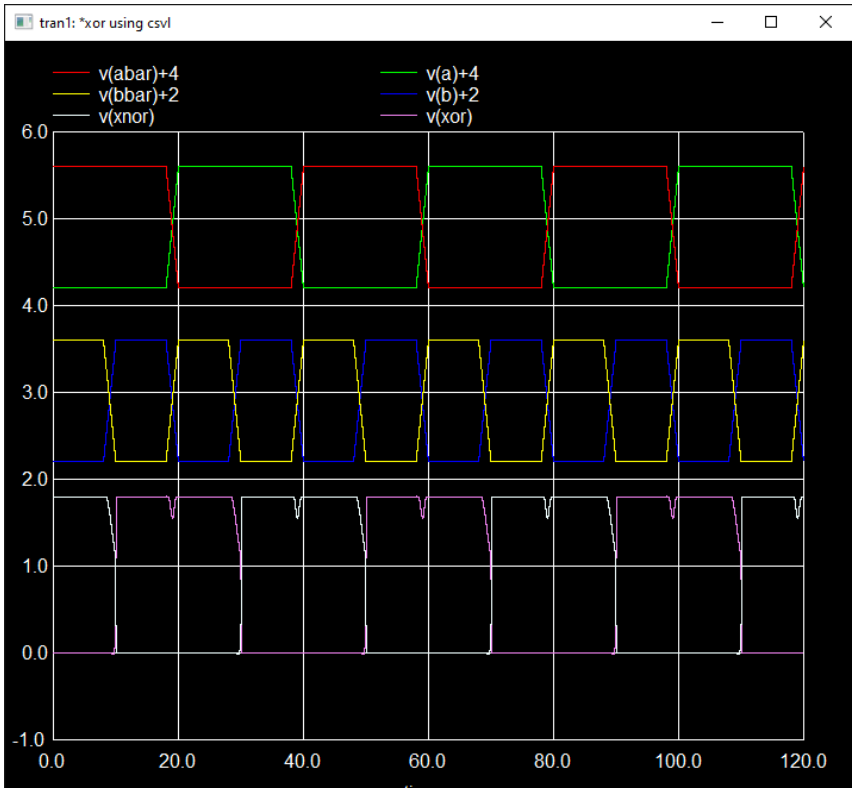




Pmos is stronger than nmos and it constitute a pseudo nMOS inverter. Nmos has to fight with pmos pull-up, so the output of the matrix can't go low.So output remains in that state only forever.

Question 2:





To accomodate series-parallel rule, width of the nmos is doubled. There is a small dip during transition but the time interval is small.