Assignment 4

Brent Kung Adder

Mohit , 20D070052

The circuit is shown in the below figure:

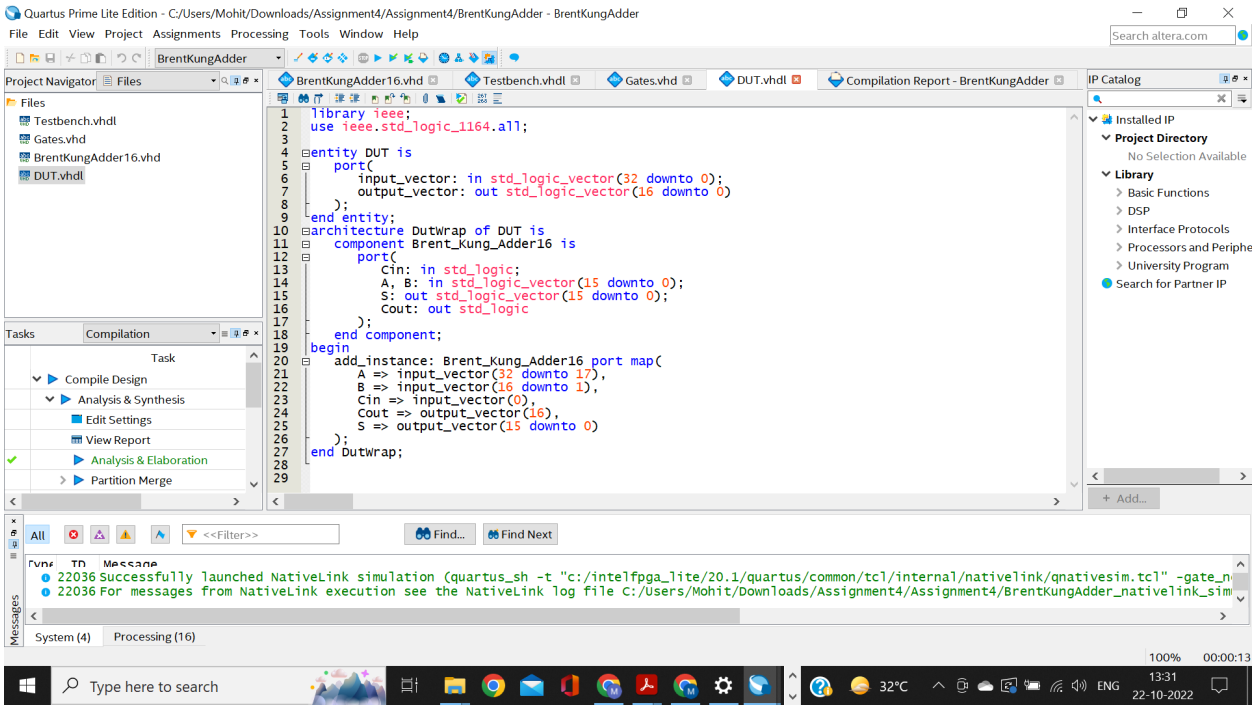
Elemental Logic Blocks :

Roll No. - 20D070052
Last Digit - 2
AND - 42ps
XOR - 54ps
A+B.C - 64ps
A.B + C.(A+B) - 64ps

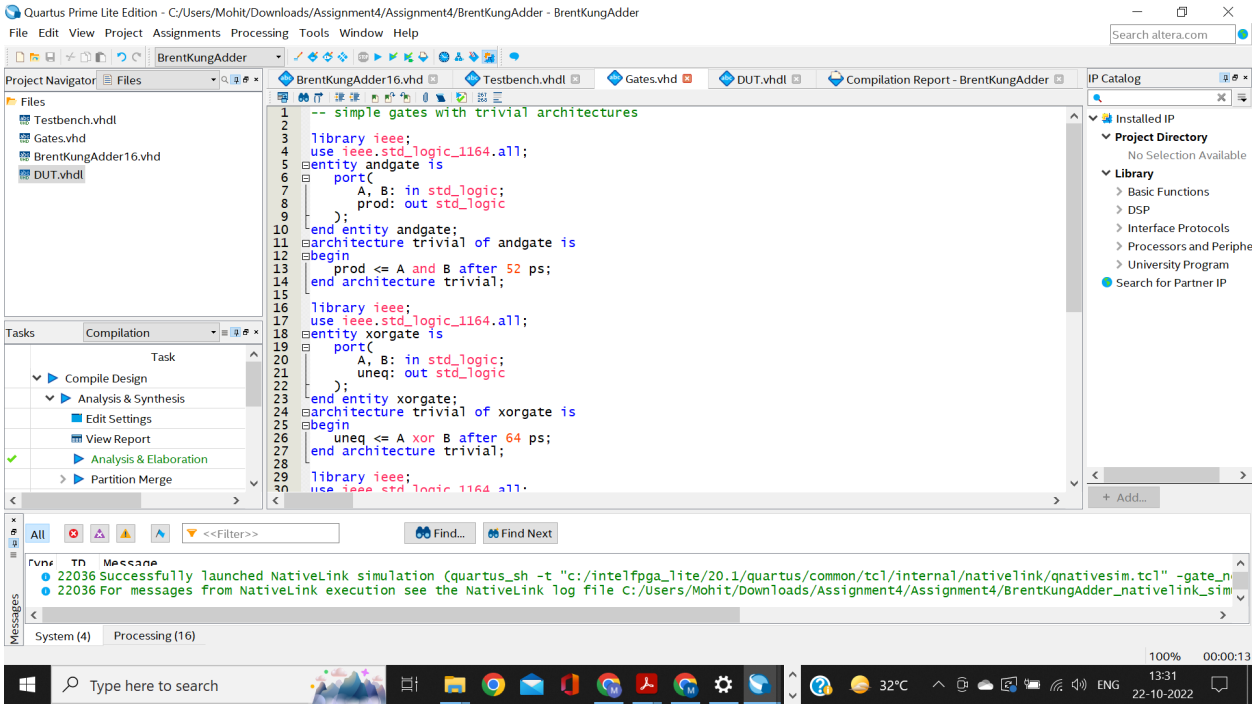
• We generate the various orders of G and P values using the logic blocks in the previous part
• We write the VHDL code that reads a pair of 16-bit numbers and single bit input carry, and generates the expected 16-bit sum and 1 bit output carry using a Brent Kung Adder
• The Brent Kung adder defined using VHDL, is simulated using ModelSim considering 32 randomly chosen pairs of 16-bit numbers and 1-bit input carry

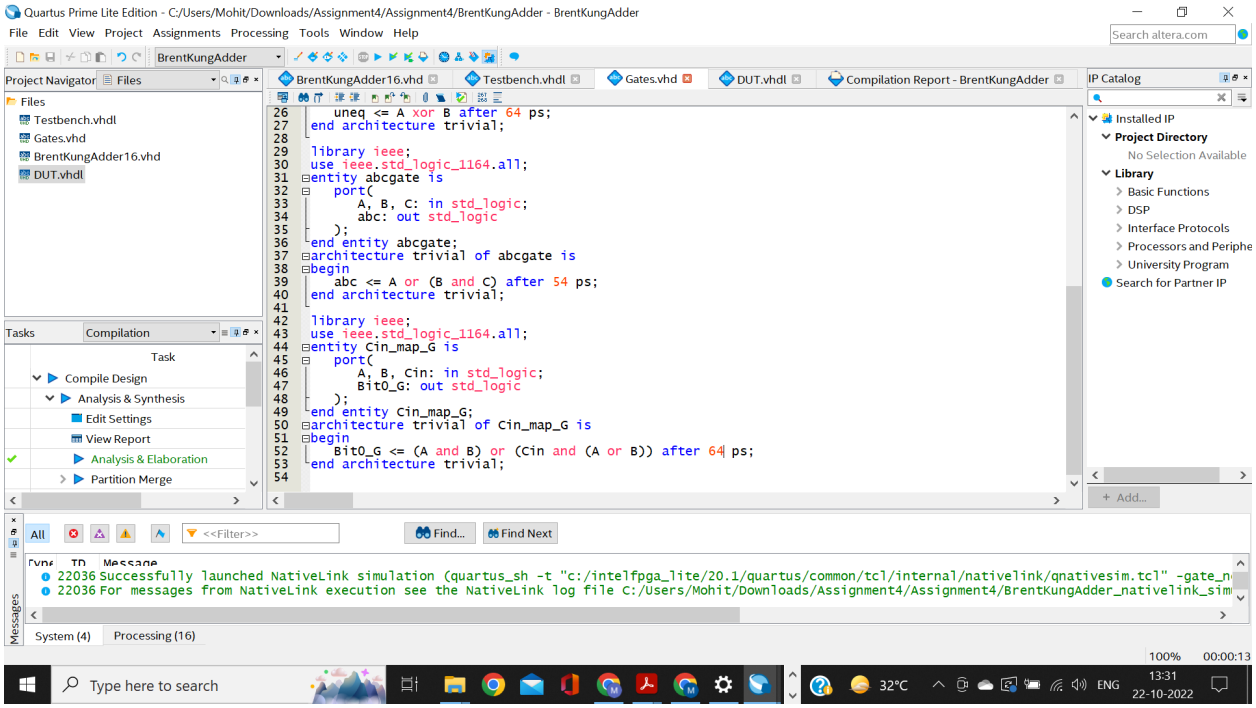
Code :

DUT FILE:

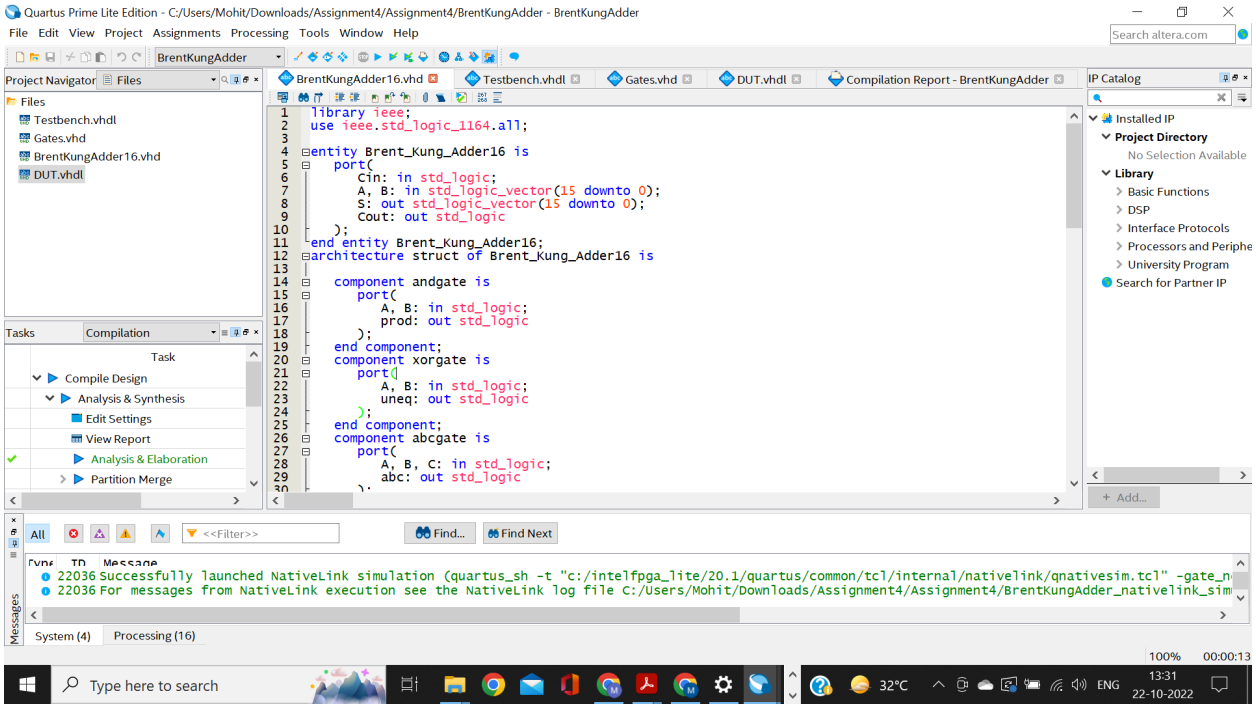


GATES INCLUDING AND , XOR ETC. :





FINAL ADDER :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BrentKungAdder
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BrentKungAdder16.vhd
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BrentKungAdder16.vhd Testbench.vhdl Gates.vhd DUT.vhdl Compilation Report - BrentKungAdder
1 library ieee;
2 use ieee.std_logic_1164.all;
3
4 entity Brent_Kung_Adder16 is
5 port(
6 Cin: in std_logic;
7 A, B: in std_logic_vector(15 downto 0);
8 S: out std_logic_vector(15 downto 0);
9 Cout: out std_logic
10);
11 end entity Brent_Kung_Adder16;
12 architecture struct of Brent_Kung_Adder16 is
13
14 component andgate is
15 port(
16 A, B: in std_logic;
17 prod: out std_logic
18);
19 end component;
20 component xorgate is
21 port(
22 A, B: in std_logic;
23 uneq: out std_logic
24);
25 end component;
26 component abcgate is
27 port(
28 A, B, C: in std_logic;
29 abc: out std_logic
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22036 Successfully launched NativeLink simulation (quartus_sh -t "c:/intelfpga_lite/20.1/quartus/common/tcl/internal/nativelink/qnativesim.tcl" -gate_n
22036 For messages from NativeLink execution see the NativeLink log file C:/Users/Mohit/Downloads/Assignment4/Assignment4/BrentKungAdder_nativelink_sim
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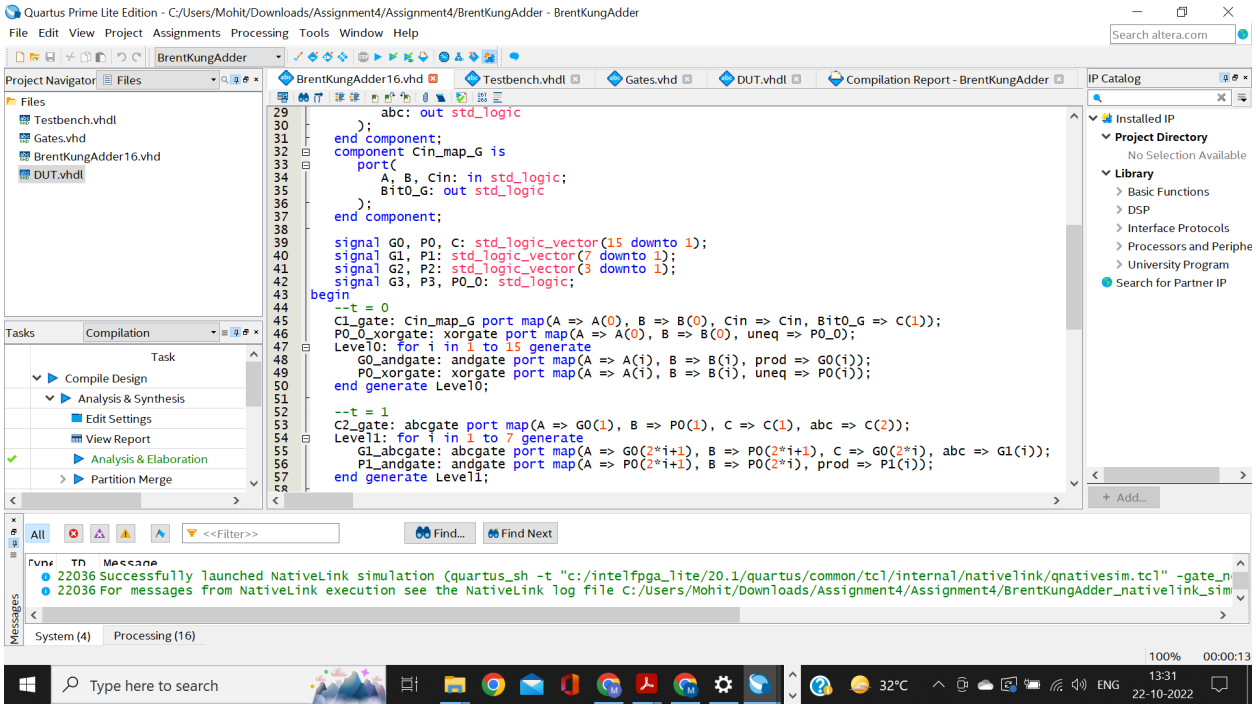
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BrentKungAdder16.vhd Testbench.vhdl Gates.vhd DUT.vhdl Compilation Report - BrentKungAdder
29 abc: out std_logic
30);
31 end component;
32 component Cin_map_G is
33 port(
34 A, B, Cin: in std_logic;
35 Bit0_G: out std_logic
36);
37 end component;
38
39 signal G0, P0, C: std_logic_vector(15 downto 1);
40 signal G1, P1: std_logic_vector(7 downto 1);
41 signal G2, P2: std_logic_vector(3 downto 1);
42 signal G3, P3, P0_0: std_logic;
43 begin
44 --t = 0
45 C1_gate: Cin_map_G port map(A => A(0), B => B(0), Cin => Cin, Bit0_G => C(1));
46 P0_0_xorgate: xorgate port map(A => A(0), B => B(0), uneq => P0_0);
47 Level0: for i in 1 to 15 generate
48 G0_andgate: andgate port map(A => A(i), B => B(i), prod => G0(i));
49 P0_xorgate: xorgate port map(A => A(i), B => B(i), uneq => P0(i));
50 end generate Level0;
51
52 --t = 1
53 C2_gate: abcgate port map(A => G0(1), B => P0(1), C => C(1), abc => C(2));
54 Level1: for i in 1 to 7 generate
55 G1_abcgate: abcgate port map(A => G0(2*i+1), B => P0(2*i+1), C => G0(2*i), abc => G1(i));
56 P1_andgate: andgate port map(A => P0(2*i+1), B => P0(2*i), prod => P1(i));
57 end generate Level1;
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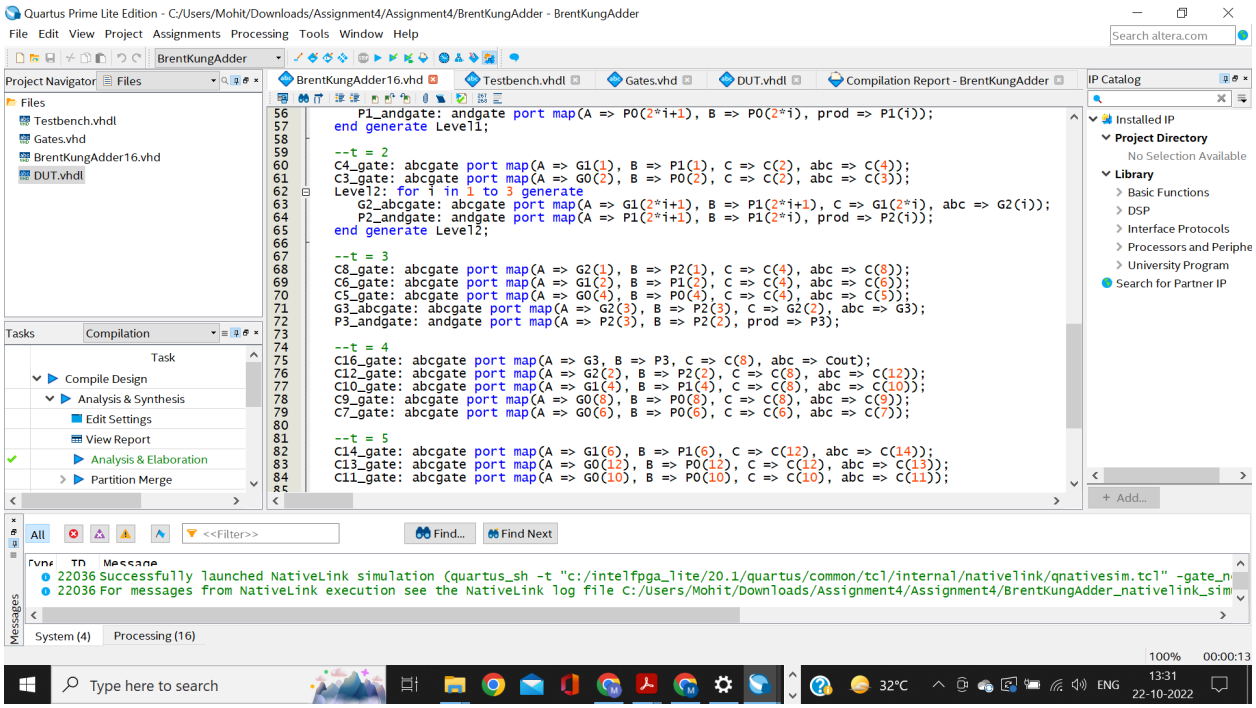
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Compilation Report - BrentKungAdder
P1_andgate: andgate port map(A => P0(2*i+1), B => P0(2*i), prod => P1(i));
end generate Level1;
--t = 2
C4_gate: abcgate port map(A => G1(1), B => P1(1), C => C(2), abc => C(4));
C3_gate: abcgate port map(A => G0(2), B => P0(2), C => C(2), abc => C(3));
Level2: for i in 1 to 3 generate
G2_abcgate: abcgate port map(A => G1(2*i+1), B => P1(2*i+1), C => G1(2*i), abc => G2(i));
P2_andgate: andgate port map(A => P1(2*i+1), B => P1(2*i), prod => P2(i));
end generate Level2;
--t = 3
C8_gate: abcgate port map(A => G2(1), B => P2(1), C => C(4), abc => C(8));
C6_gate: abcgate port map(A => G1(2), B => P1(2), C => C(4), abc => C(6));
C5_gate: abcgate port map(A => G0(4), B => P0(4), C => C(4), abc => C(5));
G3_abcgate: abcgate port map(A => G2(3), B => P2(3), C => G2(2), abc => G3);
P3_andgate: andgate port map(A => P2(3), B => P2(2), prod => P3);
--t = 4
C16_gate: abcgate port map(A => G3, B => P3, C => C(8), abc => Cout);
C12_gate: abcgate port map(A => G2(2), B => P2(2), C => C(8), abc => C(12));
C10_gate: abcgate port map(A => G1(4), B => P1(4), C => C(8), abc => C(10));
C9_gate: abcgate port map(A => G0(8), B => P0(8), C => C(8), abc => C(9));
C7_gate: abcgate port map(A => G0(6), B => P0(6), C => C(6), abc => C(7));
--t = 5
C14_gate: abcgate port map(A => G1(6), B => P1(6), C => C(12), abc => C(14));
C13_gate: abcgate port map(A => G0(12), B => P0(12), C => C(12), abc => C(13));
C11_gate: abcgate port map(A => G0(10), B => P0(10), C => C(10), abc => C(11));
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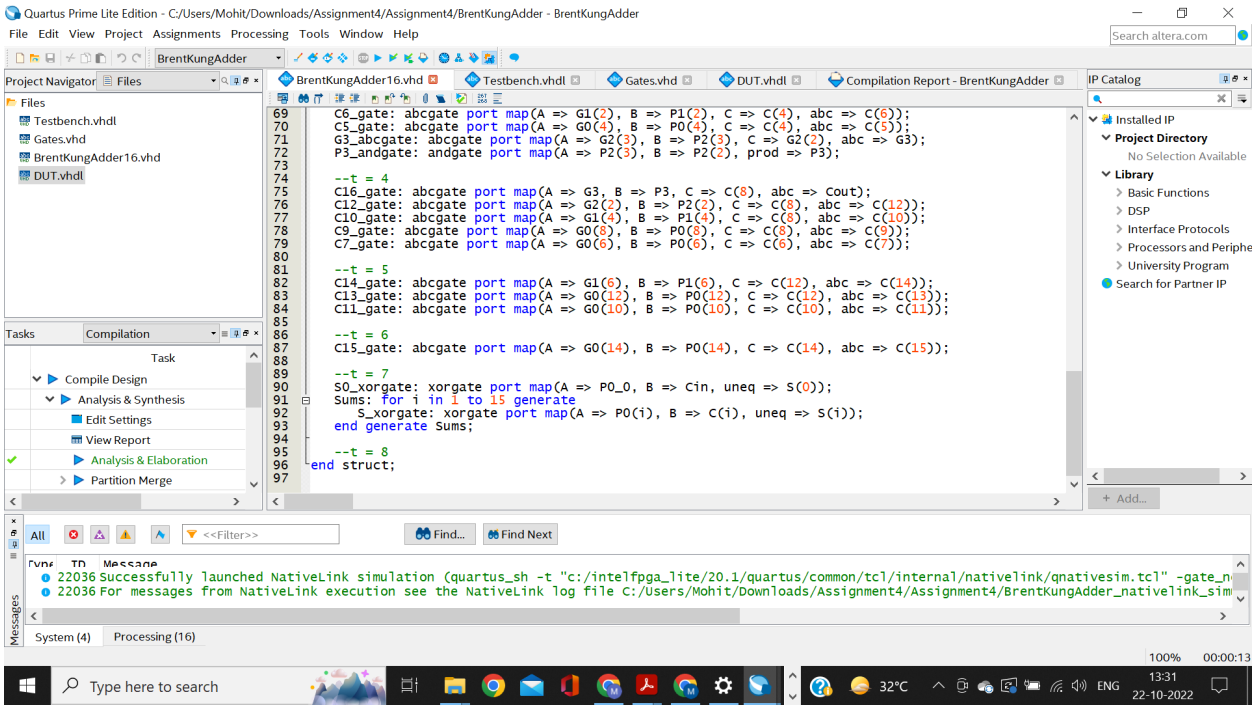
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C6_gate: abcgate port map(A => G1(2), B => P1(2), C => C(4), abc => C(6));
C5_gate: abcgate port map(A => G0(4), B => P0(4), C => C(4), abc => C(5));
G3_abcgate: abcgate port map(A => G2(3), B => P2(3), C => G2(2), abc => G3);
P3_andgate: andgate port map(A => P2(3), B => P2(2), prod => P3);
--t = 4
C16_gate: abcgate port map(A => G3, B => P3, C => C(8), abc => Cout);
C12_gate: abcgate port map(A => G2(2), B => P2(2), C => C(8), abc => C(12));
C10_gate: abcgate port map(A => G1(4), B => P1(4), C => C(8), abc => C(10));
C9_gate: abcgate port map(A => G0(8), B => P0(8), C => C(8), abc => C(9));
C7_gate: abcgate port map(A => G0(6), B => P0(6), C => C(6), abc => C(7));
--t = 5
C14_gate: abcgate port map(A => G1(6), B => P1(6), C => C(12), abc => C(14));
C13_gate: abcgate port map(A => G0(12), B => P0(12), C => C(12), abc => C(13));
C11_gate: abcgate port map(A => G0(10), B => P0(10), C => C(10), abc => C(11));
--t = 6
C15_gate: abcgate port map(A => G0(14), B => P0(14), C => C(14), abc => C(15));
--t = 7
S0_xorgate: xorgate port map(A => P0_0, B => Cin, uneq => S(0));
Sums: for i in 1 to 15 generate
S_xorgate: xorgate port map(A => P0(i), B => C(i), uneq => S(i));
end generate Sums;
--t = 8
end struct;
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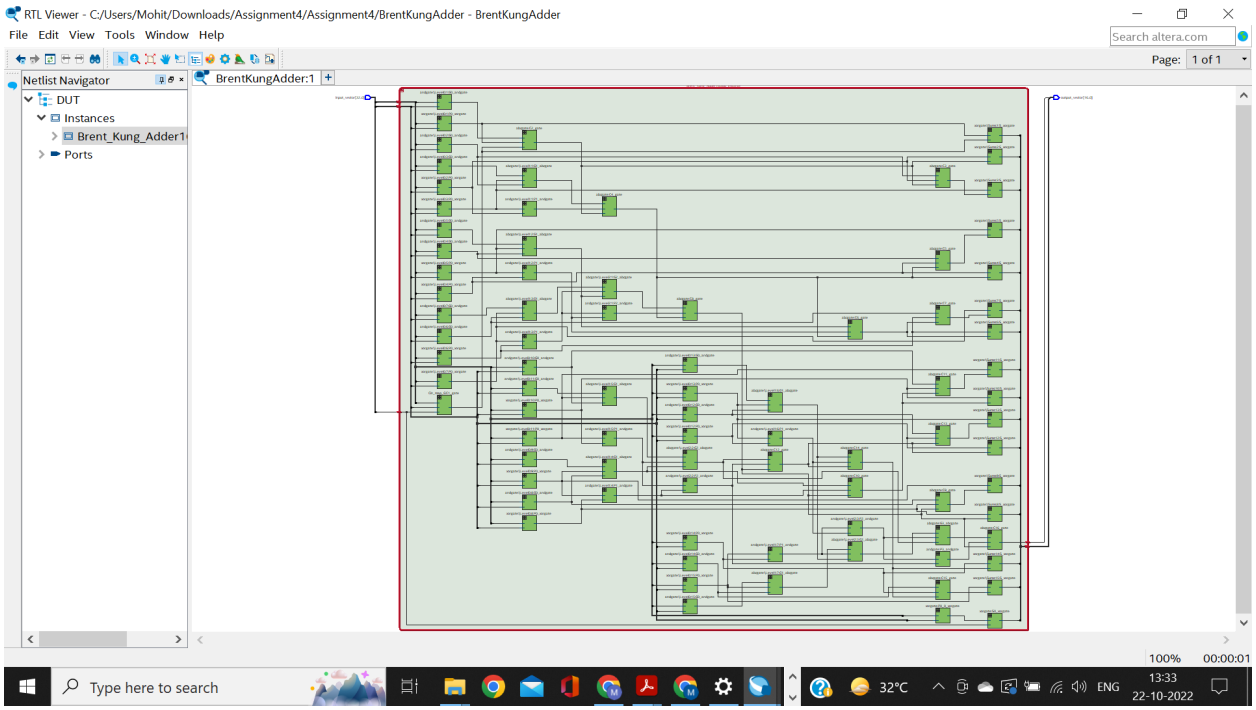
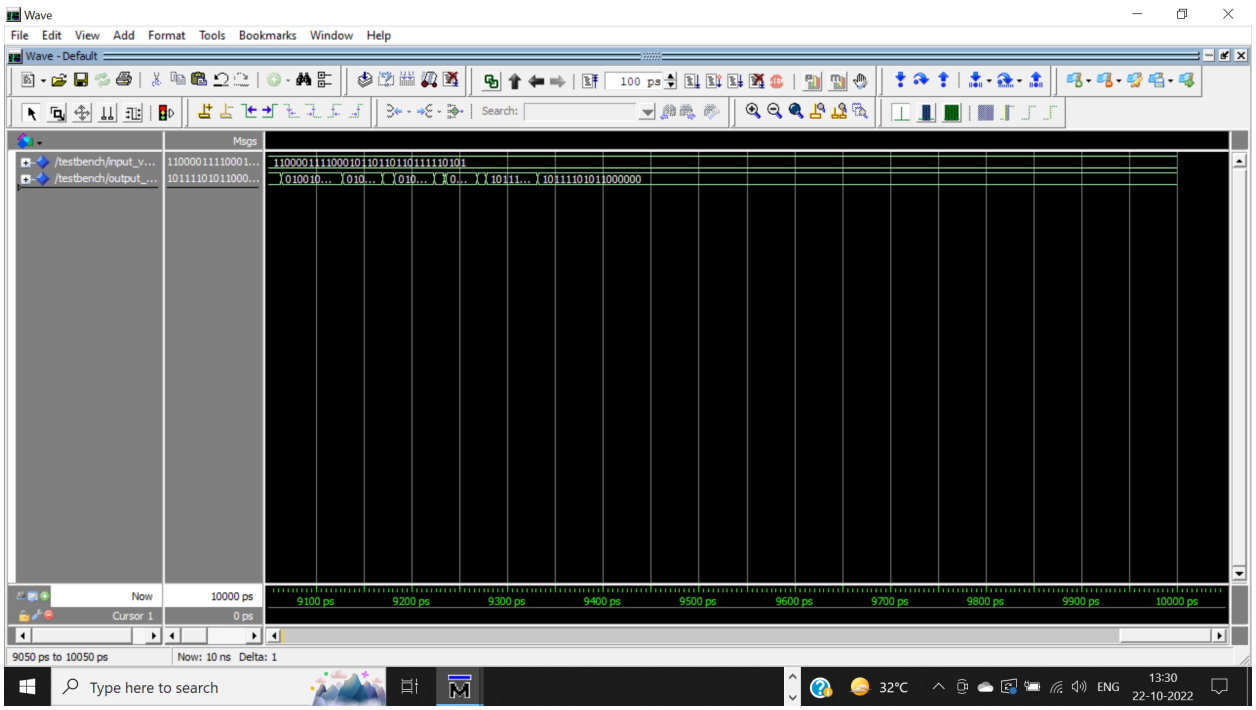
RTL VIEW OF THE CIRCUIT :



RTL SIMULATION RESULT :



GATE LEVEL SIMULATION RESULT :