EE671: VLSI Design
Assignment 4

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Abstract

Your abstract.

1 Elemental Logic Blocks

Roll No. - 20D170037
Last Digit - 7
AND - 47ps
XOR - 64ps
A+B.C - 74ps
A.B + C.(A+B) - 74ps

1.1 RTL Views:

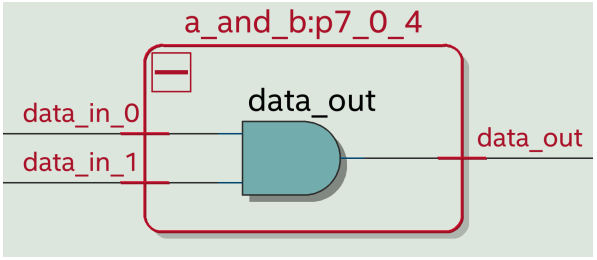


Figure 1: AND Logic Function

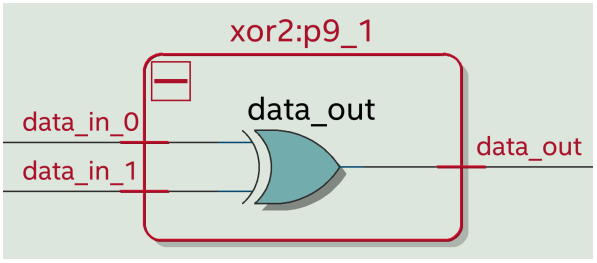


Figure 2: XOR Logic Function

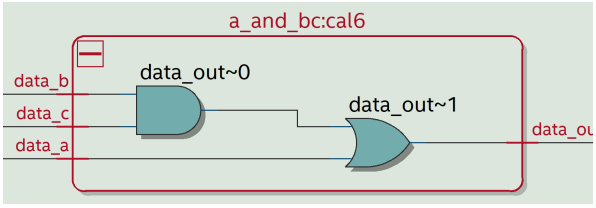


Figure 3: A + B.C Logic Function

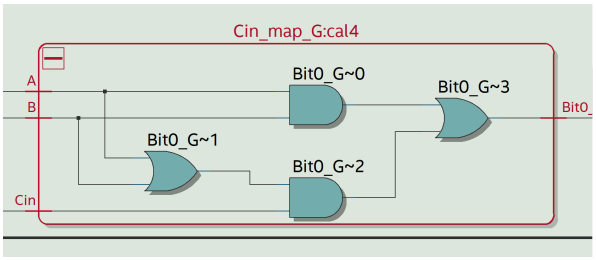


Figure 4: A.B + C.(A+B) Logic Function

2 Further Procedure

- We generate the various orders of G and P values using the logic blocks in the previous part
- We write the VHDL code that reads a pair of 16-bit numbers and single bit input carry, and generates the expected 16-bit sum and 1 bit output carry using a Brent Kung Adder
- The Brent Kung adder defined using VHDL, is simulated using ModelSim considering 32 randomly chosen pairs of 16-bit numbers and 1-bit input carry

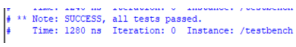
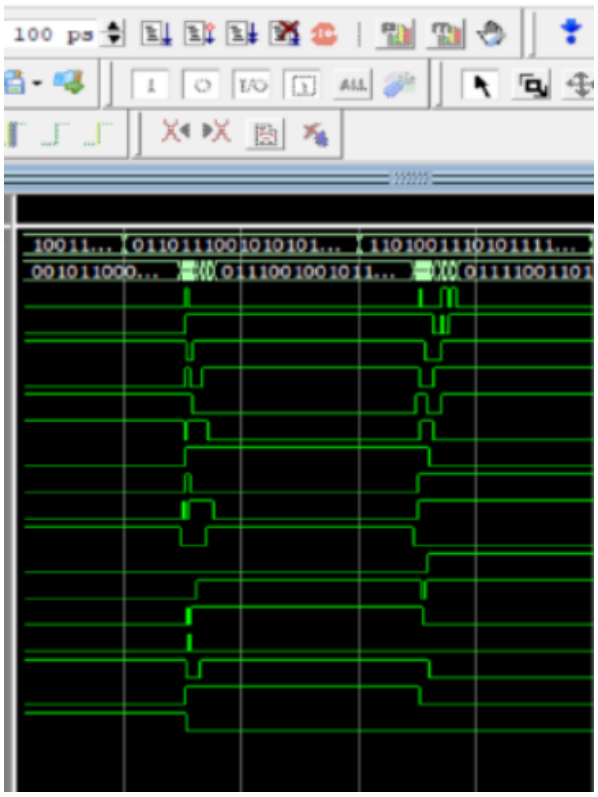


Figure 5: ModelSim window after performing simulation

3 Output Waveform



VHDL CODE FOR ALL IS PROVIDED ALONG WITH THE SUBMISSION